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(54) METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

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Related U.S. Application Data

(63) Continuation of application No. 09/276,969, filed on Mar. 26, 1999, now Pat. No. 6,204,184.

(30) **Foreign Application Priority Data**

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(52) **U.S. Cl.** **438/612**; 438/690; 438/691; 438/692

(57) ABSTRACT

In a method of manufacturing a semiconductor device having a memory mat portion in which an active region and a field region are formed densely, after a polishing stopper film is deposited on a semiconductor substrate, there are formed grooves by etching a polishing stopper film of a field region and the semiconductor substrate. Then, after an insulating film is deposited so as to fill the grooves, then insulating film is partly removed from the memory mat portion by etching. Under this state, the insulating film is chemically mechanically polished until the polishing stopper film is exposed. The film thickness of the polishing stopper film on the active region can be reduced, and an electrical element isolation characteristic of the field region can be improved. At the same time, upon chemical mechanical polishing, a silicon substrate can be prevented from being exposed at the central portion of the memory mat portion and the insulating film can be prevented from being left on the silicon nitride film near the outer periphery, thereby making it possible to form elements having uniform electrical characteristics on all active regions of the memory mat portion.

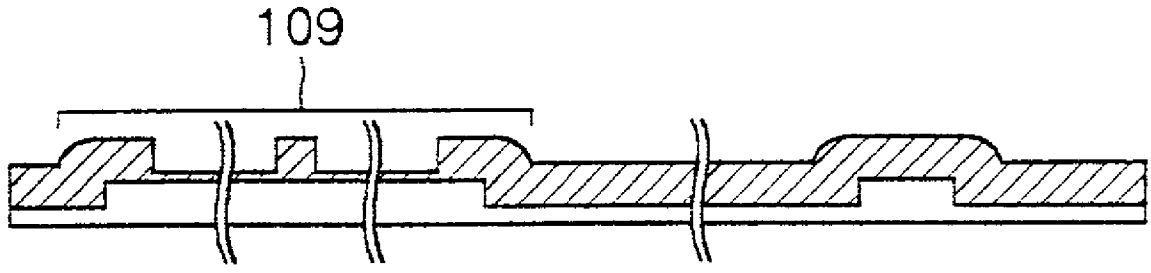


FIG.1a

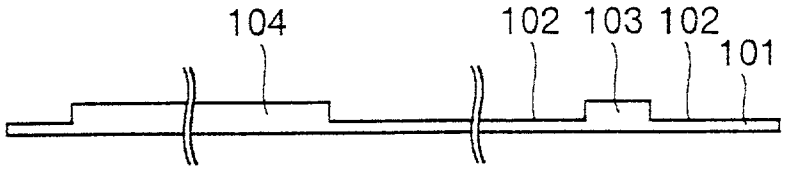


FIG.1b

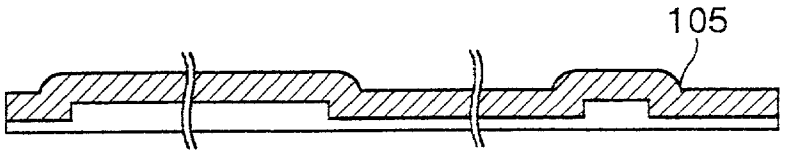


FIG.1c

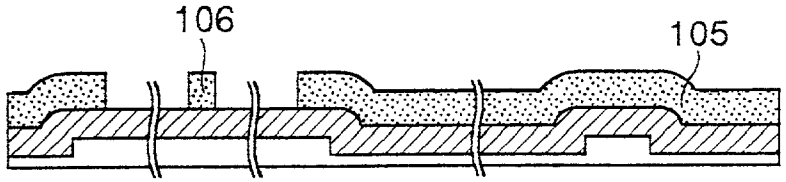


FIG.1d

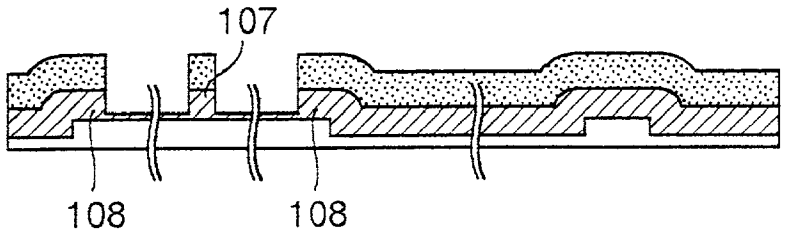


FIG.1e

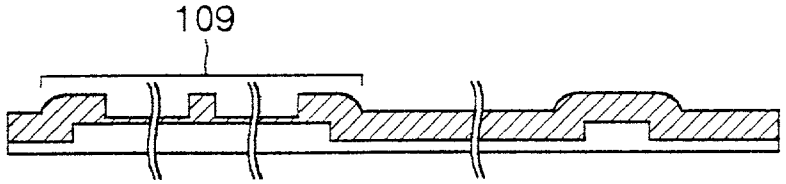


FIG.1f

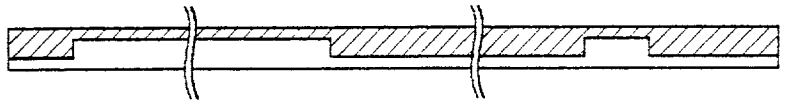


FIG.2a

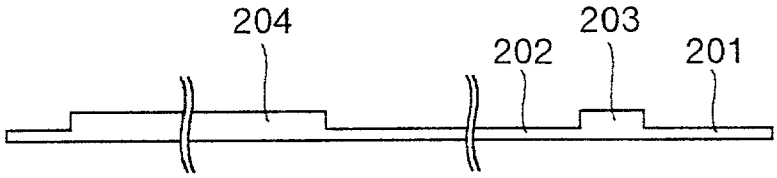


FIG.2b

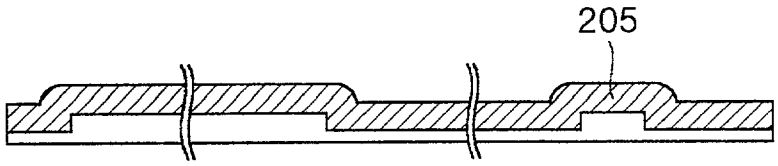


FIG.2c

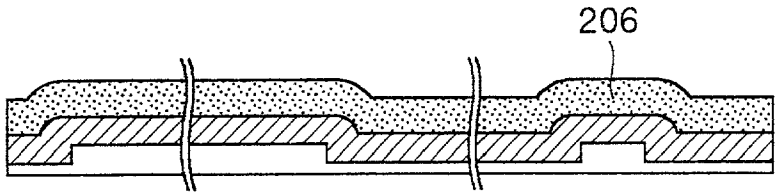


FIG.2d

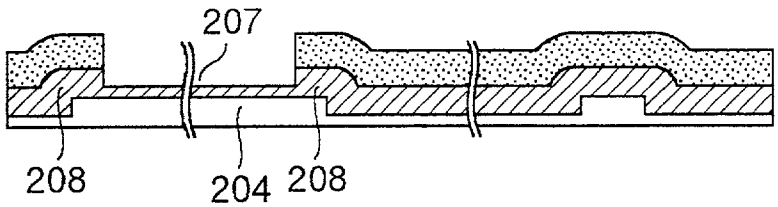


FIG.2e

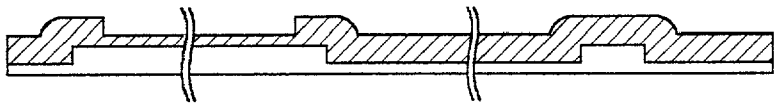


FIG.2f

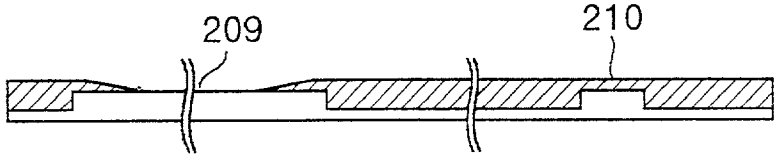


FIG.3a

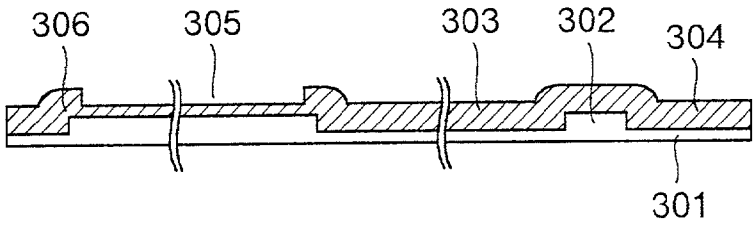


FIG.3b

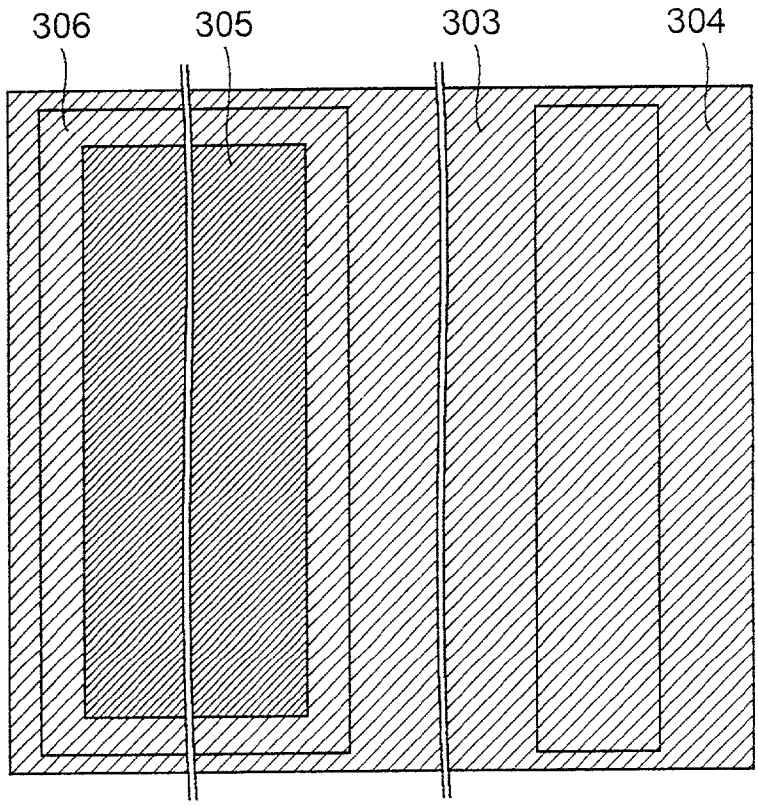


FIG.3c

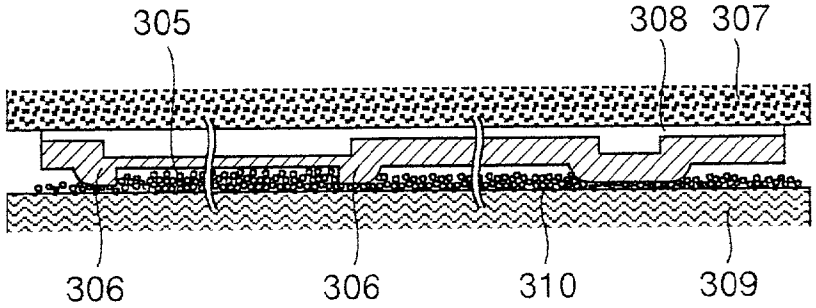


FIG.4a

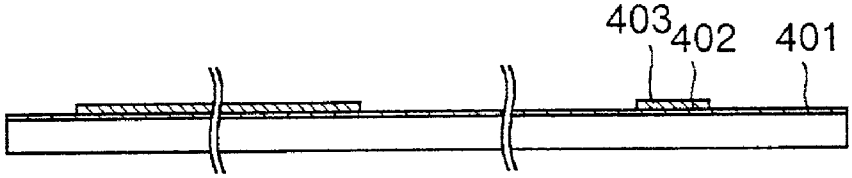


FIG.4b

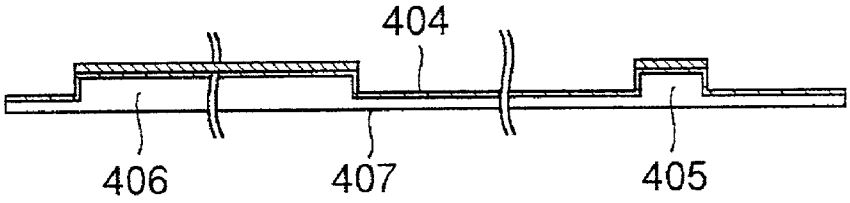


FIG.4c

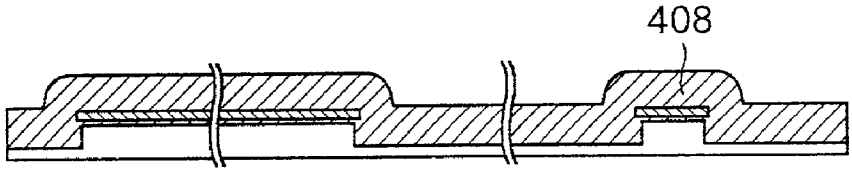


FIG.4d

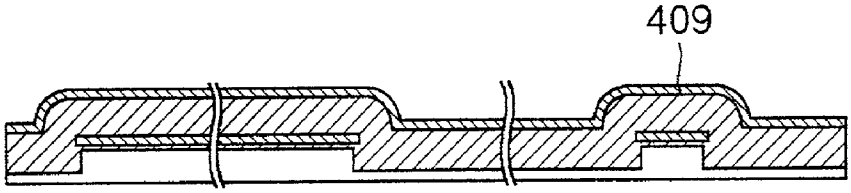


FIG.4e

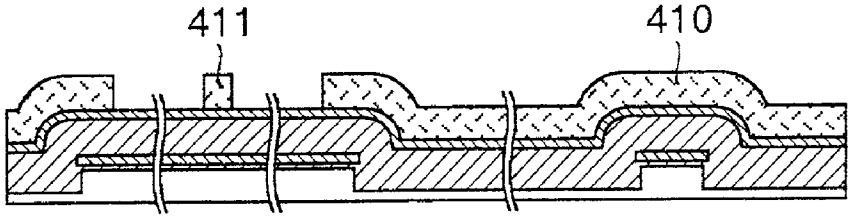


FIG.5a

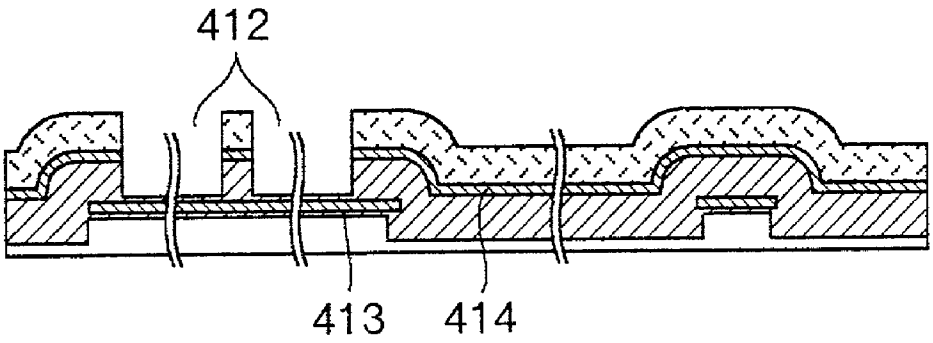


FIG.5b

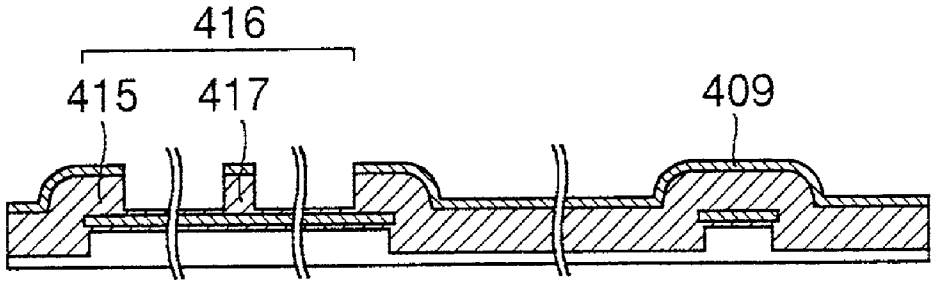


FIG.5c

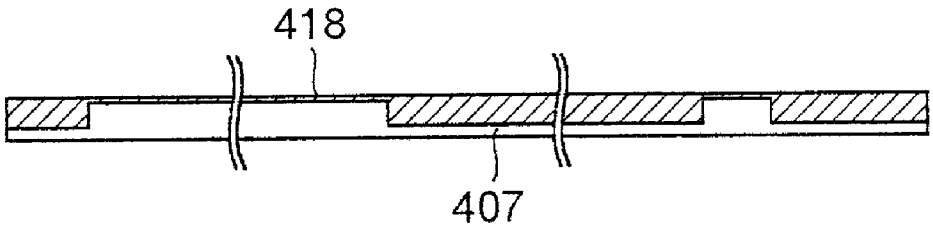


FIG.5d

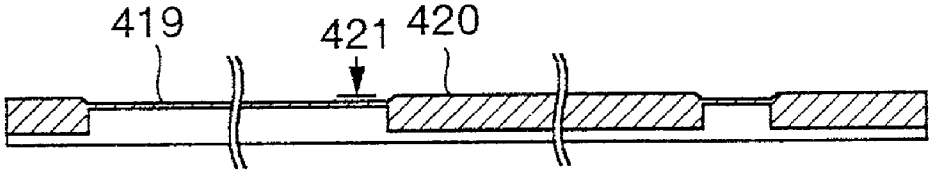


FIG.6a

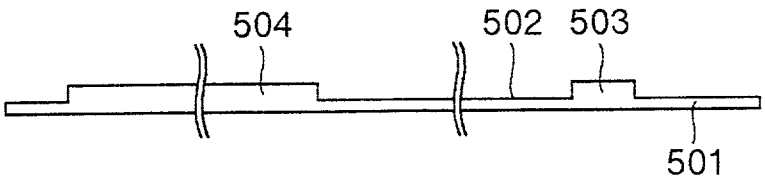


FIG.6b

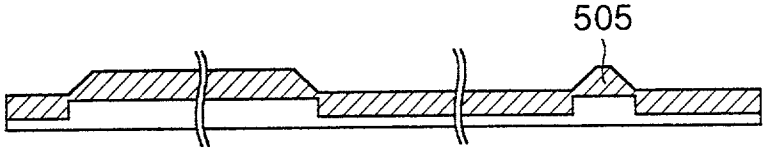


FIG.6c

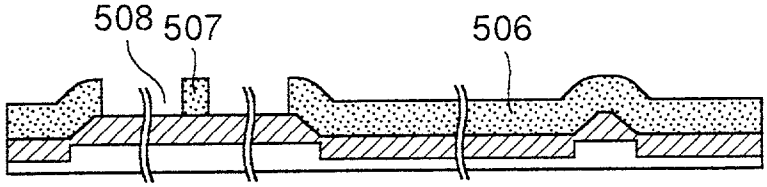


FIG.6d

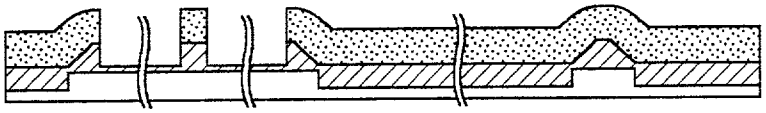


FIG.6e

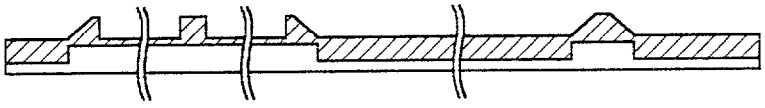


FIG.6f

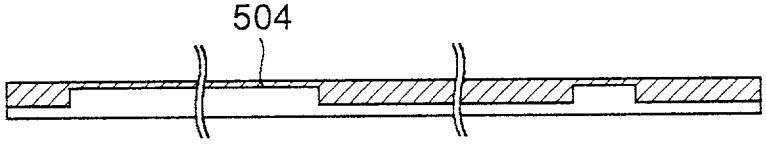


FIG.7a

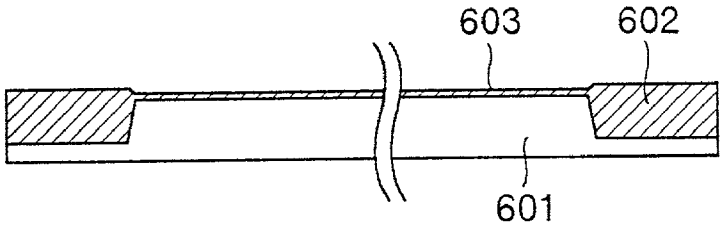


FIG.7b

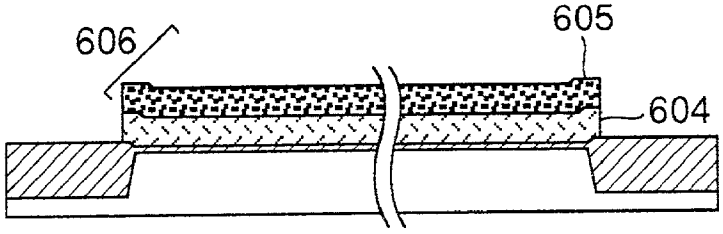


FIG.7c

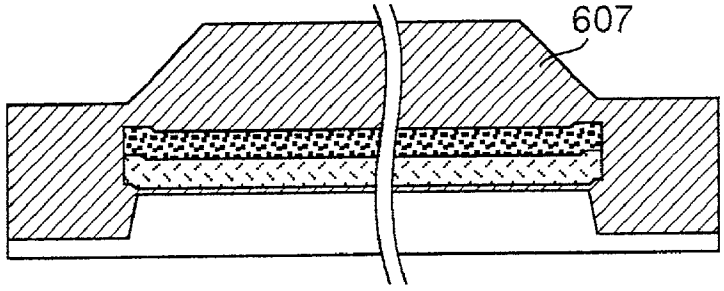


FIG.7d

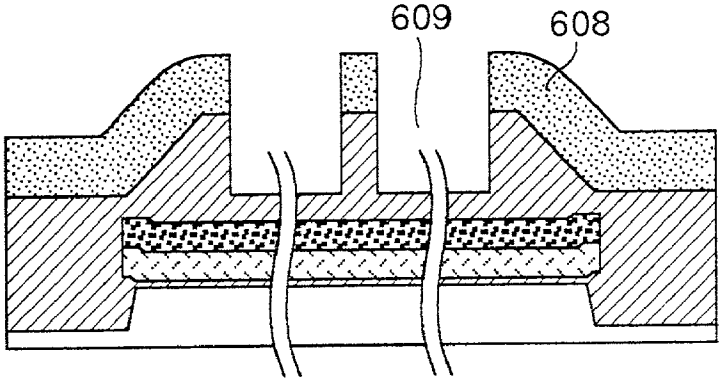


FIG.8a

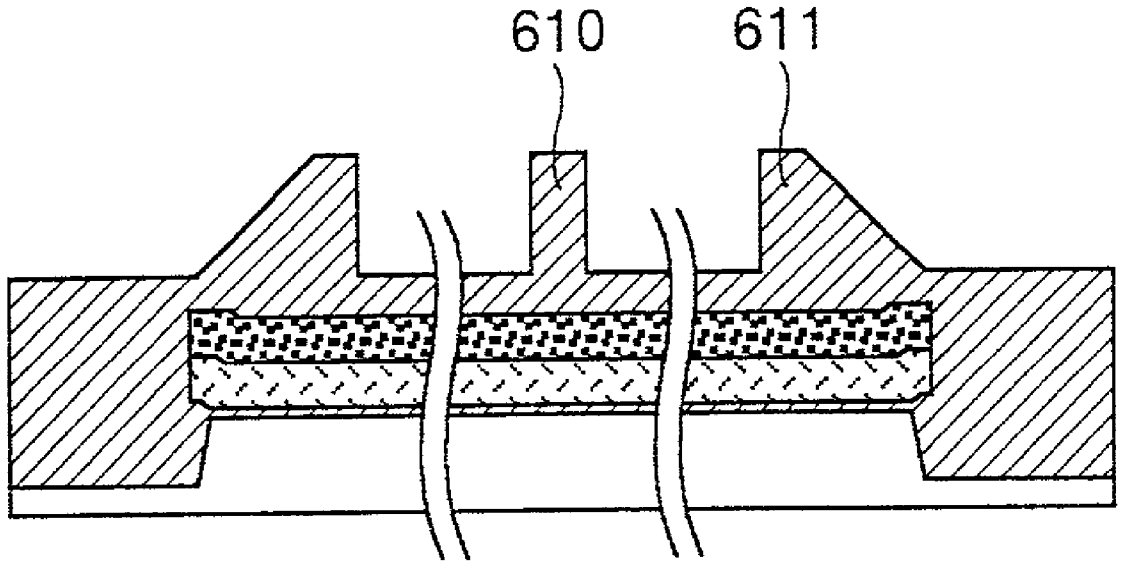


FIG.8b

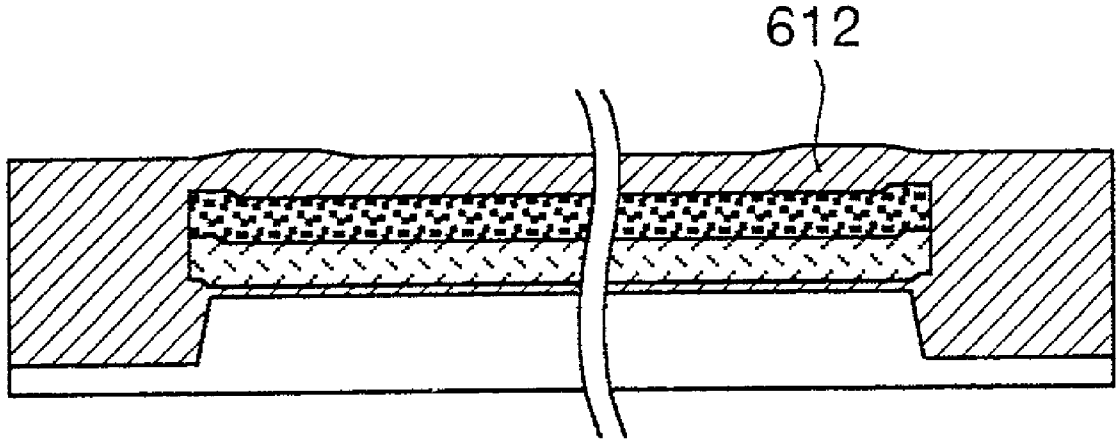


FIG.9a

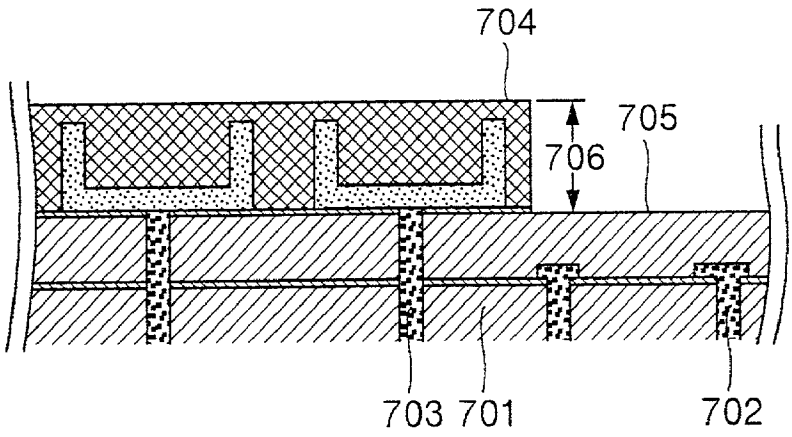


FIG.9b

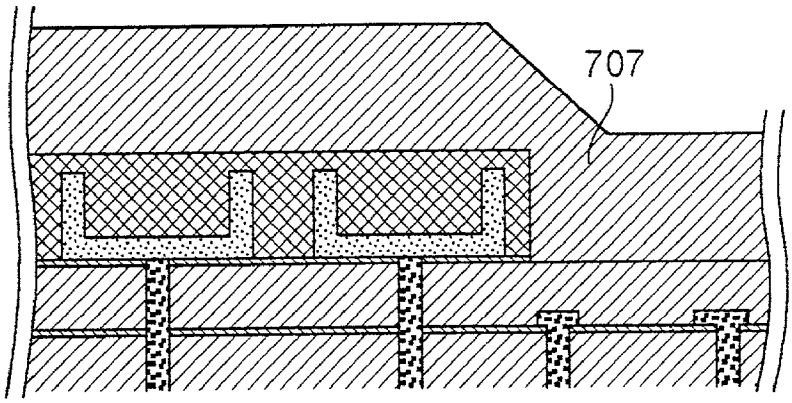


FIG.9c

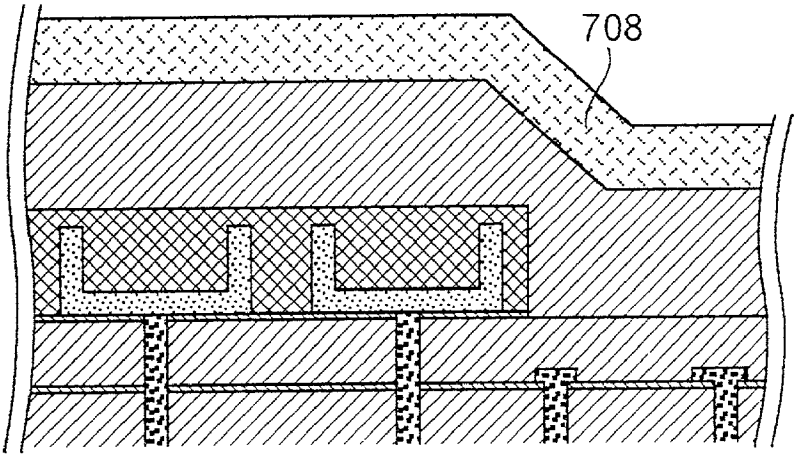


FIG.10a

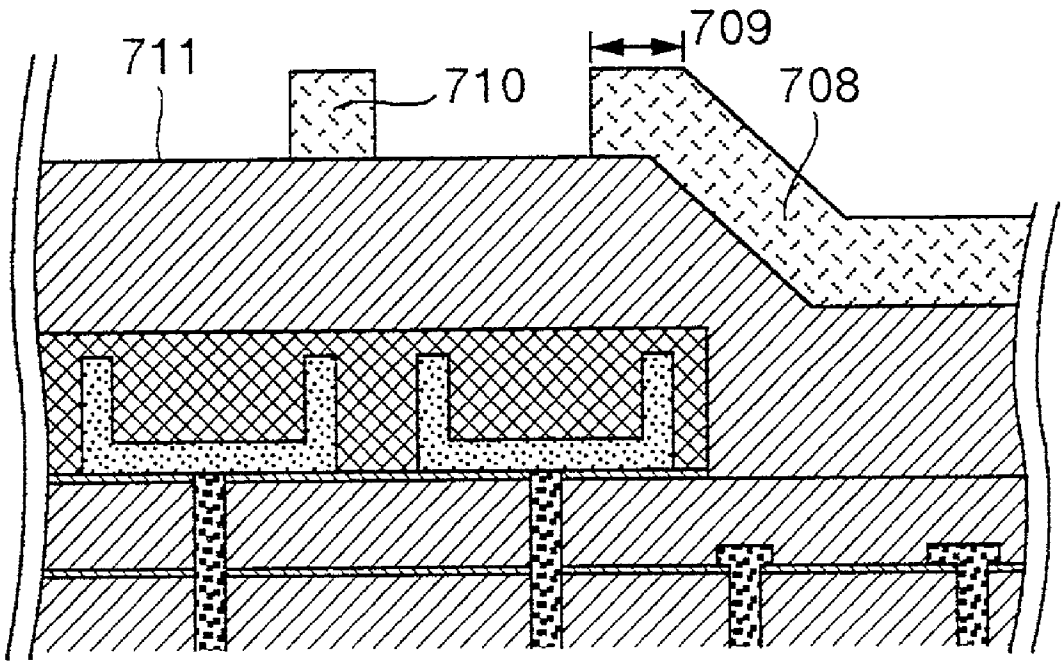


FIG.10b

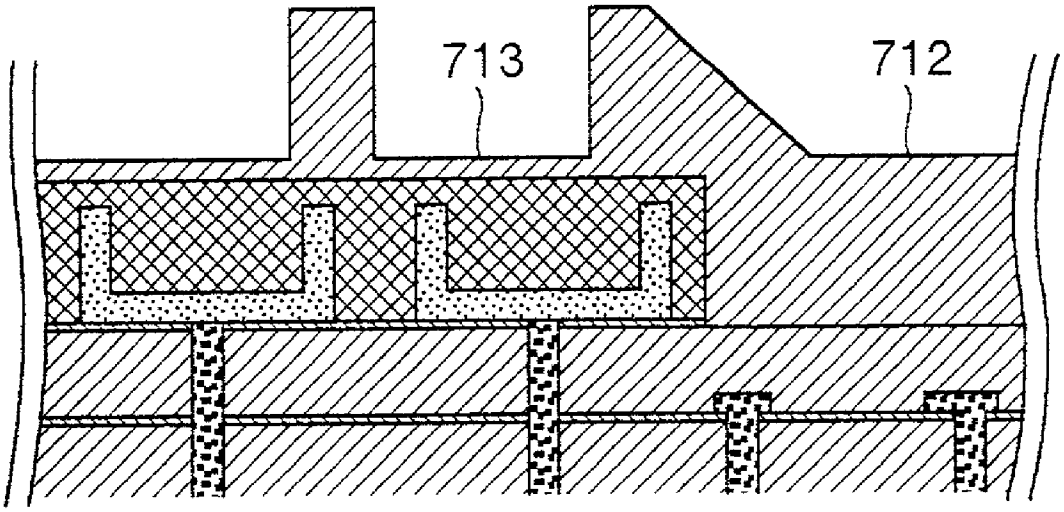


FIG.11a

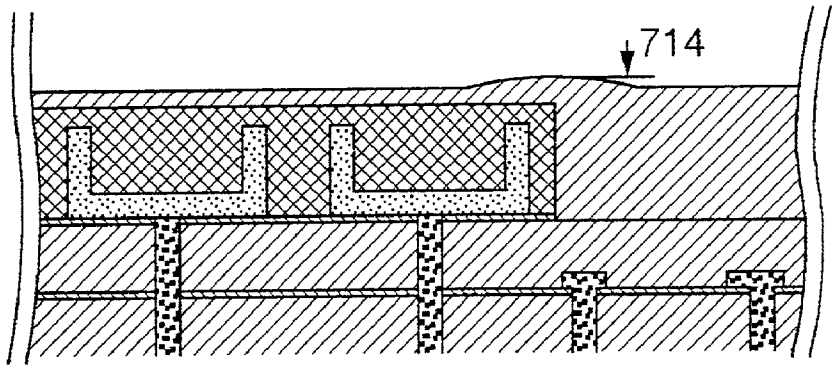


FIG.11b

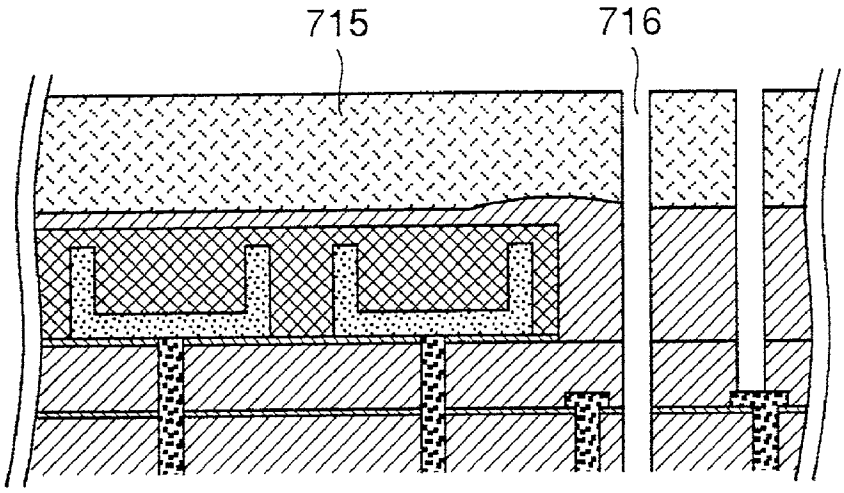


FIG.11c

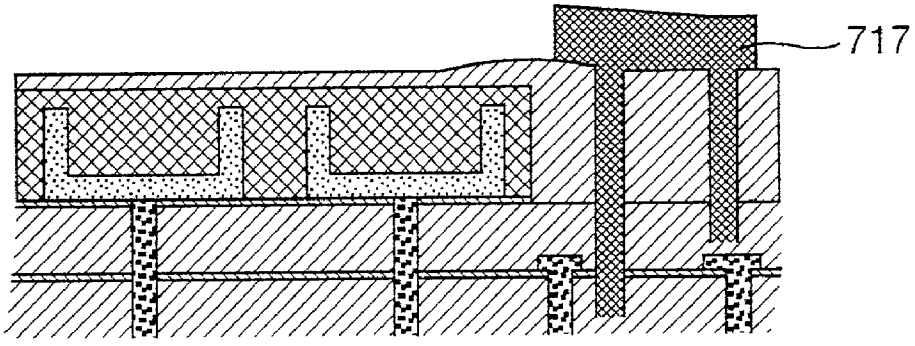


FIG.12a

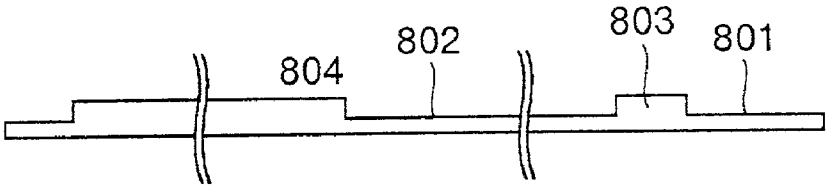


FIG.12b

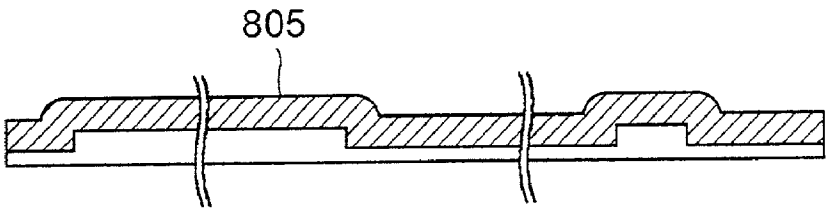


FIG.12c

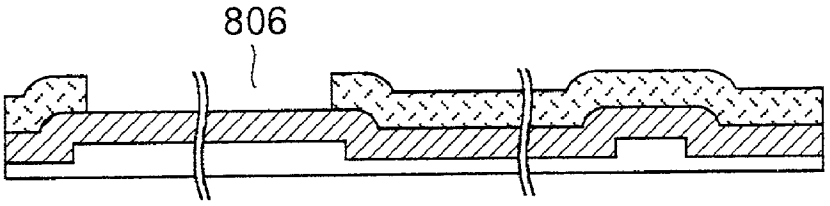


FIG.12d

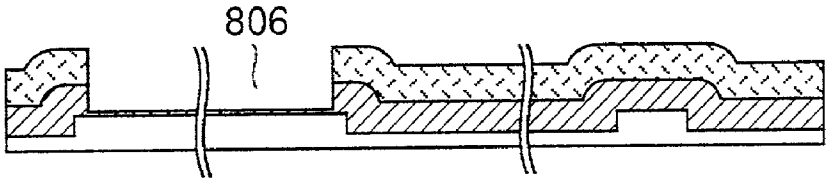


FIG.12e

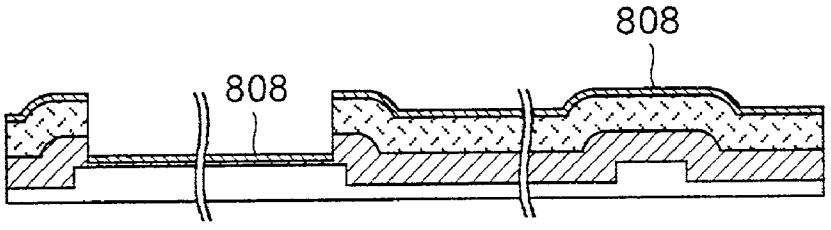


FIG.13a

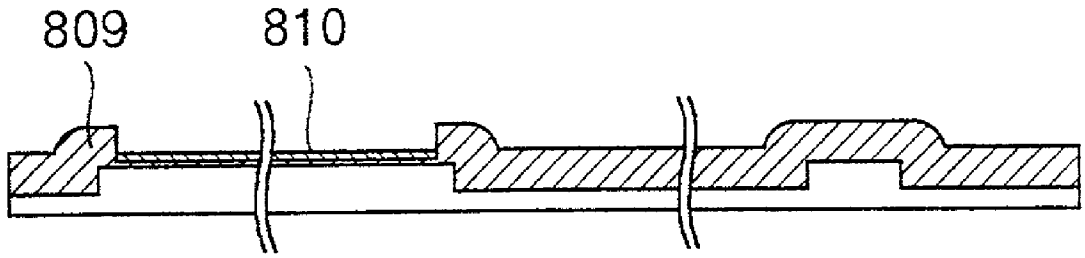


FIG.13b

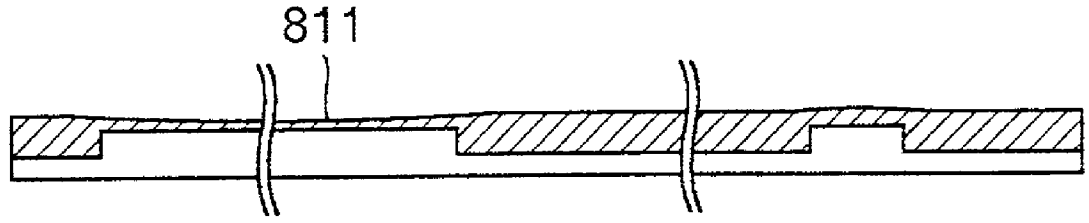


FIG.13c

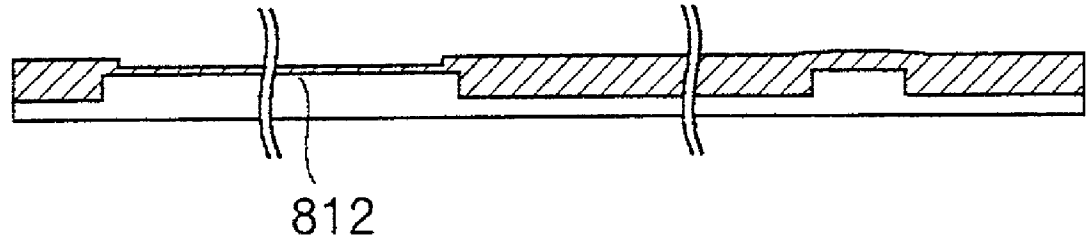


FIG.14a

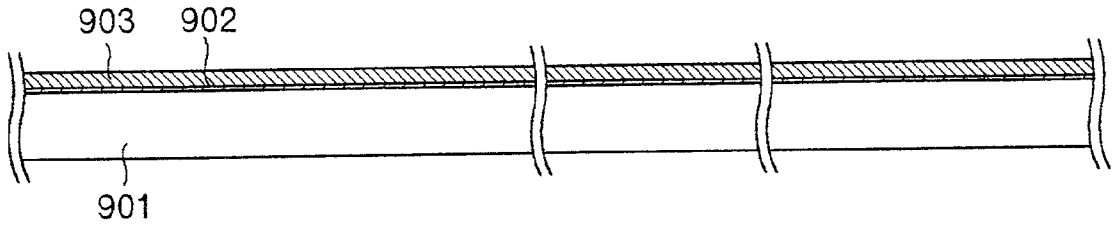


FIG.14b

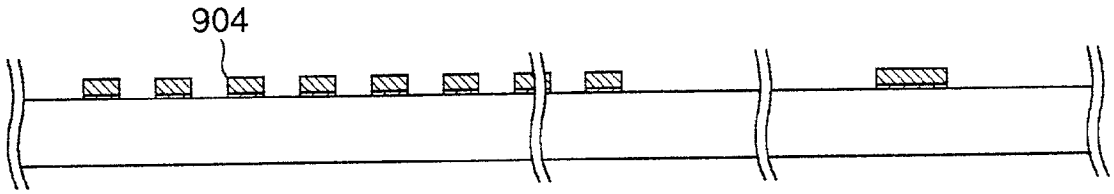


FIG.14c

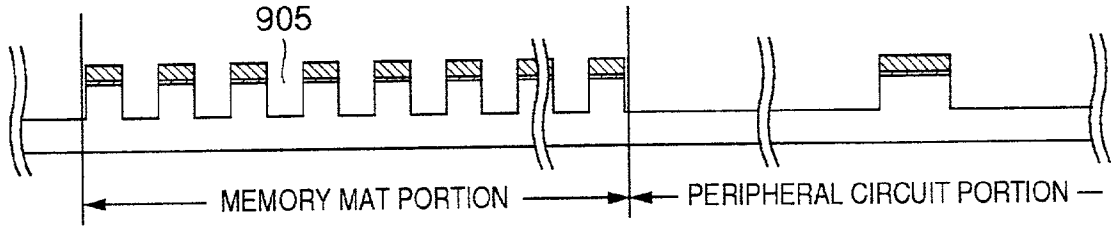


FIG.14d

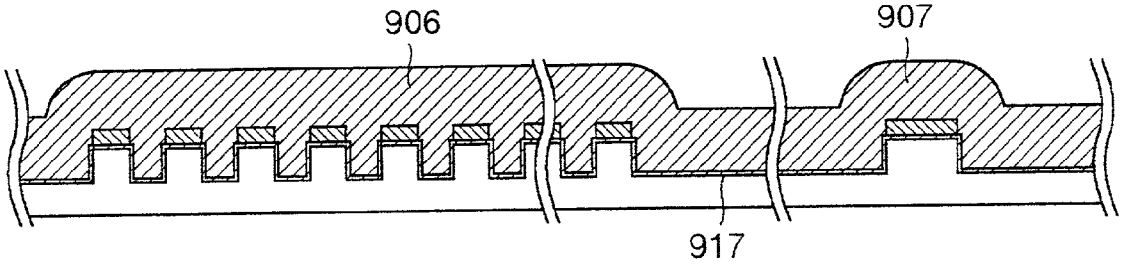


FIG.14e

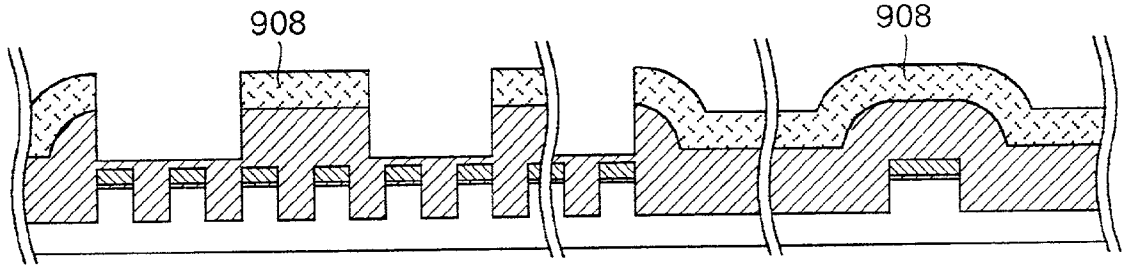


FIG.15a

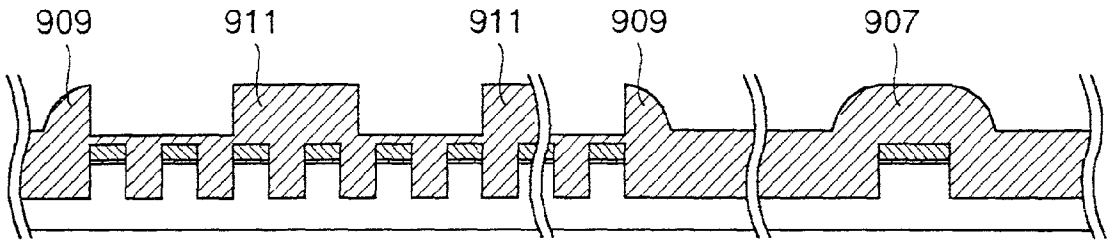


FIG.15b

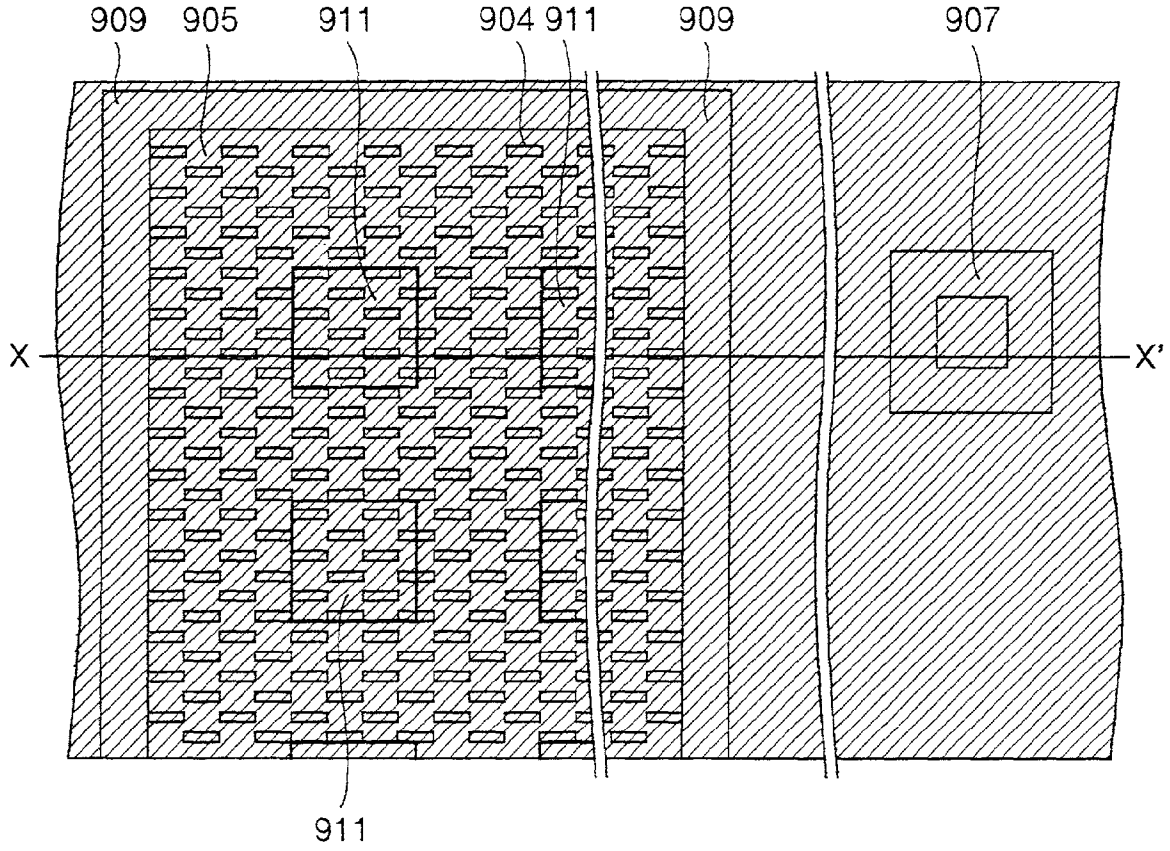


FIG.16a

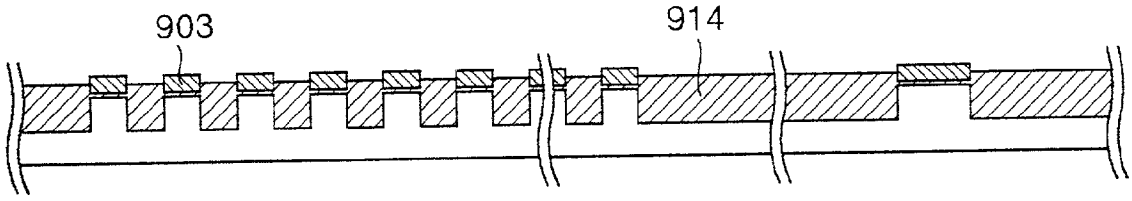


FIG.16b

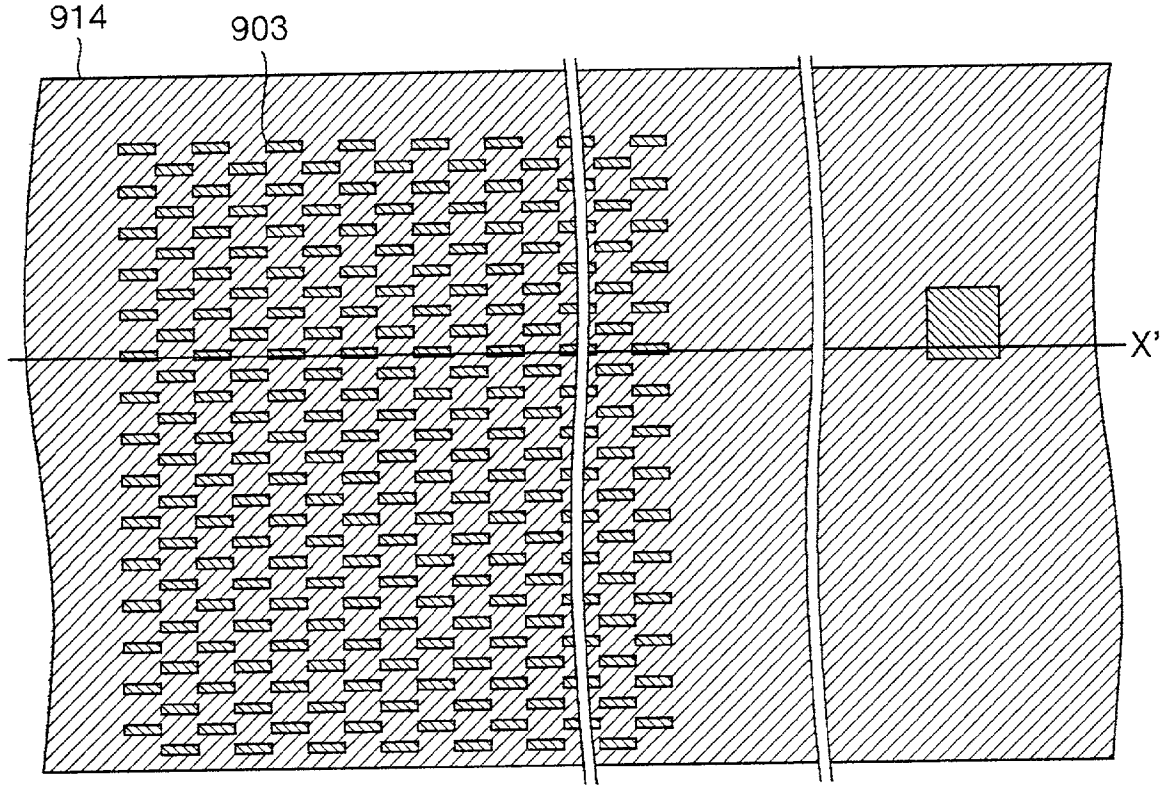


FIG.16c

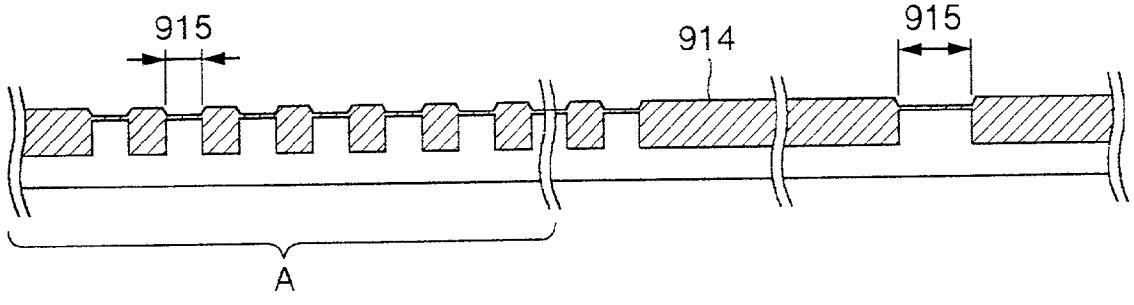


FIG.17a

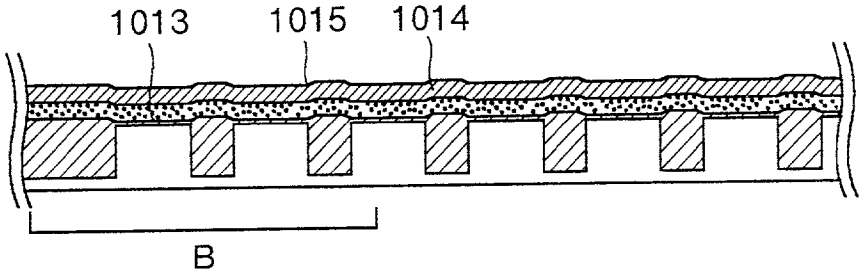


FIG.17b

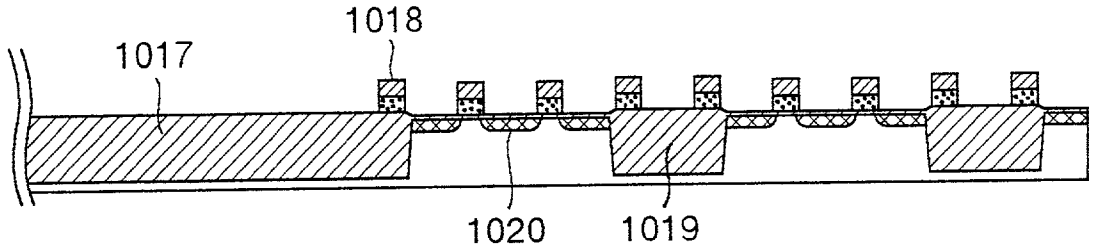


FIG.17c

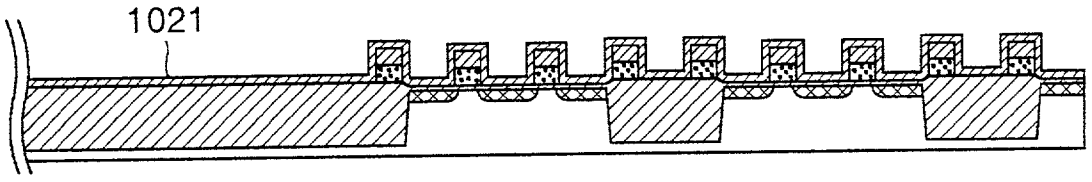


FIG.17d

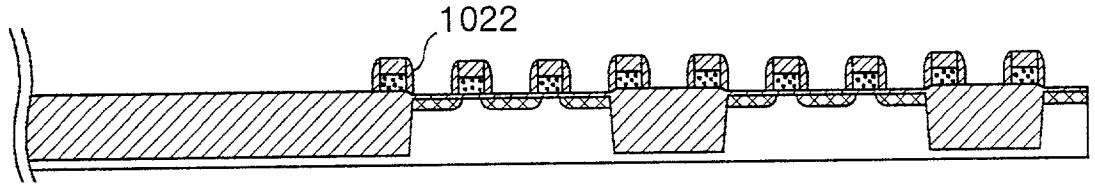


FIG.18a

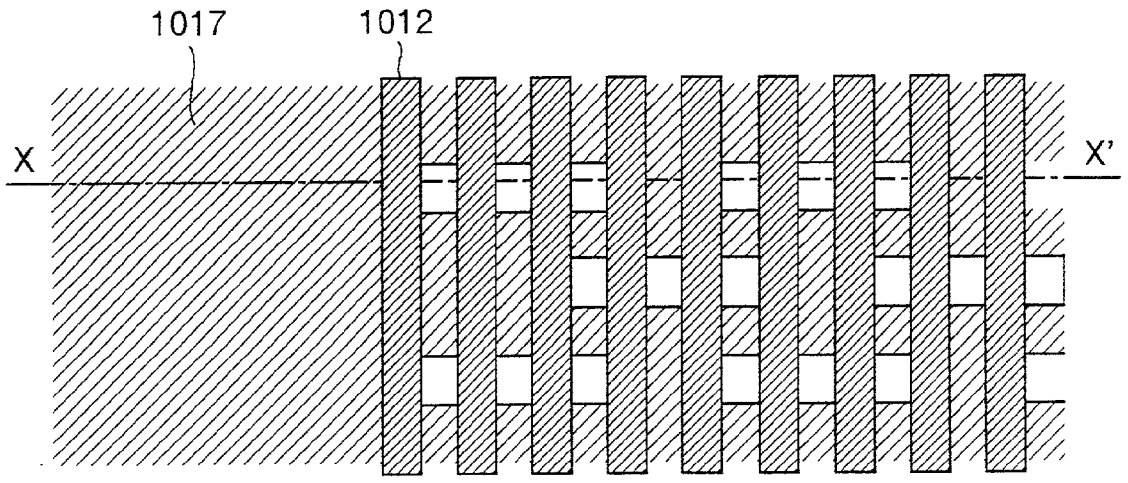


FIG.18b

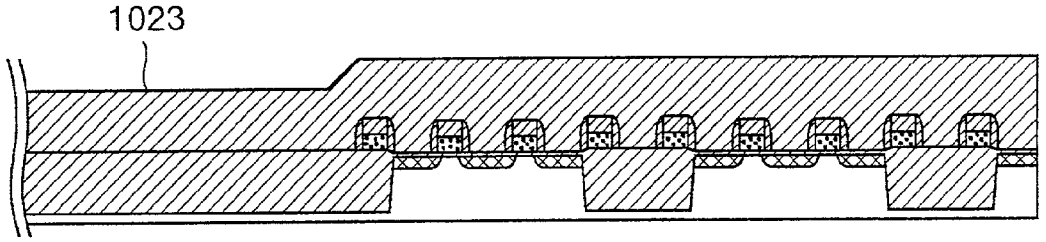


FIG.18c

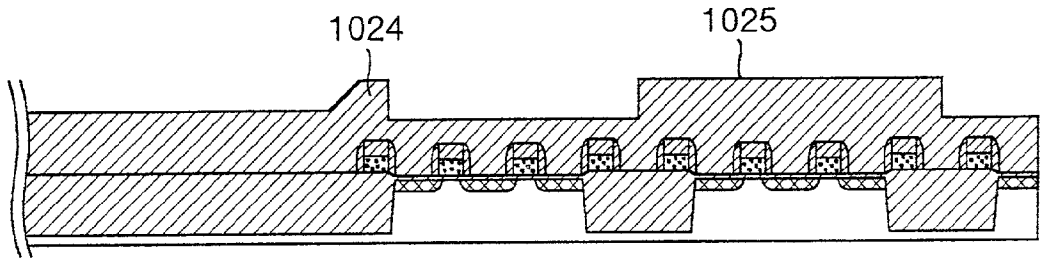


FIG.19a

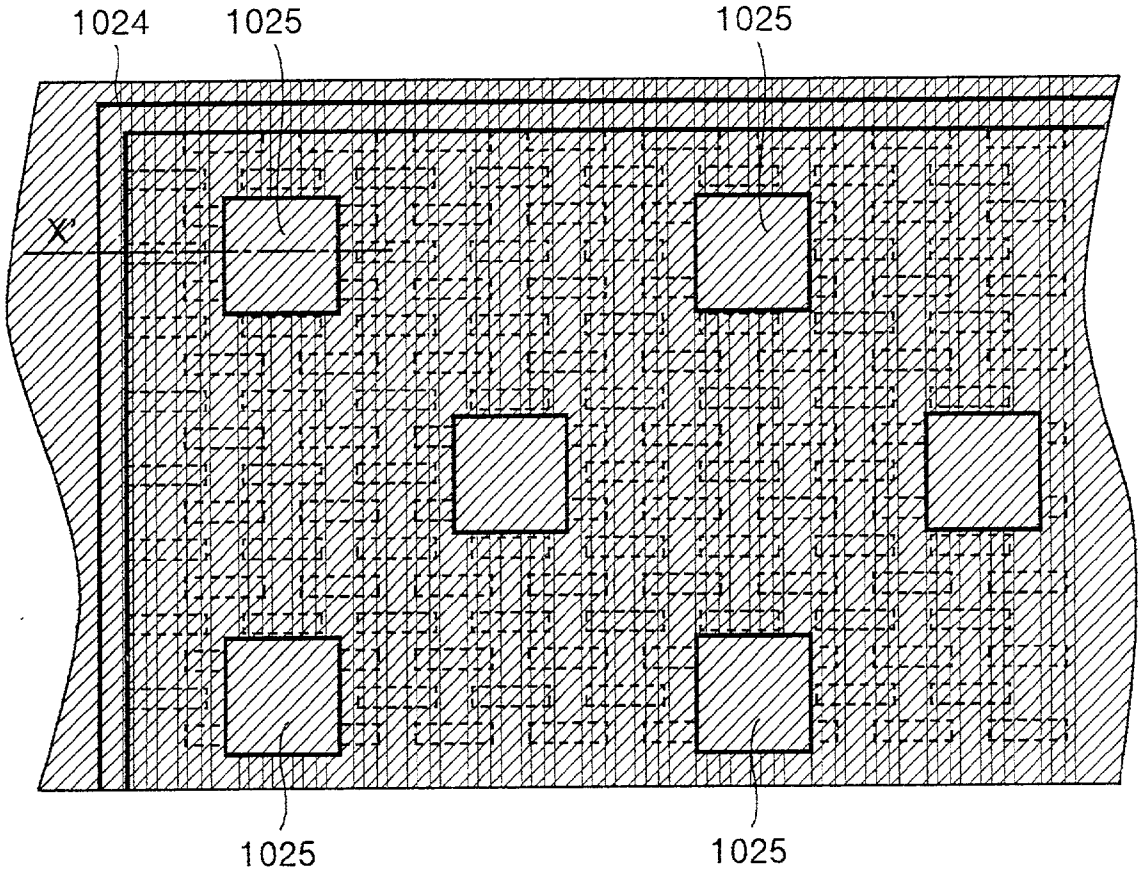


FIG.19b

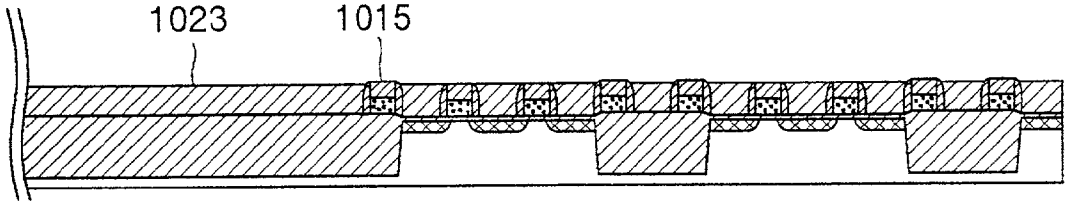


FIG.19c

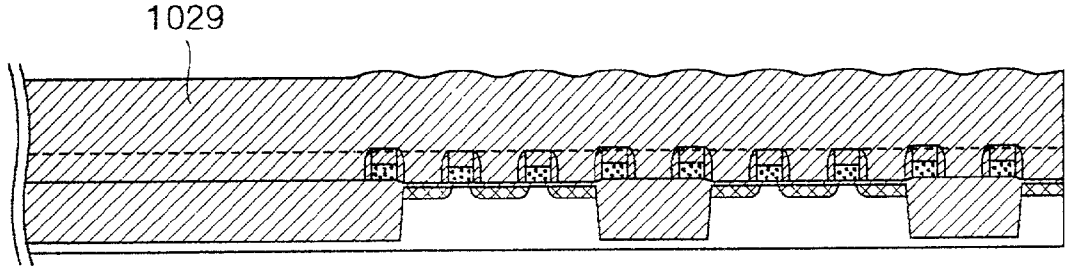


FIG.20a

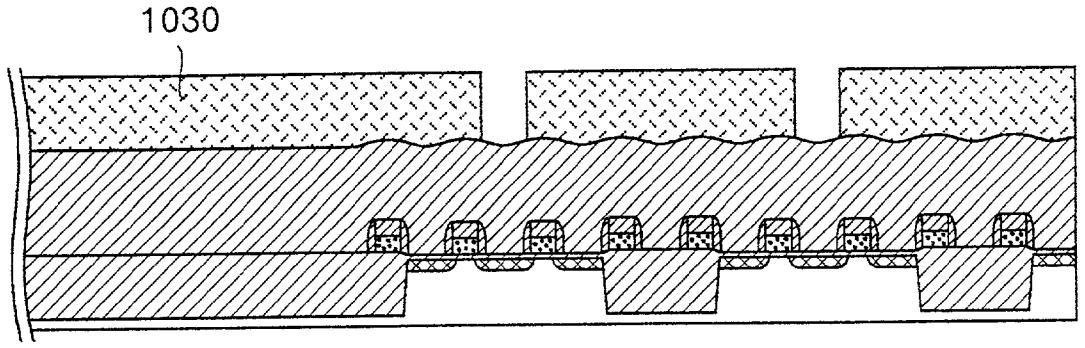


FIG.20b

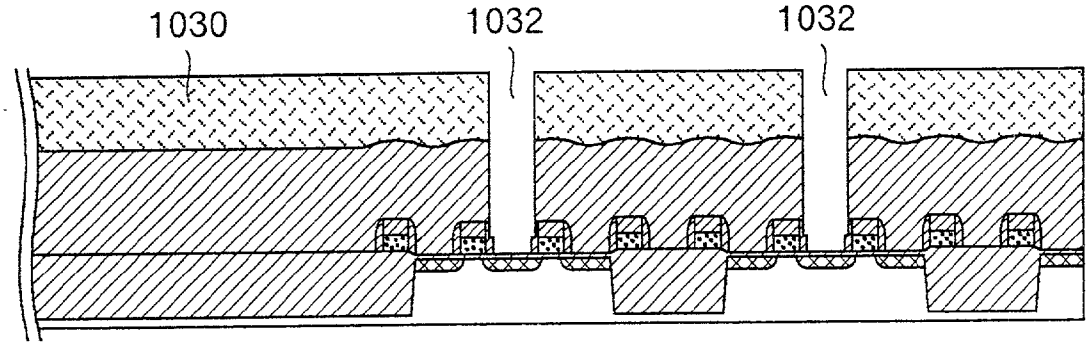


FIG.20c

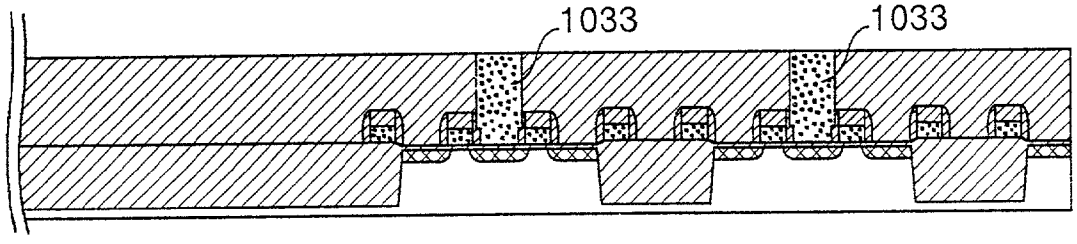


FIG.20d

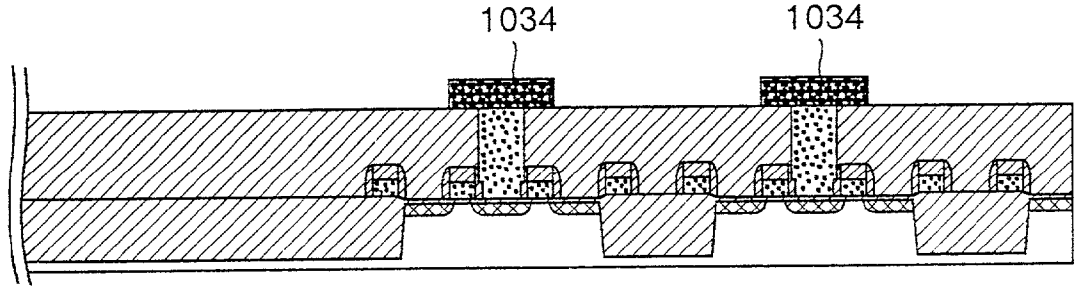


FIG.21a

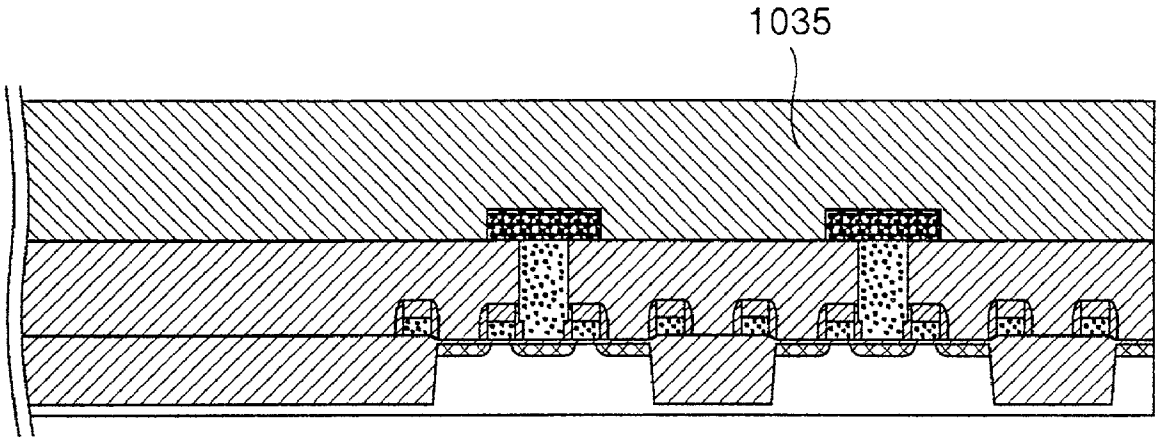


FIG.21b

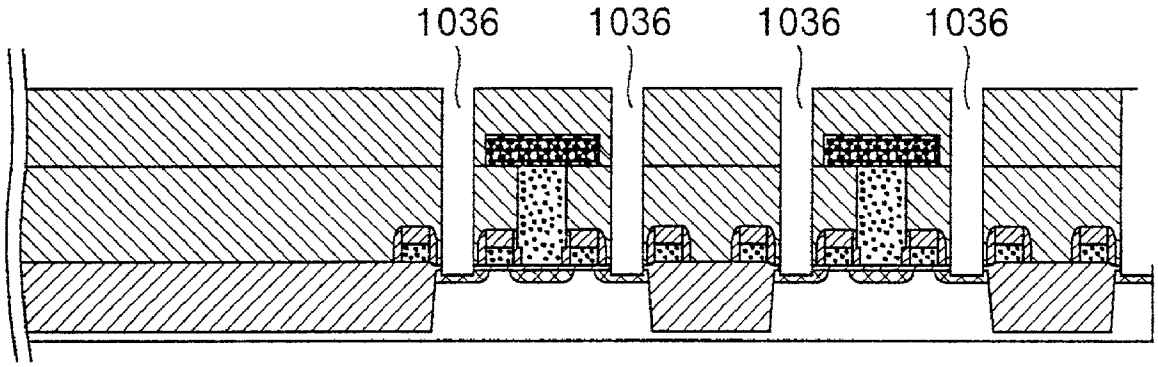


FIG.21c

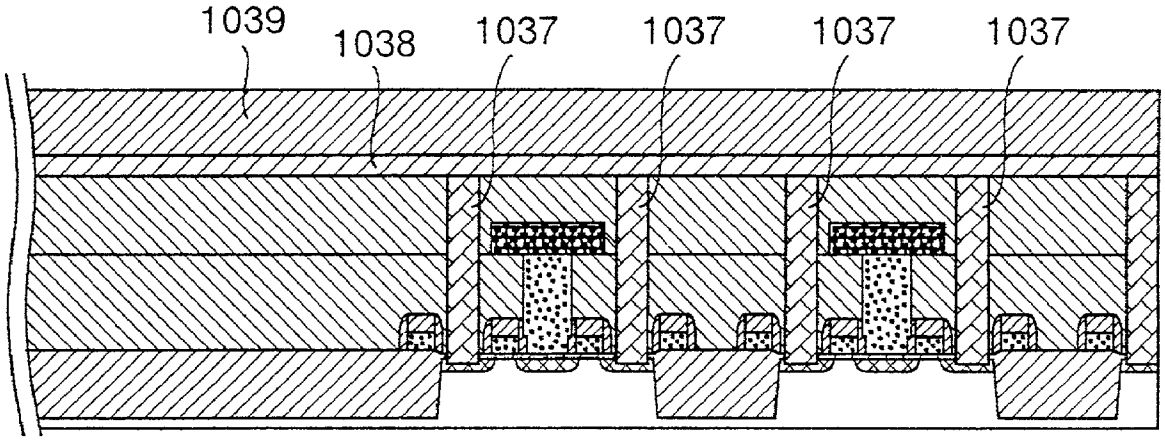


FIG.22a

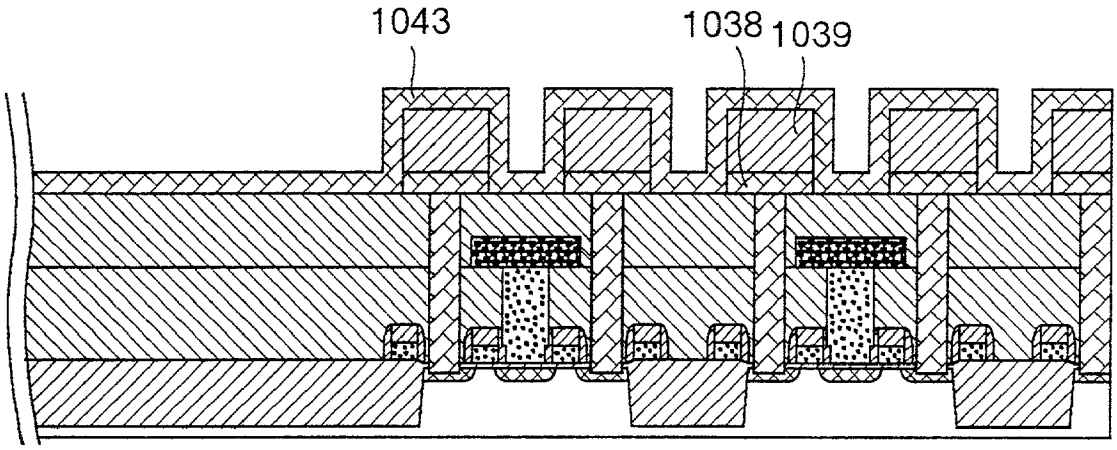


FIG.22b

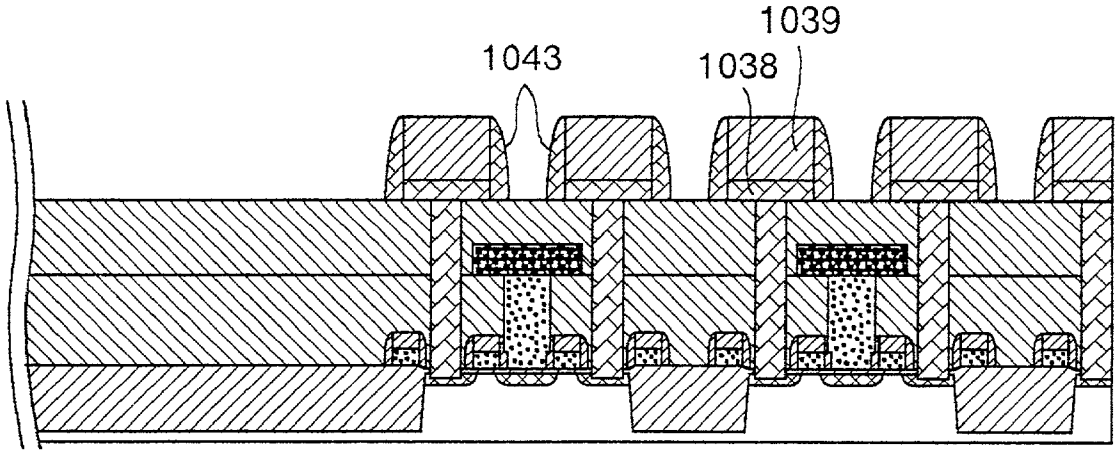


FIG.22c

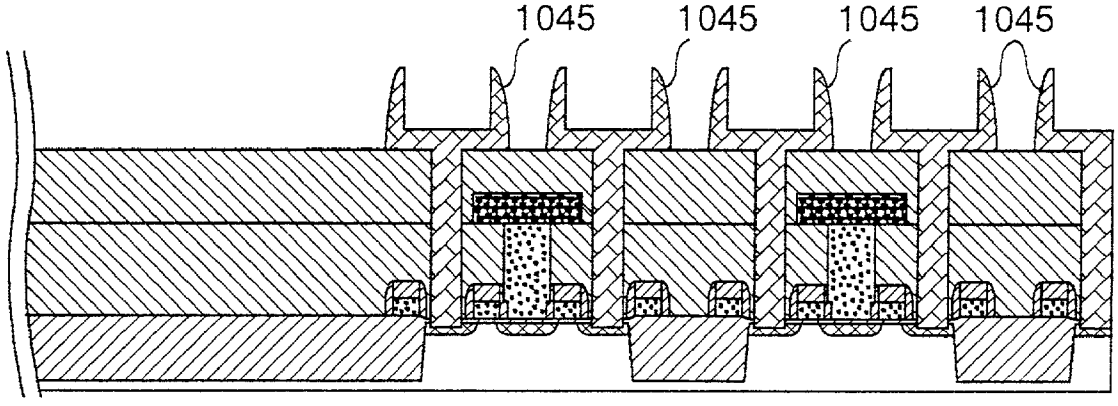


FIG.23a

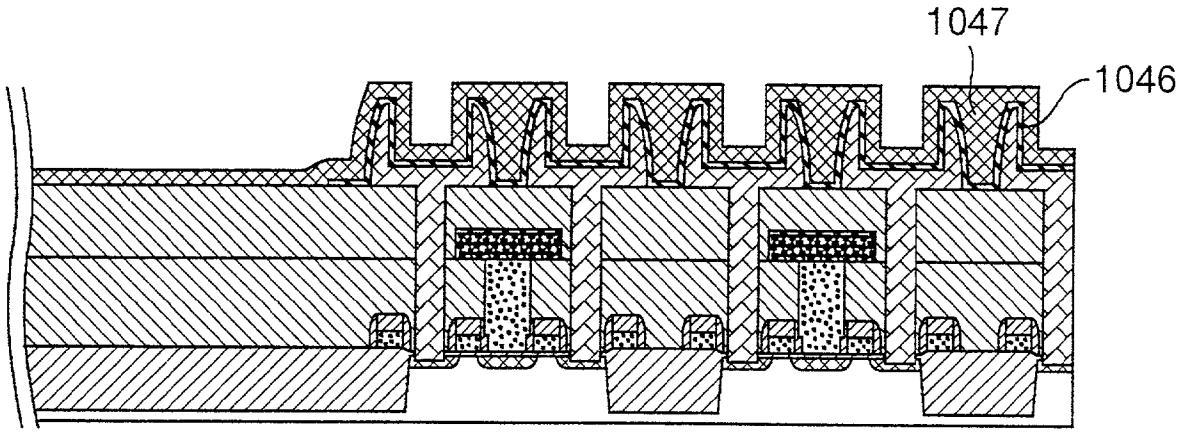


FIG.23b

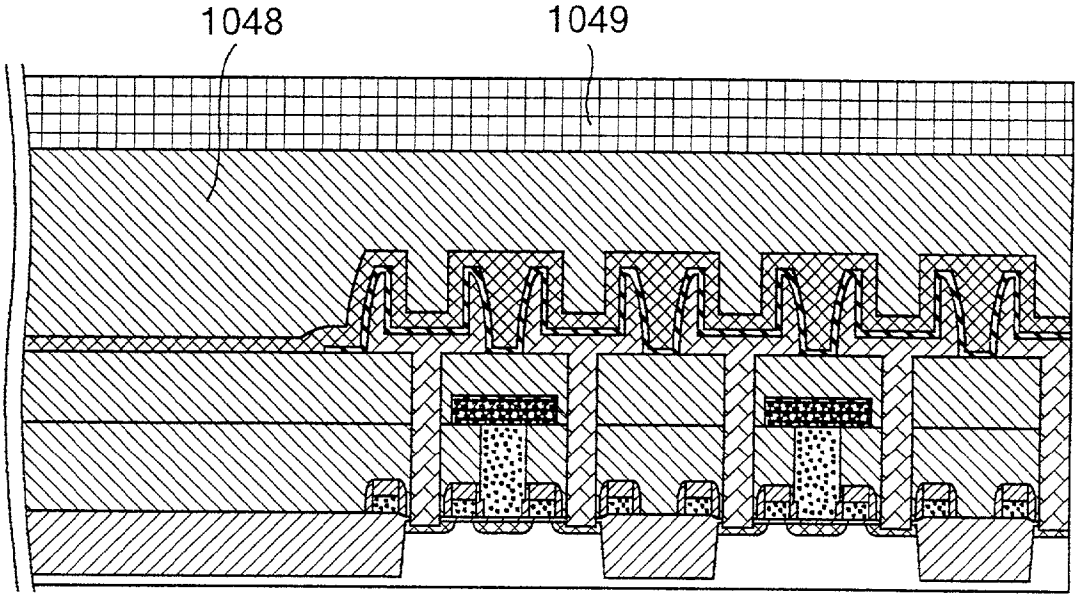


FIG.24a

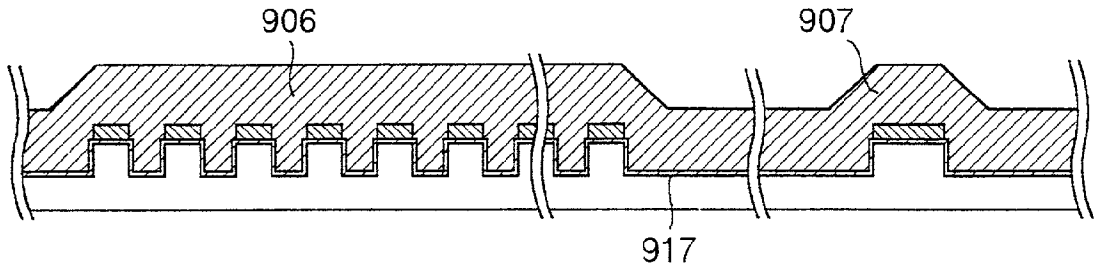


FIG.24b

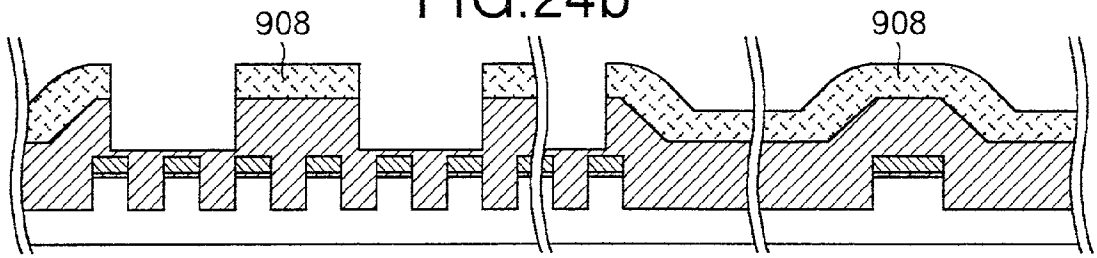


FIG.24c

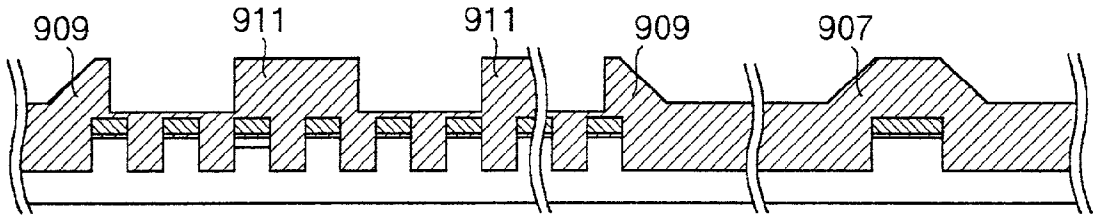


FIG.24d

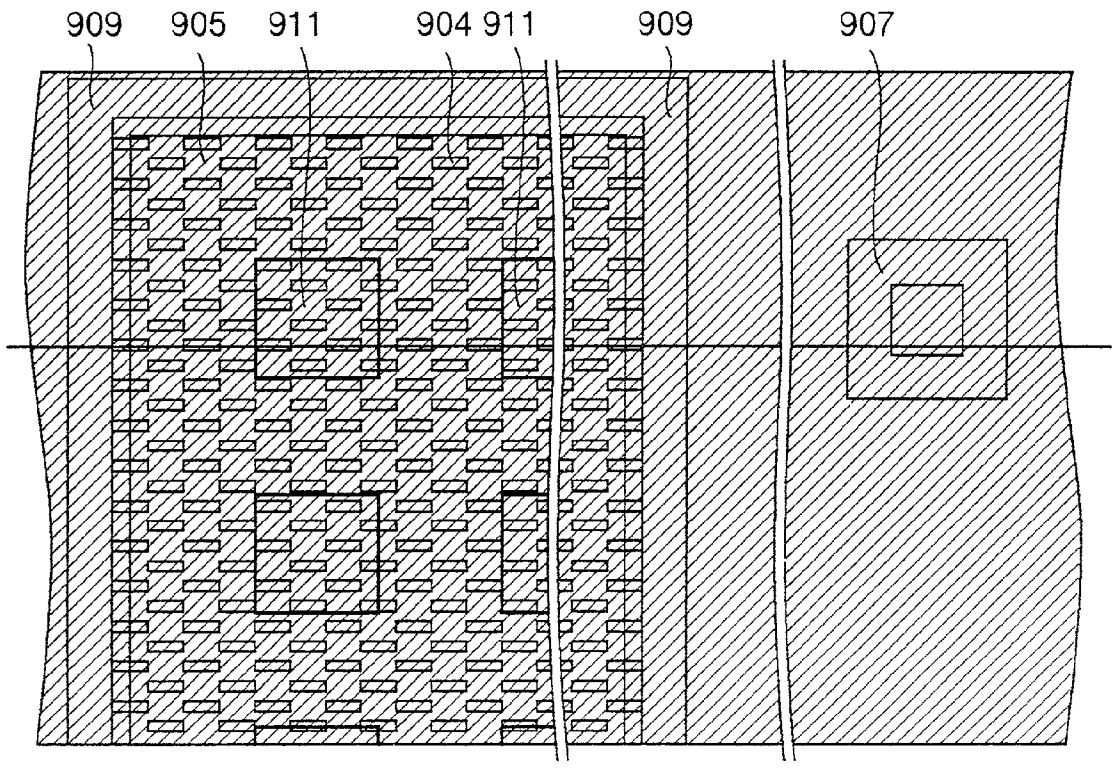
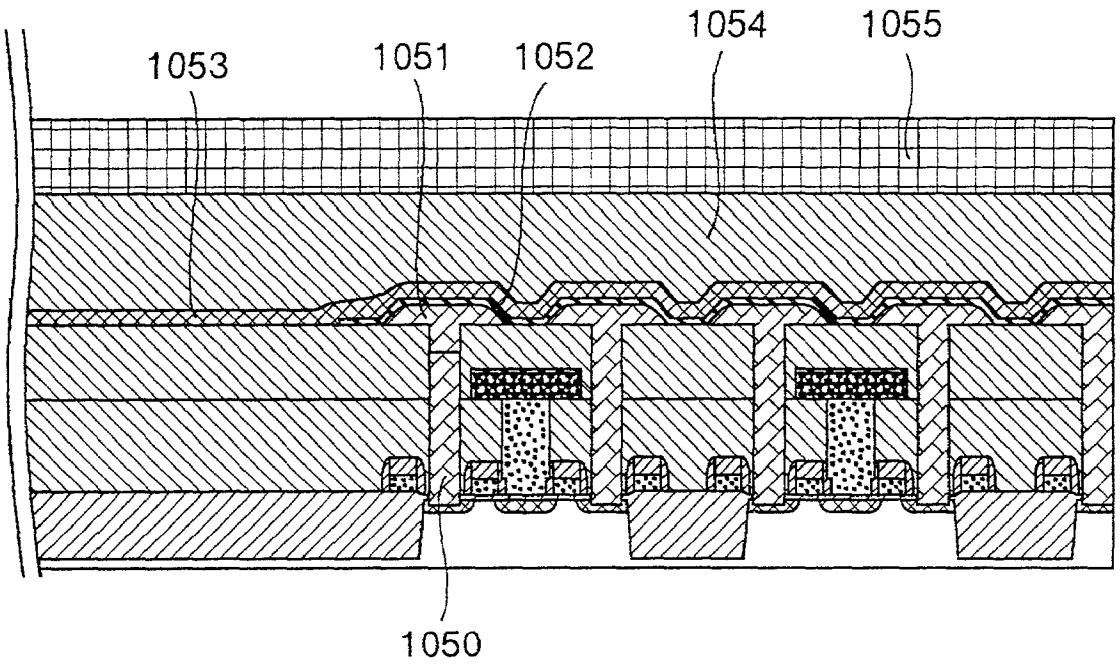


FIG.25



METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a method of making surfaces of processed products smooth, and particularly to a method of making surfaces of semiconductor devices smooth by filling concavities of uneven surfaces of semiconductor devices with an insulating film material.

[0002] Abrasive techniques have been so far used as one of techniques for processing the surface of optical glass. In the field of semiconductor devices, abrasive techniques have been used to make the surface of substrate become mirror finished. Recently, when the surface of interlayer insulators in the process of forming a multilayer interconnection is made smooth, abrasive techniques are applied to make the surface of substrate smooth after a buried insulating film is formed in the trench isolation. In the isolation process, in particular, since the size of a device isolation region that can be realized by a prior-art selection oxide film is limited, the trench isolation using abrasive techniques is indispensable for the planarization process of the surface of the semiconductor devices.

[0003] As a method of forming a trench isolation using an abrasive technique for making the surface of semiconductor device smooth, there has been proposed a method (see JP-A-6-295908 laid-open on Oct. 21, 1994) in which a first stopper layer is formed on the surface of convex portions of a semiconductor substrate having concavities and convexities on its surface, a buried insulating film is deposited on the concavities of the surface of the substrate, a second stopper layer is selectively formed on the surface of the concavities of the buried insulating film and the above-mentioned buried insulating film is removed until the surface of the first stopper layer is exposed by the planarization abrasive technique.

[0004] Also, in order to make the surface of the substrate become smoother, there are known techniques disclosed in JP-A-7-263537 laid-open on Oct. 13, 1995 and JP-A-8-8218 laid-open on Jan. 12, 1996.

SUMMARY OF THE INVENTION

[0005] The inventors of the present application obtained the following knowledge after researches and examinations.

[0006] When the uneven surface of the semiconductor substrate is made smooth by the planarization abrasive technique, it is to be appreciated that a focusing margin required by the next photolithography process is progressively reduced in accordance with the microminituarization.

[0007] According to an example of planarization methods that have been implemented by the inventors of the present application, as shown in **FIGS. 2***a* to **2***f*, an interlayer insulator **205** is deposited on concavities and convexities **202**, **203**, **204** (**FIG. 2***a*) of the surface of a semiconductor substrate **201** (**FIG. 2***b*). Then, after a resist film **206** is formed and processed by patterning, a polished interlayer insulator (**205**) on a relatively large convex portion **204** is etched in advance by photolithography and dry etching (**FIGS. 2***c* to **2***e*).

[0008] When the surface of the semiconductor substrate is made smooth by dry etching and chemical mechanical polishing, as shown in **FIG. 3***a*, corner portions **306** are left on the peripheral portion of the convex portion of the semiconductor substrate so that, as shown in **FIG. 3***c*, polishing slurries **310** are collected between a region surrounded by the corners **306** and a polishing pad **309**, thereby resulting in an etching rate of this region **305** being increased. There is then the risk that a surface **209** of the convex portion will be exposed as shown in **FIG. 2***f*. **FIG. 3***b* is a plan view of the polished surface.

[0009] The above-mentioned problem can be solved by using a semiconductor device manufacturing method shown in **FIGS. 1***a* to **1***f* according to an aspect of the present invention. That is, after an interlayer insulator **105** is deposited on concave and convex structures **102**, **103**, **104** (**FIG. 2***a*) formed on a semiconductor surface **101** (**FIG. 1***b*), by using a conventional photolithography technique, the interlayer insulator **105** is etched to leave an interlayer insulator **107** (pillar) cyclically while an island-like or line-like resist **106** is left within the region of the wide convex portion **104** (**FIGS. 1***c*, **2***d*). Here, the size and interval of the pillar are changed with the area of the convex portion. When the surface of the semiconductor substrate is processed by chemical mechanical polishing, polishing slurries can be suppressed from being collected in the region surrounded by corners **108**. Therefore, it is possible to control the excessive etching in a polished region **109** of the convex portion (**FIGS. 1***e*, **1***f*).

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] **FIGS. 1***a* to **1***f* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to an embodiment of the present invention;

[0011] **FIGS. 2***a* to **2***f* and **FIGS. 3***a* and **3***c* are cross-sectional views showing respective stages in an example of a semiconductor substrate surface planarization-method executed by the inventors of the present application prior to the present invention;

[0012] **FIG. 3***b* is a plan view showing a polishing surface in **FIG. 3***c*;

[0013] **FIGS. 4***a* to **4***e* and **FIGS. 5***a* to **5***d* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention;

[0014] **FIGS. 6***a* to **6***f* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention;

[0015] **FIGS. 7***a* to **7***d* and **FIGS. 8***a* to **8***b* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention;

[0016] **FIGS. 9***a* to **9***c*, **FIGS. 10***a* to **10***b* and **FIGS. 11***a* to **11***c* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention;

[0017] **FIGS. 12***a* to **12***e* and **FIGS. 13***a* to **13***c* are cross-sectional views showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention; and

[0018] **FIGS. 14***a* to **14***e*, **FIGS. 15***a* and **15***b*, **FIGS. 16***a* to **16***c*, **FIGS. 17***a* to **17***d*, **FIGS. 18***a* to **18***c*, **FIGS. 19***a* to **19***c*, **FIGS. 20***a* to **20***d*, **FIGS. 21***a* to **21***c*, **FIGS. 22***a* to **22***c*, **FIGS. 23***a* and **23***b*, **FIGS. 24***a* to **24***d* and **FIG. 25** are diagrams showing respective stages in a method of manufacturing semiconductor devices according to other embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Embodiment 1

[0019] An inventive example 1 will be described with reference to **FIGS. 1***a* to **1***f*. A silicon substrate **101** (**FIG. 1***a*) in which a difference in step between convex portions **103**, **104** serving as active regions and a concave portion **102** serving as a field region was cleaned by RCA cleaning, and a silicon oxide film **105** having a thickness of approximately 350 nano-meter was deposited on the silicon substrate by chemical vapor deposition (hereinafter simply referred to as CVD) (**FIG. 1***b*). Then, by a resist **06**, an opening portion was formed on a wide semiconductor region **104**. In that case, the resist **106** was left so as to form a pillar **107**. (**FIG. 1***c*).

[0020] Thereafter, the resist opening portion and the silicon oxide film were etched by dry etching having a high selection ratio between silicon and silicon oxide film (**FIG. 1***d*). At that time, etching conditions were set in such a manner that the film thickness of the remaining silicon oxide film becomes the same as the height of the surface of the silicon oxide film of the wide field portion. The resist **106** was removed by organic cleaning (**FIG. 1***e*), and the above-mentioned sample was made smooth by polishing. In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 6 minutes (**FIG. 1***f*).

[0021] According to this inventive example, it became possible to make the uneven semiconductor surface **101** smooth. In the conventional method, the semiconductor surface **209** was exposed at the central portion of the wide active region **204** due to dishing (**FIG. 2***f*) and could not made smooth. However, according to this inventive example, the semiconductor surface could be made smooth within a step difference of several 10s of nano-meter.

Embodiment 2

[0022] An inventive example **2** will be described with reference to **FIGS. 4***a* to **4***e* and **FIGS. 5***a* to **5***d*. After a silicon substrate **401** that had been cleaned by RCA cleaning was oxidized and a silicon oxide film **402** having a thickness of approximately 50 nano-meter, a silicon nitride film **403** having a film thickness of **150** nanometer was deposited by CVD. Then, a resist pattern was formed on the element forming region of the silicon nitride film surface (**FIG. 4***a*). This resist pattern was used as an etching mask, and the silicon nitride film **403**, the thermal oxide film **402** and the silicon substrate **401** were etched by a depth of approximately 0.3 micron from the surface by dry etching (**FIG. 4***b*).

[0023] After the above-mentioned substrate was cleaned, a thermal oxide film **404** having a film thickness of approximately 30 nano-meter was formed within the silicon groove by thermal oxidation. Further, a silicon oxide film **408** having a film thickness of 150 nano-meter was deposited (**FIG. 4***c*). Then, a silicon nitride film **409** having a film thickness of 150 nano-meter was deposited (**FIG. 4***d*), and a resist **411** for forming a pillar **411** was formed on a convex portion **406** by patterning as shown in **FIG. 4***e*.

[0024] Thereafter, the silicon nitride film **409** of the resist opening portion **412** and the silicon oxide film **408** between the layers were etched by dry etching (**FIG. 5***a*). In this case, the remaining film thickness **413** o the silicon oxide film formed on the convex portion was selected to be the same as the height of the silicon oxide film **414** of the wide field region. After the resist **409** was removed and the product was cleaned (**FIG. 5***b*), the resultant product was processed by chemical mechanical polishing and the surface thereof was made smooth (**FIG. 5***c*).

[0025] In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 4 minutes (**FIG. 1***f*). When the surface of the sample was made smooth by polishing, a corner **415** of the convex portion on the substrate was removed initially. In that case, since the field region **407** was protected by the silicon nitride film **409** having the small polishing rate, dishing can be avoided. Also, since the pillar **417** exists in the convex portion region **416** surrounded by the corners **415**, the etching rate can be prevented from being increased. Accordingly, as shown in **FIG. 5***c*, the surface of the sample can be made smooth.

[0026] In the chemical mechanical polishing, when the polishing reaches the silicon nitride film **418** on the active region, the polishing rate was lowered considerably. At that time point, the chemical mechanical polishing was stopped. Thereafter, the silicon nitride film **418** was removed from the active region, and the sample was cleaned (**FIG. 5***d*).

[0027] According to the method shown in this inventive example, there could be formed the active region in which an interlayer insulator **40** was buried. When the surface of the semiconductor substrate was made smooth by the conventional method, there arose the problem that the silicon substrate surface was exposed. Also, when a step difference **420** between the active region and the field region was large and the microstructure gate was formed, there arose the problem that the gate was on the step difference. According to this inventive example, it became possible to solve the above-mentioned problems.

Embodiment 3

[0028] An inventive example 3 will be described with reference to **FIGS. 6***a* to **6***f*. The surface of a silicon substrate **501** in which a step difference between active regions **503**, **504** and a field region **502** is 0.3 micrometer was cleaned by RCA cleaning (**FIG. 6***a*), and a silicon oxide film **505** having a film thickness of approximately 350 nm was deposited by HDP (High Density Plasma). In HDP, since the film is sputtered at the same time the film is deposited, the sample has a characteristic shape shown in **FIG. 6***a*. Then, an

opening portion **508** was formed on the wide semiconductor active region **504** by a resist **506** (**FIG. 6***c*).

[**0029**] In that case, an island-like resist **507** was left so as to form a pillar. Thereafter, the silicon oxide film **505** of the resist opening portion **508** was etched by dry etching having a high selection ratio between the silicon and the silicon oxide film. At that time, etching conditions were set in such a manner that the thickness of the remaining film of the silicon oxide film becomes the same as the height of the surface of the silicon oxide film of the wide field (**FIG. 6***d*). Then, the resist **506** was removed by organic cleaning (**FIG. 6***e*), and the above-mentioned sample was processed by chemical mechanical polishing. In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 6 minutes (**FIG. 6***f*).

[**0030**] According to this inventive example, it became possible to make the uneven surface of the semiconductor structure **501** smooth. According to the conventional method, the semiconductor surface formed at the center portion of the sufficiently wide active region **504** was exposed due to dishing, and the semiconductor surface could not be made smooth. According to the method of the present invention, since the HDO silicon oxide film was used to bury the interlayer insulator, the shape obtained after the deposition was special shape as shown in **FIG. 6***b*. Therefore, the mechanical polishing amount in this inventive example was small as compared with that used when the silicon oxide film deposited according to the conventional CVD. Thus, it became possible to make the semiconductor surface smooth within a step difference to approximately tens and several nano-meters by a combination of the conventional method and the inventive method.

Embodiment 4

[**0031**] An inventive example **4** will be described with reference to **FIGS. 7***a* to **7***d* and **FIGS. 8***a* and **8***b*. After a silicon substrate **601** in which a buried silicon oxide film **602** was formed so as to isolate elements was cleaned by RCA cleaning, there was formed a gate oxide film **603** having a film thickness of 6 nano-meter (**FIG. 7***a*). Thereafter, a polycrystalline silicon film **604** having a film thickness of 80 nano-meter in which phosphorous is highly added and a tungsten film **605** having a film thickness of 80 nano-meter were deposited and a wide capacitor gate electrode **606** was formed by photolithography and dry etching (**FIG. 7***b*). Incidentally, while the gate electrodes **605**/**604** are disposed in such a manner as to overlap with the element isolation oxide film **602** from a cross-sectional standpoint, they need not be disposed in such a manner. Also, while the space between the tungsten film **605** and the polycrystalline silicon **604** needs a barrier layer for suppressing the reaction, such space is omitted.

[**0032**] Subsequently, a silicon oxide film **607** having a film thickness of 200 nano-meter in which phorphorous was heavily added was deposited by HDP. Here, under the condition that the gate electrode is not processed by sputtering when the silicon oxide film **607** is formed by HDP, an HDP silicon oxide film **607** was deposited (**FIG. 7***c*). Thereafter, by photolithography and dry etching, an HDP silicon oxide film was removed from the resist opening portion **609** so as to leave pillars of the silicon oxide film on the gate electrode **606** (**FIG. 7***d*). After the resist **608** was removed, the surface of the sample was made smooth by chemical mechanical polishing. According to the inventive method, since a pillar **610** exists in the region surrounded by corners **11** (**FIG. 8***a*), an interlayer silicon oxide film **612** on the gate electrode **601** is not deteriorated by dishing and the gate electrode **606** can be prevented from being exposed (**FIG. 8***b*).

[**0033**] According to the conventional method, although the gate electrode **606** is exposed or the surface of an interlayer silicon oxide film **612** was considerably uneven, according to this inventive example, the gate electrode **606** could completely be prevented from being exposed. Further, it became possible to control the unevenness of the silicon oxide film within a range of tens and several tens of nano-meter.

Embodiment 5

[**0034**] An inventive example **5** will be described with reference to **FIGS. 9***a* to **9***c* and **FIGS. 10, 10***b* and **FIGS. 11***a* to **11***c*. After a highly-integrated memory transistor (not shown), an interlayer insulator **701** and interconnections **702**, **703** were formed on the silicon substrate surface, a protruded capacitor structure **704** called a crown structure was formed (**FIG. 9***a*). This pattern became the convex pattern formed on the substrate surface. Since the protruded capacitor **704** has a height **707** of approximately 1 micrometer, if a silicon insulating film **707** which covers the protruded capacitor is deposited, then a step difference of approximately 1 micrometer was formed between it and a region in which no capacitor was formed (**FIG. 9***a*). While the silicon oxide film **707** was deposited by HDP, in that case, the conditions in which the silicon oxide film **707** is deposited were set in such a manner that the capacitor structure may not be damaged or may not be etched by sputtering.

[**0035**] Thereafter, a resist film **708** was formed (**FIG. 9***c*), and the resist **708** was patterned by photolithography. In that case, a resist **709** was set so as to overlap with the inside of the capacitor structure **704**, and a pillar **710** was left on the portion of the capacitor structure **704** (**FIG. 10***a*). The silicon oxide film **707** of a resist opening portion **711** was etched by dry etching (**FIG. 10***b*). In that case, the dry etching conditions were set in such a manner that a silicon oxide film surface **712** in the region on which the capacitor structure is no formed may substantially agree with an etching surface **713**.

[**0036**] Thereafter, the above-mentioned sample was chemically mechanically polished (**FIG. 11***a*). In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 8 minutes. According to the method shown in this inventive example, it became possible to make the capacitor structure smooth by the silicon oxide film **707**.

[**0037**] While it was difficult to form a very small resist pattern **715** by a step difference **714** left around the capacitor structure upon conventional planarization using phospho-

rous glass, according to the planarization method of this inventive example, since the resist pattern **715** that is very smaller than that of the conventional one was formed (**FIG. 11***b*), it became possible to form a very small contact hole **716** and a narrow interconnection **717** (**FIG. 11***c*).

Embodiment 6

[**0038**] An inventive example 6 will be described with reference to **FIGS. 12***a* to **12***c* and **FIGS. 13***a* to **13***c*. The surface of a silicon substrate **801** in which a step difference between active regions **803**, **804** and a field region **802** is 0.35 micrometer was cleaned by RCA cleaning (**FIG. 12***a*), and a silicon oxide film **805** having a film thickness of approximately 350 nano-meter was deposited by chemical vapor deposition (hereinafter referred to as a CVD).

[**0039**] Then, an opening portion **806** was formed on the resist **805** of the wide semiconductor active region **804** (**FIG. 12***c*). Only the silicon oxide film **805** of the resist opening portion **806** was removed by dry etching (**FIG. 12***d*). Thereafter, a silicon nitride film **808** was deposited by sputtering (**FIG. 12***e*). Under this condition, when the silicon nitride film **808** was deposited, the silicon nitride film **808** within the opening portion **806** and the silicon nitride film **808** on the wide field **802** and the narrow active region **803** are isolated from each other. Thereafter, by removing the resist **805**, the silicon nitride film **808** on the resist **805** also was removed simultaneously (**FIG. 13***a*).

[**0040**] This sample was chemically mechanically polished (**FIG. 13***b*). In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 4 minutes. In that case, although slurries are collected in a region **810** surrounded by the corners **809** so that the polishing rate increases, the polishing rate of the silicon nitride film **808**-was approximately ¼ as compared with that of the silicon oxide film **805**. Thus, it could be confirmed that dishing was not caused in the region **810** surrounded by the corners **809**. When the polishing surface reaches the silicon nitride film **808** on the wide field **804** by chemical mechanical polishing, a rotation torque of a polishing apparatus increases so that chemical mechanical polishing is stopped. Thereafter, a silicon nitride film **811** on the wide field **804** was removed and made smooth (**FIG. 13***c*).

[**0041**] According to this inventive example, it became possible to make the uneven surface of the semiconductor structure **801** smooth. Although the element characteristic was deteriorated by depression of the silicon oxide film at the end portions of the active regions **803**, **804** according to the conventional method, with this inventive example, it became possible to completely suppress the depression of this silicon oxide film. Also, it became possible to suppress the semiconductor surface **812** from being exposed due to dishing caused on the wide active region **804**.

Embodiment 7

[**0042**] An inventive example of a DRAM manufacturing method according to this invention will be described with reference to **FIGS. 14***a* to **14***e*, **FIGS. 15***a* and **15***b*, **FIGS. 16***a* to **16***c*, **FIGS. 17***a* to **17***d*, **FIGS. 18***a* to **18***c*, **FIGS. 19***a* to **19***c*, **FIGS. 20***a* to **20***d*, **FIGS. 21***a* to **21***c*, **FIGS. 22***a* to **22***c*, **FIGS. 23***a* and **23***b*, **FIGS. 24***a* to **24***d* and **FIG. 25**.

[**0043**] Initially, as shown in **FIG. 14***a*, after a silicon substrate **901** was cleaned, there was formed a silicon oxide film **902** for protecting the surface of the silicon substrate **901** by thermal oxidization. Further, a silicon nitride film **903** was deposited on the silicon oxide film **902** by CVD. This silicon nitride film **903** serves as a polishing stopper film for suppressing an excess polishing in the later chemical mechanical polishing.

[**0044**] Next, a laminated film of the silicon oxide film **902** and the silicon nitride film **903** was patterned by photolithography and dry etching (**FIG. 14***b*). The laminated film **904** thus patterned was used as a hard mask, and a groove structure was formed by dry-etching the silicon substrate (**FIG. 14***c*). The left-hand side of **FIG. 1***c* shows the cross-sectional structure of the memory mat portion of a DRAM (Dynamic Random Access Memory), and the right-hand side thereof show the cross-sectional structure of the peripheral circuit portion, respectively. The concave portion of the silicon substrate **901** was later filled with the insulating material to become the field region for isolating elements, and the convex portion of the silicon substrate **901** became the active region in which elements will be formed later on. As shown in **FIG. 14***c*, the active region and the field region were densely formed in the memory mat portion as compared with the peripheral circuit portion.

[**0045**] Then, after the silicon substrate **901** was cleaned, a thermal oxide film (silicon oxide film) **917** was formed on the inner surface of the groove structure by thermal oxidization. Further, insulating films (silicon oxide films) **906**, **907** were deposited by CVD using well-known O_3—TEOS (**FIG. 14***d*). Since the opening portion of the groove structure became small in the memory mat portion in which the uneven patterns of the active region and the field region are formed densely (spacing between adjacent active regions is reduced), as shown in **FIG. 14***d*, the insulating film **906** whose upper surface is substantially the same height was formed over the whole surface of the memory mat portion.

[**0046**] The film thickness of the silicon nitride film **903** serving as the deposited polishing stopper in **FIG. 14***a* should preferably be made thicker from a standpoint of increasing a process margin-used in the later chemical mechanical polishing. However, when the film thickness of the silicon nitride film **903** is increased, the aspect ratio of the groove structure **905** increases. As a result, when the insulating film **906** is deposited in FIG. **14***b*, the groove structure **905** cannot be completely filled with the insulating film **906** so that the element isolation characteristic of the field region becomes insufficient. Therefore, the silicon nitride film **903** cannot be made thick.

[**0047**] Next, in order to reduce the polishing amount required in the later chemical mechanical polishing, a part of the insulating film **906** which became the convex shape on the memory mat portion was removed by photolithography/dry etching (**FIG. 14***e*). Further, when a resist **908** is removed, there is presented a cross-sectional view shown in **FIG. 15***a*. **FIG. 15***b* is a plan view of **FIG. 15***a*, and the cross-sectional structure shown by X-X' in **FIG. 15***b* corresponds to **FIG. 15***a*.

[**0048**] The first features of the inventive example 7 lies in that the insulating film **906** on the memory mat portion is not

removed from the whole area of the memory mat portion but a part of the insulating film is removed and the insulating film **906** is left partly. In the inventive example 7, the portion of this remaining insulating film is referred to as a pillar **911**. In other words, it is important to form the pillar **911** of the insulating film on the memory mat portion.

[**0049**] The shape of this pillar **911** is optimized to be dot-like shape or line-like shape in accordance with the polishing amount and the polishing target material of the chemical mechanical polishing of the insulating film, shapes of the active region and the field region of the memory mat portion and the size of the memory mat portion. Also, regardless of the pattern of the groove structure **905** of the lower layer, the pillar **911** may be disposed and the regular repetitive pattern. Further, the shape, size and location of the pillar **911** are determined in such a manner that the volume of the insulating film that should be polished by chemical mechanical polishing in the peripheral circuit portion other than the memory mat portion becomes substantially equal to a result which results from adding the volume of the pillar **911** to the volume of the corner **908** in the outer peripheral portion of the memory mat portion. Thus, the polishing amounts required in the chemical mechanical polishing become uniform on the whole.

[**0050**] **FIGS. 14***d*, **14***e*, **15***a*, **15***b* show an example in which insulating films **906**, **907** are deposited by CVD using O_3—TEOS. **FIGS. 24***a* to **24***d* show an example in which the insulating films **906**, **907** are deposited by HDP (High Density Plasma). In this case, as shown in **FIGS. 24***b* to **24***d*, when the insulating films **906**, **907** are partly removed from the memory mat portion, the inner periphery of the corner **909** comes closer to the inside as compared with the outer periphery of the memory mat portion in such a manner that the height of the corner **909** of the insulating film becomes coincident with that of the pillar **908**. The shape of the pillar **911** and the like are similar to those of the case in which O_3—TEOS was used. Incidentally, the cross-sectional structure shown by X-X' in **FIG. 24***b* corresponds to **FIG. 15***a*.

[**0051**] This sample was chemically mechanically polished (**FIG. 16***a*). A second features of the inventive example 7 lies in that the insulating films **906**, **907** on the active region are removed by chemical mechanical polishing until the silicon nitride film **903** serving as the polishing stopper on the active region is exposed. In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 500 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 4 minutes.

[**0052**] In the initial stage of the chemical mechanical polishing, the corner **909** of the insulating film surrounding the outer periphery of the memory mat portion and the pillar **911** of the insulating film which is substantially the same in height as the corner **909** of this insulating film were polished initially. Since the load of the chemical mechanical polishing concentrated in the corner **909** of the insulating film in the prior art was dispersed into the pillar **911**, the bending of the corner **909** of the insulating film could be considerably suppressed. Thus, the amount in which scratches were produced could be suppressed considerably, and the fraction defective could be lowered considerably.

[**0053**] The sample was further polished, the end of the polishing was detected in the silicon nitride film **903** serving as the polishing stopper, and the chemical mechanical polishing was ended.

[**0054**] When the pillar **911** was not formed unlike the prior art, the polishing rates are different at the portion near the center of the memory mat portion and the portion near the outer periphery so that the polishing rate of the portion near the center of the memory mat portion becomes large as compared with the polishing rate of the portion near the outer periphery. When the sample is chemically mechanically polished until the silicon nitride film **903** serving as the polishing stopper is exposed under the condition that the pillar **911** is not formed, the film thickness of the silicon nitride film **903** serving as the polishing stopper cannot be increased as mentioned before. Therefore, if the sample is polished until the silicon nitride film **903** on the active region near the outer periphery is exposed, then the silicon nitride film **903** and the silicon oxide film **902** are both polished in the active region near the center and the silicon substrate **901** is exposed. Also, if the polishing is stopped at the time point in which the silicon nitride film **903** on the active region near the center is exposed in order to prevent the silicon substrate **901** from being exposed, then the silicon nitride film **903** near the outer periphery cannot be exposed and the element cannot be formed in the active region near the outer periphery in the later process.

[**0055**] When the insulating films **906**, **907** on the active region are chemically mechanically polished until the silicon nitride film **903** on the active region is exposed (the above-mentioned second feature) like the inventive example 7, if the pillar **911** of the insulating film is formed on the memory mat portion, then the fluctuation of the polishing rate can be suppressed over the whole region of the memory mat portion. Thus, it becomes possible to execute uniform chemical mechanical polishing. **FIG. 16***b* is a plan view of **FIG. 16***a*, and the cross-sectional structure shown by X-X' in **FIG. 16***b* is **FIG. 16***a*. From the above, at the timing point in which the chemical mechanical polishing is ended, according to the inventive example 7, the silicon nitride film is exposed on the whole active region of the memory mat portion as shown in **FIG. 16***b*.

[**0056**] Incidentally, in **FIG. 16***a*, since the polishing rate of the element isolation insulating film **914** buried in the groove structure **905** is larger than that of the silicon nitride film **903**, the surface of the element isolation insulating film **914** is lower than the surface of the silicon nitride film **903**.

[**0057**] Thereafter, only the silicon nitride film **903** was removed, and a shallow groove element isolation structure was formed in the field region (**FIG. 16***c*). The surface of the element isolation insulating film **914** is constantly made higher than that of the active region **915**. If the surface of the element isolation insulating film **914** is lowered at the end portion of the active region **915**, then this affects electrical characteristics of an element which will be formed on the active region later on. According to the inventive example 7, such problem can be solved completely.

[**0058**] Then, as shown in **FIG. 17***a*, the silicon oxide film **902** of the active region was removed by cleaning and a gate insulating film **1013** made of a silicon oxide film was formed by thermal oxidization. Then, a polycrystalline silicon **1014**

and a silicon nitride film **1015** were deposited by CVD. Incidentally, **FIG. 17***a* shows a portion A of **FIG. 16***a* in an enlarged-scale.

[**0059**] Thereafter, a gate electrode **1014** was formed by patterning a laminated film of the polycrystalline silicon **1014** and the silicon nitride film **1015** according to lithography and dry etching. Incidentally, the gate electrode **1014** should preferably be made low in resistance value. In this case, in **FIG. 17***a*, a metal silicide film or metal film might be formed between the polycrystalline silicon **1014** and the silicon nitride film **1015**, and the gate electrode **1014** might be formed of a laminated film of the polycrystalline silicon and the metal silicide or a laminated film o-f the polycrystalline silicon and the metal. When the gate electrode is small in size, there is used photolithography using KrF or ArF laser beam or electron beam lithography.

[**0060**] Thereafter, as shown in **FIG. 17***b*, a patterned laminated film **1018** was used as a mask and a source-drain region **1020** was formed by adding impurities. Reference numerals **1017**, **1019** denote shallow element isolation structures of the field region. Incidentally, **FIG. 17***b* shows a B portion in **FIG. 17***a* in an enlarged-scale. Further, as shown in **FIG. 17***c*, a silicon nitride film **1021** was formed on the whole of the sample by CVD. By removing the silicon nitride film **1021** with anisotropy etching, the silicon nitride film **1021** was left only in the side wall of the laminated film **1018** and a side wall film **1022** was formed (**FIG. 17***d*).

[**0061**] **FIG. 18***a* is a plan view of **FIG. 17d**. A cross-sectional structure shown by X-X' in **FIG. 18***a* corresponds to **FIG. 17***d*. In **FIG. 18***a*, reference numeral **1017** denotes a silicon oxide film which is the element isolation insulating film in the field region, and reference numeral **1012** denotes a gate electrode whose upper surface and side surface are covered with silicon nitride films **1021**, **1015**.

[**0062**] Thereafter, a silicon oxide film **1023** was deposited so as to fill the space between the gate electrodes **12** by HDP (High Density Plasma). Incidentally, this deposition is not limited to HDP but may be CVD when a heat history or the like is not taken into consideration. Since the gate electrodes **1012** are densely formed in the memory mat portion as compared with the peripheral circuit, as shown in **FIG. 18***b*, the silicon oxide film **1023** was deposited over the whole surface of the memory mat portion in such a manner that its upper surface becomes substantially the same height.

[**0063**] Thereafter, by photolithography/dry etching, as shown in **FIG. 18***c*, a part of the silicon oxide film **1023** of the convex region was removed from the memory mat portion. Similarly to **FIG. 15***a*, also in this case, all silicon oxide films **1023** are not always removed from the memory mat portion but the silicon oxide films were removed while the pillars **1025** were partly left.

[**0064**] This pillar **1025** was formed across a plurality of gate electrodes **1012**, and its shape was optimized by the polishing amount of the chemical mechanical polishing. Also, the layout of the pillar **1025** was a regular repetitive pattern. Further, the layout of the pillar **1025** was determined in such a manner that the volume of the silicon oxide film that should polished in the chemical mechanical polishing and the result which results from adding the volume of the pillar **1025** to the calculated volume of the corner **1024** at the outer periphery of the memory mat portion become equal to each other (**FIG. 18***c*).

[**0065**] **FIG. 19***a* is a plan view in which the pillar **1025** was formed by partly etching the interlayer insulator **1023** on the memory mat portion. A cross-sectional structure shown by X-X' in **FIG. 19***a* corresponds to **FIG. 18***c*.

[**0066**] This sample was chemically mechanically polished (**FIG. 19***b*). In the chemical mechanical polishing, the sample was polished by using a foamed polyurethane pad and ammonium-based fumed silica slurry with a polishing load of 700 g/cm^2 at a revolution rate of a turntable of 20 revolutions/minute (relative velocity: 20 m/minute) during a polishing time of 7 minutes.

[**0067**] In the initial stage of the chemical mechanical polishing, a corner 1024909 and a pillar **1025** which the same in height as the corner were polished initially. In the conventional process in which the pillar **1025** of the insulating film was not formed, a large amount of scratches were produced. However, in the inventive example 7, since the load of the chemical mechanical polishing concentrated in the corner **1024** was dispersed into the pillar **1025**, the amount in which scratches were produced could be suppressed considerably.

[**0068**] The sample was further polished, the end of the polishing was detected in the silicon nitride film **1015** serving as the polishing stopper, and the chemical mechanical polishing was ended.

[**0069**] Considering the process margin of the chemical mechanical polishing, the film thickness of the silicon nitride film **1015** should preferably be made thick. In this case, the silicon oxide film **1023** was insufficiently put into the space between the adjacent gate electrodes **1012** so that the film thickness of the silicon nitride film **1015** cannot be increased. When the sample was chemically mechanically polished under such situation unlike the prior art in which the pillar **1025** was not formed, the polishing rate increased at the portion near the center of the memory mat portion so that the gate electrode **1014** was exposed. According to this inventive example 7, such problem could be solved completely.

[**0070**] Incidentally, in **FIG. 19***b*, since the polishing rate of the silicon oxide film **1023** was larger than that of the silicon nitride film **1015**, the surface of the silicon oxide film **1023** was lower than the surface of the silicon nitride film **1015**.

[**0071**] Thereafter, a silicon oxide film **1029** was deposited by CVD (**FIG. 19***c*). Since a large step difference could be prevented from being produced by the use of the pillar **1025**, large concavities and convexities could be prevented from being produced on the surface of the deposited silicon oxide film **1029**. Therefore, in the following photolithography process, there arises no trouble.

[**0072**] Thereafter, as shown in **FIGS. 20***a* and **20***b*, a pattern of a resist **1030** was used as a mask and a contact hole **1032** was formed by photolithography/dry etching. Further, after the resist **1030** was removed, a polycrystalline silicon in which impurities were heavily doped was deposited so as to fill the contact hole **1032** by CVD, and a plug **1033** was formed by chemically mechanically polishing the sample (**FIG. 20***c*). Thereafter, there was formed a metal interconnection **1034** as a data line (**FIG. 20***d*).

[**0073**] Subsequently, as shown in **FIG. 21***a*, a silicon oxide film **1035** containing boric acid and phosphorous was

deposited and heat-treated at high temperature, thereby resulting in the surface being made smooth. In this case, the silicon oxide film **1035** could be deposited by well-known CVD and the surface could be made smooth by chemical mechanical polishing. Then, a through-hole **1036** was formed by photolithography/dry etching (**FIG. 21***b*). Further, a polycrystalline silicon film in which impurities were heavily doped was deposited so as to fill the through-hole **1036**, and a plug **1037** was formed by making the surface smooth by chemical mechanical polishing. Thereafter, a polycrystalline silicon film **1038** in which impurities were heavily doped and a silicon oxide film **1039** were deposited continuously (**FIG. 21***c*).

[**0074**] After the laminated film comprising the polycrystalline silicon film **1038** and the silicon oxide film **1038** was patterned in accordance with the plan shape of the capacitor, a polycrystalline silicon **1043** in which impurities were heavily doped was deposited (**FIG. 22***a*). Then, the polycrystalline silicon **1043** was left on the side wall of the patterned laminated film by anisotropy etching. Further, by removing the above-mentioned silicon oxide film **1039**, there was formed a crown-like lower electrode **1045** comprising the polycrystalline silicon films **1038**, **1043** (**FIG. 22***c*).

[**0075**] Then, a plate electrode **1047** comprising a dielectric film **1046** and a tungsten film was deposited and then patterned (**FIG. 23***a*). Here, as the dielectric film **1046**, a silicon nitride film, tantalum pentaoxide having a large dielectric constant as compared with that of the silicon oxide film should be preferable. Further, the film thickness of the dielectric film **1046** that was converted into the film thickness of the oxide film should preferably made less than 3 nano-meter. While the polycrystalline silicon in which impurities were heavily doped as used as the crown-like lower electrode **1045**, it is possible to use a high-melting point metal film of low resistance value such as tungsten, titanium nitride film or the like. In the end, there were formed a silicon oxide film **1048** as an interlayer insulator and a metal interconnection **1049** (**FIG. 23***b*).

[**0076**] While the DRAM using the crown-like capacitor was described so far in the above-mentioned examples, it is needless to say that the present invention may be applied to a DRAM having a stack-type structure using a high-dielectric film **1052** shown in **FIG. 25**. In **FIG. 25, a** plug **1050** connected to a lower electrode **1053** and a lower electrode **1051** of a capacitor were formed of titanium nitride. As the material of the high-dielectric film **1052**, there may be used well-known high-dielectric film such as $SrTiO_3$ and (Ba, Sr)TiO_3 film (BST film) and further a ferroelectric film such as PZT.

[**0077**] Incidentally, in addition to the techniques enumerated in the conventional techniques, with respect to the technique in which the film formed on the dense uneven pattern was partly removed and the sample was chemically mechanically polished, there are techniques disclosed in JP-A-10-13521 (laid-open at May 22, 1998), JP-A-10-321625 (laid-open at Dec. 4, 1998) and JP-A10-321628 (laid-open at Dec. 4, 1998). Of these techniques disclosed in JP-A-10-321625 and JP-A-10-321628, the chemical mechanical polishing executed up to the convex portion surface of the uneven pattern of the under layer was not taken into consideration. Also, with respect to the technique disclosed in JP-A-10-135211, the polishing stopper formed on the convex portion surface of the uneven pattern of the under layer was not taken into consideration.

[**0078**] According to the above-mentioned inventive examples, the film thickness of the silicon nitride film used as the polishing stopper on the active region can be reduced so that the electrical element isolation characteristic of the field region can be improved. Since the concentration of the load of the chemical mechanical polishing can be dispersed, it is possible to suppress the occurrence of scratches considerably. Further, the silicon substrate and the gate electrode can be prevented from being exposed near the central portion of the memory mat and the insulating film on the silicon nitride film can be prevented from being left near the outer periphery upon chemical mechanical polishing. Thus, it is possible to form elements having uniform electrical characteristics on all active regions of the memory mat portion.

[**0079**] When the pillars are formed, only the pattern of the mask used in the etching of the conventional insulating film may be changed so that photolithography and other process need not be added, thereby making it possible to prevent the cost from increasing.

[**0080**] Incidentally, while the DRAM was so far described as the example in the inventive example 7, the present invention is not limited to the DRAM and may be very effectively applied to a SRAM (Static Random Access Memory) and a system LSI (Large Scale Integrated circuit) having a flash memory or DRAM mounted thereon.

[**0081**] Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments and that various changes and modifications could be effected therein by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

What is claimed is:

1. A method of manufacturing semiconductor devices having a memory mat region, comprising the steps of:

depositing a polishing stopper film on a semiconductor substrate;

forming grooves in a field region by etching said polishing stopper film and said semiconductor substrate;

depositing an insulating film so as to fill said grooves;

partially removing said insulating film from said memory mat region by etching; and

chemically mechanically polishing said insulating film until said polishing stopper film is exposed.

2. A method according to claim 1, wherein corners of said insulating film surrounding said memory mat region and a plurality of pillars of said insulating film are formed within said memory mat region in the process in which said insulating film is partially removed by etching.

3. A method according to claim 2, wherein said corners and said pillars are formed in such a manner that a volume of said insulating film that should be polished in the outside of said memory mat region and volumes of said corners and said pillars become equal to each other.

4. A method according to claim 1, wherein said polishing stopper film is a silicon nitride film.

5. A method according to claim 1, wherein said insulating film is a silicon oxide film.

6. A method according to claim 5, wherein said insulating film is deposited by CDV using O_3—TEOS.

7. A method according to claim 5, wherein said insulating film is deposited by HDP.

8. A semiconductor device manufacturing method comprising the steps of:

forming a thermal oxide film on a semiconductor substrate surface;

depositing a silicon nitride film on said thermal oxide film;

patterning said silicon nitride film in accordance with an active region;

etching said thermal oxide film and said silicon substrate with said patterned silicon nitride film used as a mask to form grooves in a field region;

depositing an insulating film;

partly etching said insulating film within said memory mat region so as to leave pillars of said insulating film in said memory mat region;

exposing said patterned silicon nitride film by chemical mechanical polishing;

removing said exposed silicon nitride film; and

forming an element on an active region by removing said thermal oxide film from said active region.

9. A method according to claim 8, wherein said insulating film is a silicon oxide film.

10. A method according to claim 9, wherein said insulating film is deposited by CVD using O_3—TEOS.

11. A method according to claim 9, wherein said insulating film is deposited by HDP.

12. A method of manufacturing a semiconductor device having a memory mat region, comprising the steps of:

forming a gate insulating film on an active region of a semiconductor substrate;

depositing a material film of a gate electrode on said semiconductor substrate;

depositing a polishing stopper film on said material film;

forming a plurality of gate electrodes by patterning a laminated film of said material film and said polishing stopper film;

forming source-drain regions on both sides of said gate electrode of said active region;

forming side wall films on side surfaces of said gate electrode;

depositing an interlayer insulator so as to fill a space between said gate electrodes;

partly removing said interlayer insulator from said memory mat region by etching; and

chemically mechanically polishing said interlayer insulator until said polishing stopper film is exposed.

13. A method according to claim 12, wherein corners of said insulating film surrounding said memory mat region and a plurality of pillars of said insulating film are formed within said memory mat region in the process in which said insulating film is partially removed by etching.

14. A method according to claim 13, wherein said corners and said pillars are formed in such a manner that a volume of said insulating film that should be polished in the outside of said memory mat region and volumes of said corners and said pillars become equal to each other.

15. A method according to claim 12, wherein the material film of said gate electrode is any one of a laminated film of a polycrystalline silicon film, a polycrystalline silicon film and a metal silicide film or a laminated film of a polycrystalline silicon film and a metal film.

16. A method according to claim 12, wherein said polishing stopper film is a silicon nitride film.

17. A method according to claim 12, wherein said insulating film is a silicon oxide film.

18. A method according to claim 17, wherein said insulating film is deposited by CVD using O_3—TEOS.

19. A method according to claim 17, wherein said insulating film is deposited by HDP.

20. A method of manufacturing a DRAM having a memory mat portion and a peripheral circuit portion, comprising the steps of:

forming a thermal oxide film on a semiconductor substrate surface;

depositing a first nitride film on said thermal oxide film;

patterning said first nitride film in accordance with an active region;

etching said thermal oxide film and said silicon substrate with said patterned first silicon nitride film used as a mask to form grooves in a field region;

depositing a first insulating film;

partly etching said first insulating film formed on said memory mat portion in such a manner that a plurality of pillars of said first insulating film are left within said memory mat portion;

exposing said patterned first silicon nitride film by chemical mechanical polishing; and

removing said exposed first silicon nitride film.

21. A method according to claim 20, wherein a volume of said first insulating film in said peripheral circuit portion and a volume of said first insulating film that should be polished in said memory mat portion become equal to each other in the process in which said first insulating film is etched partly.

22. A method according to claim 20, further comprising the steps of:

forming a gate insulating film in said active region by removing said thermal oxide film from said active region;

depositing a gate electrode material film on said semiconductor substrate;

depositing a second nitride film on said material film;

forming a plurality of gate electrodes by patterning a laminated film of said material film and said second

silicon nitride film in such a manner that two gate electrodes cross at least one active region of said memory mat portion;

forming source-drain regions on both sides of said gate electrode of said active region;

depositing a third silicon nitride film on said semiconductor substrate;

leaving a third silicon nitride film on a side surface of said gate electrode by anisotropy-etching said third silicon nitride film;

depositing a second insulating film;

partly etching said second insulating film on said memory mat portion in such a manner that a plurality of pillars of said second insulating film are left within said memory mat portion;

chemically mechanically polishing said interlayer insulator until said second silicon nitride film on said gate electrode is exposed;

depositing a third insulating film;

forming a plurality of first plugs penetrating said second and third insulating films and which are connected to a source-drain region formed between two gate electrodes of each active region of said memory mat portion;

forming a metal interconnection connected to said first plugs;

depositing a fourth insulating film;

forming a plurality of second plugs penetrating said second, third and fourth insulating films and which are connected to each source-drain region formed on the outside of two gate electrodes of each active region of said memory mat portion; and

forming a capacitor connected to said second plugs.

23. A method of manufacturing semiconductor devices having a wide active region and a narrow active region, comprising the steps of:

depositing a silicon nitride film on a semiconductor substrate;

forming grooves by etching said silicon nitride film of a field region and said semiconductor substrate;

depositing an insulating film so as to fill said grooves;

partly removing said insulating film from said wide active region by etching; and

chemically mechanically polishing said insulating film until said silicon nitride film is exposed.

24. A method according to claim 23, wherein said insulating film is a silicon oxide film.

25. A method of manufacturing semiconductor devices having a wide active region and a narrow active region, comprising the steps of:

forming a first thermal oxide film on a semiconductor substrate surface;

depositing a first silicon nitride film on said first thermal oxide film;

forming grooves by etching said first silicon nitride film of a field region, said first thermal oxide film and said semiconductor substrate;

forming a second thermal oxide film within said grooves;

depositing a silicon oxide film;

depositing a second silicon nitride film;

partly etching said silicon oxide film and said silicon nitride film on said wide active region in such a manner that a pillar of a laminated layer of said silicon oxide film and said second silicon nitride film are left within said wide active region;

chemically mechanically polishing said silicon oxide film until said first silicon nitride film is exposed; and

removing said exposed first silicon nitride film.

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