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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11C 7/00	A1	(11) International Publication Number: WO 98/28745 (43) International Publication Date: 2 July 1998 (02.07.98)

(21) International Application Number: PCT/US97/19209

(22) International Filing Date: 23 October 1997 (23.10.97)

(30) Priority Data:
08/770,397 20 December 1996 (20.12.96) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: HURTER, Andrew, J.; 5013 El Don Drive, Rocklin, CA 95677 (US). DOLLER, Edward, M.; 33305 Bellingham Place, El Dorado Hills, CA 95762 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

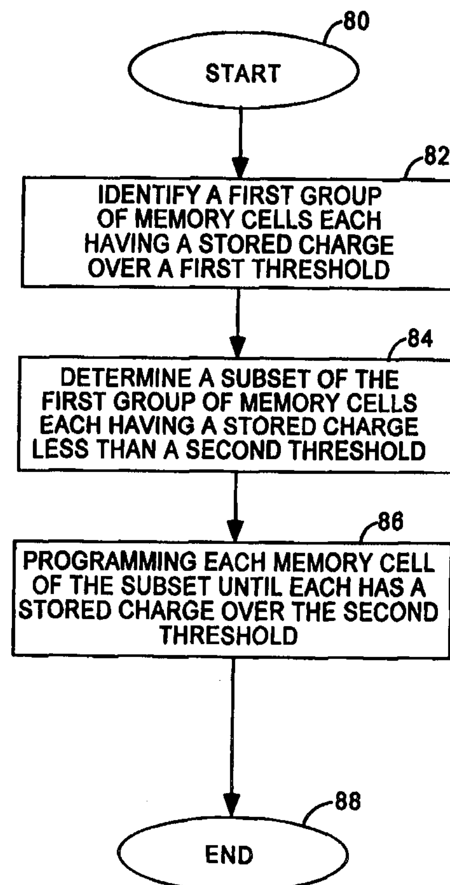
(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: NONVOLATILE WRITEABLE MEMORY WITH FAST PROGRAMMING CAPABILITY

(57) Abstract

A method and apparatus provides capability for fast programming of a nonvolatile writeable memory. One or more memory cells of a block of memory cells of the nonvolatile writeable memory is programmed using no more than one program pulse. The memory cells of the block of memory cells having a threshold voltage in an intermediate region (62) below a programmed reference level (54) and above an erase reference level (50) are identified. These identified memory cells are programmed with one or more program pulses to raise the threshold voltage of the corresponding memory cell up to the programmed reference level (52).



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NONVOLATILE WRITEABLE MEMORY WITH FAST PROGRAMMING CAPABILITY

FIELD OF THE INVENTION

The present invention relates to memory devices. More particularly, this invention relates to programming of a nonvolatile writeable memory.

BACKGROUND OF THE INVENTION

Many computing systems, such as personal computers, automotive and airplane control, cellular phones, digital cameras, and hand-held communication devices, use nonvolatile writeable memories to store either data or code, or both. Such nonvolatile writeable memories include Electrically Erasable Programmable Read-Only Memories ("EEPROMs") and flash Erasable and Electrically Programmable Read-Only Memories ("flash EPROMs" or "flash memories").

Non-volatility is advantageous for allowing the computing system to retain its data and code when power is removed from the computing system. Thus, if the system is turned off or if there is a power failure, there is no loss of code or data.

Writability, or programmability, enables the computing system to be reprogrammed. This is useful, for example, for upgrading the system, or for correcting bugs in the code.

Figure 1 is a block diagram of a prior art nonvolatile writeable memory device 20. Memory device 20 stores data using nonvolatile memory cells within memory array 22. The threshold voltages of the nonvolatile memory cells can be altered during programming, thus permitting storage of analog voltage levels, as is well known in the art. Memory array 22 may include any type of memory cell with programmable threshold voltages, such as memory cells with trapping dielectric or floating gates. In one embodiment, memory array 22 is comprised of flash memory cells.

Referring to Figure 1, Vpp is the erase/program power supply for memory device 20. In the absence of a high voltage level on the memory cells, memory device 20 acts as a read only memory. The data stored at an address indicated by address lines 24 is read from memory array 22 and is output to the external user via data lines 26.

X decoder 28 selects the appropriate row within memory array 22 in response to address signals applied to address lines 24. For this reason, X decoder 28 is also called row decoder 28. Similarly, Y decoder 30 selects the appropriate column within memory array 20 in response to address signals from address lines 24. Because of its function, Y decoder 30 is also called column decoder 30.

Data output from memory array 22 is coupled to Y decoder 30, which passes the data on to sensing circuitry 32. Sensing circuitry 32 determines the state of data presented to it using reference cell array 34. Sensing circuitry 32 then passes the results of its analysis back to Y decoder 30.

In one embodiment of memory device 20, control engine 36 controls the erasure and programming of memory array 22. In another embodiment, control engine 36 also controls the programming of multilevel cells. A multilevel cells is a cell that can store three or more charge states, as is well-known in the prior art. In one embodiment, control engine 36 includes a processor or microcontroller that is controlled by microcode stored in on-chip memory. However, the particular implementation of control engine 36 does not affect the present method of programming memory cells.

Control engine 36 manages memory array 22 via control of row decoder 28, column decoder 30, sensing circuitry 32, reference cell array 34 and voltage switch 38. Voltage switch 38 controls the various voltage levels necessary to read, program and erase memory array 22. Vcc is the device power supply and Vss is ground. Vpp is the program/erase voltage used to program or erase data stored within memory array 22. Vpp may be externally supplied or internally generated.

User commands for reading, erasure, and programming are communicated to control engine 36 via command interface 40. The external user issues commands to command interface 40 via three control pins: output enable OEB, write enable WEB and chip enable CEB.

Figure 2 is a diagram showing a prior art memory cell of the memory array 22 in terms of a threshold voltage, Vt. The state of the memory cell may be defined in terms of the memory cell threshold voltage level or the drain current. Memory cell threshold voltage Vt, and drain current Id are approximately related to each other by the expression:

$Id \propto Gm \times (Vg - Vt)$ for $Vd > Vg - Vt$, where

Gm is the transconductance of the memory cell;
Vg is the memory cell gate voltage;
Vd is the memory cell drain voltage; and
Vt is the memory cell threshold voltage.

The memory cell has associated with it, a programmed-reference level and an erased-reference level. If the charge stored on the floating gate of the memory cell corresponds to a Vt below the erased reference level, then the memory cell is defined to be in an "erased" state. If the charge stored on the floating gate of the memory cell corresponds to a Vt above the programmed-reference level, then the memory cell is defined to be in a "programmed" state.

A read reference level is typically used to read from the memory cell. If the Vt of the memory cell is higher than the read reference level, then the read indicates the memory cell is in a "programmed" state. If the Vt is below the erased reference voltage, then the read indicates the memory cell is in an "erased" state.

A memory cell is typically programmed by applying a program pulse to store charge on the floating gate of the memory cell. A program verify cycle is then performed to ensure that the Vt of the memory cell is above the programmed reference level.

If the Vt is not above the programmed reference level, then one or more subsequent program pulses are applied to the memory cell, as needed, until the Vt of the memory cell is above the programmed reference level.

Because the number of program pulses required to ensure that the Vt of the memory cell is above the programmed reference level is indeterminate, the memory has a long program latency time. Thus, the memory is not able to store data at a high transfer rate because the memory cannot guarantee that it will be able to store data by using a predetermined number of program pulses.

<u>SUMMARY OF THE INVENTION</u>

A method and apparatus for programming a nonvolatile writeable memory is described. One or more memory cells of a block of memory cells of the nonvolatile writeable memory is programmed using no more than one program pulse. The memory cells of the block of memory cells having a

threshold voltage in an intermediate region below a programmed reference level and above an erased reference level are identified. These identified memory cells are programmed with one or more program pulses to raise the threshold voltage of the corresponding memory cell up to the programmed reference level.

These and other advantages of the present invention are fully described in the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art nonvolatile writeable memory device 20.

Figure 2 is a diagram showing a prior art memory cell of the memory array 22 in terms of a threshold voltage, Vt.

Figure 3 is a diagram showing the different charge regions of a memory cell according to one embodiment of the present invention.

Figure 4 shows a flow chart illustrating the steps taken by the memory in identifying memory cells in the intermediate region 62 (Fig. 3)

Figure 5 shows a representative sense amp which is used to determine the Vt of a memory cell.

Figure 6 shows the results of a read from a first group of memory cells at the programmed reference level being compared with the results of a read from the same first group of memory cells at the nominally programmed reference level.

Figure 7 illustrates a memory device having an external fast programming pin.

DETAILED DESCRIPTION

A method and apparatus for allowing the fast programming of memory cells of a memory array is described. The memory cells are programmed with a single program pulse. This allows the memory to accept data at a rate corresponding to the latency of the single program pulse. Subsequently, the memory cells that were programmed with the single program pulse are checked to determine if any of the memory cells have a threshold voltage over an erased reference level but below a programmed reference level. Any memory cell found in this intermediate region is provided with one or more program pulses until each memory cell has a threshold voltage above the programmed reference

level. The invention may be expanded to provide an initial program cycle of any number of program pulses, as long as the initial program cycle has a predefined latency time.

Figure 3 is a diagram showing the different charge regions according to the present invention. If a memory cell has a Vt above a programmed reference level 50, then the memory cell is in a programmed state 60. If the memory cell has a Vt below the erased reference level 54, then the memory cell is in an erased state 66. The region between the programmed reference level 50 and the erased reference level 54 is comprised of an intermediate region 62 and a guardband region 64. The read reference level typically resides within the intermediate region 62.

After the initial program cycle, the invention searches for memory cells having a Vt within the intermediate region, as will be explained in further detail. Once these memory cells have been identified, then each of these memory cells is programmed to raise the Vt of that memory cell up to the programmed reference level. In one embodiment, the programmed reference level is approximately 5.3 V, and the erased reference level is approximately 3.1 V.

Figure 4 shows a flow chart illustrating the steps taken by the memory in identifying memory cells in the intermediate region 62 (Fig. 3). The flow chart starts at a block 80, from which it continues at block 82. At block 82, a first group of memory cells each having a stored charge over a first reference level is identified. Operation continues at block 84, at which a subset of the first group of memory cells is determined, wherein the subset of the first group of memory cells has a stored charge less than a second reference level. At block 86, each of the memory cells of the subset is programmed until each memory cell has a stored charge over the second reference level. Operation terminates at block 88.

Alternatively, instead of checking an entire group for memory cells having a charge state within the intermediate region and programming the identified memory cells, the process may be performed successively on each memory cell to determine whether that particular memory cell needs to be programmed before checking the next memory cell.

Figure 5 shows a representative sense amp which is used to determine the Vt of a memory cell. Each memory cell of the memory array is compared against a reference cell to determine whether the Vt of the memory cell is higher

or lower than that of the reference cell, as is well-known in the prior art. In a first embodiment, a "nominally programmed" reference cell is created corresponding to the erased reference level of the memory cell plus a guardband 64. This nominally programmed reference level is compared against each memory cell to determine whether any of the memory cells need to be programmed up to the programmed state 60.

In one embodiment, a guardband of approximately 400 mV was experimentally determined to be a sufficient buffer to prevent erased memory cells from erroneously being determined to be in the intermediate region yet still able to capture any "nominally programmed" memory cells.

In another embodiment, either a read reference cell or an erased reference cell is used to emulate a new nominally programmed reference cell.

Referring to Figure 5, the gate voltage of the reference circuit Vgr can be modified from the gate voltage of the memory cell Vga in order to emulate a reference circuit corresponding to a different Vt by the formula:

For example, Vgr = Vga - guardband, for the erased reference cell. Thus, if Vga is 5.0 V and the guardband is 400 mV, then Vgr is 4.6 V.

Figure 6 shows the results of a read from a first group of memory cells at the programmed reference being compared with the results of a read from the same first group of memory cells at the nominally programmed reference. In this case, the comparison is done via an XOR gate. Any differences between the two results indicate that at least one of the memory cells has fallen into the intermediate region and is not sufficiently programmed. The indicated memory cell(s) is then programmed to the programmed reference level.

Figure 7 illustrates a memory device having an external fast programming pin. When the fast programming pin is asserted then the memory performs in a fast programming mode of operation. The memory device may, either in addition to or alternatively, allow a fast programming command to be written to the command interface 140 to initiate the fast programming mode.

In one embodiment, the memory has a fast programming mode and a standard programming mode. In the standard programming mode, the program verify is used after each write to a memory cell to guarantee that the threshold voltage of the memory cell is above the programmed reference level. In the fast programming mode, the memory uses the initial program cycle to quickly

program a block of memory cells, where a block can be any number of memory cells. Subsequently, for example, upon exiting the fast programming mode, the memory checks the block of memory for memory cells in the intermediate region. The memory cells in the intermediate region are programmed with one or more program pulses until they have a threshold voltage above the programmed reference level. In one embodiment, the memory check is automatically performed when the memory is idle.

In another embodiment, a separate command or pin is used to search for memory cells in the intermediate region, as is described in copending application Serial No. ___________, entitled "Method for Improved Data Retention in a Nonvolatile Writeable Memory," which is assigned to the common assignee of this application. Thus, the checking for memory cells having threshold voltages in the intermediate region can be deferred until it is convenient to do the checking.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

WHAT IS CLAIMED IS:

1. A method of programming a nonvolatile writeable memory, the method comprising the steps of:

(a) programming one or more memory cells of a block of memory cells of the nonvolatile writeable memory, wherein no more than one program pulse is used to program any one memory cell;

(b) identifying memory cells of the block of memory cells having a threshold voltage in an intermediate region below a programmed reference level and above an erased reference level ; and

(c) providing one or more program pulses to each of the memory cells identified in the step (b) to raise the threshold voltage up to the programmed reference level.

2. The method of claim 1, wherein the intermediate region is above the erased reference level by approximately 300 mV to 500 mV, wherein erased memory cells have a threshold voltage below the erased reference level.

3. In a nonvolatile writeable memory having a program verify capability, a method of programming the nonvolatile writeable memory comprising the steps of:

(a) programming a block of memory cells of the nonvolatile writeable memory using an initial program cycle having a predetermined latency;

(b) checking each of the block of memory cells to determine whether any of the memory cells have a threshold voltage in an intermediate region above an erased reference level but below a programmed reference level; and

(c) programming each of the block of memory cells found in the intermediate region up to the programmed reference level.

4. In a nonvolatile writeable memory having a program verify capability, a method of programming the nonvolatile writeable memory comprising the steps of:

(a) programming a block of memory cells of the nonvolatile writeable memory without using the program verify to determine whether each memory cell was programmed to a programmed reference level ;

(b) checking each of the block of memory cells to determine whether any of the memory cells were programmed above an erased reference level but not programmed above the programmed reference level ; and

(c) programming each of the block of memory cells found in the step (b) to the programmed reference level.

5. The method of claim 4, wherein the nonvolatile writeable memory performs the steps (a) - (c) responsive to a signal provided to a pin of the nonvolatile writeable memory.

6. The method of claim 4, wherein the nonvolatile writeable memory performs the steps (a) - (c) responsive to a command written to the nonvolatile writeable memory.

7. The method of claim 4, wherein the step (a) is performed on all of the memory cells of the nonvolatile writeable memory prior to step (b) being performed.

8. In a nonvolatile writeable memory having program verify capability, a method of programming the nonvolatile writeable memory comprising the steps of:

(a) programming a block of memory cells of the nonvolatile writeable memory at a first data rate, wherein the first data rate allows no more than one program pulse to be used to program a memory cell of the nonvolatile writeable memory;

(b) identifying a subset of the memory cells programmed in the step (a) that have a threshold voltage above a fast programming reference level but below a programmed reference level, wherein the fast programming reference level corresponds to an erased reference level plus a guardband; and

(c) programming the memory cells identified in the step (b) until they are above the programmed reference level.

9. The method of claim 8 wherein the guardband is approximately 300 mV to 500 mV.

10. A nonvolatile writeable memory capable of being programmed in a first mode and a second mode, the nonvolatile writeable memory comprising:

a memory array; and

a control engine, wherein in the first mode, the control engine programs the memory array one memory cell at a time, wherein after each memory cell is programmed it is checked to determine whether it is programmed above a programmed reference level, and if it is not programmed over the programmed reference level, then it is provided with one or more program pulses until it has a threshold voltage over the programmed reference level, and wherein in the second mode, the control engine programs a block of memory cells of the memory array, wherein each memory cell of the block of memory cells is programmed with a single program pulse, and subsequently if any of the memory cells that was programmed with the single program pulse has a threshold voltage below the programmed reference level, that memory cell is programmed with one or more program pulses until it has a threshold voltage over the programmed reference level.

11. The nonvolatile writeable memory of claim 10 further comprising:

a command interface capable of decoding a fast program command that signals the control engine to program the memory array using the second mode.

12. The nonvolatile writeable memory of claim 10 further comprising:

a fast program pin, wherein a signal provided via the fast program pin indicates to the control engine to program the memory array using the second mode.

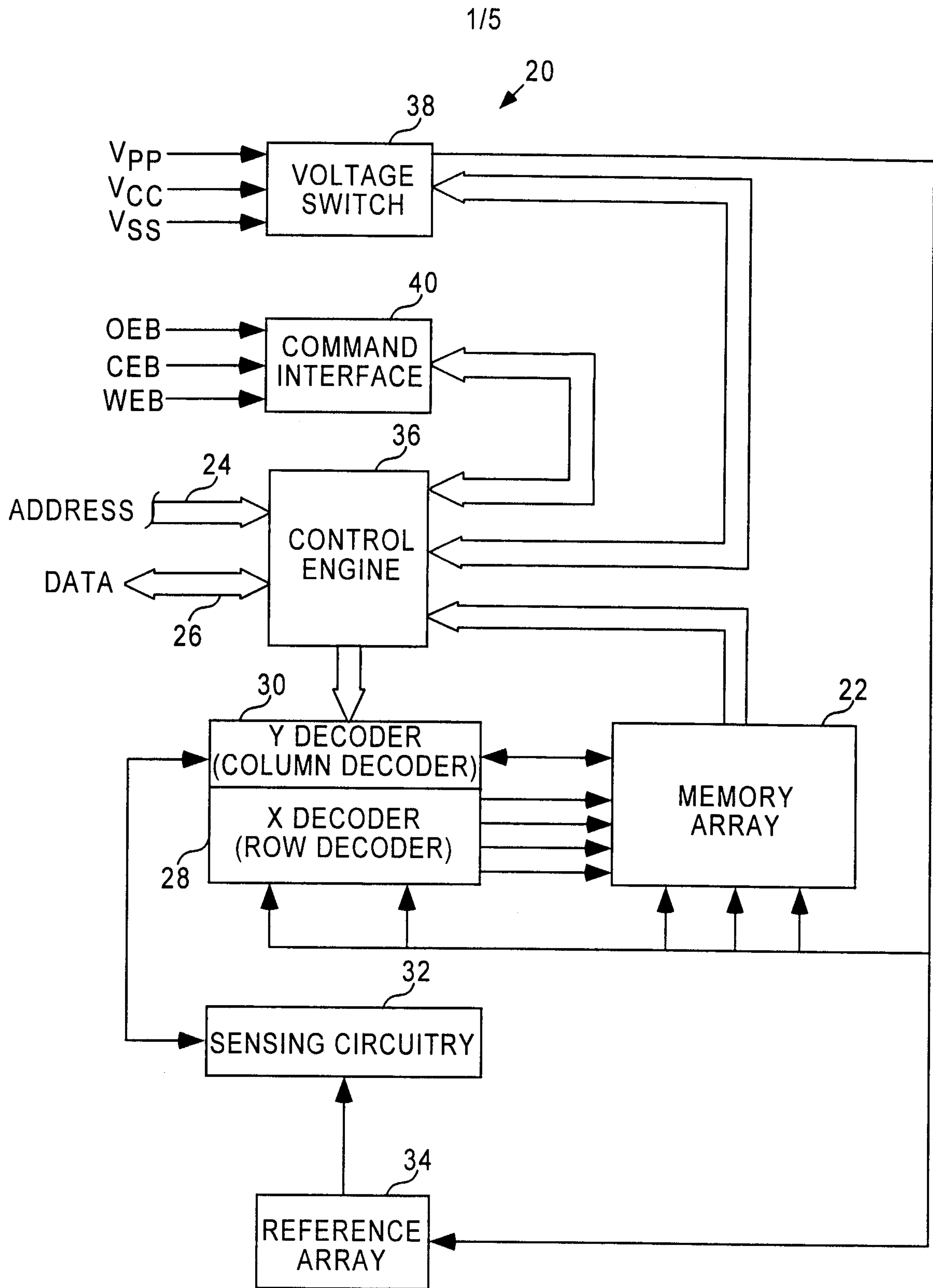

FIGURE 1 (PRIOR ART)

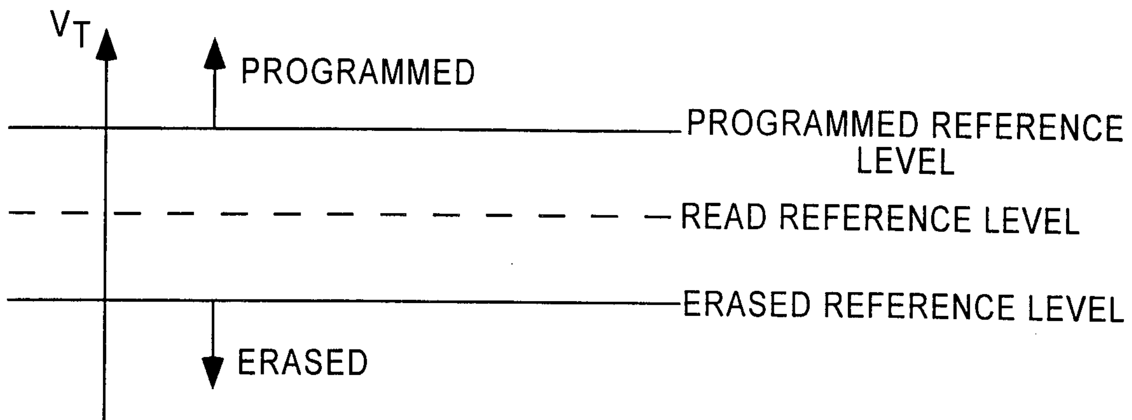

FIGURE 2 (PRIOR ART)

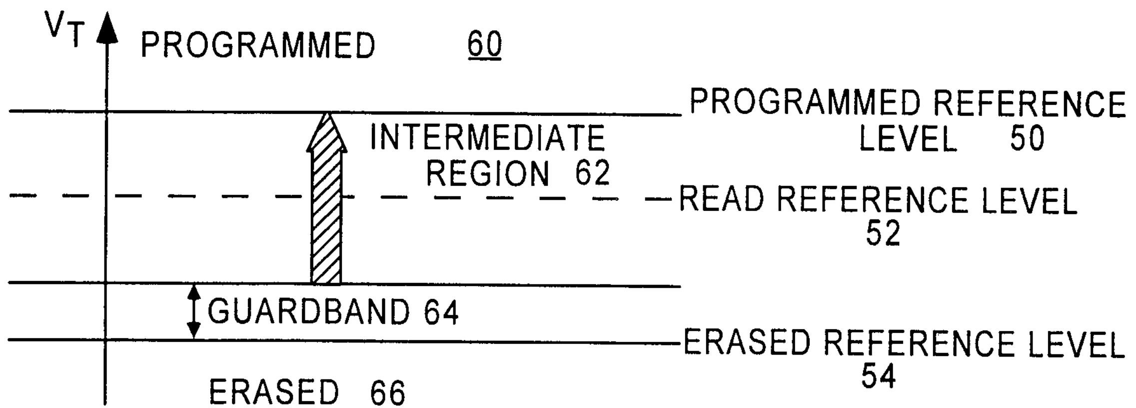

FIGURE 3

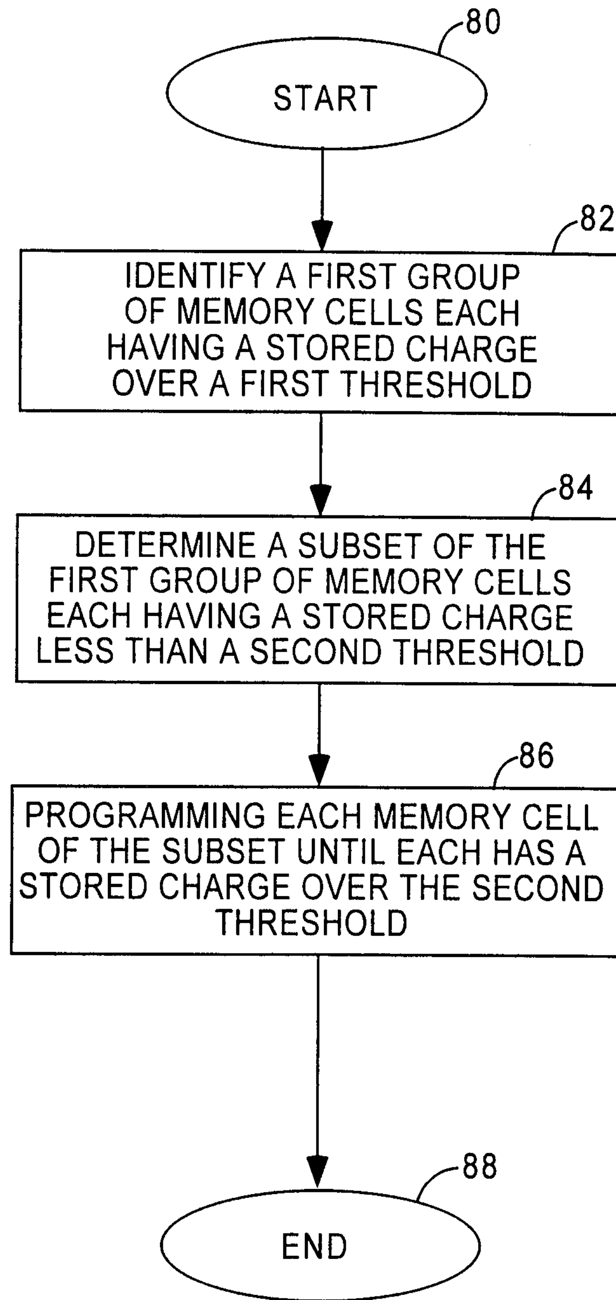

FIGURE 4

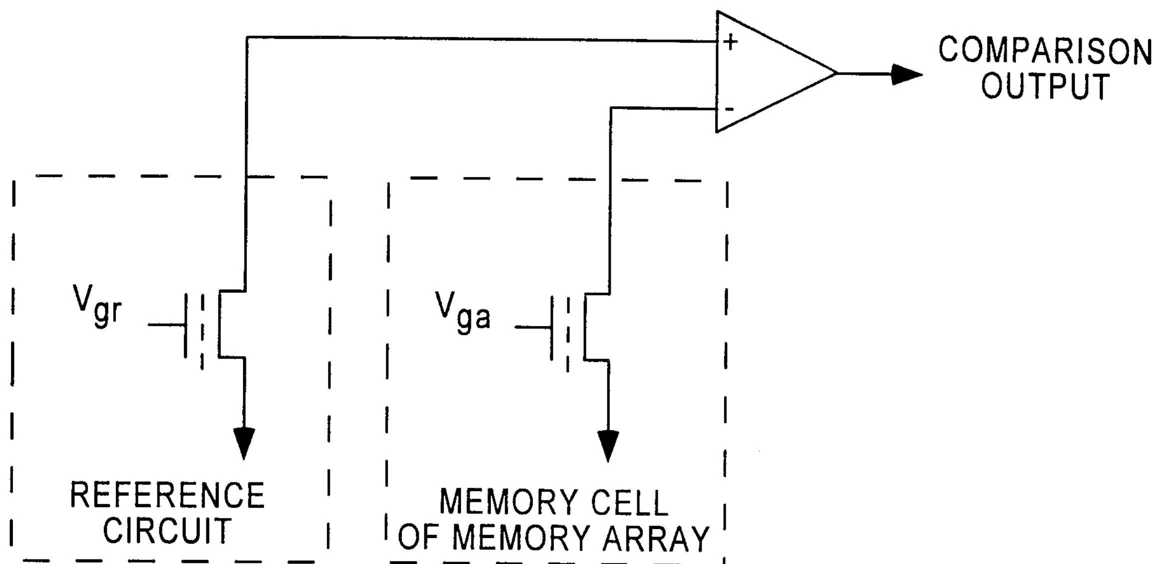

FIGURE 5

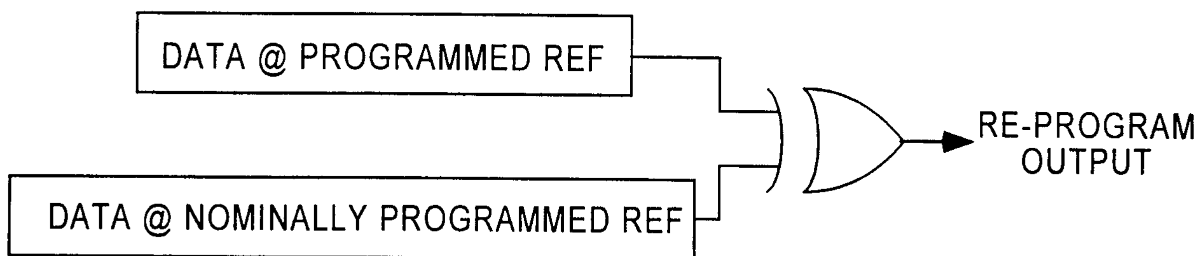

FIGURE 6

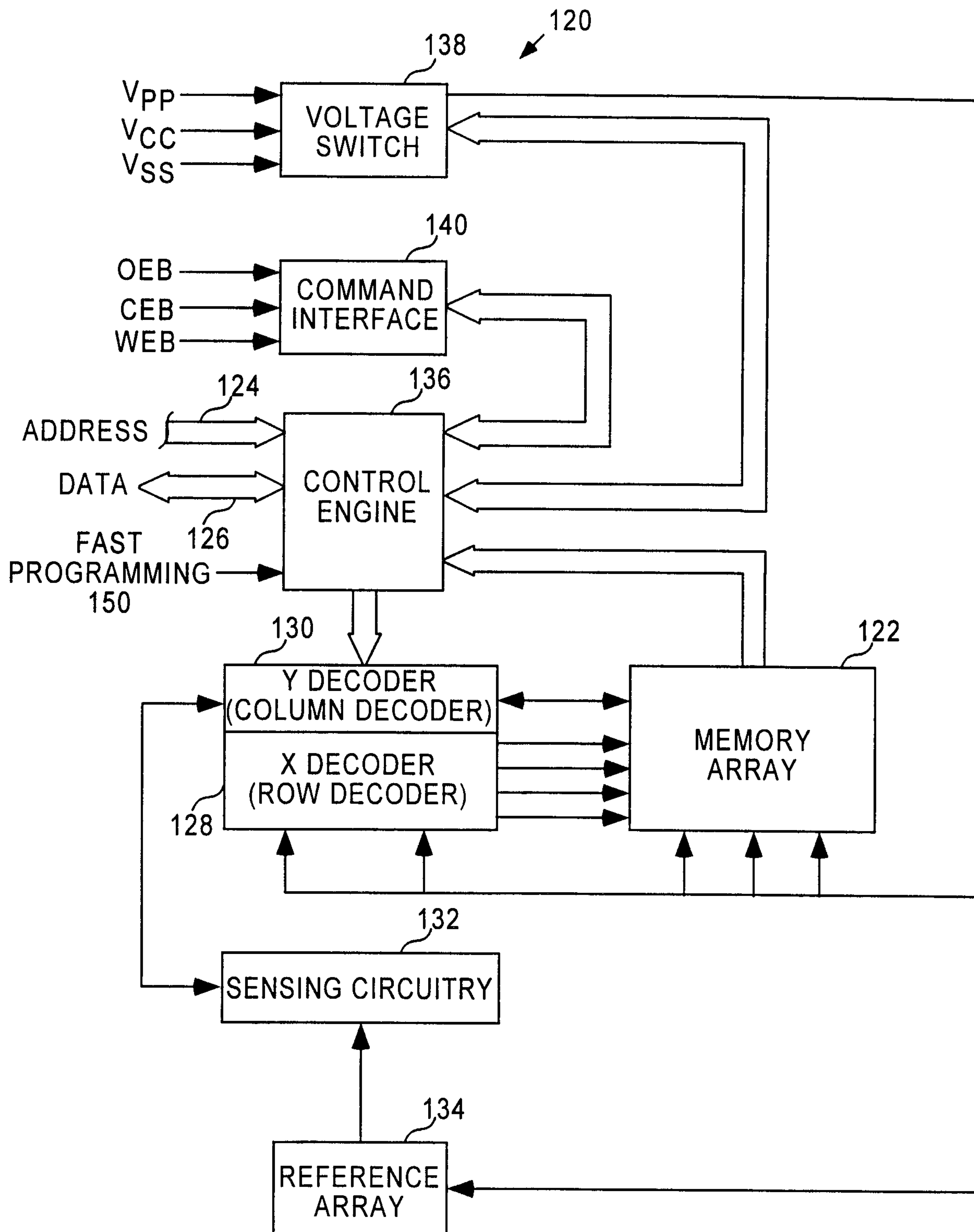

FIGURE 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/19209

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G11C 7/00
US CL :365/185.2, 185.19, 185.24
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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U.S. : 365/185.2, 185.19, 185.24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS, MAYA

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- Y	US 5,440,505 (FAZIO et al.) 08 August 1995 (08.08.95), col. 6, lines 6-18, col. 8, lines 39+, claim 1, and Fig. 5.	1, and 3-8 --------------- 10
Y	U.S. 4,888,735 (Lee et al.) 19 December 1989 (19.12.89), col. 8, lines 11-12 and Fig.10.	10

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