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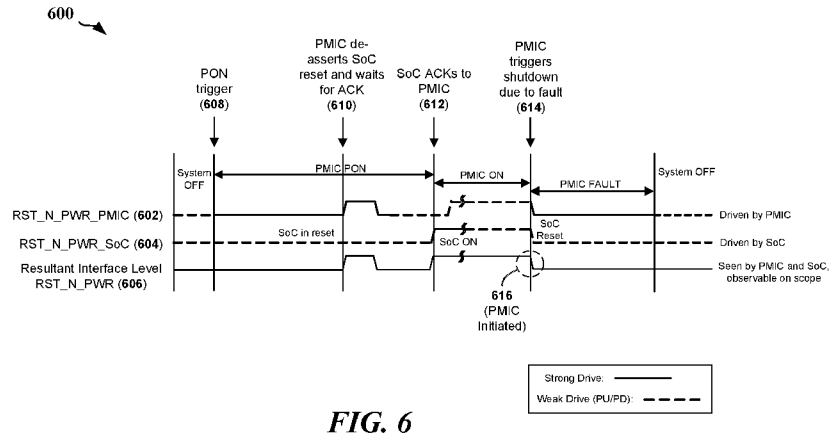

FIG. 6

(57) Abstract: System, methods, and apparatus are described that facilitate signaling between devices over a single bi-directional line. In an example, the apparatus couples a first device to a second device via a single bi-directional line, indicates initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device, and indicates initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device. In another example, a first device initiates a first action, indicates initiation of the first action by generating a first event on a single bi-directional line, and receives an indication of a second action initiated at a second device by observing a second event on the single bi-directional line.

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SINGLE-LINE PMIC-HOST LOW-LEVEL CONTROL INTERFACE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Non-Provisional Application No. 14/966,844 filed in the U.S. Patent and Trademark Office on December 11, 2015, the entire content of which is incorporated herein by reference.

BACKGROUND

Field

[0002] The present disclosure relates generally to high-speed data communications, and more particularly, to systems and methods for signaling between devices using a single bi-directional line.

Background

[0003] High-speed interfaces are frequently used between circuits and components of mobile wireless devices and other complex apparatus. For example, certain devices may include processing, communications, storage and/or display devices that interact with one another through communications links. Some of these devices, including synchronous dynamic random access memory (SDRAM), may be capable of providing or consuming data and control information at processor clock rates. Other devices, such as display controllers, may require variable amounts of data at relatively low video refresh rates.

[0004] Electronic devices (cellular telephones, wireless modems, computers, digital music players, Global Positioning System units, Personal Digital Assistants, gaming devices, etc.) have become a part of everyday life. Small computing devices are now placed in everything from automobiles to housing locks and have increasingly become more complex. For example, many electronic devices have one or more processors that help control the device, as well as a number of digital circuits to support the processor and other parts of the device. An electronic device may include multiple integrated circuits which require board level interconnects for communication and operational coordination. However, the presence of multiple

interconnects causes board level congestion. Accordingly, what is needed is a scheme for improving the pin efficiency of interfaces that allows for an interconnect to be eliminated. Elimination of the interconnect reduces board level congestion as well as preserves pins and associated circuitry for other uses that would otherwise be required for the interconnect.

SUMMARY

[0005] Embodiments disclosed herein provide systems, methods and apparatus for signaling between devices.

[0006] In an aspect of the disclosure, a method of signaling between devices includes coupling a first device to a second device via a single bi-directional line, indicating initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device, and indicating initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device. The method further includes triggering, at the second device, a response to the first action upon receiving the first single transition sent from the first device, and triggering, at the first device, a response to the second action upon receiving the second single transition sent from the second device.

[0007] In an aspect of the disclosure, the first single transition is at least one of a rising edge or a falling edge, and the second single transition is at least one of the rising edge or the falling edge. In a further aspect of the disclosure, the first single transition sent by the first device is a rising edge and the second single transition sent by the second device is a falling edge.

[0008] In an aspect of the disclosure, one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC). In another aspect of the disclosure, the first action is at least one of a reset action or a boot sequence handshake, and the second action is at least one of the reset action or the boot sequence handshake.

[0009] In an aspect of the disclosure, an apparatus for signaling between devices includes a first device, a second device, and a single bi-directional line coupling the first device to the second device. The first device indicates initiation of a first action, initiated at the first device, by sending a first single transition on the single

bi-directional line to the second device, and the second device indicates initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line to the first device. Moreover, the second device triggers a response to the first action upon receiving the first single transition sent from the first device, and the first device triggers a response to the second action upon receiving the second single transition sent from the second device.

[0010] In an aspect of the disclosure, an apparatus for signaling between devices includes means for coupling a first device to a second device via a single bi-directional line, means for indicating initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device, means for indicating initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device, means for triggering, at the second device, a response to the first action upon receiving the first single transition sent from the first device, and means for triggering, at the first device, a response to the second action upon receiving the second single transition sent from the second device.

[0011] In an aspect of the disclosure, a processor-readable storage medium having one or more instructions which, when executed by a processing circuit, cause the processing circuit to couple a first device to a second device via a single bi-directional line, indicate initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device, indicate initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device, trigger, at the second device, a response to the first action upon receiving the first single transition sent from the first device, and trigger, at the first device, a response to the second action upon receiving the second single transition sent from the second device.

[0012] In an aspect of the disclosure, a method of signaling at a first device includes initiating a first action, indicating initiation of the first action by generating a first event on a single bi-directional line, and receiving an indication of a second action initiated at a second device by observing a second event on the single bi-directional line. The method further includes triggering a response to the second action upon

receiving a first transition associated with the second event. In an aspect of the disclosure, the triggered response is variable depending on a state of a system that includes the first device and the second device.

[0013] In an aspect of the disclosure, the first event includes a first number of pulses, and the second event includes a second number of pulses different from the first number. In another aspect of the disclosure, the first event includes a single pulse and the second event includes a double pulse, or the first event includes the double pulse and the second event includes the single pulse. In a further aspect of the disclosure, the first event is differentiated from the second event by at least one of a voltage level, an impedance level, a pulse width, or a number of pulses.

[0014] In an aspect of the disclosure, one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC). In another aspect of the disclosure, the first action is at least one of a reset action or a boot sequence handshake, and the second action is at least one of the reset action or the boot sequence handshake. In a further aspect of the disclosure, the first action and the second action are variable depending on a state of a system that includes the first device and the second device.

[0015] In an aspect of the disclosure, a first device includes a memory and a processing circuit coupled to the memory. The processing circuit is configured to initiate a first action, indicate initiation of the first action by generating a first event on a single bi-directional line, receive an indication of a second action initiated at a second device by observing a second event on the single bi-directional line, and trigger a response to the second action upon receiving a first transition associated with the second event.

[0016] In an aspect of the disclosure, a first device includes means for initiating a first action, means for indicating initiation of the first action by generating a first event on a single bi-directional line, means for receiving an indication of a second action initiated at a second device by observing a second event on the single bi-directional line, and means for triggering a response to the second action upon receiving a first transition associated with the second event.

[0017] In an aspect of the disclosure, a processor-readable storage medium having one or more instructions which, when executed by a processing circuit, cause the processing circuit to initiate a first action, indicate initiation of the first action by

generating a first event on a single bi-directional line, receive an indication of a second action initiated at a second device by observing a second event on the single bi-directional line, and trigger a response to the second action upon receiving a first transition associated with the second event.

[0018] According to aspects of the disclosure, although the systems, methods and/or apparatus for signaling between devices using the single bi-directional signaling were described with respect to only two devices (e.g., first device and second device), the systems, methods, and/or apparatus may implement more than two devices. The manner in which such devices drive the single bi-directional line may be distinguished from each other. In an aspect of the disclosure, each device may be differentiated by generating a signal having a unique number of pulses, e.g., a third device triggers a reset/shutdown procedure or boot sequence handshake by generating three pulses on the single bi-directional line, a fourth device triggers a reset/shutdown procedure or boot sequence handshake by generating four pulses on the single bi-directional line, and so forth. In other aspects of the disclosure, each device may be differentiated by generating a signal having a unique pulse width, a unique voltage level, or a unique impedance level, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 depicts an apparatus for signaling between devices over a single bi-directional line.

[0020] FIG. 2 illustrates a system architecture for an apparatus that facilitates signaling between devices over a single bi-directional line.

[0021] FIG. 3 is a diagram illustrating a low-level interface between a PMIC and a SoC.

[0022] FIG. 4 is a diagram illustrating a timing behavior of low-level control signals.

[0023] FIG. 5 is diagram illustrating a novel low-level interface between a PMIC and a SoC.

[0024] FIG. 6 is a diagram illustrating device behavior during a PMIC-initiated reset/shutdown procedure when implementing bi-directional signaling over a single wire.

[0025] FIG. 7 is a diagram illustrating device behavior during a SoC-initiated reset/shutdown procedure when implementing bi-directional signaling over a single wire.

[0026] FIG. 8 is an illustration of an apparatus configured to support operations related to signaling between devices over a single bi-directional line according to one or more aspects of the disclosure.

[0027] FIG. 9 is a flowchart illustrating a method of signaling between devices over a single bi-directional line according to an aspect of the disclosure.

[0028] FIG. 10 is a flowchart illustrating a method of signaling at a first device over a single bi-directional line according to another aspect of the disclosure.

DETAILED DESCRIPTION

[0029] Various aspects of the disclosure are now described with reference to the drawings. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects. It may be evident, however, that such aspect(s) may be practiced without these specific details.

Overview

[0030] Aspects of the present disclosure relate to a low-level control interface between a power management integrated circuit (PMIC) and an associated host-processor (e.g., system-on-chip (SoC)). In an aspect of the disclosure, the low-level control interface between the PMIC and the SoC typically involves signaling at a very early stage of system boot, or at a later time when dependency on a bus-based control scheme does not guarantee robust system behavior. Examples of such signaling include, but are not limited to, a power-on/reset signal (PON_RESET_N), a watch dog timer input signal (WDT_IN), and a power supply hold signal (PS_HOLD). The low-level control interface may further involve other types of control signals as newer generation systems may have additional low-level signaling requirements.

[0031] In an aspect of the disclosure, the low-level control interface may require one pin for each type of signal communicated. As such, a dedicated control pin must be added to the interface to support each additional type of information to be communicated. However, this approach is problematic as the addition of the dedicated control pins adds to package level cost, and further, may be impermissible due to package-size and cost constraints. The present disclosure addresses the

problems of the multi-pin approach by using a single bi-directional line to facilitate communication of low-level control functions.

Exemplary Operating Environment

[0032] Certain disclosed examples relate to systems and apparatus for signaling between devices over a single bi-directional line.

[0033] Certain aspects of the disclosure may be applicable to communications links deployed between electronic components, which may include subcomponents of devices such as telephones, mobile computing devices, appliances, automobile electronics, avionics systems, etc. Referring to FIG. 1, for example, an apparatus 100 for signaling between devices over a single bi-directional line may include a processing circuit 102 that is configured to control operation of the apparatus 100. The processing circuit 102 may access and execute software applications and control logic circuits and other devices within the apparatus 100. In one example, the apparatus 100 may include a wireless communication device that communicates through a radio frequency (RF) communications transceiver 106 with a radio access network (RAN), a core access network, the Internet and/or another network. The communications transceiver 106 may be operably coupled to a processing circuit 102. The processing circuit 102 may include one or more IC devices, such as an application specific integrated circuit (ASIC) 108. The ASIC 108 may include one or more processing devices, logic circuits, and so on. The processing circuit 102 may include and/or be coupled to processor readable storage 112 that may maintain instructions and data that may be executed by the processing circuit 102. The processing circuit 102 may be controlled by one or more of an operating system and an application programming interface (API) 110 layer that supports and enables execution of software modules residing in the storage 112 of the wireless device. The storage 112 may include read only memory (ROM) or random access memory (RAM), electrically erasable programmable read only memory (EEPROM), a flash memory device, or any memory device that can be used in processing systems and computing platforms. The processing circuit 102 may include and/or access a local database 114 that can maintain operational parameters and other information used to configure and operate the apparatus 100. The local database 114 may be implemented using one or more of a database module or server, flash memory,

magnetic media, EEPROM, optical media, tape, soft or hard disk, or the like. The processing circuit may also be operably coupled to external devices such as an antenna 122, a display 124, operator controls, such as a button 128 and a keypad 126, among other components.

[0034] FIG. 2 is a block schematic illustrating certain aspects of an apparatus 200 such as a wireless mobile device, a mobile telephone, a mobile computing system, a wireless telephone, a notebook computer, a tablet computing device, a media player, a gaming device, or the like. The apparatus 200 may include a plurality of IC devices 202 and 230 that exchange data and control information through a communications link 220. The communications link 220 may be used to connect the IC devices 202 and 230, which may be located in close proximity to one another or physically located in different parts of the apparatus 200. In one example, the communications link 220 may be provided on a chip carrier, substrate or circuit board that carries the IC devices 202 and 230. In another example, a first IC device 202 may be located in a keypad section of a flip-phone while a second IC device 230 may be located in a display section of the flip-phone. A portion of the communications link 220 may include a cable or an optical connection.

[0035] The communications link 220 may include multiple channels 222, 224 and 226. One or more channel 226 may be bidirectional, and may operate in half-duplex mode and/or full-duplex mode. One or more channels 222, 224 may be unidirectional. The communications link 220 may be asymmetrical, providing higher bandwidth in one direction. In one example described herein, a first communications channel 222 may be referred to as a forward link 222 while a second communications channel 224 may be referred to as a reverse link 224. The first IC device 202 may be designated as a host, master and/or transmitter, while the second IC device 230 may be designated as a client, slave and/or receiver, even if both IC devices 202 and 230 are configured to transmit and receive on the communications link 220. In one example, the forward link 222 may operate at a higher data rate when communicating data from a first IC device 202 to a second IC device 230, while the reverse link 224 may operate at a lower data rate when communicating data from the second IC device 230 to the first IC device 202.

[0036] The IC devices 202 and 230 may each include a processor or other processing and/or computing circuit or device 206, 236. In one example, the first IC device 202

may perform core functions of the apparatus 200, including maintaining wireless communications through a wireless transceiver 204 and an antenna 214, while the second IC device 230 may support a user interface that manages or operates a display controller 232, and may control operations of a camera or video input device using a camera controller 234. Other features supported by one or more of the IC devices 202 and 230 may include a keyboard, a voice-recognition component, and other input or output devices. The display controller 232 may include circuits and software drivers that support a display such as a liquid crystal display (LCD) panel, a touch-screen display, an indicator, and so on. The storage media 208 and 238 may include transitory and/or non-transitory storage devices adapted to maintain instructions and data used by the respective processing circuits 206 and 236, and/or other components of the IC devices 202 and 230. Communication between each processing circuit 206, 236 and its corresponding storage media 208 and 238 and other modules and circuits may be facilitated by one or more buses 212 and 242, respectively.

[0037] The reverse link 224 may be operated in the same manner as the forward link 222. The forward link 222 and the reverse link 224 may be capable of transmitting at comparable speeds or at different speeds, where speed may be expressed as a data transfer rate and/or a clocking rate. The forward and reverse data rates may be substantially the same or may differ by orders of magnitude, depending on the application. In some applications a single bidirectional link 226 may support communications between the first IC device 202 and the second IC device 230. The forward link 222 and/or the reverse link 224 may be configurable to operate in a bidirectional mode when, for example, the forward and reverse links 222 and 224 share the same physical connections and operate in a half-duplex manner.

[0038] In certain examples, the reverse link 224 derives a clocking signal from the forward link 222 for synchronization purposes, for control purposes, to facilitate power management and/or for simplicity of design. The clocking signal may have a frequency that is obtained by dividing the frequency of a symbol clock used to transmit signals on the forward link 222. The symbol clock may be superimposed or otherwise encoded in symbols transmitted on the forward link 222. The use of a clocking signal that is a derivative of the symbol clock allows fast synchronization

of transmitters and receivers (transceivers 210, 240) and enables fast start and stop of data signals without the need for framing to enable training and synchronization.

[0039] In certain examples, a single bidirectional link 226 may support communications between the first IC device 202 and the second IC device 230. In some instances, the first IC device 202 and the second IC device 230 provide encoding and decoding of data, address and control signals transmitted between a processing device and memory devices such as dynamic random access memory (DRAM).

Exemplary Description of Signaling Between Devices

[0040] FIG. 3 is a diagram 300 illustrating a low-level interface between a PMIC 302 and a SoC 304. Pin count reduction is a chipset goal to drive cost, area, and routing optimizations. As shown in FIG. 3, a low-level PMIC-to-SoC interface for boot, reset, and shutdown coordination may be implemented with two pins (two wire interfaces) on each integrated circuit (IC). In particular, the low-level PMIC-to-SoC interface may involve two signals: 1) PON_RESET_N communicated on wire 306; and 2) PS_HOLD communicated on wire 308. Both the PMIC 302 and the SoC 304 use two pins (e.g., dual-pin or dual-wire interface scheme) for communicating the two signals. As further shown in FIG. 3, the PMIC 302 and the SoC 304 may share a system power management interface (SPMI) 310, as well as a number of power rails, e.g., a first power rail (PWR_RAIL#1) 312(1) to a N-th power rail (PWR_RAIL#N) 312(N).

[0041] In an aspect of the disclosure, access to PON_RESET_N and PS_HOLD is crucial for system level verifications and debug of any issues related to power-up/power-down and reset functions. The dual-pin scheme may be used for validating power-up timing and identifying source(s) of reset and power-down functions. The dual-pin scheme also provides timing association with potential triggers. However, the dual-pin scheme is problematic as the number of pins required by the interface adds to package level cost. Moreover, the interface may not be permitted to support such a number of pins due to package-size and cost constraints. Accordingly, the present disclosure resolves the problems of the dual-pin scheme by functionally consolidating control functions (e.g., PON_RESET_N and PS_HOLD) into a single wire interface. This saves at least two chipset pins and at least one route between the PMIC and the SoC.

[0042] FIG. 4 is a diagram 400 illustrating a timing behavior of low-level control signals. A timing behavior of PON_RESET_N is shown at 402. A timing behavior of PS_HOLD is shown at 404. As shown at 406, an appreciable gap (approximately 56 μs) exists between de-assertion of PON_RESET_N and assertion of PS_HOLD. According to aspects of the disclosure, the timing of the two signals (PON_RESET_N and PS_HOLD), as well as their operational behavior, are maintained.

[0043] In an aspect of the disclosure, the PON_RESET_N line 402 and the PS_HOLD line 404 are combined. A shaded region 408 shows the steady state behavior of the two signals when a system is working properly. Within the region 408, the PON_RST_N line 402 goes low if, for example, a user initiates a system reset by pressing a system reset button. The PS_HOLD line 404 goes low if, for example, a system software starts a soft reset or system power cycle, or if a watch dog timer (WDT) overflow event is encountered.

[0044] FIG. 5 is diagram 500 illustrating a novel low-level interface between a PMIC 502 and a SoC 504. As shown in FIG. 5, the novel architecture uses a bi-directional signaling approach over a single wire. In particular, a single control signal (e.g., RST_N_PWR) may be communicated from the PMIC 502 to the SoC 504, or from the SoC 504 to the PMIC 502 over a single bi-directional line 506. In an aspect of the disclosure, RST_N_PWR is a consolidation/combination of PON_RESET_N and PS_HOLD of FIG. 3. As further shown in FIG. 5, the PMIC 502 and the SoC 504 may share a system power management interface (SPMI) 510, as well as a number of power rails, e.g., a first power rail (PWR_RAIL#1) 512(1) to a N-th power rail (PWR_RAIL#N) 512(N).

[0045] Communication of RST_N_PWR allows for the provision of output impedance, pull-up (PU) control, pull-down (PD) control, necessary logic, and timing control elements to enable unhindered operation of the system by maintaining all real-time timing requirements of the low level control signals. The novel architecture saves one pin on each IC and eliminates a top level trace between the PMIC 502 and the SoC 504. The novel architecture preserves the same system level behavior and visibility as with the dual-pin interface scheme. The novel architecture further supports simple standalone test bench booting without need for complex signaling.

[0046] FIG. 6 is a diagram 600 illustrating device behavior during a PMIC-initiated reset/shutdown procedure when implementing bi-directional signaling over a single wire. The manner in which the PMIC drives the single wire (e.g., bi-directional line 506 of FIG. 5) to communicate RST_N_PWR is shown at 602. The manner in which the SoC drives the single wire to communicate RST_N_PWR is shown at 604. A resultant interface level of the single wire as a result of being driven by the PMIC and/or the SoC is shown at 606. The resultant interface level 606 may be observed by the PMIC and the SoC, and verifiable via oscilloscope.

[0047] As shown in FIG. 6, while the system is off, a power-on trigger (PON trigger) may occur at 608 prompting the PMIC to power on. During this time, the SoC may be in a reset mode. At 610, the PMIC de-asserts the SoC reset by generating, for example, a pulse having a rising edge and a falling edge on the single wire. After generating the pulse, the PMIC waits for an acknowledgement (ACK) from the SoC. At 612, the SoC sends the ACK to the PMIC by generating, for example, a pulse with a rising edge on the single wire. The SoC subsequently powers on after sending the ACK.

[0048] At 614, the PMIC may observe a fault condition (or watchdog event). Accordingly, the PMIC triggers a reset/shutdown due to the fault condition by generating, for example, a single pulse on the single bi-directional line. The SoC observes the single pulse and responds by transitioning to a reset mode.

[0049] In an aspect of the disclosure, triggering the reset/shutdown by generating the single pulse on the single bi-directional line is unique to the PMIC. Hence, the reset/shutdown procedure initiated by the PMIC may be distinguished by observing the single pulse at 616. In an aspect of the disclosure, the single pulse includes a single transition on the single bi-directional line. The single transition may be a rising edge or a falling edge. The response from the SoC may be triggered upon observing the single transition, whether it be a rising edge or a falling edge.

[0050] In an aspect of the disclosure, procedures other than the reset/shutdown procedure may be triggered by the PMIC at 614. For example, the PMIC may trigger a boot sequence handshake at 614 by generating the single pulse on the single bi-directional line.

[0051] FIG. 7 is a diagram 700 illustrating device behavior during a SoC-initiated reset/shutdown procedure when implementing bi-directional signaling over a single

wire. The manner in which the PMIC drives the single wire (e.g., bi-directional line 506 of FIG. 5) to communicate RST_N_PWR is shown at 702. The manner in which the SoC drives the single wire to communicate RST_N_PWR is shown at 704. A resultant interface level of the single wire as a result of being driven by the PMIC and/or the SoC is shown at 706. The resultant interface level 706 may be observed by the PMIC and the SoC, and verifiable via oscilloscope.

[0052] As shown in FIG. 7, while the system is off, a power-on trigger (PON trigger) may occur at 708 prompting the PMIC to power on. During this time, the SoC may be in a reset mode. At 710, the PMIC de-asserts the SoC reset by generating, for example, a pulse having a rising edge and a falling edge on the single wire. After generating the pulse, the PMIC waits for an acknowledgement (ACK) from the SoC. At 712, the SoC sends the ACK to the PMIC by generating, for example, a pulse with a rising edge on the single wire. The SoC subsequently powers on after sending the ACK.

[0053] At 714, the SoC may initiate a reset/shutdown (warm reset or power off) due to, for example, the observance of a watchdog event. The SoC triggers the reset/shutdown by generating, for example, a double pulse on the single bi-directional line. The PMIC observes the double pulse and responds by transitioning to a warm reset or power off mode.

[0054] In an aspect of the disclosure, triggering the reset/shutdown by generating the double pulse on the single bi-directional line is unique to the SoC. Hence, the reset/shutdown procedure initiated by the SoC may be distinguished by observing the double pulse at 716. In an aspect of the disclosure, the double pulse may include a number of transitions on the single bi-directional line including a rising edge and/or a falling edge. The response from the SoC may be triggered upon observing a first transition of the double pulse, whether it be a rising edge or a falling edge.

[0055] In an aspect of the disclosure, procedures other than the reset/shutdown procedure may be triggered by the SoC at 714. For example, the SoC may trigger a boot sequence handshake at 714 by generating the double pulse on the single bi-directional line.

[0056] Referring to FIGs. 6 and 7, the novel architecture using bi-directional signaling over a single wire allows for easy oscilloscope verification of which IC (PMIC or SoC) drives the single bi-directional line. This facilitates debugging to gather the

same insight as with a dual-pin interface. In an aspect of the disclosure, the PMIC's active drive low has to delay long enough for the double pulse to be seen to differentiate PMIC initiation from SoC initiation. In a further aspect of the disclosure, the novel scheme preserves the ability for simple standalone PMIC booting by strapping RST_N_PWR to a 1.8V IO rail through a high valued resistor (which can be overcome by the PMIC's pulldown at PON completion).

[0057] In an aspect of the disclosure, although the novel architecture using bi-directional signaling over a single wire was described with respect to only two devices (PMIC and SoC), the novel architecture may be implemented by more than two devices, including non-PMIC and non-SoC devices. The manner in which such devices drive the single bi-directional line are to be distinguished from each other. For example, each device may be differentiated by generating a signal having a unique number of pulses, e.g., a third device triggers a reset/shutdown procedure or boot sequence handshake by generating three pulses on the single bi-directional line, a fourth device triggers a reset/shutdown procedure or boot sequence handshake by generating four pulses on the single bi-directional line, and so forth. In other examples, each device may be differentiated by generating a signal having a unique pulse width, a unique voltage level, or a unique impedance level, etc.

Exemplary Device and Methods for Communicating over Single Bi-Directional Line

[0058] FIG. 8 is an illustration of an apparatus 800 configured to support operations related to signaling between devices over a single bi-directional line according to one or more aspects of the disclosure (e.g., aspects related to the methods of FIGs. 9 and 10 described below). The apparatus 800 includes a communication interface (e.g., at least one transceiver) 802, a storage medium 804, a user interface 806, a memory device 808, and a processing circuit 810.

[0059] These components can be coupled to and/or placed in electrical communication with one another via a signaling bus or other suitable component, represented generally by the connection lines in FIG. 8. The signaling bus may include any number of interconnecting buses and bridges depending on the specific application of the processing circuit 810 and the overall design constraints. The signaling bus links together various circuits such that each of the communication interface 802,

the storage medium 804, the user interface 806, and the memory device 808 are coupled to and/or in electrical communication with the processing circuit 810. The signaling bus may also link various other circuits (not shown) such as timing sources, peripherals, voltage regulators, and power management circuits, which are well known in the art, and therefore, will not be described any further.

[0060] The communication interface 802 may be adapted to facilitate wireless communication of the apparatus 800. For example, the communication interface 802 may include circuitry and/or code (e.g., instructions) adapted to facilitate the communication of information bi-directionally with respect to one or more communication devices in a network. The communication interface 802 may be coupled to one or more antennas 812 for wireless communication within a wireless communication system. The communication interface 802 can be configured with one or more standalone receivers and/or transmitters, as well as one or more transceivers. In the illustrated example, the communication interface 802 includes a transmitter 814 and a receiver 816.

[0061] The memory device 808 may represent one or more memory devices. As indicated, the memory device 808 may maintain network-related information 818 along with other information used by the apparatus 800. In some implementations, the memory device 808 and the storage medium 804 are implemented as a common memory component. The memory device 808 may also be used for storing data that is manipulated by the processing circuit 810 or some other component of the apparatus 800.

[0062] The storage medium 804 may represent one or more computer-readable, machine-readable, and/or processor-readable devices for storing code, such as processor executable code or instructions (e.g., software, firmware), electronic data, databases, or other digital information. The storage medium 804 may also be used for storing data that is manipulated by the processing circuit 810 when executing code. The storage medium 804 may be any available media that can be accessed by a general purpose or special purpose processor, including portable or fixed storage devices, optical storage devices, and various other mediums capable of storing, containing or carrying code.

[0063] By way of example and not limitation, the storage medium 804 may include a magnetic storage device (e.g., hard disk, floppy disk, magnetic strip), an optical disk

(e.g., a compact disc (CD) or a digital versatile disc (DVD)), a smart card, a flash memory device (e.g., a card, a stick, or a key drive), a random access memory (RAM), a read only memory (ROM), a programmable ROM (PROM), an erasable PROM (EPROM), an electrically erasable PROM (EEPROM), a register, a removable disk, and any other suitable medium for storing code that may be accessed and read by a computer. The storage medium 804 may be embodied in an article of manufacture (e.g., a computer program product). By way of example, a computer program product may include a computer-readable medium in packaging materials. In view of the above, in some implementations, the storage medium 804 may be a non-transitory (e.g., tangible) storage medium.

[0064] The storage medium 804 may be coupled to the processing circuit 810 such that the processing circuit 810 can read information from, and write information to, the storage medium 804. That is, the storage medium 804 can be coupled to the processing circuit 810 so that the storage medium 804 is at least accessible by the processing circuit 810, including examples where at least one storage medium is integral to the processing circuit 810 and/or examples where at least one storage medium is separate from the processing circuit 810 (e.g., resident in the apparatus 800, external to the apparatus 800, distributed across multiple entities, etc.).

[0065] Code and/or instructions stored by the storage medium 804, when executed by the processing circuit 810, causes the processing circuit 810 to perform one or more of the various functions and/or process operations described herein. For example, the storage medium 804 may include operations configured for regulating operations at one or more hardware blocks of the processing circuit 810, as well as to utilize the communication interface 802 for wireless communication utilizing their respective communication protocols.

[0066] The processing circuit 810 is generally adapted for processing, including the execution of such code/instructions stored on the storage medium 804. As used herein, the term “code” or “instructions” shall be construed broadly to include without limitation programming, instructions, instruction sets, data, code, code segments, program code, programs, subprograms, software modules, applications, software applications, software packages, routines, subroutines, objects, executables, threads of execution, procedures, functions, etc., whether referred to as software, firmware, middleware, microcode, hardware description language, or otherwise.

[0067] The processing circuit 810 is arranged to obtain, process and/or send data, control data access and storage, issue commands, and control other desired operations. The processing circuit 810 may include circuitry configured to implement desired code provided by appropriate media in at least one example. For example, the processing circuit 810 may be implemented as one or more processors, one or more controllers, and/or other structure configured to execute executable code. Examples of the processing circuit 810 may include a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic component, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may include a microprocessor, as well as any conventional processor, controller, microcontroller, or state machine. The processing circuit 810 may also be implemented as a combination of computing components, such as a combination of a DSP and a microprocessor, a number of microprocessors, one or more microprocessors in conjunction with a DSP core, an ASIC and a microprocessor, or any other number of varying configurations. These examples of the processing circuit 810 are for illustration and other suitable configurations within the scope of the disclosure are also contemplated.

[0068] According to one or more aspects of the disclosure, the processing circuit 810 may be adapted to perform any or all of the features, processes, functions, operations and/or routines for any or all of the apparatuses described herein. As used herein, the term "adapted" in relation to the processing circuit 810 may refer to the processing circuit 810 being one or more of configured, employed, implemented, and/or programmed to perform a particular process, function, operation and/or routine according to various features described herein.

[0069] According to at least one example of the apparatus 800, the processing circuit 810 may include one or more of a device coupling circuit/module 820, an action initiating circuit/module 822, an action indicating circuit/module 824, a response triggering circuit/module 826, and an action receiving circuit/module 828, that are adapted to perform any or all of the features, processes, functions, operations and/or routines described herein (e.g., features, processes, functions, operations and/or routines described with respect to FIG. 9 and/ or FIG. 10).

[0070] The device coupling circuit/module 820 may include circuitry and/or instructions (e.g., device coupling instructions 830 stored on the storage medium 804) adapted to perform several functions relating to, for example, coupling a first device to a second device via a single bi-directional line.

[0071] The action initiating circuit/module 822 may include circuitry and/or instructions (e.g., action initiating instructions 832 stored on the storage medium 804) adapted to perform several functions relating to, for example, initiating a first action at the first device and/or initiating a second action at the second device.

[0072] The action indicating circuit/module 824 may include circuitry and/or instructions (e.g., action indicating instructions 834 stored on the storage medium 804) adapted to perform several functions relating to, for example, indicating initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device and indicating initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device. In another aspect of the disclosure, the action indicating circuit/module 824 may be adapted to perform several functions relating to, for example, indicating initiation of the first action by generating a first event on a single bi-directional line.

[0073] The response triggering circuit/module 826 may include circuitry and/or instructions (e.g., response triggering instructions 836 stored on the storage medium 804) adapted to perform several functions relating to, for example, triggering, at the second device, a response to the first action upon receiving the first single transition sent from the first device and triggering, at the first device, a response to the second action upon receiving the second single transition sent from the second device. Accordingly, the action receiving circuit/module 828 may include circuitry and/or instructions (e.g., action receiving instructions 838 stored on the storage medium 804) adapted to perform several functions relating to, for example, receiving the first single transition sent from the first device and receiving the second single transition sent from the second device.

[0074] The action receiving circuit/module 828 may further include circuitry and/or instructions (e.g., action receiving instructions 838 stored on the storage medium 804) adapted to perform several functions relating to, for example, receiving an

indication of a second action initiated at a second device by observing a second event on the single bi-directional line. Accordingly, the response triggering circuit/module 826 may further be adapted to perform several functions relating to, for example, triggering a response to the second action upon receiving a first transition associated with the second event.

[0075] As mentioned above, instructions stored by the storage medium 804, when executed by the processing circuit 810, causes the processing circuit 810 to perform one or more of the various functions and/or process operations described herein. For example, the storage medium 804 may include one or more of the device coupling instructions 830, the action initiating instructions 832, the action indicating instructions 834, the response triggering instructions 836, and the action receiving instructions 838.

[0076] FIG. 9 is a flowchart 900 illustrating a method of signaling between devices over a single bi-directional line. The method may be performed by an apparatus (e.g., apparatus 100 of FIG. 1, devices 502 and 504 of FIG. 5, or apparatus 800 of FIG. 8).

[0077] The apparatus couples a first device to a second device via a single bi-directional line 902. In an aspect of the disclosure, one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC).

[0078] The apparatus indicating initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device 904. The apparatus indicates initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device 906. In an aspect of the disclosure, the first single transition is distinct from the second single transition.

[0079] As used in this application, the term "action" may include, but is not limited to, an event, a triggering event, a procedure, a process, or a change of state. In an aspect of the disclosure, the first action is at least one of a reset action or a boot sequence handshake, and the second action is at least one of the reset action or the boot sequence handshake.

[0080] The apparatus triggers, at the second device, a response to the first action upon receiving the first single transition sent from the first device 908. The apparatus

triggers, at the first device, a response to the second action upon receiving the second single transition sent from the second device 910.

[0081] In an aspect of the disclosure, the first single transition is at least one of a rising edge or a falling edge, and the second single transition is at least one of the rising edge or the falling edge. In another aspect of the disclosure, the first single transition sent by the first device is a rising edge and the second single transition sent by the second device is a falling edge.

[0082] FIG. 10 is a flowchart 1000 illustrating a method of signaling over a single bi-directional line. The method may be performed by a first device (e.g., apparatus 100 of FIG. 1, one of the devices 502 and 504 of FIG. 5, or apparatus 800 of FIG. 8).

[0083] The first device initiates a first action 1002. The first device indicates initiation of the first action by generating a first event on a single bi-directional line 1004. The first device receives an indication of a second action initiated at a second device by observing a second event on the single bi-directional line 1006.

[0084] As mentioned above, the term "action" may include, but is not limited to, an event, a triggering event, a procedure, a process, or a change of state. In an aspect of the disclosure, one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC). In an aspect of the disclosure, the first action is at least one of a reset action or a boot sequence handshake, and the second action is at least one of the reset action or the boot sequence handshake. In a further aspect of the disclosure, the first action and the second action are variable depending on a state of a system that includes the first device and the second device.

[0085] The first device triggers a response to the second action upon receiving a first transition associated with the second event 1008. In an aspect of the disclosure, the triggered response is variable depending on a state of a system that includes the first device and the second device.

[0086] In an aspect of the disclosure, the first event includes a first number of pulses, and the second event includes a second number of pulses different from the first number. In a further aspect of the disclosure, the first event includes a single pulse and the second event includes a double pulse, or the first event includes the double pulse and the second event includes the single pulse. In yet another aspect of the

disclosure, the first event is differentiated from the second event by a voltage level, an impedance level, a pulse width, and/or a number of pulses.

[0087] It is understood that the specific order or hierarchy of steps in the processes disclosed is an illustration of exemplary approaches. The specific order or hierarchy of steps in the processes may be rearranged based upon design preferences. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0088] As used in this application, the terms "component," "module," "system" and the like are intended to include a computer-related entity, such as, but not limited to hardware, firmware, a combination of hardware and software, software, or software in execution. For example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program and/or a computer. By way of illustration, both an application running on a computing device and the computing device can be a component. One or more components can reside within a process and/or thread of execution and a component may be localized on one computing device and/or distributed between two or more computing devices. In addition, these components can execute from various computer readable media having various data structures stored thereon. The components may communicate by way of local and/or remote processes such as in accordance with a signal having one or more data packets, such as data from one component interacting with another component in a local system, distributed system, and/or across a network such as the Internet with other systems by way of the signal.

[0089] Moreover, the term "or" is intended to mean an inclusive "or" rather than an exclusive "or." That is, unless specified otherwise, or clear from the context, the phrase "X employs A or B" is intended to mean any of the natural inclusive permutations. That is, the phrase "X employs A or B" is satisfied by any of the following instances: X employs A; X employs B; or X employs both A and B. In addition, the articles "a" and "an" as used in this application and the appended claims should generally be construed to mean "one or more" unless specified otherwise or clear from the context to be directed to a singular form.

[0090] The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined

herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more." Unless specifically stated otherwise, the term "some" refers to one or more. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase "means for."

CLAIMS

1. A method of signaling between devices, comprising:

coupling a first device to a second device via a single bi-directional line;

indicating initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line from the first device to the second device; and

indicating initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line from the second device to the first device.

2. The method of claim 1, further comprising:

triggering, at the second device, a response to the first action upon receiving the first single transition sent from the first device; and

triggering, at the first device, a response to the second action upon receiving the second single transition sent from the second device.

3. The method of claim 1, wherein the first single transition is at least one of a rising edge or a falling edge, and the second single transition is at least one of the rising edge or the falling edge.

4. The method of claim 1, wherein the first single transition sent by the first device is a rising edge and the second single transition sent by the second device is a falling edge.

5. The method of claim 1, wherein one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC).

6. The method of claim 1, wherein:

the first action is at least one of a reset action or a boot sequence handshake; and

the second action is at least one of the reset action or the boot sequence handshake.

7. An apparatus for signaling between devices, comprising:

a first device;

a second device; and

a single bi-directional line coupling the first device to the second device,

wherein the first device indicates initiation of a first action, initiated at the first device, by sending a first single transition on the single bi-directional line to the second device, and

wherein the second device indicates initiation of a second action, initiated at the second device, by sending a second single transition on the single bi-directional line to the first device.

8. The apparatus of claim 7, wherein:

the second device triggers a response to the first action upon receiving the first single transition sent from the first device; and

the first device triggers a response to the second action upon receiving the second single transition sent from the second device.

9. The apparatus of claim 7, wherein the first single transition is at least one of a rising edge or a falling edge, and the second single transition is at least one of the rising edge or the falling edge.

10. The apparatus of claim 7, wherein the first single transition sent by the first device is a rising edge and the second single transition sent by the second device is a falling edge.

11. The apparatus of claim 7, wherein one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC).

12. The apparatus of claim 7, wherein:

the first action is at least one of a reset action or a boot sequence handshake; and

the second action is at least one of the reset action or the boot sequence handshake.

13. A method of signaling at a first device, comprising:

initiating a first action;

indicating initiation of the first action by generating a first event on a single bi-directional line; and

receiving an indication of a second action initiated at a second device by observing a second event on the single bi-directional line.

14. The method of claim 13, further including triggering a response to the second action upon receiving a first transition associated with the second event.

15. The method of claim 14, wherein the triggered response is variable depending on a state of a system that includes the first device and the second device.

16. The method of claim 13, wherein:

the first event includes a first number of pulses; and

the second event includes a second number of pulses different from the first number.

17. The method of claim 16, wherein:

the first event includes a single pulse and the second event includes a double pulse, or

the first event includes the double pulse and the second event includes the single pulse.

18. The method of claim 13, wherein the first event is differentiated from the second event by at least one of:

a voltage level;

an impedance level;

a pulse width; or

a number of pulses.

19. The method of claim 13, wherein one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC).

20. The method of claim 13, wherein:

the first action is at least one of a reset action or a boot sequence handshake; and

the second action is at least one of the reset action or the boot sequence handshake.

21. The method of claim 13, wherein the first action and the second action are variable depending on a state of a system that includes the first device and the second device.

22. A first device, comprising:

a memory; and

a processing circuit coupled to the memory and configured to:

initiate a first action,

indicate initiation of the first action by generating a first event on a single bi-directional line, and

receive an indication of a second action initiated at a second device by observing a second event on the single bi-directional line.

23. The first device of claim 22, wherein the processing circuit is further configured to trigger a response to the second action upon receiving a first transition associated with the second event.

24. The first device of claim 23, wherein the triggered response is variable depending on a state of a system that includes the first device and the second device.

25. The first device of claim 22, wherein:

the first event includes a first number of pulses; and

the second event includes a second number of pulses different from the first number.

26. The first device of claim 25, wherein:

the first event includes a single pulse and the second event includes a double pulse, or

the first event includes the double pulse and the second event includes the single pulse.

27. The first device of claim 22, wherein the first event is differentiated from the second event by at least one of:

a voltage level;

an impedance level;

a pulse width; or

a number of pulses.

28. The first device of claim 22, wherein one of the first device and the second device is a power management integrated circuit (PMIC) and the other of the first device and the second device is a system-on-chip (SoC).

29. The first device of claim 22, wherein:

the first action is at least one of a reset action or a boot sequence handshake; and

the second action is at least one of the reset action or the boot sequence handshake.

30. The first device of claim 22, wherein the first action and the second action are variable depending on a state of a system that includes the first device and the second device.

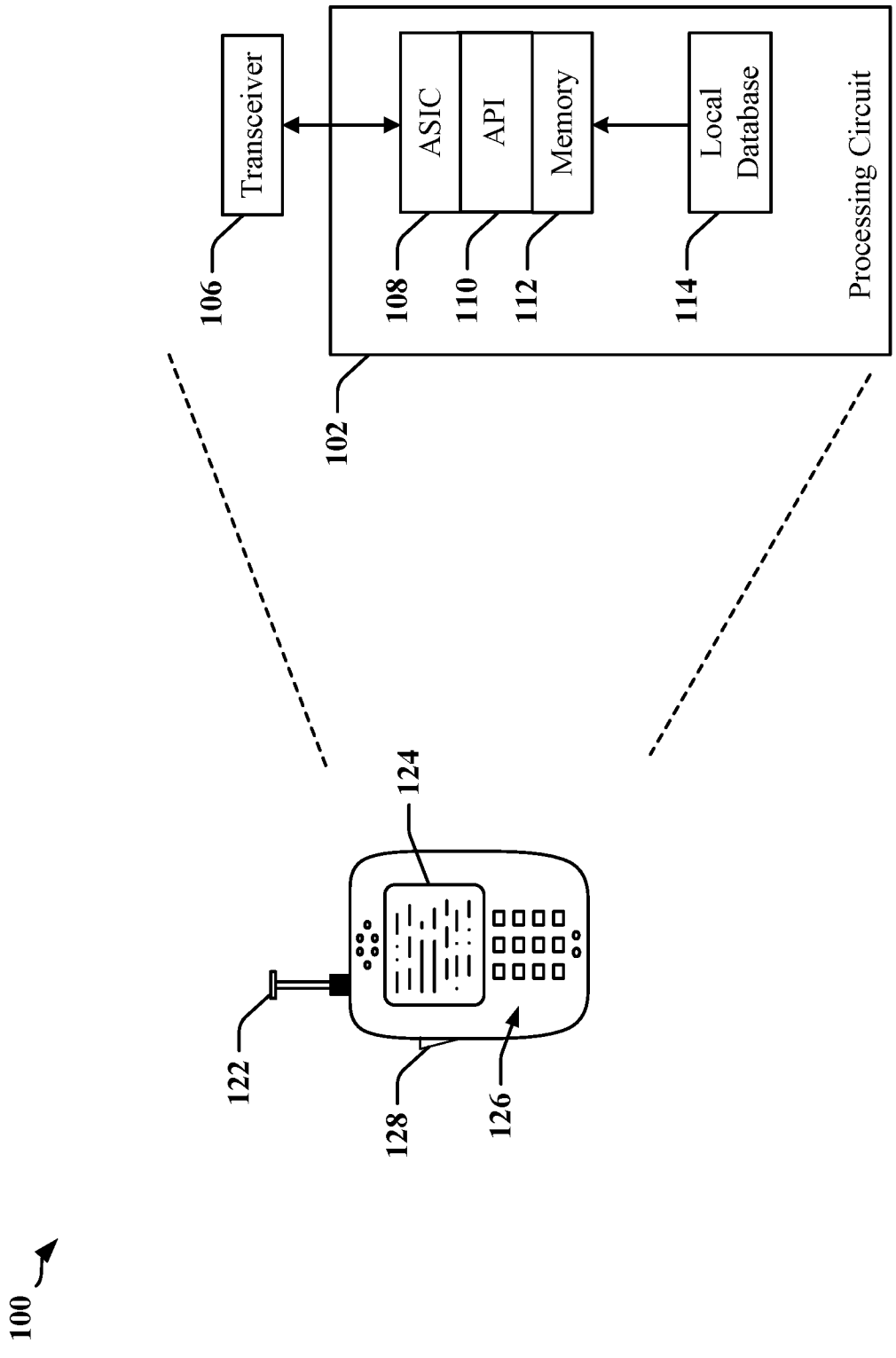
100
102
Processing Circuit
Transceiver
ASIC
API
Memory
Local Database
106
108
110
112
114
122
124
126
128

FIG. 1

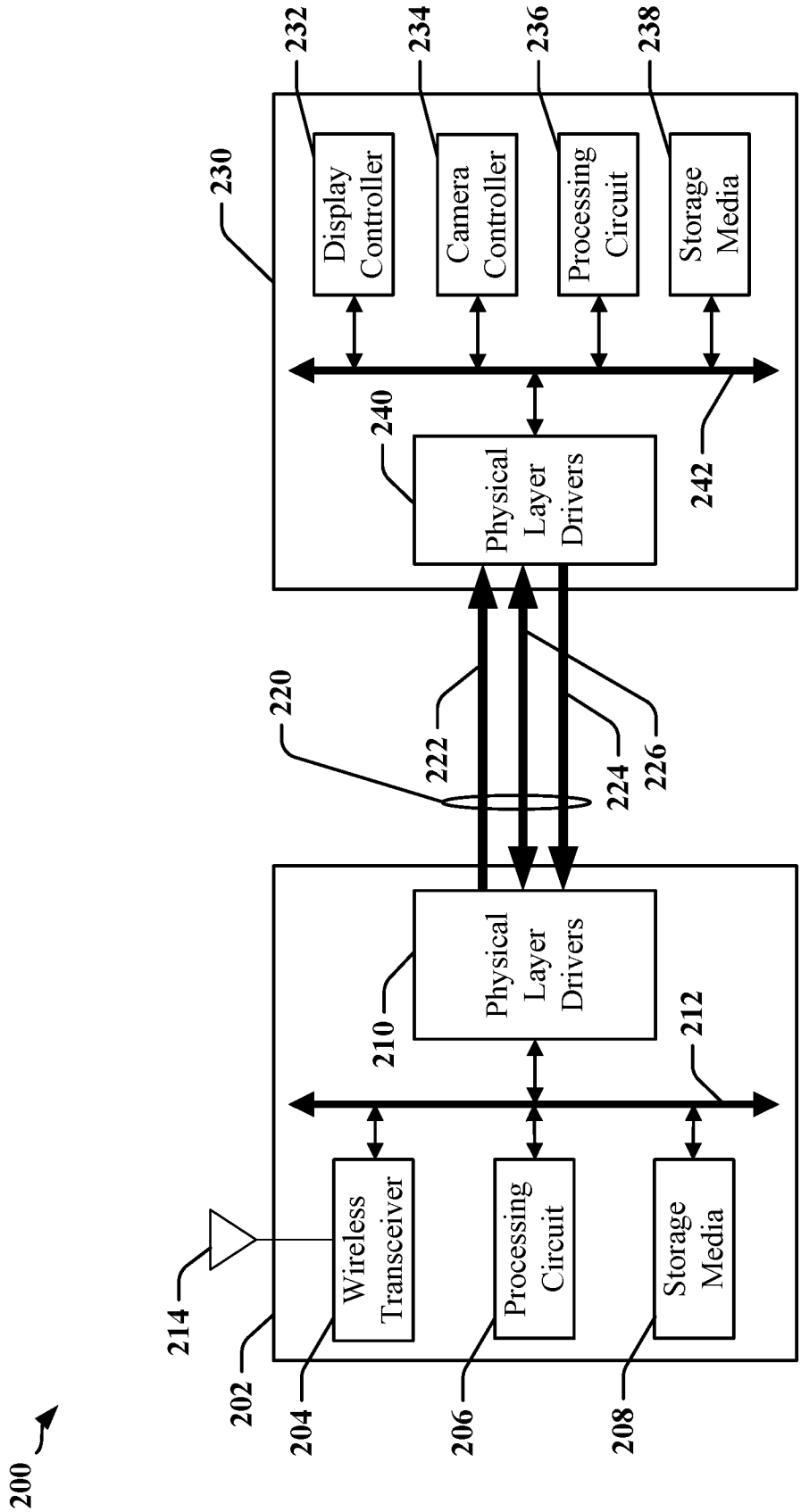
200
202
204
206
208
210
212
214
220
222
224
226
230
232
234
236
238
240
242
Wireless Transceiver
Processing Circuit
Storage Media
Physical Layer Drivers
Physical Layer Drivers
Display Controller
Camera Controller
Processing Circuit
Storage Media

FIG. 2

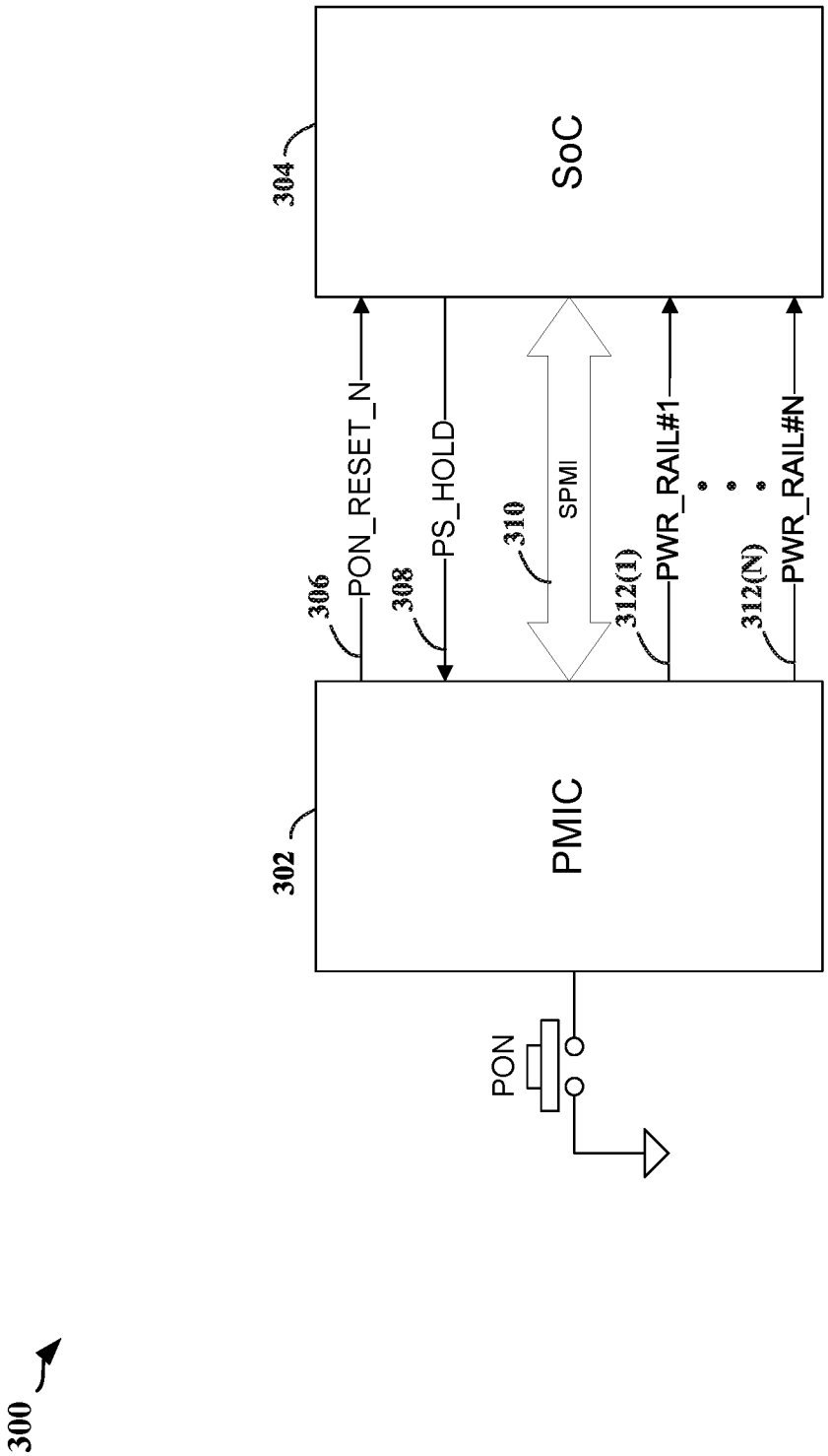
300
302
PMIC
304
SoC
PON
306
PON_RESET_N
308
PS_HOLD
310
SPMI
312(1)
PWR_RAIL#1
312(N)
PWR_RAIL#N

FIG. 3

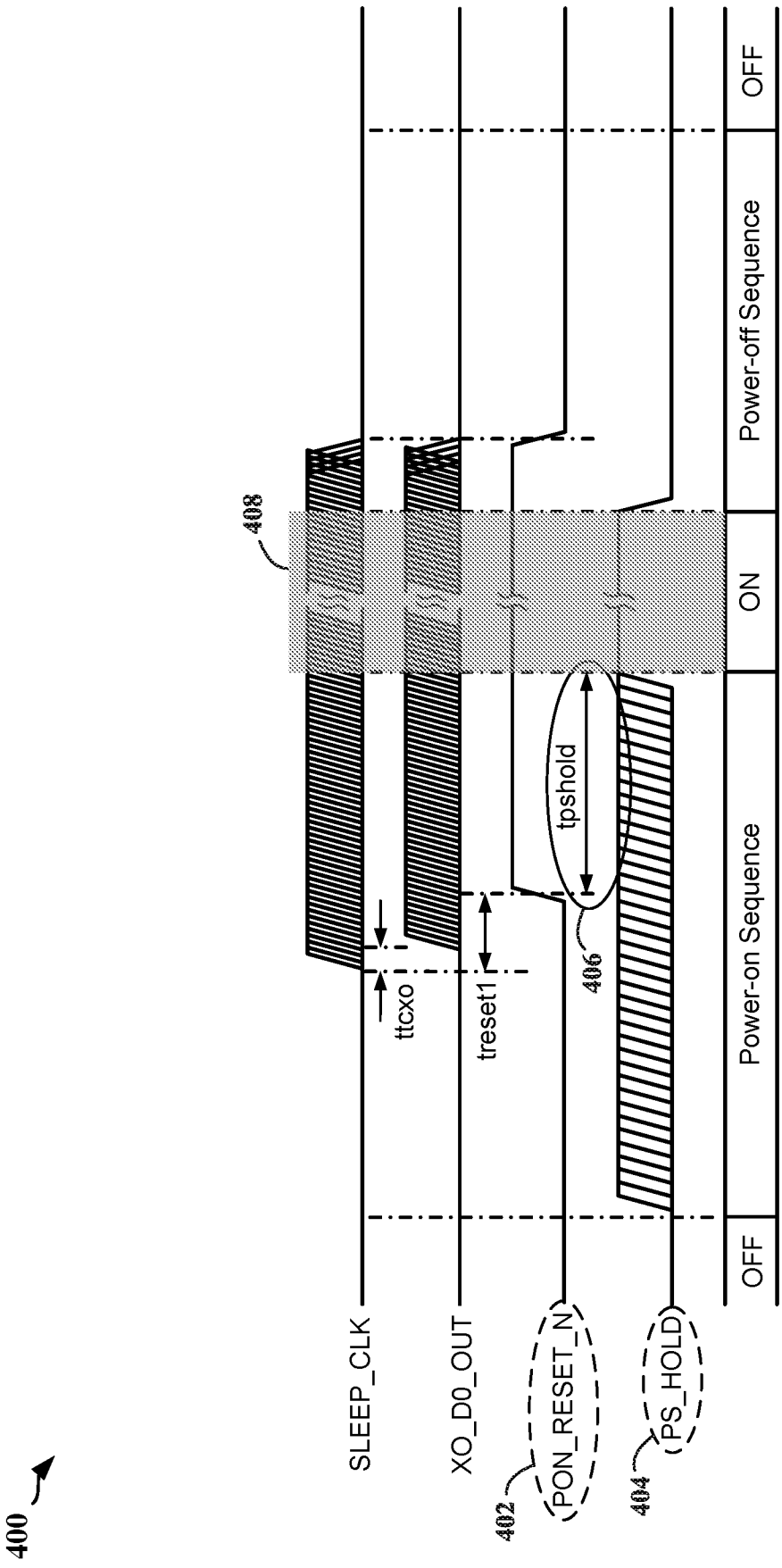
400
SLEEP_CLK
XO_D0_OUT
PON_RESET_N
PS_HOLD
402
404
406
408
ttcxo
treset1
tpshold
OFF
Power-on Sequence
ON
Power-off Sequence
OFF

FIG. 4

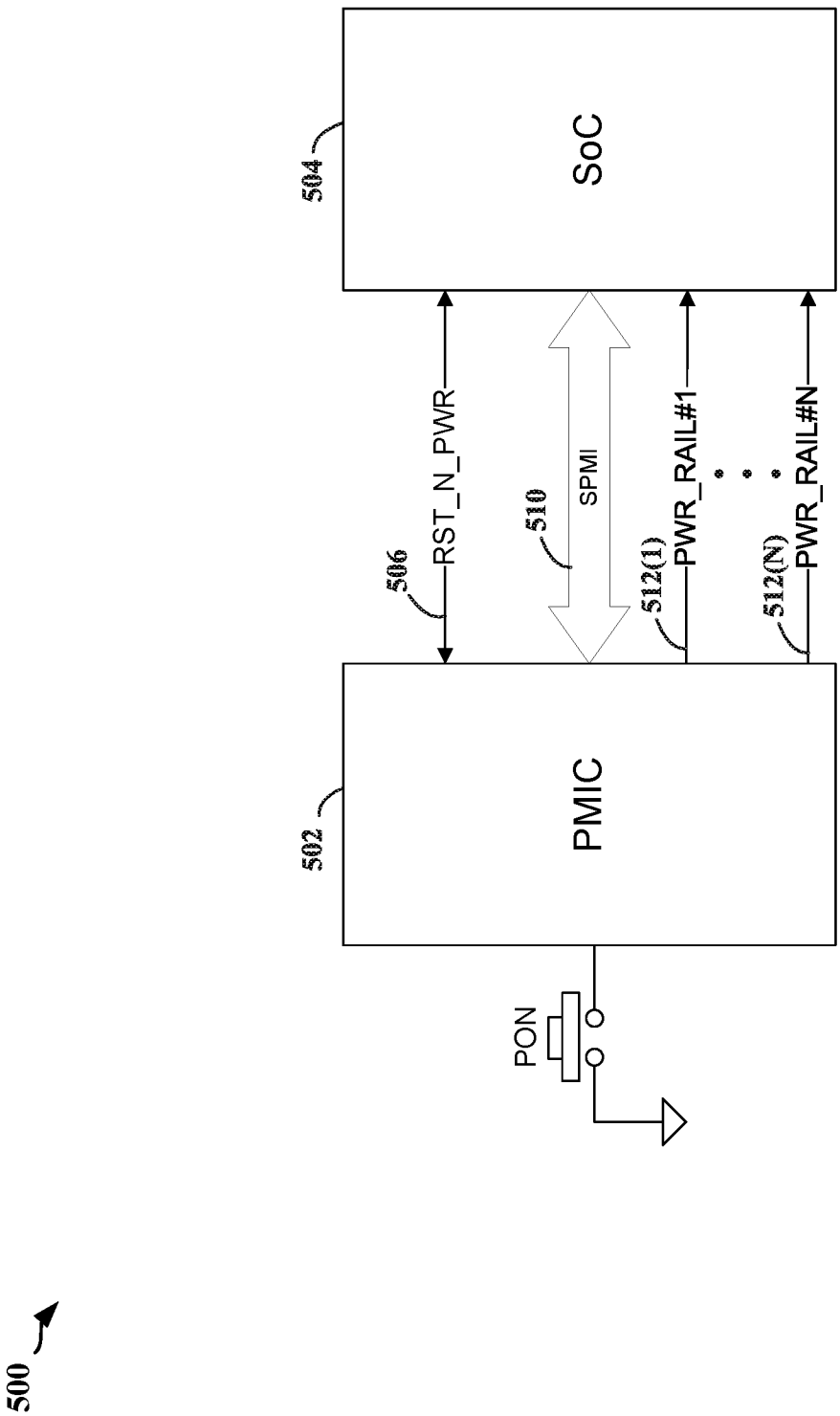
500
502
PMIC
504
SoC
506
RST_N_PWR
510
SPMI
512(1)
PWR_RAIL#1
512(N)
PWR_RAIL#N
PON

FIG. 5

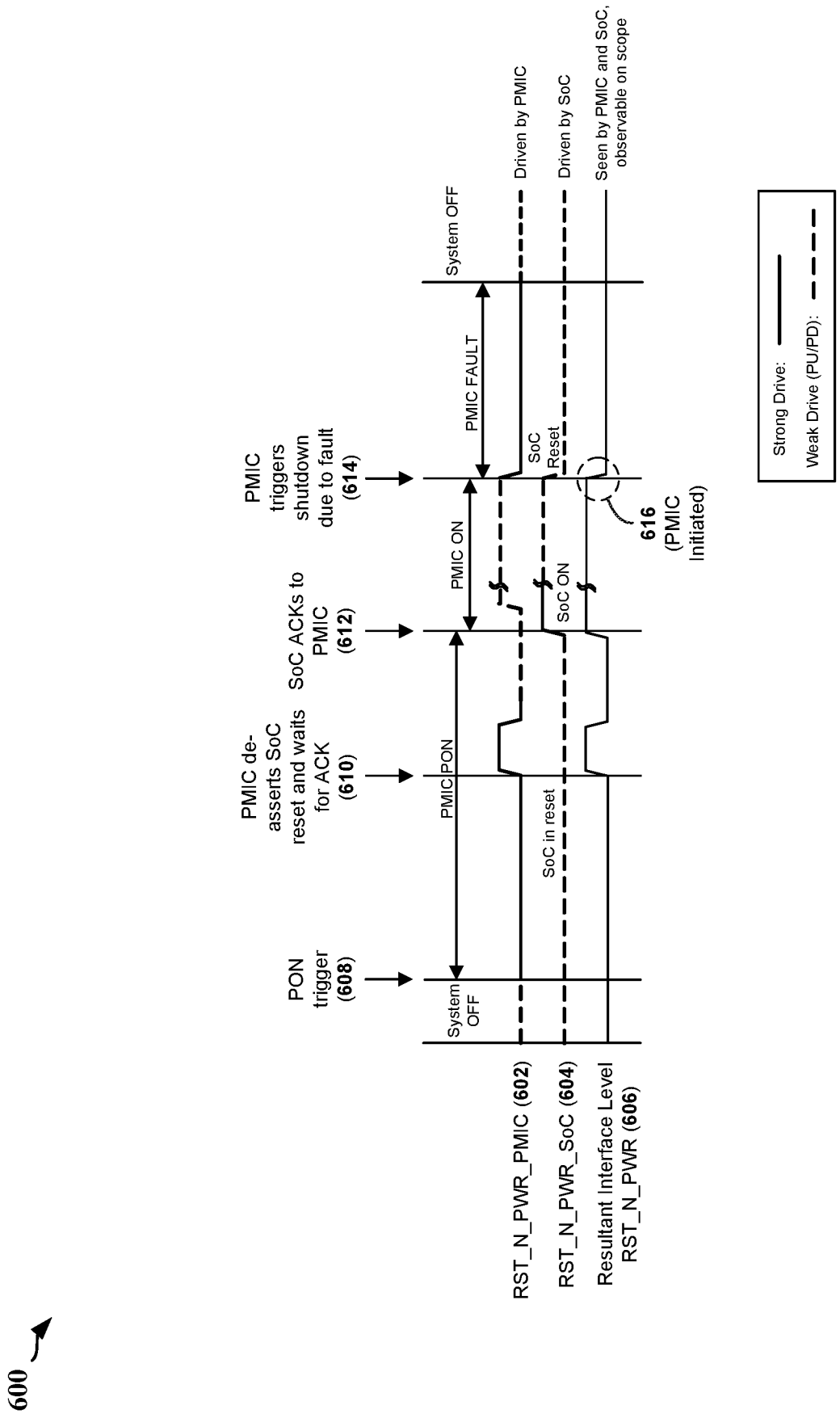
600
RST_N_PWR_PMIC (602)
RST_N_PWR_SoC (604)
Resultant Interface Level RST_N_PWR (606)
System OFF
PON trigger (608)
PMIC PON
SoC in reset
PMIC de-asserts SoC reset and waits for ACK (610)
SoC ACKs to PMIC (612)
PMIC ON
SoC ON
PMIC triggers shutdown due to fault (614)
PMIC FAULT
SoC Reset
616 (PMIC Initiated)
System OFF
Driven by PMIC
Driven by SoC
Seen by PMIC and SoC, observable on scope
Strong Drive:
Weak Drive (PU/PD):

FIG. 6

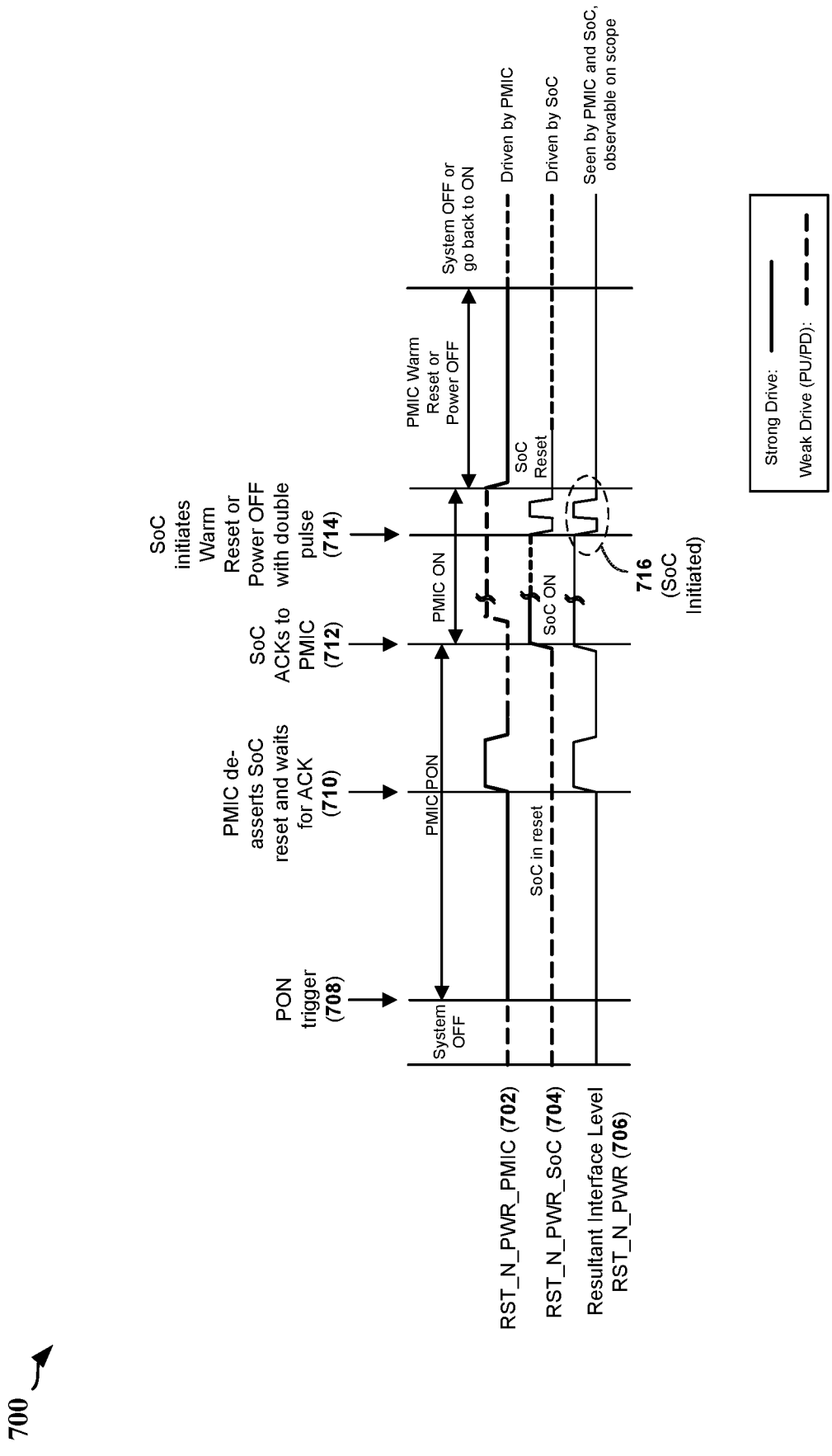
700
RST_N_PWR_PMIC (702)
RST_N_PWR_SoC (704)
Resultant Interface Level RST_N_PWR (706)
System OFF
PON trigger (708)
PMIC PON
PMIC de-asserts SoC reset and waits for ACK (710)
SoC in reset
SoC ACKs to PMIC (712)
PMIC ON
SoC ON
SoC initiates Warm Reset or Power OFF with double pulse (714)
SoC Reset
716 (SoC Initiated)
PMIC Warm Reset or Power OFF
System OFF or go back to ON
Driven by PMIC
Driven by SoC
Seen by PMIC and SoC, observable on scope
Strong Drive:
Weak Drive (PU/PD):

FIG. 7

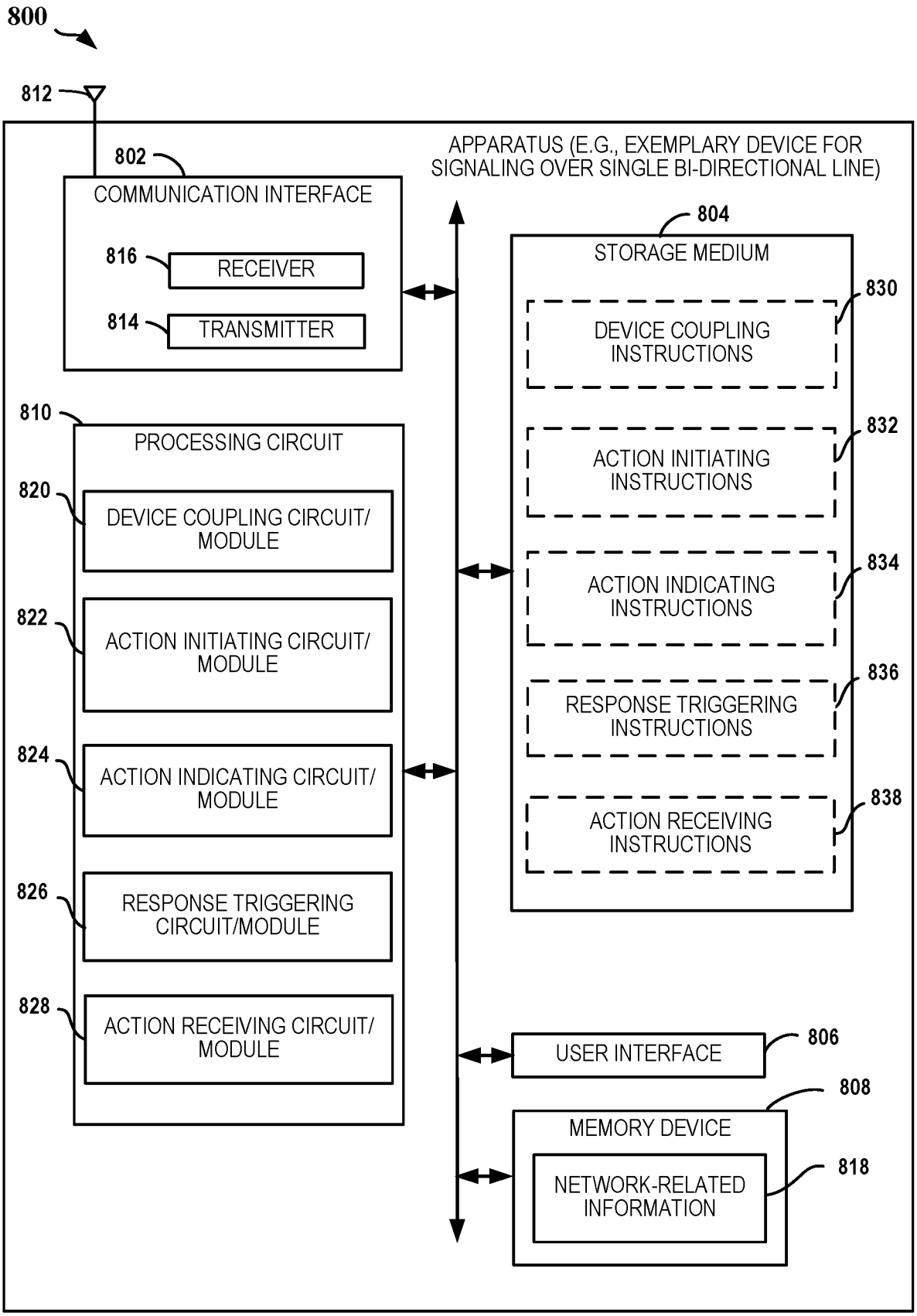
800
812
APPARATUS (E.G., EXEMPLARY DEVICE FOR SIGNALING OVER SINGLE BI-DIRECTIONAL LINE)
802
COMMUNICATION INTERFACE
816
RECEIVER
814
TRANSMITTER
804
STORAGE MEDIUM
830
DEVICE COUPLING INSTRUCTIONS
832
ACTION INITIATING INSTRUCTIONS
834
ACTION INDICATING INSTRUCTIONS
836
RESPONSE TRIGGERING INSTRUCTIONS
838
ACTION RECEIVING INSTRUCTIONS
810
PROCESSING CIRCUIT
820
DEVICE COUPLING CIRCUIT/ MODULE
822
ACTION INITIATING CIRCUIT/ MODULE
824
ACTION INDICATING CIRCUIT/ MODULE
826
RESPONSE TRIGGERING CIRCUIT/MODULE
828
ACTION RECEIVING CIRCUIT/ MODULE
806
USER INTERFACE
808
MEMORY DEVICE
818
NETWORK-RELATED INFORMATION

FIG. 8

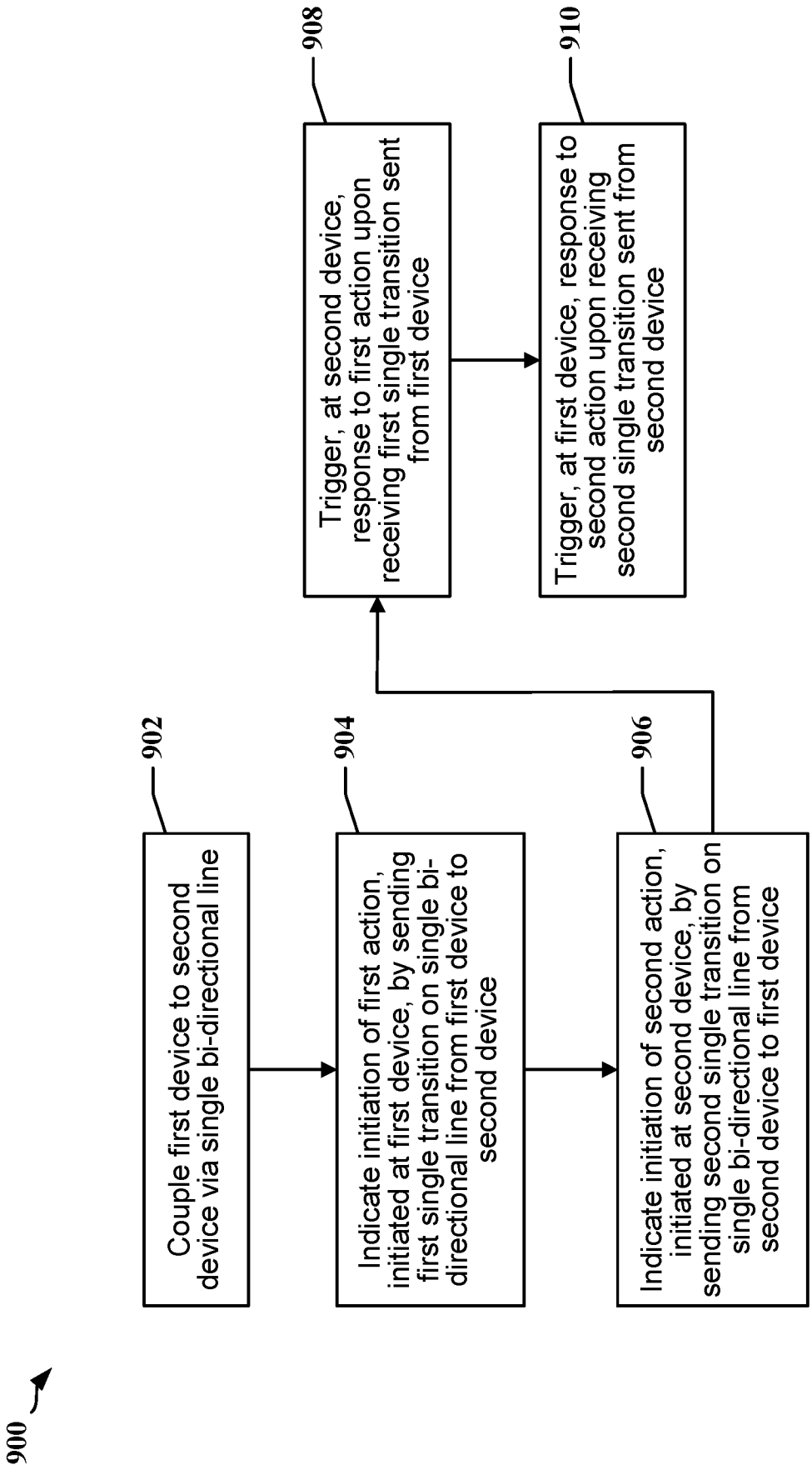
900
902
Couple first device to second device via single bi-directional line
904
Indicate initiation of first action, initiated at first device, by sending first single transition on single bi-directional line from first device to second device
906
Indicate initiation of second action, initiated at second device, by sending second single transition on single bi-directional line from second device to first device
908
Trigger, at second device, response to first action upon receiving first single transition sent from first device
910
Trigger, at first device, response to second action upon receiving second single transition sent from second device

FIG. 9

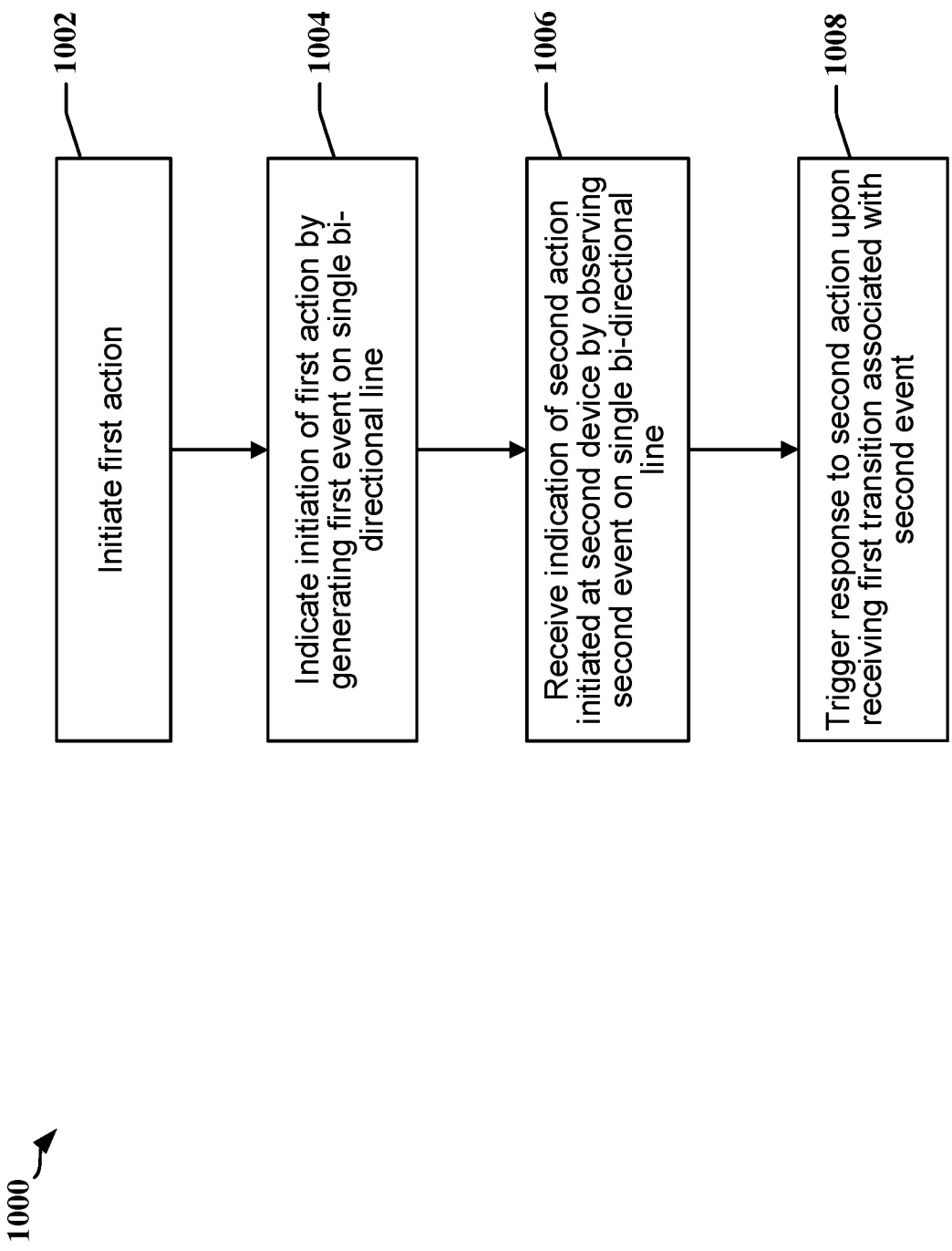
1000
1002
Initiate first action
1004
Indicate initiation of first action by generating first event on single bi-directional line
1006
Receive indication of second action initiated at second device by observing second event on single bi-directional line
1008
Trigger response to second action upon receiving first transition associated with second event

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/061392

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/233917 A1 (ROCAS GABRIEL [FR] ET AL) 25 November 2004 (2004-11-25) abstract paragraph [0001] - paragraph [0021] figures 1-5 claims 1, 9, 15	1-30
X	EP 2 778 937 A2 (INTEL CORP [US]) 17 September 2014 (2014-09-17) abstract paragraph [0024] - paragraph [0158] figures 2-4, 8	1-30
X	US 2004/049619 A1 (LIN PETER [TW]) 11 March 2004 (2004-03-11) abstract paragraph [0003] - paragraph [0017] paragraph [0029] - paragraph [0045] figures 5-6	1-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2017	21/02/2017

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/061392

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