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(54) Title: PIEZOELECTRIC ULTRASONIC TRANSDUCER AND PROCESS

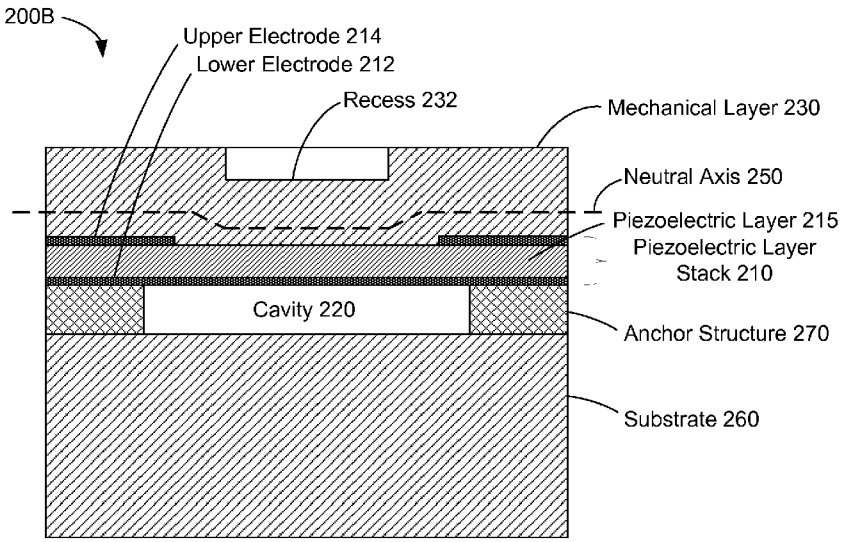

Figure 2B

(57) Abstract: A piezoelectric micromechanical ultrasonic transducer (PMUT) includes a multilayer stack disposed on a substrate. The multilayer stack may include an anchor structure disposed over the substrate, a piezoelectric layer stack disposed over the anchor structure, and a mechanical layer disposed proximate to the piezoelectric layer stack. The piezoelectric layer stack may be disposed over a cavity. The mechanical layer may seal the cavity and, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

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PIEZOELECTRIC ULTRASONIC TRANSDUCER AND PROCESS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This disclosure claims priority to U.S. Provisional Patent Application No. 62/022,140 (Attorney Docket No. QUALP264PUS/145636P1), filed July 8, 2014, entitled "PIEZOELECTRIC ULTRASONIC TRANSDUCER AND PROCESS," to U.S. Utility Patent Application 14/569,256, filed on December 12, 2014, entitled "PIEZOELECTRIC ULTRASONIC TRANSDUCER AND PROCESS," and to Provisional Patent Application No. 61/915,361, filed on December 12, 2013 and entitled "MICROMECHANICAL ULTRASONIC TRANSDUCERS AND DISPLAY," which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] This disclosure relates to a piezoelectric transducer and to techniques for fabricating piezoelectric transducers, and more particularly to a piezoelectric ultrasonic transducer suitable for use in an electronic sensor array or interactive display for biometric sensing, imaging, and touch or gesture recognition.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] Thin film piezoelectric ultrasonic transducers are attractive candidates for numerous applications including biometric sensors such as fingerprint sensors, gesture detection, microphones and speakers, ultrasonic imaging, and chemical sensors. The transducers typically include a piezoelectric stack suspended over a cavity. The piezoelectric stack may include a layer of piezoelectric material and a layer of patterned or unpatterned electrodes on each side of the piezoelectric layer.

[0004] Figure 1 is an elevation view of a piezoelectric ultrasonic transducer. As shown in Figure 1, it is known to configure a piezoelectric ultrasonic transducer 100 such that it includes a piezoelectric layer stack 110 disposed over a mechanical layer 130 and a cavity 120 that may be formed in, for example, a silicon-on-insulator (SOI) wafer. The

piezoelectric layer stack 110 includes a piezoelectric layer 115 with associated lower electrode 112 and upper electrode 114 disposed, respectively below and above the piezoelectric layer 115. The cavity 120 may be formed in a semiconductor substrate 160 such as a silicon wafer or in some implementations, a silicon-on-insulator (SOI) wafer. The mechanical layer 130 may be formed from an active silicon layer of the SOI wafer.

[0005] Portions of the present disclosure relate to micromechanical ultrasonic transducers, aspects of which have been described in United States Provisional Patent Application No. 61/915,361, filed on December 12, 2013 and entitled "MICROMECHANICAL ULTRASONIC TRANSDUCERS AND DISPLAY," and in a United States Patent Application filed concurrently herewith, Attorney Docket Number QUALP228US/141202, and entitled "MICROMECHANICAL ULTRASONIC TRANSDUCERS AND DISPLAY", assigned to the assignee of the present invention and hereby incorporated by reference into the present application in its entirety for all purposes.

SUMMARY

[0006] The systems, methods and devices of this disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0007] One innovative aspect of the subject matter described in this disclosure relates to a piezoelectric micromechanical ultrasonic transducer (PMUT) including a multilayer stack disposed on a substrate. The multilayer stack includes an anchor structure disposed over the substrate, a piezoelectric layer stack disposed over the anchor structure, and a mechanical layer disposed proximate to the piezoelectric layer stack. The piezoelectric layer stack is disposed over a cavity. The mechanical layer seals the cavity and, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits acoustic or ultrasonic signals. In some examples, the mechanical layer may have a thickness such that a neutral axis of the multilayer stack is displaced, relative to a neutral axis of the piezoelectric layer stack, towards the mechanical layer to allow an

out-of-plane bending mode. In some examples, the mechanical layer may be substantially thicker than the piezoelectric layer stack. In some examples, the neutral axis may pass through the mechanical layer.

[0008] In some examples, the cavity may be formed by removing a sacrificial material through at least one release hole, the mechanical layer may be formed after removing the sacrificial material, and forming the mechanical layer may seal the cavity by sealing the at least one release hole.

[0009] In some examples, the piezoelectric layer stack may include a piezoelectric layer, a lower electrode disposed below the piezoelectric layer, and an upper electrode disposed above the piezoelectric layer.

[0010] In some examples, the mechanical layer may include a recess where the mechanical layer is locally thinned.

[0011] In some examples, the mechanical layer may be disposed over a side of the piezoelectric stack opposite to the substrate.

[0012] In some examples, the mechanical layer may be disposed below a side of the piezoelectric stack facing the substrate.

[0013] In some examples, the PMUT may further include an acoustic coupling medium disposed above the piezoelectric layer stack, wherein the PMUT is configured to receive or transmit ultrasonic signals through the coupling medium.

[0014] According to some implementations, a PMUT includes a multilayer stack disposed on a substrate. The multilayer stack includes an anchor structure disposed over the substrate, a piezoelectric layer stack disposed over the anchor structure, and a mechanical layer disposed proximate to the piezoelectric layer stack, the mechanical layer including a recess where the mechanical layer is locally thinned. The piezoelectric layer stack is disposed over a cavity and the mechanical layer, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

[0015] In some examples, the cavity may be formed by removing a sacrificial material through at least one release hole, the mechanical layer may be formed after removing the sacrificial material, and forming the mechanical layer may seal the cavity by sealing the at least one release hole.

[0016] According to some implementations, a method of making a PMUT includes forming an anchor structure over a substrate, the anchor structure disposed proximate to regions of sacrificial material, forming a piezoelectric layer stack over the anchor structure, removing the sacrificial material so as to form a cavity under the piezoelectric layer stack, and disposing a mechanical layer proximate to the piezoelectric layer stack, wherein the piezoelectric layer stack and the mechanical layer form part of a multilayer stack, the mechanical layer seals the cavity and, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

[0017] In some examples, removing the sacrificial material may form a cavity under the piezoelectric layer stack.

[0018] In some examples, removing the sacrificial material may include removing the sacrificial material through at least one release hole and the mechanical layer seals the at least one release hole.

[0019] In some examples, the anchor structure may be disposed in a lower layer, the lower layer being parallel to the piezoelectric stack layer and including the regions of sacrificial material.

[0020] In some examples, the mechanical layer may have a thickness such that a neutral axis of the multilayer stack is displaced relative to a neutral axis of the piezoelectric layer stack and towards the mechanical layer to allow an out-of-plane bending mode. In some examples, the mechanical layer is substantially thicker than the piezoelectric layer stack. In some examples, the neutral axis may pass through the mechanical layer.

[0021] According to some implementations, an apparatus includes an array of PMUT sensors and an acoustic coupling medium. At least one PMUT includes a multilayer stack disposed on a substrate. The multilayer stack includes an anchor structure disposed over the substrate, a piezoelectric layer stack disposed over the anchor structure and a cavity, and a mechanical layer disposed proximate to the piezoelectric layer stack, the mechanical layer sealing the cavity. The acoustic coupling medium is disposed above the piezoelectric layer stack and the PMUT is configured to receive or transmit ultrasonic signals through the coupling medium.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Details of one or more implementations of the subject matter described in this specification are set forth in this disclosure and the accompanying drawings. Other features, aspects, and advantages will become apparent from a review of the disclosure. Note that the relative dimensions of the drawings and other diagrams of this disclosure may not be drawn to scale. The sizes, thicknesses, arrangements, materials, etc., shown and described in this disclosure are made only by way of example and should not be construed as limiting. Like reference numbers and designations in the various drawings indicate like elements.

[0023] Figure 1 is an elevation view of a piezoelectric ultrasonic transducer.

[0024] Figures 2A–2D show examples of implementations of a PMUT stack, configured in accordance with the presently disclosed techniques.

[0025] Figure 3 illustrates an example implementation of a PMUT.

[0026] Figures 4A and 4B illustrate an example of a process flow for fabricating a PMUT.

[0027] Figure 5A shows a cross-sectional illustrative view of another implementation of a PMUT having a mechanical layer.

[0028] Figure 5B shows a cross-sectional illustrative view of a yet further implementation of a PMUT stack having a mechanical layer.

[0029] Figure 5C shows a cross-sectional illustrative view of a PMUT having a top mechanical layer and an acoustic port formed in the substrate.

[0030] Figure 6A illustrates a plan view of an array of PMUTs, according to some implementations.

[0031] Figures 6B-6E show illustrative cross-sectional elevation views of PMUT arrays in various configurations.

[0032] Figures 7A–7F show cross-sectional elevation views of various anchor structure configurations for a PMUT.

[0033] Figures 8A–8H show top views of various geometrical configurations of PMUTs and anchor structures.

[0034] Figure 9 illustrates a further example of a process flow for fabricating a PMUT.

[0035] Figures 10A–10C illustrate process flows for integrating electronic circuitry with PMUTs as described above.

[0036] Figures 11A–11C illustrate cross-sectional views of various configurations of PMUT ultrasonic sensor arrays.

[0037] Figure 12 illustrates another example of a process flow for fabricating a PMUT.

[0038] Figures 13A and 13B illustrate another example of a process flow for fabricating a PMUT.

[0039] Figures 14A and 14B illustrate another example of a process flow for fabricating a PMUT.

[0040] Figures 15A and 15B illustrate another example of a process flow for fabricating a PMUT.

[0041] Figures 16A and 16B illustrate another example of a process flow for fabricating a PMUT.

[0042] Figures 17A and 17B illustrate another example of a process flow for fabricating a PMUT.

[0043] Figure 18 illustrates another example of a process flow for fabricating a PMUT.

DETAILED DESCRIPTION

[0044] The following description is directed to certain implementations for the purposes of describing the innovative aspects of this disclosure. However, a person having ordinary skill in the art will readily recognize that the teachings herein may be applied in a multitude of different ways. The described implementations may be implemented in any device, apparatus, or system that includes an ultrasonic sensor. For example, it is contemplated that the described implementations may be included in or associated with a variety of electronic devices such as, but not limited to: mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth® devices, personal data assistants (PDAs), wireless electronic

mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, global positioning system (GPS) receivers/navigators, cameras, digital media players (such as MP3 players), camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), mobile health devices, computer monitors, auto displays (including odometer and speedometer displays, etc.), cockpit controls and/or displays, camera view displays (such as the display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (such as in electromechanical systems (EMS) applications including microelectromechanical systems (MEMS) applications, as well as non-EMS applications), aesthetic structures (such as display of images on a piece of jewelry or clothing) and a variety of EMS devices. The teachings herein also may be used in applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes and electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0045] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein. One innovative aspect of the subject matter described in this disclosure can be implemented in a piezoelectric micromechanical ultrasonic transducer (PMUT) configured as a multilayer stack that includes a piezoelectric layer stack and a mechanical layer disposed over a cavity. The cavity may be formed in a lower layer of the multilayer stack, above which is formed the piezoelectric layer stack. A mechanical layer is disposed proximate to the piezoelectric layer stack. The mechanical layer may seal the cavity and, together with the piezoelectric layer stack, may be supported by an anchor structure and form a membrane over the cavity. The membrane may be configured to undergo one or both of flexural motion and vibration when the PMUT

receives or transmits acoustic or ultrasonic signals. The anchor structure may be disposed on the substrate, in a lower layer that is parallel to the piezoelectric layer stack and includes one or more regions of sacrificial material. The sacrificial material may be removed sacrificially to form one or more cavities under the piezoelectric layer stack.

[0046] In some implementations, the mechanical layer has a thickness such that a neutral axis of the multilayer stack is displaced relative to a neutral axis of the piezoelectric layer stack and towards the mechanical layer to allow an out-of-plane bending mode. As a result, the neutral axis of the PMUT stack may be a distance removed from the piezoelectric layer in a direction opposite to the substrate. More particularly, the neutral axis may pass through the mechanical layer, in a plane that is above the piezoelectric layer stack and the cavity and is approximately parallel to the piezoelectric layer stack. In some implementations, the neutral axis of the PMUT stack may be a distance removed from the piezoelectric layer in a direction towards the substrate. More particularly, the neutral axis may pass through the mechanical layer, in a plane that is below the piezoelectric layer stack and is approximately parallel to the piezoelectric layer stack.

[0047] One innovative aspect of the subject matter described in this disclosure can be implemented in an apparatus that includes a one- or two-dimensional array of piezoelectric micromechanical ultrasonic transducer (PMUT) elements positioned below, beside, with, on, or above a backplane of a display or an ultrasonic fingerprint sensor array.

[0048] In some implementations, the PMUT array may be configurable to operate in modes corresponding to multiple frequency ranges. In some implementations, for example, the PMUT array may be configurable to operate in a low-frequency mode corresponding to a low-frequency range (e.g., 50 kHz to 200 kHz) or in a high-frequency mode corresponding to a high-frequency range (e.g., 1 MHz to 25 MHz). When operating in the high-frequency mode, an apparatus may be capable of imaging at relatively higher resolution. Accordingly, the apparatus may be capable of detecting touch, fingerprint, stylus, and biometric information from an object such as a finger placed on the surface of the display or sensor array. Such a high-frequency mode may be referred to herein as a fingerprint sensor mode, a touch mode, or a stylus mode.

[0049] When operating in the low-frequency mode, the apparatus may be capable of emitting sound waves that are capable of relatively greater penetration into air than when the apparatus is operating in the high-frequency mode. Such lower-frequency sound waves may be transmitted through various overlying layers including a cover glass, a touchscreen, a display array, a backlight, or other layers positioned between an ultrasonic transmitter and a display or sensor surface. In some implementations, a port may be opened through one or more of the overlying layers to optimize acoustic coupling from the PMUT array into air. The lower-frequency sound waves may be transmitted through the air above the display or sensor surface, reflected from one or more objects near the surface, transmitted through the air and back through the overlying layers, and detected by an ultrasonic receiver. Accordingly, when operating in the low-frequency mode, the apparatus may be capable of operating in a gesture detection mode, wherein free-space gestures near the display may be detected.

[0050] Alternatively, or additionally, in some implementations, the PMUT array may be configurable to operate in a medium-frequency mode corresponding to a frequency range between the low-frequency range and the high-frequency range (e.g., about 200 kHz to about 1 MHz). When operating in the medium-frequency mode, the apparatus may be capable of providing touch sensor functionality, although with somewhat less resolution than the high-frequency mode.

[0051] The PMUT array may be addressable for wavefront beam forming, beam steering, receive-side beam forming, and/or selective readout of returned signals. For example, individual columns, rows, sensor pixels and/or groups of sensor pixels may be separately addressable. A control system may control an array of transmitters to produce wavefronts of a particular shape, such as planar, circular or cylindrical wave fronts. The control system may control the magnitude and/or phase of the array of transmitters to produce constructive or destructive interference in desired locations. For example, the control system may control the magnitude and/or phase of the array of transmitters to produce constructive interference in one or more locations in which a touch or gesture has been detected.

[0052] In some implementations, PMUT devices may be co-fabricated with thin-film transistor (TFT) circuitry on the same substrate, which may be a glass or plastic substrate in some examples. The TFT substrate may include row and column

addressing electronics, multiplexers, local amplification stages and control circuitry. In some implementations, an interface circuit including a driver stage and a sense stage may be used to excite a PMUT device and detect responses from the same device. In other implementations, a first PMUT device may serve as an acoustic or ultrasonic transmitter and a second PMUT device may serve as an acoustic or ultrasonic receiver. In some configurations, different PMUT devices may be capable of low- and high-frequency operation (e.g. for gestures and for fingerprint detection). In other configurations, the same PMUT device may be used for low- and high-frequency operation. In some implementations, the PMUT may be fabricated using a silicon wafer with active silicon circuits fabricated in the silicon wafer. The active silicon circuits may include electronics for the functioning of the PMUT or PMUT array.

[0053] Figures 2A–2D show examples of implementations of a PMUT stack, configured in accordance with the presently disclosed techniques. In the illustrated implementation, a PMUT 200A includes a mechanical layer 230 disposed above a piezoelectric layer stack 210. The piezoelectric layer stack 210 includes a piezoelectric layer 215 with associated lower electrode 212 and upper electrode 214 disposed, respectively below and above the piezoelectric layer 115. Mechanical layer 230 is disposed over a side of the piezoelectric stack opposite to the substrate.

[0054] The mechanical layer 230 is disposed above a side of the piezoelectric layer stack 210 opposite to a cavity 220 and, together with the piezoelectric layer stack 210, may form a drum-like membrane over the cavity 220. The membrane may be configured to undergo flexural motion and/or vibration when the PMUT receives or transmits acoustic or ultrasonic signals. In the implementation illustrated in Figure 2A, the piezoelectric layer stack 210 is between the cavity 220 and the mechanical layer 230 whereas, in the configuration illustrated in Figure 1, the mechanical layer 130 of PMUT 100 is between the piezoelectric layer stack 110 and the cavity 120. In some implementations, the mechanical layer 230 may be substantially thicker that the piezoelectric layer stack.

[0055] The mechanical layer 230 may be made of an electrically insulating material and may be deposited towards the end of the microfabrication process, i.e. after forming and patterning of the piezoelectric layer stack 210 and the cavity 220 over which the piezoelectric layer stack 210 is disposed. The mechanical layer 230 may be configured

to have dimensions and mechanical properties such that a neutral axis 250 of the PMUT stack is a distance above the piezoelectric layer stack 210. More particularly, the neutral axis 250 is disposed in a plane that includes the mechanical layer 230 above the piezoelectric layer stack 210. It may be observed that the mechanical layer 230 is proximate to a side of the piezoelectric layer stack 210 that is opposite to the cavity 220 and to the substrate 260. In some implementations, the neutral axis 250 may be disposed in a plane that is substantially parallel to the piezoelectric layer stack 210, passing though the piezoelectric layer stack 210 a distance apart from the neutral axis of the piezoelectric layer stack 210 in a direction towards the mechanical layer 230.

[0056] For many multi-layer microstructural devices that include a piezoelectric layer, it is preferable for the neutral axis of the multilayer stack to be a distance apart from the neutral axis of the piezoelectric layer. For example, the mechanical layer 230 of the presently disclosed PMUT causes the neutral axis 250 of the multilayer stack to be a distance apart from the neutral axis of the piezoelectric layer 210. The distance may be determined by the thicknesses of various layers and their elastic properties, which in turn may be determined by resonant frequency and quality factor requirements for the transducer. In some implementations, the neutral axis 250 may be a distance apart from the neutral axis of the piezoelectric layer 210 and displaced towards the mechanical layer 230, yet the neutral axis 250 may still reside within the piezoelectric layer or within the piezoelectric stack. For example, the mechanical layer 230 may have a thickness to allow an out-of-plane bending mode of the multilayer stack. In some implementations, the mechanical layer 230 may be configured to allow the multilayer stack to be primarily excited in an out-of-plane mode, for example a piston mode or a fundamental mode. The out-of-plane mode can cause displacement of portions of the multilayer stack proximate to the cavity 220 (which may be referred to herein as the "released portions"), for example, at the center of a circular, square, or rectangular shaped PMUT. In some implementations, displacement of the neutral axis 250 permits transducer operation in a d_{31} or e_{31} mode in which the neutral axis of the multilayer stack of the membrane in the transducing area may be offset from the neutral axis of the active piezoelectric material in the stack.

[0057] As will be described in more detail below, the mechanical layer 230 may be configured to provide an encapsulation layer that seals cavity 220. In addition, the mechanical layer 230 may serve as a passivation layer for electrodes of the piezoelectric

layer stack 210. By judicious selection of material properties, thickness and internal stress of the mechanical layer 230, certain transducer parameters may be improved. For example, the resonant frequency, static and dynamic deflections, acoustic pressure output, as well as membrane shape (bow) that may result from residual stresses in various layers may be tuned by appropriately configuring the mechanical layer 230.

[0058] In some implementations, the mechanical layer 230 may be configured to provide planarization for attachment of an acoustic coupling layer, for building electrical circuitry after transducer fabrication and/or to provide an insulating layer to create additional routing layers on top of the mechanical layer 230 for capacitive de-coupling with respect to the piezoelectric layer stack 210.

[0059] In some implementations, the mechanical layer 230 may include a recess that reduces the total thickness of part of the PMUT stack. The size and geometry of the recess and recess features may be designed to influence transducer parameters such as resonant frequency, static and dynamic deflections, acoustic pressure output, mechanical quality factor (Q), and membrane shape (bow). Figure 2B shows a cross-sectional view of a PMUT structure having a recess 232 formed in an upper portion of the mechanical layer 230, where the mechanical layer is locally thinned. In the implementation shown, the recess 232 is formed in a central region of the mechanical layer 230 of PMUT 200B.

[0060] It may be observed that the neutral axis 250 moves downwards towards the cavity 220 proximate to the recess 232. The recess 232 may include a substantially axisymmetric feature such as a circle or a ring formed partially into a circular PMUT diaphragm near the diaphragm center, or an angular trench or portions of an angular trench formed near the periphery of a circular diaphragm. In some implementations, the recess 232 may include a square or rectangular feature formed into the mechanical layer 230 near the center of a square or rectangular PMUT diaphragm. In some implementations, recess 232 may include features such as narrow rectangles, local trenches, or slots formed near the periphery of a square, rectangular or circular diaphragm. In some implementations, a sequence of radial slots may be combined with central or peripheral recess features. In some implementations, the recess or recessed features may be formed by etching partially or substantially through the mechanical layer 230, stopping on the underlying piezoelectric layer stack 210. In some

implementations, the recess 232 and/or features thereof may be formed into the mechanical layer 230 based, for example, on an etch time. In some implementations, the mechanical layer 230 may include two or more deposited layers, one of which may serve as an etch stop or barrier layer to allow precise definition of the recess and recessed features during fabrication.

[0061] Figure 2C shows another example of an implementation of a PMUT stack, configured in accordance with the presently disclosed techniques. In the illustrated implementation, the mechanical layer 230 of PMUT 200C is disposed above the cavity 220 and below the piezoelectric layer stack 210. Thus, the mechanical layer 230 is disposed below a side of the piezoelectric layer stack 210 that is facing the cavity 220 and the substrate 260. Together with the piezoelectric layer stack 210, the mechanical layer 230 may form a drum-like membrane or diaphragm over the cavity 220 which is configured to undergo flexural motion and/or vibration when the PMUT receives or transmits acoustic or ultrasonic signals. In some implementations, the mechanical layer 230 may be substantially thicker that the piezoelectric layer stack.

[0062] As will be described in more detail below, the mechanical layer 230 may be configured to provide an encapsulation layer that seals cavity 220. By judicious selection of material properties, thickness and internal stress of the mechanical layer 230, certain transducer parameters may be improved. For example, the resonant frequency, static and dynamic deflections, acoustic pressure output, as well as membrane shape (bow) that may result from residual stresses in various layers may be tuned by appropriately configuring the mechanical layer 230.

[0063] In some implementations, the mechanical layer 230 may include a recess that reduces the total thickness of part of the PMUT stack. The size and geometry of the recess and recess features may be designed to influence transducer parameters such as resonant frequency, static and dynamic deflections, acoustic pressure output, mechanical quality factor (Q), and membrane shape (bow). Figure 2D shows a cross-sectional view of a PMUT structure having a recess 232 formed in the lower portion of the mechanical layer 230, where mechanical layer 230 is locally thinned. In the implementation shown, the recess 232 is formed in a central region of the mechanical layer 230 of PMUT 200D.

[0064] The recess 232 may include a substantially axisymmetric feature such as a circle or a ring formed partially into a circular PMUT diaphragm near the diaphragm center, or an angular trench or portions of an angular trench formed near the periphery of a circular diaphragm. In some implementations, the recess 232 may include a square or rectangular feature formed into the mechanical layer 230 near the center of a square or rectangular PMUT diaphragm. In some implementations, recess 232 may include features such as narrow rectangles, local trenches, or slots formed near the periphery of a square, rectangular or circular diaphragm. In some implementations, a sequence of radial slots may be combined with central or peripheral recess features. In some implementations, the recess or recessed features may be formed by etching partially through an underlying sacrificial layer (not shown) prior to deposition of the mechanical layer 230 and piezoelectric layer stack 210. In some implementations, the recess 232 and/or features thereof may be formed by etching partially into the underlying sacrificial layer based on an etch time. In some implementations, the sacrificial layer may include a stack of two or more deposited layers, one of which may allow local raised portions of the sacrificial layer to be formed prior to deposition of the mechanical layer 230 and piezoelectric layer stack 210, and one of which may serve as an etch stop or barrier layer to allow precise definition of the recess and recessed features during fabrication. In some implementations, the upper surface of mechanical layer 230 may be planarized prior to forming the piezoelectric layer stack 210. For example, mechanical layer 230 may be planarized with chemical-mechanical polishing (CMP), also referred to as chemical-mechanical planarization.

[0065] A better understanding of the presently disclosed techniques may be obtained by referring next to Figure 3. Figure 3 illustrates an example implementation of a PMUT. The illustrated PMUT 300 includes a piezoelectric layer stack 310 disposed above a cavity 320i. As described in more detail hereinbelow, the cavity 320i may be formed by removal of a sacrificial layer formed within an anchor structure 370 through one or more release holes 320o. The anchor structure 370 may be deposited on a substrate 360, as described in more detail below. For scalability, it is preferred that these structures are made using processes common in IC, MEMS and LCD industries.

[0066] In the illustrated implementation, the piezoelectric layer stack 310 includes a piezoelectric layer 315 disposed between a lower electrode 312 and an upper electrode 314. A mechanical layer 330 is disposed above a side of the piezoelectric layer stack

310 opposite to a cavity 320i and, together with the piezoelectric layer stack 310, may form a drum-like membrane or diaphragm over the cavity 320i which is configured to undergo flexural motion and/or vibration when the PMUT receives or transmits acoustic or ultrasonic signals. In some implementations, the mechanical layer 330 may be configured so as to provide that the neutral axis 350 is disposed substantially external to (above) the piezoelectric layer stack 310. Advantageously, the mechanical layer 330 may serve as an encapsulation layer that seals the one or more release holes 320o and isolates the cavity 320i from external liquids and gases, as shown in Section B-B of Figure 3, while also providing additional structural support for the PMUT 300.

[0067] Figures 4A and 4B illustrate an example of a process flow for fabricating a PMUT. In the illustrated example, at step S401, a first layer portion 472 of an anchor structure 470 is deposited onto substrate 360. The first layer portion 472 may also be referred to as an oxide buffer layer. In some implementations, the oxide buffer layer 472 may be a silicon dioxide (SiO_2) layer having a thickness in the range of about 500 to about 30,000 Å. For example, in an implementation the thickness of the oxide buffer layer 472 is about 5,000 Å. The substrate 360 may be a glass substrate, a silicon wafer, or other suitable substrate material.

[0068] In the illustrated example, at step S402, sacrificial regions 425i and 425o may be formed by first depositing a sacrificial layer 425 of a sacrificial material that may include amorphous silicon (a-Si), polycrystalline silicon (poly-Si), or a combination of a-Si and poly-Si onto the oxide buffer layer 472. Alternatively, other sacrificial layer materials may be used such as molybdenum (Mo), tungsten (W), polyethylene carbonate (PEC), polypropylene carbonate (PPC) or polynorbornene (PNB). Step S402 may also include patterning and etching the sacrificial layer 425 to form the sacrificial regions 425i and 425o. Inner sacrificial region 425i may be disposed at a location corresponding to cavity 320i of Figure 3, whereas outer sacrificial region 425o may be disposed at a location corresponding to the release hole 320o. One or more release channels or release vias of sacrificial layer material (not illustrated) may connect the outer sacrificial region 425o with the inner sacrificial region 425i. In some implementations using PEC, PPC or PNB, release channels or release vias may not be needed to form underlying cavities in the PMUTs, as these sacrificial materials may be thermally decomposed to produce gaseous byproducts such as carbon dioxide (CO2), monatomic or diatomic hydrogen, or monatomic or diatomic oxygen that may diffuse

through the somewhat permeable overlying layers. In some implementations, the sacrificial layer 425 has a thickness in the range of about 500 to 20,000 Å. For example, in an implementation the thickness of the sacrificial layer 425 is about 10,000 Å.

[0069] In the illustrated example, at step S403, an anchor portion 474 of the anchor structure 470 is deposited onto the oxide buffer layer 472, so as to encompass the sacrificial regions 425i and 425o. In some implementations, the anchor portion 474 may be an SiO_2 layer having a thickness in the range of about 750 to about 22,000 Å. For example, in an implementation the thickness of the anchor portion 474 is about 12,000 Å. Following deposition, the anchor portion 474 may optionally undergo chemical mechanical planarization (CMP) to planarize the upper portions of the deposited layers. Alternatively, or in addition, the anchor portion 474 may be thinned with a chemical, plasma, or other material removal method.

[0070] In the illustrated example, at step S404, a piezoelectric layer stack 410 is formed on the anchor structure 470. More particularly, in some implementations a sequence of deposition processes may be carried out that results in a first layer (or "barrier layer") 411 of aluminum nitride (AlN), silicon dioxide (SiO_2) or other suitable etch-resistant layer being deposited onto the anchor structure 470 and sacrificial regions 425i and 425o; a lower electrode layer 412 of molybdenum (Mo), platinum (Pt) or other suitable conductive material being deposited onto the barrier layer 411; a piezoelectric layer 415 such as AlN, zinc oxide (ZnO), lead-zirconate titanate (PZT) or other suitable piezoelectric material being deposited onto the lower electrode layer 412; and an upper electrode layer 414 of Mo, Pt or other suitable conductive layer being deposited onto the piezoelectric layer 415. In some implementations, the barrier layer 411 may have a thickness in the range of about 300 to 1000 Å. For example, in an implementation the thickness of the barrier layer 411 is about 500 Å. In some implementations, the lower electrode layer 412 may have a thickness in the range of about 1000 to 30,000 Å. For example, in an implementation the thickness of the lower electrode layer 412 is about 1000 Å. In some implementations, the piezoelectric layer 415 may have a thickness in the range of about 1000 to 30,000 Å. For example, in an implementation the thickness of the active piezoelectric layer 415 is about 10,000 Å. In some implementations, the upper electrode layer 414 may have a thickness in the range of about 1000 to 30,000 Å. For example, in an implementation the thickness of the upper electrode layer 414 is

about 1000 Å. The first layer or barrier layer 411 may, in some implementations, serve as a seed layer for the subsequent lower electrode and/or piezoelectric layer deposition.

[0071] Following step S404, a sequence of patterning and forming operations may be executed so as to selectively expose, in a desired geometric configuration, the various layers included in the piezoelectric layer stack 410. In the illustrated example, at step S405, the upper electrode layer 414 of molybdenum may undergo patterning and etching to expose selected areas of the piezoelectric layer 415. At step S406, the piezoelectric layer 415 of AlN or other piezoelectric material may undergo patterning and etching so as to expose selected areas of lower electrode layer 412. At step S407, the lower electrode layer 412 of molybdenum may undergo patterning and etching so as to us expose selected areas of barrier layer 411.

[0072] In the illustrated example, at step S408, an isolation layer 416 may be deposited onto the upper electrode layer 414 and other surfaces exposed during the preceding masking and etching operations of steps S404 through S407. In some implementations, the isolation layer 416 may be SiO_2, for example, and have a thickness in the range of about 300 to 5,000 Å. For example, in an implementation the thickness of the isolation layer 416 is about 750 Å. Step S408 may also include patterning and etching the isolation layer 416 so as to expose selected areas of upper electrode layer 414, lower electrode layer 412, and outer sacrificial region 425o. In some implementations using thermally decomposable sacrificial materials such as PEC, PPC or PNB, patterning and etching the isolation layer 416 need not expose any outer sacrificial regions 425o.

[0073] In the illustrated example, at step S409, a metal interconnect layer 418 may be deposited onto the surfaces exposed during the preceding masking and etching operations of step S408. The interconnect layer 418 may be aluminum, for example, and have a thickness in the range of about 1000 to 50,000 Å. For example, in an implementation the thickness of interconnect layer 418 is about 1000 Å. Step S409 may also include patterning and etching the interconnect layer 418 so as to expose selected areas of the isolation layer 416 and the outer sacrificial region 425o. In implementations using thermally decomposable sacrificial materials, patterning and etching the interconnect layer 418 need not expose any outer sacrificial regions 425o.

[0074] In the illustrated example, at step S410, the sacrificial material, deposited at step S402 to form inner sacrificial region 425i and outer sacrificial region 425o, may be

removed, thereby forming release hole 420o and cavity 420i. Removal of the sacrificial material from the inner sacrificial region 425i, the outer sacrificial region 425o, and one or more connecting release channels between the outer and inner sacrificial regions 425o and 425i may occur through the release hole 420o. For example, the a-Si/PolySi sacrificial layer 425 may be removed by exposing the sacrificial material to an etchant, for example xenon difluoride (XeF_2). By providing a release channel or via that couples outer sacrificial region 425o with inner sacrificial region 425i, substantially all of the sacrificial material of the inner sacrificial region 425i may be removed through the one or more release holes 420o. In some implementations using thermally decomposable sacrificial materials, raising the temperature of the substrate to a decomposition temperature (e.g. about 200C for PEC and about 425C for PNB) may selectively remove the sacrificial material, with gaseous byproducts diffusing through the overlying layers or emanating through any exposed release channels or vias during decomposition.

[0075] In the illustrated example, at step S411, a mechanical layer 430 may be deposited onto surfaces exposed during the preceding masking and etching operations of Step 409. The mechanical layer 430 may include SiO_2, SiON, silicon nitride (SiN), other dielectric material, or a combination of dielectric materials or layers. The mechanical layer 430 may have a thickness in the range of about 1000 to 50,000 Å. For example, in an implementation the thickness of mechanical layer 430 is about 20,000 Å. Step S409 may also include patterning and etching the mechanical layer 430 so as to achieve a desired profile. As illustrated in Figures 4A-4B, the mechanical layer 430 may be configured to mechanically seal (encapsulate) the release hole 420o. As a result, deposition of the mechanical layer 430 at step S411 may provide a substantial degree of isolation between the encapsulated cavity 420i and the ambient environment. The mechanical layer 430 may also serve as a passivation layer over the upper electrode layer 414 and other exposed layers. In implementations using thermally decomposable sacrificial materials, the deposition of the mechanical layer 430 may not be needed to seal or otherwise encapsulate the underlying cavity 420i.

[0076] Figure 5A shows a cross-sectional illustrative view of another implementation of a PMUT having a mechanical layer. In the illustrated implementation, PMUT 500A is formed by forming an anchor structure 570 on a substrate 560 such as a silicon wafer or a glass substrate. A piezoelectric layer stack 510, including a lower electrode layer 512, a piezoelectric layer 515 and an upper electrode layer 514, is formed on the anchor

structure 570. A portion of the piezoelectric layer stack 510 is removed from the substrate 560 using, for example, a sacrificial etchant to selectively remove a sacrificial layer (not shown) and form a cavity 520 between the piezoelectric layer stack 510 and the substrate 560. Portions of the sacrificial layer in the cavity region may be accessed through a central release hole 522 that extends through a central portion of the piezoelectric layer stack 510 of the PMUT 500A. Alternatively, one or more release holes and release channels as described above may be used for sacrificial material removal to form the cavity 520. A mechanical layer 530 may be positioned on or otherwise disposed on the piezoelectric layer stack 510. The mechanical layer 530 may serve as a sealing layer for the release hole 522. The mechanical layer 530, together with the piezoelectric layer stack 510, may form a drum-like membrane over the cavity 520 which is configured to undergo flexural motion and/or vibration when the PMUT receives or transmits acoustic or ultrasonic signals. A neutral axis 550 passes through the mechanical layer 530, positioned above the piezoelectric layer stack 510 on a side opposite to the cavity 520. In some implementations, the neutral axis 550 may be disposed in a plane that is substantially parallel to the piezoelectric layer stack 510, passing though the piezoelectric layer stack 510 a distance apart from the neutral axis of the piezoelectric layer stack 510 in a direction towards the mechanical layer 530.

[0077] In some implementations, the mechanical layer 530 may be applied by laminating, adhering or otherwise bonding the mechanical layer 530 to an exposed upper surface of the piezoelectric layer stack 510. For example, the mechanical layer 530 may include a thick patternable film such as SU8, polyimide, a photosensitive silicone dielectric film, a cyclotene polymer film such as benzocyclobutene or BCB, a dry resist film, or a photo-sensitive material. Alternatively, the mechanical layer 530 may include a laminated layer of plastic such as polyethylene terephthalate (PET), polyethylene napthalate (PEN), polyimide (PI), polycarbonate (PC), a silicone, an elastomeric material, or other suitable material. The mechanical layer 530 may be laminated or otherwise bonded with an adhesive or other connective layer. Examples of adhesives include silicones, polyurethane, thermoplastics, elastomeric adhesives, thermoset adhesives, UV-curable adhesives, hot curing adhesives, hot-melt adhesives, phenolics, one- and two-part epoxies, cyanoacrylates, acrylics, acrylates, polyamides, contact adhesives and pressure sensitive adhesives (PSAs). The mechanical layer 530 may be deposited, coated, laminated, adhered or otherwise bonded directly or indirectly

to the piezoelectric layer stack and may have a wide range of thicknesses, from less than 2 microns to over 500 microns, for example.

[0078] Figure 5B shows a cross-sectional illustrative view of a yet further implementation of a PMUT stack having a mechanical layer. In the illustrated implementation, the mechanical layer 530 of PMUT 500B includes an upper mechanical layer 530b that may be laminated or otherwise attached to a deposited lower mechanical layer 530a positioned above a piezoelectric layer stack 510 on a side opposite to the cavity 520 and substrate 560. The lower mechanical layer 530a may include one or more deposited layers, as described above. One or more release holes 522 may be formed in the lower mechanical layer 530a and in the underlying piezoelectric layer stack 510 to allow removal of sacrificial material to form the cavity 520. In the illustrated implementation, the release hole 522 may be sealed upon attachment of upper mechanical layer 530b onto an exposed upper surface of lower mechanical layer 530a. As a result, the upper mechanical layer 530b may serve as a sealing layer for the release hole 522. The neutral axis 550 may pass through either lower mechanical layer 530a or upper mechanical layer 530b, depending on the thicknesses and elastic moduli of the individual layers. In a region near the release hole 522, a central portion of the neutral axis 550 may be disposed at a location farther away from the cavity 520 than remaining portions of the neutral axis.

[0079] Figure 5C shows a cross-sectional illustrative view of a PMUT having a top mechanical layer and an acoustic port formed in the substrate. The acoustic port 580 may be formed in the substrate 560 underneath the piezoelectric layer stack 510. The acoustic port 580 may be configured to provide acoustic coupling between the PMUT 500C and the backside of the substrate 560. The cross-sectional dimensions of the acoustic port 580 may be substantially the same, larger than, or smaller than the dimensions of a cavity 520 between the piezoelectric layer stack 510 and the acoustic port 580. The cavity 520 may be formed prior to or after formation of the acoustic port 580 by removal of sacrificial material in the cavity region. A mechanical layer 530 may be disposed on the piezoelectric layer stack 510. A neutral axis 550 of the multilayer stack may pass through the mechanical layer 530, separated by a distance from the piezoelectric stack 510 in a direction opposite to the cavity 520 and the acoustic port 580. The acoustic port 580 may allow the transmission of ultrasonic or acoustic waves from the PMUT 500C to a region exterior to the substrate 560. Similarly, the acoustic

port 580 allows the reception of ultrasonic or acoustic waves by the PMUT 500C from a region exterior to the substrate 560.

[0080] Figures 5A-5C illustrate implementations of individual PMUTs and PMUT stacks, however the mechanical layer 530 may extend beyond an individual PMUT stack and cover one or more adjacent PMUTs. Figure 6A illustrates a plan view of an array of PMUTs, according to some implementations. Each PMUT 600 is configured on a common substrate 660 with a bonded mechanical layer 630 extending over and between two or more PMUTs 600 in the PMUT array 600A. The bonded portion of mechanical layer 630 may serve as an acoustic coupling layer. In one mode of operation, the PMUTs 600 in the array may be simultaneously actuated to generate and transmit a quasi-plane wave from an upper surface of the mechanical layer 630. In some implementations, the mechanical layer 630 is continuous between adjacent PMUTs. In some implementations, the mechanical layer 630 may be patterned, diced, sliced, slit, cut or otherwise formed to align with the peripheries of PMUTs 600 or to selectively expose portions of one more layers underlying the mechanical layer 630 such as metal bond pads. Although the implementation illustrated in Figure 6A includes an array of circular PMUTs 600, other shapes are within the contemplation of the present disclosure, such as square-shaped or rectangular-shaped PMUTs. For example, in some implementations, hexagonal-shaped PMUTs may be contemplated whereby an increase in packing density in terms of number of pixels per unit area may be obtained. The array of PMUTs 600 may be configured as a square or rectangular array as illustrated in Figure 6A. In some implementations, the array may include staggered rows or columns of PMUTs 600, such as a triangular or hexagonal array.

[0081] Figures 6B-6E show illustrative cross-sectional elevation views of PMUT arrays in various configurations. PMUT array 600B includes an array of PMUTs 600 disposed on a substrate 660. An upper mechanical layer 630 may be laminated, bonded or otherwise attached to an upper surface of the array of PMUTs 600, such as with an adhesive layer 632. Flexural motions and/or vibrations of each PMUT 600 may bend, flex, compress or expand portions of the mechanical layer 630. In some implementations, synchronous vibrations of PMUTs 600 in the PMUT array 600B may launch substantially planar ultrasonic waves up and through the mechanical layer 630. In some implementations, the mechanical layer 630 may bend and flex with controlled actuation of underlying PMUTs 600 to launch acoustic or ultrasonic waves with

controlled wavefronts, which may be useful for transmit-side beamforming applications. In some implementations, ultrasonic waves returning through the mechanical layer 630 may cause flexural motions and/or vibrations of the underlying PMUTs 600 and be detected accordingly. In some implementations, the mechanical layer 630 may serve as an acoustic coupling medium. In some implementations, the mechanical layer 630 may serve as an encapsulation layer that may mechanically encapsulate or otherwise seal cavities within PMUTs 600. The mechanical layer 630 may include, for example, a layer of polymer or plastic such as polycarbonate (PC), polyimide (PI), or polyethylene terephthalate (PET). The adhesive layer 632 may include a thin layer of epoxy, UV-curable material, pressure-sensitive adhesive (PSA), or other suitable adhesive material that couples the mechanical layer 630 to the PMUTs 600 in the PMUT array 600B.

[0082] Figure 6C illustrates a PMUT array 600C configured with a portion of a cover glass, enclosure wall, button cover or platen 690 overlying a mechanical layer 630 and an array of PMUTs 600 that are disposed on a substrate 660. Adhesive layers 632 and 634 may mechanically connect the mechanical layer 630 to the PMUTs 600 and the overlying platen 690. In some implementations, the mechanical layer 630 may provide acoustic coupling between the array of PMUTs 600 and the overlying platen 690 for use in ultrasonic fingerprint sensors, touch sensors, ultrasonic touch pads, stylus detection, biometric sensors, or other ultrasonic devices. An acoustic impedance matching layer 692 such as a polymeric coating may be deposited, screened, painted, adhered or otherwise disposed on an outer surface of the cover glass or platen 690. The acoustic matching layer 692 may serve as a scratch-resistant coating. Further description of the mechanical layer 630 is provided with respect to Figure 6B above.

[0083] Figure 6D illustrates a PMUT array 600D with a mechanical layer 630 coupled to an array of PMUTs 600 via an array of micropillars 636. The micropillars 636 may provide mechanical and acoustic coupling between PMUTs 600 and the overlying mechanical layer 630. The micropillars 636 may serve as acoustic waveguides, allowing acoustic or ultrasonic waves generated by the PMUTs 600 to travel through the waveguides with some level of acoustic isolation between neighboring PMUTs 600. Similarly, the micropillars 636 may serve as acoustic waveguides that can guide ultrasonic waves back to the PMUTs 600, which may act as either ultrasonic transmitters or ultrasonic receivers. In some implementations, the micropillars 636 may be substantially square, rectangular or circular in cross section, aligning substantially

with the periphery of each PMUT 600 in the PMUT array 600D, with each micropillar 636 separated from a neighboring micropillar 636 by a gap. In some implementations, the micropillars 636 may be formed from a photo-patternable polymer, such as a photoresist or a photoimageable polymer laminate (e.g., a layer of SU-8 negative-acting photoresist, a photosensitive silicone dielectric film or a cyclotene polymer film). For example, a relatively thick layer of negative or positive photoresist may be applied to an upper surface of PMUTs 600 on the substrate 660, dried, patterned with a suitable photomask, developed, and baked to form the micropillars 636. In some implementations, a dry-resist photo-patternable film, also known as a dry-resist film, may be pre-patterned prior to alignment and attachment to the array of PMUTs 600. The dry-resist film may have a layer of photo-sensitive material on a relatively inert backing layer such as acetate, PC, PI or PET. In some implementations, an adhesion promoter or adhesive layer 632 may be positioned between the micropillars 636 and the underlying PMUTs 600 to provide mechanical and acoustic coupling. In some implementations, the backing layer for the dry-resist film may be removed. Alternatively, the backing layer for the dry-resist film may be retained and serve as a mechanical layer 630. The acoustic waveguides (e.g. micropillars 636) formed photolithographically on one or more PMUTs 600 may provide a low-cost batch process with tight alignment and geometry definition capability for PMUTs disposed on a substrate or configured in a PMUT array. In some implementations, a polymer laminate may be used as a tent to cover a plurality of release holes associated with the PMUTs 600 while planarizing the PMUT topology prior to attachment of a cover glass or platen.

[0084] Figure 6E illustrates a PMUT array 600E with an array of micropillars 636 and a platen 690 serving as a fingerprint sensor array. An acoustic matching layer 692 may be disposed on an outer surface of a cover glass or platen 690. PMUTs 600 in the PMUT array 600E on a substrate 660 may generate and transmit ultrasonic waves 664 that propagate through the micropillars 636, through an optional mechanical layer 630, and into the platen 690. A portion of the ultrasonic waves 664 may reflect back from an outer surface of the platen 690 or acoustic matching layer 692, with an amplitude dependent in part on the acoustic mismatch between the platen 690 or acoustic matching layer 692 and an overlying object such as the fingerprint ridges and valleys of a finger of a user placed in contact with the outer surface of the platen 690. The reflected waves may travel back through the acoustic matching layer 692 and platen 690, through

optional mechanical layer 630 and micropillars 636, and be detected by the underlying PMUTs 600. Adhesive layers 632 and 634 may serve to mechanically and acoustically couple together various layers of the PMUT array 600E.

[0085] Figures 7A–7F show cross-sectional elevation views of various anchor structure configurations for a PMUT 700. Figure 7A shows a peripheral anchor structure 770 positioned between a substrate 760 and a piezoelectric layer stack 710 having a mechanical layer 730 formed thereon. The mechanical layer 730, together with the piezoelectric layer stack 710, may form a drum-like membrane or diaphragm over a cavity 720 and may be configured to undergo flexural motion and/or vibration when the PMUT receives or transmits acoustic or ultrasonic signals. In the illustrated implementations, a mechanical neutral axis 750 passes through the mechanical layer 730 and above the piezoelectric layer stack 710 and cavity 720. In some implementations, the neutral axis 750 may be displaced relative to the neutral axis of the piezoelectric layer stack 710 and towards the mechanical layer 730 that is positioned above the piezoelectric layer stack 710, to allow out-of-plane bending modes.

[0086] Figure 7B shows a central anchor structure 770 positioned between the piezoelectric layer stack 710 and the substrate 760. Figure 7C shows a variant of the peripheral anchor structure 770 with a central release hole 722. The configuration shown in Figure 7C may alternatively represent a pair of cantilevered PMUTs 700. The dual vertical arrows in Figures 7A-7F represent one mode of operation, such as an out-of-plane bending mode, where the released portions of the PMUT 700 may be driven to oscillate or otherwise deflect in the directions indicated by the corresponding arrows. Figure 7D shows a PMUT 700 with a peripheral anchor structure 770 positioned between a substrate 760 and the piezoelectric layer stack 710, with a mechanical layer 730 positioned between the piezoelectric layer stack 710 and the cavity 720. The mechanical neutral axis 750 of the multilayer stack may be displaced relative to the neutral axis of the piezoelectric layer stack 710 in a direction towards the underlying cavity 720 and substrate 760, to allow one or more out-of-plane bending modes. Figure 7E shows a PMUT 700 with a central anchor structure 770 positioned between the piezoelectric layer stack 710 and the substrate 760, with a mechanical layer 730 positioned between the piezoelectric layer stack 710 and the cavity 720. Similar to the PMUT 700 in Figure 7D, the mechanical neutral axis 750 of the multilayer stack may be displaced from the neutral axis of the piezoelectric layer stack 710 towards the cavity

720 and the substrate 760. Figure 7F shows a PMUT 700 with a peripheral anchor structure 770 having a central release hole 722. Alternatively, the configuration shown in Figure 7F may represent a pair of cantilevered PMUTs 700. The mechanical layer 730 is positioned between the piezoelectric layer stack 710 and the cavity 720. The mechanical neutral axis 750 of the multilayer stack may be displaced from the center of the piezoelectric layer stack 710 towards the underlying cavity 720 and substrate 760.

[0087] Figures 8A–8H show top views of various geometrical configurations of PMUTs and anchor structures. A circular PMUT 800 with a circular mechanical layer 830 and a peripheral anchor structure 870 is shown in Figure 8A. A circular PMUT 800 with a circular mechanical layer 830 and a central anchor structure 870 is shown in Figure 8B. Figures 8C and 8D show square PMUTs 800 with a peripheral anchor structure 870 and a central anchor structure 870, respectively. Figures 8E and 8F show long rectangular PMUTs 800 with a peripheral anchor structure 870 and a centered anchor structure 870, respectively. Figure 8G shows a rectangular PMUT 800 with a pair of side anchor structures 870. Figure 8H shows a pair of rectangular PMUTs 800 also referred to as ribbon PMUTs or PMUT strips with side anchor structures 870a and 870b. The PMUTs 800 shown in Figures 8A–8H are illustrative, with connective electrodes, pads, traces, etch holes and other features omitted for clarity. In some implementations, particularly those with central or otherwise centered anchor structures, the anchor structures may be referred to as anchor posts or simply "posts". The PMUTs shown in Figures 8A-8H may be configured with substantial portions of the mechanical layer positioned above the piezoelectric layer stack, as shown in Figure 2A, or with substantial portions of the mechanical layer positioned below the piezoelectric layer stack, as shown in Figure 2C.

[0088] The PMUTs described in this disclosure may in general be sealed or unsealed. Sealed PMUTs have at least a portion of an associated cavity sealed from the external environment. In some implementations, sealed PMUTs may have a vacuum sealed inside the cavity region. In some implementations, the sealed PMUTs may have a gas such as argon, nitrogen or air at a reference pressure within the cavity region that is below, above or substantially at atmospheric pressure. The acoustic performance of sealed PMUTs may exceed that of unsealed PMUTs, in that damping of the PMUT structure may be higher with unsealed PMUTs. In some implementations, unsealed PMUTs may be utilized. For example, PMUTs with a central anchor or post structure may be unsealed or otherwise considered to be an open structure. Unsealed PMUTs

may allow liquid, gas, or other viscous medium to penetrate the cavity region. PMUTs with associated acoustic ports, for example, may be unsealed on one or both sides of the PMUT to allow the transmission and reception of acoustic or ultrasonic waves. One or more acoustic ports such as holes etched or otherwise formed in the substrate under the PMUT may be included with the various implementations of PMUTs and fabrication methods described above. In some implementations, an unsealed PMUT or an array of unsealed PMUTs may be covered with a cover layer that may serve as a top mechanical layer or a supplement to the top mechanical layer, such as the upper mechanical layer 530b shown in Figure 5B. The cover layer may extend over one or more release holes associated with the PMUT(s) and attached to the PMUT membranes with, for example, an adhesive layer, to seal the PMUT cavities and provide isolation from ambient gases and liquids.

[0089] Figure 9 illustrates a further example of a process flow for fabricating a PMUT. Method 900 includes a step 910 for forming an anchor structure over a substrate. The substrate may include a glass substrate such as a glass plate, panel, sub-panel or wafer. In some implementations, the substrate may be plastic or may be flexible. The substrate may include TFT circuitry. Alternatively, the substrate may include a semiconductor substrate such as silicon wafer with or without prefabricated integrated circuitry. The anchor structure may include one or more layers of deposited dielectric materials such as silicon dioxide, silicon nitride, or silicon oxynitride. The anchor structure may include a silicide such as nickel silicide. The anchor structure may be disposed proximate to regions of sacrificial material patterned so as to allow for the eventual formation of one or more cavities, release holes, vias, and channels. The sacrificial material may include amorphous silicon (a-Si), polycrystalline silicon (poly-Si), or a combination of a-Si and poly-Si. A planarizing sequence such as CMP or chemical thinning may be used to planarize the anchor structure and the sacrificial layer.

[0090] In step 920, a piezoelectric layer stack is formed over the anchor structure. The piezoelectric layer stack may include a piezoelectric layer such as AlN, ZnO or PZT with one or more electrode layers electrically coupled to the piezoelectric layer. The piezoelectric layer stack may be patterned and etched to form via or release holes and other features. In step 930, the sacrificial material is removed. Removing the sacrificial material may be achieved by removal of the sacrificial layer from a cavity region through release holes. In some implementations, removing the sacrificial material may

be achieved by etching of the sacrificial layer through one or more release vias or holes and one or more release channels that may connect one or more outer release holes with the cavity region. In step 940, a mechanical layer is disposed over the piezoelectric layer stack, such that a neutral axis of the resulting assembly is located a distance towards the mechanical layer and away from the substrate so that the neutral axis passes through the mechanical layer and does not pass through the piezoelectric layer stack. In some implementations, the mechanical layer may be disposed over the piezoelectric layer stack with a thickness such that the neutral axis of the resulting multilayer stack is displaced relative to the neutral axis of the piezoelectric layer stack and towards the mechanical layer to allow out-of-plane bending modes. In some implementations, the mechanical layer may include a deposited layer, a composite of one or more layers, a bonded layer, or a bonded layer over a deposited layer or set of layers. The mechanical layer may be patterned to form features such as a top recess where the mechanical layer is locally thinned. As shown in step 950 and depending on the implementation, one or more release holes may be sealed when the mechanical layer is disposed over the piezoelectric layer stack.

[0091] Figures 10A–10C illustrate process flows for integrating electronic circuitry with PMUTs as described above. Figure 10A illustrates a "TFT first" process 1000a, where TFT or other integrated circuitry is formed on/in a substrate in step 1010, followed by formation of one or more PMUTs on the substrate that may be on top of or beside the circuitry, as shown in step 1020. This approach allows a first fabrication facility to form active circuitry on a substrate, and a second fabrication facility to receive the substrate with the active circuitry and form the PMUTs on the substrate. Figure 10B illustrates a "TFT last" process 1000b, where TFT or other integrated circuitry is formed on/in a substrate after the PMUTs are formed, as shown in steps 1040 and 1050. Planarization steps and thick dielectric layers may serve to provide surfaces onto which TFT circuitry may be formed, as described above. Figure 10C illustrates a combined or co-fabricated process 1000c where PMUTs and active circuitry are formed on a substrate, as shown in steps 1060 and 1070. This approach may benefit from utilizing common layers for both active circuitry and PMUT formation that can reduce the total number of masking and deposition steps required compared to a PMUT-first or PMUT-last process. For example, metal interconnect layers for TFT or silicon-based transistors may be used for the upper or lower electrode layers for the PMUTs. In

another example, dielectric layers between metal layers for the active circuitry may be used for buffer or barrier layers in the PMUTs, or for use in the mechanical layer or for sealing. Etch sequences for metal or dielectric layers may be used in common to form portions of the active circuitry and the PMUTs on the substrate. In another example, passivation layers for the TFT or active circuitry may be used for passivation of the PMUT devices. In some implementations, the TFT or active circuitry may include row and column addressing electronics, multiplexers, local amplification stages or control circuitry. In some implementations, an interface circuit including a driver stage and a sense stage may be used to excite a PMUT device and detect responses from the same or another PMUT device. In some implementations, the active silicon circuits may include electronics for the functioning of the PMUT or a PMUT array.

[0092] Figures 11A–11C illustrate cross-sectional views of various configurations of PMUT ultrasonic sensor arrays. Figure 11A depicts an ultrasonic sensor array 1100A with PMUTs as transmitting and receiving elements that may be used, for example, as an ultrasonic fingerprint sensor, an ultrasonic touchpad, or an ultrasonic imager. PMUT sensor elements 1162 on PMUT sensor array substrate 1160 may emit and detect ultrasonic waves. As illustrated, an ultrasonic wave 1164 may be transmitted from a PMUT sensor element 1162. The ultrasonic wave 1164 may travel through an acoustic coupling medium 1165 and a platen 1190a towards an object 1102 such as a finger or a stylus positioned on an outer surface of the platen 1190a. A portion of the outgoing ultrasonic wave 1164 may be transmitted through the platen 1190a and into the object 1102, while a second portion is reflected from a surface of platen 1190a back towards the sensor element 1162. The amplitude of the reflected wave depends in part on the acoustic properties of the object 1102. The reflected wave may be detected by the sensor element 1162, from which an image of the object 1102 may be acquired. For example, with sensor arrays having a pitch of about 50 microns (about 500 pixels per inch), ridges and valleys of a fingerprint may be detected. An acoustic coupling medium 1165 such as an adhesive, gel, a compliant layer or other acoustic coupling material may be provided to improve coupling between an array of PMUT sensor elements 1162 disposed on the sensor array substrate 1160 and the platen 1190a. The acoustic coupling medium 1165 may aid in the transmission of ultrasonic waves to and from the sensor elements 1162. The platen 1190a may include, for example, a layer of

glass, plastic, sapphire, or other platen material. An acoustic impedance matching layer (not shown) may be disposed on an outer surface of the platen 1190a.

[0093] Figure 11B depicts an ultrasonic sensor and display array 1100B with PMUT sensor elements 1162 and display pixels 1166 co-fabricated on a sensor and display substrate 1160. The sensor elements 1162 and display pixels 1166 may be collocated in each cell of an array of cells. In some implementations, the sensor element 1162 and the display pixel 1166 may be fabricated side-by-side within the same cell. In some implementations, part or all of the sensor element 1162 may be fabricated above or below the display pixel 1166. Platen 1190b may be positioned over the sensor elements 1162 and the display pixels 1166 and may function as or include a cover lens or cover glass. The cover glass may include one or more layers of materials such as glass, plastic or sapphire, and may include provisions for a capacitive touchscreen. An acoustic impedance matching layer (not shown) may be disposed on an outer surface of the platen 1190b. Ultrasonic waves 1164 may be transmitted and received from one or more sensor elements 1162 to provide imaging capability for an object 1102 such as a stylus or a finger placed on the cover glass 1190b. The cover glass 1190b is substantially transparent to allow optical light from the array of display pixels 1166 to be viewed by a user through the cover glass 1190b. The user may choose to touch a portion of the cover glass 1190b, and that touch may be detected by the ultrasonic sensor array. Biometric information such as fingerprint information may be acquired, for example, when a user touches the surface of the cover glass 1190b. An acoustic coupling medium 1165 such as an adhesive, gel, or other acoustic coupling material may be provided to improve acoustic, optical and mechanical coupling between the sensor array substrate 1160 and the cover glass. In some implementations, the coupling medium 1165 may be a liquid crystal material that may serve as part of a liquid crystal display (LCD). In LCD implementations, a backlight (not shown) may be optically coupled to the sensor and display substrate 1160. In some implementations, the display pixels 1166 may be part of an amorphous light-emitting diode (AMOLED) display with light-emitting display pixels. In some implementations, the ultrasonic sensor and display array 1100B may be used for display purposes and for touch, stylus or fingerprint detection.

[0094] Figure 11C depicts an ultrasonic sensor and display array 1100C with a sensor array substrate 1160a positioned behind a display array substrate 1160b. An acoustic

coupling medium 1165a may be used to acoustically couple the sensor array substrate 1160a to the display array substrate 1160b. An optical and acoustic coupling medium 1165b may be used to optically and acoustically couple the sensor array substrate 1160a and the display array substrate 1160b to a cover lens or cover glass 1190c, which may also serve as a platen for the detection of fingerprints. An acoustic impedance matching layer (not shown) may be disposed on an outer surface of the platen 1190c. Ultrasonic waves 1164 transmitted from one or more sensor elements 1162 may travel through the display array substrate 1160b and cover glass 1190c, reflect from an outer surface of the cover glass 1190c, and travel back towards the sensor array substrate 1160a where the reflected ultrasonic waves may be detected and image information acquired. In some implementations, the ultrasonic sensor and display array 1100C may be used for providing visual information to a user and for touch, stylus or fingerprint detection from the user. Alternatively, a PMUT sensor array may be formed on the backside of the display array substrate 1160b. Alternatively, the sensor array substrate 1160a with a PMUT sensor array may be attached to the backside of the display array substrate 1160b, with the backside of the sensor array substrate 1160a attached directly to the backside of the display array substrate 1160b, for example, with an adhesive layer or adhesive material (not shown).

[0095] As described above in connection with Figures 4A and 4B, a process flow for forming a PMUT stack according to the presently disclosed techniques may include a sequence of microfabrication processes, including deposition, patterning, etching and CMP. In addition to the process flow illustrated in Figures 4A and 4B, a number of alternative process flows are within the contemplation of the present disclosure.

[0096] Figure 12 illustrates another example of a process flow for fabricating a PMUT. In the illustrated example, a process 1200 incorporates a silicide formation process that can planarize the top of the anchor structure and the top of the sacrificial layer. As a result, a CMP sequence included in step S403 (Figure 4A) may be avoided. The silicide may form at least a portion of the anchor structure for the PMUT, and serve as an etch-resistant layer during removal of the sacrificial material to form the PMUT cavity.

[0097] The process 1200 may begin with step S401. Step S401, as described hereinabove in connection with Figure 4A, may include depositing a first layer portion 472 of anchor structure 470 onto substrate 360.

[0098] At step S1202, sacrificial regions 425i and 425o (Figure 4A) are formed by first depositing a sacrificial layer 425 of a sacrificial material that may include amorphous silicon (a-Si), polycrystalline silicon (poly-Si), or a combination of a-Si and poly-Si onto the oxide buffer layer 472. Alternatively, other sacrificial layer materials may be used such as molybdenum (Mo) or tungsten (W). In some implementations, the sacrificial layer 425 has a thickness in the range of about 500 to 20,000Å. For example, in an implementation the thickness of the sacrificial layer 425 is about 10,000Å.

[0099] At step S1203 a nickel layer 1275 may be deposited onto the sacrificial layer 425. The nickel layer 1275 may have a thickness in a range of about 250 to 10,000 Å. For example, in an implementation the thickness of the nickel layer 1275 is about 5000 Å. Step S1203 may also include patterning and etching the nickel layer 1275 so as to expose the sacrificial layer 425 in selected regions.

[0100] At step S1204, a silicide formation process is contemplated whereby a layer of metal such as nickel may be deposited and patterned on top of the sacrificial layer 425 of polycrystalline or amorphous silicon. The silicide may be formed by interacting the metal with the silicon of the sacrificial layer 425. Nickel silicide may be formed, for example, by interacting the patterned nickel layer 1275 with the silicon of the sacrificial layer 425. Formation of silicide in portions 1276 of the sacrificial layer 425 may be achieved by diffusing the metal locally into the sacrificial layer, consuming the deposited metal and forming the silicide down to an underlying buffer layer (such as SiO2 or SiN on a silicon substrate) or down to an insulating substrate (such as glass). Metal diffusion into the underlying sacrificial layer can be achieved, for example, by elevating the process temperature of the substrate and deposited layers to a silicide formation temperature for a predetermined period of time. Alternatively, a rapid thermal anneal (RTA) process may be used to quickly elevate the temperature to allow intermetallic diffusion and silicide formation. Alternatively, application of focused laser light of a suitable wavelength, energy and time may be used to locally form the silicide, which may be particularly attractive with the use of transparent substrates where the laser light may be applied from either above or below the substrate.

[0101] Subsequent steps of the process 1200 may be substantially identical to steps S404 through S411 described hereinabove in connection with Figures 4A and 4B.

[0102] Figures 13A and 13B illustrate another example of a process flow for fabricating a PMUT. Process flow 1300 provides three layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate. In a first step S1301, a substrate 360 is provided, such as a glass, plastic or semiconductor (e.g. silicon) substrate upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer layer, may be deposited on the substrate 360. A sacrificial layer 425 of a sacrificial material may be deposited on the buffer layer. The sacrificial layer 425 may be patterned and etched to form one or more inner sacrificial regions 425i and outer sacrificial regions 425o (not shown), with the etchant stopping on the underlying buffer layer or substrate. In step S1302, an anchor portion 474 of the anchor structure 470 such as a silicon dioxide layer may be deposited onto the buffer layer and the sacrificial region 425i, then thinned using CMP to form a substantially planar surface while retaining a small portion 474i of the silicon dioxide layer above the sacrificial region 425i. In step S1303, a multilayer stack may be deposited including a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, a piezoelectric layer 415, and an upper electrode layer 414. The upper electrode layer may be patterned and etched to form upper electrodes 414a and 414b that are in electrical contact with the piezoelectric layer 415. In step S1304, the piezoelectric layer 415 may be patterned and etched, stopping on the lower electrode layer 412. In step S1305, the lower electrode layer 412 may be patterned and etched along with the underlying seed layer 411, stopping on the mechanical layer 430. In step S1306, a dielectric isolation layer 416 may be deposited, patterned and etched to form electrical vias 416a and 416b that expose portions of the upper electrode layer 414 and lower electrode layer 412, respectively.

[0103] Process flow 1300 continues in Figure 13B with the deposition, patterning and etching of a metal interconnect layer 418 in step S1307. The metal interconnect layer 418 may provide electrical traces and electrical contact 418a to portions of upper electrode layer 414 and electrical contact 418b to portions of lower electrode layer 412 through electrical vias 416a and 416b, respectively.

[0104] In step S1308, one or more recesses 422 may be formed in the mechanical layer 430. For example, recesses 422a may be formed external to the PMUT membrane to provide mechanical isolation or to increase sensitivity. Recesses 422b may be formed

internal to the PMUT membrane to increase sensitivity, for example, by allowing the PMUT membrane to flex or vibrate with a larger mechanical amplitude relative to a planar PMUT membrane. The recesses 422 may include substantially axisymmetric features such as a circle or a ring formed partially into a circular PMUT diaphragm near the diaphragm center, or an angular trench or portions of an angular trench formed near the periphery of a circular diaphragm. In some implementations, the recesses 422 may include a square or rectangular feature formed into the mechanical layer 430 near the center of a square or rectangular PMUT diaphragm. In some implementations, the recesses 422 may include features such as narrow rectangles, local trenches, or slots formed near the periphery of or external to a square, rectangular or circular diaphragm. In some implementations, a sequence of radial slots may be combined with central or peripheral recess features. In some implementations, the recess or recessed features may be formed by etching partially or substantially through the mechanical layer 430. In some implementations, the recess 422 and/or features thereof may be formed into the mechanical layer 430 based, for example, on an etch time. In some implementations, the mechanical layer 430 may include two or more deposited layers, one of which may serve as an etch stop or barrier layer to allow precise definition of the recess 422 and recessed features during fabrication. The formation of recesses 422 is optional, and associated process sequences may be omitted accordingly. Dashed lines in step S1308 for recesses 422a and 422b indicate that their positions, when used, may be formed under etched portions of the piezoelectric layer stack 410 such as where first layer 411, lower electrode layer 412, piezoelectric layer 415, upper electrode layer 414, dielectric isolation layer 416 and metal interconnect layer 418 have been removed.

[0105] In step S1309, portions of mechanical layer 430 and other layers may be patterned and etched to provide access (not shown) to sacrificial regions 425i and 425o, which allows the selective removal of exposed sacrificial material in the sacrificial layer 425, resulting in the formation of one or more cavities 420. More details of release holes, release channels, and the sacrificial etching process may be found with respect to Figure 4A-B above (not shown here for clarity). Implementations with thermally decomposable sacrificial materials may not require direct access to cavities 420 through release holes and release channels, as described with respect to Figure 4A-B above.

[0106] In step S1310, a passivation layer 432 may be deposited over the interconnect layer 418 and exposed portions of the lower electrode layer 412 and upper electrode

layer 414. Optionally, one or more upper recesses 432a may be formed in the passivation layer 432. For example, recesses 432a may be formed external to the PMUT membrane to provide mechanical isolation or to increase sensitivity. Recesses 432a may be formed internal to the PMUT membrane to increase sensitivity, for example, by allowing the PMUT membrane to flex or vibrate with a larger mechanical amplitude relative to a planar PMUT membrane. The recesses 432a may include substantially axisymmetric features such as a circle or a ring formed partially into a circular PMUT diaphragm near the diaphragm center, or an angular trench or portions of an angular trench formed near the periphery of a circular diaphragm. In some implementations, the recesses 432a may include a square or rectangular feature formed into the passivation layer 432 near the center of a square or rectangular PMUT diaphragm. In some implementations, the recesses 432a may include features such as narrow rectangles, local trenches, or slots formed near the periphery of or external to a square, rectangular or circular diaphragm. In some implementations, a sequence of radial slots may be combined with central or peripheral recess features. In some implementations, the recess or recessed features may be formed by etching partially or substantially through the passivation layer 432. In some implementations, the recess 432a and/or features thereof may be formed into the passivation layer 432 based on, for example, an etch time. In some implementations, the passivation layer 432 may include two or more deposited layers, one of which may serve as an etch stop or barrier layer to allow precise definition of the recess 432a and other recessed features during fabrication. The formation of recesses 432a is optional, and associated process sequences may be omitted accordingly. In step S1311, one or more contact pad openings or vias 434a and 434b may be patterned and etched through the passivation layer 432 to provide access to underlying metal features such as bond pads.

[0107] Figures 14A and 14B illustrate another example of a process flow for fabricating a PMUT. Process flow 1400 provides three layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate, utilizing a silicide-based planarization method as described above with respect to steps S1202-S1204 of Figure 12. In step S1401, a substrate 360 is provided upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer or barrier layer, may be deposited on the substrate 360. A sacrificial layer 425 of amorphous or polycrystalline silicon may be deposited on the

buffer layer, followed by the deposition of a metal layer such as a nickel layer 1275. The nickel layer 425 may be patterned and etched to expose one or more inner sacrificial regions 425i and outer sacrificial regions 425o (not shown), with the etchant stopping on the sacrificial layer 425. In step S1402, the nickel layer 1275 and underlying sacrificial layer 425 may be reacted in a high-temperature environment to locally form a silicide layer 1276 such as nickel silicide. Portions of the silicide layer 1276 may form an anchor portion 474 of the anchor structure 470. In step S1403, a multilayer stack may be deposited, including a thin barrier layer 476, a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, a piezoelectric layer 415, and an upper electrode layer 414. The upper electrode layer 414 may be patterned and etched to form upper electrodes 414a and 414b that are in electrical contact with the piezoelectric layer 415. In step S1404, the piezoelectric layer 415 may be patterned and etched, stopping on the lower electrode layer 412. In step S1405, the lower electrode layer 412 may be patterned and etched along with the underlying seed layer 411, stopping on the mechanical layer 430. In step S1406, a dielectric isolation layer 416 may be deposited, patterned and etched to form electrical vias 416a and 416b that expose portions of the upper electrode layer 414 and lower electrode layer 412, respectively.

[0108] Process flow 1400 continues in Figure 14B with the deposition, patterning and etching of a metal interconnect layer 418 in step S1407. The metal interconnect layer 418 may provide electrical traces and electrical contact 418a to portions of upper electrode layer 414 and electrical contact 418b to portions of lower electrode layer 412 through electrical vias 416a and 416b, respectively. In step S1408, one or more recesses 422 may be optionally formed in mechanical layer 430. Dashed lines in Figure 14B for recesses 422a and 422b indicate that their positions, when used, may be formed in regions not directly under non-etched portions of the piezoelectric layer stack 410. In step S1409, portions of the mechanical layer 430 and other layers may be patterned and etched (not shown) to provide access to sacrificial regions 425i and 425o. Selective removal of exposed sacrificial material in the sacrificial layer 425 results in the formation of one or more cavities 420. More details of release holes, release channels, and the sacrificial etching process may be found with respect to Figure 4A-B above. Implementations with thermally decomposable sacrificial materials may not require direct access to cavities 420 through release holes and release channels, as described

with respect to Figure 4A-B. In step S1410, a passivation layer 432 may be deposited over the interconnect layer 418 and exposed portions of the lower electrode layer 412 and upper electrode layer 414. Optionally, one or more upper recesses 432a may be formed in the passivation layer 432. In step S1411, one or more contact pad openings or vias 434a and 434b may be patterned and etched through the passivation layer 432 to provide access to underlying metal features such as bond pads in metal interconnect layer 418.

[0109] Figures 15A and 15B illustrate another example of a process flow for fabricating a PMUT. Process flow 1500 utilizes two layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate. In a first step S1501, a substrate 360 is provided upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer layer, may be deposited on the substrate 360. A sacrificial layer 425 of a sacrificial material may be deposited on the buffer layer. The sacrificial layer 425 may be patterned and etched to form one or more inner sacrificial regions 425i and outer sacrificial regions 425o (not shown), with the etchant stopping on the underlying buffer layer or substrate. In step S1502a, an anchor portion 474 of the anchor structure 470 may be deposited onto the buffer layer and the sacrificial regions, then thinned using CMP to form a substantially planar surface while retaining a small portion 474i above the sacrificial region as shown in step S1502b. In step S1504, a multilayer stack may be deposited, including a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, and a piezoelectric layer 415. The piezoelectric layer 415 may be patterned and etched, stopping on the lower electrode layer 412. In step S1505, the lower electrode layer 412 and the underlying seed layer 411 may be patterned and etched, stopping on the mechanical layer 430. In step S1506, a dielectric isolation layer 416 may be deposited, patterned and etched to form electrical vias 416a and 416b that expose portions of the piezoelectric layer 415 and lower electrode layer 412, respectively. Alternatively, electrical coupling between the upper electrode layer 414 and underlying portions of the piezoelectric layer 415 may be achieved capacitively through the dielectric isolation layer 416, allowing excitation and detection of ultrasonic waves from flexural motions and vibrations of piezoelectric layer 415 without direct electrical contact, as described with respect to step S1507

below. In this implementation, one or more electrical vias 416a may be omitted and the dielectric isolation layer 416 would not be etched in the via region (not shown).

[0110] Process flow 1500 continues in Figure 15B with the deposition, patterning and etching of a metal interconnect layer 418 in step S1507. The metal interconnect layer 418 may provide electrical traces and electrical contacts 418a to portions of piezoelectric layer 415 and electrical contact 418b to portions of lower electrode layer 412 through electrical vias 416a and 416b, respectively. In the capacitive coupling implementation described with respect to step S1506, the metal interconnect layer 418 may be dielectrically isolated from the piezoelectric layer 415 and one or more electrical vias 416a omitted. In step S1508, one or more recesses 422 may be formed in the mechanical layer 430. Dashed lines in step S1508 for recesses 422a and 422b indicate that their positions, when used, may be formed under etched portions of the piezoelectric layer stack 410. In step S1509, portions of mechanical layer 430 and other layers may be patterned and etched to provide access (not shown) to sacrificial regions 425i, which allows the selective removal of exposed sacrificial material in the sacrificial layer 425, resulting in the formation of one or more cavities 420. In some implementations with thermally decomposable sacrificial materials, direct access to cavities 420 through release holes and release channels may not be required, as described with respect to Figure 4A-B above. In step S1510, the passivation layer 432 may be deposited over the interconnect layer 418 and exposed portions of the lower electrode layer 412 and upper electrode layer 414. Optionally, one or more upper recesses 432a may be formed in the passivation layer 432. In step S1511, one or more contact pad openings or vias 434a and 434b may be patterned and etched through the passivation layer 432 to provide access to underlying metal features such as bond pads in metal interconnect layer 418.

[0111] Figures 16A and 16B illustrate another example of a process flow for fabricating a PMUT. Process flow 1600 utilizes two layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate, utilizing a silicide-based planarization method as described above with respect to steps S1202-S1204 of Figure 12. In step S1601, a substrate 360 is provided upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer or barrier layer, may be deposited on the substrate 360. A sacrificial layer 425 of amorphous or polycrystalline silicon may be deposited on the buffer layer,

followed by the deposition of a metal layer such as a nickel layer 1275. The nickel layer 425 may be patterned and etched to expose one or more inner sacrificial regions 425i and outer sacrificial regions 425o (not shown), with the etchant stopping on the sacrificial layer 425. In step S1602a, the nickel layer 1275 and underlying sacrificial layer 425 may be reacted in a high-temperature environment to locally form a silicide layer 1276 such as nickel silicide. Portions of the silicide layer 1276 may form an anchor portion 474 of the anchor structure 470. In step S1602b, a thin barrier layer 476 may be deposited. A portion 476i of the thin barrier layer 476 may reside over the sacrificial regions 425i and 425o. In step S1604, a multilayer stack may be deposited, including a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, and a piezoelectric layer 415. The piezoelectric layer 415 may be patterned and etched, stopping on the lower electrode layer 412. In step S1605, the lower electrode layer 412 and the underlying seed layer 411 may be patterned and etched, stopping on the mechanical layer 430. In step S1606, a dielectric isolation layer 416 may be deposited, patterned and etched to form electrical vias 416a and 416b that expose portions of the piezoelectric layer 415 and lower electrode layer 412, respectively. Alternatively, electrical coupling between the upper electrode layer 414 and underlying portions of the piezoelectric layer 415 may be achieved capacitively through the dielectric isolation layer 416, allowing excitation and detection of ultrasonic waves from flexural motions and vibrations of piezoelectric layer 415 without direct electrical contact, as described with respect to step S1607 below. In this implementation, one or more electrical vias 416a may be omitted and the dielectric isolation layer 416 would not be etched in the via region (not shown).

[0112] Process flow 1600 continues in Figure 16B with the deposition, patterning and etching of a metal interconnect layer 418 in step S1607. The metal interconnect layer 418 may provide electrical traces and electrical contact 418a to portions of piezoelectric layer 415 and electrical contact 418b to portions of lower electrode layer 412 through electrical vias 416a and 416b, respectively. In the capacitive coupling implementation described with respect to step S1606, the metal interconnect layer 418 may be dielectrically isolated from the piezoelectric layer 415 and one or more electrical vias 416a omitted. In step S1608, one or more recesses 422 may be formed in the mechanical layer 430. Dashed lines in step S1608 for recesses 422a and 422b indicate that their positions, when used, may be formed under etched portions of the

piezoelectric layer stack 410. In step S1609, portions of mechanical layer 430 and other layers may be patterned and etched to provide access (not shown) to sacrificial regions 425i, which allows the selective removal of exposed sacrificial material in the sacrificial layer 425, resulting in the formation of one or more cavities 420. In some implementations with thermally decomposable sacrificial materials, direct access to cavities 420 through release holes and release channels may not be required, as described with respect to Figure 4A-B above. In step S1610, a passivation layer 432 may be deposited over the interconnect layer 418 and exposed portions of the lower electrode layer 412 and upper electrode layer 414. Optionally, one or more upper recesses 432a may be formed in the passivation layer 432. In step S1611, one or more contact pad openings or vias 434a and 434b may be patterned and etched through the passivation layer 432 to provide access to underlying metal features such as bond pads in metal interconnect layer 418.

[0113] Figures 17A and 17B illustrate another example of a process flow for fabricating a PMUT. Process flow 1700 provides three layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate, providing for an unsealed PMUT that may be subsequently sealed with a laminated or bonded upper mechanical layer (not shown here, but described above with respect to Figures 6A-6E). In a first step S1701, a substrate 360 is provided upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer layer, may be deposited on the substrate 360. A sacrificial layer 425 of a sacrificial material may be deposited on the buffer layer. The sacrificial layer 425 may be patterned and etched to form one or more inner sacrificial regions 425i, with the etchant stopping on the underlying buffer layer or substrate. In step S1702, an anchor portion 474 of the anchor structure 470 such as a silicon dioxide layer may be deposited onto the buffer layer and the sacrificial regions, then thinned using CMP to form a substantially planar surface while retaining a small portion 474i of the silicon dioxide layer above the sacrificial region 425i. In step S1703, a multilayer stack may be deposited, including a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, a piezoelectric layer 415, and an upper electrode layer 414. The upper electrode layer may be patterned and etched to form an upper electrode 414a that is in electrical contact with the piezoelectric layer 415. In step S1704, the piezoelectric layer 415 may be patterned and etched,

stopping on the lower electrode layer 412. In step S1705, the lower electrode layer 412 may be patterned and etched along with the underlying seed layer 411, stopping on the mechanical layer 430. In step S1706, a dielectric isolation layer 416 may be deposited, patterned and etched to form electrical vias 416a and 416b that expose portions of the upper electrode layer 414 and lower electrode layer 412, respectively.

[0114] Process flow 1700 continues in Figure 17B with the deposition, patterning and etching of a metal interconnect layer 418 in step S1707. The metal interconnect layer 418 may provide electrical traces and electrical contact 418a to portions of upper electrode layer 414 and electrical contact 418b to portions of lower electrode layer 412 through electrical vias 416a and 416b, respectively. In step S1708, one or more recesses 422 may be formed in mechanical layer 430. Dashed lines in step S1708 for recesses 422a and 422b indicate that their positions, when used, may be formed under etched portions of the piezoelectric layer stack 410. In step S1709, a passivation layer 432 may be deposited over the interconnect layer 418 and exposed portions of the lower electrode layer 412 and upper electrode layer 414. Optionally, one or more upper recesses 432a may be formed in the passivation layer 432. In step S1710, portions of mechanical layer 430 and other layers such as dielectric isolation layer 416 may be patterned and etched to provide access to sacrificial region 425i, which allows the selective removal of exposed sacrificial material in the sacrificial layer 425, resulting in the formation of one or more cavities 420. Also in step S1710, one or more contact pad openings or vias 434a and 434b may be patterned and etched through the passivation layer 432 to provide access to underlying metal features such as bond pads. In step S1711, exposed portions of sacrificial layer 425 in sacrificial region 425i may be selectively etched, stopping on exposed surfaces of the anchor portion 474, first layer portion 472 and substrate 360 and resulting in the formation of one or more cavities 420. In some implementations, an upper mechanical layer 630 (not shown) may be laminated or otherwise bonded to the upper surface of the PMUT, such as described with respect to Figure 6B. In some implementations, an upper mechanical layer 630 may be coupled to an array of micropillars 636 (not shown), such as described with respect to Figure 6D.

[0115] Figure 18 illustrates another example of a process flow for fabricating a PMUT. Process flow 1800 provides two layers of metal interconnections for a PMUT with a mechanical layer positioned substantially between the piezoelectric layer stack and the underlying substrate, providing for an unsealed PMUT that may be subsequently sealed

with a laminated or bonded upper mechanical layer (not shown here, but described above with respect to Figures 6A-6E). In a first step S1801, a substrate 360 is provided upon which to fabricate the PMUTs. A first layer portion 472, such as an oxide buffer layer, may be deposited on the substrate 360. A sacrificial layer 425 of a sacrificial material may be deposited on the buffer layer. The sacrificial layer 425 may be patterned and etched to form one or more inner sacrificial regions 425i, with the etchant stopping on the underlying buffer layer or substrate. Also in step S1801, an anchor portion 474 of the anchor structure 470 such as a silicon dioxide layer may be deposited onto the buffer layer and the sacrificial regions, then thinned using CMP to form a substantially planar surface while retaining a small portion 474i of the silicon dioxide layer above the sacrificial region 425i. In step S1802, a multilayer stack may be deposited, including a mechanical layer 430, a first layer 411 of the piezoelectric stack 410 that may serve as a seed layer, a lower electrode layer 412, a piezoelectric layer 415, and an upper electrode layer 414. The upper electrode layer 414 may be patterned and etched to form upper electrodes 414a that are in electrical contact with the piezoelectric layer 415. Also in step S1802, the piezoelectric layer 415 may be etched, stopping on the lower electrode layer 412. In step S1803, the lower electrode layer 412 may be patterned and etched along with the underlying seed layer 411, stopping on the mechanical layer 430 to expose portions 435a and 435b of the upper electrode layer 414 and lower electrode layer 412, respectively, to allow for subsequent wire bonding or the inclusion of an additional interconnect layer (not shown). In step S1804, portions of mechanical layer 430 and any underlying layers may be patterned and etched to form one or more release holes 430a and provide access to sacrificial region 425i. In step S1805, exposed portions of sacrificial layer 425 in sacrificial region 425i may be selectively etched, resulting in the formation of one or more cavities 420. In some implementations, an upper mechanical layer 630 (not shown) may be laminated or otherwise bonded to the upper surface of the PMUT, as described with respect to Figure 6B. In some implementations, an upper mechanical layer 630 may be coupled to an array of micropillars 636 (not shown), as described with respect to Figure 6D.

[0116] Thus, a PMUT having a mechanical layer disposed above or below a piezoelectric layer stack, providing a seal for an underlying cavity, and techniques for fabrication such a PMUT have been disclosed. It will be appreciated that a number of alternative configurations and fabrication techniques may be contemplated.

[0117] As used herein, a phrase referring to "at least one of" a list of items refers to any combination of those items, including single members. As an example, "at least one of: a, b, or c" is intended to cover: a, b, c, a-b, a-c, b-c, and a-b-c.

[0118] The various illustrative logics, logical blocks, modules, circuits and algorithm processes described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and processes described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0119] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor or any conventional processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular processes and methods may be performed by circuitry that is specific to a given function.

[0120] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by or to control the operation of data processing apparatus.

[0121] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium, such as a non-

transitory medium. The processes of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media include both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, non-transitory media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

[0122] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. Additionally, as a person having ordinary skill in the art will readily appreciate, the terms "upper" and "lower", "top" and bottom", "front" and "back", and "over", "overlying", "on", "under" and "underlying" are sometimes used for ease of describing the figures and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the device as implemented.

[0123] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in

certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0124] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. A piezoelectric micromechanical ultrasonic transducer (PMUT) comprising:

a multilayer stack disposed on a substrate and including:

an anchor structure disposed over the substrate;

a piezoelectric layer stack disposed over the anchor structure; and

a mechanical layer disposed proximate to the piezoelectric layer stack; wherein:

the piezoelectric layer stack is disposed over a cavity; and

the mechanical layer seals the cavity and, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

2. The PMUT of claim 1, wherein the mechanical layer has a thickness such that a neutral axis of the multilayer stack is displaced, relative to a neutral axis of the piezoelectric layer stack, towards the mechanical layer to allow an out-of-plane bending mode.

3. The PMUT of claim 2, wherein the mechanical layer is substantially thicker than the piezoelectric layer stack.

4. The PMUT of claim 2, wherein the neutral axis passes through the mechanical layer.

5. The PMUT of claim 1, wherein:

the cavity is formed by removing a sacrificial material through at least one release hole;

the mechanical layer is formed after removing the sacrificial material; and

forming the mechanical layer seals the cavity by sealing the at least one release hole.

6. The PMUT of claim 1, wherein the piezoelectric layer stack includes a piezoelectric layer, a lower electrode disposed below the piezoelectric layer, and an upper electrode disposed above the piezoelectric layer.

7. The PMUT of claim 1, wherein the mechanical layer includes a recess where the mechanical layer is locally thinned.

8. The PMUT of claim 1, wherein the mechanical layer is disposed over a side of the piezoelectric stack opposite to the substrate.

9. The PMUT of claim 1, wherein the mechanical layer is disposed below a side of the piezoelectric stack facing the substrate.

10. The PMUT of claim 1, further comprising an acoustic coupling medium disposed above the piezoelectric layer stack, wherein the PMUT is configured to receive or transmit ultrasonic signals through the coupling medium.

11. A piezoelectric micromechanical ultrasonic transducer (PMUT) comprising:

a multilayer stack disposed on a substrate and including:

an anchor structure disposed over the substrate;

a piezoelectric layer stack disposed over the anchor structure; and

a mechanical layer disposed proximate to the piezoelectric layer stack, the mechanical layer including a recess where the mechanical layer is locally thinned; wherein

the piezoelectric layer stack is disposed over a cavity; and

the mechanical layer, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

12. The PMUT of claim 11, wherein:

the cavity is formed by removing a sacrificial material through at least one release hole;

the mechanical layer is formed after removing the sacrificial material; and

forming the mechanical layer seals the cavity by sealing the at least one release hole.

13. The PMUT of claim 11, wherein the mechanical layer is disposed over a side of the piezoelectric stack opposite to the substrate.

14. The PMUT of claim 11, wherein the mechanical layer is disposed below a side of the piezoelectric stack facing the substrate.

15. The PMUT of claim 11, further comprising an acoustic coupling medium disposed above the piezoelectric layer stack, wherein the PMUT is configured to receive or transmit ultrasonic signals through the coupling medium.

16. A method of making a piezoelectric micromechanical ultrasonic transducer (PMUT) comprising:

forming an anchor structure over a substrate, the anchor structure disposed proximate to regions of sacrificial material;

forming a piezoelectric layer stack over the anchor structure;

removing the sacrificial material so as to form a cavity under the piezoelectric layer stack; and

disposing a mechanical layer proximate to the piezoelectric layer stack, wherein the piezoelectric layer stack and the mechanical layer form part of a multilayer stack, the mechanical layer seals the cavity and, together with the piezoelectric layer stack, is supported by the anchor structure and forms a membrane over the cavity, the membrane being configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

17. The method of claim 16, wherein removing the sacrificial material includes removing the sacrificial material through at least one release hole and the mechanical layer seals the at least one release hole.

18. The method of claim 16, wherein the anchor structure is disposed in a lower layer, the lower layer being parallel to the piezoelectric layer stack and including the regions of sacrificial material.

19. The PMUT of claim 16, wherein the mechanical layer has a thickness such that a neutral axis of the multilayer stack is displaced, relative to a neutral axis of the piezoelectric layer stack, towards the mechanical layer to allow an out-of-plane bending mode.

20. The PMUT of claim 19, wherein the mechanical layer is substantially thicker than the piezoelectric layer stack.

21. The PMUT of claim 19, wherein the neutral axis passes through the mechanical layer.

22. An apparatus comprising:

an array of piezoelectric micromechanical ultrasonic transducer (PMUT) sensors; and

an acoustic coupling medium, wherein:

at least one PMUT includes a multilayer stack disposed on a substrate and including an anchor structure disposed over the substrate, a piezoelectric layer stack disposed over the anchor structure and a cavity, and a mechanical layer disposed proximate to the piezoelectric layer stack, the mechanical layer sealing the cavity;

the acoustic coupling medium is disposed above the piezoelectric layer stack; and

the PMUT is configured to receive or transmit ultrasonic signals through the coupling medium.

23. The apparatus of claim 22, wherein the mechanical layer, together with the piezoelectric layer stack, forms a membrane over the cavity, the membrane being

configured to undergo one or both of flexural motion and vibration when the PMUT receives or transmits ultrasonic signals.

24. The apparatus of claim 22, wherein the mechanical layer has a thickness such that a neutral axis of the multilayer stack is displaced, relative to a neutral axis of the piezoelectric layer stack, towards the mechanical layer to allow an out-of-plane bending mode.

25. The apparatus of claim 24, wherein the mechanical layer is substantially thicker than the piezoelectric layer stack.

26. The apparatus of claim 24, wherein the neutral axis passes through the mechanical layer.

27. The apparatus of claim 22, wherein:

the cavity is formed by removing a sacrificial material through at least one release hole;

the mechanical layer is formed after removing the sacrificial material; and

the mechanical layer seals the cavity by sealing the at least one release hole.

28. The apparatus of claim 22, wherein the mechanical layer includes a recess where the mechanical layer is locally thinned.

29. The apparatus of claim 22, wherein the mechanical layer is disposed over a side of the piezoelectric stack opposite to the substrate or below a side of the piezoelectric stack facing the substrate.

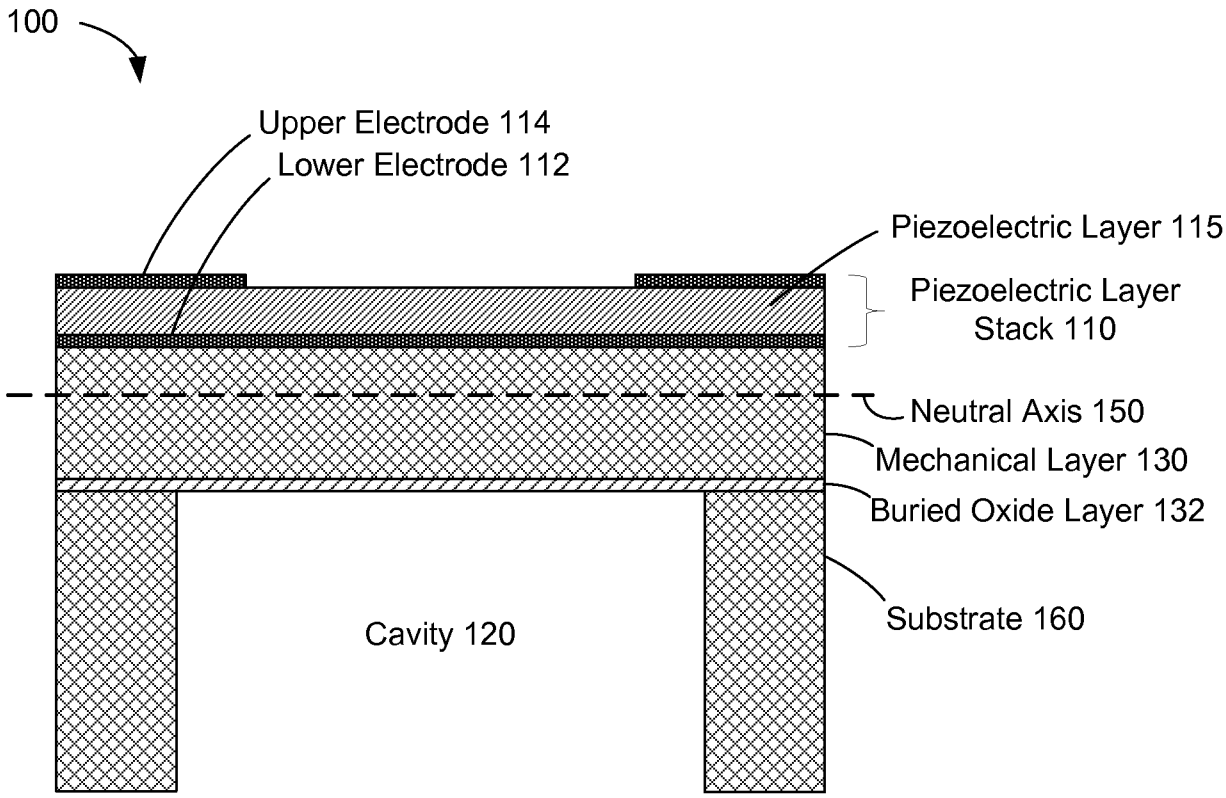

100
Upper Electrode 114
Lower Electrode 112
Piezoelectric Layer 115
Piezoelectric Layer Stack 110
Neutral Axis 150
Mechanical Layer 130
Buried Oxide Layer 132
Substrate 160
Cavity 120

Figure 1

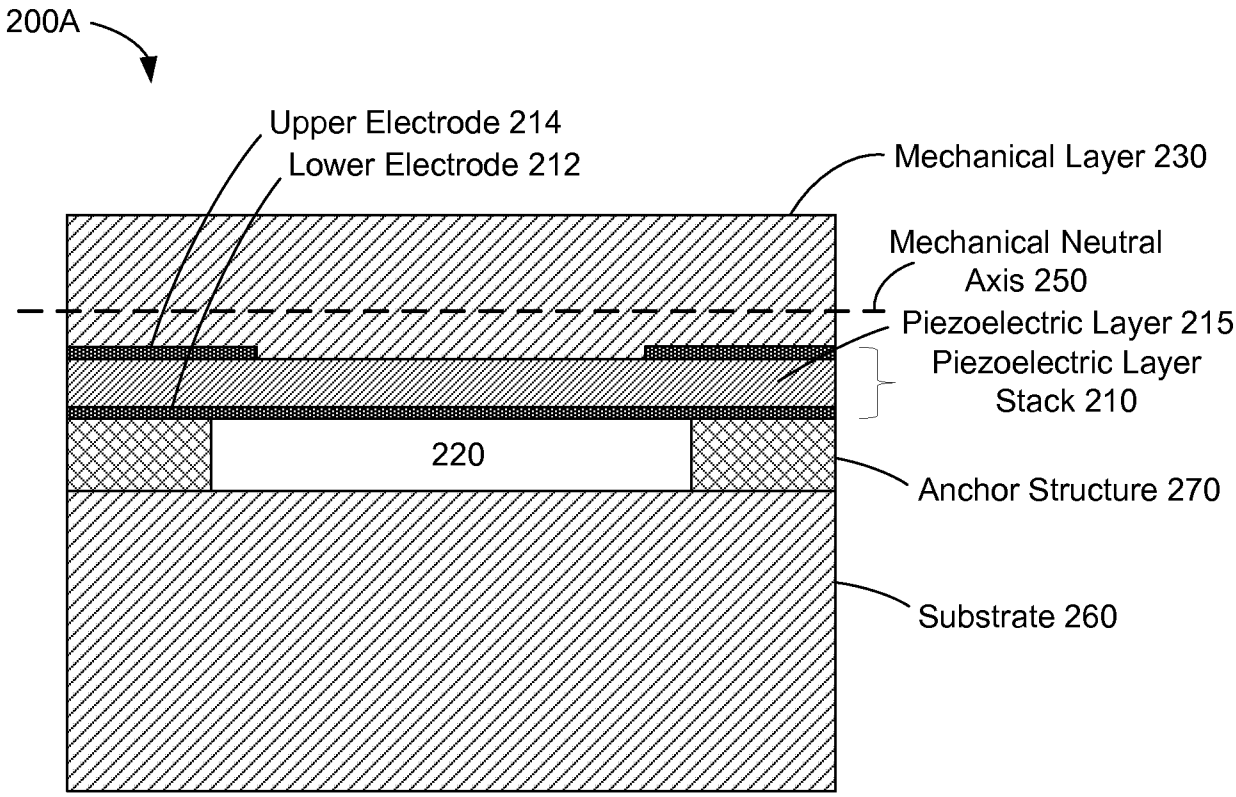

200A
Upper Electrode 214
Lower Electrode 212
Mechanical Layer 230
Mechanical Neutral Axis 250
Piezoelectric Layer 215
Piezoelectric Layer Stack 210
220
Anchor Structure 270
Substrate 260

Figure 2A

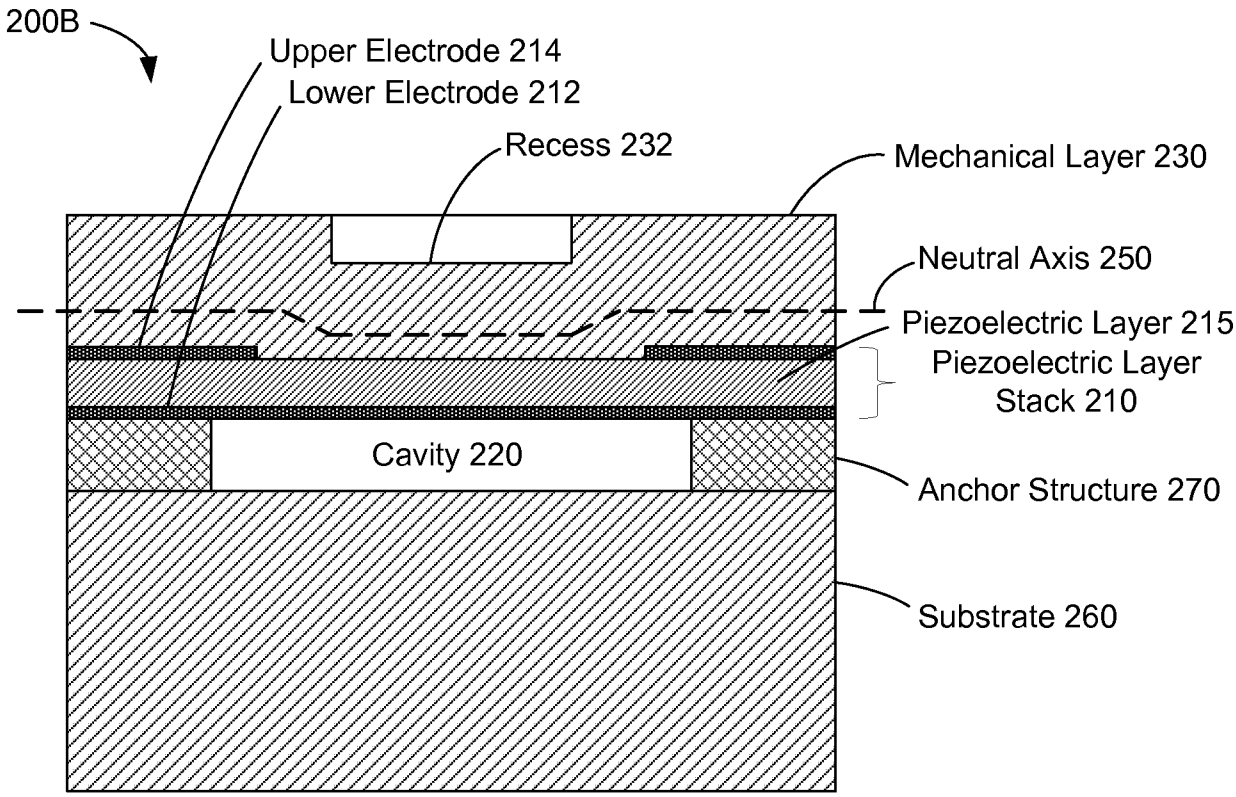

200B
Upper Electrode 214
Lower Electrode 212
Recess 232
Mechanical Layer 230
Neutral Axis 250
Piezoelectric Layer 215
Piezoelectric Layer Stack 210
Cavity 220
Anchor Structure 270
Substrate 260

Figure 2B

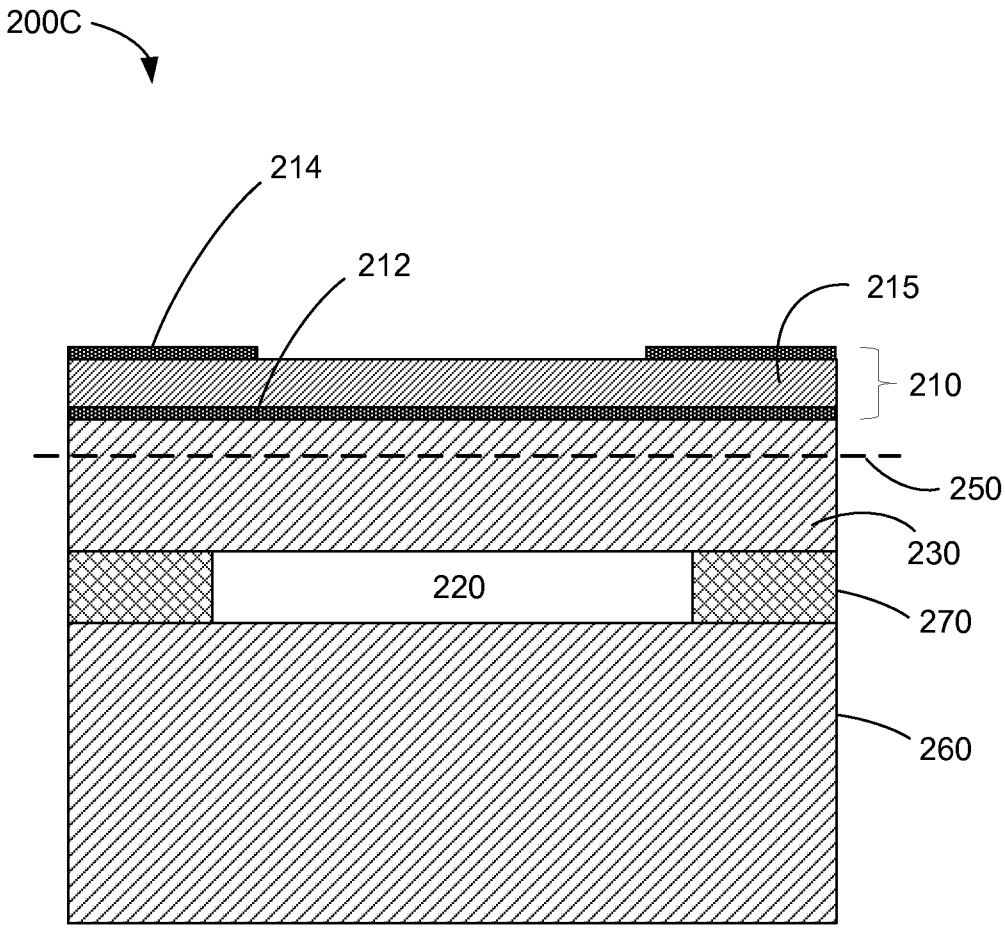


Figure 2C

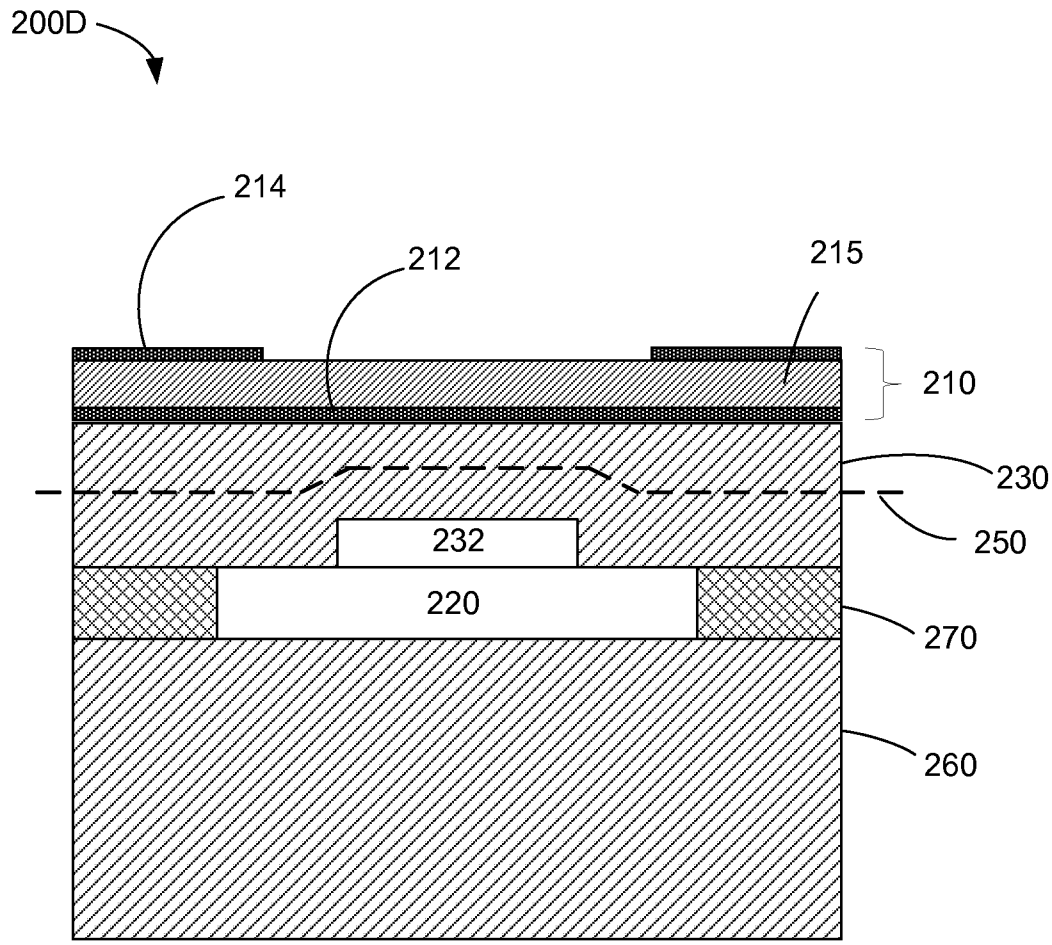


Figure 2D

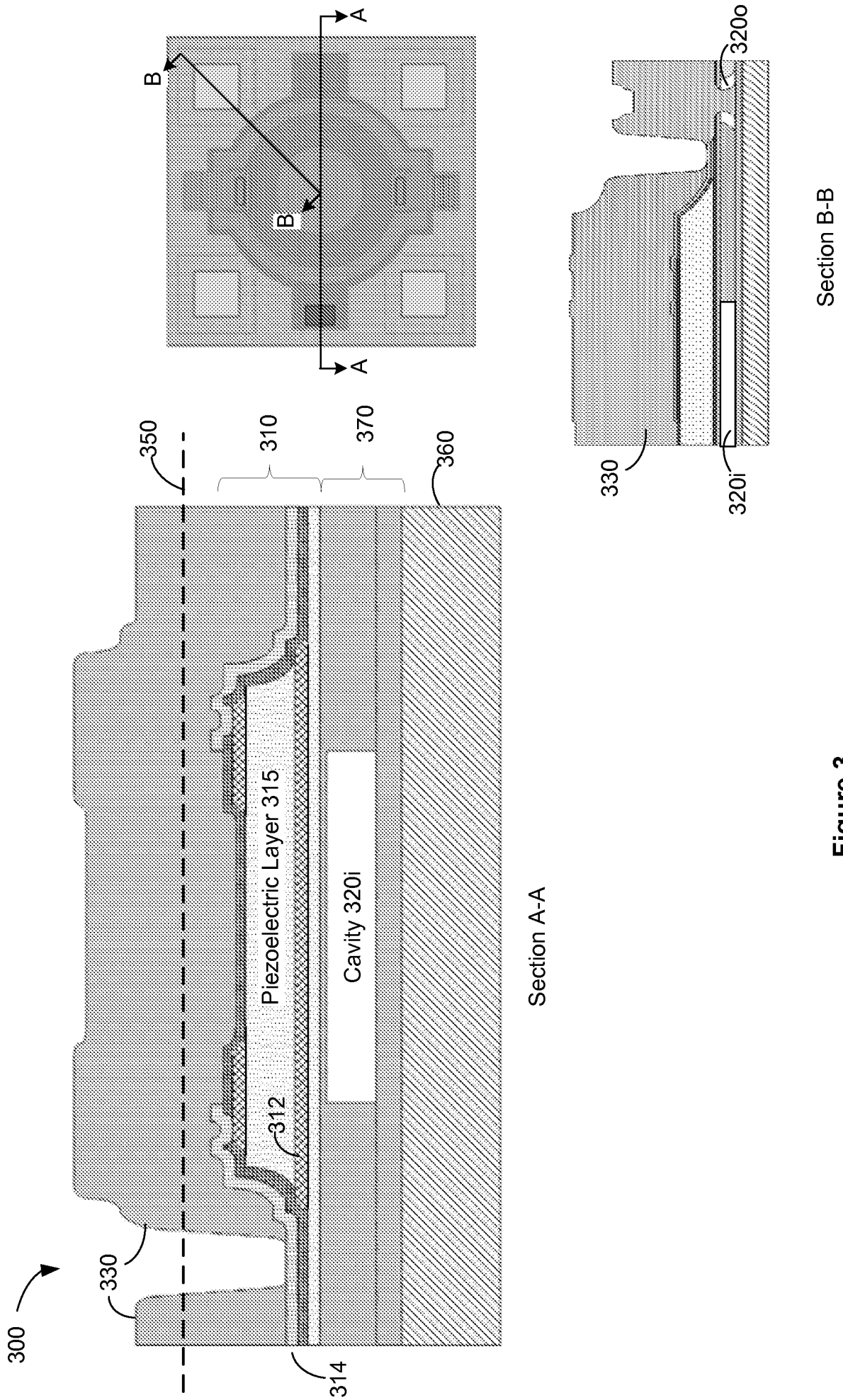

A
B
B
A
320o
320i
330
Section B-B
350
310
370
360
Piezoelectric Layer 315
Cavity 320i
312
330
300
314
Section A-A

Figure 3

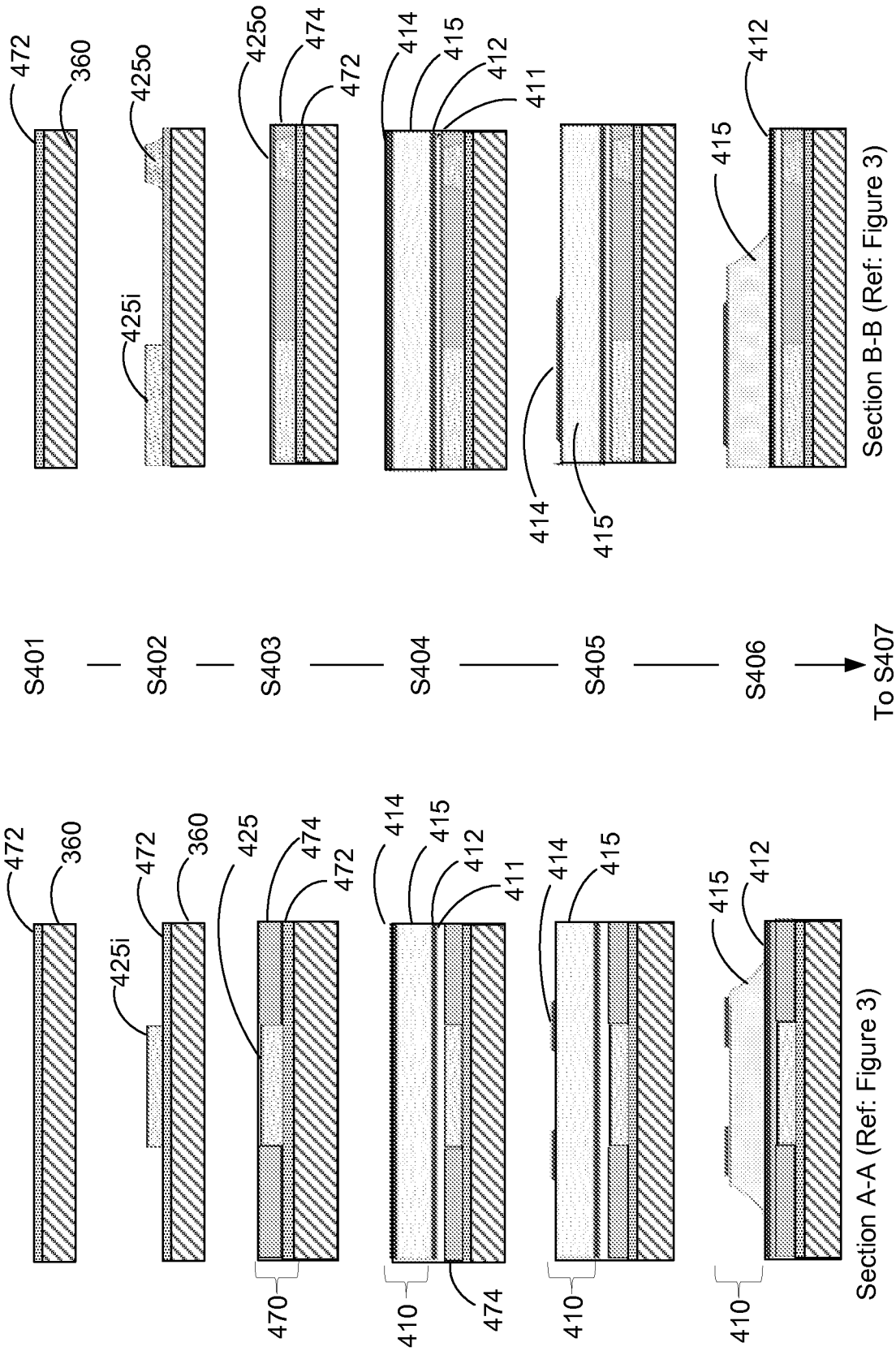

S401
S402
S403
S404
S405
S406
To S407
Section B-B (Ref: Figure 3)
Section A-A (Ref: Figure 3)
472
360
425i
425o
474
414
415
412
411
425
410
470

Figure 4A

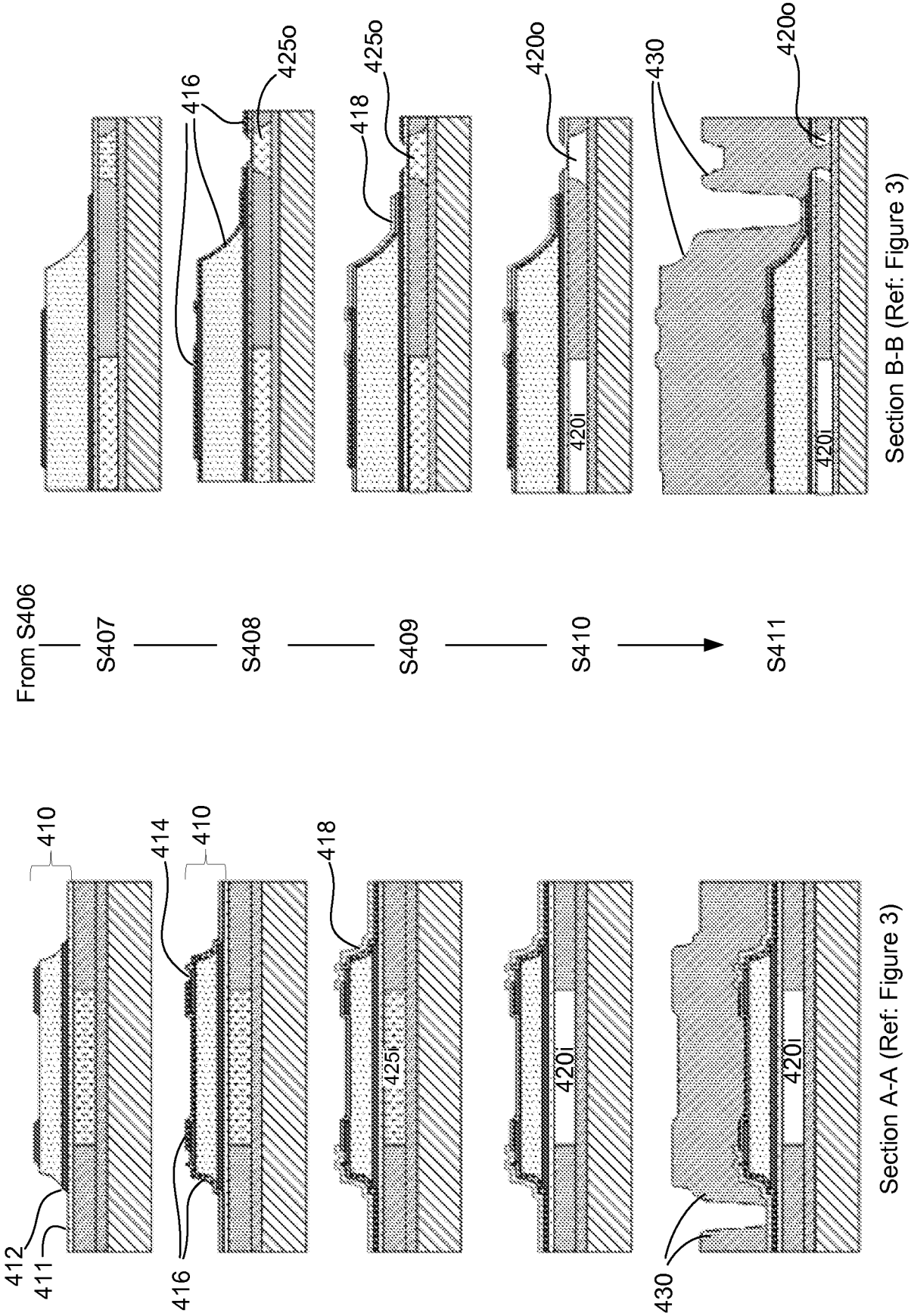

From S406
S407
S408
S409
S410
S411
Section A-A (Ref: Figure 3)
Section B-B (Ref: Figure 3)
410
414
410
418
412
411
416
425i
420i
430
416
425o
418
425o
420o
420i
430
420o
420i

Figure 4B

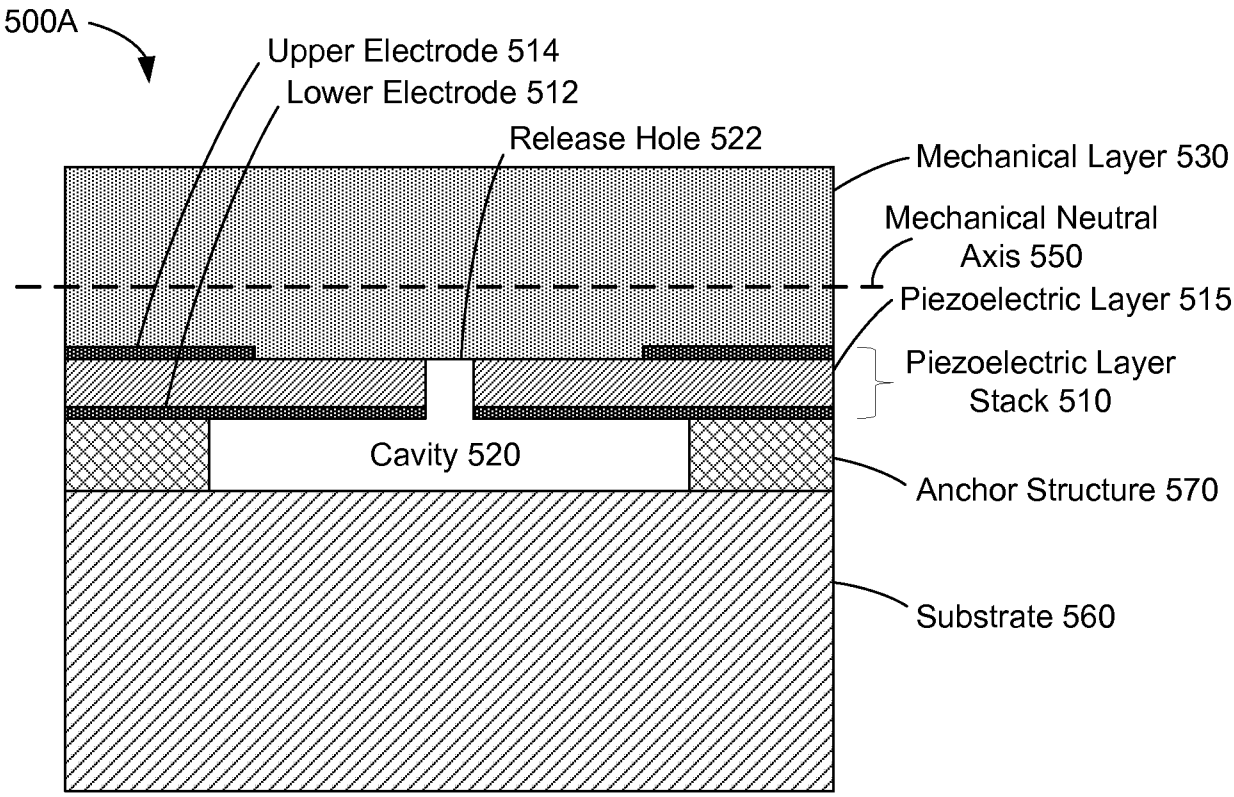

500A
Upper Electrode 514
Lower Electrode 512
Release Hole 522
Mechanical Layer 530
Mechanical Neutral Axis 550
Piezoelectric Layer 515
Piezoelectric Layer Stack 510
Cavity 520
Anchor Structure 570
Substrate 560

Figure 5A

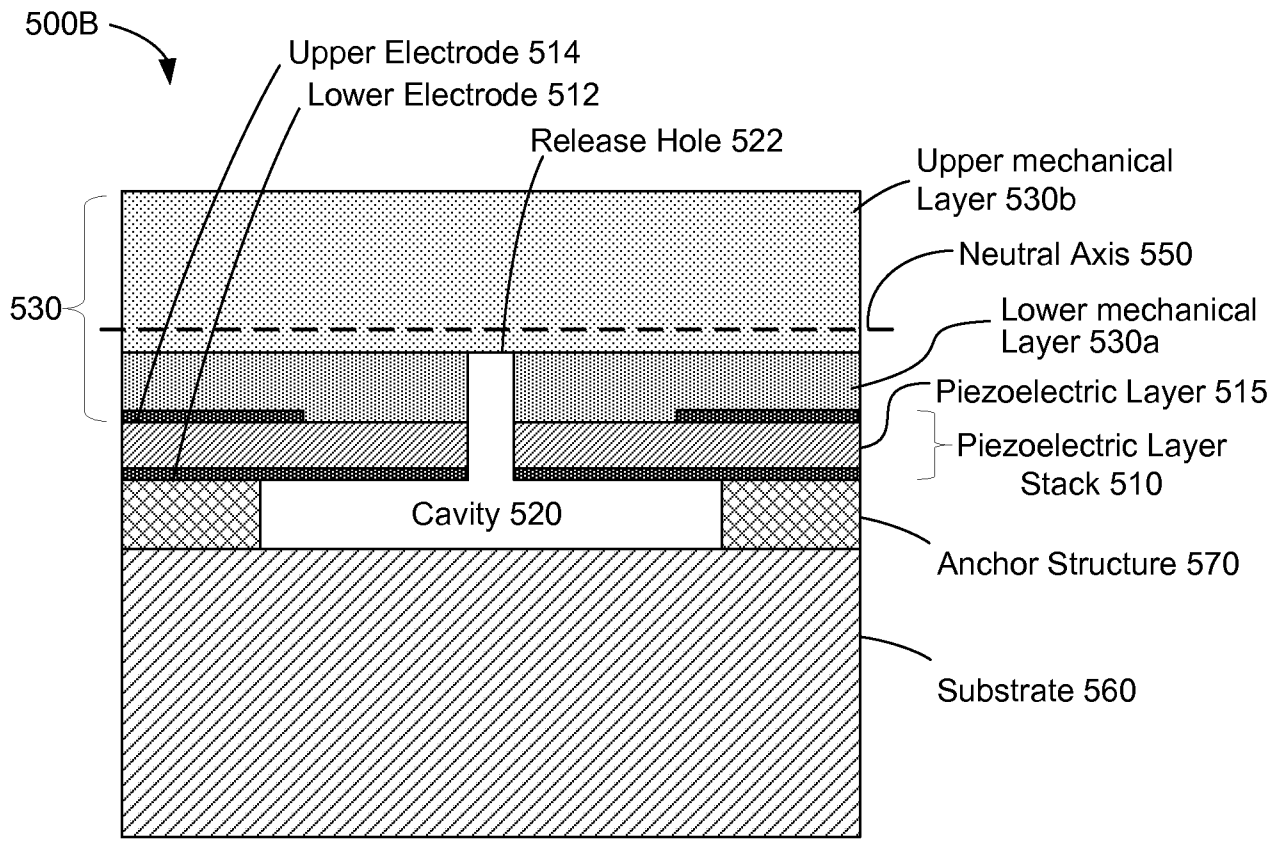

500B
Upper Electrode 514
Lower Electrode 512
Release Hole 522
Upper mechanical Layer 530b
Neutral Axis 550
530
Lower mechanical Layer 530a
Piezoelectric Layer 515
Piezoelectric Layer Stack 510
Cavity 520
Anchor Structure 570
Substrate 560

Figure 5B

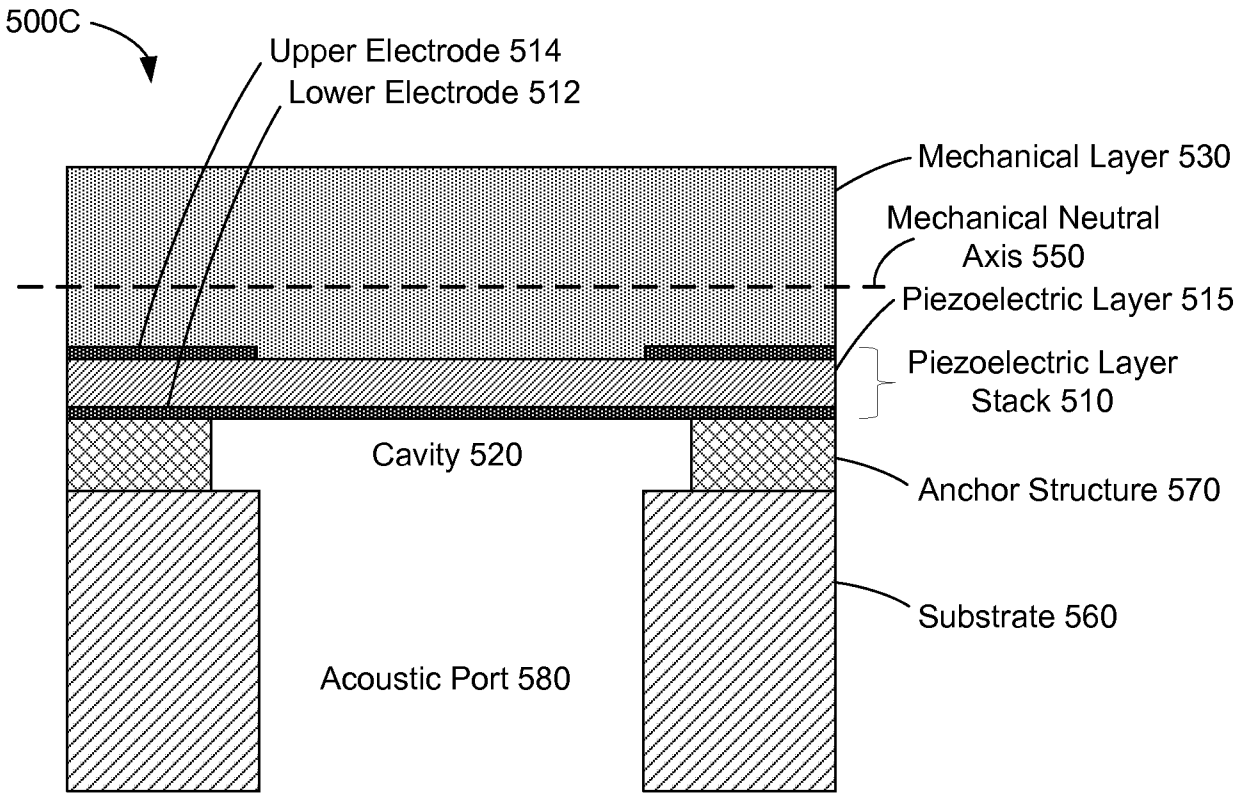

500C
Upper Electrode 514
Lower Electrode 512
Mechanical Layer 530
Mechanical Neutral Axis 550
Piezoelectric Layer 515
Piezoelectric Layer Stack 510
Cavity 520
Anchor Structure 570
Substrate 560
Acoustic Port 580

Figure 5C

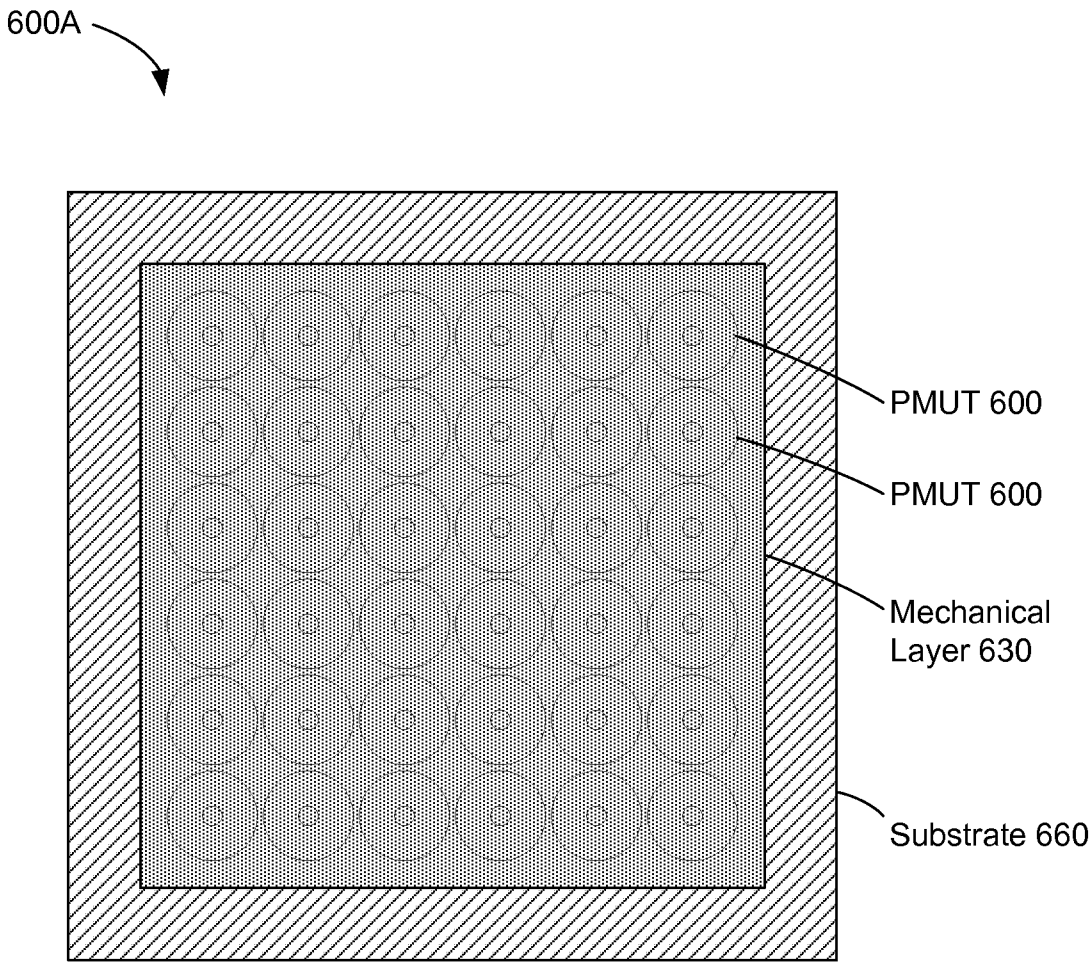


Figure 6A

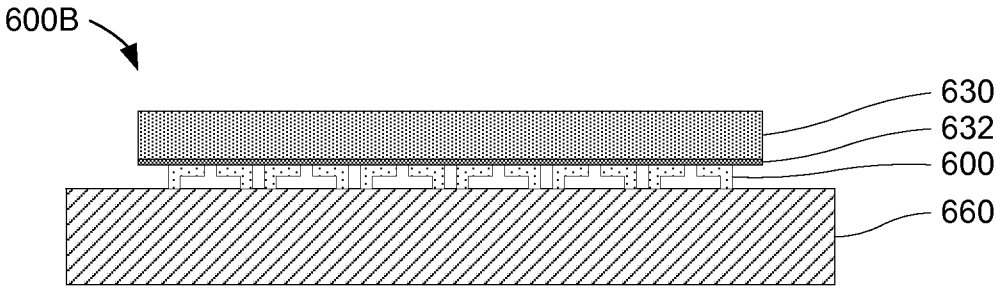


Figure 6B

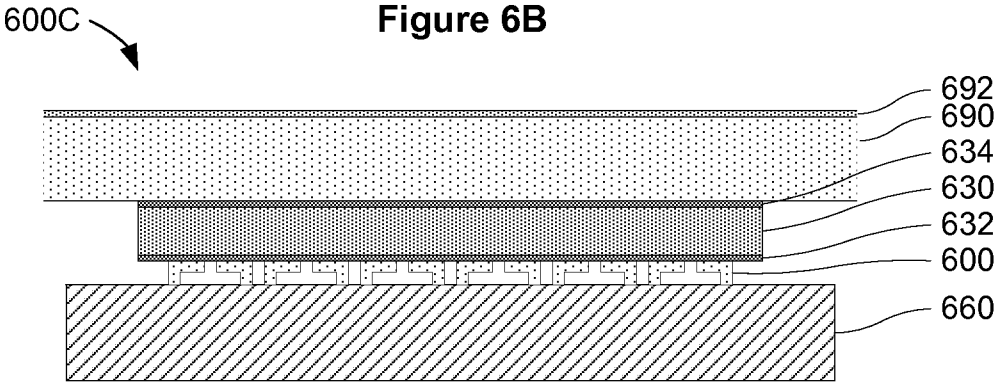


Figure 6C

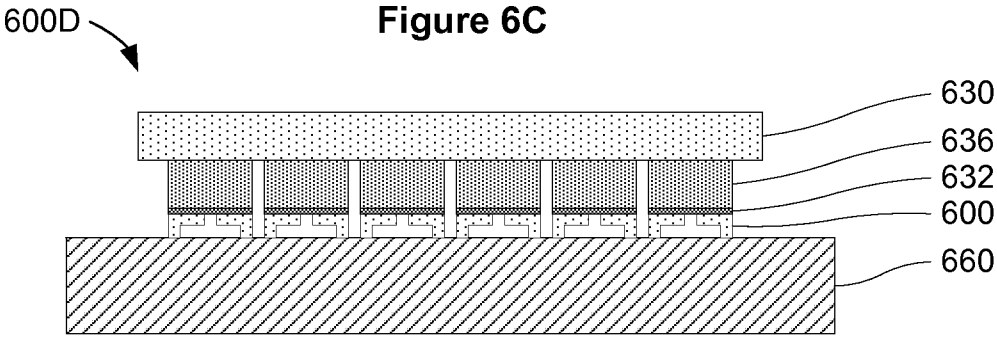


Figure 6D

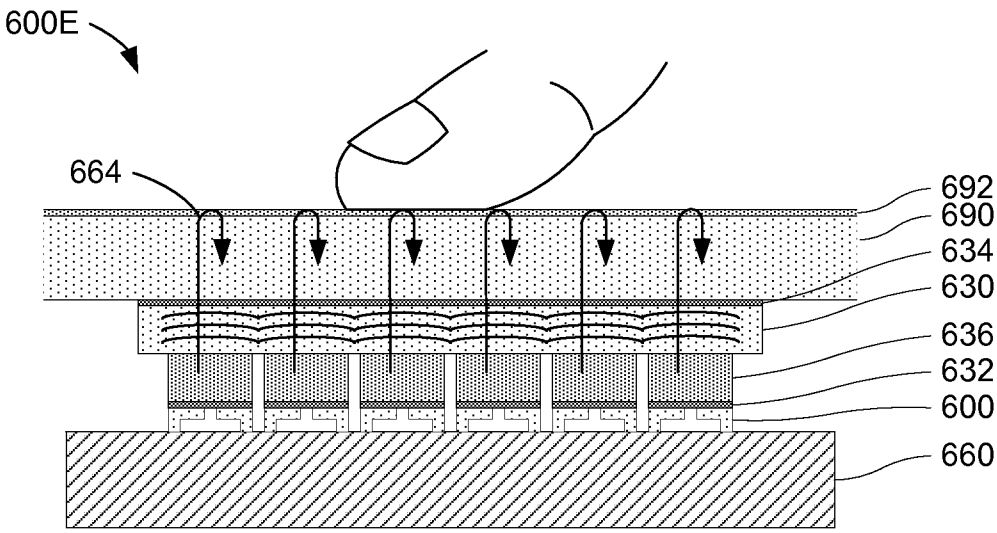


Figure 6E

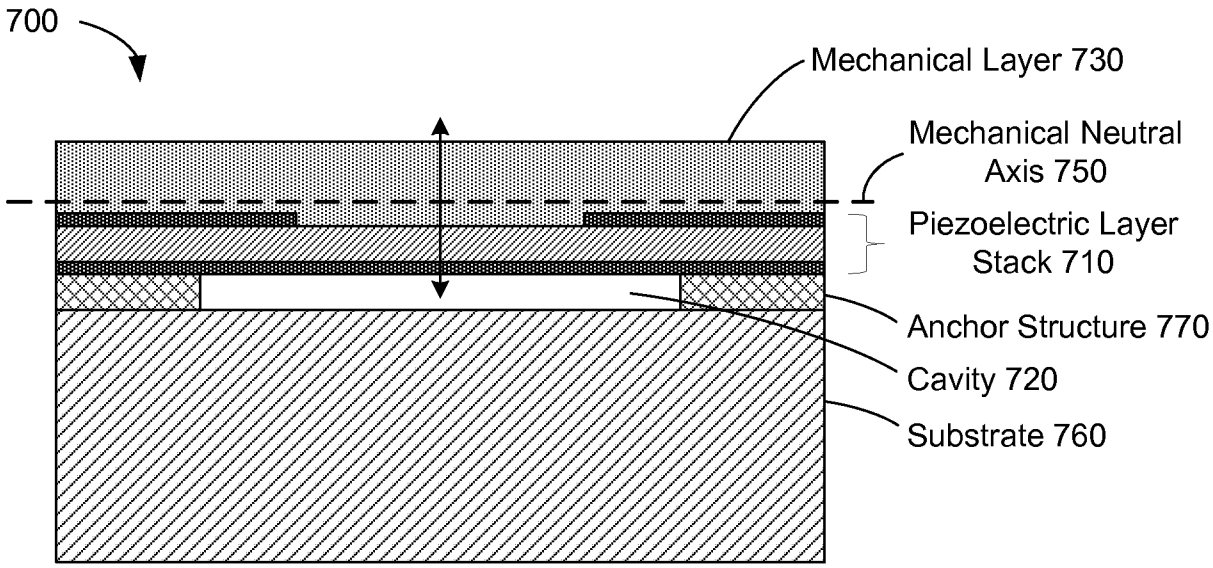


Figure 7A

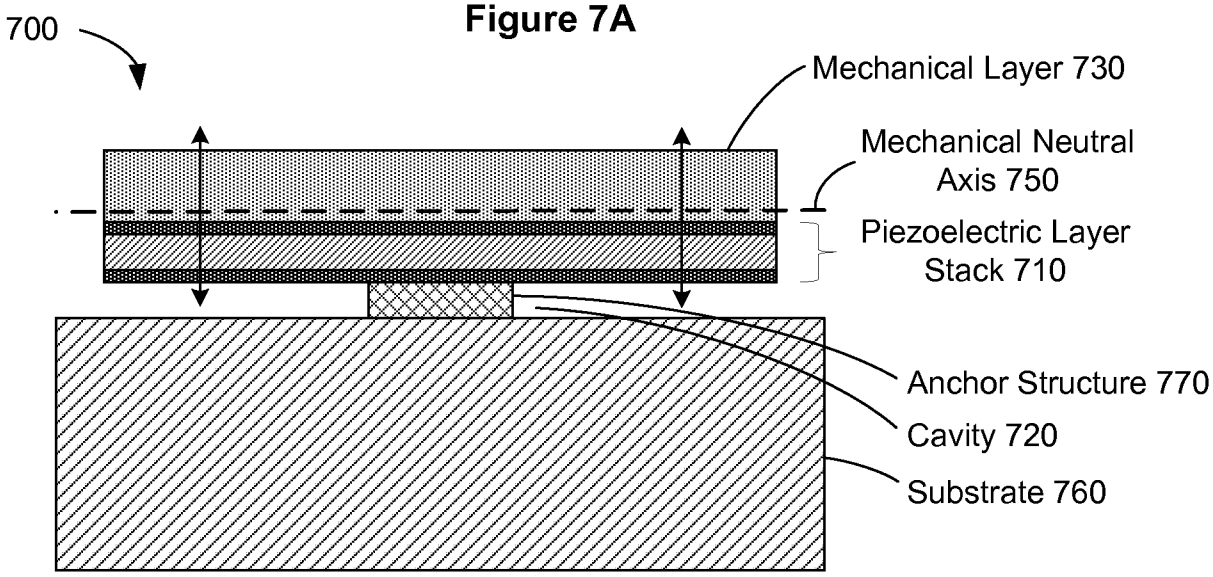


Figure 7B

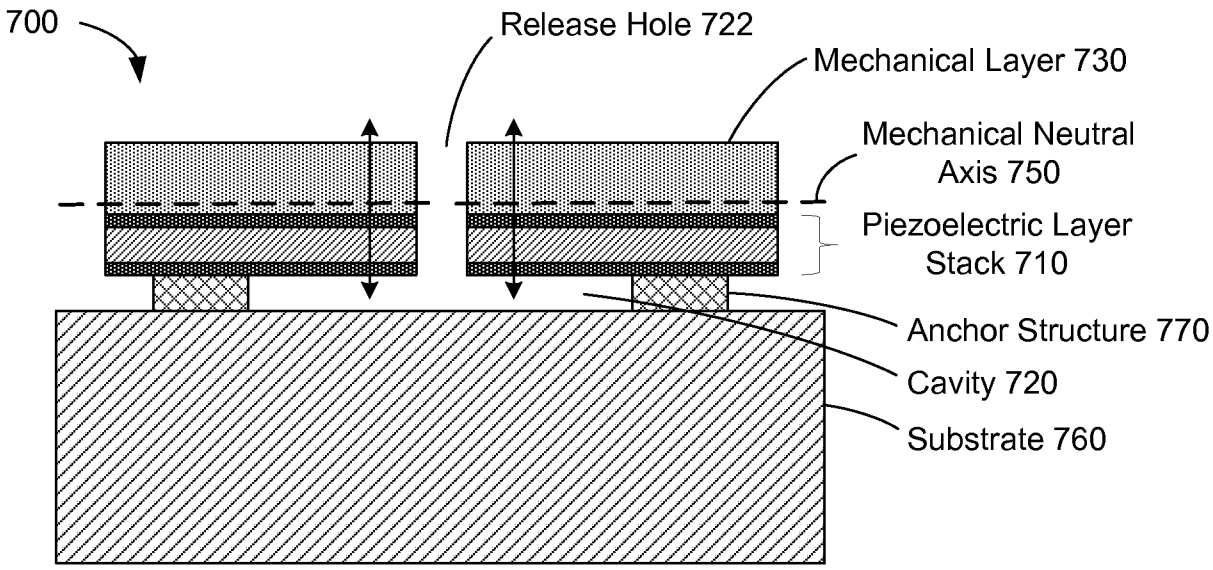


Figure 7C

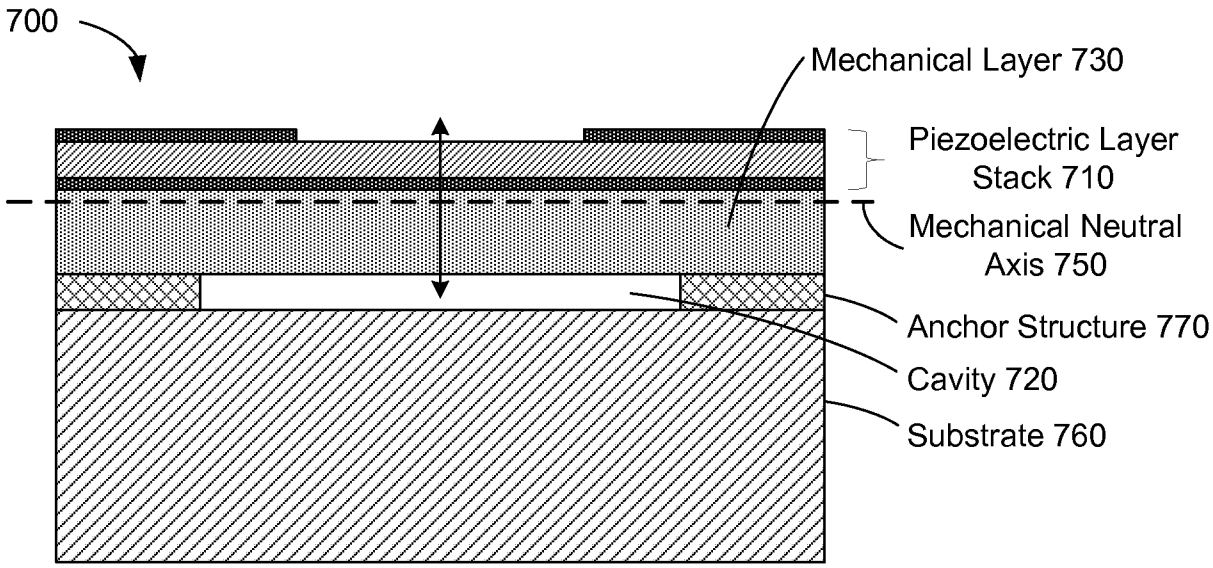


Figure 7D

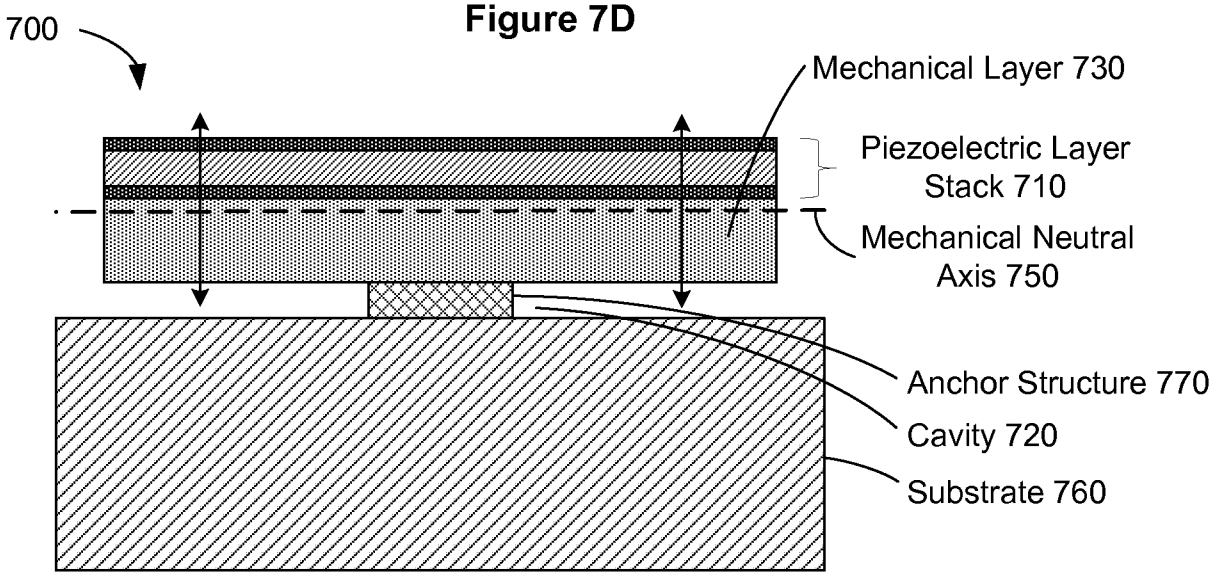


Figure 7E

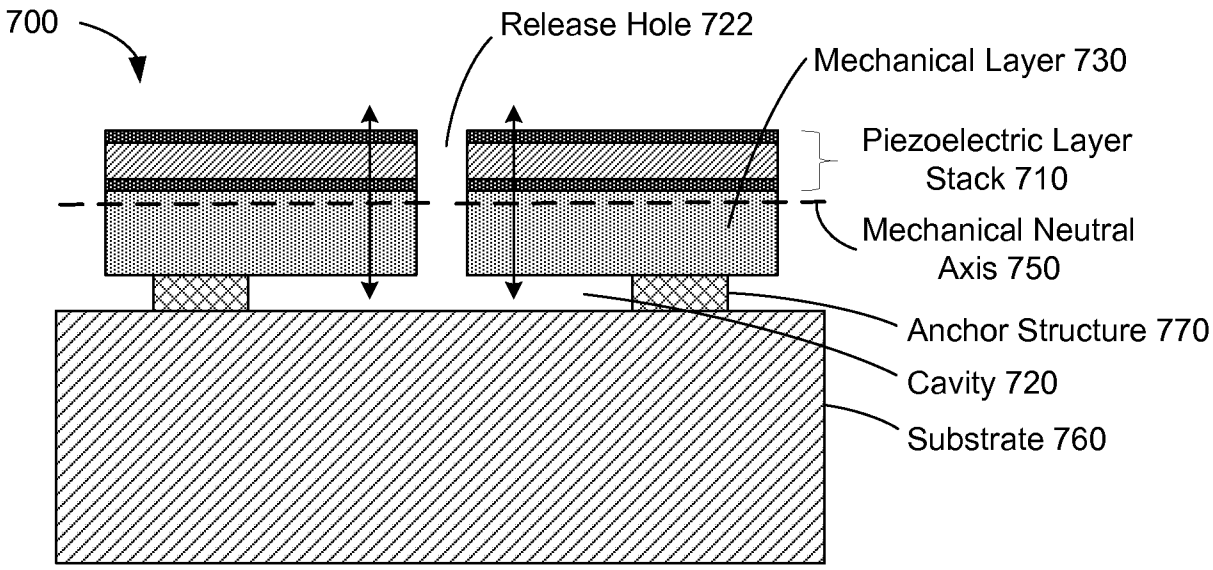


Figure 7F

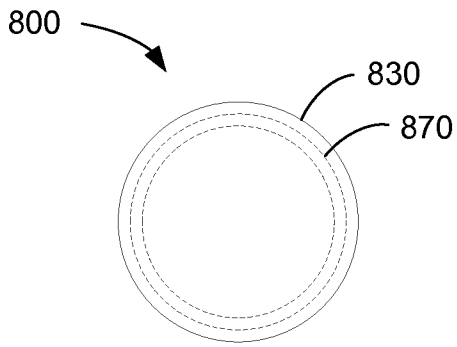


Figure 8A

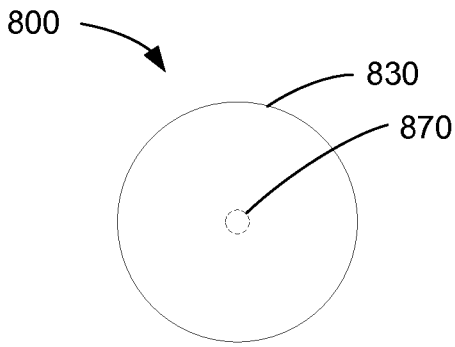


Figure 8B

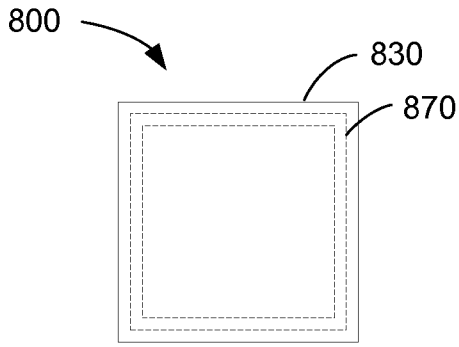


Figure 8C

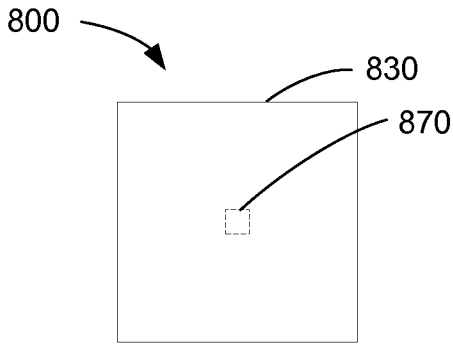


Figure 8D

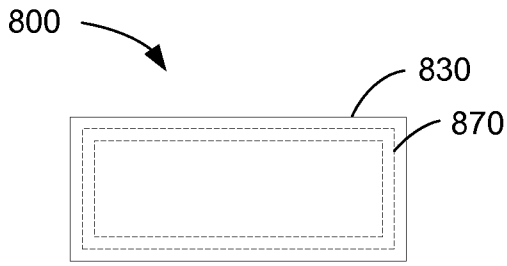


Figure 8E

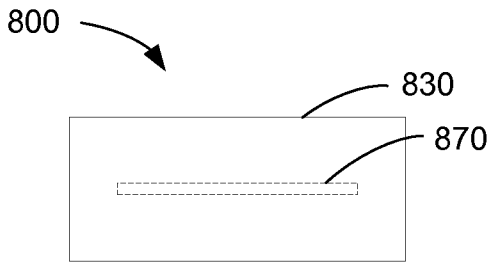


Figure 8F

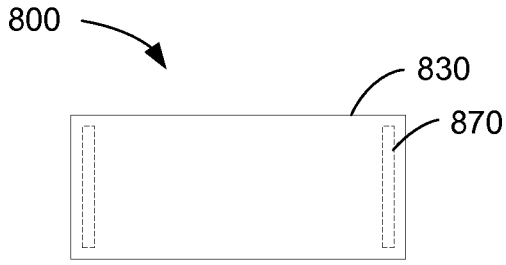


Figure 8G

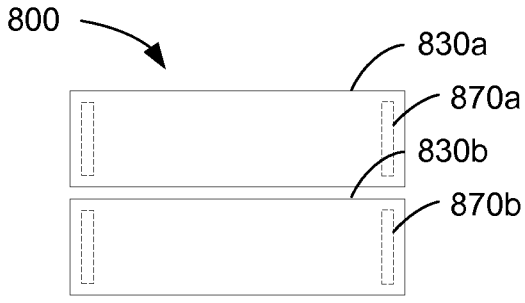


Figure 8H

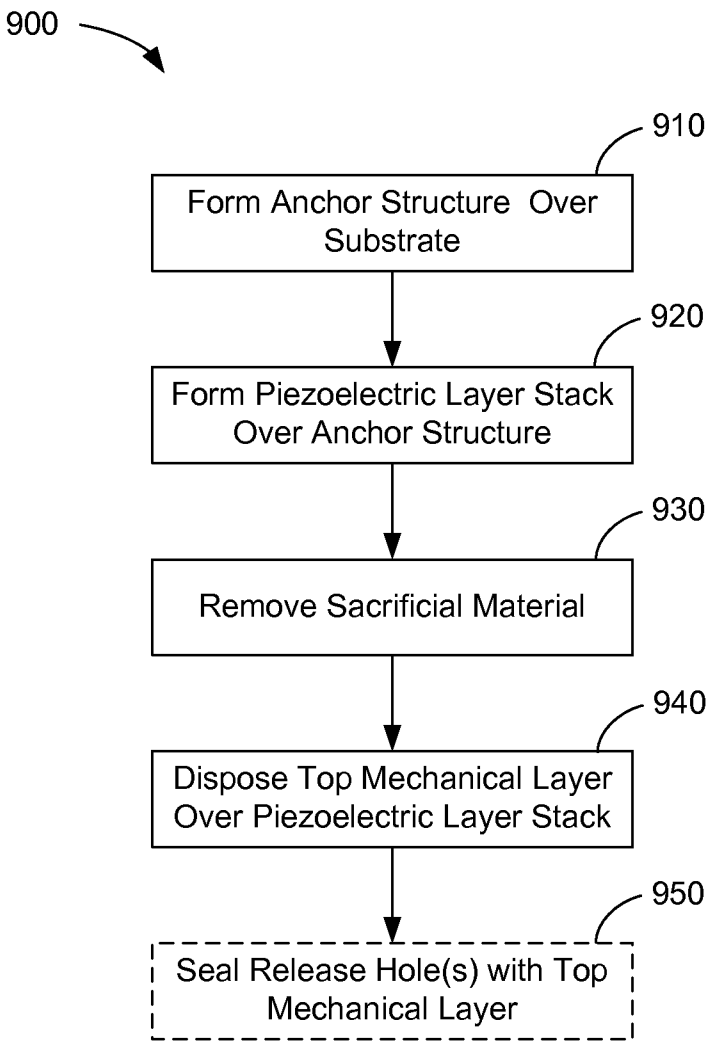

900
910
Form Anchor Structure Over Substrate
920
Form Piezoelectric Layer Stack Over Anchor Structure
930
Remove Sacrificial Material
940
Dispose Top Mechanical Layer Over Piezoelectric Layer Stack
950
Seal Release Hole(s) with Top Mechanical Layer

Figure 9

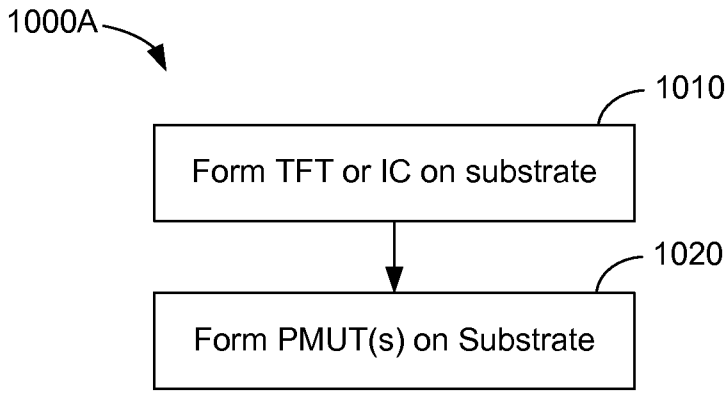


Figure 10A

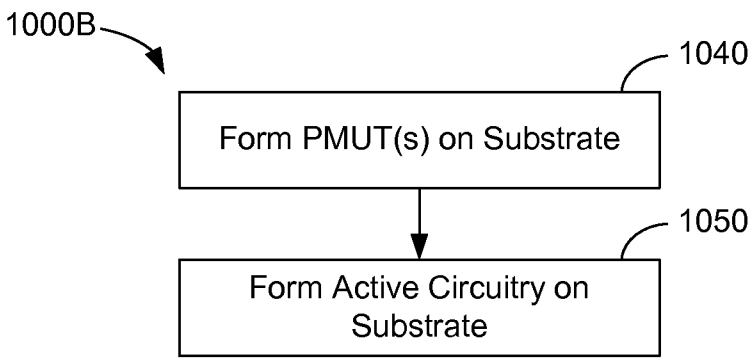


Figure 10B

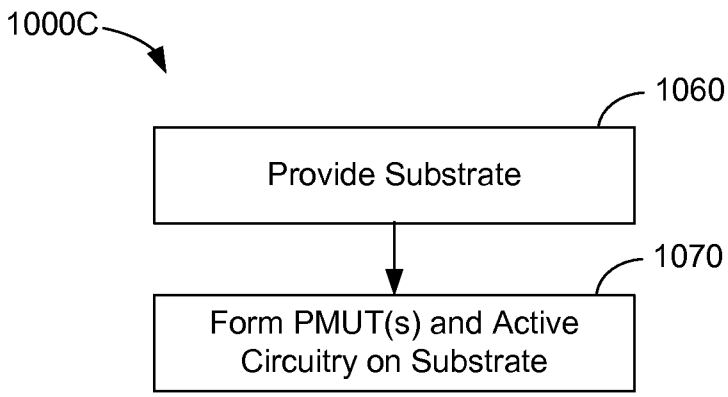


Figure 10C

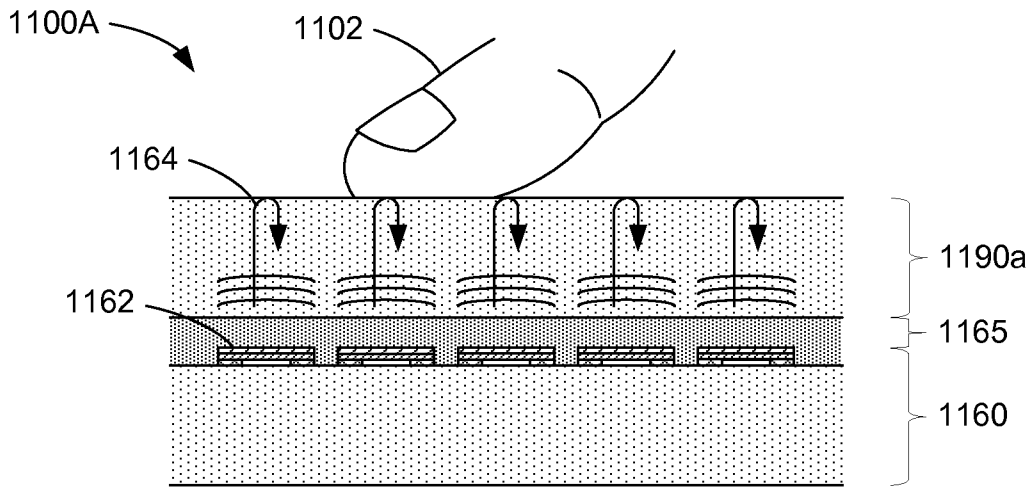


Figure 11A

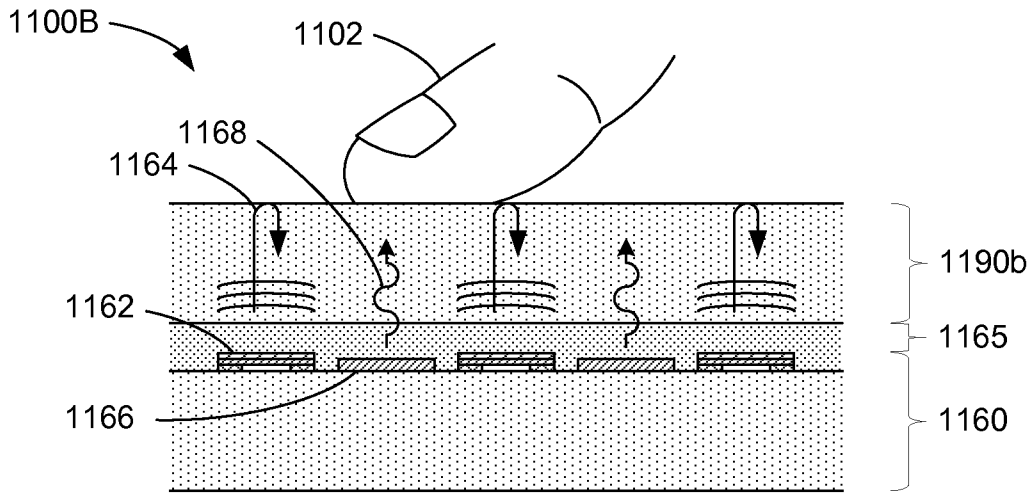


Figure 11B

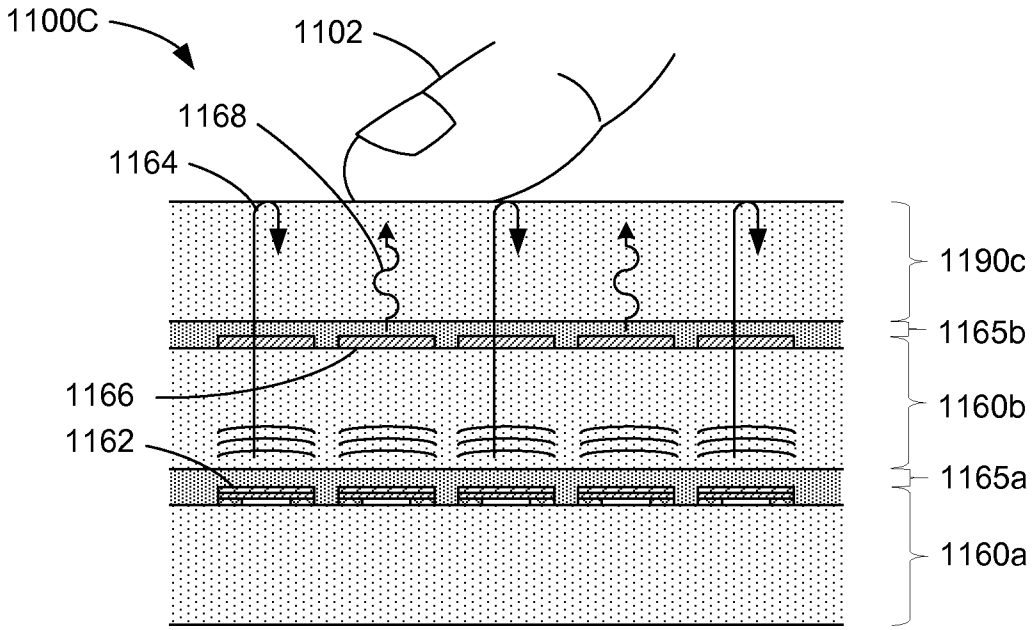


Figure 11C

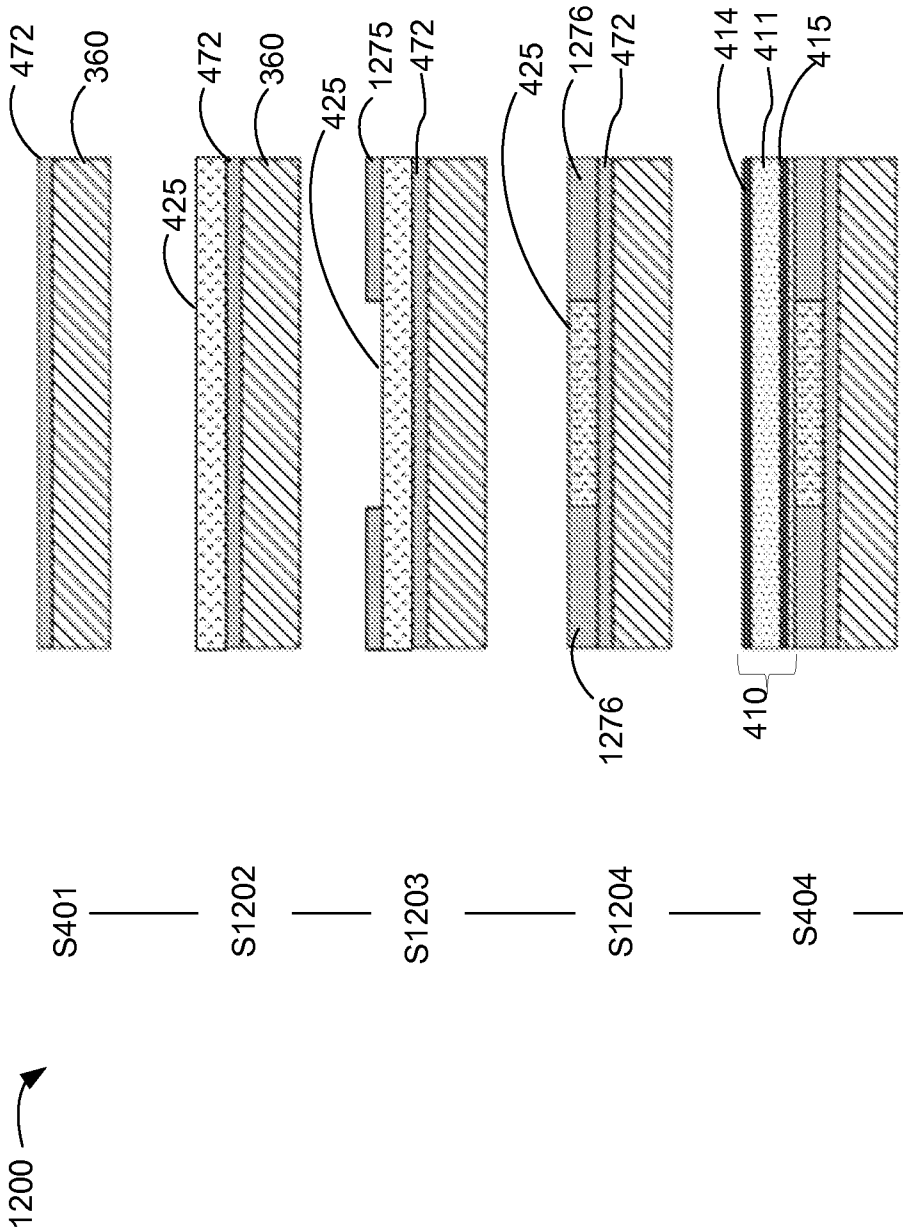

1200
S401
S1202
S1203
S1204
S404
To S405-S411
Figures 4A, 4B
472
360
425
1275
1276
414
411
415
410
Section A-A (Ref: Figure 3)

Figure 12

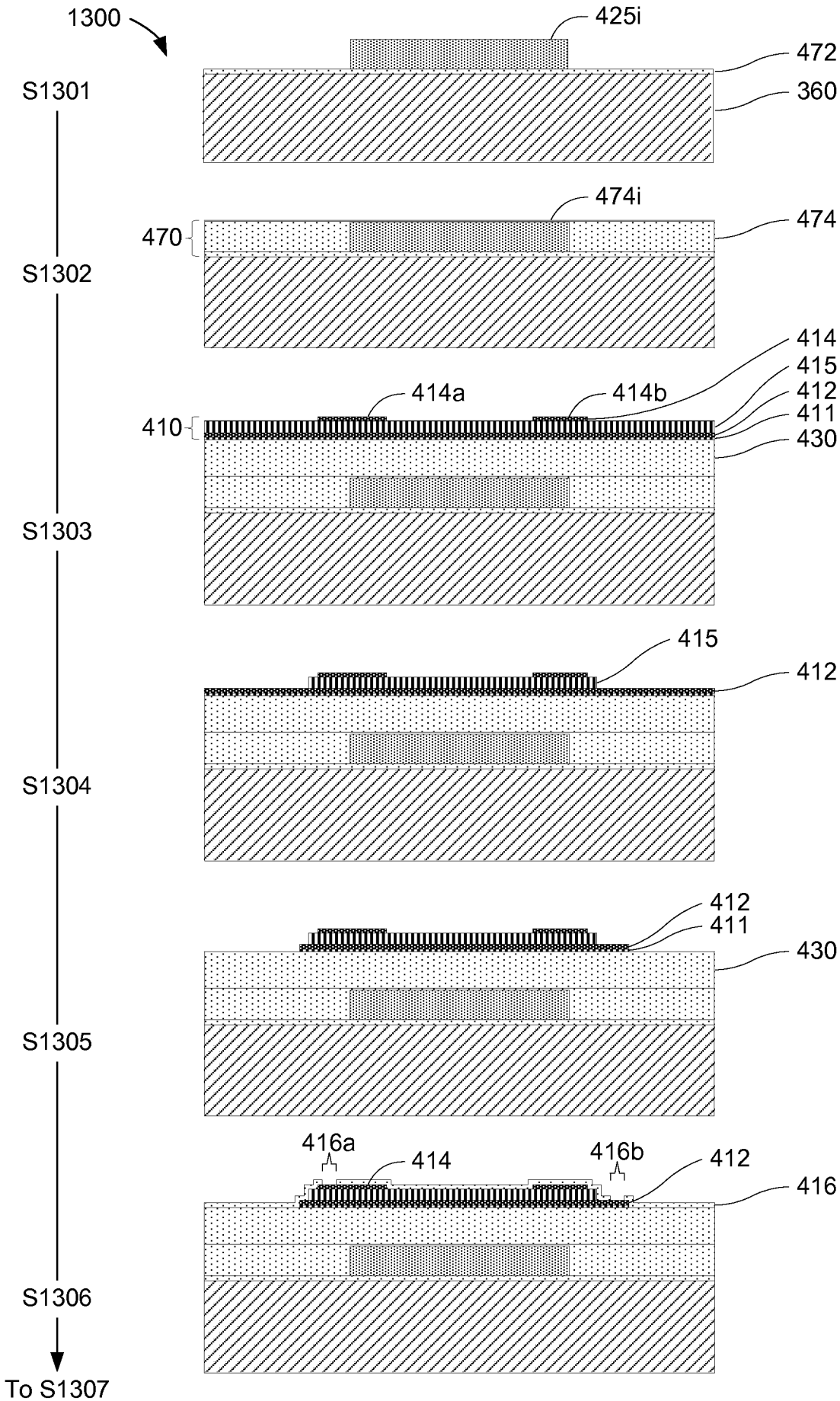

1300
S1301
S1302
S1303
S1304
S1305
S1306
To S1307
425i
472
360
474i
470
474
414
415
412
411
430
414a
414b
410
415
412
412
411
430
416a
414
416b
412
416

Figure 13A

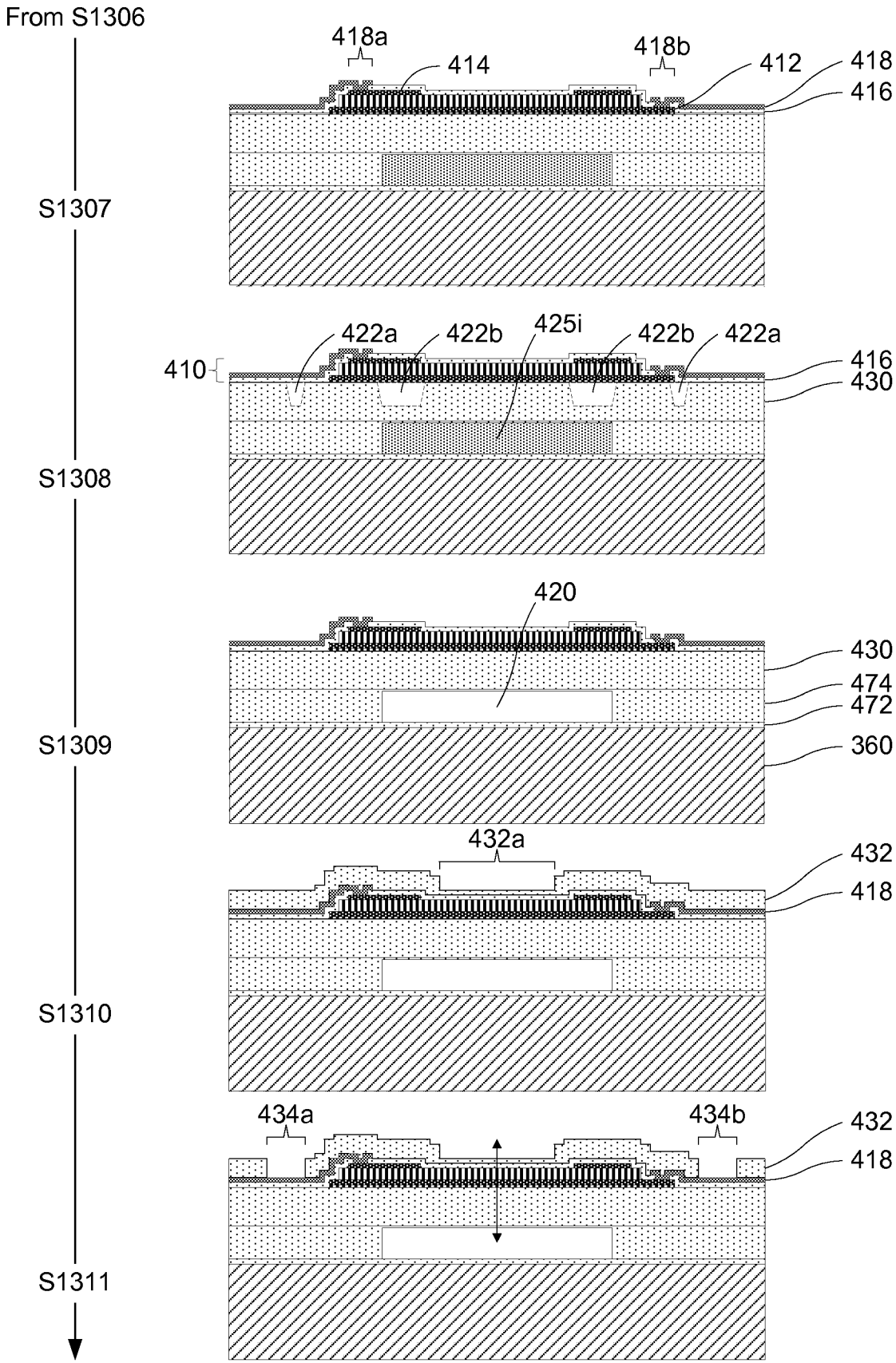

From S1306
418a
414
418b
412
418
416
S1307
422a
422b
425i
422b
422a
410
416
430
S1308
420
430
474
472
S1309
360
432a
432
418
S1310
434a
434b
432
418
S1311

Figure 13B

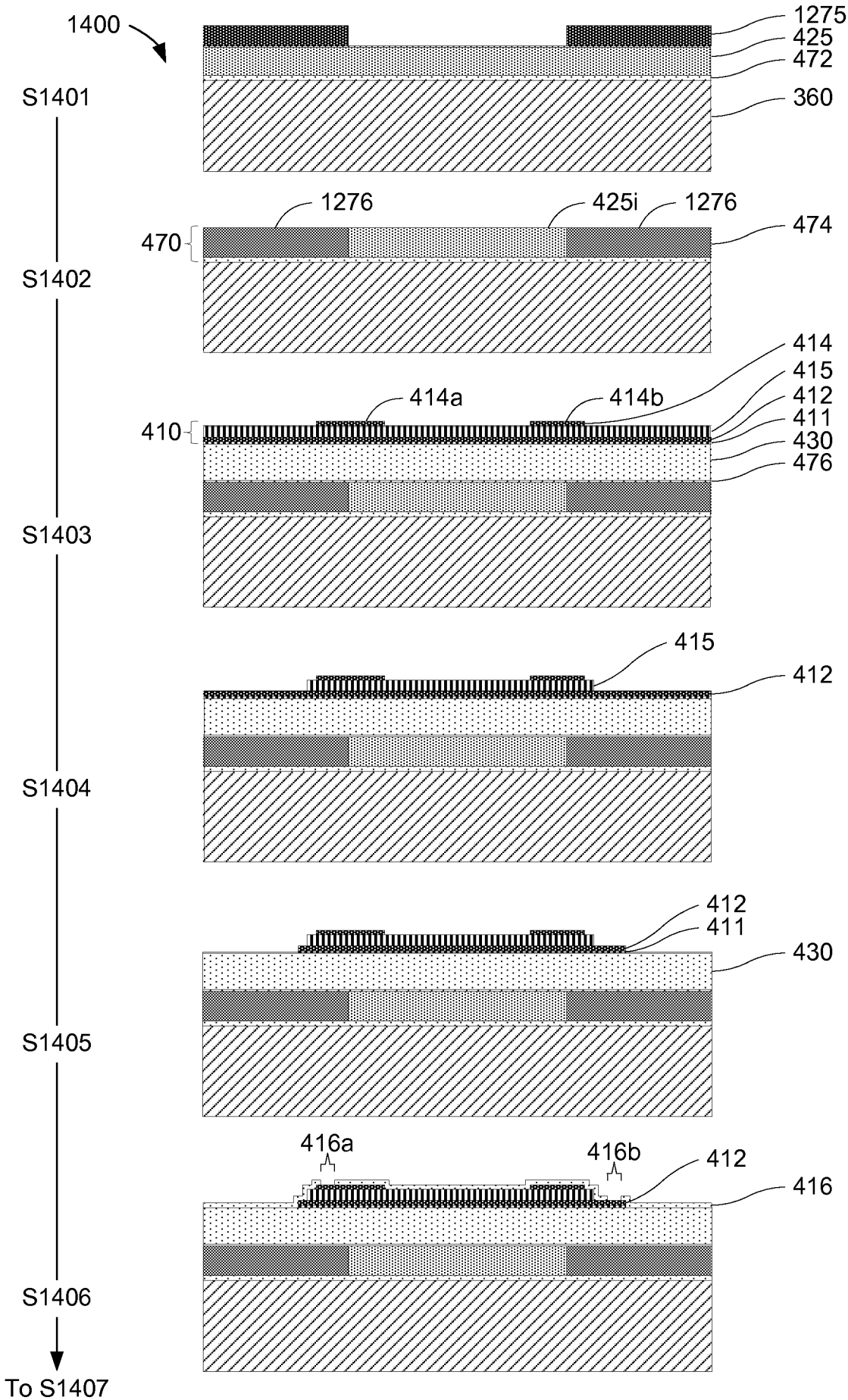

1400
S1401
1275
425
472
360
S1402
1276
425i
1276
470
474
S1403
414
415
414a
414b
412
410
411
430
476
S1404
415
412
S1405
412
411
430
S1406
416a
416b
412
416
To S1407

Figure 14A

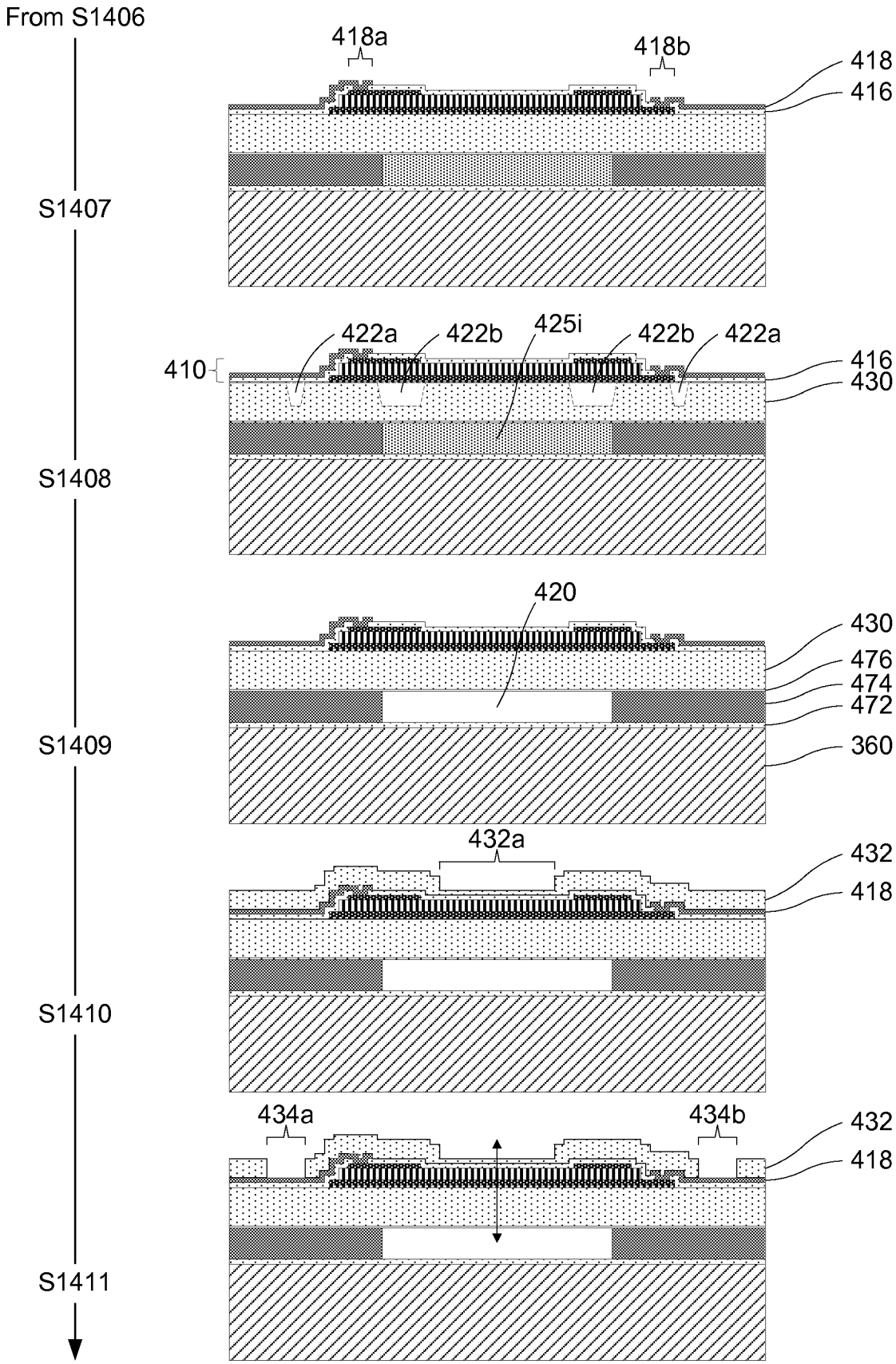

From S1406
418a
418b
418
416
S1407
422a
422b
425i
422b
422a
410
416
430
S1408
420
430
476
474
472
S1409
360
432a
432
418
S1410
434a
434b
432
418
S1411

Figure 14B

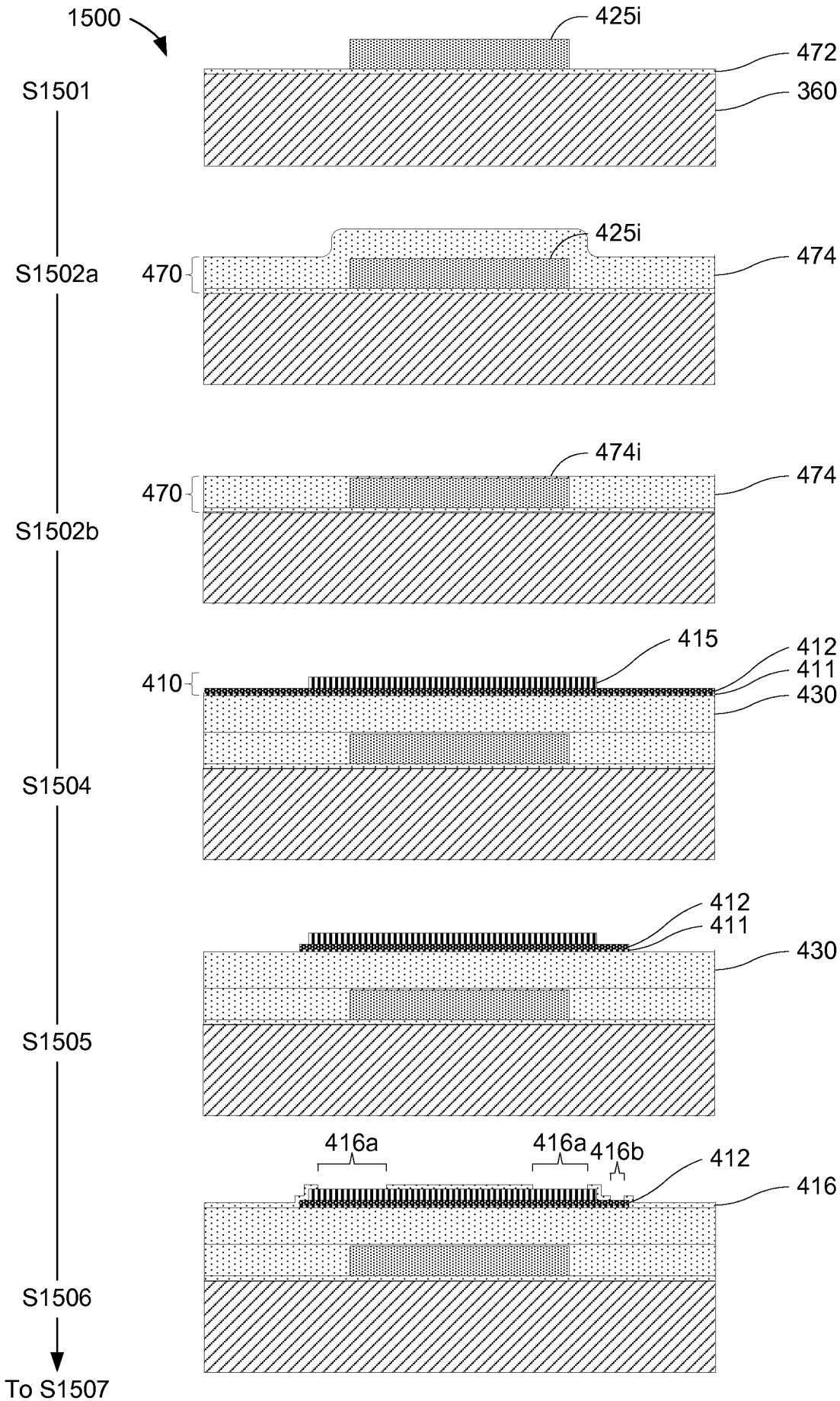

1500
S1501
425i
472
360
S1502a
470
425i
474
S1502b
470
474i
474
S1504
410
415
412
411
430
S1505
412
411
430
S1506
416a
416a
416b
412
416
To S1507

Figure 15A

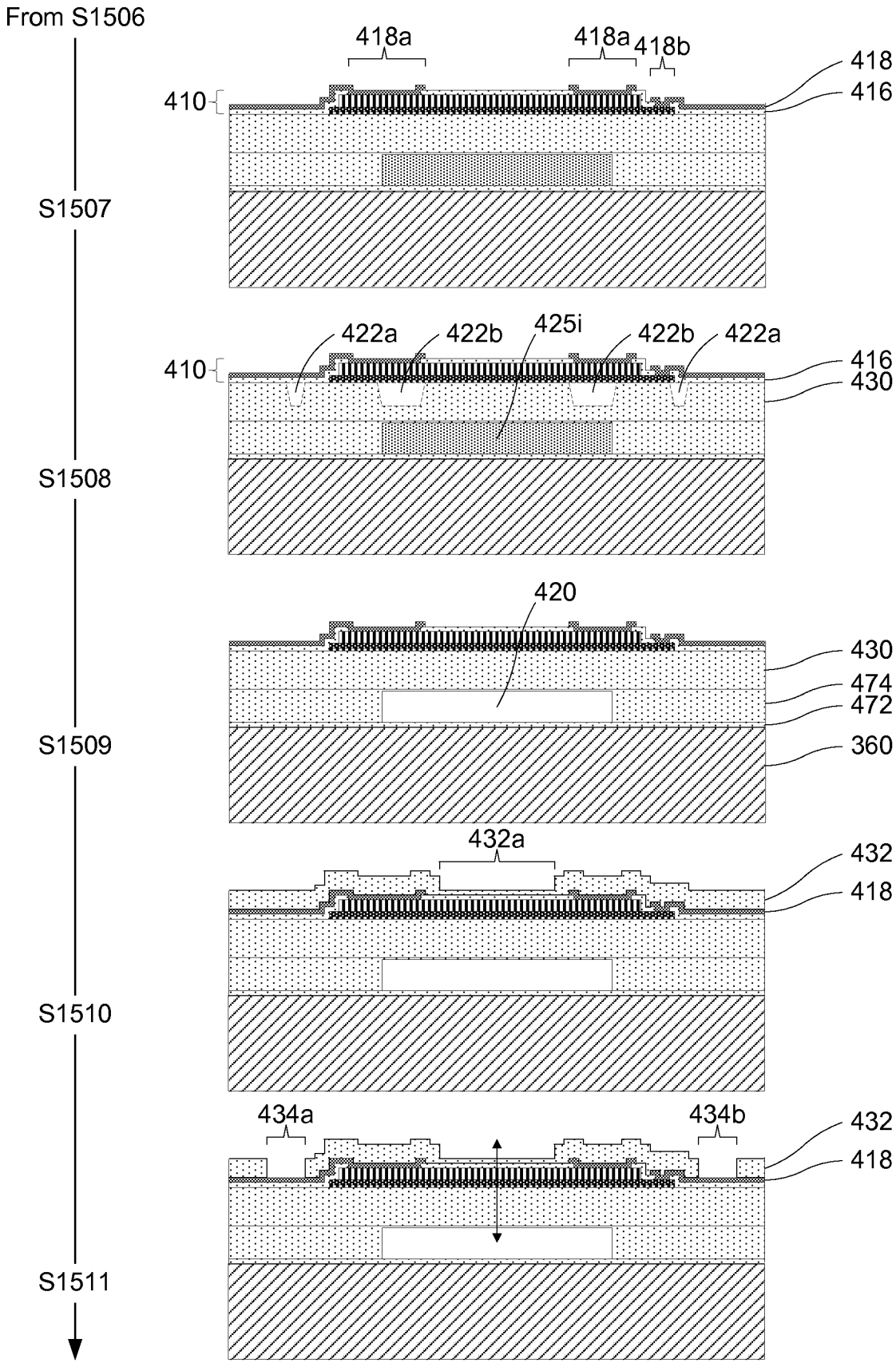

From S1506
S1507
S1508
S1509
S1510
S1511
418a
418a
418b
418
416
410
422a
422b
425i
422b
422a
410
416
430
420
430
474
472
360
432a
432
418
434a
434b
432
418

Figure 15B

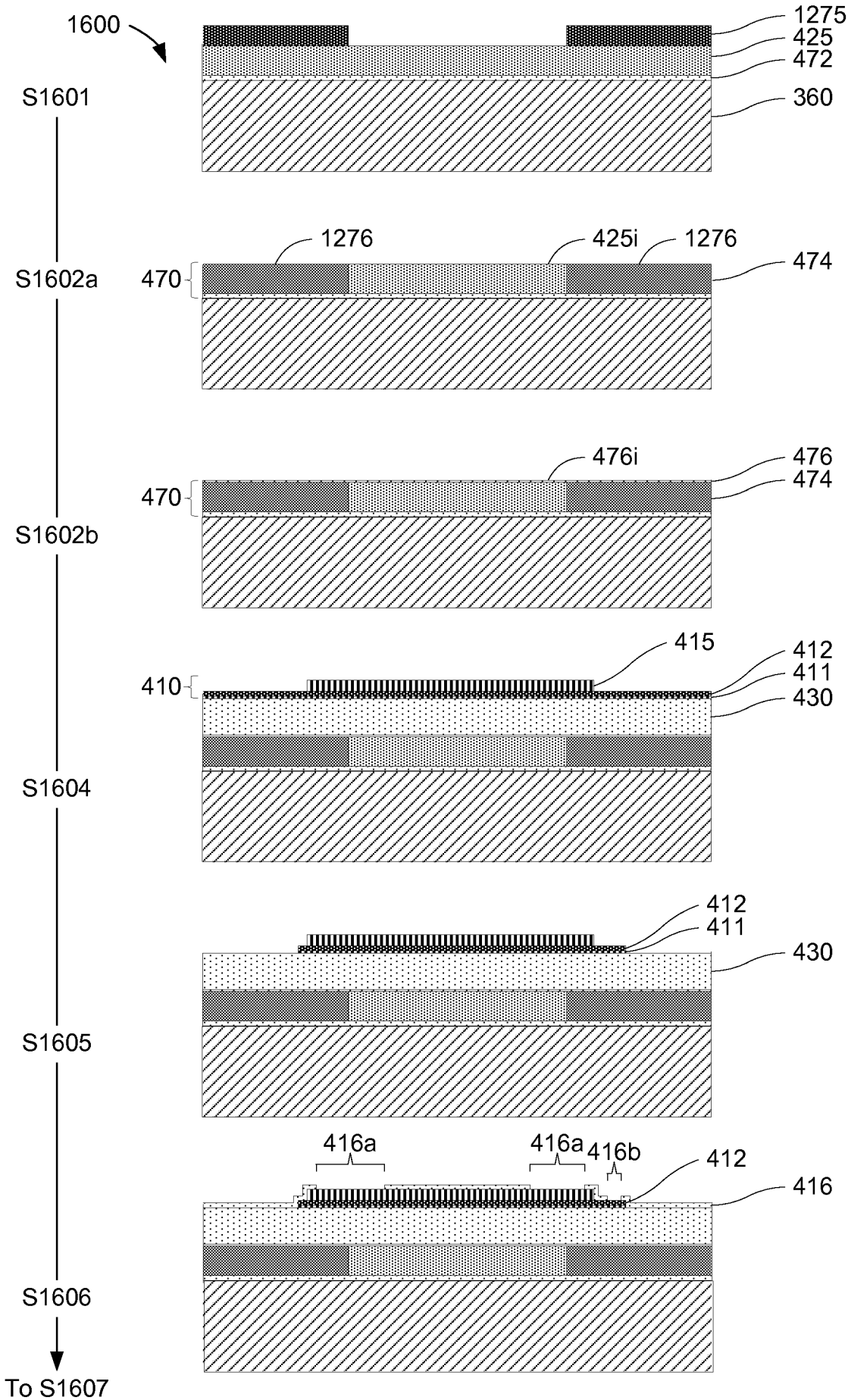

1600
S1601
1275
425
472
360
S1602a
470
1276
425i
1276
474
S1602b
470
476i
476
474
S1604
410
415
412
411
430
S1605
412
411
430
S1606
416a
416a
416b
412
416
To S1607

Figure 16A

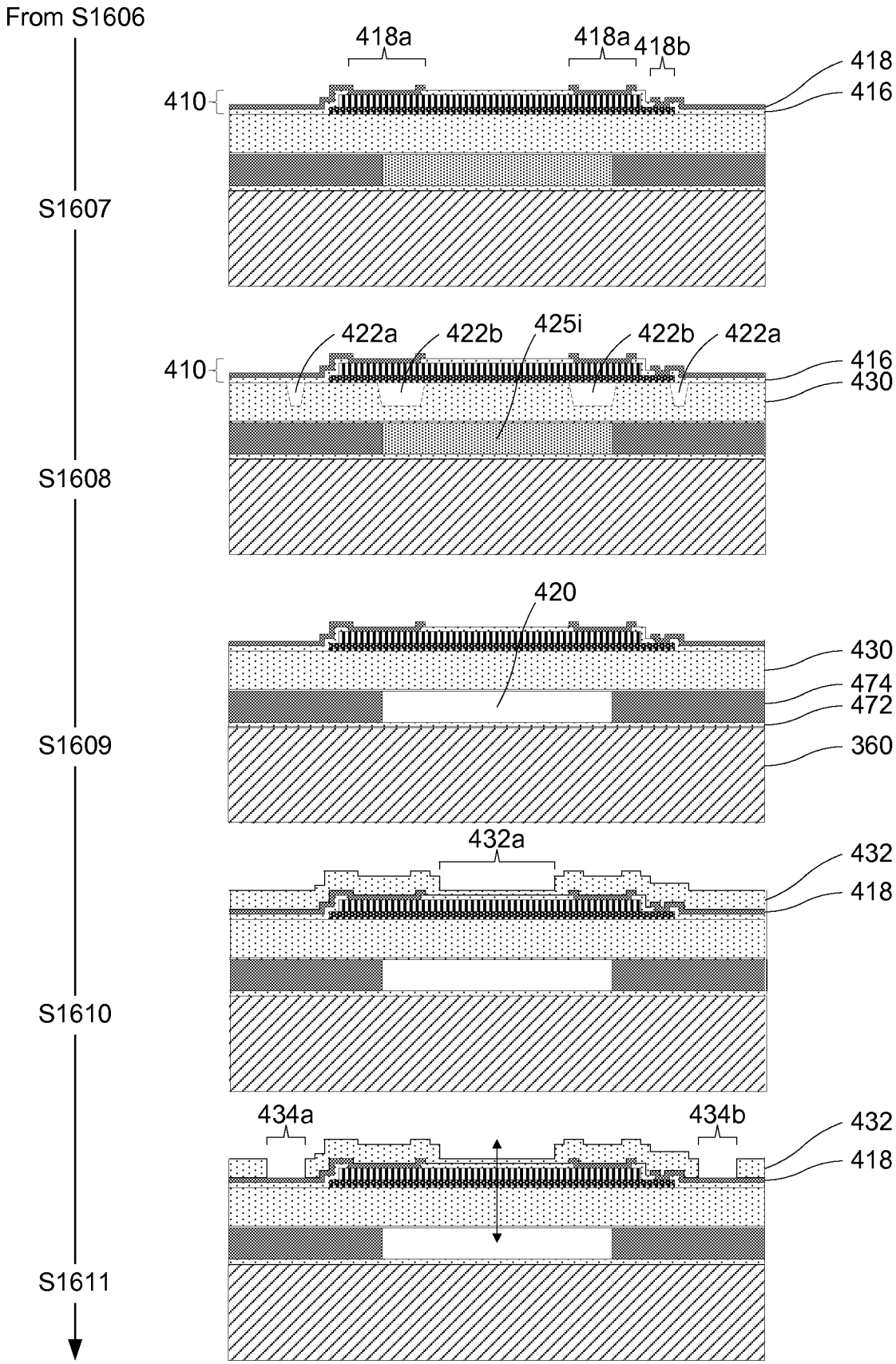
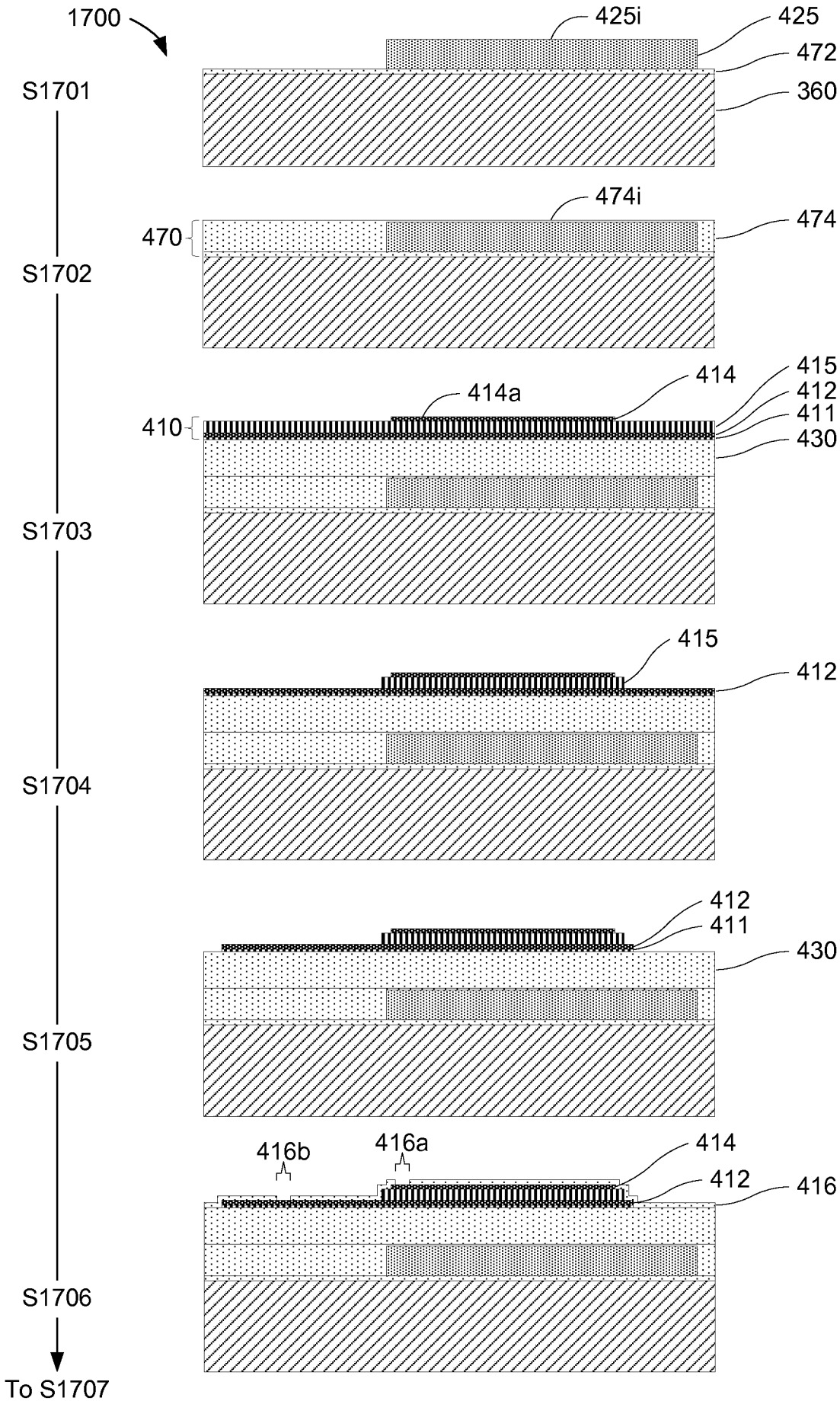

From S1606
S1607
S1608
S1609
S1610
S1611
418a
418a
418b
418
416
410
422a
422b
425i
422b
422a
416
430
410
420
430
474
472
360
432a
432
418
434a
434b
432
418

Figure 16B


1700
S1701
425i
425
472
360
S1702
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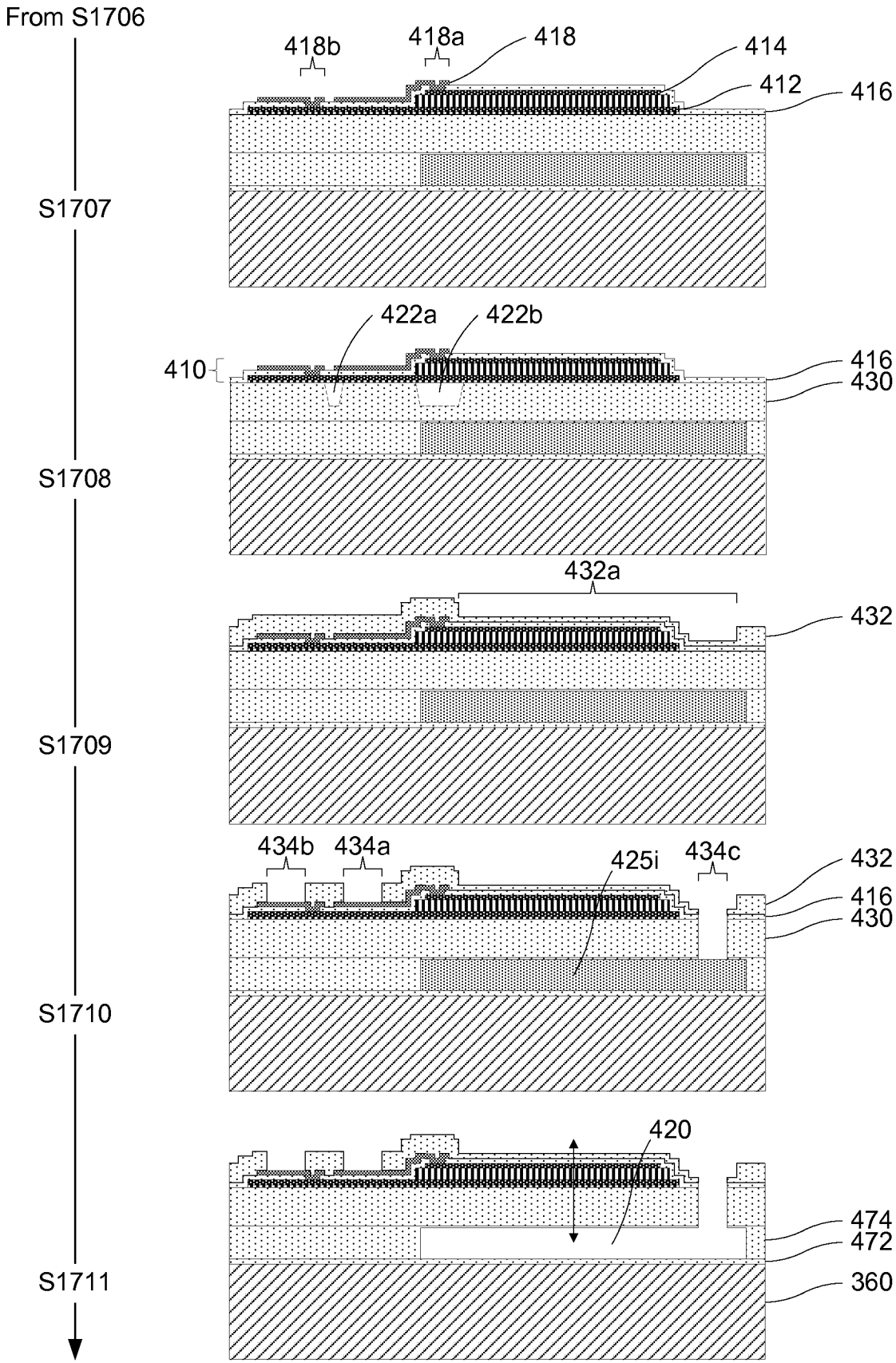
474i
474
S1703
410
414a
414
415
412
411
430
S1704
415
412
S1705
412
411
430
S1706
416b
416a
414
412
416
To S1707

Figure 17A


From S1706
418b
418a
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S1707
422a
422b
410
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430
S1708
432a
432
S1709
434b
434a
425i
434c
432
416
430
S1710
420
474
472
S1711
360

Figure 17B

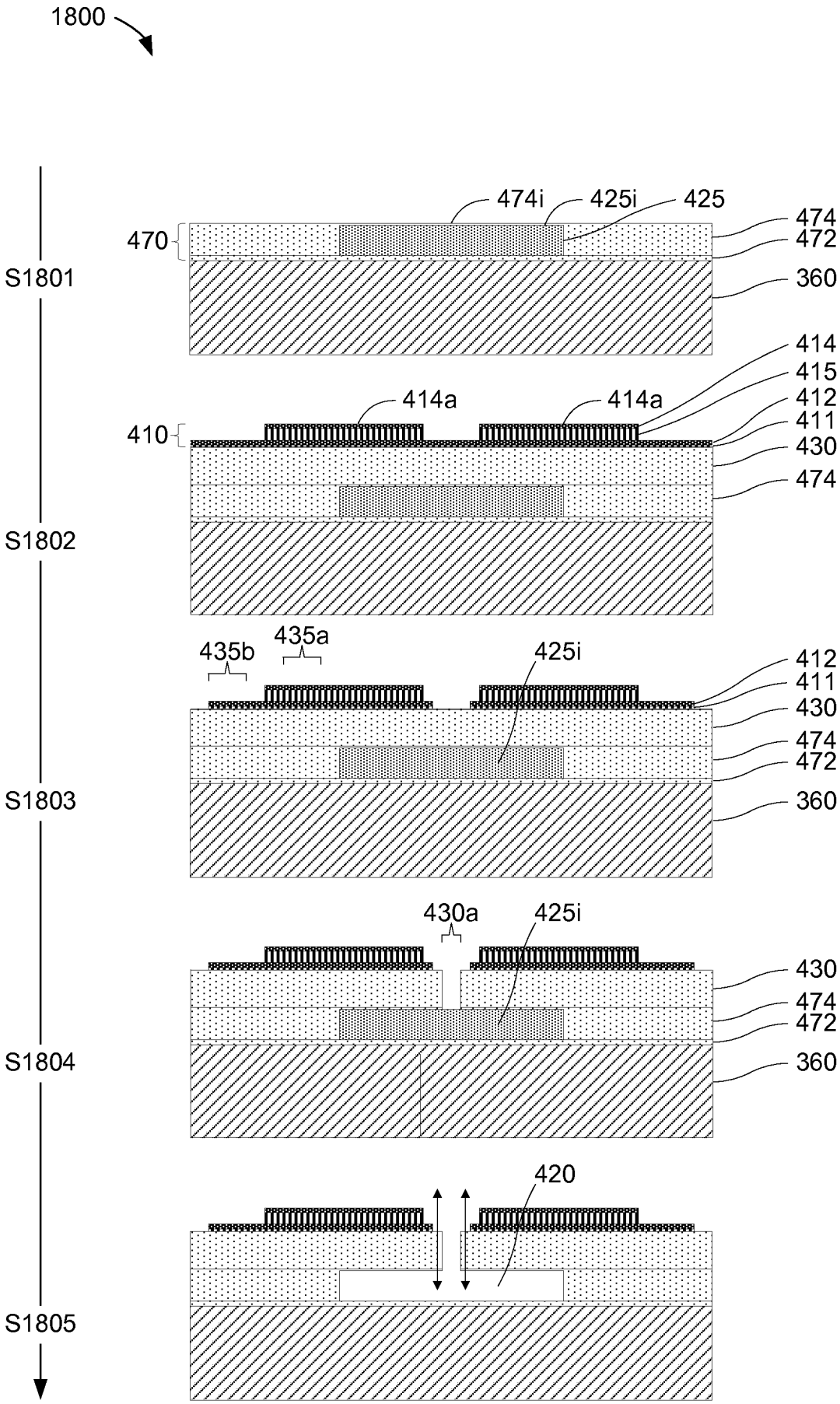
1800
S1801
S1802
S1803
S1804
S1805
470
474i
425i
425
474
472
360
410
414a
414a
414
415
412
411
430
474
435b
435a
425i
412
411
430
474
472
360
430a
425i
430
474
472
360
420

Figure 18

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/034729

A. CLASSIFICATION OF SUBJECT MATTER
INV. B06B1/06
ADD. G06F3/043 H01L41/09

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B06B G06F H01L G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/294201 A1 (HAJATI ARMAN [US]) 7 November 2013 (2013-11-07) figures 1-3B paragraphs [0031] - [0038], [0040] - [0045]	1-29
X Y	CN 101 712 028 A (CHINESE ACAD INST ACOUSTICS) 26 May 2010 (2010-05-26) figures 3-24 paragraphs [0002] - [0005], [0007] - [0011], [0062] - [0102]	1-6,8,9, 16-21 3,7, 10-15, 22-29

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2015	13/11/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Sartoni, Giovanni

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/034729

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/040477 A1 (SUGIURA MAKIKO [JP] ET AL) 22 February 2007 (2007-02-22)	1,2,4, 6-11, 13-15, 22-24, 26,28,29
Y	figures 1-6 paragraphs [0077] - [0082], [0092], [0135] - [0173], [0179], [0182], [0213]	3,7, 10-15, 22-29
A	- [0221]	16-21

X	US 2012/206014 A1 (BIBL ANDREAS [US] ET AL) 16 August 2012 (2012-08-16)	1,2,4,6, 8-10, 22-24, 26,29
Y	figures 1-5 paragraphs [0039] - [0041], [0054] - [0069], [0075] - [0090], [0016] - [0109]	3,10, 22-29
A		11-21

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/034729

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-29

All searchable inventions

1.1. claims: 1-6, 8-10, 16-27, 29

Piezoelectric micromechanical ultrasonic transducer comprising a mechanical layer disposed proximate to a piezoelectric layer stack, the mechanical layer together with the piezoelectric layer stack is supported by a anchor structure and forms a membrane over a cavity, the mechanical layer seals the cavity.

1.2. claims: 7, 11-15, 28

Piezoelectric micromechanical ultrasonic transducer comprising a mechanical layer disposed proximate to a piezoelectric layer stack, the mechanical layer together with the piezoelectric layer stack is supported by a anchor structure and forms a membrane over a cavity, the mechanical layer including a recess where the mechanical layer is locally thinned.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/034729

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013294201 A1	07-11-2013	CN 104271264 A	07-01-2015
		EP 2844400 A2	11-03-2015
		JP 2015521409 A	27-07-2015
		KR 20150005961 A	15-01-2015
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		DE 102005040081 A1	16-03-2006
		FR 2874780 A1	03-03-2006
		JP 4513596 B2	28-07-2010
		JP 2006094459 A	06-04-2006
		KR 20060050660 A	19-05-2006
		US 2006043843 A1	02-03-2006
		US 2007040477 A1	22-02-2007
		US 2008116765 A1	22-05-2008
US 2012206014 A1	16-08-2012	CN 103493510 A	01-01-2014
		EP 2676459 A2	25-12-2013
		JP 2014511055 A	01-05-2014
		KR 20140005289 A	14-01-2014
		US 2012206014 A1	16-08-2012
		US 2012235539 A1	20-09-2012
		US 2015298173 A1	22-10-2015
		US 2015298174 A1	22-10-2015
		WO 2012112540 A2	23-08-2012