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(54) **Title**: ARRAY SUBSTRATE AND REPAIR METHOD, DISPLAY PANEL AND DISPLAY APPARATUS

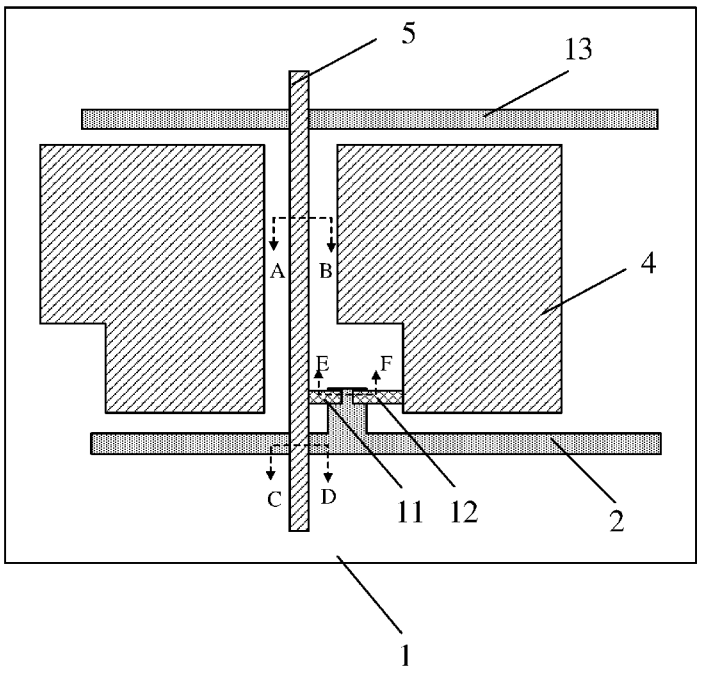

FIG. 1

(57) **Abstract**: An array substrate and a repair method are disclosed. The array substrate comprises a first metal layer including a signal line(3); a first repair layer; and a first insulating layer(9). The first insulating layer(9) is disposed between, and provides insulation between, the first metal layer and the first repair layer, and it is configured to be penetrable to allow the first repair layer to electrically connect the signal line(3) to thereby repair connection weakness of the signal line(3). The first repair layer can comprise a first repair line(5), which is disposed over and along the signal line(3) and is configured to be able to electrically connect two ends of a weak connection portion of the signal line(3) through penetrating the first insulating layer(9).

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ARRAY SUBSTRATE AND REPAIR METHOD, DISPLAY PANEL AND DISPLAY APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

[001] The present application claims priority to Chinese Patent Application No. 201610086241.1 filed on February 15, 2016, the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[002] The present disclosure relates to display technologies, and more specifically to an array substrate and its repair method, a display panel and a display apparatus.

BACKGROUND

[003] Flat-panel display apparatuses, such as Liquid Crystal Display (LCD) apparatus, Plasma Display Panel (PDP), Organic Light-Emitting Diode (OLED) display apparatuses, etc., have been developed rapidly due to their advantages over traditional displays, such as light weight, small size, and low power consumption.

SUMMARY

[004] The inventors of the present disclosure have recognized that when repairing data line open circuits employing bridging with tungsten powder, and laser cutting or scraping, the second transparent electrode layer can be easily damaged, causing decreased display quality or display abnormalities of peripheral pixels.

[005] In one aspect, the present disclosure provides an array substrate. The array substrate comprises a first metal layer including a signal line, a first repair layer, and a first insulating layer. The first insulating layer is disposed between, and provides insulation between, the first metal layer and the first repair layer, and it is configured to be penetrable to allow the first repair layer to electrically connect the signal line to thereby repair connection weakness of the signal line.

[006] In some embodiments, the first repair layer comprises a first repair line, which is disposed over and along the signal line and is configured to be able to electrically connect two ends of a weak connection portion of the signal line through vias penetrating the first insulating layer.

[007] In some embodiments, the array substrate further includes a substrate, and the projection of the first repair line on the substrate overlaps with the projection of the signal line on the substrate in a longitudinal direction.

[008] The signal line in the first metal layer can comprise a data line, but can also comprise some other type of the signal line.

[009] The first repair line can be an integral wire, but in some preferred embodiments, the first repair line can comprise a plurality of first segments, which are electrically disconnected from one another.

[010] The array substrate can further comprise a second repair layer including a second repair line. The second repair line is insulated from, and disposed over and along, the data line. The projection of the second repair line on the substrate overlaps with the projection of the data line on the substrate in a longitudinal direction; and the second repair line can also include a plurality of second segments, which are electrically disconnected from one another. The plurality of first segments of the first repair line and the plurality of second segments of the second repair line are configured such that at least one of one corresponding first segment of the first repair line or one corresponding second segment of the second repair line is able to electrically connect the two ends of the weak

connection portion of the data line through one or more vias.

[011] In some of the embodiments as described above, tach one of the plurality of first segments of the first repair line can be staggered with, and partially overlapped at ends with, one of the plurality of second segments of the second repair line.

[012] In some embodiments, the first repair layer and the second repair layer can be a pixel electrode layer and a common electrode layer, or can be a common electrode layer or a pixel electrode layer.

[013] In embodiments where the first repair layer is a pixel electrode layer, and the second repair layer is a common electrode layer, the pixel electrode layer can also include a plurality of pixel electrodes, which are insulated from the first repair line, and the common electrode layer can include a plurality of common electrodes, which are insulated from the second repair line.

[014] The array substrate can further comprise a second metal layer, which includes a plurality of gate lines. In such an embodiment, the second repair layer, the second metal layer, the first metal layer, and the first repair layer can be sequentially disposed on the substrate; and the plurality of gate lines in the second metal layer are insulated from the second repair line in the second repair layer.

[015] In some embodiments, the array substrate can further include a second insulating layer, which is disposed between, and configured to insulate, the second metal layer and the first metal layer.

[016] In a second aspect, the present disclosure provides a display panel, which includes the array substrate according to any of the embodiments as described above.

[017] In a third aspect, the present disclosure provides a display apparatus, which includes the display panel as described above.

[018] In a fourth aspect, the present disclosure provides a method for

repairing the array substrate as described above. The method includes a step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line.

[019] In some embodiments of the method, the step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line is performed by welding the first repair line with the two ends of the weak connection portion of the signal line through vias.

[020] In some embodiments of the method, the first repair line can include a plurality of first segments, which are electrically disconnected from one another; and the step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line can be performed by welding one of the plurality of first segments of the first repair line with the two ends of the weak connection portion of the signal line through vias.

[021] In some embodiments, the array substrate may also include a second repair layer and second repair lines. The repair method may include: connecting the two ends of the weak connection portion of the data line with vias through at least one of one corresponding first segment of the first repair line or one corresponding second segment of the second repair line.

[022] If projection of the weak connection portion of the data line on the substrate falls within projection of one first segment of the first repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected by welding the one first segment of the first repair line with the two ends of the weak connection portion of the data line with two vias.

[023] Alternatively, if projection of the weak connection portion of the data line on the substrate falls within projection of one second segment of the second repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected by welding the one second segment of the second repair line with the two ends of the

weak connection portion of the data line with two vias.

[024] Alternatively, if projection of the weak connection portion of the data line on the substrate falls within an overlapping region between projection of one first segment of the first repair line on the substrate and projection of one second segment of the second repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected by welding the one second segment of the second repair line with the two ends of the weak connection portion of the data line with two vias, or by welding the one second segment of the second repair line with the two ends of the weak connection portion of the data line with two vias.

[025] Other embodiments and implementations can become apparent in view of the following descriptions and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[026] To more clearly illustrate some of the embodiments of the disclosure, the following is a brief description of the drawings. The drawings are only illustrative of some embodiments, and for those of ordinary skill in the art, other drawings of other embodiments can become apparent based on these drawings.

[027] FIG. 1 is a partial view of the structure of an array substrate according to one embodiment of the present disclosure;

[028] FIG. 2 is a partial top view of the structure of the pixel electrode and the first repair line in the array substrate as shown in FIG. 1;

[029] FIG. 3 is a partial cross-section view of the array substrate at position AB as shown in FIG. 1;

[030] FIG. 4 is a partial cross-section view of the array substrate at position CD as shown in FIG. 1;

[031] FIG. 5 is a partial cross-section view of the array substrate at position EF as shown in FIG. 1;

[032] FIG. 6 is a partial view of the structure of an array substrate according to another embodiment of the present disclosure;

[033] FIG. 7 is a partial top view of the common electrode and the second repair line in the array substrate as shown in FIG. 6;

[034] FIG. 8 is a partial top view of the pixel electrode and the first repair line in the array substrate as shown in FIG. 6;

[035] FIG. 9 is a partial cross-section view of the array substrate at position AB as shown in FIG. 6;

[036] FIG. 10 is a partial cross-section view of the array substrate at position CD as shown in FIG. 6.

[037] FIG. 11 is a partial top view of an array substrate where an open portion of a data line is reconnected according to a first embodiment of the repair method.

DETAILED DESCRIPTION

[038] In the following, with reference to the drawings of various embodiments disclosed herein, the technical solutions of the embodiments of the disclosure will be described in a clear and fully understandable way. It is obvious that the described embodiments are merely a portion but not all of the embodiments of the disclosure. Based on the described embodiments of the disclosure, those ordinarily skilled in the art can obtain other embodiment(s), which come(s) within the scope sought for protection by the disclosure.

[039] It should be noted that throughout the disclosure same or similar reference numerals denote the same or similar components or components

that have same or similar functionality.

[040] In an advanced super dimension switch (ADS) display apparatus, a fringe electrical field can be formed through electrodes between pixels within the same plane. Liquid crystal molecules between the electrodes and directly over the electrodes can rotate in the direction of the plane, that is, in a direction parallel to the substrate. As a result, the viewing angel can be increased, and the light-emitting efficiency can be improved.

[041] A conventional array substrate of an ADS display apparatus typically includes: a first transparent electrode layer, a gate layer, a gate insulating layer, a source-drain electrode layer, a second insulating layer, and a second transparent electrode layer of the pixel electrode.

[042] The transparent electrode layer can comprise indium-tin oxide (ITO). The first transparent electrode layer is usually a common electrode layer. The second transparent electrode layer is usually the pixel electrode layer. The gate line and the common electrode line are usually formed in the gate layer. The data line is usually formed in the source-drain electrode layer. As such, the array substrate comprising thin film transistors can be formed.

[043] If there is a data line failure, a repair process may be employed, such as laser cutting, laser chemical vapor deposition (Laser CVD), laser welding, etc. For data line open circuit failures, in most cases a laser CVD equipment is needed to bridge and connect the open portions of the data line with tungsten powder, and the surrounding area of the bridge needs to be processed. For example, laser cutting or scraping of the second transparent electrode layer may be employed.

[044] When repairing data line open circuits employing the conventional repair process, such as bridging with tungsten powder, laser cutting, or scraping, the second transparent electrode layer can be easily damaged, causing decreased display quality or display abnormalities of peripheral pixels.

[045] In order to address these above issues, the present disclosure provides an array substrate. The array substrate comprises a first metal layer including a signal line; a first repair layer; and a first insulating layer. The first insulating layer is disposed between, and provides insulation between, the first metal layer and the first repair layer, and it is configured to be penetrable to allow the first repair layer to electrically connect the signal line to thereby repair connection weakness of the signal line.

[046] In some embodiments, the first repair layer comprises a first repair line, which is disposed over and along the signal line and is configured to be able to electrically connect two ends of a weak connection portion of the signal line through vias penetrating the first insulating layer.

[047] In some embodiment as illustrated below, the signal line can be data lines.

[048] Embodiment 1:

[049] With reference to FIGS. 1-3, the disclosure provides an array substrate, comprising a second metal layer, a first metal layer, and a pixel electrode layer, which are sequentially disposed over a substrate 1. The first metal layer comprises data lines 3; the second metal layer comprises gate lines 2; and the pixel electrode layer comprises pixel electrodes 4.

[050] First repair lines 5 are also disposed in the pixel electrode layer, and the vertical projection of the first repair lines 5 on the substrate 1 falls within the vertical projection of the data lines 3 on the substrate. The first repair lines 5 are configured to connect the two ends of the data lines 3 that are disconnected with vias when the vertical projection of the area where the data line 3 is disconnected falls within the vertical projection of the first repair line 5 in the longitudinal direction.

[051] It should be noted that when only forming the first repair lines 5 over the pixel electrode layer, each of the first repair lines 5 can be an integral wire, as shown in FIG. 1. Because the first repair lines 5 are

only formed in the pixel electrode layer, the fabrication process of this structure is relatively simple, but short circuits with a pixel electrode layer can easily occur at the time of repairing. Each of the first repair lines 5 can be divided into different segments according to different situations. However, because the first repair lines 5 are only formed in the pixel electrode layer, if each of the first repair lines 5 is divided into different segments, it is possible that there are no segments of the first repair lines 5 arranged at the disconnected area of the data line 3.

[052] FIG. 2 is a partial top view of the structure of the pixel electrodes 4 and the first repair lines 5 in the pixel electrode layer of the array substrate as shown in FIG. 1.

[053] FIG. 3 is a partial cross-sectional view of FIG. 1 at position AB, which illustrates a substrate 1, a first insulating layer 9, a data line 3, a second insulating layer 10, and a first repair line 5, wherein position of the first repair line 5 and position of the data line 3 correspond with each other.

[054] FIG. 4 is a partial cross-sectional view of FIG. 1 at position CD, illustrating a substrate 1, a gate line 2, a first insulating layer 9, a data line 3, a second insulating layer 10 and a first repair line 5, wherein position of the first repair line 5 and position of the data line 3 correspond to each other.

[055] The array substrate further comprises common electrode lines 13 and thin film transistor structures, as shown in FIG. 5, which is a partial cross sectional view of FIG. 1 at position EF. The thin film transistor (TFT) structure comprises a substrate 1, a gate line 2 (i.e. gate electrode, which is part of the gate line 2), a first insulating layer 9, an active layer 8, a source electrode 11, a drain electrode 12 and a second insulating layer 10.

[056] The beneficial effects of this embodiment are as follows: by configuring first repair lines 5 corresponding to data lines 3 in the pixel electrode layer, when open circuit occurs on a data line 3, the first repair

line 5 and the two ends of the disconnected data line 3 can be connected together by welding, such that the disconnected data lines 3 can be fixed without influencing the pixel electrodes 4 in peripheral pixels.

[057] Embodiment 2:

[058] Embodiment 2 is shown in FIGS. 6-8. In this embodiment, an array substrate comprises a second metal layer, a first metal layer, and a pixel electrode layer, sequentially formed over a substrate 1. The first metal layer comprises data lines 3; the second metal layer comprises gate lines 2; and the pixel electrode layer comprises pixel electrodes 4.

[059] The pixel electrode layer further comprises first repair lines 5, and the vertical projection of the first repair lines 5 on the substrate 1 falls within the vertical projection of the data lines 3 on the substrate 1, the first repair lines 5 are configured to connect the two ends of the disconnected data line 3 with vias when the vertical projection of the area of the disconnected data lines 3 falls within the vertical projection of the first repair lines 5 on the substrate 1 in the longitudinal direction.

[060] The array substrate further comprises a common electrode layer, disposed between the substrate 1 and the second metal layer. The common electrode layer comprises common electrodes 6 and second repair lines 7. The vertical projection of the second repair lines 7 on the substrate 1 falls within the vertical projection of the data lines 3 on the substrate 1; the common electrodes 6 and the second repair lines 7 are insulated from each other. Each of the second repair lines 7 can be an integral wire, and can have a structure similar to that of the first repair lines 5 as shown in FIG. 1. The description is not repeated herein.

[061] Because forming relatively long repair lines has a high requirement for the manufacturing process, and open circuits are easy to occur on relatively long repair lines, in some embodiments as shown in FIG. 7, a second repair line 7 can comprise a plurality of segments 71, wherein the segments 71 and the gate lines 2 are insulated from each other, the segments 71 are configured to connect the two ends of the disconnected

data lines 3 with vias when the vertical projection of the area of the disconnected data line 3 on the substrate 1 falls within the vertical projection of the second repair line segments 71 on the substrate 1 in the longitudinal direction, or it is configured to connect the ends of the disconnected data line 3 with vias when the vertical projection of the ends of the disconnected data line 3 on the substrate 1 falls within the vertical projection of the second repair line segments 71 on the substrate 1 in the longitudinal direction.

[062] It is noted that the second repair line 7 that comprises a plurality of second repair line segments 71 can be directly combined with the structure as shown in FIG. 1, i.e., the first repair lines 5 can each be an integral wire, and the second repair lines 7 each comprises a plurality of segments 71.

[063] However, in order to avoid short circuit at the time of repairing, preferably, as shown in FIG. 8, each of the first repair lines 5 can also comprise a plurality of first repair line segments 51, the vertical projections of each first repair line segment 51 and of each second repair line segment 71 corresponding to the same data line 3 on the substrate 1 are staggered and partially overlapped only at the ends. The first repair line segments 51 are configured to connect two ends of an open portion of a data line 3 with vias if the vertical projection of the open portion of the data line 3 on the substrate 1 falls within the vertical projection of one first repair line segment 51 on the substrate 1 in the longitudinal direction.

[064] FIG. 7 is a partial top view of the common electrodes 6 and the second repair line 7 in the common electrode layer, wherein the second repair line 7 comprises a plurality of the second repair line segments 71.

[065] FIG. 8 is a partial top view of the pixel electrodes 4 and the first repair lines 5 in the pixel electrode layer, wherein the first repair line 5 comprises a plurality of the first repair line segments 51.

[066] It should be noted that the second repair line segments 71 and the common electrode lines 13 should be insulated from each other.

[067] FIG. 9 is a partial cross-sectional view of FIG. 6 at position AB, wherein the array substrate comprises a substrate 1, a second repair line 7, a first insulating layer 9, a data line 3 and a second insulating layer 10, wherein the position of the second repair line 7 and the position of the data line 3 correspond to each other.

[068] FIG. 10 is a partial cross-sectional view of the FIG. 6 at position CD, wherein the array substrate comprises a substrate 1, a gate line 2, a first insulating layer 9, a data line 3, a second insulating layer 10, and a first repair line 5, wherein the position of the first repair line 5 and the position of the data line 3 correspond to each other. The array substrate as shown in FIG. 6 has the same thin film transistor structure as the array substrate as shown in FIG. 1, which is shown in FIG. 5, and will not be repeated herein.

[069] The beneficial effects of embodiments of the present disclosure are as follows:

[070] By arranging repair lines corresponding to data lines 3, and arranging first repair lines 5 corresponding to data lines 3, when open circuit occurs on a data line 3, the first repair line 5 and the two ends of the corresponding disconnected data line 3 can be connected together via welding directly without influencing the pixel electrode 4 in peripheral pixels.

[071] Furthermore, first repair lines 5 having segments 51 and second repair line 7 having segments 71 are configured such that each of the segments 51 of each first repair line 5 and each of the segments 71 of each second repair line 7 are staggered and partially overlapped at the ends of each first repair line segment 51 and each second repair line segment 71. When open circuit occurs on a data line 3, the first repair line segments 51 and the second repair line segments 71 and the two ends of the corresponding disconnected data line 3 can be connected together by welding directly so as to repair the disconnected data line 3 without influencing the pixel electrodes 4 in peripheral pixels. Configuration of

first repair lines 5 and second repair lines 7 is flexible, and it is not influenced by the configuration of wires such as gate lines 2 and common electrode lines 13.

[072] In another aspect, the present disclosure provides a display panel, comprising the array substrate according to the above-described embodiments. Furthermore, a display apparatus is provided, which comprises the display panel as described above.

[073] In yet another aspect, the present disclosure provides a method for repairing an array substrate according to Embodiment 1, comprising the following steps:

[074] If the vertical projection of an open portion of a data line on the substrate falls within the vertical projection of a first repair line on the substrate in the longitudinal direction, the two ends of the open portion of the data line can be re-connected with the first repair line with vias.

[075] The beneficial effects of the embodiments of the present disclosure are as follows: by forming repair lines corresponding to data lines over the pixel electrode layer, when open circuit occurs on a data line, the repair line and the two ends of the corresponding disconnected data line can be connected together by welding directly to repair the disconnected data line without influencing the pixel electrodes in peripheral pixels.

[076] The present disclosure further provides a method for repairing an array substrate according to Embodiment 2, comprising the following steps.

[077] As illustrated in FIG. 11, if the vertical projection of an open portion 100 of a data line on the substrate falls within the vertical projection of a segment 51 of a first repair line on the substrate in the longitudinal direction, the two ends of the open portion 100 of the data line can be re-connected with the segment 51 of the first repair line with two vias 200, wherein the two vias 200 can be configured on the segment 51 of the first repair line, at positions such that the vertical projection of the two vias

200 on the substrate respectively fall on two sides of the vertical projection of the open portion 100 of the data line on the substrate.

[078] Alternatively, if the vertical projection of an open portion 100 of a data line on the substrate falls within the vertical projection of a segment 71 of a second repair line on the substrate in the longitudinal direction, the two ends of the open portion 100 of the data line can be re-connected with the segment 71 of the second repair line with two vias 200, wherein the two vias 200 can be configured on the segment 71 of the second repair line, at positions such that the vertical projection of the two vias 200 on the substrate respectively fall on two sides of the vertical projection of the open portion 100 of the data line on the substrate (figure not shown).

[079] Alternatively, it is possible that the vertical projection of an open portion 100 of a data line on the substrate falls within an overlapping region 300 between the vertical projection of a segment 51 of a first repair line on the substrate and the vertical projection of a segment 71 of a second repair line on the substrate. Under this situation, the two ends of the open portion 100 of the data line can be re-connected either with the segment 51 of the first repair line with two vias 200, or with the segment 71 of the second repair line with two vias 200. In either of these two solutions, the two vias 200 can be configured at positions such that the vertical projection of the two vias 200 on the substrate respectively fall on two sides of the vertical projection of the open portion 100 of the data line on the substrate (figure not shown).

[080] The beneficial effects of the embodiments of the present disclosure are as follows: by configuring segmented first repair lines and segmented second repair lines over the common electrode layer and the pixel electrode layer respectively, and by configuring that each of the segments of the first repair line and each of the segments of the second repair line are staggered and partially overlapped at the ends, if open circuit occurs on a data line, the first repair line segments and the second repair line segments can be connected with the two ends of the disconnected data line via welding directly to repair the disconnected data line without

influencing the pixel electrodes in peripheral pixels.

[081] Although specific embodiments have been described above in detail, the description is merely for purposes of illustration. It should be appreciated, therefore, that many aspects described above are not intended as required or essential elements unless explicitly stated otherwise. Various modifications of, and equivalent acts corresponding to, the disclosed aspects of the exemplary embodiments, in addition to those described above, can be made by a person of ordinary skill in the art, having the benefit of the present disclosure, without departing from the spirit and scope of the disclosure defined in the following claims, the scope of which is to be accorded the broadest interpretation so as to encompass such modifications and equivalent structures.

CLAIMS

1. An array substrate, comprising:

a first metal layer, including a signal line;

a first repair layer; and

a first insulating layer disposed between, and provides insulation between, the first metal layer and the first repair layer;

wherein:

the first insulating layer is configured to be penetrable to allow the first repair layer to electrically connect the signal line to thereby repair connection weakness of the signal line.

2. The array substrate of Claim 1, wherein the first repair layer comprises a first repair line, disposed over and along the signal line, and configured to be able to electrically connect two ends of a weak connection portion of the signal line through vias penetrating the first insulating layer.

3. The array substrate of Claim 2, further comprising a substrate, wherein projection of the first repair line on the substrate overlaps with projection of the signal line on the substrate in a longitudinal direction.

4. The array substrate of Claim 3, wherein the signal line in the first metal layer comprises a data line.

5. The array substrate of Claim 4, wherein the first repair line is an integral wire.

6. The array substrate of Claim 4, wherein the first repair line comprises a plurality of first segments, electrically disconnected from one another.

7. The array substrate of Claim 6, further comprising: a second repair layer including a second repair line, wherein:

the second repair line is insulated from, and disposed over and along, the data line;

projection of the second repair line on the substrate overlaps with projection of the data line on the substrate in a longitudinal direction; and

the second repair line comprises a plurality of second segments, electrically disconnected from one another;

wherein:

the plurality of first segments of the first repair line and the plurality of second segments of the second repair line are configured such that at least one of one corresponding first segment of the first repair line or one corresponding second segment of the second repair line is able to electrically connect the two ends of the weak connection portion of the data line through one or more vias.

8. The array substrate of Claim 7, wherein each one of the plurality of first segments of the first repair line is staggered with, and partially overlapped at ends with, one of the plurality of second segments of the second repair line.

9. The array substrate of Claim 7 or Claim 8, wherein one of the first repair layer and the second repair layer is a pixel electrode layer, and another thereof is a common electrode layer.

10. The array substrate of Claim 9, wherein the first repair layer is a pixel electrode layer, and the second repair layer is a common electrode layer, wherein:

the pixel electrode layer comprises a plurality of pixel electrodes, insulated from the first repair line;

the common electrode layer comprises a plurality of common electrodes, insulated from the second repair line.

11. The array substrate of Claim 10, further comprising a second metal layer, the second metal layer comprising a plurality of gate lines, wherein:

the second repair layer, the second metal layer, the first metal layer, and the first repair layer are sequentially disposed on the substrate; and

the plurality of gate lines in the second metal layer are insulated from the second repair line in the second repair layer.

12. The array substrate of Claim 11, further comprising a second insulating layer,

wherein the second insulating layer is disposed between, and configured to insulate, the second metal layer and the first metal layer.

13. A display panel, comprising the array substrate of any one of Claims 1-12.

14. A display apparatus, comprising the display panel of Claim 13.

15. A method for repairing an array substrate according to Claim 1, the method comprising a step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line.

16. The method of Claim 15, wherein the step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line is performed by welding the first repair line with the two ends of the weak connection portion of the signal line through vias.

17. The method of Claim 15, wherein:

the first repair line comprises a plurality of first segments, electrically disconnected from one another; and

the step of connecting the two ends of the weak connection portion of the signal line with vias through the first repair line is performed by welding one of the plurality of first segments of the first repair line with the two ends of the weak connection portion of the signal line through vias.

18. A method for repairing an array substrate according to Claim 7, the method comprising: connecting the two ends of the weak connection portion of the data line with vias through at least one of one corresponding first segment of the first repair line or one corresponding second segment of the second repair line.

19. The method of Claim 18, wherein: if projection of the weak connection portion of the data line on the substrate falls within projection of one first segment of the first repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected by welding the one first segment of the first repair line with the two ends of the weak connection portion of the data line with two vias.

20. The method of Claim 18, wherein: if projection of the weak connection portion of the data line on the substrate falls within projection of one second segment of the second repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected by welding the one second segment of the second repair line with the two ends of the weak connection portion of the data line with two vias.

21. The method of Claim 18, wherein: if projection of the weak connection portion of the data line on the substrate falls within an overlapping region between projection of one first segment of the first repair line on the substrate and projection of one second segment of the second repair line on the substrate, the two ends of the weak connection portion of the data line are electrically connected:

by welding the one first segment of the first repair line with the two ends of the weak connection portion of the data line with two vias; or

by welding the one second segment of the second repair line with the two ends of the weak connection portion of the data line with two vias.

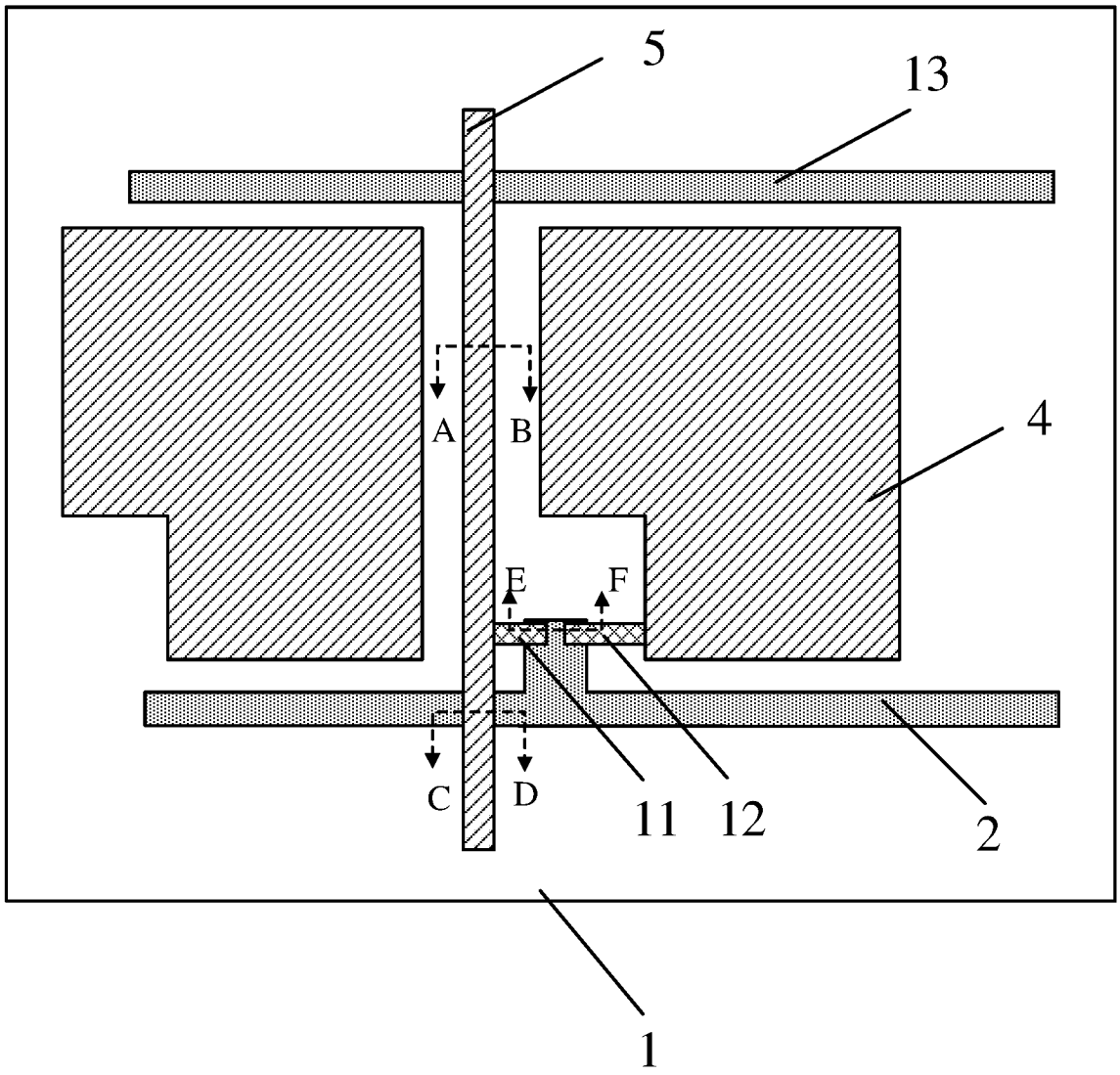

FIG. 1

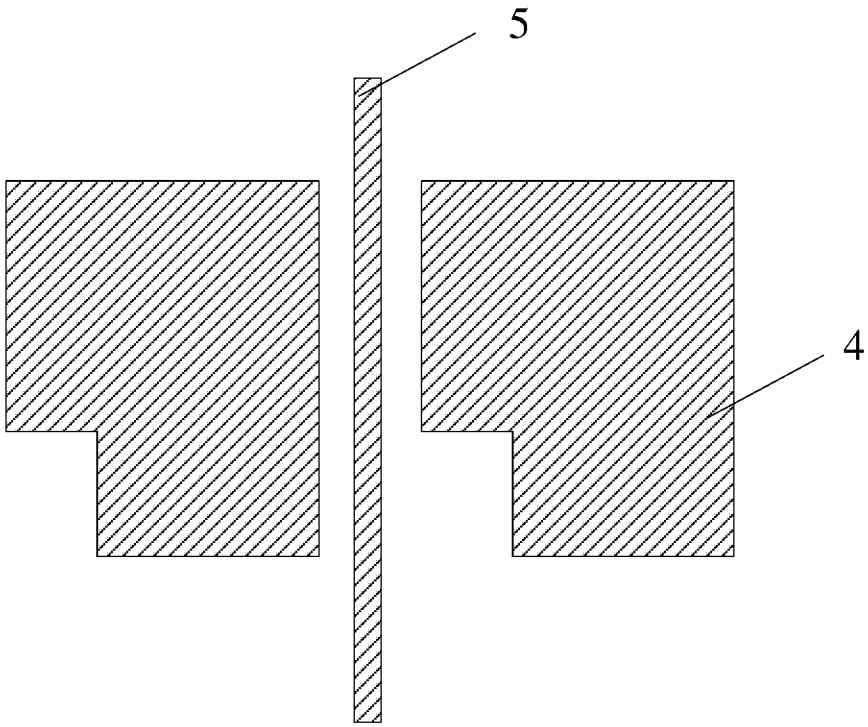

FIG. 2

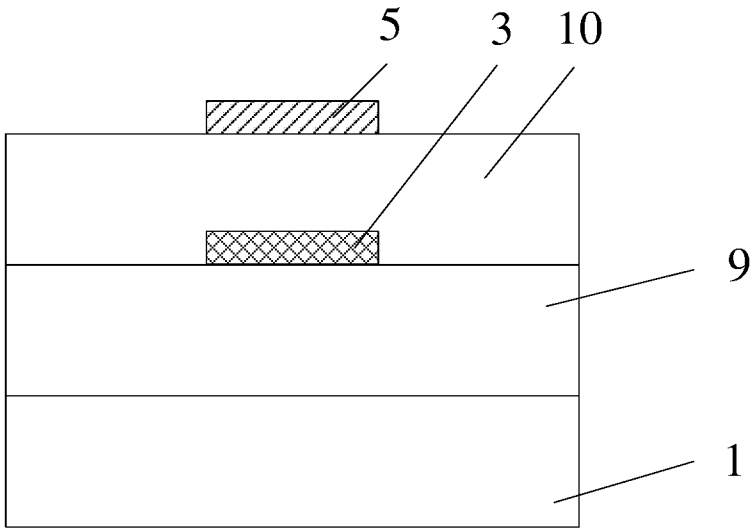

FIG. 3

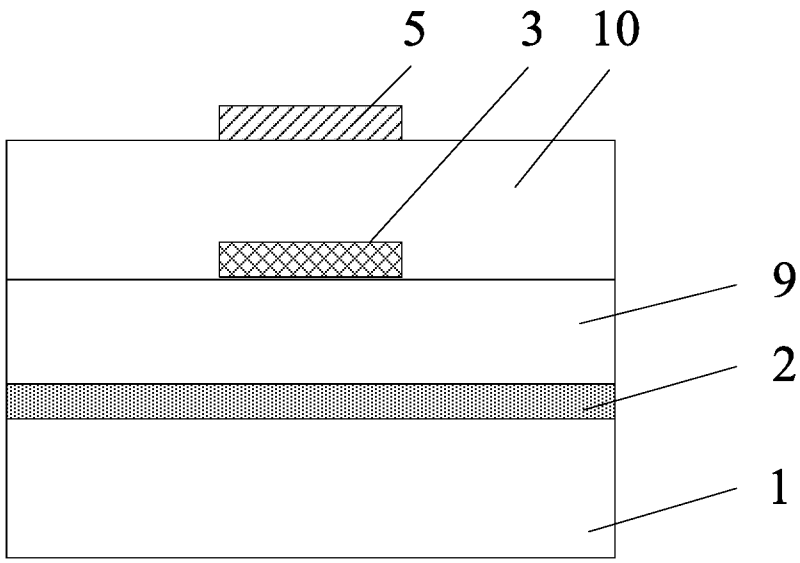

FIG. 4

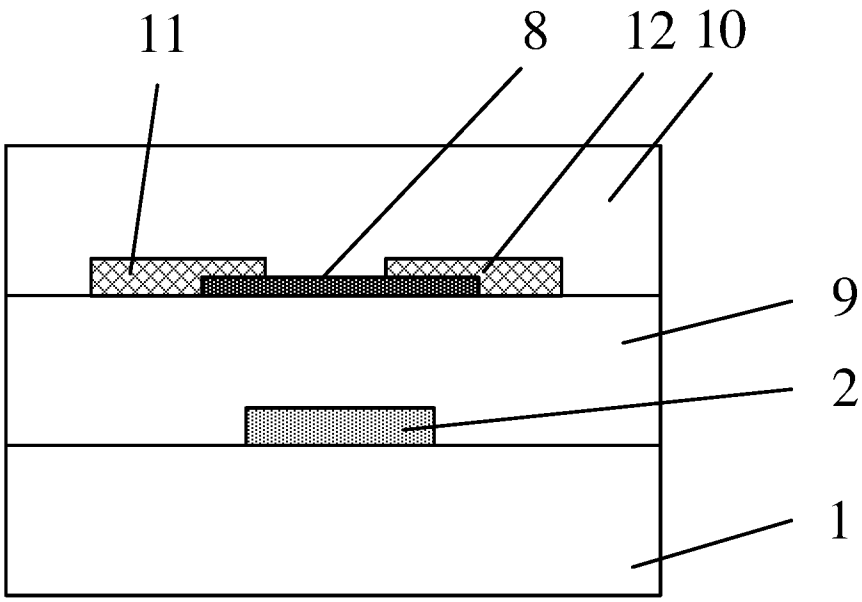

FIG. 5

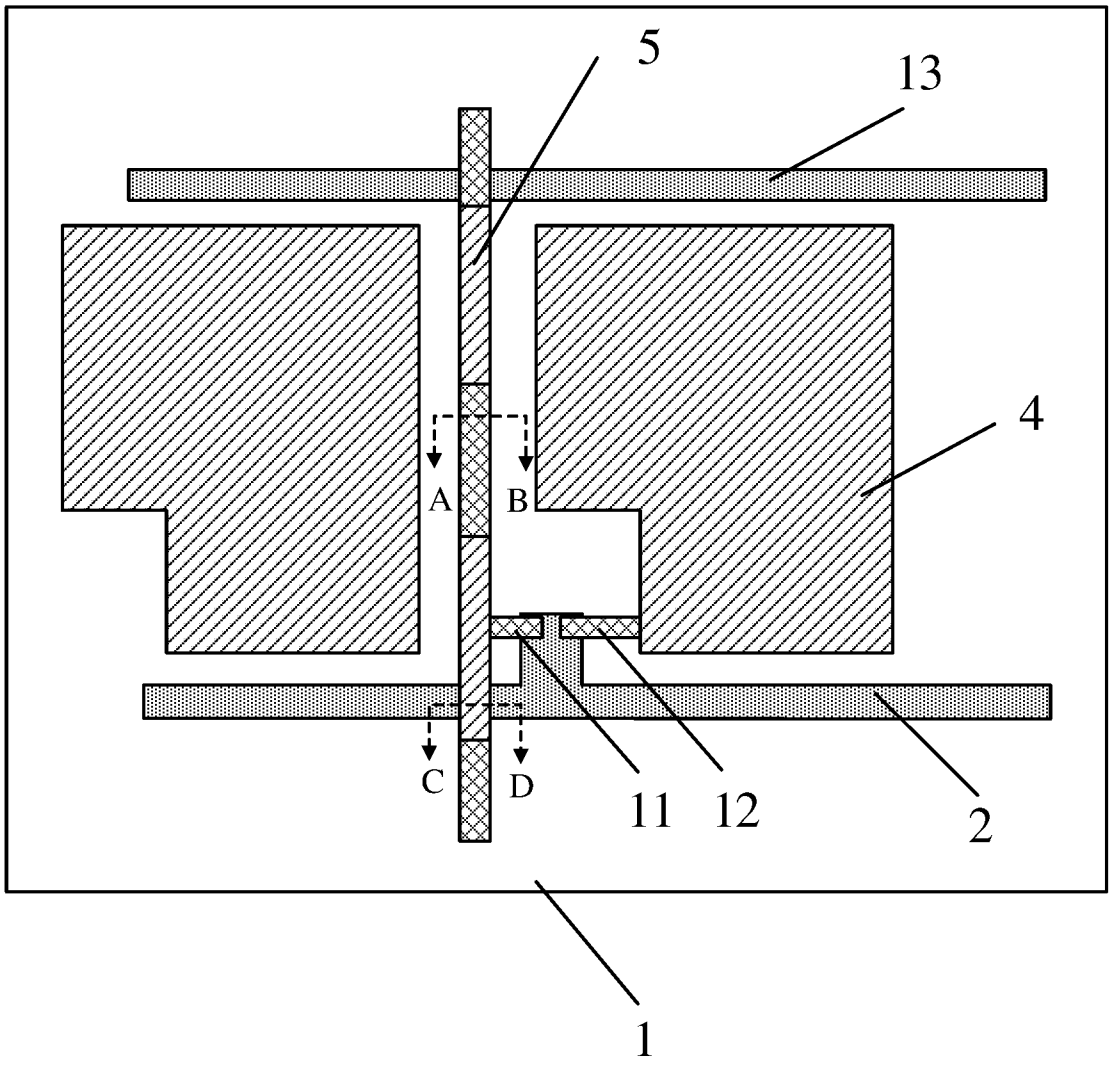

FIG. 6

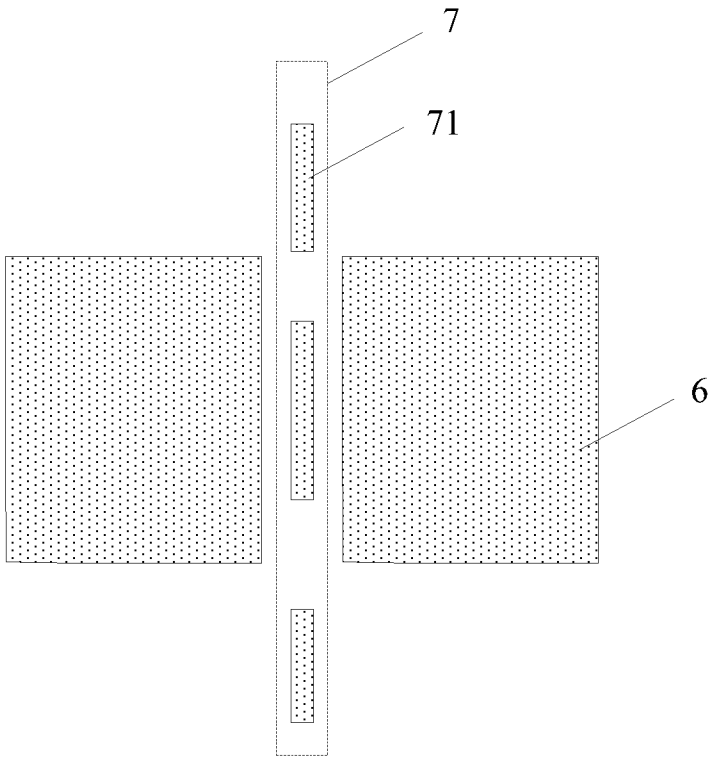

FIG. 7

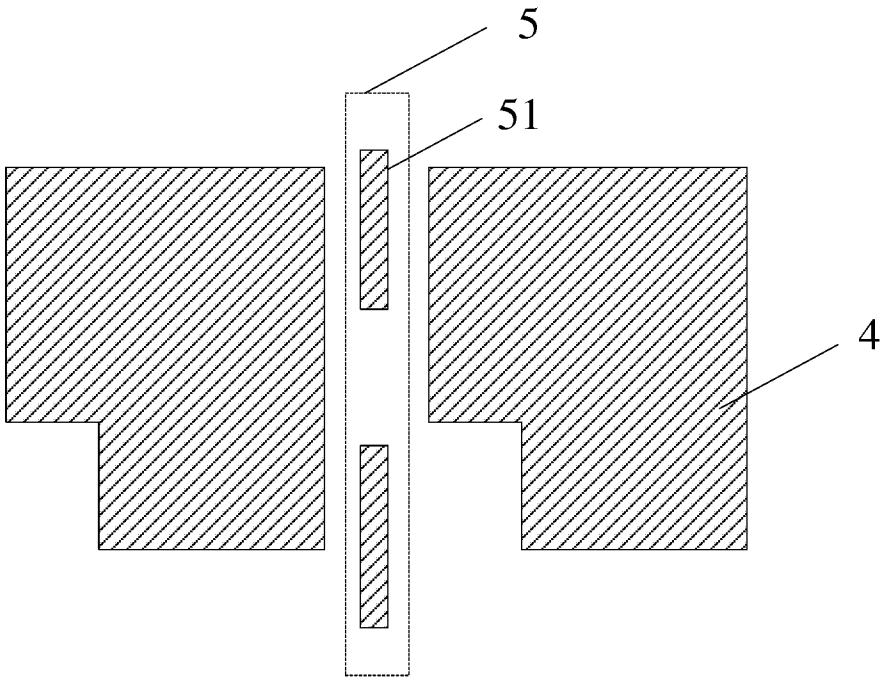

FIG. 8

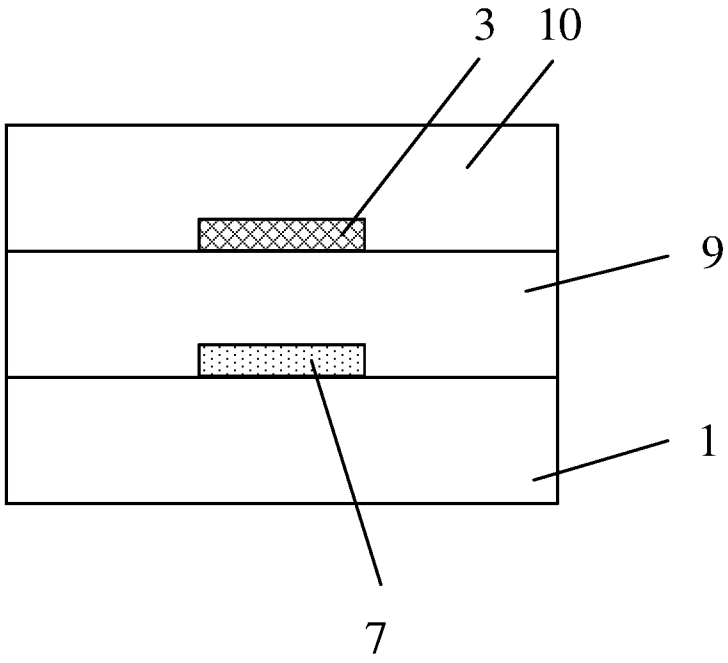

FIG. 9

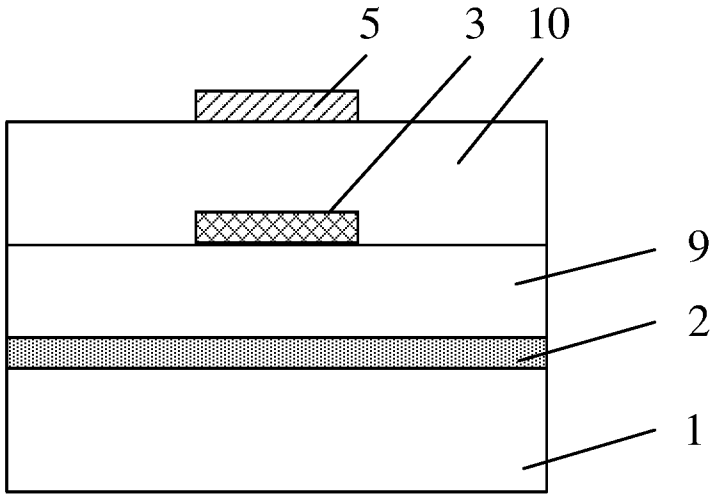

FIG. 10

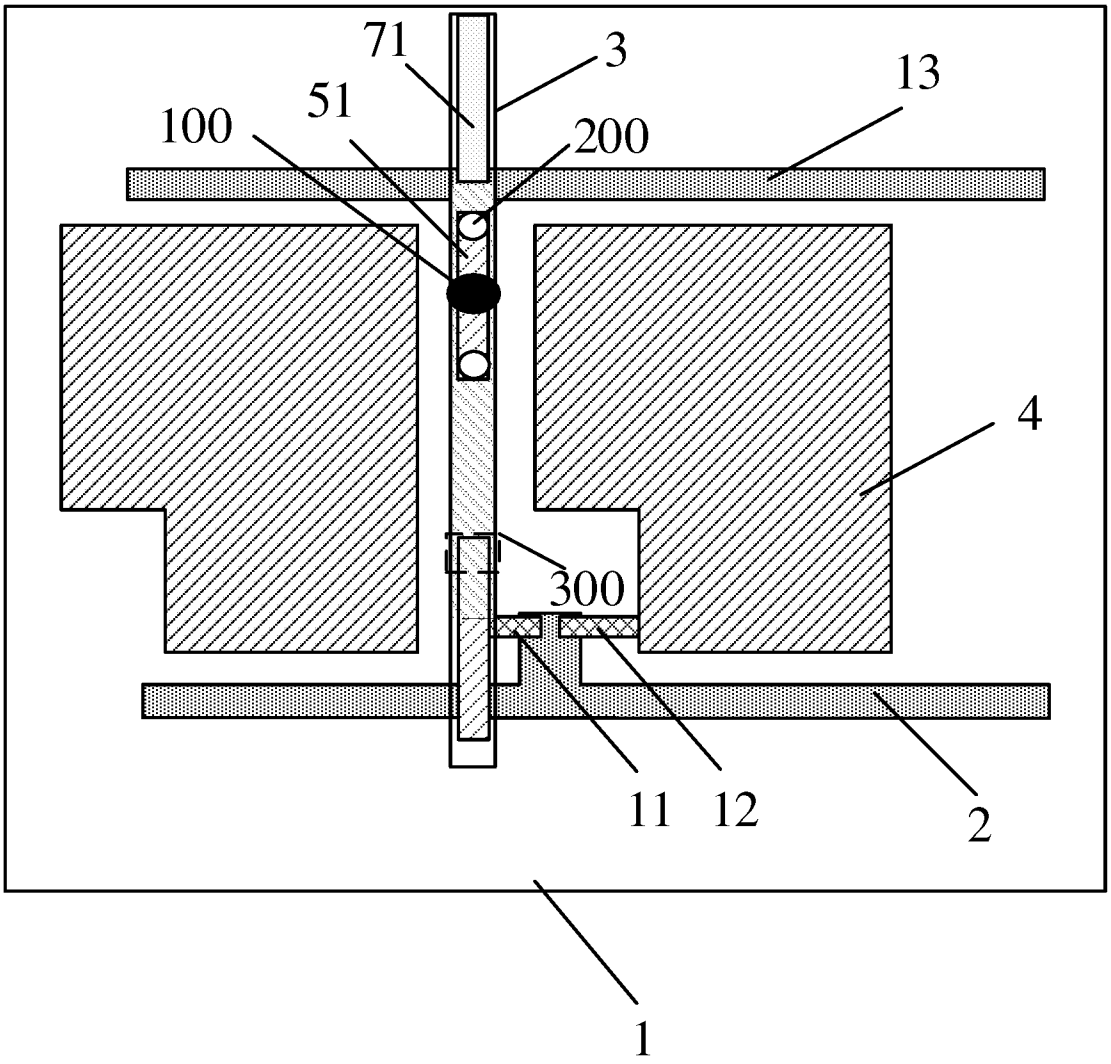

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/088173

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/13(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F 1/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: BOE, array, substrate, data, signal, line, repair+, weak, open+, overlap+, penetrat+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 105527736 A (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 27 April 2016 (2016-04-27) description paragraphs 39-60, figures 1-10	1-21
X	CN 1359020 A (HITACHI LTD.) 17 July 2002 (2002-07-17) description pages 3-8, figures 1-8	1-21
X	CN 104932128 A (HEFEI XINSHENG OPTOELECTRONIC TECHNOLOGY CO., LTD. ET AL.) 23 September 2015 (2015-09-23) description paragraphs 5-35、48-112, figures 4-7	1-21
X	CN 1877399 A (QUANTA DISPLAY INC.) 13 December 2006 (2006-12-13) description pages 5-9, figures 2-6	1-21
X	US 2006176415 A1 (ADVANCED DISPLAY INC.) 10 August 2006 (2006-08-10) description paragraphs 5-64, figures 2-11	1-21
A	CN 101114655 A (SHANGHAI GUANGDIAN PHOTOELECTRON CO., LTD.) 30 January 2008 (2008-01-30) the whole document	1-21

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2016	**15 November 2016**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**WANG,Jianliang**
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/088173

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				US	7042532	B2	09 May 2006
				JP	2004054069	A	19 February 2004
				US	2006012728	A1	19 January 2006
				US	6958802	B2	25 October 2005
				TW	200403508	A	01 March 2004
				KR	100750548	B1	20 August 2007
				US	7515243	B2	07 April 2009
				TW	I241446	B	11 October 2005
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