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(54) **Title**: PROTECTION OF STORED DATA USING OPTICAL EMITTING ELEMENTS

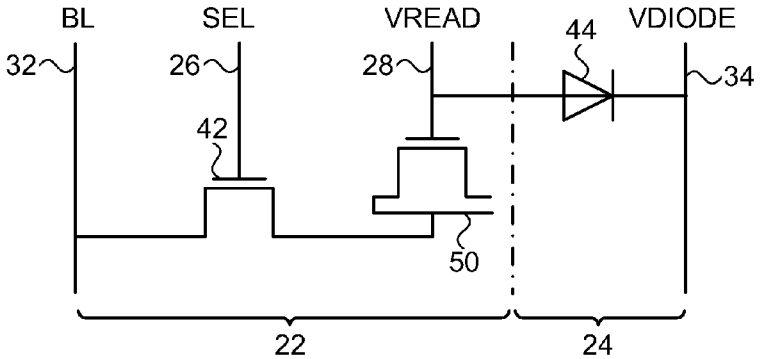

FIG. 2B

(57) **Abstract**: An integrated circuit device (20, 60) includes a plurality of memory cells (22), which are configured to store data. Multiple P-N junctions (24) are arranged so that a single, respective P-N junction is disposed in proximity to each memory cell and is configured to emit optical radiation during readout from the memory cell with a wavelength matching an emission wavelength of the memory cell.

WO 2012/117311 A1

PROTECTION OF STORED DATA USING OPTICAL EMITTING ELEMENTS

FIELD OF THE INVENTION

The present invention relates generally to electronic devices, and specifically to methods and circuits for prevention of unauthorized data readout from such devices.

BACKGROUND OF THE INVENTION

In some integrated circuits, such as non-volatile memory, readout of data from a memory cell can cause emission of infrared light. Although low in power, such emissions can be detected, particularly if integrated over time while the circuit is in operation. Given sensitive equipment and enough time, it may be possible to use these emissions in order to extract the information that is stored in the cell.

U.S. Patent Application Publication 2010/0213878 describes a method and apparatus for reducing optical emissions in an integrated circuit. The integrated circuit is provided with first circuitry having first and second transistors that emit light during a change in state between states of low and high resistance and second circuitry having third transistors that emit light during a change in state. The third transistors are disposed near at least one of the first and second transistors so that light emissions from the third transistors hinder optical detection of a pattern of light emitted by the first and second transistors.

U.S. Patent 7,962,767 describes an integrated circuit having first and second circuitry which are configured to emit light when undergoing changes in state. The first and second circuitry are operated to change state at the same time so as to hinder optical detection of the light emitted by the first circuitry.

Various types of one-time programmable memory cells are known in the art. For example, U.S. Patent 6,777,757 describes a programmable memory cell comprising a transistor located at the crosspoint of a column bitline and a row wordline. The

transistor has its gate formed from the column bitline and its source connected to the row wordline. The memory cell is programmed by applying a voltage potential between the column bitline and the row wordline to produce a programmed n+ region in the substrate underlying the gate of the transistor.

As another example, U.S. Patent 7,511,982 describes a high-speed sensing scheme for a non-volatile memory array. The memory array includes non-volatile memory cells arranged in a complementary bitline configuration, precharge circuits for precharging the bitlines to a first voltage level such as VSS, a reference circuit for applying a reference charge on the reference bitlines of the complementary bitline pairs, and bitline sense amplifiers for sensing a voltage differential between the complementary bitline pairs. A voltage on the data bitline is changed when a programmed non-volatile memory cell connected to an activated wordline couples the wordline voltage to the data bitline.

U.S. Patent 7,812,420 describes a polydiode structure for a photodiode. An integrated circuit device for converting an incident optical signal into an electrical signal comprises a semiconductor substrate, a well region formed inside the semiconductor substrate, a dielectric layer formed over the well region, and a layer of polysilicon for receiving the incident optical signal, formed over the dielectric layer, including a p-type portion, an n-type portion and an undoped portion disposed between the p-type and n-type portions. The well region is biased to control the layer of polysilicon for providing the electrical signal.

SUMMARY

Embodiments of the present invention that are described hereinbelow provide methods and circuits for creating optical emissions from a point in proximity to a memory cell, and

thereby frustrate attempts to extract the data stored in the cell.

There is therefore provided, in accordance with an embodiment of the present invention, an integrated circuit device, including a plurality of memory cells, which are configured to store data. Multiple P-N junctions are arranged so that a single, respective P-N junction is disposed in proximity to each memory cell and is configured to emit optical radiation during readout from the memory cell with a wavelength matching an emission wavelength of the memory cell.

In certain embodiments, the memory cells may include anti-fuse cells, fuse cells, floating gate cells, or read-only memory (ROM) cells.

In a disclosed embodiment, each memory cell includes a circuit element that emits during readout from the cell, and the respective P-N junction is located at a distance no greater than 0.5 μm from the circuit element.

In some embodiments, the P-N junctions are configured as diodes, such as poly-silicon diodes, which are biased to emit the optical radiation. Typically, each diode is coupled to a respective memory cell so as to receive a forward bias and emit the optical radiation when the respective memory cell is read out. The device may include a readout power line, for supplying a voltage to the memory cells during readout, and a diode power line, wherein each diode is coupled between the readout power line to the respective memory cell and the diode power line. The P-N junctions may be biased at a level that is selected so as to cause the P-N junctions to emit the optical radiation with a wavelength and brightness matching an emission of the memory cells.

In one embodiment, the P-N junctions are coupled to the memory cells so that each P-N junction emits the optical

radiation only during readout from the memory cell in proximity to which the P-N junction is disposed. Alternatively, the P-N junctions may be coupled to the memory cells so that multiple P-N junctions emit the optical radiation during readout from one or more of the memory cells. Further alternatively, the P-N junctions may be driven to emit the optical radiation continuously while the device receives electrical power.

In a disclosed embodiment, the memory cells have a given area and are produced using a set of photolithographic masks, and the P-N junctions are contained within the given area and produced using the same set of photolithographic masks.

There is also provided, in accordance with an embodiment of the present invention, a method for producing an integrated circuit device. The method includes arranging a plurality of memory cells to store data in the device. Multiple P-N junctions are arranged in the device so that a single, respective P-N junction is disposed in proximity to each memory cell and is configured to emit optical radiation during readout from the memory cell with a wavelength matching an emission wavelength of the memory cell.

The present invention will be more fully understood from the following detailed description of the embodiments thereof, taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic layout of a part of an integrated circuit, in accordance with an embodiment of the present invention;

Figs. 2A and 2B are schematic circuit diagrams showing a memory cell with an associated optical emission unit, in accordance with embodiments of the present invention; and

Fig. 3 is a schematic layout of an array of memory cells and emission units in an integrated circuit, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Some integrated circuit devices store sensitive data, such as encryption keys, in non-volatile memory (NVM), which may comprise, for example, an array of one-time programmable (OTP) memory cells or read-only memory (ROM) cells of other types. As noted earlier, readout from such cells may inherently cause the cells to emit optical radiation. The near-infrared (IR) portion of the emission passes through the silicon substrate and can be sensed from the back side of the memory chip. The emission from any given cell varies depending upon the bit content of the cell. Measuring these emissions may therefore give an indication of the data stored in the memory and may thus enable unauthorized parties to access the data, notwithstanding electronic data protection measures that are implemented in the device.

Sensitive optical instruments are capable, given sufficient measurement time, of detecting the sort of weak radiation that is emitted by the memory cells. Advanced instruments of this sort have sufficient spatial resolution to distinguish between emissions from different cells on the same integrated circuit device and from other emitting elements in the device. There are physical limits, however, on the ultimate resolution of such instruments. In the near-IR range, around 1 μm, for example, where silicon junctions emit radiation, the finest achievable resolution is in the range of 0.25 μm.

Embodiments of the present invention that are described hereinbelow address these issues by arranging P-N junctions to emit optical radiation in proximity to a set of memory cells, and specifically in proximity to the point from which these

memory cells emit radiation. The P-N junctions thus "dazzle" detectors that may be used in attempts to detect the optical radiation that is emitted from the memory cells. (The term "optical radiation," as used in the context of the present patent application and in the claims, includes visible, infrared and ultraviolet radiation.)

In the disclosed embodiments, a single, respective P-N junction is disposed adjacent to each memory cell and emits optical radiation during readout from the memory cell, at approximately the same wavelength as the memory cell itself. The distance between any given memory cell and the respective P-N junction may be, for example, no more than 0.25 μm, in the range of the resolution limit of measurement devices. Alternatively, larger separation between the memory cell and the P-N junction is possible, such as 0.5 μm, although in such designs it is desirable that the P-N junction be designed for relatively brighter emission. As a result of the emission from the P-N junction, the emission from the cell upon readout will be indistinguishable from the emission from the P-N junction, thereby frustrating attempts to optically read out the data stored in the memory.

In some embodiments, the P-N junctions are configured as diodes, which are biased to emit the optical radiation. The bias level (i.e., the voltage and direction - forward or backward) may be selected to give the appropriate emission wavelength and brightness to match the emission wavelength of the memory cell and mask the emission from the memory cell. Poly-silicon diodes are particularly advantageous in this regard because of their small size and bright radiation output. Each diode is coupled to its respective memory cell so as to receive a forward bias and emit the optical radiation when the respective memory cell is read out. Specifically, the diodes

may be coupled between the readout power line of the memory cells (which may be fixed or switched) and a dedicated diode power line. The diodes may be coupled to the memory cells in this manner so that each diode emits optical radiation only during readout from the memory cell in proximity to which the diode is disposed.

In alternative embodiments, the P-N junctions may be coupled to the memory cells so that multiple P-N junctions emit optical radiation during readout from one or more of the memory cells. As yet another alternative, the P-N junctions may be driven to emit the optical radiation continuously while the device receives electrical power. Still a further alternative is to drive the P-N junctions to emit radiation during only a part of the readout time or Page: 7 only during certain readouts and not others. For example, some or all of the P-N junctions can be driven to emit radiation only on every odd read count. In all of these alternative embodiments, the P-N junctions emit optical radiation during readout from the memory cells, but simply with different timing properties.

The embodiments that are shown in the figures and are described hereinbelow relate specifically to devices in which diodes are used as optical emitters in conjunction with OTP anti-fuse cells. The principles of the present invention, however, may equally be applied in protecting the contents of OTP fuse cells, as well as other types of NVM, such as floating gate and ROM cells. Furthermore, although the diodes shown in these embodiments are coupled to the readout power lines of the respective memory cells, the P-N junctions that are used to emit dazzling radiation may be powered and controlled separately from the memory cells.

Reference is now made to Figs. 1, 2A and 2B, which schematically illustrate a part of an integrated circuit 20, in accordance with an embodiment of the present invention. The integrated circuit comprises memory cells 22 along with emission units 24. Fig. 1 is a top view of the actual circuit layout on a silicon substrate 21, including two cells 22 (in this case anti-fuse OTP cells) and two emission units 24. Figs. 2A and 2B are schematic circuit diagrams showing the electrical connections within and between a single cell 22 and emission unit 24. In Fig. 2, cell 22 contains a generic non-volatile memory component 40, while Figs. 1 and 3 specifically show an example of OTP anti-fuse cells with an anti-fusePage: 8 device 50 based on a CMOS capacitor.

As shown in Fig. 1, two cells 22 are formed back-to-back on silicon substrate 21, which is N-doped in the region of cells 22. (All poly-silicon lines in region 22 are N-doped, as well.) Each cell 22 holds one bit of data. Typically, multiple cells 22 of this types and structure are formed in an array on substrate 21, but only these two cells are shown in Fig. 1 for the sake of simplicity. This particular cell design is shown here by way of example, and emission units 24 may similarly be integrated with other cell designs, such as those described in the patents cited above in the Background section.

One emission unit 24 is formed adjacent to each cell 22. A poly-silicon extension 46 in the region of unit 24 is P-doped on one side and N-doped on the other side, thus creating a P-N junction 44. It can be seen in the figure that the use of this sort of P-N junctions as emitters requires little or no increase the overall integrated circuit area. In fact, the design of emission units 24 that is shown in Fig. 1 does not increase the cell area at all and requires no additional photolithographic

masks for fabrication of the emission units beyond those already used to produce cell 22.

Anti-fuse devices 50 in cells 22 are formed over an active area 30 of the cells. (Poly-silicon lines above this area form the transistors in the cells.) The bit stored in each device 50 is read out by switching a select transistor 42, under control of a select line 26, with power supplied via a VPP/VREAD line 28. Transistor 42 passes the bit values to a bit line 32. During readout, device 50 emits infrared radiation, particularly in the vicinity of its outer edge (at the top and bottom of active area 30 in Fig. 1).

In emission unit 24, poly-line extension 46 connects P-N junction 44 to VPP/VREAD line 28. The other side of junction 44 is connected to a VDIODE line 34 made from poly-silicon. The VDIODE line serves as a variable power supply for junction 44, forming a diode. VDIODE may be held at any suitable voltage (including ground) that gives a forward bias across junction 44 during readout of cell 22. To form the P-N junction diode on poly-line extension 46, the poly-silicide above the area of junction 44 is removed within a rectangular window 36.

It can be seen in Fig. 1 that P-N junction 44 is adjacent and in close proximity to anti-fuse device 50. In the pictured embodiment, the distance between junction 44 and device 50 is less than 0.25 μm, which is below the spatial resolution of available infrared detectors, as noted above. Thus, whenever cell 26 is selected for read by select line 26, junction 44 will be driven to emit radiation, which will dazzle the detector and render any simultaneous radiation from device 50 undetectable. The use of a single P-N junction as the dazzling element is advantageous in this regard in terms of its small size and high brightness. Alternatively, larger or smaller distances and

other emitting configurations may be used depending on application requirements and available detection technologies.

Fig. 3 is a schematic layout of an array 60 of memory cells 22 and emission units 24 in an integrated circuit, in accordance with an embodiment of the present invention. The memory cells and emission units are similar to those shown above in Fig. 1. They are arranged in the embodiment of Fig. 3 in multiple rows 62 and columns 64. Array 60 has a given area and is produced using a set of photolithographic masks. Emission units 24 are contained within this same area and may be produced using the same set of photolithographic masks.

Although the embodiment described above relates to an anti-fuse cell formed on an N-doped substrate, in other embodiments the anti-fuse cell may be formed on a P-doped substrate. In this case, the doping of the emission unit is reversed as well (whereby the direction of the N-P junction is also reversed).

Furthermore, although emission units 24 in the embodiments shown above are driven to emit radiation directly by the circuitry of the corresponding cells 22 to which they are adjacent, other driving configurations may alternatively be used and are considered to be within the scope of the present invention. For example, when cells 22 are arranged in rows on substrate 21, with emission units 24 in corresponding rows alongside them, all the emission units in a given row may be activated whenever any of the cells in the row are read out. As another example, the circuits used to drive the emission units may be separate from those of the memory cells and controlled by external logic, rather than tied directly to the VPP/VREAD lines of the memory cells. Other geometrical arrangements of the emission units and memory cells may also be used, such as arrangements in which a single emission unit in proximity to one memory cell is sufficiently close to one or more other memory

cells to dazzle detectors attempting to measure radiation from the other cells, as well.

It will thus be appreciated that the embodiments described above are cited by way of example, and that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and subcombinations of the various features described hereinabove, as well as variations and modifications thereof which would occur to persons skilled in the art upon reading the foregoing description and which are not disclosed in the prior art.

CLAIMS

1. An integrated circuit device, comprising:

a plurality of memory cells, which are configured to store data; and

multiple P-N junctions, which are arranged so that a single, respective P-N junction is disposed in proximity to each memory cell and is configured to emit optical radiation during readout from the memory cell with a wavelength matching an emission wavelength of the memory cell.

2. The device according to claim 1, wherein the memory cells comprise anti-fuse cells.

3. The device according to claim 1, wherein the memory cells comprise fuse cells.

4. The device according to claim 1, wherein the memory cells comprise floating gate cells.

5. The device according to claim 1, wherein the memory cells comprise read-only memory (ROM) cells.

6. The device according to any of claims 1-5, wherein each memory cell comprises a circuit element that emits during readout from the cell, and wherein the respective P-N junction is located at a distance no greater than 0.5 μm from the circuit element.

7. The device according to any of claims 1-6, wherein the P-N junctions are configured as diodes, which are biased to emit the optical radiation.

8. The device according to claim 7, wherein the diodes are poly-silicon diodes.

9. The device according to claim 7 or 8, wherein each diode is coupled to a respective memory cell so as to receive a bias and

emit the optical radiation when the respective memory cell is read out.

10. The device according to claim 9, and comprising a readout power line, for supplying a voltage to the memory cells during readout, and a diode power line, wherein each diode is coupled between the readout power line to the respective memory cell and the diode power line.

11. The device according to any of claims 7-10, wherein the P-N junctions are biased at a level that is selected so as to cause the P-N junctions to emit the optical radiation with the wavelength and a brightness matching an emission of the memory cells.

12. The device according to any of claims 1-11, wherein the P-N junctions are coupled to the memory cells so that each P-N junction emits the optical radiation only during readout from the memory cell in proximity to which the P-N junction is disposed.

13. The device according to any of claims 1-11, wherein the P-N junctions are coupled to the memory cells so that multiple P-N junctions emit the optical radiation during readout from one or more of the memory cells.

14. The device according to any of claims 1-11, wherein the P-N junctions are driven to emit the optical radiation continuously while the device receives electrical power.

15. The device according to any of claims 1-14, wherein the memory cells are arranged in an array having a given area and are produced using a set of photolithographic masks, and wherein the P-N junctions are contained within the given area and produced using the same set of photolithographic masks.

16. A method for producing an integrated circuit device, the method comprising:

arranging a plurality of memory cells to store data in the device; and

arranging multiple P-N junctions in the device so that a single, respective P-N junction is disposed in proximity to each memory cell and is configured to emit optical radiation during readout from the memory cell with a wavelength matching an emission wavelength of the memory cell.

17. The method according to claim 16, wherein the memory cells comprise anti-fuse cells.

18. The method according to claim 16, wherein the memory cells comprise fuse cells.

19. The method according to claim 16, wherein the memory cells comprise floating gate cells.

20. The method according to claim 16, wherein the memory cells comprise read-only memory (ROM) cells.

21. The method according to any of claims 16-20, wherein each memory cell comprises a respective circuit element that emits during readout from the cell, and wherein arranging the second plurality of the P-N junctions comprises locating each P-N junction at a distance no greater than 0.5 μm from the respective circuit element.

22. The method according to any of claims 16-21, wherein arranging the second plurality of the P-N junctions comprises configuring the P-N junctions as diodes, which are biased to emit the optical radiation.

23. The method according to claim 22, wherein the diodes are poly-silicon diodes.

24. The method according to claim 22 or 23, wherein arranging the second plurality of the P-N junctions comprises coupling each diode to a respective memory cell so as to receive a bias and emit the optical radiation when the respective memory cell is read out.

25. The method according to claim 24, and comprising coupling a readout power line to supply a voltage to the memory cells during readout, and coupling each diode between the readout power line to the respective memory cell and a diode power line.

26. The method according to any of claims 22-25, wherein configuring the P-N junctions comprises biasing the P-N junctions at a level that is selected so as to cause the P-N junctions to emit the optical radiation with the wavelength and brightness matching an emission of the memory cells.

27. The method according to any of claims 16-26, wherein arranging the second plurality of the P-N junctions comprises coupling the P-N junctions to the memory cells so that each P-N junction emits the optical radiation only during readout from the memory cell in proximity to which the P-N junction is disposed.

28. The method according to any of claims 16-26, wherein arranging the second plurality of the P-N junctions comprises coupling the P-N junctions to the memory cells so that multiple P-N junctions emit the optical radiation during readout from one or more of the memory cells.

29. The method according to any of claims 16-26, wherein arranging the second plurality of the P-N junctions comprises driving the P-N junctions to emit the optical radiation continuously while the device receives electrical power.

30. The method according to any of claims 16-29, wherein the memory cells have a given area and are produced using a set of

photolithographic masks, and wherein arranging the second plurality of the P-N junctions comprises fabricating the device so that the P-N junctions are contained within the given area and produced using the same set of photolithographic masks.

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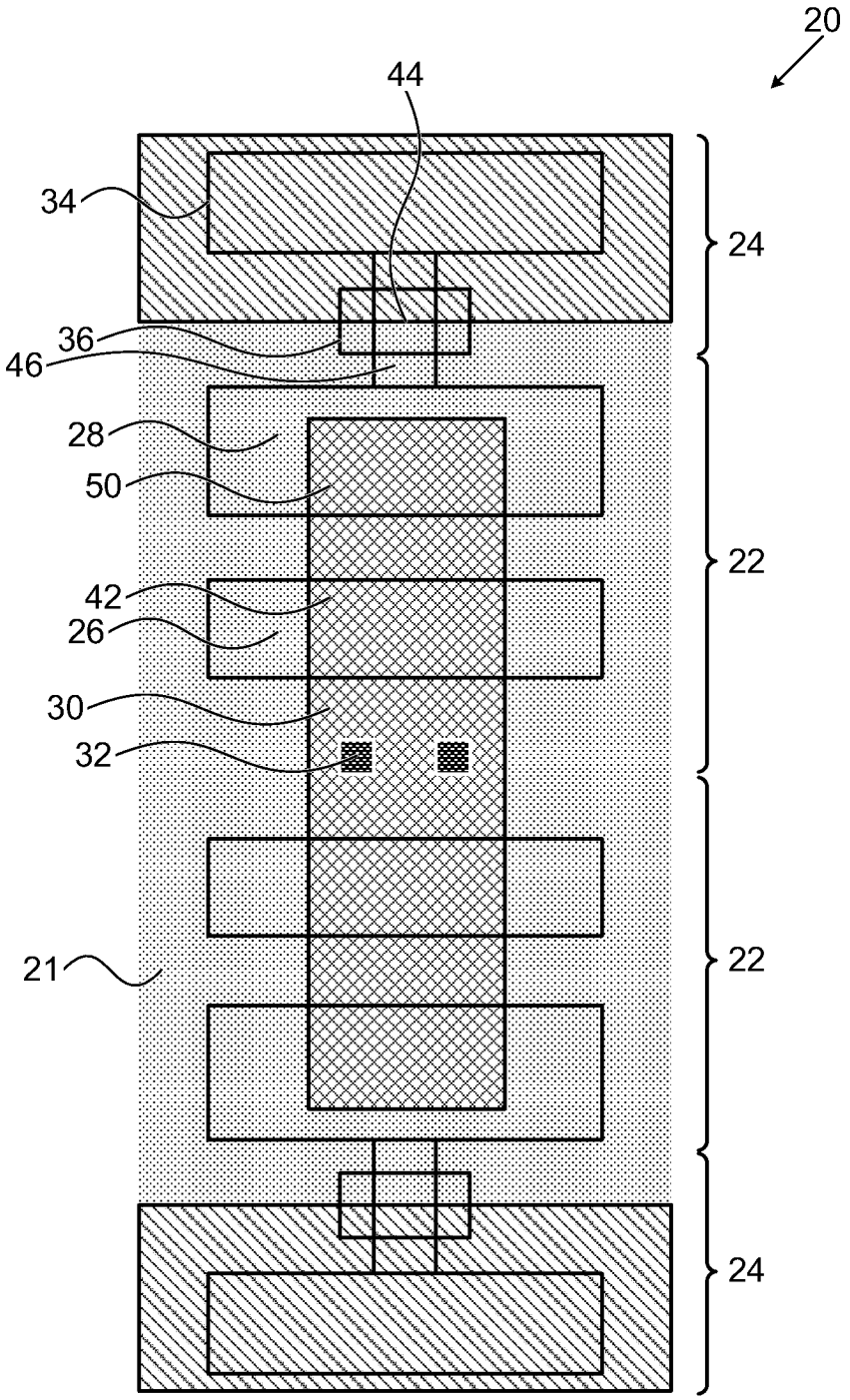

FIG. 1

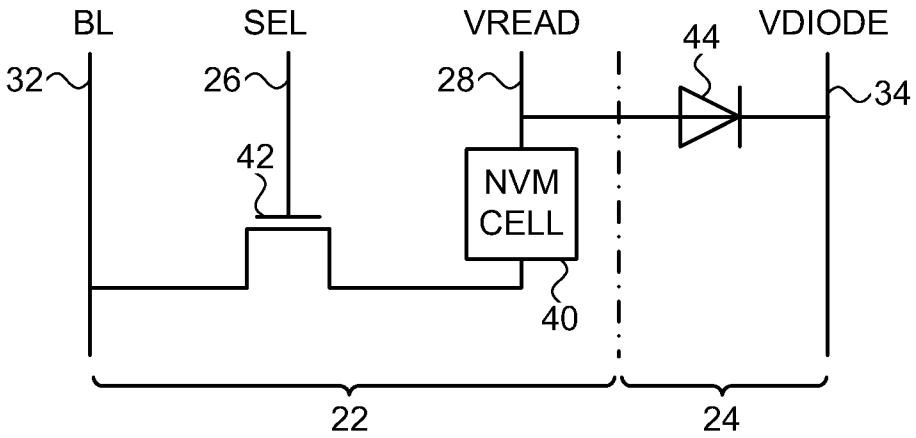
BL
SEL
VREAD
44
VDIODE
32
26
28
34
42
NVM
CELL
40
22
24

FIG. 2A

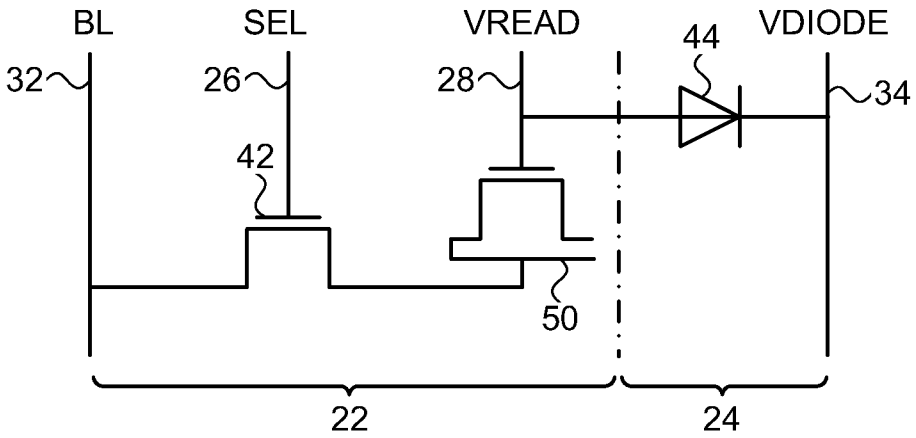
BL
SEL
VREAD
44
VDIODE
32
26
28
34
42
50
22
24

FIG. 2B

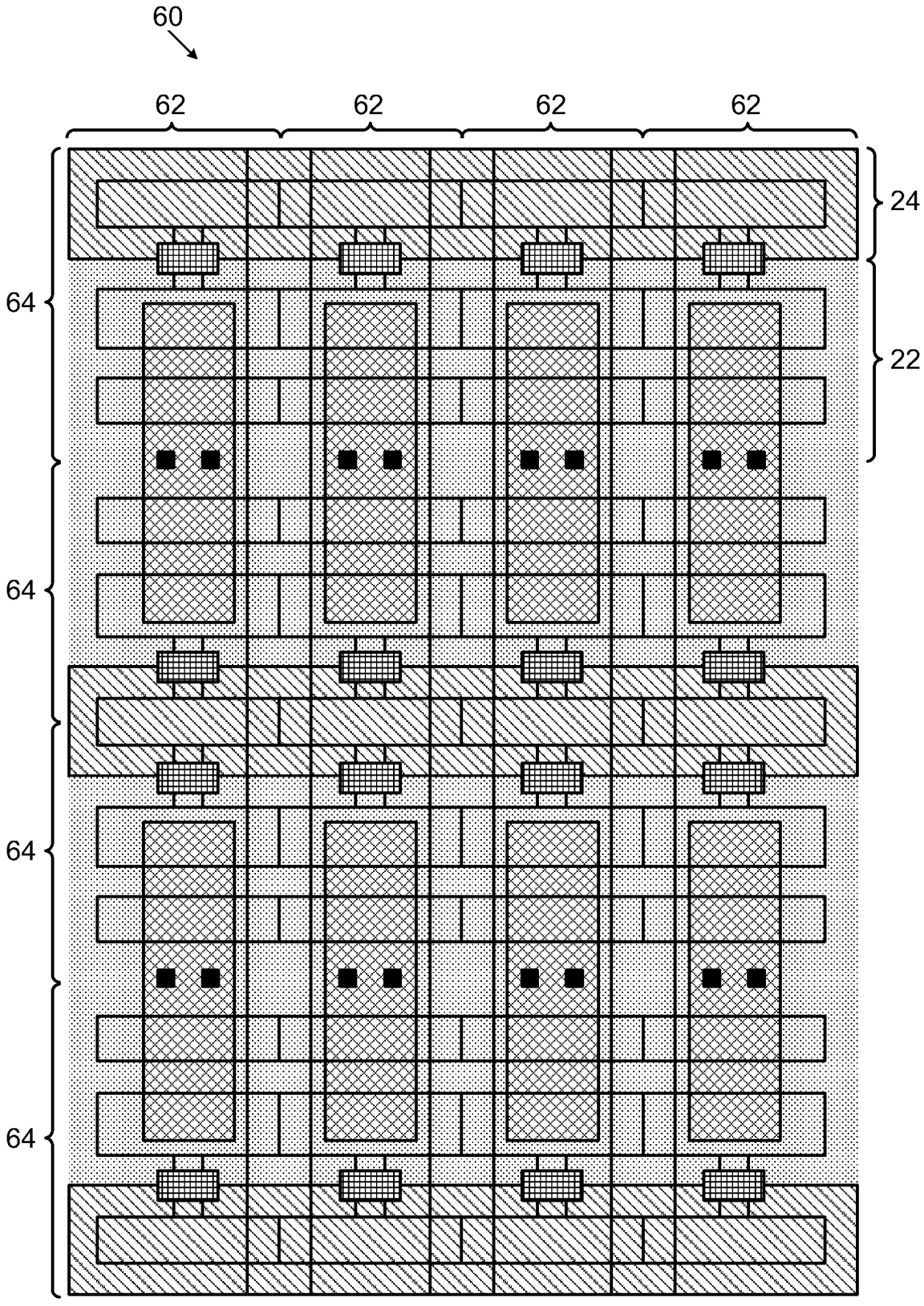

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/050743

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C16/22 G06F21/00 G11C7/24 G06K19/073
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C G06F G06K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/033705 A1 (WALMSLEY SIMON ROBERT [AU] ET AL) 10 February 2005 (2005-02-10) cited in the application	1-30
A	US 2004/159835 A1 (KRIEGER JURI HEINRICH [US] ET AL) 19 August 2004 (2004-08-19)	1-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 June 2012	02/07/2012

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2012/050743

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