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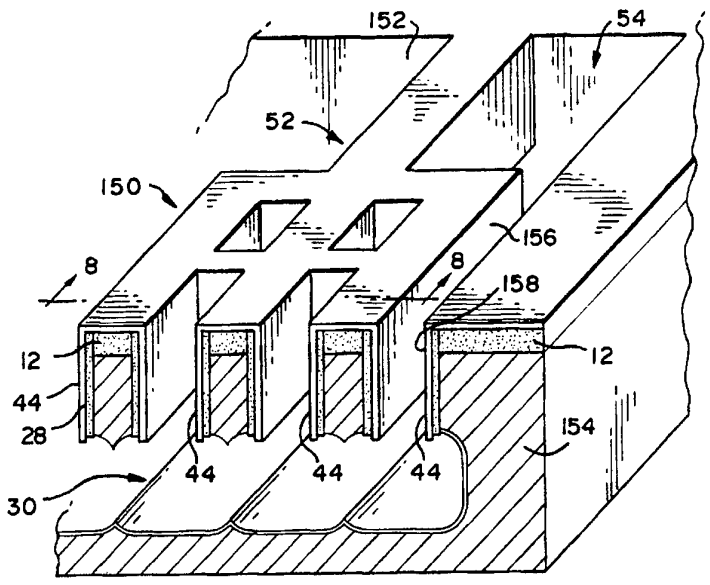

(57) Abstract

The invention provides a single mask, low temperature reactive ion etching process for fabricating high aspect ratio, released single crystal microelectromechanical structures independent of crystal orientation. A dielectric mask (12) on a single-crystal substrate (154) is patterned to define isolating trenches. A protective conformal layer (28) is applied to the resultant structure. The conformal layer (28) on the floor of the trenches is removed and a second etch deepens the trench to expose the mesa walls which are removed during the release step by isotropic etching. A metal layer (44) is formed on the resultant structure providing opposed plates (156) and (158) of a capacitor. The cantilever beam (52) with the supporting end wall (152) extends the grid-like structure (150) into the protection of the deepened isolation trenches (54). A membrane can be added to the released structures to increase their weight for use in accelerometers, and polished for use as movable mirrors.

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MICROSTRUCTURES AND SINGLE MASK, SINGLE-CRYSTAL PROCESS FOR FABRICATION THEREOF

Background of the Invention

This invention was made with Government support under Grant No. DABT 63-92-C-0019, awarded by DARPA and Grant Nos. ECS 8805866 and ECS 8815775 awarded by the National Science Foundation. The Government has certain rights in the invention.

This invention relates, in general, to microstructures and to a single mask process for fabricating them and more particularly, to microelectromechanical and microoptomechanical structures and to a single-mask process for fabricating complete structures including released, movable elements and connectors such as pads, runners, electrodes, and the like on a substrate.

Recent developments in micromechanics have successfully led to the fabrication of microactuators utilizing processes which have involved either bulk or surface micromachining. The most popular surface micromachining process has used polysilicon as the structural layer in which the mechanical structures are formed. In a typical polysilicon process, a sacrificial layer is deposited on a silicon substrate prior to the deposition of the polysilicon layer. The mechanical structures are defined in the polysilicon, and then the sacrificial layer is etched partially or completely down to the silicon substrate to free the structures.

The initial research into surface micromachining established the viability of the technology. Moving rotors, gears, accelerometers, and other structures have been fashioned through the use of such a process to permit relative motion between the structures and the substrate. This process relies on chemical vapor deposition (CVD) to form the alternating layers of oxide and polysilicon and provides significant freedom in device design; however, CVD silicon is usually limited to layers no thicker than 1-2μm, since residual stress in thicker layers overwhelms the structure and causes curling. Thus, although a large variety of layers can be combined to form very complicated structures, each layer is limited in thickness. In addition, the wet chemistry needed to remove the interleaved oxide layers often takes tens of hours of etching to remove, and once released the structures often reattach or stick to the substrate because of static electricity, and this requires elaborate process steps to overcome. The structures made of polysilicon inherently have a crystalline structure which has low breaking strength because of grain sizes, as well as electronic properties which are inferior to single crystal silicon. Furthermore although this technology is well established, it is not easily scaled for the formation of submicron, high aspect ratio mechanical structures.

In bulk micromachining, a silicon substrate is etched and sculpted to leave a structure. This has typically been done using wet chemical etchants such as EDP, KOH, and hydrozine to undercut single crystal silicon structures from a

silicon wafer. However, such processes are dependent on the crystal orientation within the silicon substrate, since the chemistry etches as much as ten times faster in some crystallographic planes of silicon than in other planes. Although the shapes can be controlled to some degree by the use of photolithography and by heavy implantation of boron, which acts as an etch stop, it is difficult to control the process and accordingly, the type, shape and size of the structures that can be fabricated with the wet chemical etch techniques are severely limited. In particular, wet etch processes are not applicable to small (micron size) structure definition, because they are not controllable on that scale.

A dry bulk micromachining process which utilizes thermolateral oxidation to completely isolate 0.5μm wide islands of single crystal silicon is described, for example, in the article entitled "Formation of Submicron Silicon-On-Insulator Structures by Lateral Oxidation of Substrate-Silicon Islands", Journal of Vacuum Science Technology, B 6(1), Jan/Feb 1988, pp. 341-344, by S.C. Arney et al. This work led to the development of a reactive ion etching (RIE) process for the fabrication of submicron, single crystal silicon, movable mechanical structures wherein the oxidation-isolation step described in the Arney et al publication was replaced with an SF_6 isotropic release etch. This process, which allowed the release of wider structures, in the range of 1.0μm, and deeper structures, in the range of 2-4μm, is described in U.S. Patent application Serial No. 07/821,944, filed Jan. 16, 1992, assigned to the assignee of the present

application. As there described, this dry etch process utilizes multiple masks to define structural elements and metal contacts and permitted definition of small, complex structures in single crystal silicon, and was easy to implement. However, the second lithography step was difficult to apply to deeper structures, particularly because of problems in aligning the second mask. Furthermore, that process relied upon the formation of a silicon dioxide layer on a single crystal silicon substrate, but since other materials such as GaAs or SiGe do not generate an oxide layer the way silicon does, the process could not be transferred to such other substrate materials.

In copending U.S. Patent Application Serial No. 07/829,348, a process for releasing micromechanical structures in single crystal materials other than silicon is described. This process uses chemically assisted ion beam etching (CAIBE) and/or reactive ion beam etching (RIBE) to make vertical structures on a substrate, and uses reactive ion etching (RIE) to laterally undercut and release the structure. The process utilizes multiple masks, however, and thus encountered similar problems to the silicon process described above in the formation of deeper structures, and in the alignment of the second mask.

The use of single-crystal materials for mechanical structures can be beneficial, since these materials have fewer defects, no grain boundaries and therefore scale to submicron dimensions while retaining their structural and mechanical properties. In addition, the use of single-crystal materials, particularly single

crystal silicon and gallium arsenide, to produce mechanical sensors and actuators can facilitate and optimize electronic and photonic system integration. For example, single crystal silicon structures having a very small mass can resonate without failure at 5 MHz for 2 billion cycles with a vibrational amplitude of plus or minus 200 nm. Accordingly, the fabrication of submicron mechanical structures with high aspect ratios would be highly desirable.

Summary of the Invention

It is therefore, an object of the present invention to provide an improved self-aligned dry-etch process for the fabrication of microelectromechanical structures (MEMS).

It is another object of the invention to provide a process for fabricating structures having micrometer-scale dimensions through a simplified, single-mask, dry-etch process.

Another object of the invention is to provide a low-temperature, single-mask, dry-etch process for fabricating high aspect ratio, released structures with micrometer-scale dimensions.

Still another object of the invention is to provide an improved, low-temperature process for the fabrication of microstructures in preexisting integrated circuit wafers, such as wafers which incorporate electronic circuitry, and to provide a process for connecting such structures to preexisting circuitry.

Another object of the invention is to provide a single-mask, low-temperature, dry etch process for fabricating microstructures on single crystal

substrates in which circuit elements have been constructed by a different process.

A still further object of the invention is to provide a single mask, low temperature process for making movable microstructures having deep trenches with substantially parallel walls and high aspect ratios independent of grain orientation in the substrate.

A still further object of the invention is to provide a single mask, low temperature process for fabricating mechanical actuator microstructures movable within a substrate or movable out of the plane of the substrate.

A still further object of the invention is the provision of movable microstructures in single crystal silicon, such microstructures being fabricated by a dry etch, single mask process, the structures being usable as sensors, resonators and actuators, inductors, capacitors, and the like.

A still further object of the invention is the provision of movable microstructures on single crystal silicon substrates, the structures optionally including membranes, and being used as sensor/actuators, resonators, optical reflectors, and the like movable in the plane of the substrate and rotatable out of that plane, such microstructures being fabricated by a dry etch, single mask process and by selective deposition of metal.

Briefly, the process of the present invention is a single-mask, low temperature (less than about 300°), self-aligned process for the fabrication of microelectromechanical (MEM) structures, the process allowing the fabrication of discrete MEM devices as well as the integration of such

structures on completed integrated circuit wafers. The process may be used to produce a variety of sensor devices such as accelerometers, as well as a variety of actuator devices, resonators, movable optical reflectors, and the like either as separate, discrete devices on a substrate, or as components on previously-fabricated integrated circuits. The process may be referred to as the SCREAM-I process (Single Crystal Reactive Etch and Metal).

The present SCREAM-I process is a dry bulk micromachining process which uses reactive ion etching to both define and release structures of arbitrary shape, and to provide defined metal surfaces on the released structure as well as on stationary interconnects, pads and the like. The earlier process defined in the above-mentioned copending application Serial No. 07/821,944 also permitted fabrication of microstructures, but required two masks to define the structural elements and the metal contacts. The present invention was developed from that earlier process, but improves on it by extending the structural depth to about 10 to 20μm, permitting formation of beam elements 0.5μm to 5μm in width, eliminating the second mask/lithography step of the prior process, and allowing all structural elements, including movable elements such as beams and stationary elements such as interconnects, beams and contact pads to be defined with a single mask so that the metal contacts applied to the structure are self-aligned.

The process relies, in general, on the formation of a dielectric mask on a single-crystal substrate such as silicon, gallium arsenide,

silicon germanium, indium phosphide, compound and complex structures such as aluminum-gallium arsenide-gallium arsenide and other quantum well or multi layer super lattice semiconductor structures in which movable released structural elements electrically isolated from surrounding substrate materials and metallized for selective electrical connections can be fabricated using a single mask. The structure so fabricated can be discrete; i.e., fabricated in its own wafer, in which case any of the aforementioned substrate materials can be used, or it can be integrated in a silicon integrated circuit wafer, in which case the substrate material will be silicon, allowing low temperature processing in accordance with the invention.

Complex shapes can be fabricated in accordance with the invention, including triangular and rectangular structures, as well as curved structures such as circles, ellipses and parabolas for use in the fabrication of fixed and variable inductors, transformers, capacitors, switches, and the like. Released structures are fabricated for motion along X and Y axes in the plane of the substrate, along a Z axis perpendicular to the plane of the substrate, and for torsional motion out of the plane of the substrate.

In essence, the invention permits fabrication of released structures and the subsequent metallization of such structures with a single dielectric mask by using that mask to define deep isolating trenches completely around the structures, undercutting these structures to selectively release them and to produce cavities

at the bases of surrounding mesas, and then metallizing the exposed surfaces. The undercutting and cavity formation breaks the continuity of the deposited metal, thereby electrically isolating the metal on released structures and defined mesas from the metal on the bottom of the trenches, and a dielectric layer isolates the metal from the underlying substrate. The elements defined by the trenches are interconnected by the metal layer so that released structures can be electrically connected through the metal layer to pads in the surrounding mesas, with interconnects provided in selected locations and with the interconnects and pads also being defined by the trenches.

When the single mask process is carried out on a discrete substrate or wafer, the process can be carried out by either high or low temperature processes, but when the structures are to be integral with existing circuitry on a wafer, a low temperature process is preferred to prevent damage to the existing circuitry. The process of the invention, in forming deep, narrow trenches to define the isolated and released structures produces high aspect ratio structures which can be metallized on their side walls for high capacitance between adjacent walls. In addition, the process permits a deep etching below the released structures to reduce parasitic capacitance between the released structures and metal on the trench floor. The etching process also produces extended cavities in the side walls of the mesas surrounding the released structures so reduce leakage current between metal on the side walls and on the trench floor. The

metallization on the released structures cooperates with metallization on mesa side walls and metallization on the trench floors to capacitively control and/or sense horizontal and vertical motion of the released structure.

If desired, it is also possible to carry out additional steps after completion of the single mask processing described above to modify the resulting structure. For example, an additional masking step can permit reduction of the spring constant of a released beam. In addition, a membrane can be added to released structures to increase their weight for use in accelerometers, and these membranes can be polished for use as movable mirrors. Additional steps may be used to connect metal layers to external circuitry, as by way of vias, and plural layers can be fabricated to form superimposed structures.

A wide range of devices can be fabricated utilizing the process of the present invention. As noted above, the process is independent of crystal structure in the substrate, so that essentially any shape can be fabricated and released. Thus, single or multiple fingers cantilevered to a side wall of a substrate and extending outwardly over a trench bottom wall, various grids and arrays can be fabricated and various electrical components can be formed. These various structures may be referred to herein as "beams" or "released beams", it being understood that such beams or released beams can be of any desired shape and can be single or multiple structures.

The metallization of selected walls and surfaces of the beams and surrounding substrate

allows capacitive control and sensing of horizontal motion in the released structures while metallization of the trench bottom wall allows control and sensing of vertical motion by providing a relatively wide released structure, for example in the form of a grid or plate, supported axially by single beams to a surrounding mesa wall, and by selectively applying a potential between one side or the other of the plate and the metal on the trench bottom permits torsional rotation of the plate about the axis of its supporting arms. Such a torsional rotation of a plate has numerous applications; for example, in optics.

The released structures of the present invention can be in the form of, for example, a single beam which serves as an accelerometer or a sensor and which is movable horizontally and vertically or in the form of plural beams in side by side parallel arrangement, or in various other arrays. Plural beam structures can work together, for example moving horizontally toward and away from each other to form "tweezers" or can have varying characteristics, such as thickness, to provide varying responses and thus to provide a wide range of motion or sensitivity in, for example, an accelerometer. Various grid-like arrays may be provided to add mass or to provide torsional motion as described above, the process of the present invention permitting an exceptionally wide variety of arrays.

An example of the use of structures fabricated in accordance with the process of the present invention is in torsional resonators fabricated from single crystal silicon. Micro-

machined resonators have been employed in a wide range of sensor applications, and in such applications the most important resonator characteristic is mechanical dissipation. Often, a sensor application requires operation of a resonator in a gas or liquid medium such as air and because of their small mass, such resonators are expected to have their dissipation determined by the surrounding medium. Torsional resonators fabricated of single crystal silicon in accordance with the invention have a lower mechanical dissipation, and thus are valuable in this application. Furthermore, torsional resonators constructed in accordance with the present invention undergo motions out of the single crystal silicon wafer plane and are capable of large motions in this direction. Such out of plane motion presents potentially useful actuator and rotating mirror applications.

The basic process of the present invention can be outlined as follows.

First, a dielectric layer of oxide or nitride is deposited on a wafer or substrate, this layer serving as a mask throughout the remainder of the steps. A standard PECVD process is used because of its high deposition rate and low deposition temperature. Thereafter, resist is spun, exposed and developed on the mask layer. Standard photolithographic resist techniques are used to define the desired beams, pads, interconnects and like structures. Thereafter, the pattern produced in the resist is transferred from the resist to the mask dielectric using, for example, CHF_3 magnetron ion etching (MIE) or RIE.

An O_2 plasma etch may be used to strip the resist layer, and the patterned dielectric mask is then used to transfer the pattern into the underlying wafer to form trenches around the desired structures. A deep vertical reactive ion etch (RIE) or chemically assisted ion beam etch (CAIBE) is required for this purpose. Depending on the choice of structure height, the trenches may be from 4 to 20μm deep, with substantially vertical, smooth walls.

After completion of the trenches, a protective conformal layer of PECVD oxide or nitride is applied to cover the silicon beams/structures to a thickness of about 0.3μm thick. The conformal dielectric layer covers the top surfaces of the surrounding substrate (or mesa), the defined structures, and the sides and the bottom wall of the trench, so it is necessary to remove the dielectric from the trench bottom wall, as by an anisotropic CF_4/O_2 RIE at 10 mT. This etch does not require a mask, but removes 0.3μm of dielectric from the beam and mesa top surfaces and from the trench bottom, leaving the side wall coating undisturbed. As a result, the beam is left with a top surface layer and a side wall layer of dielectric, with the bottom of the trench being film-free.

A deep RIE or CAIBE is then used to etch the trench floor down below the lower edge of the sidewall dielectric. This etch preferably exposes 3 to 5μm of substrate underneath the dielectric on each side of the beams and under the dielectric on the walls of the surrounding mesa, and it is this exposed substrate under the beams and on the mesa walls which is to be removed during the release

step. The release is carried out by an isotropic RIE which etches the substrate out from under the beams or other structures, thus releasing them, and etching the substrate on the mesa walls to form cavities. The etch has high selectivity to the dielectric, allowing several microns of substrate to be etched without appreciably affecting the protective dielectric coating. After release, the beams are held cantilevered over the bottom wall of the deep silicon trench by their connections to the surrounding mesa at their ends, for example.

Each released, cantilevered structure has a core of semiconductor material such as single crystal silicon and a conformal coating of dielectric surrounding it on the top surface and side walls. The structural beams may be cantilevered at the ends and free-floating in the center, for example. To activate the structure, either by measuring its motion or by driving it into motion, a metal layer is required. Accordingly, as a final step, an aluminum layer is sputter deposited onto the beam top surface and side walls of the beam, onto the floor of the trenches, and onto the top surface and side walls of the surrounding mesa. The structure is now complete and simply needs to be connected to suitable circuitry to activate it. The circuitry may be on a separate substrate or may be formed in the wafer adjacent the location of the beam prior to fabrication of the beam. It may also be desirable, depending on the application, to add a thin passivation oxide layer 100 to 200nm thick to prevent shorting between moving structures.

In designing and fabricating a single-mask MEM device using the present invention, only a single layer of metal is used because of the simplified nature of the process. Furthermore, in addition to surrounding the beams, a trench must surround every electrically complete set of interconnects, contact pads and capacitive plates. This trench serves a dual purpose. It isolates and defines the individual structured elements such as the beams, pads and conductors and, because of the self aligned nature of the process, the trench automatically patterns the metal. Released MEM beams normally are narrow to facilitate the release step and to provide flexibility and light weight, while interconnects formed by the same process normally are wider to prevent release and to provide stable support for the released beam. Beams destined for release typically would be about 1μm wide and preferably less than a maximum of between 3 and 5μm. Interconnects typically are not meant to move, and thus can be wider than 5μm.

Because of the low temperature requirements of some embodiments, the simple design rules and the short process times of the present invention, the process described herein can be added to conventional very large scale integrated circuits without damaging such circuits or interfering with their construction. One of the benefits of the present process is the ability to define all the electrical components with a single mask. In prior processes, after every metal deposition, a photolithography step became necessary to etch back the metal and define the interconnects. In the present invention, the etch back is not

necessary, for the metal runners are self aligned and self-defined.

Brief Description of the Drawings

Although the foregoing and additional objects, features and advantages of the present invention will become apparent to those of skill in the art from the following more detailed description of a preferred embodiment, taken in conjunction with the accompanying drawings, in which:

Figs. 1A - 1J illustrate steps 1 through 10, respectively, of the process of the present invention;

Fig. 1K illustrates a modification of Step 9 of the process;

Fig. 1L illustrates a further modification of the process of steps 1-10;

Fig. 2 is a top plan view of a beam and associated contact pads and interconnects fabricated by the process of Figs. 1A-1J;

Fig. 3 is a cross-sectional view of the device of Fig. 2, taken along lines 3-3 thereof;

Fig. 4 is a cross-sectional view of the device of Fig. 2, taken along lines 4-4 thereof;

Figs. 5A-5C illustrate optional preliminary steps for a second embodiment of the invention, wherein a MEM structure fabricated in accordance with the process of Figs. 1A-1J is incorporated in an integrated circuit wafer;

Figs. 5D-5I illustrated additional steps for the second embodiment of the invention;

Fig. 6 is a diagrammatic view of a third embodiment of the invention;

Fig. 7 is a diagrammatic view of a fourth embodiment of the invention;

Figs. 8A-8L illustrate the steps of a fifth embodiment of the invention;

Fig. 9 is a diagrammatic perspective view of a structure for providing torsional motion;

Figs. 10A-10C illustrate steps for producing electrodes for use in the structure of Fig. 9;

Figs. 11A-11C illustrate steps for producing a modified form of electrodes for use in the structure of Fig. 9;

Fig. 12 is a partial cross-sectional view of Fig. 9 illustrating a modification of the torsional structure; and

Fig. 13 illustrates a structure fabricated in accordance with the process of the invention.

Detailed Description of the Invention

Although a number of variations on the basic process of the present invention are described hereinbelow, the basic process is capable of fabricating a functioning MEM structure with a single mask. The basic process and its variations all rely on the characteristics of single-crystal structures for the substrates, and further depend on the use of standard fabrication tools, on the use of optical or E-beam lithography and on self-aligned construction. The invention permits definition of high-aspect-ratio structures having walls closely spaced to corresponding walls on a substrate for high capacitance between the adjacent walls. The basic process is illustrated in steps 1 through 10 of Figs. 1A through 1J, respectively, of the drawings, which outline a single-mask, low-temperature, self-aligned process

for making microelectromechanical structures. These figures illustrate the fabrication of a released, cantilevered beam which is free to move left or right in a generally horizontal path (as viewed in the Figures), and illustrate an adjacent vertical static plate which forms a parallel capacitor plate to measure the motion of the beam or, in the alternative, to cause motion of the beam.

The illustrated process is implemented with a single mask, with the structure being fabricated as a discrete element on a wafer or die. As previously noted, a discrete element is defined as an element on a wafer without electronic circuitry but which has bonding/contact pads that will be wire-bonded to external circuitry. Another embodiment of the invention, discussed below, relates to fabrication of an integrated element which, as used herein, refers to a structure fabricated on an integrated circuit chip and directly connected to on-chip circuitry through interconnects or vias.

The following Table I outlines the process of the present invention, as will be described more fully hereinbelow.

TABLE I

Step Number	Description (Single Crystal Silicon)	Description (Gallium Arsenide)
1. Mask dielectric	PECVD (1-2μM) oxide or nitride	PECVD oxide or nitride
2. Photolithorgraphy	Vapor prim	Vapor prime
	Spin & bake resist	Spin & bake resist
	Expose	Expose

	Develop	Develop
	Descum	Descum
3. Pattern transfer	CHF_3 MIE	CHF_3 MIE
4. Resist removal	O_2 plasma	O_2 plasma (optional)
5. Trench etch #1	Cl_2 RIE	Cl_2 CAIBE
6. Sidewall dielectric	PECVD (0.3μm) oxide or nitride	PECVD oxide or nitride
7. Clear floor dielectric	CF_4 RIE	CF_4 RIE oxide or nitride
8. Trench Etch #2	Cl_2 RIE	Cl_2 CAIBE
9. Release	SF_6 RIE	BCl_3 RIE
10. Sputter metal	Aluminum or equivalent metal	
11. Wire bond		

Steps 1 through 10 of the Table correspond to steps 1 through 10 of Figure 1. Two processes are outlined in the Table, one for single crystal silicon substrates and the other for Gallium Arsenide substrates. The following description refers first to a process for fabricating single crystal silicon.

Referring now to Figure 1A, in Step 1 of the process, a clean, open area of bare silicon such as a top surface 8 of a single crystal silicon wafer 10 is provided, on which is deposited a layer 12 of oxide (SIO_2), this layer serving as a mask throughout the remainder of the steps. Although this oxide may be grown in a furnace, this would be suitable only for discrete elements, for the formation of a thermal oxide requires temperatures of 1000° or more, which would damage any electrical elements on the wafer. The oxide layer 12 can be deposited by PECVD or by some

combination of PECVD and thermal growth, but a standard PECVD process is preferred because of its high deposition rate and the fact that it has a low deposition temperature, in the range of 300-500°, which is suitable for fabrication of integral elements on wafers carrying electrical components. The minimum oxide thickness is determined by how fast the later RIE steps (to be described) will etch the oxide, but in general, the oxide mask layer can be a great deal thicker than the required minimum thickness. In a typical process where the beam or other structure height is to be 10μm, a thickness of about 0.7μm is desirable for the oxide.

The height of the structure to be fabricated is, more precisely, the height of a silicon "skeleton" which will be located inside the oxide-coated released beams fabricated by the present process. This silicon skeleton is the major component of the beams produced by the process and, as noted above, typically can have a height of about 10μm or more with a minimum height of about 3μm.

Step 2, illustrated in Fig. 1B, is a photolithography step wherein a resist material 14 is spun onto the top surface 16 of the mask oxide, is exposed, and is developed, using standard optical photolithographic resist techniques to produce a pattern 18. Optical techniques are preferred, since a resolution of less than about 0.5μm generally is not required; however, if better resolution is needed, electron beam lithography with a tri-level resist and an aluminum lift-off mask can be used.

Using the pattern 18 developed in the resist, the underlying oxide layer 12 is etched to transfer the pattern to the oxide mask, as illustrated in Fig. 1C, Step 3. As there illustrated, the oxide layer 12 is etched using, for example, CHF_3 in a magnetron-ion etching (MIE) machine. Such etching is virtually identical to RIE, except it utilizes a large magnet which concentrates the plasma and increases the etch rate. The high etch rate of MIE helps to prevent resist burning. In addition, the MIE etches at a very low pressure (about 1 to 3mTorr), provides vertical side walls and increases throughput. The pattern 18 formed in the resist material 14 is thus transferred to the mask oxide 12, as illustrated by mask pattern 20.

The resist material is not used to mask the pattern 18 directly onto the silicon substrate 10 because the Cl_2 etch (to be described), which is used to dig the trenches in the silicon to form the beam structures, etches resist material much more quickly than oxide. Thus, the use of an oxide mask allows the silicon etch to last longer and to dig deeper than could be done with the same thickness of resist.

Following the pattern transfer of step 3, the resist material is stripped, as illustrated in Step 4, Fig. 1D. The resist is removed in known manner as, for example, by an O_2 plasma etch utilizing a "barrel asher", wherein ionized oxygen radicals attack the resist, or by utilizing a wet chemical resist strip using a chemical solvent that dissolves the resist. The O_2 plasma etch is preferred since it is fast, removes the resist

completely to leave a clean surface, and has a high throughput.

The deep silicon etch illustrated in step 5 (Fig. 1E) is critical to the process of the present invention. This is a deep silicon etch in which the pattern 20 is transferred into the silicon 10 by a deep, vertical anisotropic BCl_3/Cl_2 RIE to form deep trenches 22. The etch is carried out in three steps in a standard RIE chamber, as illustrated in the following Table II.

TABLE II

Parameter	Step 1	Step 2	Step 3
Power:	200 Volts	300 Volts	475 Volts
Pressure:	20 mTorr	20 mTorr	40 mTorr
Time:	1 min.	1 min.	(user defined)
Chemistry:			
Cl_2	0 sccm	2 sccm	50 sccm
BCl_3	14 sccm	14 sccm	5 sccm
H_2	7 sccm	7 sccm	0 sccm
Erch rate: Si	1900Å/min. =	11.4μm/hr	
Etch rate: SiO_2	96Å/min. =	0.576μm/hr	
Selectivity:	20:1:Silicon:Oxide		

Because of the very high selectivity in the main Cl_2 etch, in the range of 20 to 1 for silicon and silicon oxide, the presence of a native oxide can cause unwanted masking. Therefore, the first two etch steps are used to attack and remove the first 10 to 20nm of oxide, while the third step is used to carve out the silicon trench. The BCl_3 gas etches oxide, while the Cl_2 etches silicon.

A better selectivity in the etch could be obtained by eliminating the BCl_3 and using pure Cl_2 so that 40μm of silicon would be etched for every 1μm of oxide. However, any small pieces of oxide that might fall into the trench would act as an undesired mask because of this selectivity. This commonly happens during etching, with sputtered pieces of oxide falling into the trench and acting as minute masks. The BCl_3 etches the oxide that falls into the trench and thus improves the quality of etch.

The Cl_2/BCl_3 etch has an additional effect which is very helpful; namely, in situ side wall thin film deposition. This etch deposits a thin layer 24 of silicon dioxide on the side wall and bottom of the trenches during the etch, and this thin layer acts as an additional side wall mask which can be used in subsequent steps.

At this point in the process, as illustrated in Fig. 1E, deep trenches 22 have been carved into the substrate 10, following the pattern 20 of the mask oxide 12. A cross-section of the substrate, such as that shown in Fig. 1E, reveals one or more silicon islands 26 (only one of which is illustrated) surrounded by trenches which separate the islands from the surrounding substrate which forms a mesa 27. The islands can be any selected width, for example about one micron, can be several microns tall, can be hundreds of microns long, and can be in any desired shape or pattern, as established by the photolithograph step. The islands 26 and the surrounding substrate 27 may both be referred to as mesas, and each has an oxide mask 12 on the mesa top and a thin oxide layer 24 on the side walls caused by the Cl_2 etch.

The core of the island 26 is single crystal silicon, as is the substrate 10 which forms mesa 27.

In order to release the island structures, a protective film is provided on the top surface and on the side walls, with the trench bottom being bare silicon so that an isotropic RIE can be used to etch the silicon out from under the islands to form cantilevered or free standing beams, and to etch the silicon out from under the surrounding mesa to form undercut cavities.

More particularly, a protective film for the silicon islands and surrounding mesa is provided in accordance with step 6, illustrated in Fig. 1F, wherein the entire wafer is coated with a protective oxide layer 28, using a standard plasma enhanced chemical vapor deposition (PECVD) process. This is very similar to an RIE, except that the gases which flow into the chamber react to form films, rather than attack them. SiH_4 and NO_2 react to form silicon dioxide and NH_3, with the individual molecules of silicon dioxide bonding to the surface of the wafer and forming a thin film of oxide. The reaction is very conformal; that is, it covers all surfaces with an equally thick layer, regardless of angle or orientation. The layer of oxide 28 illustrated in Fig. 1F incorporates the thin layer 24 illustrated in Fig. 1E. In accordance with this process, the layer 28 extends over the mask layer 12 so that the thickness of the silicon dioxide on the island and mesa tops is thicker than that at the floor 30 of the trenches 22.

As illustrated in Fig. 1G, in step 7 of the process the oxide layer 28 on the floor 30 of the

trenches is removed by an anisotropic CF_4/O_2 RIE. This etch carves straight down, with very little lateral influence and is easily done with a low pressure RIE. This effectively removes one layer from every horizontal surface; in this case, the island and mesa top surfaces and the trench bottom, and does not affect the side walls, thereby leaving an oxide layer that covers the top and sides of the island 26 and surrounding mesa 27, but leaves the floor 30 open, as illustrated in Fig. 1G.

With the trench floor 30 film-free, a second anisotropic Cl_2/BCl_3 RIE silicon etch is carried out, as illustrated at step 8 in Fig. 1H. At this point, the mask and side wall oxides 12 and 28 are in place on the mesas 26 and 27 and only the trench floor is film-free silicon. This second silicon etch adds about 3 to 5μm of depth to the trench bottom 30; that is, the trench bottom is etched 3 to 5μm below the lower edge 32 of the side wall oxide layer 28, thereby exposing 3 to 5μm of side wall silicon 34. This etch facilitates the next following isotropic release etch (step 9) by exposing the silicon at the bases of the islands 26. This etch has three benefits; it facilitates the release of the structures, it lowers the trench floor to control the spacing between the beam, when it is released, and the floor, and it prevents excessive upward etching of the structure behind the side wall oxide coating 28.

Step 9, Fig. 1I, illustrates the isotropic release etch step which separates and releases the islands from the underlying substrate to produce released beams such as the beam 36, which may, for

example, be connected at one end to extend in a cantilevered fashion over the floor of the trench. This etch step is an SF_6 isotropic high pressure, low power RIE process which attacks the silicon at the trench floor 30 and the lower side wall portion 34 to etch the silicon from under the mesas in the region 38 indicated by the dotted lines. The island 36 is narrow in the region of the etch so it is fully released. The SF_6 etch also etches out a cavity 40 in the side wall of the substrate mesa 27, adjacent the location of the beam 36, the upper portion of the mesa side wall being protected by the oxide layers 12 and 28, discussed above, creating a new trench floor 30'.

It is noted that although the second silicon etch of step 8 is preferred, it is not essential because the SF_6 release etch of step 9 can etch downwardly through the floor 30 of the trench and eventually will etch away under the mesas. However, this takes an additional amount of etching time because the SF_6 etchant reaction is "transport limited"; that is, the etchant can't reach the surfaces to be etched fast enough in the narrow trenches. In contrast, the SF_6 etch will be more efficient if step No. 8 is included, for in that case a large, open silicon side wall is presented which allows lateral etching to begin immediately to minimize the required SF_6 release time.

By including step No. 8, the vertical distance between the released beams 36 and the trench bottom 30 (Fig. 1I) can be controlled. If step No. 8 is excluded, the beam to floor distance will depend only on the SF_6 release time, but by

adding a silicon etch before the release this distance can be increased as required.

It has been found that as the SF_6 etchant begins to etch underneath the mesas 24, it begins to reach up underneath the beams, within the protective layers 28, since the etchant etches in all directions equally. Normally, a plasma etch is directed toward to the surface to be etched with an accelerating potential which drives the etchant down to the substrate, so an RIE normally is an inherently directional etch. However, isotropic etching can be obtained by increasing the pressure so that the directionality is less evident and lateral etching is more evident, and the present invention preferably utilizes a sufficiently high pressure to make the release more isotropic than directional and to rapidly undercut the island.

If the deepening of step 8 is not used, the initial distance from the undersurface of beam 36 to floor 30 will be from 3-5μm. However, if the etch of step 8 is used, this distance increases to between 5 and 9μm from beam 36 to floor 30' by the end of the etch. The increase in the distance between the beam and the floor of the trench during the etching process also limits the upward etch rate under the protective oxide layers 28, thus ensuring a high aspect ratio for the released beam 36.

As illustrated in step 10, Figure 1J, a sputter deposition of aluminum can be used to provide metallization of the beam top surface and side walls, as well as the surface and side walls of mesa 27. Such a metal layer is illustrated at 44 in Fig. 1J, with the spacing between the beam

and the floor 30 and the cavity 40 providing isolating breaks in the coating. The metallization on the top surfaces and side walls of the mesas is thus isolated from that on the floor 30 of the trenches, thereby producing a complete, electrically isolated metallized structure such as the beam 36 which can then be interconnected to suitable circuitry. It is noted that the metal layer 44 is also electrically isolated from the underlying silicon by oxide layers 12 and 28.

Fig. 1K illustrates an alternative to Fig. 1I, wherein the released etch of step 9 is continued for an extended period of time to increase the depth of the trenches 22 produce an enlarged cavity 40' in mesa 27 and to increase the distance between floor 30 and the released beam 36. The cavity 40' extends upwardly behind the side wall oxide layer 28 so that when the metal layer 44 is applied (step 10) an extended leakage path, indicated by dotted line 46 is created to reduce leakage between metal 44 and the substrate silicon in the mesa 27. If desired, the etch can be continued through the bottom of the substrate to produce an aperture through the wafer in which the MEM structure such as beam 36 is suspended.

Extension of the etching time also serves to etch the bottom of beam 36, producing a cavity 48 between the beam side wall oxide and metal layers, again as illustrated in Fig. 1K. The reduced side of beam 36 reduces its mass and increases its flexibility, a feature which is highly desirable in some applications.

Fig. 1L illustrates a further alternative to the process described in Figs. 1A-1J, wherein a

conformal dielectric layer 49 of CVD oxide or nitride is deposited on the structure of Fig. 1I before the metallization step of Fig. 1J. This conformal layer covers the top, bottom and sides of released beam 36, covers the sidewall oxide 28 on the mesa 27, and covers the floor 30' of the etched trenches, providing an insulating layer between the underlying substrate and the metallization layer 44 deposited in accordance with Fig. 1J.

A further alternative is to thermally grow oxide on the exposed silicon surfaces (floor 30' and the bottom of beam 36) of Fig. 1I to provide insulation between the metal layer 44 and the silicon substrate. However, this is less preferred, since thermal oxide is a high temperature process. Further, the deposition process of Fig. 1L provides a thicker layer of dielectric on the mesas, and increases the electrical path between the metal layer on the sidewalls and the metal on floor 30'.

The foregoing description of the process set out in steps 1 through 10 of Table I is directed to the application of the process to single crystal silicon. However, the process is also applicable to other materials, such as gallium arsenide, as set out in the corresponding right-hand column in Table I. These steps are also illustrated in Figs. 1A through 1J, although different materials are used, as set out in the Table. Thus, for example, in step 1 the dielectric mask is a PECVD oxide or nitride, the oxide being deposited since the gallium arsenide cannot be oxidized in the manner of silicon. The dielectric may also be nitride, if desired.

The photolithography process of step 2 is the same, as is the pattern transfer of step 3. When using a gallium arsenide substrate, the resist removal process of step 4 is optional, and may not be required.

The trench etch of step 5 is a CAIBE process using Cl_2, rather than the RIE process used with single crystal silicon. The side wall dielectric is applied by PECVD oxide or nitride, and step 7 utilizes CF_4 RIE in the manner used with single crystal silicon.

The trench etch step 8 is again a Cl_2 CAIBE process, while the release step 9 uses BCl_3 RIE. With these changes, the process of the present invention can be used to produce gallium arsenide released beam structures which can be metalized in accordance with step 10 in a single mask process.

If the released structure is in a discrete wafer, the device may be connected as by a wire bond (Step 11 in Table I) to suitable external circuitry. A suitable structure for such wire bonding is illustrated in Fig. 2 which is a top view of a simple microelectromechanical device constructed in accordance with the process of Figure 1. As there illustrated, a wafer 50 of single crystal silicon is patterned to produce a single released beam 52 located in a trench 54, the beam 52 being similar to beam 36 of Fig. 1J. Formed on each side of the released beam 52 by trench 54 are fixed structures such as electrodes 56 and 58, illustrated in cross-section in Fig. 3 and corresponding to mesa 27 in Fig. 1J. The cross-section is taken along lines 3-3 of Fig. 2.

Also defined by the trench 54 are additional fixed structures such as contact pads 60, 62 and

64 and their corresponding interconnects. Pad 62 is connected to the released beam 52 by way of interconnect 66, as illustrated in Fig. 4, which is a cross-section taken along line 4-4 of Fig. 2. The interconnect is illustrated as being wider than the released beam 52 of Fig. 3, and is not released from the substrate 50 so that it is stationary and provides a support wall at region 68 (Fig. 2) for mounting a fixed end of the cantilevered released beam 52. Contact pads 60 and 64 are connected to the electrodes 56 and 58, respectively, by way of interconnects 70 and 72, respectively, these interconnects being similar to interconnect 66. As illustrated, the interconnects, contact pads, and electrode supports are all formed as mesas, are covered by dielectric layers 74 and 76 on the top surfaces and side walls, respectively and are surrounded by the trench 54. Upon metallization of the device, as described with respect to Fig. 1J, a metal coating 78 will be applied between the contact pad 62 and beam 52 only by way of interconnect 66, will connect contact pad 60 to electrode 56 only by way of interconnect 70, and will connect contact pad 64 to electrode 58 only by way of interconnect 72. Thus, the trench 54 and the oxide layers 74 and 76 electrically isolate the metal from the substrate and from adjacent structures.

The metal layer 78 on the electrodes 56 and 58 includes vertical side wall portions which cooperate with the side wall portions of the metal layer 78 on relief beam 52 to produce the parallel plates of capacitors. When the two electrodes 56 and 58 are located in close proximity to the beam

52, the capacitance therebetween, which is a function of distance, can be measured. Therefore, any movement of the beam 52 with respect to beams 56 and 58 can be accurately measured. The side wall parallel plates can be in the range of 10 to 20μm tall, depending on the height of the beam 52, and can have 1 to 2μm of interplate spacing. The beam and electrodes can be several thousands of microns in length, so that a large capacitance can be provided. Such a structure has an important use as an accelerometer by measuring relative motion of the released beam with respect to the stationary electrodes.

It is noted that the process of the present invention permits automatic definition of the metallization for the capacitors, interconnects, and contact pads without the need for additional photolithographic steps. All that is required is that the shape of these structures be established by the initial oxide layer which defines the location of the trenches, and these trenches then serve to isolate the metal from the substrate, as described above with respect to Figures 1A-1K. The overhanging oxide produced by the cavity 40 illustrated in step 9 (Figs. 1I or 1K) prevents the sputtered metal from contacting the substrate and prevents leakage current between the metal and the substrate to ensure this isolation. The sputter deposition of the metal is semiconformal and will laterally deposit on the side walls, but will not deposit underneath the overhanging edges of the oxide. Accordingly, the process provides a self-aligned and self-defined movable microelectromechanical device and provides electrical connectors for that device.

In addition to fabrication of the discrete structure illustrated in Figs. 2-4, the process of the present invention permits fabrication of integrated structures, wherein released beams and other microelectromechanical structures may be interconnected with an on-chip integrated circuit (IC). In accordance with this modification of the process, which is illustrated in Figs. 5A-5I, an integrated circuit wafer can be batch fabricated using standard integrated circuit technologies to produce desired circuits and circuit components on the wafer, and thereafter a microelectromechanical device can be fabricated on the wafer utilizing the process of the present invention without varying the standard IC technology. In this embodiment, the single crystal silicon process described above is utilized, since IC wafers are conventionally silicon. The single crystal silicon process of the invention operates at a sufficiently low temperature to permit the fabrication of released structures on existing IC wafers without thermal damage to the existing circuitry or circuit components. Of course, such a wafer could incorporate a segment of another substrate material such as gallium arsenide, if desired, in which case the alternative process of the present invention could be used, again without thermal damage to the existing circuits.

The process of fabricating microelectromechanical devices on existing IC wafers is outlined in the following Table III.

TABLE III

Step Number	Description
0a. Photolithography	Thin Passivation region for MEM device · Vapor prime; spin, bake, expose, develop & descum
0b. CF_4 isotropic RIE	Thin passivation layer
0c. O_2 plasma etch	Removal residual resist
Steps 1-9	(Same as Table I)
10. Photolithography	Open via windows to buried contacts · Vapor prime; spin, bake, expose, develop & descum
11. CF_4 Isotropic RIE	Etch oxide
12. Wet chemical resist strip & O_2 plasma	Remove residual resist
13. Sputter metal	Aluminum (pumpdown & deposit)
14. Photolithography	Pattern top level metal · Vapor prime; spin, bake, long exposure, long development & descum
15. Cl_2 Isotropic RIE	Etch sidewall aluminum
16. Wet chemical resist strip & O_2 plasma	Remove residual resist
17. PECVD Dielectric	Deposit thin passivation dielectric

In order to integrate released beams fabricated in accordance with the present invention, it is necessary that the fabricated integrated circuit die, or wafer, incorporate one or more buried metal contact pads, have a thick passivation oxide layer, and have sufficient space available for the microelectromechanical (MEM) device. Any kind of integrated circuit can be on the wafer for connection to the released structure

as long as any connections to the circuit or circuit components are by way of metal pads. These pads are buried directly beneath a passivation oxide layer so that they can be accessed by way of a via etch. The passivation layer preferably is PECVD oxide across the entire wafer, and is used as the mask oxide for the fabrication process of the present invention. Such a passivation oxide is conventionally placed over a finished IC wafer as a hermetic seal against water and other contaminants during handling and thus provides a convenient beginning point for the present process. This layer is generally in the range of 0.5 to 1.0μm thick, but if this is too thin, additional PECVD dielectric material such as oxide or nitride can be added in the fabrication process of the present invention. On the other hand, if it is too thick, or does not provide a good enough mask, then it can be removed and replaced by another PECVD oxide or nitride layer as needed. Preparation of the IC wafer prior to the fabrication of the MEM is described in steps a, b, and c, outlined in Table III, above, and is illustrated in Figs. 5A through 5C, to which reference is now made.

An integrated circuit (IC) wafer 100 includes a passivation oxide layer 102 which is formed as a final step in conventional IC fabrication to serve as a protective layer over the wafer. The thickness of this oxide layer preferably is no less than the minimum mask requirements discussed above. The wafer includes, for example, a metal contact pad 104 located in an insulating layer 105 such as oxide, the pad being a part of an integrated circuit (not shown) and connected into

that circuit in known manner. The wafer also includes a region generally indicated at 106 for receiving a MEM device. In general, the MEM device region will include a second layer 108 of oxide in addition to the passivation layer 102. This second layer is a field oxide, which is a thermally grown wet oxide placed between active devices as an isolation layer. The passivation oxide 102 is generally 0.5 to 1.0μm thick, while the field oxide 108 is generally 0.6μm thick.

Step 0a in Fig. 5A illustrates a photolithographic step which prepares the passivation layer 102 for fabrication of the MEM device. A resist layer 110 is spun onto the top surface of the wafer, is exposed and is developed to produce a pattern 112 defining the location of the MEM device. Thereafter, the oxide layers 102 and 108 can be thinned, if required, at step 0b in Fig. 5B, as by CF_4 isotropic RIE, leaving only a part of layer 102, as illustrated. Alternatively, the oxide can be thickened by the addition of more PECVD oxide, if required. The residual resist layer 110 is then removed by an O_2 plasma etch, as illustrated in Fig. 5C. In this illustrated embodiment, the photolithographic process thins the passivation oxide in the region 106 set aside for the MEM devices, without thinning the oxide over the previously fabricated IC devices, allowing more precise control over the mask oxide thickness.

Following the preparatory treatment of the wafer in steps 5A through 5C, the MEM device is processed within the region 106 of wafer 100, following steps 1-9 illustrated in Figs. 1A through 1I, resulting in the dielectric-covered

structure of Fig. 5D (also labelled as step 9), prior to metallization. Thereafter, the process of the present embodiment includes opening a via window to the buried contact and connecting it to the MEM device. As described in step 10 in Table III, a resist 120 (Fig. 5E) is spun onto the top surface of the mask oxide layer 122, which consists of the passivation layer 102, as well as the additional oxide layers on the top surface and on the trench side walls that are added during the fabrication of the released structure in steps 1-9. The resist 120 is exposed and developed to produce a via mask opening 124 in alignment with the contact pad 104. The oxide layer 122 is etched through the via mask opening 124 as by an isotropic CF_4 RIE illustrated in Fig. 5F, to produce via 126. Thereafter, the resist is removed by a wet chemical and O_2 plasma stripping step, also illustrated in Fig. 5F as step 12, thereby exposing the contact pad through a via 126.

Step 13 (Fig. 5G) is a sputter deposition step in which a metal layer 130 is deposited on the top surface of the wafer 100 and on the floor and the side walls of the trenches 54 in the manner illustrated and described with respect to Fig. 1J.

The deposited metal 130 is conformal, and coats contact pad 104 to thereby interconnect the MEM structure (for example, beam 52) with the contact 104. It will be understood that other similar contacts may also be connected to the metal layer by similar vias. Thereafter, the metal 130 is trimmed back to define the specific shape of the interconnects between the IC contact

points and the MEM structure. Since the sputter deposition is conformal and deposits metal on the top surfaces, down the side walls and on the floor of all the trenches, as illustrated in Fig. 5G, it becomes necessary to pattern the metal to limit the metallization to the desired interconnections. This involves photolithography across mesa tops, side walls, and trench-bottom surfaces, and is accomplished by first applying a high viscosity resist 132 to planarize the wafer, the resist filling the trenches and protectively coating the MEM devices. A long exposure is used to pattern the thick resist material, so that the patterning can be carried out through as much as 20 micrometers of resist material. A long development time is then required to develop the exposed resist.

Fig. 5H illustrates the resist material 132 which remains after exposure and development in step 14 of the process. Although resolution is lost by using a thick resist, long exposure times and long development times, nevertheless the resolution obtained by this process is more than sufficient. Although to a large extent the metal layer 130 is etched by the development process, nevertheless it is preferred that following the development of the resist layer 132, an isotropic Cl_2 RIE is carried out to isotropically etch all exposed aluminum. Thus, the aluminum not covered by resist 132 is etched away, as illustrated in Fig. 5I at step 15, leaving the metal layer 130 only in the via 126, along the location of the desired interconnect 134, and onto the cantilevered beam 52, so as to connect the beam to the integrated circuit. The resist layer 132 is

then removed by the wet chemical and O_2 plasma resist strip of step 16, also in Fig. 5I.

As a final step, a thin conformal PECVD dielectric is deposited on the entire surface of the wafer to insulate and passivate the devices. Note that because MEM structures are designed to move, they cannot be buried under several microns of passivation, so only about 100 to 300nm of oxide is used for this purpose. Nitride could also be used, although it is stiffer than oxide and may inhibit motion. The oxide deposition of step 17 is illustrated by arrows 136 in Fig. 5I.

It will be noted that the interconnection of the MEM device to an integrated circuit requires additional masking steps, as illustrated in Figs. 5E through 5I. However, the basic process for forming the MEM structure is a single mask process, as described above, and it is only the later processing that require these additional masking steps.

A further embodiment of the invention is illustrated in Fig. 6, wherein an elongated, released structure such as beam 52 further is treated to increase its lateral flexibility. The beam, which is fabricated in accordance with the single-mask process of Fig. 1, includes a metal layer 44 over oxide layers 12 and 28, and these layers tend to reduce the flexibility of the single crystal silicon core 36 of beam 52. Flexibility of the beam can be increased by removing the side wall oxide 28 and the side wall metal 44 from the beam in selected locations. Since the spring constant varies with the cube of the width of the beam, such removal can reduce the spring constant by one to two orders of magnitude.

In accordance with this embodiment, a thick resist layer (not shown) is spun onto the wafer, filling in the trench around the released beam. The resist is exposed in a conventional photolithographic step and developed to expose the aluminum layer 44 in the region 140 illustrated by the dotted lines in Fig. 6. By a Cl_2 isotropic RIE step, the exposed aluminum is etched on the top and side walls of beam 52 in the region 140 and the residual resist material is removed by a wet chemical resist stripping step. Thereafter, a layer 142 of aluminum is evaporated only onto the top surface of the beam 52 and this evaporated aluminum together with the remaining metal layer 44 is used as an etch mask for a CF_4 isotropic RIE etch of the side wall oxide 28 in the regions 144 of the beam so that the beams are film-free silicon on the sides in the region 140. Accordingly, in this region the beam is as narrow as the original silicon island 36, while the top of the beam carries a thin film of mask oxide 12 and the evaporated aluminum 142 so that electrical connectivity is achieved from the contact pads to the MEM device along the top surface of spring portion 140 of the beam.

An important use for the released beam 52 fabricated in accordance with the present invention is as an accelerometer, wherein flexing of the beam with respect to the capacitive electrodes, as illustrated in Fig. 2, is a measure of acceleration applied to the wafer on which the beam is mounted. In order to increase the sensitivity of such an accelerator, the beam can be made in a variety of shapes to increase its mass, for example, by adding a grid-like structure

150 to the free end of beam 52, as illustrated in Fig. 7. This grid-like structure is fabricated following the process of Fig. 1, steps 1-9, with the grid shape being determined by the initial photolithographic step. Such a grid may be of any desired width and length, and with any desired number of beams, and adds mass to the beam 52 to improve its function as an accelerometer. In large designs the grid may be 200μm by 900μm, with beams on 5μm or 10μm grid points. The beams may be from 1 to 2μm wide with openings between them being 3 to 4μm or 8 to 9μm wide. The grid is illustrated as being connected to one end of a released beam 52 which is cantilevered above the floor 30 of the surrounding trench and is mounted to an end wall 152 of a surrounding mesa portion 154. However, it will be understood that the grid can be placed at the center of an elongated beam 52 which can be connected at both ends to end walls of the surrounding trench 54, the exact shape and size of the grid and its supports being dependent on the degree of relative movement desired, and thus on the desired sensitivity of the accelerometer. It will be understood that a plurality of such movable structures can be provided in a single trench 54 or in a number of trenches on a single wafer, with each having selective characteristics which may be slightly different from each other to provide a wide range of sensitivity for the accelerometer device. As illustrated in Fig. 7, the beam 52 in grid 150 are covered by a metal layer such as the layer 44 provided in the process of Fig. 1 so that the metal on the side wall 156 of the grid cooperates with the metal on the side wall 158 of the mesa

154 to provide the opposed plates of a capacitor by means of which the motion of the grid with respect to the mesa can be detected or, conversely, by the application of a potential, the grid can be moved.

The mass of the accelerometer of Fig. 7 can be further increased by the addition of a layer of tungsten about 5 to 10μm thick over the surface of the grid. The process for adding such a layer of tungsten is outlined in the following Table IV:

TABLE IV

Step Number	Description
Steps 1-9	Same as Table I
10. PECVD Oxide	Deposit thin dielectric coating to prevent WSCVD
11. PECVD Silicon	Deposit seed layer for WSCVD
12. Photolithography	Pattern seed layer with thick resist · Vapor prime; spin, bake, long exposure, long decelopment & descum
13. SF_6 Isotropic RIE of aSi	Etch seed layer
14. Wet chemical resist strip & O_2 plasma	Remove residual resist
15. WSCVD	Tungsten Selective Chemical Vapor Deposition
16. Photolithography	Trim undesired tungsten with thick resist · Vapor prime; spin, bake, long exposure, long development & descum
17. Wet Chemical of W	Etch unwanted Tungsten
18. Wet Chemical resist strip & O_2 plasma	Remove residual resist

19. Metal Sputter Deposition (e.g. Al)	Same as Fig. 2
20. Wire Bond	Same as Fig. 2

As illustrated in Table IV and in Fig. 8A, the process of applying a tungsten layer is initiated after the release of the beams at step 9 illustrated in Fig. 1I. At that point in the process, the silicon beams 52 are covered on the top and side by oxide layers 12 and 28 and the beams are cantilevered over the floor 30 of deep silicon trenches 54. The undersides of the beams and the trench floors are film-free silicon. Since tungsten does not deposit on nonmetal surfaces, an attempt to apply tungsten to the structure at this point in the process would result in the tungsten growing only on the trench floor and on the beam undersides. To prevent that, a conformal dielectric coating such as PECVD oxide 160 (Fig. 8B) is deposited on the entire wafer. This layer 160 services as an etch stop for the seed layer patterning step, and prevents the tungsten from contacting the substrate underneath the beams and on the trench floor.

With the wafer lightly sealed off by the dielectric layer 160, a thin seed layer 162 of amorphous silicon (Fig. 8C, Step 11 of Table IV) is then deposited on the wafer, covering all surfaces. Because of the underlying dielectric layer 160, the silicon is electrically isolated from the substrate. A thick photoresist layer 164 is then applied to the wafer, filling the trench 54 and covering the grid 150 as well as the top of the mesa 154. The resist 164 is then exposed and

developed, as illustrated in Fig. 8E, which is a continuation of step 12, to remove the photoresist material from areas where tungsten is not desired. Thus, the photoresist material is removed from the mesa 154 and from one of the grid beams 52, the figure showing a beam 166 freed of the photoresist layer.

In Fig. 8E, removal of the seed layer 162 from the exposed beam 166 and from the exposed mesa 154 is illustrated. An isotropic SF_6 RIE removes the exposed layer 162 of silicon, with the oxide underlayer 160 serving as an etch stop. This exposed the dielectric layer 162 on beam 166 and mesa 154, as illustrated in Fig. 8F to prevent the growth of tungsten in these areas.

As illustrated in Fig. 8G, step 14 of Table IV, the resist 164 is next removed from the wafer to expose the grid 150, leaving the silicon layer 162 exposed on the beams indicated at 168 and 170 and on a portion of the floor 30 of trench 54. Thereafter, in step 15, illustrated in Fig. 8H, a tungsten selective CVD (WSCVD) is deposited, with deposition only occurring on the exposed metal layer 162 and being prevented on the oxide 160, thereby producing a tungsten layer 170 which is several microns thick on both the grid 150 and on the floor 30 where silicon is exposed. By depositing a thick layer of tungsten, a "blanket" is formed on top of the grid 150 and extends across the gaps between adjacent beams, as illustrated between beams 168 and 170 in Fig. 8H.

Since the process of tungsten deposition is not perfect, some tungsten will be deposited on the oxide layers 160, and therefore the same photolithographic process that was used to define

the area of the tungsten is used to re-expose the areas around the grid 150 and a quick wet-chemical tungsten etch is used to clean the oxide surfaces of the spurious tungsten. Thus, as illustrated in Fig. 8I, step 16, a photoresist layer 170 is applied to the wafer, again filling the trench 54 in the region of the mesa 154 and the beam 166. The resist 172 is exposed and developed as illustrated in step 17 to uncover the oxide layer 160 so that a wet chemical etch of the unwanted tungsten can be performed in those regions. The resist 172 is then stripped (Fig. 8K), leaving a blanket of tungsten 170 across the selected part of the grid 150, as illustrated. The blanket of tungsten covers a selected portion of the top of the grid and fills in the interbeam spaces to produce the thick conformal blanket.

After the tungsten has been deposited on the MEM device as described above, the remainder of the device is covered by the oxide coating 160, and accordingly, the standard SCREAM-I process can be continued by a sputter deposition of metal such as aluminum, in accordance with step 10 of Fig. 1J, to produce a metal coating 180 on the opposed sidewalls of grid 150 and mesa 154, as illustrated in Fig. 8L, and as discussed above with respect to Fig. 7.

As indicated above, the process of Fig. 1A through 1I can be used to fabricated a wide variety of structures. A grid structure has been discussed above with respect to Fig. 7, and Fig. 9, to which reference is now made, illustrates another example of such a grid structure fabricated using the process of Figures 1A through 1I. In this case, a complex grid 200 is

fabricated within a trench 202 and is secured between opposed trench walls 204 and 206 by means of axially aligned beams 208 and 210. The grid includes a plurality of longitudinal beams such as beams 212 and a plurality of cross beams such as beams 214. These beams are spaced apart to define spaced openings or apertures 216.

The grid 200 is fabricated for torsional motion, with the mounting beams 208 and 210 serving as micron-size torsion rods and the entire device being fabricated from single crystal silicon, as discussed above. As described with respect to Figs. 1A through 1I, a sequence of dielectric depositions and reactive ion etches are used to define and release the silicon beams 208, 210, 212 and 214 from the substrate silicon 218. To produce torsional motion, an electrode actuator scheme is provided in accordance with either Figures 10A through 10C or Figures 11A through 11C, both sets of figures being cross sectional views taken at 10-10 of Fig. 9. The processes illustrated in Figs. 10A through 10C and Figs. 11A through 11C differ in how the metal electrodes used in actuating the torsional resonator 200 are defined. In both cases, the electrodes are fabricated by an isotropic dry etch and the released structure is formed by an undercut-etch of the silicon beams. The grid 200 serves to increase the mass of the resonator, as discussed above, with respect to Fig. 7. When suitable potentials are applied across these electrodes, the resonator 200 rotates about the common axis of beams 208 and 210, as indicated by the arrows 220. The torsion beams 208 and 210 may be about 0.8μm wide and 2μm high, for example.

In accordance with the process of Figs. 10A through 10C, the trench 202 is etched in the substrate 218 with the surfaces covered by a mask oxide 222, in the manner illustrated in Fig. 1F. The bottom of the trench 202 is etched in the manner in Figs. 1G and 1H, and the beams 212 and released in the manner described with respect to Fig. 1I, leaving the beams spaced above the floor 224 of the trench. Thereafter, as illustrated in Fig. 10C, metal 226 is evaporated through the released structure to coat the top surface and side walls of the surrounding mesa and the beams 212, as previously discussed, and also providing metal on the bottom wall 224, as illustrated at 228 and 230 in Fig. 10C. Shadowing of the evaporated metal by the grid structure 200, and more particularly by beams 212 in Fig. 10C, produces a break 232 in the metal on floor 224 of the trench so that the metal area 228 lying between the grid 200 and side wall 234 of trench 202 (Fig. 9) is electrically isolated from the remaining metal on the floor of the trench. By extending the trench past the end wall 206 as indicated at 236 to a contact pad diagrammatically illustrated at 238, electrical connections can be made to the metal 228 to form an electrode. Similarly, the metal 226 on the grid 200 can also be electrically connected to a suitable pad, in the manner illustrated in Fig. 2, so that a potential can be applied between the metal on the grid 200 and the metal layer 228 on the floor of the trench.

A similar electrode structure is provided on the opposite side of grid 200, adjacent the side wall 240 (Fig. 9) with the electrode formed on the

floor of the trench adjacent wall 240 extending to a contact pad 242 for connection to suitable circuitry. Potentials provided between the grid 200 and either of the electrode adjacent wall 234 or the electrode adjacent wall 240 apply torsional forces to the grid 200, causing it to pivot about its mounting beams 208, 210, so that the grid twists in the direction of arrows 220, raising one lateral edge or the other out of the plane of substrate 218.

Figs. 11A through 11C provide an alternative electrode arrangement, but in this case a second masking step is required. As illustrated in Fig. 11A, the wafer is patterned to form islands 250 covered by an oxide layer 252 in the manner illustrated in Fig. 1F. A metal layer 254 is then applied to the entire top surface of the wafer and the metal is patterned to remove it from the floor of the trenches between the islands 250 and to partially remove the metal from the floor of the trench extending between the islands and the substrate side wall 256. Thereafter, the oxide layer 252 is removed from the floors of the trenches in the manner illustrated in Fig. 1G, and the silicon is etched in the manner described with respect to Fig. 1I to release the grid 200, and its corresponding beams 212 (Fig. 11C). This process leaves a side wall electrode on wall 256 with a horizontal lip 258 which extends toward the grid 200 and functions generally in the manner of the bottom electrode 228 described with respect to Fig. 10C.

In both of the structures of Figs. 10C and 11C, the metal coating on the grid is capacitively coupled with the corresponding electrode 228 or

258, respectively, to provide the necessary torsional force on grid 200. No additional external electrodes above the surface of the wafer are required to produce rotational motion out of the plane of the substrate. If desired, the grid 200 can be covered tungsten in the manner described with respect to Figures 8A through 8L to increase its mass. Furthermore, the tungsten can be mechanically polished to a flat surface so that the metal layer can act as a mirror, whereby rotation of the grid about the axes 208, 210 can provide accurate directional control of a reflected beam of light. Such a structure is illustrated in Fig. 12 wherein a tungsten layer 260 is shown as having a flat, polished top surface 262.

It is noted that the capacitive effect between the stationary electrodes on the substrate and the movable electrodes on the grid in the devices of Fig. 10C and 11C are dependent upon the spacing between the grids as well as upon the potential applied between the electrodes. In accordance with the process of the present invention, this spacing can be in the range of 5μm so that this capacitant is more significant than any capacitance that exists between the grid and the ground plane of the substrate beneath the grid, thereby allowing the potential across the capacitive plates to control the motion of the grid.

Although tungsten is preferred as the coating for the grid, as illustrated in Figs. 8L and 12, it will be understood that a dielectric such as nitride or oxide can be used as a membrane on a grid structure such as that illustrated in Fig. 7,

or even on the structure of Fig. 9, for use in pressure sensing or like applications.

Although the foregoing illustrations have all been directed to essentially rectangular beam structures, it will be understood that the photolithographic process described above can be used to fabricate any desired shape. Examples of such shapes are illustrated in Fig. 13, wherein a pair of spiral beams 270 and 272 are fabricated in a trench 274 formed in a substrate, or wafer 276. The spiral shape of the beam structures is produced in the photolithographic step, and the resulting beam is coated by a dielectric and by a metal layer in the manner illustrated in Figs. 1A through 1J. One end of the spiral is connected to a side wall 278 of the cavity 274 and the metal is connected to a contact pad diagrammatically illustrated at 280 on the substrate 276. In similar manner, one end of the second spiral 272 is connected to wall 78, for example, with its metal layer connected to a contact pad 282.

To connect the opposite end of the spiral to an electrode so that each spiral can form an inductor, the free end 284 and 286 of spirals 270 and 272, respectively, are connected by way of dielectric bridges 288 and 290, respectively, to the opposite side wall 292, for example, of trench 274. This dielectric bridge extends across the intervening spiral portions of the respective beams to provide supports and electrical isolation for subsequent deposition of electrodes 294 and 26, respectively, which extends to pads at the edge of the wafer for electrical connection to the spiral beams. In this way, microelectromechanical inductors can be fabricated in accordance with the

invention, with the adjacent inductors 270 and 272 forming a microtransformer, if desired. If desired, metal electrodes can be deposited on the floor of the trench 274 beneath one or both of the spiral beams so that a potential can be applied between the electrodes on the beams and on the floor to provide capacitive control of vertical motion of the beam. Such a variation in the position of one spiral with respect to the other changes the inductive relationship between the two to thereby provide a variable transformer. Similarly, electrodes on the side walls of the trench 274, such as side wall 278, permit a capacitive connection with electrodes on the side walls of the spirals 270 and 272 to permit lateral motion of the spirals to thereby change the spacing between adjacent coils and change the inductance of the beams.

In summary, the present invention is directed to a silicon process for fabricating single crystal silicon MEM devices utilizing a single mask to define all components. The process is low temperature, self-aligned, and independent of crystal orientation, and relies on industry standard fabrication processes and tools. The process can be used to produce discrete devices on wafers, or can be used in combination with VLSI integrated circuit processes without major modification of the IC processes because of its low temperature requirements, simple design rules, and short process times. The low temperatures used in the present process do not adversely affect existing IC circuits, so MEM devices can be fabricated on completed IC wafers. The device as an important application has an accelerometer,

allowing such devices to be incorporated in integrated circuits, for example, or fabricated on discrete wafers for use in a wide range of applications, with a tungsten process being provided to increase the mask of the MEM device for such applications.

Although the invention has been described in terms of preferred embodiments, it will be apparent to those of skill in the art that numerous variations and modifications may be made without departing from the true spirit and scope thereof, as set forth in the following claims:

WHAT IS CLAIMED IS:

1. A single-mask, low temperature reactive ion etching process for fabricating high aspect ratio, submicron, released single crystal microelectromechanical structures independently of crystal orientation, comprising:

forming a mask dielectric layer on a top surface of a single crystal substrate;

patterning said mask layer to produce a dielectric mask defining a structure of arbitrary shape to be formed in and surrounded by said substrate, said shape being independent of crystal orientation in said substrate and including at least a beam portion to be released;

etching said substrate through the pattern defined by said mask to produce corresponding deep trenches in said substrate surrounding the defined structure of arbitrary shape, said structure having a top surface covered by said oxide mask and having substantially vertical side walls;

forming a dielectric layer on said structure side walls, on the floor of said trenches, and on said dielectric mask;

removing the dielectric layer from the floor of said trenches to expose said single crystal substrate while leaving said mask and said side wall dielectric substantially intact;

releasing at least said beam portion by reactive ion etching said exposed single crystal substrate in said trenches; and

coating said defined structure and surrounding substrate with a metal layer, the metal on said defined structure being electrically isolated from the metal on the surrounding substrate by said trenches.

2. The process of claim 1, wherein the step of etching and exposed single crystal substrate includes anisotropically etching said substrate.

3. The process of claim 1, further including reactive ion etching said exposed single crystal substrate at the bottom of said trenches to deepen them prior to said releasing step.

4. The process of claim 3, wherein the step of releasing said beam portion includes isotropically etching said substrate in a high pressure, low power reactive ion etch.

5. The process of claim 4, wherein the step of coating said defined structure and surrounding substrate with a metal layer includes depositing metal at least on said top surface mask and on said side wall dielectric of said defined structure and surrounding substrate, and on the bottom of said trench.

6. The process of claim 5, wherein the step of isotropically etching said substrate includes undercutting said surrounding substrate to prevent continuous deposition of metal between said sidewalls and the bottom of said trenches.

7. The process of claim 1, further including reducing the lateral spring constant of a released beam portion of said structure.

8. The process of claim 7, wherein the step of reducing the lateral spring constant includes removing said metal layer and said sidewall dielectric from a selected portion of the sidewall of a beam.

9. The process of claim 1, further including increasing the mass of a selected released beam portion.

10. The process of claim 9, wherein the step of increasing the mass of a selected released beam portion includes defining the shape of a segment of said beam portion to have increased dimensions.

11. The process of claim 10, wherein the step of increasing the mass of a selected released beam portion includes depositing a blanket of metal on said portion of increased dimensions.

12. The process of claim 1, further including electrically connecting said metal layer on said defined structure to an electrical circuit element.

13. The process of claim 1 wherein the step of defining a structure of arbitrary shape further includes defining an electrical contact pad and an interconnect between said contact pad and said released beam portion.

14. The process of claim 1, wherein the step of forming a mask layer on a substrate includes:

providing a substrate wafer containing integrated circuit components including at least a contact pad covered by a passivation layer, wherein the step of forming a mask layer includes treating said passivation layer on said wafer in a region adjacent said integrated circuit components to produce a dielectric mask layer.

15. The method of claim 14, further including, before coating said defined structure and surrounding substrate with a metal layer, the step of opening a via window through said mask layer to said integrated circuit contact pad, whereby said metal layer contacts said contact pad.

16. The method of claim 15, further including patterning and etching said metal layer

to define a metal interconnect between said released beam portion and said contact pad.

17. The method of claim 1, wherein the step of patterning said mask includes defining a beam portion including a grid mounted on said surrounding substrate by axial arms.

18. The method of claim 17, wherein the step of coating includes applying a metal coating to a portion of said trench floor adjacent said released beam portion grid to provide capacitive coupling to said beam grid for producing torsional motion thereof.

19. The method of claim 18, further including depositing a blanket of material on said released beam portion grid.

20. The method of claim 18, further including depositing a blanket of tungsten on said released beam portion grid.

21. The method of claim 1, wherein the step of patterning said mask includes defining electrode means adjacent said beam portion to be released, and wherein the step of coating includes providing capacitor plates on said released beam portion and an adjacent electrode means to provide capacitive coupling therebetween.

22. The method of claim 21, wherein the step of patterning said mask includes defining contact pad means in said substrate and connector means between said released beam portion, said electrode means and corresponding contact pad means.

23. The method of claim 1, wherein the step of patterning said mask includes defining a beam portion as an inductive coil.

24. The method of claim 1, wherein the step of forming a mask dielectric layer includes depositing a PECVD oxide layer.

25. The method of claim 1, wherein the step of forming a mask dielectric layer includes depositing a nitride layer.

26. The method of claim 1, wherein said substrate is single crystal silicon, and wherein the step of releasing said beam portion includes SF_6 reactive ion etching.

27. The method of claim 1, wherein said substrate is gallium arsenide and wherein the step of releasing said beam portion includes BCl_3 reactive ion etching.

28. A microelectromechanical structure fabricated in a single crystal substrate independently of crystal orientation by a low temperature, single mask process, comprising:

a single crystal wafer having a top surface;

trench means in the surface of said wafer defining a released beam spaced from a surrounding substrate, said beam being movable with respect to said substrate; and

an electrically conductive coating on said released beam and on said substrate, said trench means electrically isolating the coating on said beam from the coating on said substrate.

29. The device of claim 28, further including means for producing a potential difference between said trench coating and said substrate coating for producing motion of said beam in the plane of said top surface.

30. The device of claim 28, further including contact pad means and interconnect means extending between said beam and said contact pad

in the surface of said wafer, said contact pad and interconnect means being defined by said trench means.

31. The device of claim 30, wherein said electrically conductive coating is on said interconnect means and said contact pad means and is electrically isolated from said substrate coating by said trench means.

32. The device of claim 30, further including electrode means and corresponding contact pad and interconnect means in the top surface of said wafer, said electrode means having an electrically conductive coating and being electrically isolated from said beam means by said trench means to provide capacitive coupling between said released beam and said electrode means.

33. The device of claim 30, wherein said released beam comprises an elongated, cantilevered arm.

34. The device of claim 33, wherein said released beam further comprises enlarged grid means carried by said arm.

35. The device of claim 34, further including means carried by said grid for increasing the mass thereof.

36. The device of claim 34, further including a membrane carried by said grid.

37. The device of claim 34, further including electrode means in said trench adjacent at least one edge of said grid and positioned to provide capacitive coupling between said grid and said electrode means to produce torsional motion of said grid about said cantilevered arm.

AMENDED CLAIMS

[received by the International Bureau on 19 April 1994 (19.04.94);
original claims 2,3,5 and 6 amended;
new claims 38-49 added;
remaining claims unchanged (9 pages)]

1. A single-mask, low temperature reactive ion etching process for fabricating high aspect ratio, submicron, released single crystal microelectromechanical structures independently of crystal orientation, comprising:

forming a mask dielectric layer on a top surface of a single crystal substrate;

patterning said mask layer to produce a dielectric mask defining a structure of arbitrary shape to be formed in and surrounded by said substrate, said shape being independent of crystal orientation in said substrate and including at least a beam portion to be released;

etching said substrate through the pattern defined by said mask to produce corresponding deep trenches in said substrate surrounding the defined structure of arbitrary shape, said structure having a top surface covered by said oxide mask and having substantially vertical side walls;

forming a dielectric layer on said structure side walls, on the floor of said trenches, and on said dielectric mask;

removing the dielectric layer from the floor of said trenches to expose said single crystal substrate while leaving said mask and said side wall dielectric substantially intact;

releasing at least said beam portion by reactive ion etching said exposed single crystal substrate in said trenches; and

coating said defined structure and surrounding substrate with a metal layer, the metal on said defined structure being electrically isolated from the metal on the surrounding substrate by said trenches.

2. The process of claim 1, wherein the step of releasing said beam portion by etching said exposed single crystal substrate includes partially undercutting said surrounding substrate and thereby producing electrically isolating breaks in said metal layer.

3. The process of claim 1, further including reactive ion etching said exposed single crystal substrate at the floor of said trenches to deepen them prior to said releasing step.

4. The process of claim 3, wherein the step of releasing said beam portion includes isotropically etching said substrate in a high pressure, low power reactive ion etch.

5. The process of claim 4, wherein the step of coating said defined structure and surrounding substrate with a metal layer includes depositing metal at least on said top surface mask and on said side wall dielectric of said defined structure and surrounding substrate, and on the floor of said trench.

6. The process of claim 5, wherein the step of isotropically etching said substrate includes undercutting said surrounding substrate to prevent continuous deposition of metal between said sidewalls and the floor of said trenches.

7. The process of claim 1, further including reducing the lateral spring constant of a released beam portion of said structure.

8. The process of claim 7, wherein the step of reducing the lateral spring constant includes removing said metal layer and said sidewall dielectric from a selected portion of the sidewall of a beam.

9. The process of claim 1, further including increasing the mass of a selected released beam portion.

10. The process of claim 9, wherein the step of increasing the mass of a selected released beam portion includes defining the shape of a segment of said beam portion to have increased dimensions.

11. The process of claim 10, wherein the step of increasing the mass of a selected released beam portion includes depositing a blanket of metal on said portion of increased dimensions.

12. The process of claim 1, further including electrically connecting said metal layer on said defined structure to an electrical circuit element.

13. The process of claim 1 wherein the step of defining a structure of arbitrary shape further includes defining an electrical contact pad and an interconnect between said contact pad and said released beam portion.

14. The process of claim 1, wherein the step of forming a mask layer on a substrate includes:

providing a substrate wafer containing integrated circuit components including at least a contact pad covered by a passivation layer, wherein the step of forming a mask layer includes treating said passivation layer on said wafer in a region adjacent said integrated circuit components to produce a dielectric mask layer.

15. The method of claim 14, further including, before coating said defined structure and surrounding substrate with a metal layer, the step of opening a via window through said mask layer to said integrated circuit contact pad,

whereby said metal layer contacts said contact pad.

16. The method of claim 15, further including patterning and etching said metal layer to define a metal interconnect between said released beam portion and said contact pad.

17. The method of claim 1, wherein the step of patterning said mask includes defining a beam portion including a grid mounted on said surrounding substrate by axial arms.

18. The method of claim 17, wherein the step of coating includes applying a metal coating to a portion of said trench floor adjacent said released beam portion grid to provide capacitive coupling to said beam grid for producing torsional motion thereof.

19. The method of claim 18, further including depositing a blanket of material on said released beam portion grid.

20. The method of claim 18, further including depositing a blanket of tungsten on said released beam portion grid.

21. The method of claim 1, wherein the step of patterning said mask includes defining electrode means adjacent said beam portion to be released, and wherein the step of coating includes providing capacitor plates on said released beam portion and an adjacent electrode means to provide capacitive coupling therebetween.

22. The method of claim 21, wherein the step of patterning said mask includes defining contact pad means in said substrate and connector means between said released beam portion, said electrode means and corresponding contact pad means.

23. The method of claim 1, wherein the step of patterning said mask includes defining a beam portion as an inductive coil.

24. The method of claim 1, wherein the step of forming a mask dielectric layer includes depositing a PECVD oxide layer.

25. The method of claim 1, wherein the step of forming a mask dielectric layer includes depositing a nitride layer.

26. The method of claim 1, wherein said substrate is single crystal silicon, and wherein the step of releasing said beam portion includes SF_6 reactive ion etching.

27. The method of claim 1, wherein said substrate is gallium arsenide and wherein the step of releasing said beam portion includes BCl_3 reactive ion etching.

28. A microelectromechanical structure fabricated in a single crystal substrate independently of crystal orientation by a low temperature, single mask process, comprising:

a single crystal wafer having a top surface;

trench means in the surface of said wafer defining a released beam spaced from a surrounding substrate, said beam being movable with respect to said substrate; and

an electrically conductive coating on said released beam and on said substrate, said trench means electrically isolating the coating on said beam from the coating on said substrate.

29. The device of claim 28, further including means for producing a potential difference between said trench coating and said substrate coating for producing motion of said beam in the plane of said top surface.

30. The device of claim 28, further including contact pad means and interconnect means extending between said beam and said contact pad in the surface of said wafer, said contact pad and interconnect means being defined by said trench means.

31. The device of claim 30, wherein said electrically conductive coating is on said interconnect means and said contact pad means and is electrically isolated from said substrate coating by said trench means.

32. The device of claim 30, further including electrode means and corresponding contact pad and interconnect means in the top surface of said wafer, said electrode means having an electrically conductive coating and being electrically isolated from said beam means by said trench means to provide capacitive coupling between said released beam and said electrode means.

33. The device of claim 30, wherein said released beam comprises an elongated, cantilevered arm.

34. The device of claim 33, wherein said released beam further comprises enlarged grid means carried by said arm.

35. The device of claim 34, further including means carried by said grid for increasing the mass thereof.

36. The device of claim 34, further including a membrane carried by said grid.

37. The device of claim 34, further including electrode means in said trench adjacent at least one edge of said grid and positioned to provide capacitive coupling between said grid and

said electrode means to produce torsional motion of said grid about said cantilevered arm.

38. The process of claim 2, wherein the step of producing said electrically isolating breaks in said metal layer forms a complete structure electrically isolated from the surrounding substrate with the metal layer being electrically insulated from the single crystal substrate.

39. The process of claim 38, wherein the step of releasing said beam includes increasing the depth of said trenches to produce an enlarged cavity in said substrate to reduce electric current leakage.

40. The process of claim 1, wherein the step of forming a mask dielectric layer on a single crystal substrate includes forming a silicon dioxide layer on a single crystal silicon substrate.

41. A single-mask, low temperature process for fabricating high aspect ratio, submicron, released microelectromechanical structures comprising:

forming a mask dielectric layer on a substantially horizontal top surface of an etchable substrate;

patterning said mask layer to produce a single dielectric mask defining a structure of arbitrary shape to be formed in and surrounded by said substrate, said shape being independent of crystal orientation in said substrate and including at least a beam portion to be released for movement with respect to said substrate;

etching said substrate through the pattern defined by said dielectric mask to produce a corresponding deep trench having substantially

vertical side walls and a substantially horizontal floor in said substrate and surrounding the defined structure of arbitrary shape, said defined structure having a top surface covered by said dielectric mask;

forming a second dielectric layer on said side walls, on the floor of said trench, and on said dielectric mask;

removing said second dielectric layer from the dielectric mask and from the floor of said trench to expose the substrate at said floor while leaving said dielectric mask and said side wall dielectric layer substantially intact;

releasing at least said beam portion of said defined structure by etching said exposed substrate at the floor of said trench, the etching completely undercutting said beam portion to free it for motion with respect to said substrate and partially undercutting said surrounding substrate; and

thereafter coating said defined structure and surrounding substrate with a metal layer, the metal on said defined structure being electrically isolated from the metal on the surrounding substrate by said trench and said undercutting of said surrounding substrate.

42. The process of claim 41, wherein the step of forming a mask dielectric layer on an etchable substrate includes forming an oxide mask on a silicon substrate.

43. The process of claim 41, further including the step of etching the floor of said trench to expire substrate beneath said beam portions prior to releasing said beam portion.

44. The process of claim 41, wherein the step of coating includes depositing a layer of metal on at least said dielectric mask, said side wall dielectric layer.

45. The process of claim 41, wherein the step of forming mask dielectric layer on an etchable substrate includes depositing an oxide layer on a single crystal silicon substrate.

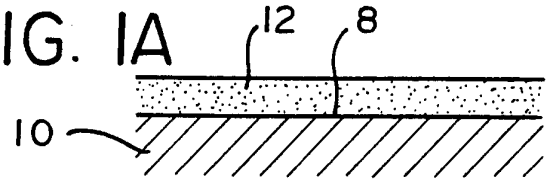
46. The process of claim 41, further including depositing a further layer on at least a part of said defined structure to increase its mass.

47. The process of claim 41, further including selectively electrically connecting said metal layer on said defined structure to said metal layer on said surrounding substrate.

48. The process of claim 41, wherein the step of patterning said mask layer includes defining a structure of arbitrary shape having at least a beam portion, an electrical contact pad portion, and an interconnect therebetween.

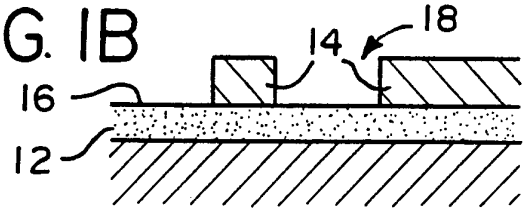
49. The process of claim 48, further including selectively electrically connecting said metal layer on said contact pad portion to said metal layer on said surrounding substrate.

FIG. IA



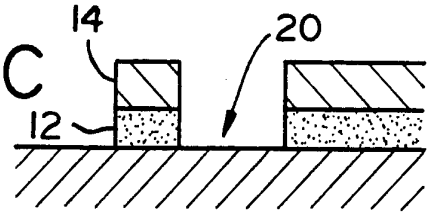
Step 1: Deposit Mask Oxide
Mask Oxide
Silicon Substrate

FIG. IB



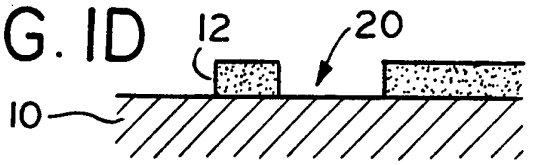
Step 2: Photolithography
Exposed Photoresist
Mask Oxide
Silicon Substrate

FIG. IC



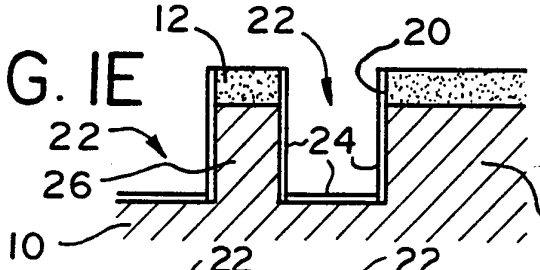
Step 3: Transfer Pattern
Resist
Mask Oxide
Silicon Substrate

FIG. ID



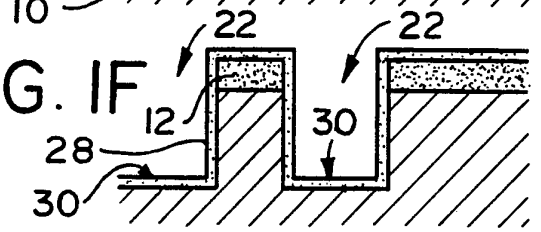
Step 4: Strip Resist
Mask Oxide
Silicon Substrate

FIG. IE



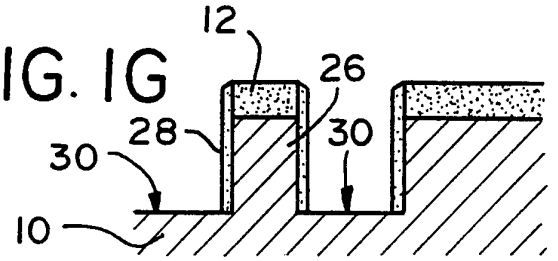
Step 5: Deep Silicon Etch
Mask Oxide
Silicon Substrate

FIG. IF



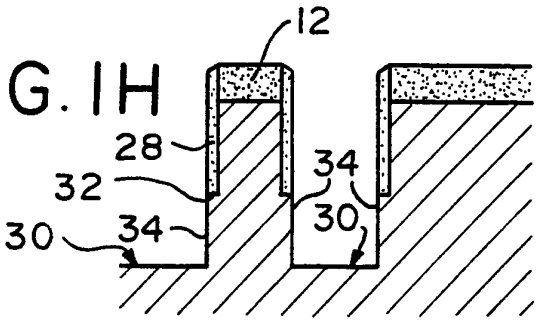
Step 6: Deposit PECVD Oxide
Sidewall Oxide
Mask Oxide
Silicon Substrate

FIG. IG



Step 7: Vertical Oxide Etch
Mask Oxide
Silicon Substrate

FIG. IH



Step 8: Silicon Etch #2
Mask Oxide
Silicon Substrate

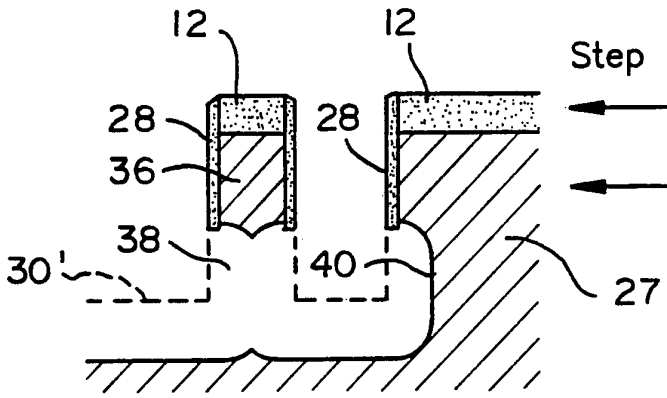


FIG. 11

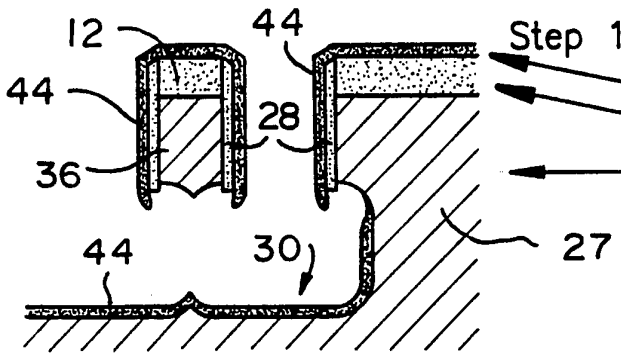


FIG. 1J

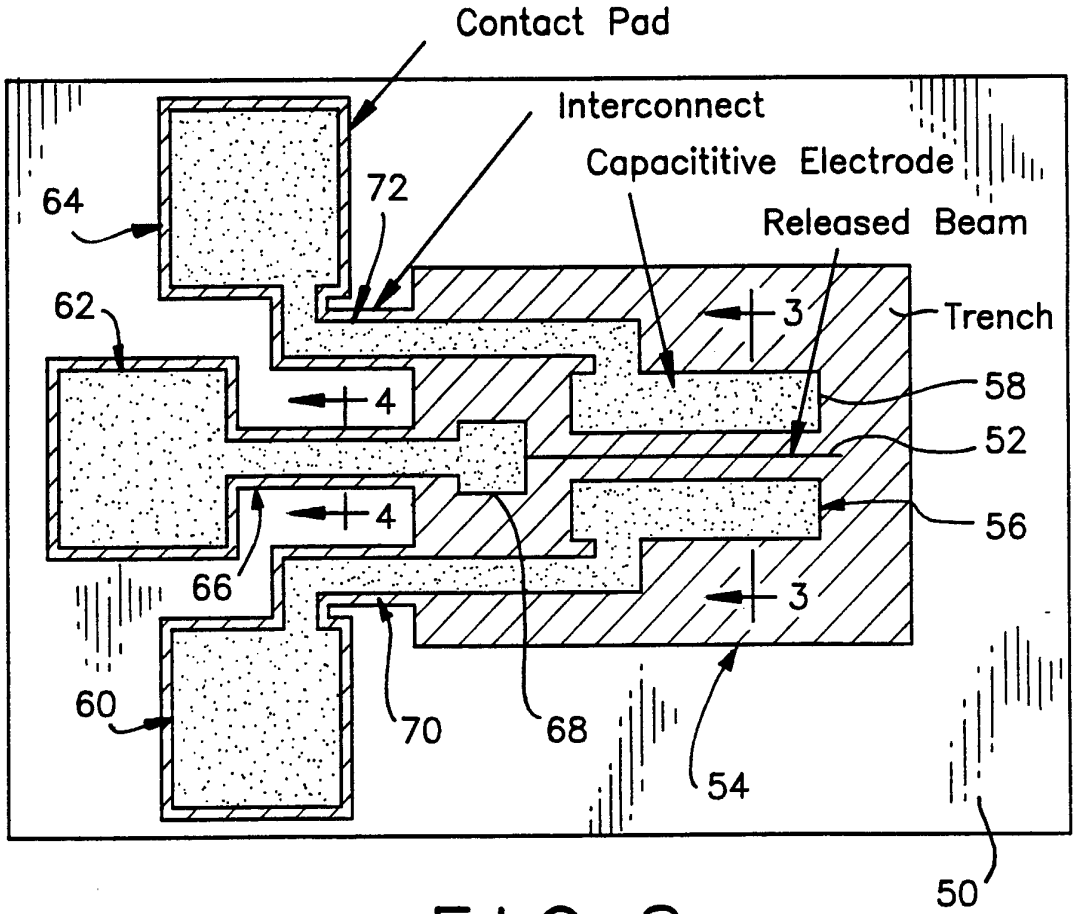
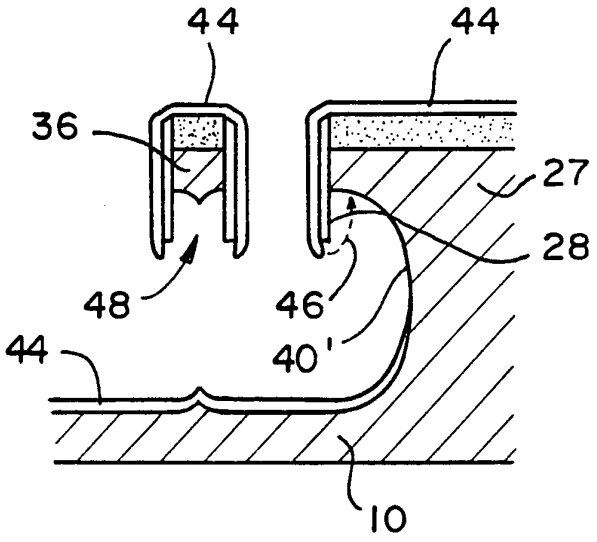


FIG. 2



Step 9 (modified) and Step 10

FIG. 1K
(optional)

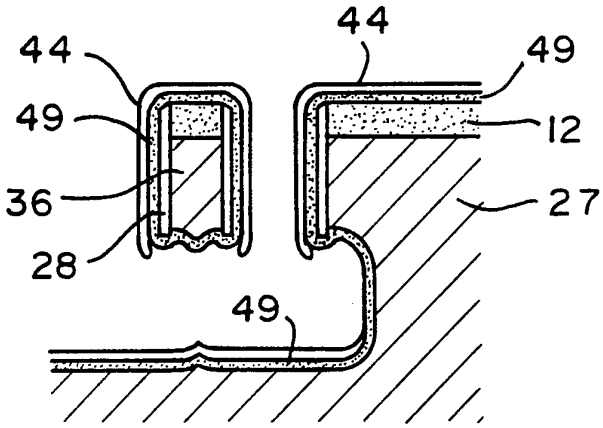


FIG. 1L
(optional)

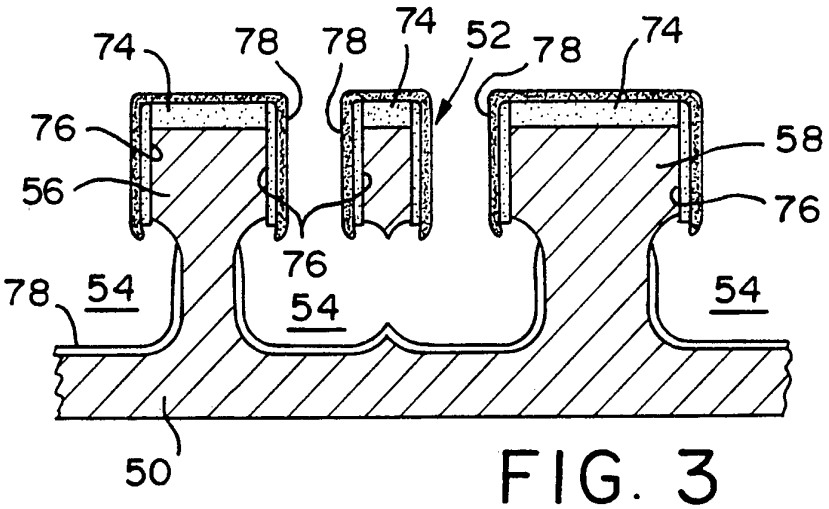


FIG. 3

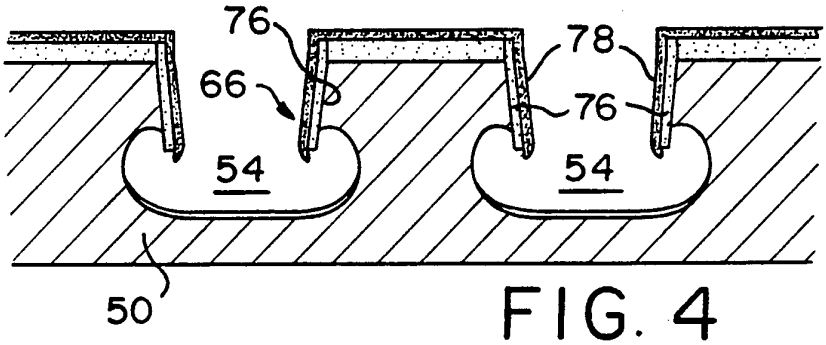


FIG. 4

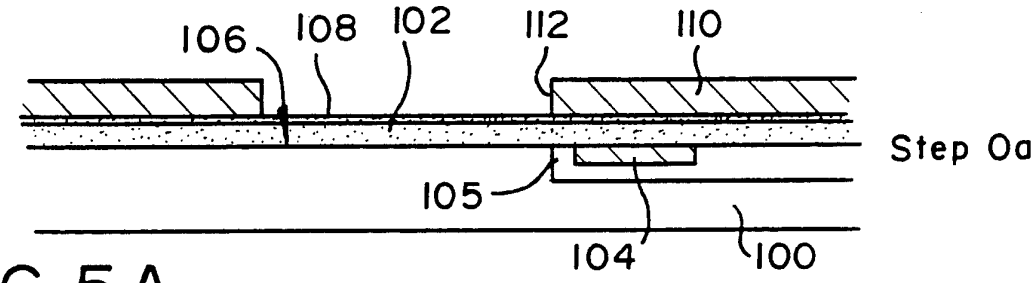


FIG. 5A

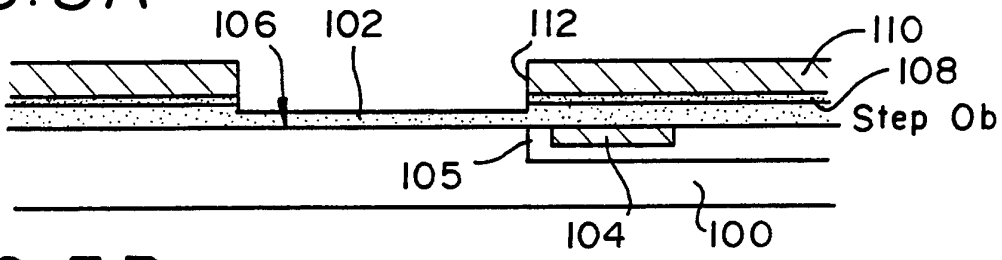


FIG. 5B

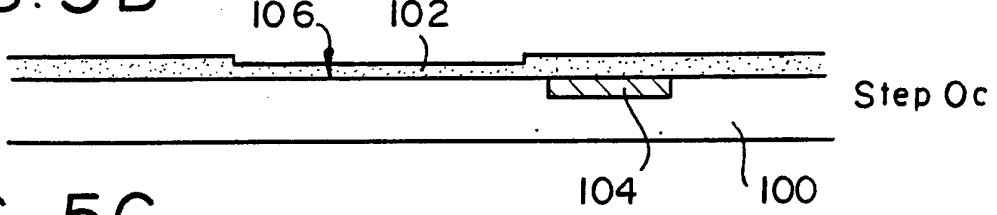


FIG. 5C

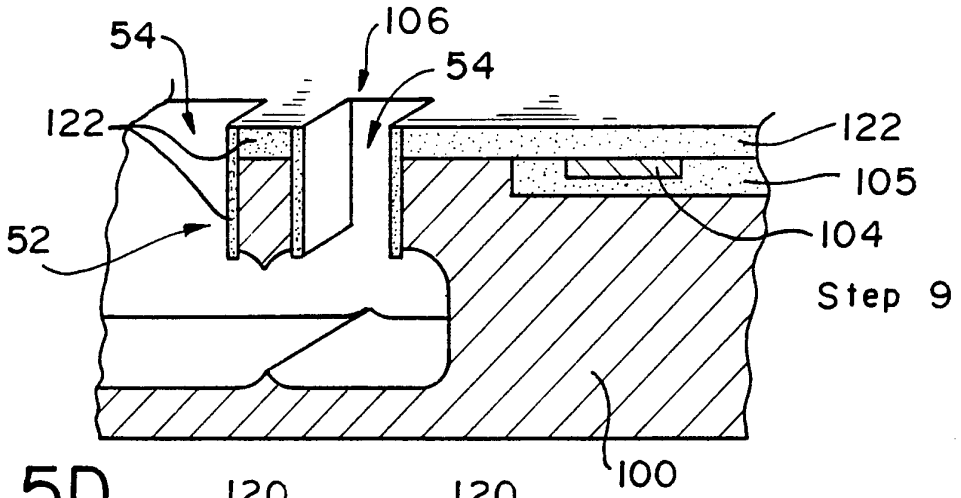


FIG. 5D

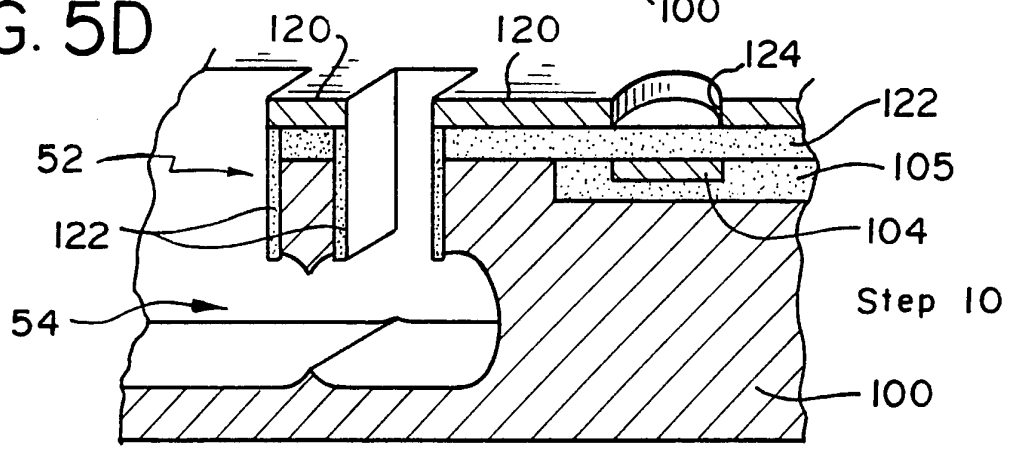


FIG. 5E

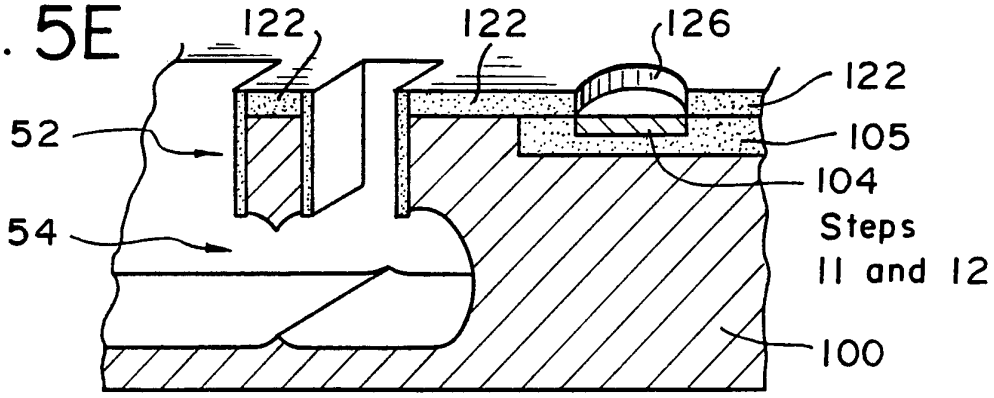


FIG. 5F

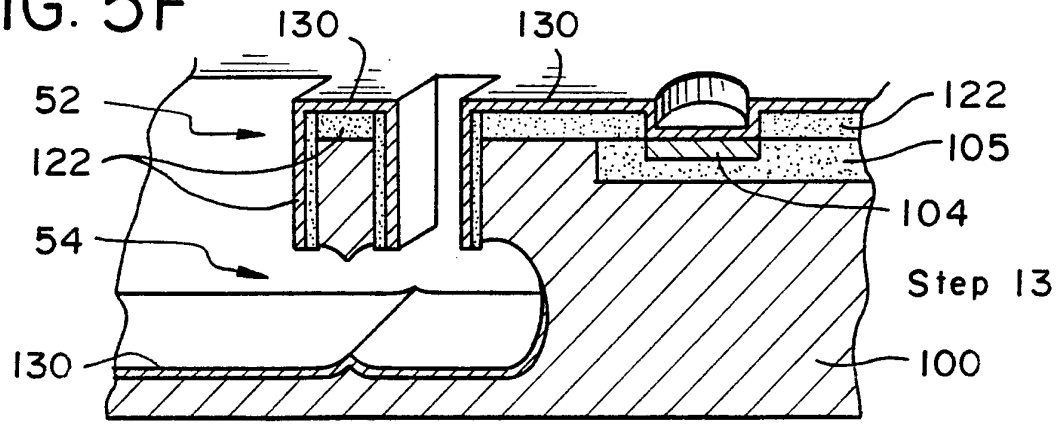


FIG. 5G

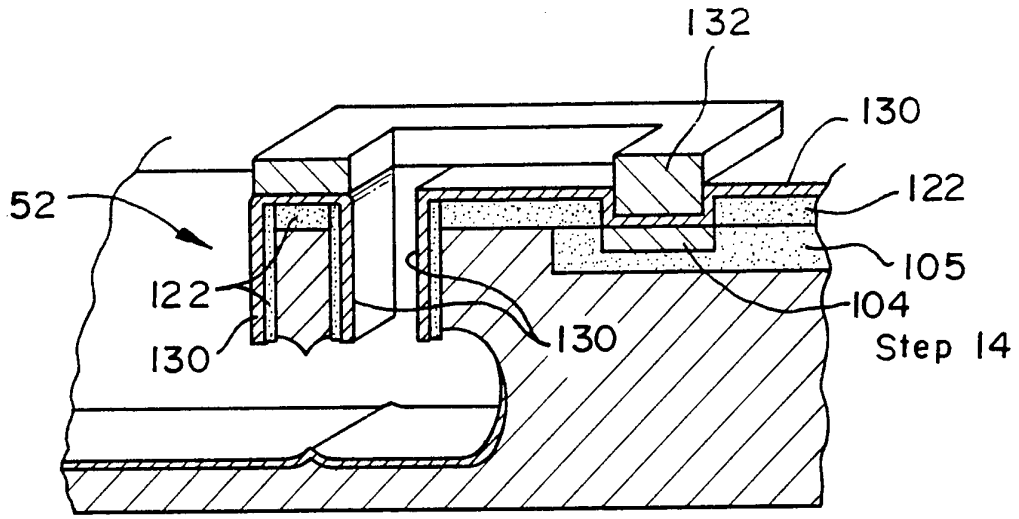


FIG. 5H

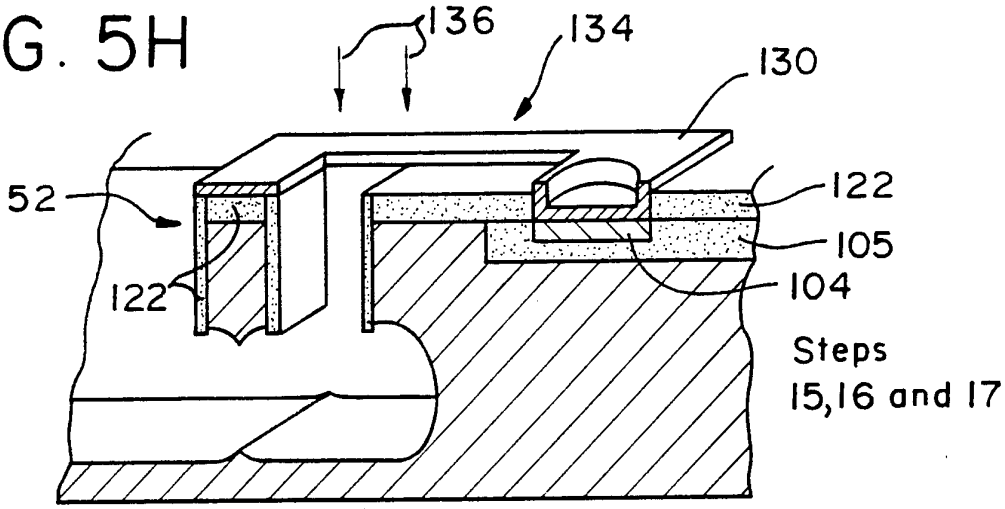


FIG. 5I

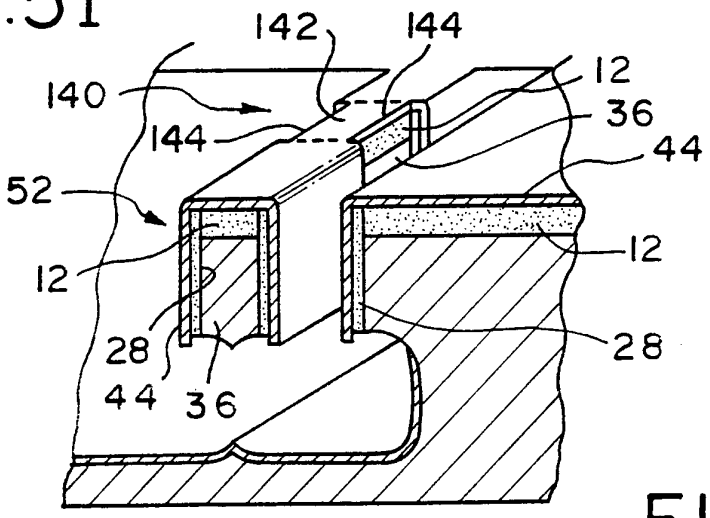
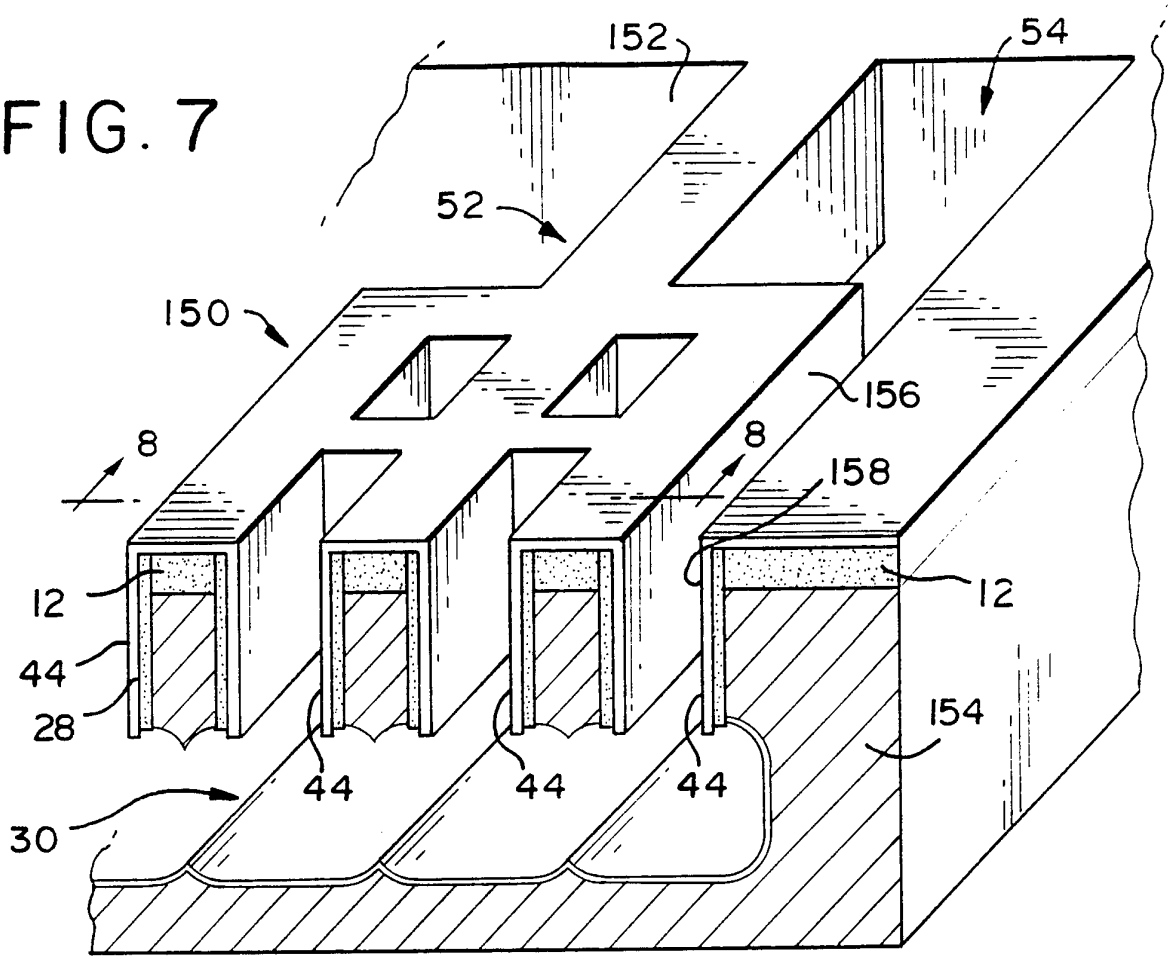


FIG. 6

FIG. 7



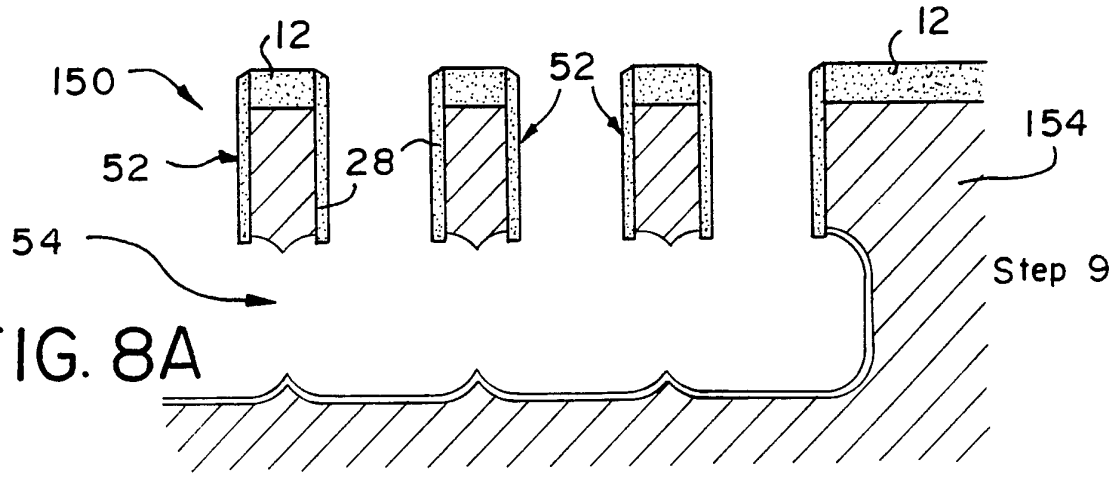


FIG. 8A

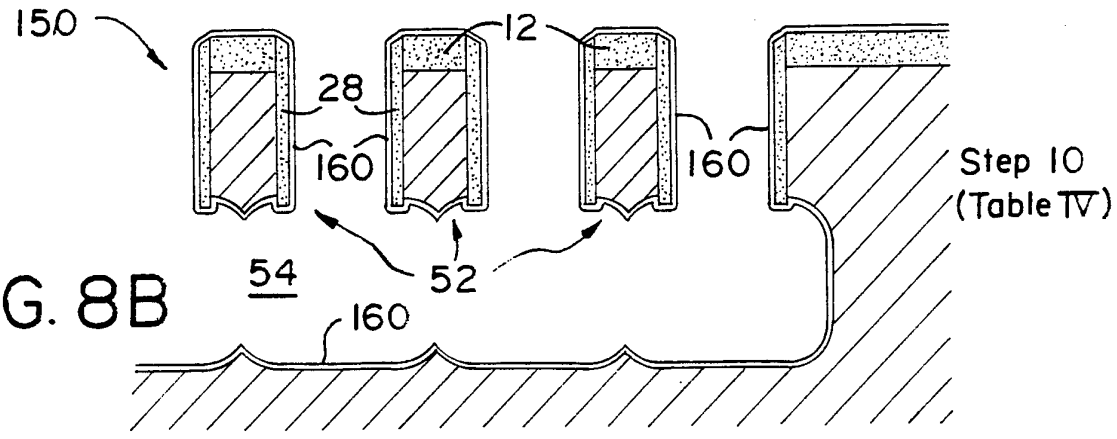


FIG. 8B

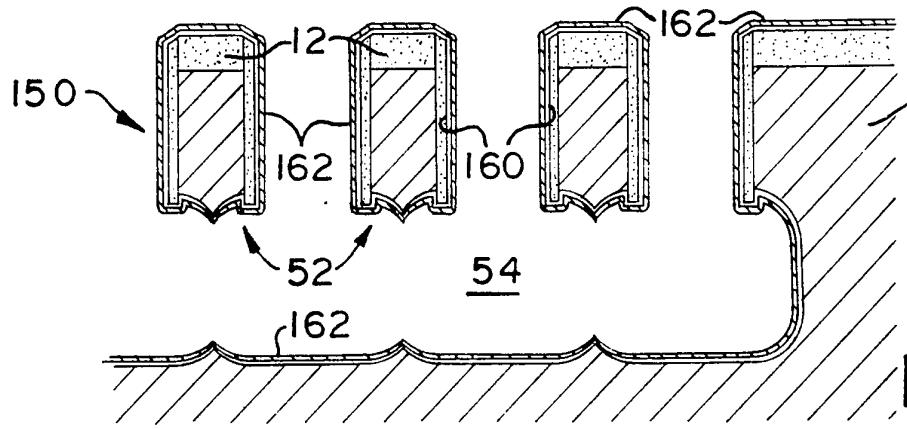


FIG. 8C

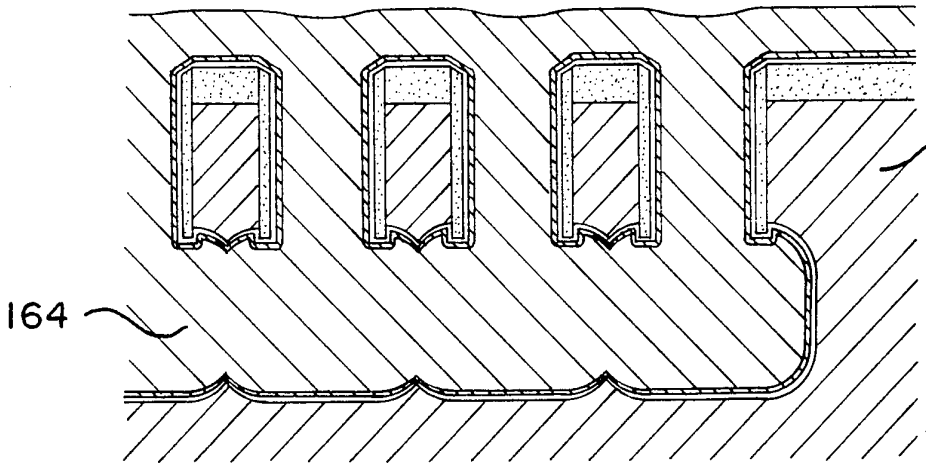


FIG. 8D

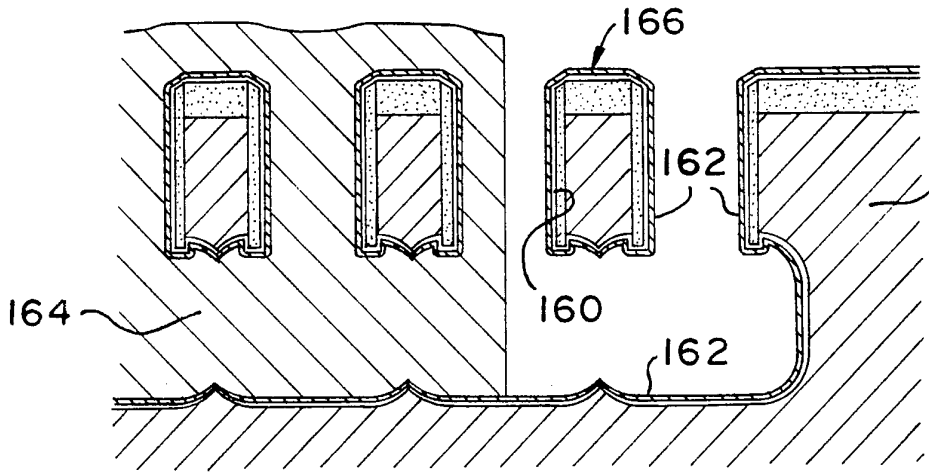


FIG. 8E

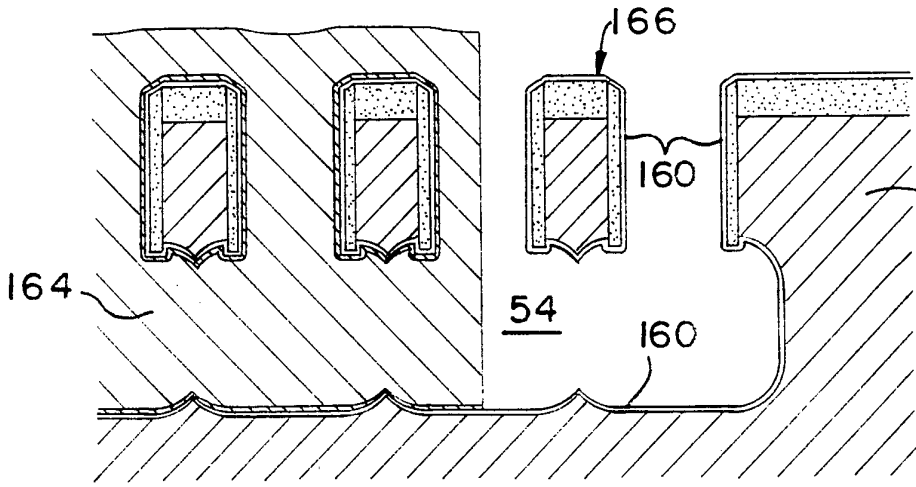


FIG. 8F

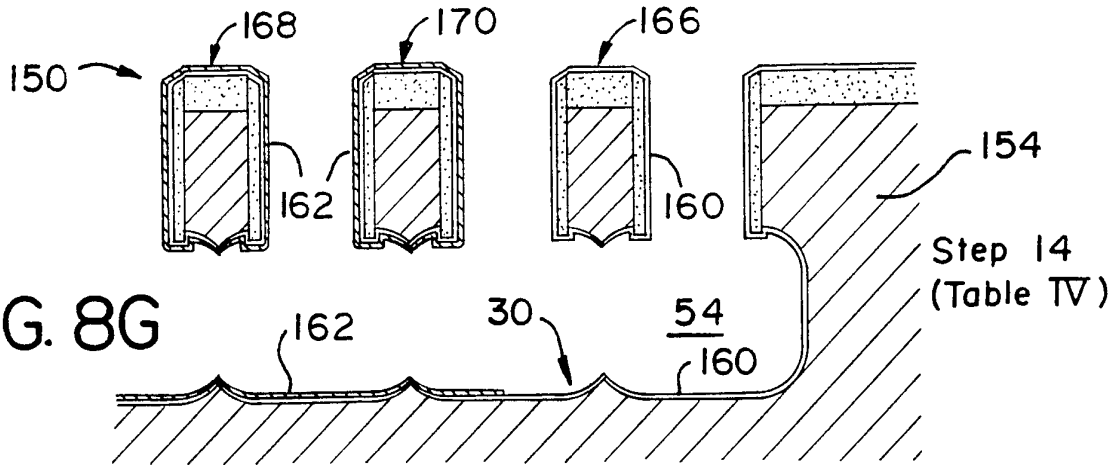


FIG. 8G

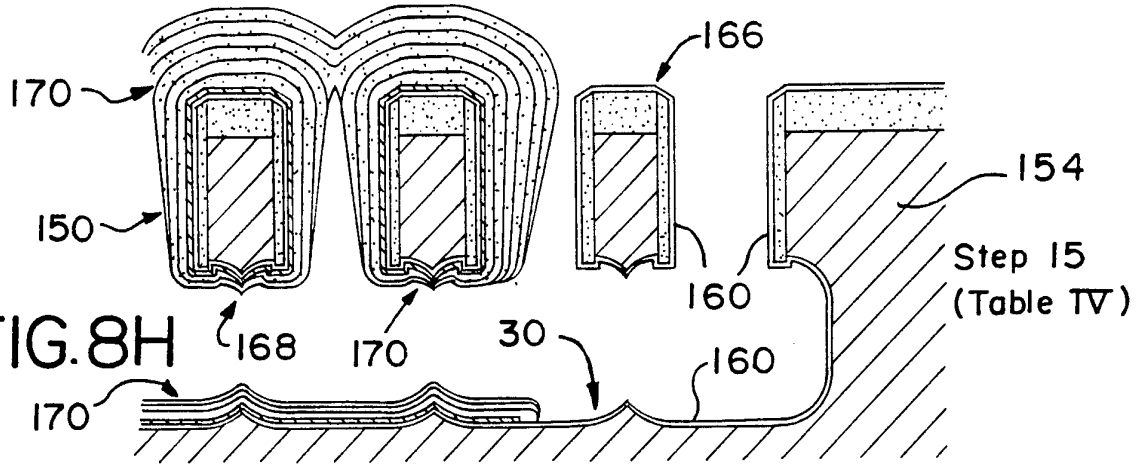


FIG. 8H

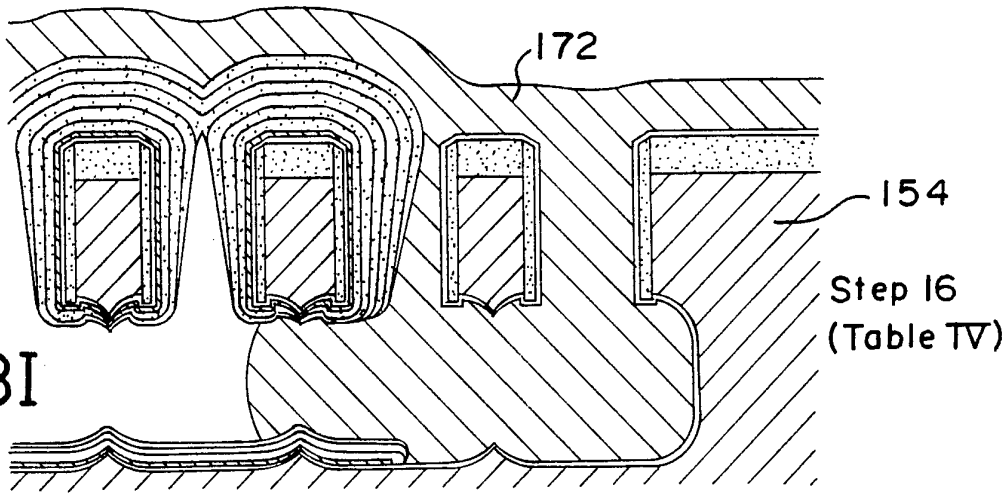


FIG. 8I

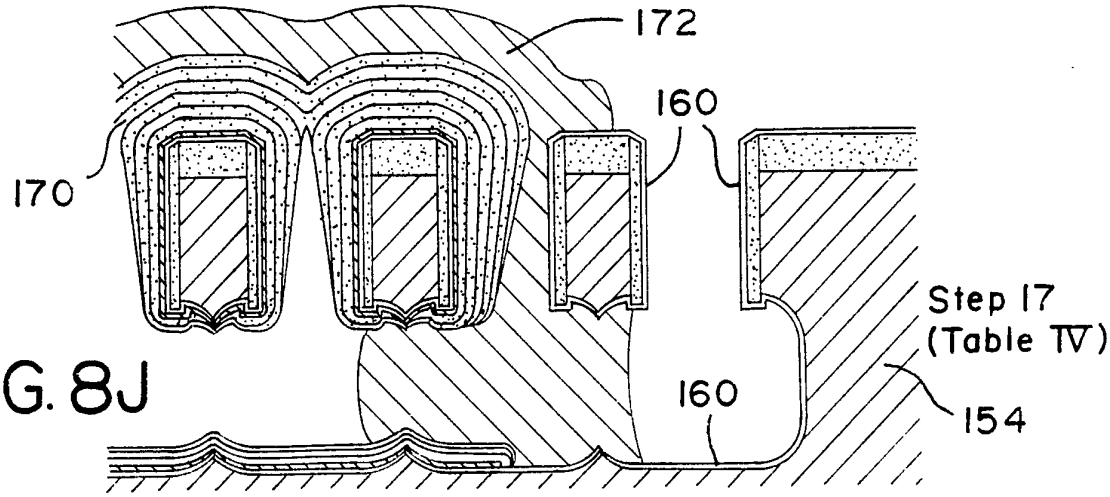


FIG. 8J

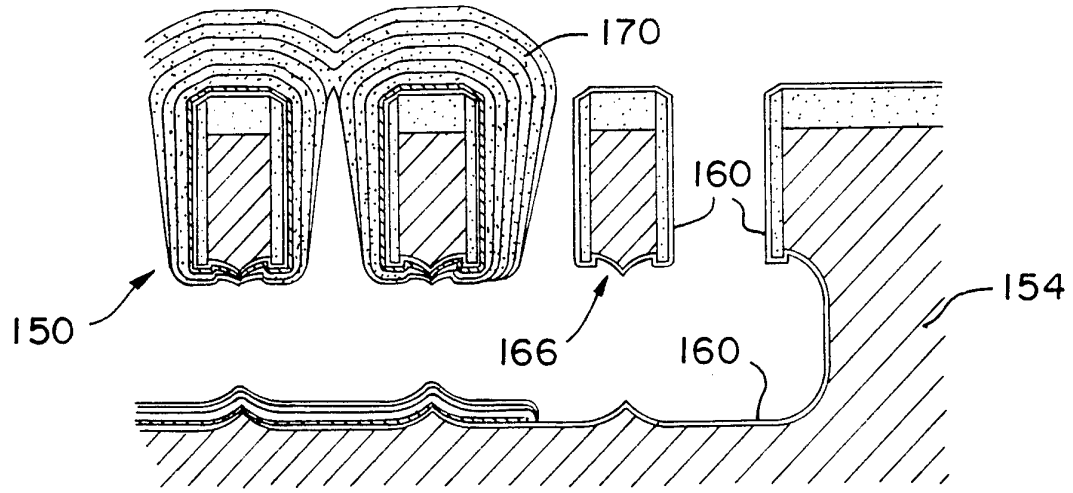


FIG. 8K

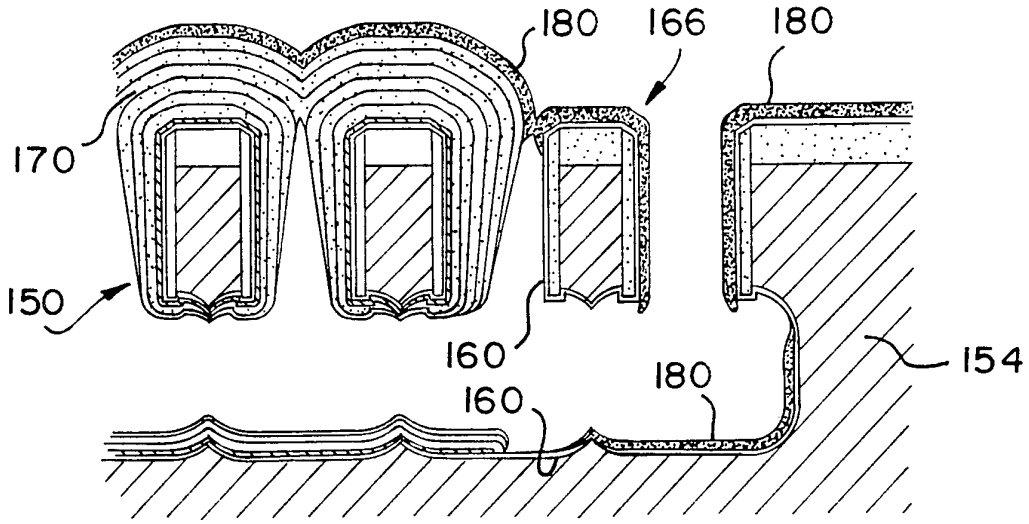


FIG. 8L

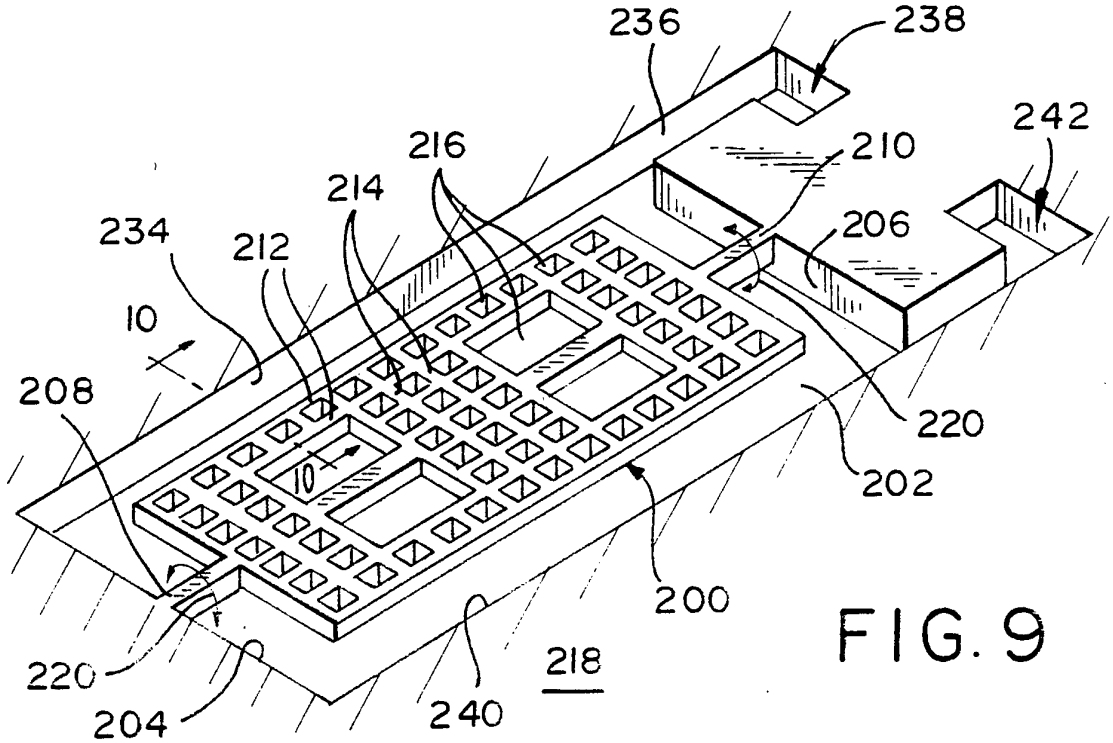


FIG. 9

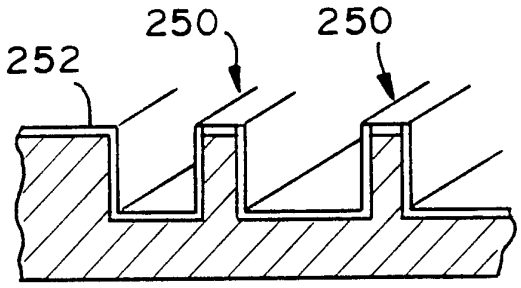


FIG. 11A

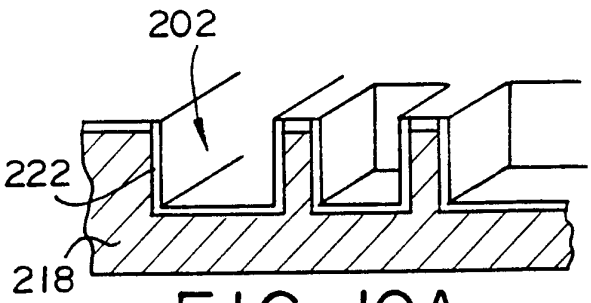


FIG. 10A

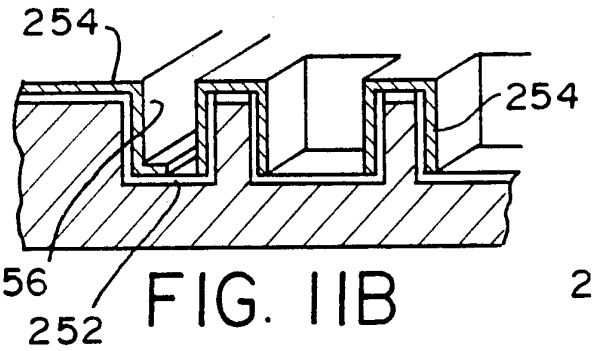


FIG. 11B

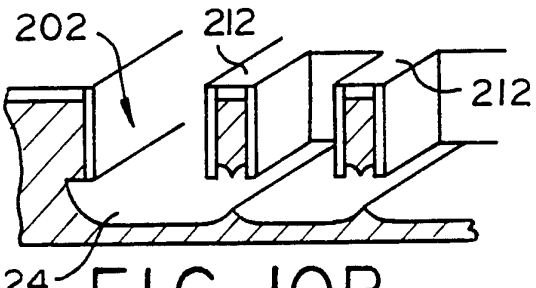


FIG. 10B

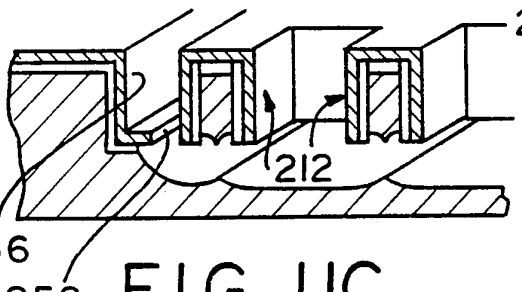


FIG. 11C

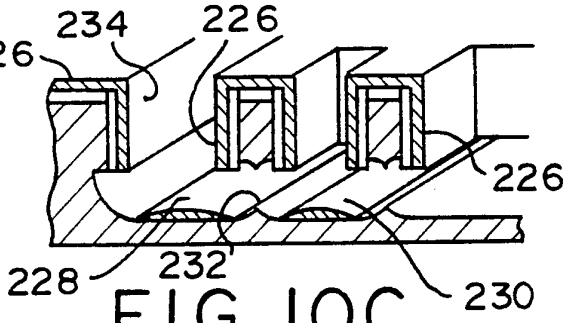


FIG. 10C

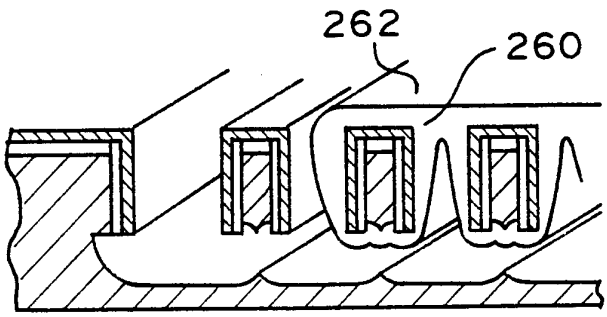
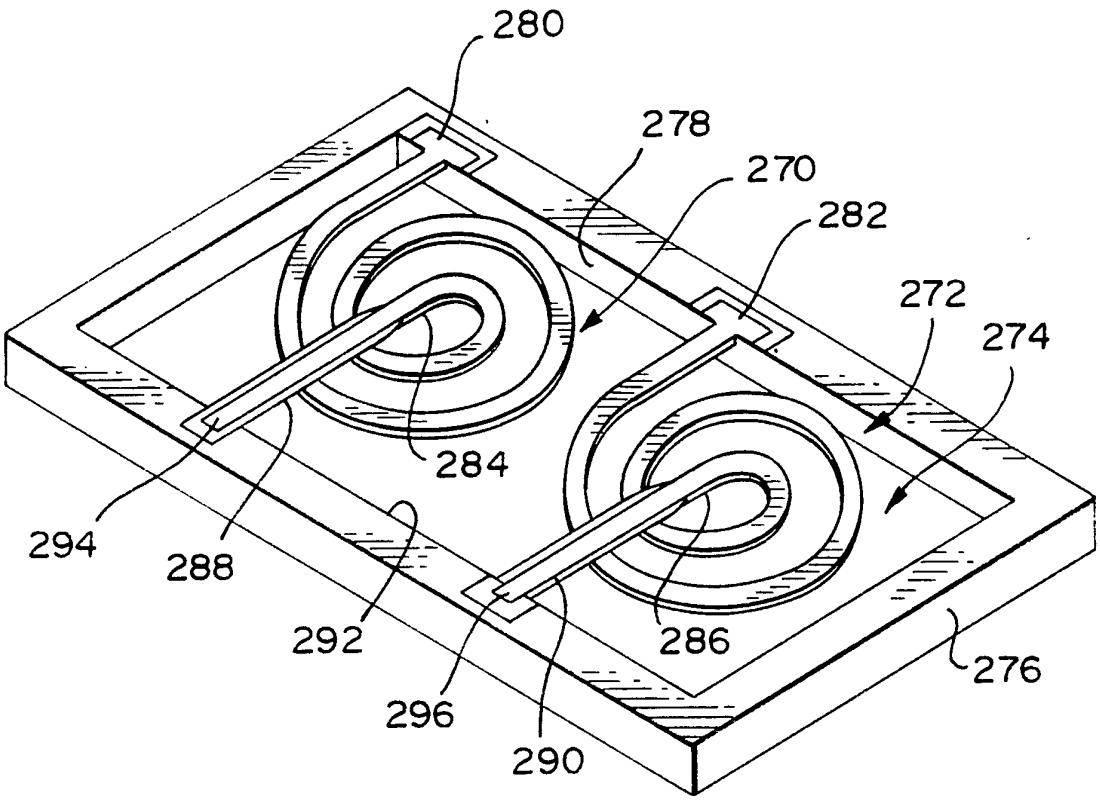


FIG. 12

FIG. 13



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/11584

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 21/44,449,302, 23/48, 29/06,86,84,96
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/203, 228; 156/ 644, 647, 649, 651, 73.755, 777, 257/419; 148/DIG 50, DIG 51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS-cantilever, beam, substrate, trench, release?, metal, etch?, accelerometer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P Y,P	US,A 5,198,390 (MacDonald et al) 30 March 1993, see col. 3, line 45-col. 5, line 54.	1-2,24,26-28 5,30-31,33
Y	US,A 4,685,198 (Kawakita et al) 11 August 1987, see col. 6, line 18.	3,4,25
X	US,A 4,682,503 (Higashi et al) 28 July 1987, see col. 10, line 67.	28
Y,P	Japan 58-89859 (Shinozaki) 28 May 1993, see Abstract.	12-13,21-22,29,32
A	US,A 4,776,924 (Delapierre) 11 October 1988	1-27

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 JANUARY 1994	Date of mailing of the international search report MAR 04 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer for DAVID MASON Telephone No. (703) 308-3858

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/11584

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A 5,072,288 (MacDonald et al) 10 December 1991	28-37
A	US,A 4,783,237 (Aine et al) 08 November 1988	1-27
A	US,A 4,472,239 (Johnson et al) 18 September 1984	1-27
A	US,A 4,522,682 (Soclof) 11 June 1985	1-27

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/11584

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

437/203, 228; 156/644, 649, 651; 73/755, 777; 257/419; 148/D1G 50, D1G51