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(54) **DIFFERENTIAL SIGNAL PROBING SYSTEM**

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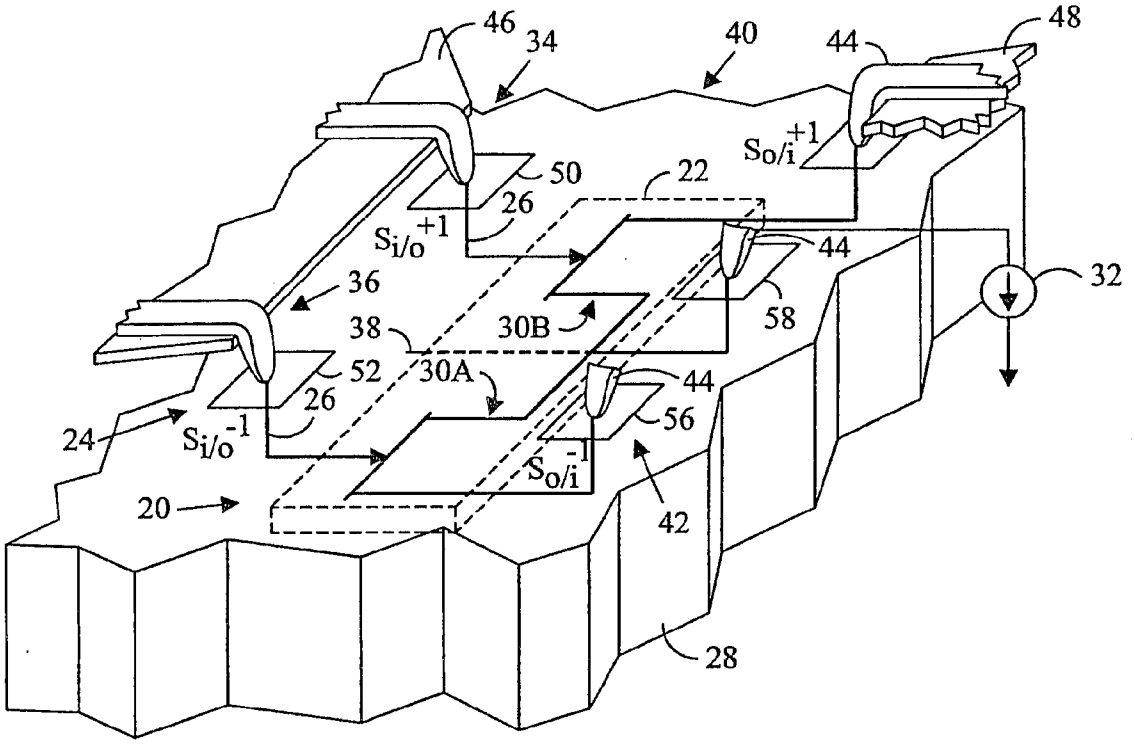
G01R 31/02 (2006.01)

(52) **U.S. Cl.** **324/754**

(57) **ABSTRACT**

A probe measurement system comprises a probe with a linear array of probe tips enabling a single probe to be used when probing a test structure with a differential signal



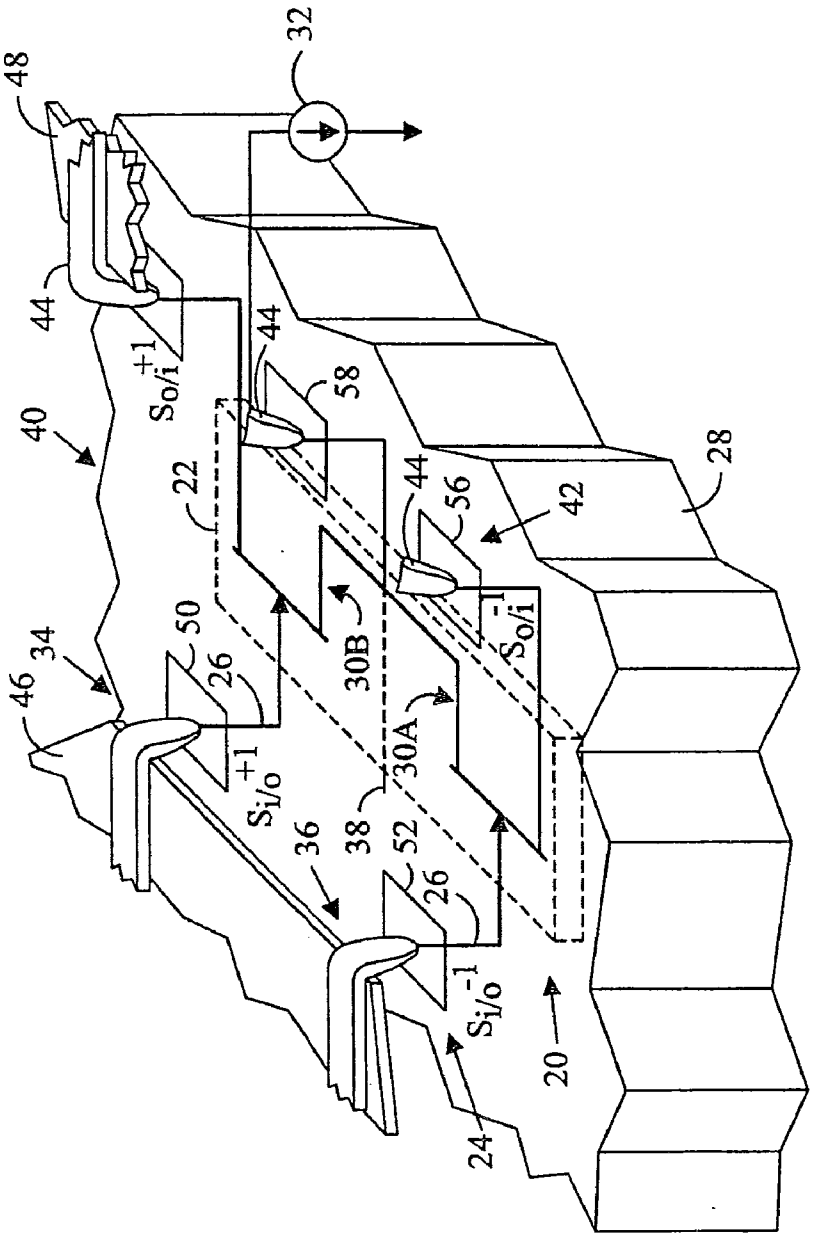

48
32
44
40
$S_{o/i}^{+1}$
44
58
22
28
42
56
44
50
26
34
46
30B
$S_{o/i}^{-1}$
30A
$S_{i/o}^{+1}$
36
38
52
26
$S_{i/o}^{-1}$
20
24

FIG. 1

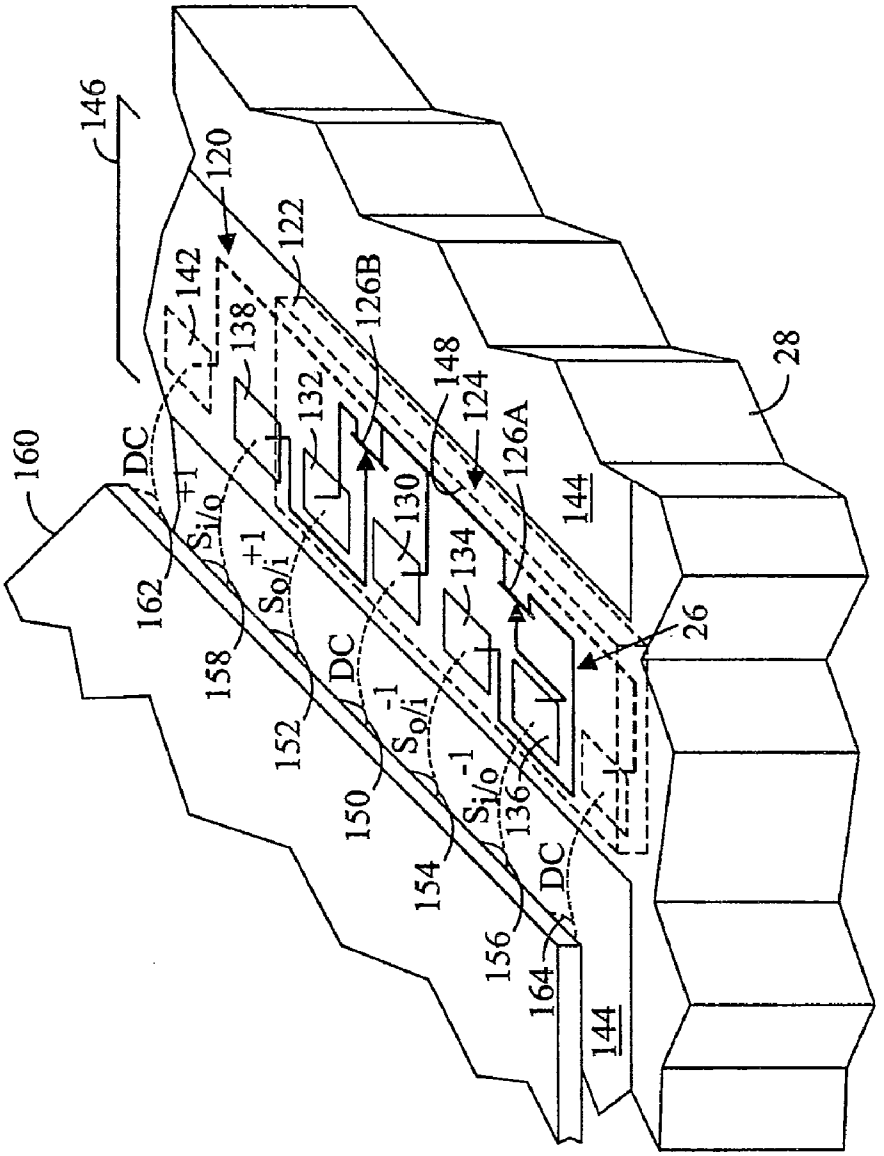

146
120
142
122
138
126B
148
124
132
126A
130
144
134
28
160
DC
+1
$S_{i/o}$
+1
$S_{o/i}$
162
158
DC
152
$S_{o/i}^{-1}$
150
$S_{i/o}^{-1}$
136
154
DC
156
164
144
26

FIG. 2

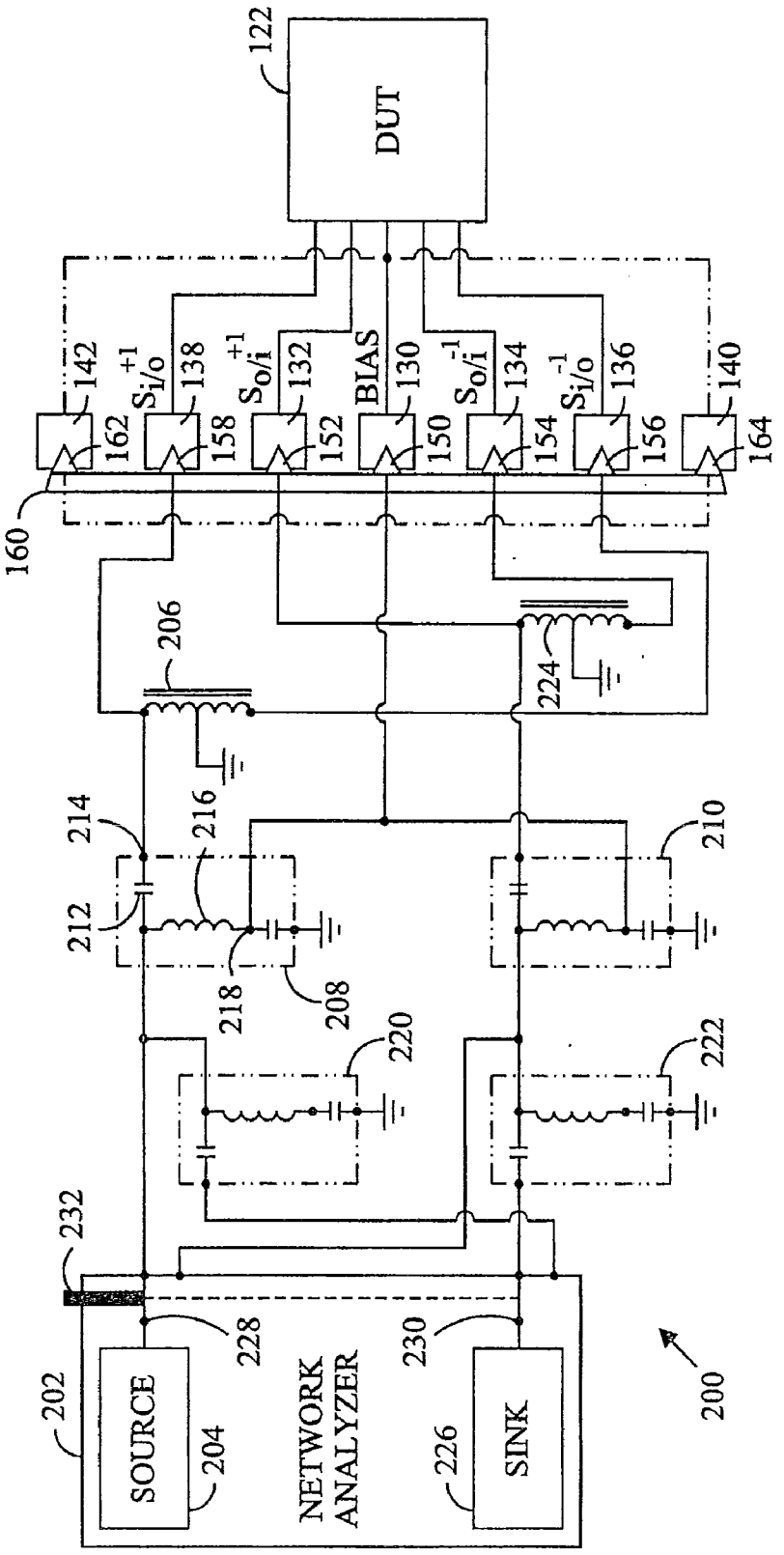

122
DUT
142
138
132
130
134
136
140
162
158
152
150
154
156
164
160
206
224
214
216
212
218
208
210
220
222
232
228
230
202
SOURCE
204
NETWORK ANALYZER
226
SINK
200

FIG. 3

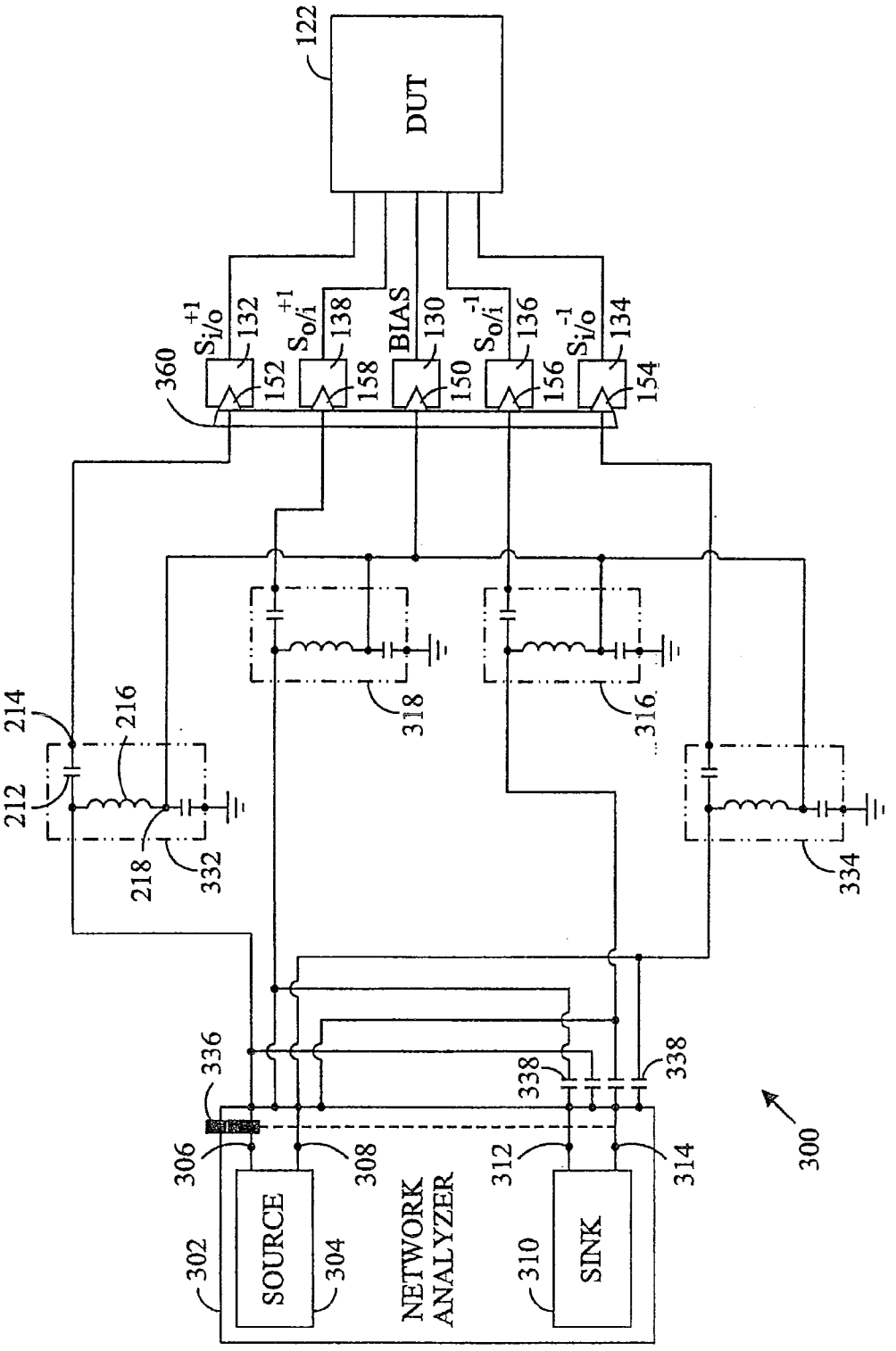

122
DUT
360
$S_{i/o}^{+1}$ 132
$S_{o/i}^{+1}$ 138
BIAS 130
$S_{o/i}^{-1}$ 136
$S_{i/o}^{-1}$ 134
152
158
150
156
154
214
216
212
218
332
318
316
334
336
338
338
306
308
312
314
300
302
SOURCE
304
NETWORK ANALYZER
310
SINK

FIG. 4

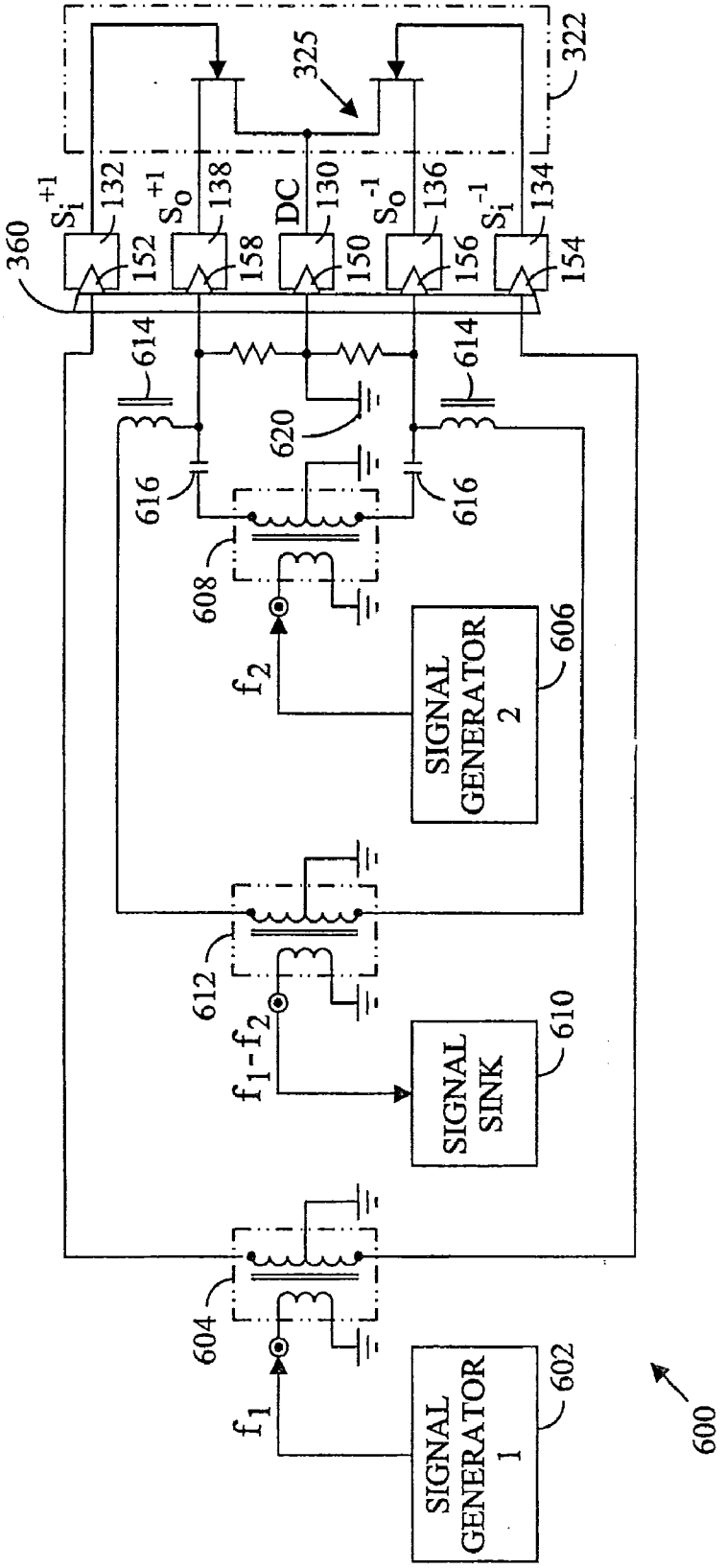
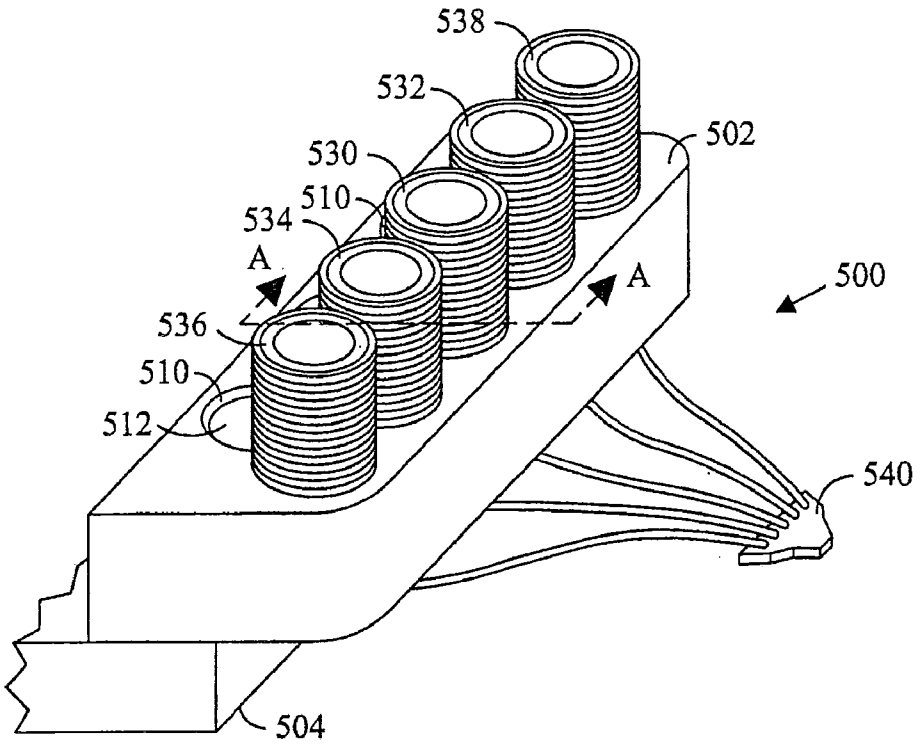

322
325
360
S_i^{+1}
132
S_o^{+1}
138
DC
130
S_o^{-1}
136
S_i^{-1}
134
152
158
150
156
154
614
620
616
608
606
SIGNAL GENERATOR 2
f_2
612
610
SIGNAL SINK
f_1-f_2
604
602
SIGNAL GENERATOR 1
f_1
600

FIG. 5


538
532
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540
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FIG. 6

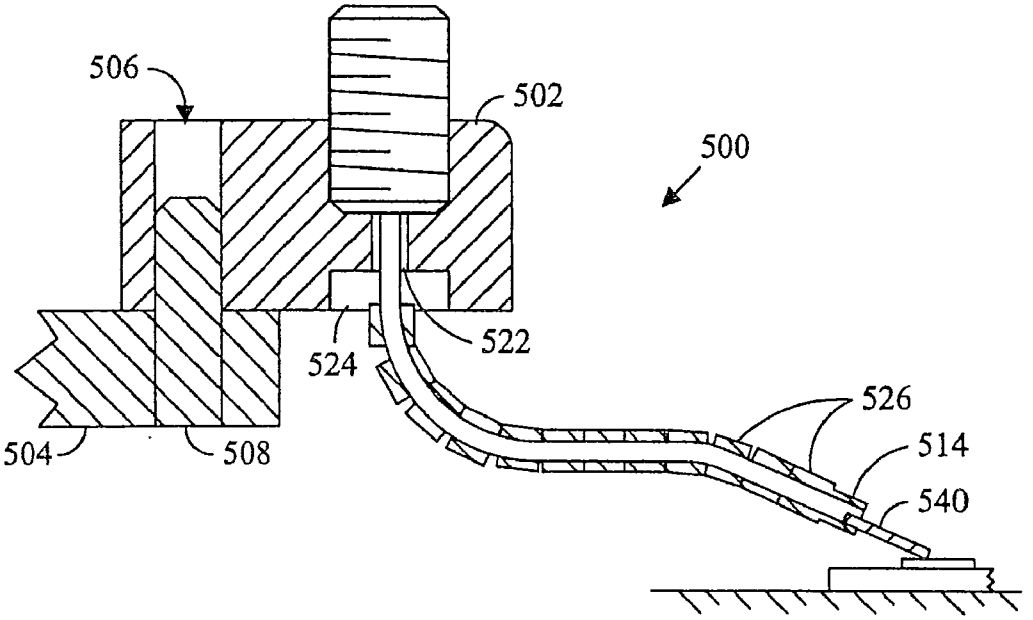
506
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FIG. 7

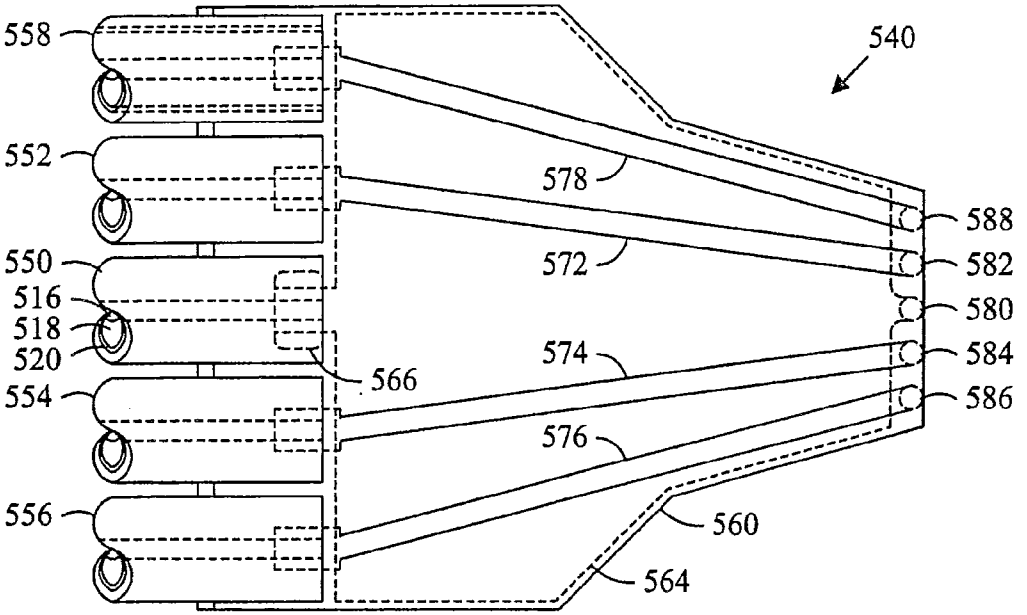
558
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FIG. 8

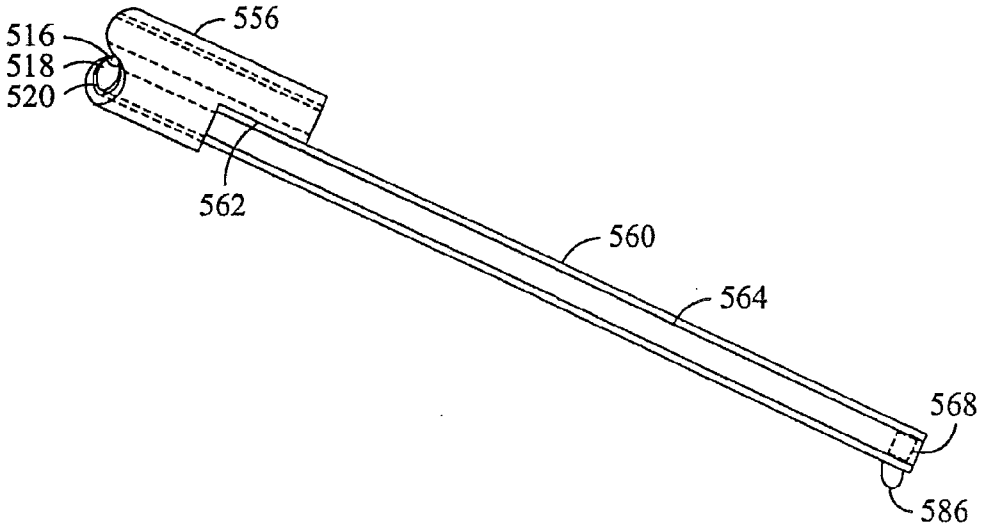
516
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FIG. 9

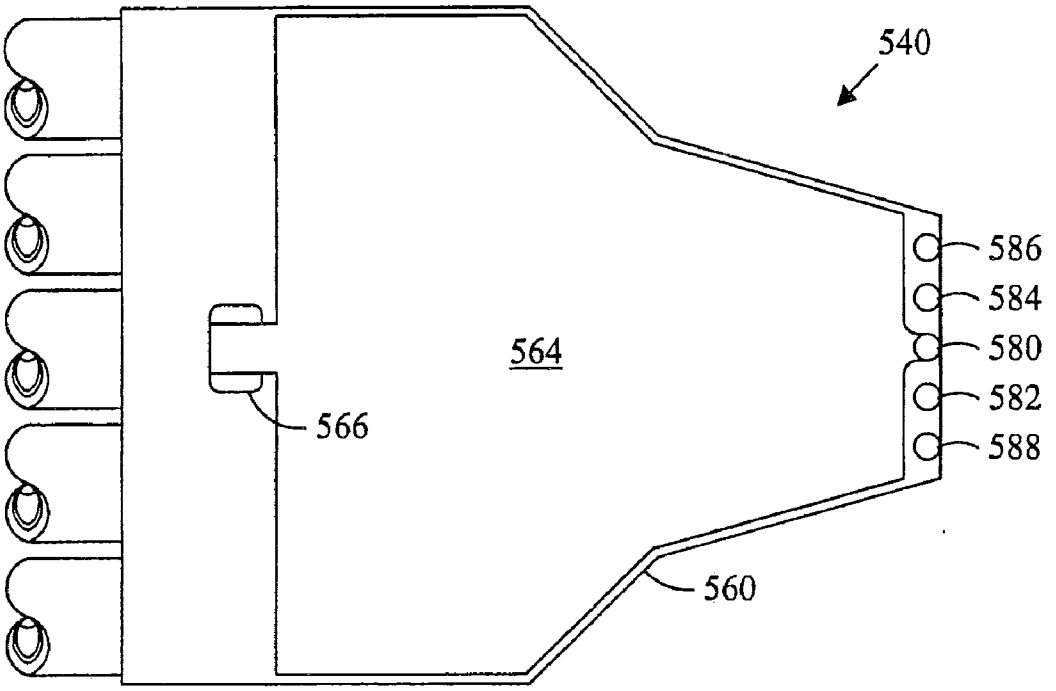
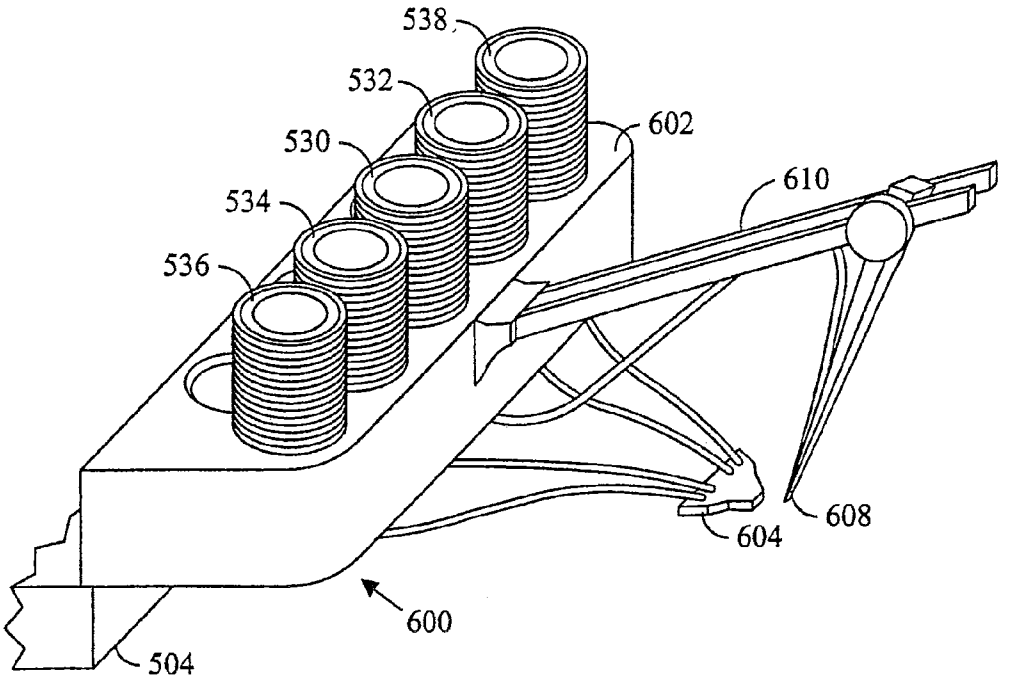


FIG. 10


538
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600
504

FIG. 11

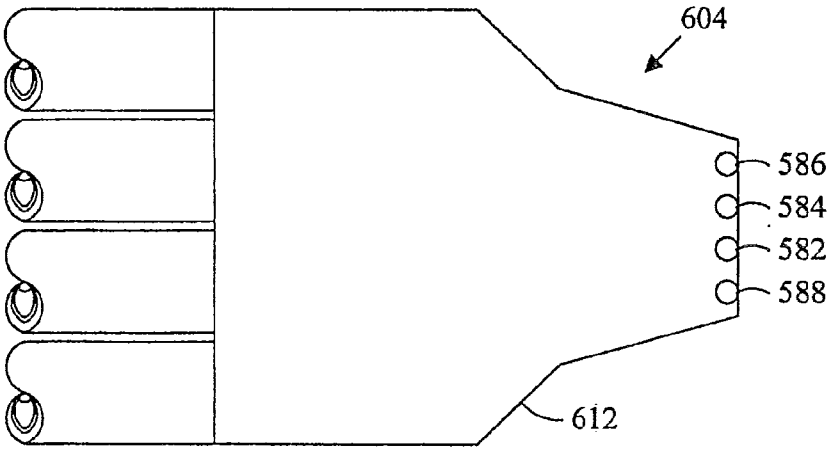

604
586
584
582
588
612

FIG. 12

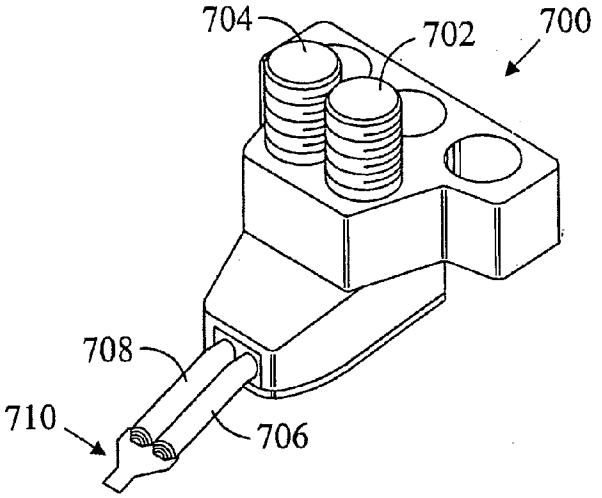
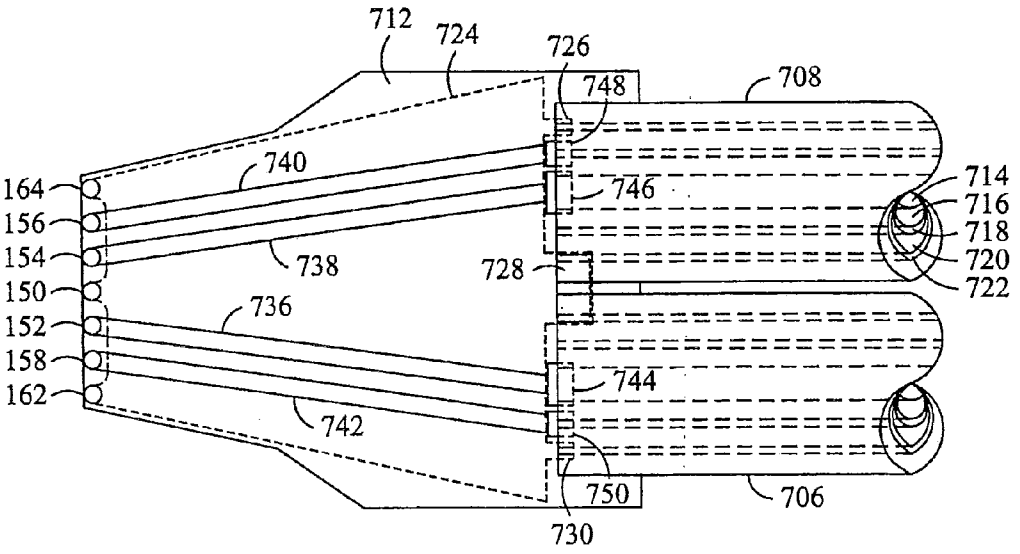

704
702
700
708
710
706

FIG. 13


712
724
726
748
708
740
746
714
716
718
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722
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150
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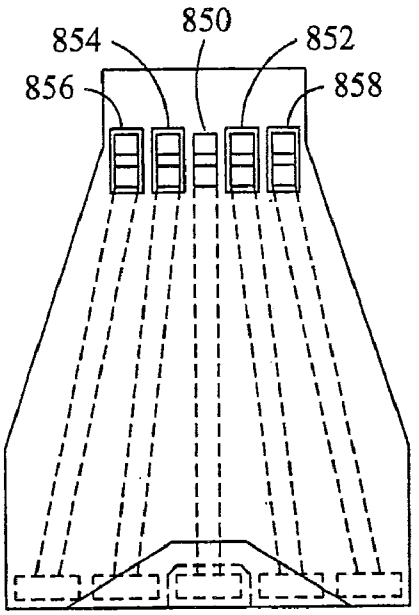
736
744
742
750
706
730

FIG. 14


850
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852
856
858

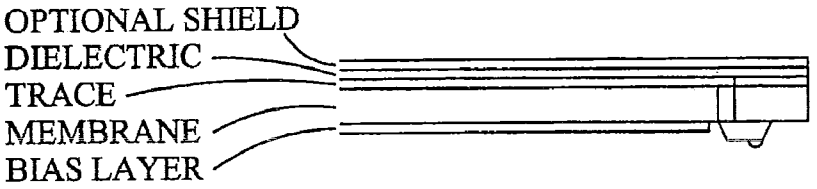
OPTIONAL SHIELD
DIELECTRIC
TRACE
MEMBRANE
BIAS LAYER

FIG. 15

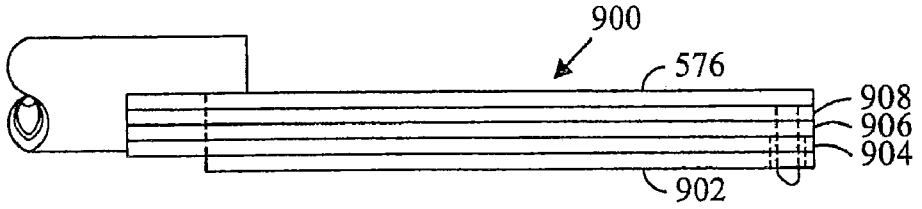
900
576
908
906
904
902

FIG. 17

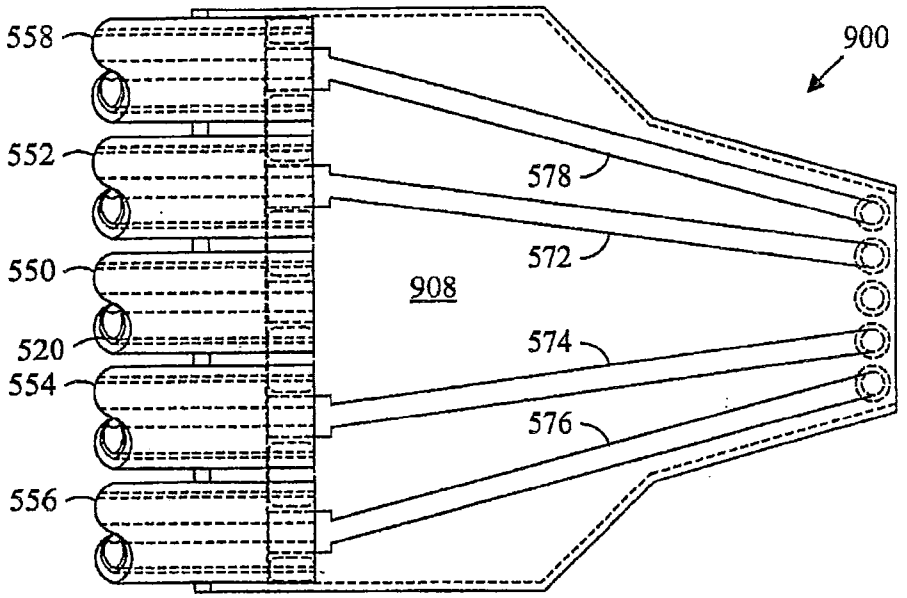
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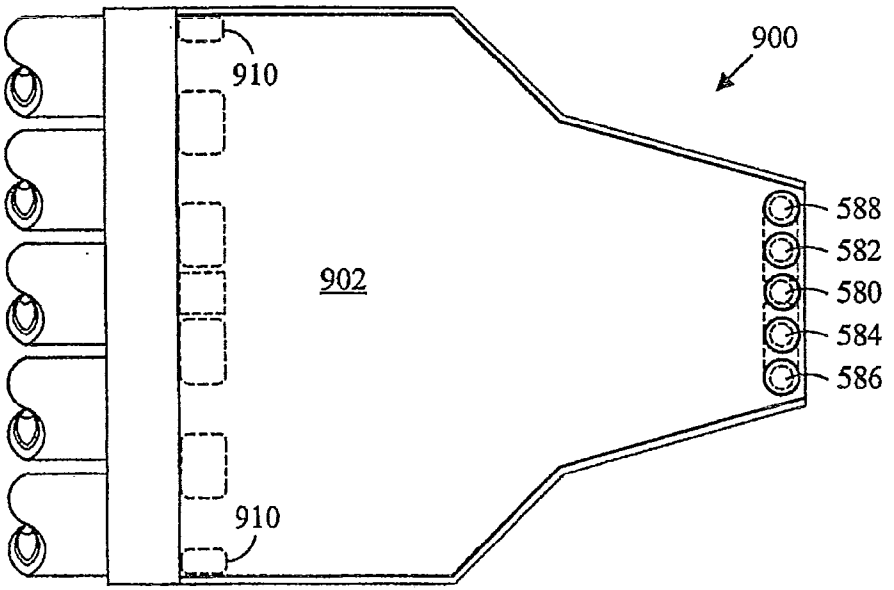
FIG. 16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902
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580
584
586
910

FIG. 18

DIFFERENTIAL SIGNAL PROBING SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 11/710,225 filed Feb. 22, 2007 which claims the benefit of U.S. Provisional Application No. 60/813,119, filed Jun. 12, 2006 and U.S. Provisional Application No. 60/813,477, filed Jul. 17, 2006.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to probe measurement systems for testing integrated circuits and other microelectronic devices and, more particularly, probe measurement systems utilizing differential signaling for testing microelectronic devices.

[0003] Integrated circuits (ICs) are economically attractive because large numbers of often complex circuits, for example microprocessors, can be inexpensively fabricated on the surface of a wafer or substrate. Following fabrication, individual dies, including one or more circuits, are separated or singulated and encased in a package that provides for electrical connections between the exterior of the package and the circuit on the enclosed die. The separation and packaging of a die comprises a significant portion of the cost of manufacturing an integrated circuit device and to monitor and control the IC fabrication process and avoid the cost of packaging defective dies, manufacturers commonly add electrical circuits or test structures to the wafer to enable on-wafer testing or "probing" to verify characteristics of the integrated circuits before the dies are singulated.

[0004] Referring to FIG. **1**, a test structure **20** typically includes a device-under-test (DUT) **22**, a plurality of metallic probe or bond pads **24** that are deposited at the wafer's surface and a plurality of conductive vias **26** that connect the probe pads to the DUT which is typically fabricated beneath the surface of the wafer **28**. The DUT typically comprises a simple circuit that includes a copy of one or more of the basic elements of the integrated circuit, such as a single line of conducting material, a chain of vias or a single transistor. The circuit elements of the DUT are typically produced with the same process and in the same layers of the fabrication as the corresponding elements of the integrated circuit. The marketable ICs are typically evaluated or characterized "on-wafer" by applying a test instrument generated signal to the test structure and measuring the response of the test structure to the signal. Since the circuit elements of the DUT are fabricated with the same process as the corresponding elements of the marketable integrated circuit, the electrical properties of the DUT are expected to be representative of the electrical properties of the corresponding components of the ICs.

[0005] Integrated circuits commonly utilize single ended or ground referenced signaling with a ground plane at the lower surface of the substrate on which the active and passive devices of the circuit are fabricated. As a result of the physical make up of the devices of an integrated circuit, parasitic interconnections exist between many of the parts of the individual devices and between parts of the devices and the wafer on which the devices are fabricated. These interconnections are commonly capacitive and/or inductive in nature and have frequency dependent impedances. For example, the terminals of transistors fabricated on semi-conductive substrates or wafers are typically capacitively interconnected, through the substrate, to the ground plane. The impedance of this parasitic capacitive interconnection is frequency dependent and at higher frequencies the ground potential and the true nature of ground referenced signals becomes uncertain.

[0006] Balanced devices utilizing differential signals are more tolerant to poor radio frequency (RF) grounding than single ended devices making them attractive for high performance ICs. A differential gain cell **30** is a balanced device comprising two nominally identical circuit halves **30**A, **30**B. When biased, with a DC current source **32**, and stimulated with a differential mode signal, comprising even and odd mode components of equal amplitude and opposite phase (S_i^{+1} and S_i^{-1}) **34**, **36**, a virtual ground is established at the symmetrical axis **38** of the two circuit halves. At the virtual ground, the potential at the operating frequency does not change with time regardless of the amplitude of the stimulating signal. The quality of the virtual ground of a balanced device is independent of the physical ground path and, therefore, balanced or differential circuits can tolerate poor RF grounding better than circuits operated with single ended signals.

[0007] In addition, the two waveforms of the differential output signal (S_o^{+1} and S_o^{-1}) **40**, **42** are mutual references providing faster and more certain transition from one binary value to the other for digital devices and enabling operation with a reduced voltage swing for the signal. Typically, differential devices can operate at lower signal power and higher data rates than single ended devices. Moreover, noise from external sources, such as adjacent conductors, tends to couple, electrically and electromagnetically, in the common mode and cancel in the differential mode. As a result, balanced or differential circuits have good immunity to noise, including noise at even-harmonic frequencies since signals that are of opposite phase at the fundamental frequency are in phase at the even harmonics. Improved tolerance to poor RF grounding, increased resistance to noise and reduced power consumption make differential devices attractive for ICs that operate at higher frequencies. A test structure comprising a differential gain cell enables on wafer testing and characterization of differential devices included in the marketable ICs fabricated on the wafer.

[0008] At higher frequencies, on-wafer characterization is commonly performed with a network analyzer. The network analyzer comprises a source of an AC signal, commonly, a radio frequency (RF) signal, that is used to stimulate the DUT of a test structure. A forward-reverse switch directs the stimulating signals to one or more of the probe pads of the test structure. Directional couplers or bridges pick off the forward or reverse waves traveling to or from the test structure which are down-converted by intermediate frequency (IF) sections of the network analyzer where the signals are filtered, amplified and digitized for further processing and display. The result is a plurality of s-parameters (scattering parameters), the ratio of a normalized power wave comprising the response of the DUT to the normalized power wave comprising the stimulus supplied by the signal source.

[0009] At higher frequencies, the preferred interconnection for communicating signals between the test structure, the source of the stimulating test signal and the sink for the output signals of the test structure is coaxial cable. The transition between the coaxial cable and the probe pads of the test structure is preferably provided by movable probes having one or more conductive probe tips **44** that are arranged to be co-locatable with respective probe pads of the test structure.

The test instrumentation and the test structure can be temporarily interconnected for probing by bringing the probe tips of the probe(s) into contact with the probe pads of the test structure. Typically, two probes **46**, **48** are utilized when probing a differential or balanced test structure. A differential gain cell requires two input probe pads **50**, **52** and two output probe pads **54**, **56** for the even and odd mode components of the differential input and output signals and a bias probe pad **58** through which the transistors of the cell are biased. The probe pads of differential test structures are arranged to avoid physical contact and crosstalk between the two probes during simultaneous engagement with the test structure. As a result, the probe pads of a differential test structure occupy a significant portion of the useable surface of a wafer and, typically, must be fabricated in an area of the wafer in which one or more dies containing marketable ICs could otherwise be fabricated. However, test structures serve no purpose after the dies containing the marketable ICs are singulated and manufacturers of ICs are under continuous cost pressure to maximize the number of marketable ICs that are manufactured on each wafer.

[0010] What is desired, therefore, is a compact, simplified probe measurement system for communicating differential signals between a test instrument and a test structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** is a perspective illustration of a portion of a wafer including a differential test structure having probe pads arranged for engagement by a two probes.

[0012] FIG. **2** is a perspective illustration of a portion of a wafer including a differential test structure engageable by a single probe having a linear array of probe tips.

[0013] FIG. **3** is a schematic diagram of a probe system utilizing a two-port network analyzer for testing a differential test structure.

[0014] FIG. **4** is a schematic diagram of a probe system utilizing a four-port network analyzer for testing a differential test structure.

[0015] FIG. **5** is a schematic diagram of a probe system utilizing a differential test structure as a frequency converter.

[0016] FIG. **6** is a perspective view of a probe for testing a differential test structure.

[0017] FIG. **7** is a section view of the probe of FIG. **6** along line A-A.

[0018] FIG. **8** is a top view of a probe head of a probe for engaging a differential test structure.

[0019] FIG. **9** is an elevation view of the probe head of FIG. **8**.

[0020] FIG. **10** is a bottom view of the probe head of FIG. **8**.

[0021] FIG. **11** is a perspective view of a probe including a linear array of four probe tips and a fifth probe tip.

[0022] FIG. **12** is a bottom view of a probe head of the probe of FIG. **11**.

[0023] FIG. **13** is a perspective view of an embodiment of a differential signal probe comprising cables including having a plurality of conductors.

[0024] FIG. **14** is a top view of a probe head of the probe of FIG. **13**.

[0025] FIG. **15** is a top view and an elevation view of a probe head comprising a dielectric membrane plate.

[0026] FIG. **16** is a top view of an additional embodiment of a probe head.

[0027] FIG. **17** is an elevation view of the probe head of FIG. **16**.

[0028] FIG. **18** is a bottom view of the probe head of FIG. **16**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0029] Circuits utilizing differential signaling are becoming increasingly common for a wide range of higher frequency applications. The benefits of differential signaling or balanced devices include lower power levels, faster state transition for binary devices, good immunity from noise, minimal susceptibility to electromagnetic coupling at higher frequencies, and greater tolerance of poor grounding conditions which are commonly encountered when integrated circuits are operated at high frequencies. The integrity of the process used to manufacture marketable integrated circuits (ICs) is tested by fabricating a plurality of test structures on the wafer using the same process that is used to fabricate the ICs. Characteristics of the marketable ICs are inferred by stimulating the test structure with a test instrument generated signal and capturing the response of the test structure. While test structures are typically simple circuits, the response of similar devices included in the more complex marketable ICs is expected to be similar to the response of the test structure because the devices in the marketable ICs and similar devices in the test structures are fabricated with the same process.

[0030] While differential signaling provides a number of advantages, particularly at higher frequencies and in noisier environments, the use of balanced or differential devices in the DUTs of test structures is limited. The probe pads of differential test structures are arranged so that two probes can simultaneously engage the probe pads while avoiding physical contact and crosstalk between the probe tips. The probe pads are spread over a significant area of the surface of the wafer and, typically, must be fabricated in an area of the wafer that could otherwise accommodate one or more dies containing marketable ICs. However, test structures serve no purpose after the dies containing the marketable ICs are singulated and manufacturers of ICs are under continuous cost pressure to maximize the number of marketable ICs manufactured on each wafer. The inventors concluded that the number of dies comprising marketable ICs fabricated on a wafer could be increased if the differential test structure could be connected to the test instrumentation with a single probe enabling rearrangement of the probe pads and fabrication of the test structure in a saw street between dies.

[0031] Referring in detail to the drawings where similar parts are identified by like reference numerals, and, more particularly to FIG. **2**, the test structure **120** comprises a DUT **122** that includes a differential gain cell **124** that is responsive to a differential mode input signal. The differential mode input signal comprises an even mode component (S_i^{+1}) and an odd mode component (S_i^{-1}) that has substantially the same amplitude as the even mode component but which is opposite in phase of the even mode component. The differential gain cell **124** comprises two substantially identical field effect (JFET) transistors **126**A and **126**B. However, a DUT typically comprises components corresponding to the components utilized in the marketable integrated circuits fabricated on the wafer and other types of transistors, such as bipolar junction (BJT) transistors or MOSFET transistors can be used in the construction of the differential gain cell of a test structure.

[0032] The five probe pads **130**, **132**, **134**, **136** and **138** through which the DUT is biased and through which the components of the differential signals are communicated to and from the test structure are arranged in a substantially linear array reducing the breadth of the probe pad arrangement and enabling placement of the test structure between dies **144** in a saw street **146** (indicated by a bracket) that is only slightly wider that the width of a probe pad. The source terminals of the transistors of the differential gain cell are interconnected as a transistor bias terminal **148**. The bias terminal is interconnected to the bias bond or probe pad **130** located in the center of the linear array of probe pads. The gates of the transistors comprise input terminals of the DUT and are connected to respective signal input probe pads **136**, **138**. The drains of the transistors of the differential gain cell comprise the output signal terminals of the DUT and are interconnected to the output signal probe pads **132**, **134**. Typically, the DUT **122** is relatively small and comprises circuit elements that are fabricated beneath the surface of the wafer. The probe pads are conductively connected to the terminals of the DUT by vias **26** that extend from the probe pads on the surface of the wafer to the subsurface strata in which the circuit elements of the DUT and the corresponding circuit elements of the integrated circuit have been fabricated.

[0033] Referring to FIG. **3**, at higher frequencies the DUT, for example the DUT **122**, of a differential test structure is typically stimulated with a signal generated by a network analyzer. A typical two-port network analyzer **202** outputs a single ended (ground referenced) modulated signal, which may include a DC offset, at the port of an RF signal source **204**. In the probe measurement system **200**, the single ended input signal is conducted to a balun **206** which converts the single ended signal to a balanced or differential signal comprising differential components having substantially the same amplitude but opposite phase. The two components of the differential input signal are transmitted to respective bias tees **208**, **210** which separate the modulated portion of the input signal from the DC portion. A bias tee comprises a capacitor **212** in series with an RF port **214** that blocks transmission of the DC component of the input signal from the RF port. An inductor **216**, in series with a DC port **210** of the bias tee blocks, the modulated signal but permits transmission of the DC portion of the input signal to the DC port. The modulated components of differential input signal, S_i^{+1} and S_i^{-1}, are communicated to respective probe tips **156**, **158** via interconnections to the RF ports of the respective input signal bias tees. The probe tips **156**, **158** are arranged on a probe **160** which is movable relative to the test structure so that the probe tips may be co-located with the respective input signal probe pads **136**, **138** connected to the DUT **122** of a test structure.

[0034] Similarly, the differential output signal components (S_o^{+1} and S_o^{-1}) which are controlled by the input signals at the respective input terminals of the differential gain cell are communicated from the respective probe pads **132**, **134** to respective output signal probe tips **152**, **154** that are interconnected to respective bias tees **220**, **222**. The modulated portions of the differential output signal components are transmitted to a balun **224** while DC portions of the differential output signal components are blocked from the network analyzer by the capacitors **214** in series with the RF ports of the bias tees. The balun converts the differential signal components to a single ended signal which is transmitted to a signal sink **226** of the network analyzer. The signal sink typically comprises one or more intermediate frequency (IF) sections where, typically, the signals are filtered, amplified and digitized for further processing and display.

[0035] The transistors of the differential gain cell of the DUT are biased by a DC current that is communicated between the DC ports of the bias tees and bias probe pad **130** by a bias probe tip **150** of the probe. An alternative embodiment of the test structure **122** includes additional probe pads **140**, **142** located distal of the respective ends of the linear array of five probe pads and which are interconnected with the bias probe pad **130**. Spatially corresponding additional probe tips **162**, **164**, interconnected with the centrally located bias probe tip **150**, are included in an alternative embodiment of the probe **160** to engage the additional probe pads of the alternative test structure probe pad arrangement.

[0036] While many network analyzers output only single ended signals, the accuracy of a probe system utilizing single ended signals to probe a differential test structure is limited because the reference plane for de-embedding the test structure is located at the ports of the baluns nearest the DUT. Referring to FIG. **4**, a four port network analyzer **302** can output differential signals directly permitting mixed mode analysis and de-embedding of the DUT at its terminals. In the probe measurement system **300**, the differential input signal components, including a DC offset, are output at the ports **306**, **308** of the signal source **304** and transmitted to respective bias tees **316**, **318**. The capacitor **320** in series with the RF port of a bias tee blocks the transmission of the DC component of the input signal from the RF port. The modulated portion of the differential input signal components (S_i^{+1} and S_i^{-1}) are communicated from the RF port of the respective bias tee **316**, **318** to a respective probe tip **156**, **158** of the probe **360**. Each of the probe tips is co-locatable with a respective one of the probe pads **136**, **138** that is interconnected to conduct an input signal component to the DUT. Similarly, the differential output signal components (S_o^{+1} and S_o^{-1}) are transmitted from respective probe pads **132**, **134** to respective probe tips **152**, **154** and then to respective bias tees **332**, **334**. The capacitors of the bias tees in series with the RF port, block the transmission of DC from the bias tees to the two signal input ports **312**, **310** of the signal sink **302**. The outputs at the DC ports of the bias tees are transmitted to the bias probe tip **150** which is arranged for contact with the bias probe pad **130** of the DUT. FIG. **4** illustrates another alternative arrangement of probe pads and probe tips where the output signals are sourced from the probe pads at the ends of the linear array of five probe pads and the input signals are transmitted to the probe pads immediately adjacent to the central probe pad of the linear array of five probe pads.

[0037] A network analyzer is expensive and the cost of a probe measurement system that includes a network analyzer substantially impacts the cost of producing high frequency ICs. The inventors realized that the differential gain cell could be utilized as a passive frequency converter enabling parametric RF testing with a less costly probe measurement system that utilizes a low frequency spectrum analyzer rather than a more costly network analyzer. Referring to FIG. **5**, in the probe measurement system **600** a first signal generator **602** transmits a single ended, modulated signal having a frequency (f_1) to a first balun **604**. The balun converts the single ended signal to a differential signal comprising even and odd mode components of substantially equal amplitude and opposite phase angle. The differential signal components are conducted to a probe **360** including a plurality of probe tips arranged to be co-locatable with the probe pads of a test

structure including a DUT **322** comprising a differential gain cell **325**. The components of the differential signals from the first signal generator are conducted by probe tips **152** and **154** to respective probe pads **132** and **134** which are connected to the gates of the transistors of the differential gain cell. The transistors of the differential gain cell are biased by the connection of their source terminals to ground **620** through the probe pad **130** and the contacting probe tip **150**.

[0038] A second signal generator **606** outputs a second single ended, modulated signal having a second frequency (f_2) to a second balun **608** which converts the single ended signal to a differential signal comprising components of substantially equal amplitude and opposite phase. The signal is transmitted to the drains of the transistors of the differential gain cell through high pass filter capacitors **616** which block the transmission of low frequency signals. The outputs of the DUT which are controlled by the input signals at the respective gates of the transistors are conducted to the output signal probe pads **136** and **138** and respective contacting probe tips **156**, **158**. The respective components of the signals from the second signal generator and the output terminals of the DUT, having respective second and first frequencies, are combined producing respective components of a differential combined output signal. The components of the combined output signal comprise an upper frequency (f_1+f_2) combined output signal band and a lower frequency (f_1-f_2) combined output signal band. The differential components of the lower frequency combined output signal band are separated from the upper frequency combined output signal band by the low pass filters **614** and converted to a single ended signal by a balun **612**. The lower frequency (f_1-f_2), single ended signal is conducted to a signal sink **610** for analysis, such as comparison with the results obtained by testing other differential gain cells having known characteristics, and display. Utilizing the differential test structure as a frequency converter enables stimulation of the test structure with a high frequency signal but permits analyzing the result with a relatively less expensive, lower frequency capable, signal sink, such as a spectrum analyzer.

[0039] Typically, coaxial cable interconnects the network analyzer, other test instrumentation and the probe which provides the transition from the signal paths provided by the coaxial cable to the signal paths comprising the probe pads fabricated on the surface of a wafer. Referring FIGS. **6**, **7** and **8**, the probe **500** comprises a support block **502** which is suitably constructed for connection to a movable probe supporting member **504** of a probe station. For example, the support block **502** includes an aperture **506** for engagement by a snugly fitting alignment pin **508** that projects vertically from the probe supporting member. In addition, the support block includes a pair of countersunk apertures **510** to accept a pair of fastening screws **512** arranged to engage threaded holes in the probe supporting member and secure the probe to the probe supporting member.

[0040] The probe includes a plurality of input ports **530**, **532**, **534**, **536**, **538** which, in the embodiment depicted, comprise spark-plug type, K connectors. This connector enables the external connection of an ordinary coaxial cable to an input port permitting a well shielded high frequency transmission channel to be established between the probe and the test instrument. If desired, other types of connectors can be used, such as a 2.4 mm. connector, a 1.85 mm. connector or a 1 mm. connector.

[0041] In the depicted embodiment, a semi-rigid coaxial cable **514** is connected at its rearward end to each K connector comprising one of the ports of the probe. These coaxial cables preferably include an inner conductor **516**, an inner dielectric **518** and an outer conductor **520** and are preferably of phase-stable low-loss type. The coaxial cable may likewise include other layers of materials, as desired. To prepare the rearward ends of the cables for connection to an appropriate K-connector, the rearward end is stripped to expose the inner conductor, and this inner conductor is temporarily held inside a dummy connector while the adjacent outer conductor is soldered within a bore **522** formed in the primary support block. A recess **524** in the support block below this bore provides access to facilitate the soldering process. The dummy connector is then removed and a K-connector is screwed into each of the threaded openings formed in the block above the bore so as to effect electrical connection between the connectors and the coaxial cables. A thread locking compound may be applied to the threads of the K-connectors prior to their installation to ensure a secure physical connection.

[0042] The forward ends of the cables remain freely suspended and, in this condition, serve as a movable support for a probe head **540** of the probe. Before being connected to the K-connector, the cables are bent along first and second intermediate portions in the manner shown so that a generally upwardly curving 90° bend and a downwardly curving bend, respectively, are formed in the cable. The protruding ends of the coaxial cables may be slidably inserted into a tube **526** comprising semi-flexible microwave-absorbing material. One material used for forming the tube comprises iron and urethane. The semi-flexible tube of microwave absorbing material serves to substantially reduce the levels of microwave energy that travel along the outer conductor of the semi-rigid cable.

[0043] Referring also to FIGS. **9** and **10**, the probe includes a microstrip style probe head **540** that includes a dielectric plate **560** having generally planar upper and lower surfaces that is affixed to the forward ends of the coaxial cables **550**, **552**, **554**, **556**, **558**. The underside of each cable is cut away to form a shelf **562**, and the dielectric plate is affixed to the shelf. Alternatively, the dielectric plate may be supported by an upwardly facing shelf cut away from the cable or the end of the cable without a shelf. A conductive bias layer **564** comprising a thin, generally planar conductive material is affixed to the bottom of the dielectric plate. A thin, generally planar, bias layer has a low profile that is less likely to interfere with the ability to effectively probe a DUT by accidentally contacting the device. A via **566**, electrically couples the bias layer to the center conductor of the coaxial cable **550** connected to the bias input port **530** of the probe. The bias layer may be provided with any DC voltage potential suitable for biasing the transistors of the differential gain cell of the DUT. The bias layer preferably covers substantially all of the lower surface of the dielectric plate. Alternatively, the bias layer may cover a portion greater than 50%, 60%, 70%, 80%, 90% of the surface of the dielectric plate and/or the region directly under a majority (or more) of the length of a conductive signal trace secured to the opposing side of the plate.

[0044] One or more conductive signal traces are supported by the upper surface of the dielectric plate. The conductive traces may be deposited, using any technique, or otherwise secured on the upper surface of the dielectric plate. A conductive signal trace is electrically interconnected to the inner conductor of each of the coaxial cables **552**, **554**, **556**, **558**. The respective interconnected conductive traces **572**, **574**, **576**, **578** normally conduct the components of the differential

signals to and from the DUT. Separated by dielectric material, each conductive trace, together with the bias layer, forms one type of a microstrip transmission structure. Other layers above, below, and/or between the bias layer and the conductive trace(s) may be included, if desired.

[0045] Conductive vias **568** passing through the dielectric plate enables transference of the signal path from the conductive traces on the upper surface of the plate to the lower surface of the plate. The conductive via substantially reduces the capacitance of the signal path compared to a conductive finger extending over the end of the dielectric plate. The conductive via provides a path from one side of the plate to the other that is free from an air gap between the via and the dielectric for at least a majority of the thickness of the plate.

[0046] The lower surface of the dielectric plate includes a plurality of contact bumps or probe tips **580**, **582**, **584**, **586**, **588** that are respectively electrically connected to the bias layer or to the vias extending from respective conductive traces on the upper surface of the dielectric plate. The probe tips are arranged in a linear array with the centroids of the lower ends of the probe tips being substantially aligned and arranged generally parallel to forward edge of the probe head. The probe tips are spatially arranged proximate the adjacent tip(s) in the linear array so as to be co-locatable with the respective probe pads that conduct the signals for the test structure that is to be probed. It is to be understood that the probe tips may take any suitable form, such as a bump, a patterned structure, or an elongate conductor. The bias layer may laterally encircle one or more of the probe tips or may extend beyond one or more of the probe tips to reduce crosstalk with other probes.

[0047] Referring to FIGS. **16**, **17** and **18**, in an additional embodiment of a probe head **900** for testing a differential test structure, a conductive shield **902**, which is preferably planar in nature, is affixed to the bottom of a lower dielectric plate **904**. The conductive shield, may be for example, a thin conductive material (or otherwise) that is affixed to the lower plate **904**. A shield of thin generally planar conductive material is less likely to accidentally contact the test structure when the probe tips are contact with the probe pads. The conductive shield is electrically coupled to an outer conductor **520** of at least one of the coaxial cables **550**, **552**, **554**, **556**, **558** by a via **910** to form a ground plane. The outer conductor is typically connected to ground, though the outer conductor may be provided with any suitable voltage potential (either DC or AC). The conductive shield **902** preferably covers substantially all of the lower surface of the lower dielectric plate **904**. Alternatively, the conductive shield **902** may cover greater than 50%, 60%, 70%, 80%, 90%, and/or the region directly under a majority (or more) of the length of a conductive signal trace on the opposing side of the probe head. The bias voltage for the transistors of the DUT is conducted to the bias probe tip **580** through a middle conductive layer **906** which is conductively connected to the bias probe tip and to the center conductor of the coaxial cable **550** by vias. Overlaying the middle conductive layer, an upper dielectric plate **908** includes an upper surface to which are secured the traces **572**, **574**, **576**, **578** that conduct the components of the differential input and output signals. The traces are in contact with the center conductors of the respective coaxial cables and are connected to the respective probe tips by vias extending from the upper surface of the upper dielectric plate to the probe tips.

[0048] Referring to FIGS. **11** and **12**, in another embodiment of a probe for a testing a differential test structure, the probe **600** comprises support block **602** securable to the probe supporting member **504**. A plurality of ports **532**, **534**, **536**, **538** are attached to the support block and electrically connected to a plurality of coaxial cables that extend to a probe head **604**. The connector of the centrally located port **530** is electrically connected to a coaxial cable **606** which extends to a probe tip **608** supported by an arm **610** attached to the support block **602**. The probe head **604** comprises a dielectric plate **612** which supports four probe tips **582**, **584**, **586**, **588** arranged in a linear array and which conduct the components of the differential input and output signals to and from the test structure. The bias for the transistors of the test structure is conducted from the port **530** to a probe pad of a test structure by a probe tip **608** which is proximate the third and fourth probe tips of the linear array of probe tips **582**, **584**, **586**, **588** but not in linear alignment with the probe tips included in the linear array through which the components of the differential signals are conducted.

[0049] Referring to FIGS. **13** and **14**, the ports **702**, **704** of the probe **700** of alternative embodiment are arranged to provide electrical interconnections to a coaxial cable having more than two conductors. For example, the conductors may be triaxial cables having three conductors separated by intervening dielectric layers. The triaxial cables **706**, **708** are electrically interconnected to the respective ports, at least one of which is insulated from the support block, at their rearward ends. The freely suspended forward support ends of the triaxial cables support a probe head **710** comprising a dielectric plate **712** secured to a shelf formed in each of the ends of the two triaxial cables. The removal of a portion of the triaxial cable to form the shelf exposes the inner conductor **714**, the inner dielectric layer **716**, the intermediate conductor **718**, the outer dielectric layer **720** and the outer conductor **722** that comprise the cable. The conductors of the triaxial cables are interconnected to respective probe tips formed on the lower surface of the dielectric plate. For example, if the DC bias is conducted to the probe head through the outer conductors of the triaxial cables, the central probe tip **150** can be interconnected to the outer conductors by a bias layer **724** supported on the lower surface of the dielectric plate that is electrically interconnected to the central probe tip **150** and electrically interconnected to the outer conductors by vias **726**, **728**, **730** extending through the dielectric plate. In addition, the linear array of probe tips includes probe tips **162** and **164** for engaging probe pads **142** and **140** of an alternative embodiment comprising seven probe pads and are also interconnected to the bias layer. The components of the differential input and output signals are conducted from the respective inner conductors and respective intermediate conductors to the probe tips **152**, **154**, **156** and **158** by traces **736**, **738**, **740**, **742** on the upper surface of the dielectric plate that are electrically interconnected to the respective conductor exposed at the shelf in the triaxial cable and vias **744**, **746**, **748**, **750** extending between the upper and lower surfaces of the dielectric plate.

[0050] Referring to FIG. **15**, in an additional embodiment a flexible dielectric membrane plate **802** may be substituted for a more rigid dielectric plate. An example of membrane material is described in U.S. Pat. No. 5,914,613. In general, membrane based probes are characterized by a flexible (or semi-flexible) plate or substrate with traces supported thereon together with contacting portions or probe tips being supported thereon. The linear array of probe tips **850**, **852**, **854**,

856, **858** are arranged to be co-locatable with the probe pads of the DUT. The traces are normally on the opposing side of the membrane and connected to the probe tips with vias. In many cases, the membrane technology may be significantly thinner than ceramic based substrates or plates, such as 40, 30, 20, 10, 5, or 3 microns or less. Normally the dielectric constant of the membrane material is 7 or less, sometimes less than 6, 5, or 4 depending on the particular material used. While normally using a membrane substrate with a lower dielectric constant is unsuitable, using a significantly thinner substrate together with a material having a lower dielectric constant raises the theoretical frequency range of effective signal transmission to hundreds of GHz. The significantly thinner substrate material permits positioning the lower bias layer significantly closer to the signal traces than the relatively thick ceramic substrate, and therefore tends to more tightly confine the electromagnetic fields.

[0051] When a probe tip of a membrane based probe head comes into contact with a probe pad, as in most probes, it tends to skate across the pad as additional pressure is exerted. This skating is the result of the angled probe and/or co-axial cable flexing while under increasing pressure against the probe pad. A limited amount of skating is useful to "scrub" away oxide layers, or otherwise, that may build up on the probe pad. In many cases the probe pad is typically relatively small and excessive skating from the application of slightly too much pressure results in the probe simply skating off the probe pad. In addition, if excessive pressure is exerted damage to the probe and/or probe pad may result. Accordingly, there is an acceptable range of pressure and skating that should be maintained.

[0052] A probe measurement system including a probe comprising a linear array of probe tips enables testing of a differential or balanced test structure with a single probe facilitating fabrication of the test structure in a saw street between dies on a wafer.

[0053] The detailed description, above, sets forth numerous specific details to provide a thorough understanding of the present invention. However, those skilled in the art will appreciate that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuitry have not been described in detail to avoid obscuring the present invention.

[0054] All the references cited herein are incorporated by reference.

[0055] The terms and expressions that have been employed in the foregoing specification are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims that follow.

I (we) claim:

1. A probe for testing a differential test structure having a plurality of probe pads, said probe comprising:

(a) a first probe tip operable to conduct a first mode component of a first differential signal;

(b) a second probe tip proximate said first probe tip and operable to conduct a first mode component of a second differential signal;

(c) a third probe tip proximate said second probe tip;

(d) a fourth probe tip proximate said third probe tip and operable to conduct a second mode component of said second differential signal together with conduction of said first mode component of said first differential signal by said first probe tip; and

(e) a fifth probe tip proximate said fourth probe tip and operable to conduct a second mode component of said first differential signal together with conduction of said first mode component of said second differential signal by said second probe tip; said first, said second, said fourth and said fifth probe tips being arranged in a substantially linear array and, with said third probe tip, co-locatable with respective probe pads of said test structure.

2. The probe of claim **1** wherein a source of said first differential signal comprises said respective probe pads of said test structure co-locatable with said first and said fifth probe tips.

3. The probe of claim **1** wherein a source of said second differential signal comprises said respective probe pads of said test structure co-locatable with said second and said fourth probe tips.

4. The probe of claim **1** wherein said third probe tip is interconnected to a source of a direct current.

5. The probe of claim **1** wherein said third probe tip is aligned substantially linearly with said linear array of said first, said second, said fourth and said fifth probe tips.

6. The probe of claim **5** further comprising:

(a) a sixth probe tip proximate said first probe tip; and

(b) a seventh probe tip proximate said fifth probe tip; said sixth and said seventh probe tips being arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips; interconnected to said third probe tip and co-locatable with respective probe pads of said test structure.

7. The probe of claim **6** wherein said third probe tip is interconnected to a source of a direct current.

8. A probe for testing a differential test structure having a plurality of probe pads, said probe comprising:

(a) a dielectric plate having a substantially planar first surface and a second surface;

(b) a first probe tip projecting from said first surface and operable to conduct a first mode component of a first differential signal;

(c) a second probe tip projecting from said first surface proximate said first probe tip and operable to conduct a first mode component of a second differential signal;

(d) a third probe tip projecting from said first surface proximate said second probe tip;

(e) a fourth probe tip projecting from said first surface proximate said third probe tip and operable to conduct a second mode component of said second differential signal together with conduction of said first mode component of said first differential signal by said first probe tip; and

(f) a fifth probe tip projecting from said first surface proximate said fourth probe tip and operable to conduct a second mode component of said first differential signal together with conduction of said first mode component of said second differential signal by said second probe tip; said first, said second, said fourth and said fifth probe tips being arranged in a substantially linear array and co-locatable with respective probe pads of said test structure.

9. The probe of claim **8** wherein a source of said first differential signal comprises said respective probe pads of said test structure co-locatable with said first and said fifth probe tips.

10. The probe of claim **8** wherein a source of said second differential signal comprises said respective probe pads of said test structure co-locatable with said second and said fourth probe tips.

11. The probe of claim **8** wherein said third probe tip is interconnected to a source of a direct current.

12. The probe of claim **8** wherein said third probe tip is aligned substantially linearly with said linear array of said first, said second, said fourth and said fifth probe tips.

13. The probe of claim **12** further comprising:

(a) a sixth probe tip proximate said first probe tip; and

(b) a seventh probe tip proximate said fifth probe tip; said sixth and said seventh probe tips being arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips; interconnected to said third probe tip and co-locatable with respective probe pads of said test structure.

14. The probe of claim **8** further comprising:

(a) a first conductor overlaying an area of said first surface and electrically interconnected with said third probe tip;

(b) a second conductor extending from said first surface to said second surface of said dielectric plate and electrically interconnected with said first conductor; and

(c) a conductor of direct current electrically interconnected with said second conductor.

15. The probe of claim **14** further comprising:

(a) a sixth probe tip projecting from said first surface proximate said first probe tip; and

(b) a seventh probe tip projecting from said first surface proximate said fifth probe tip, said sixth and said seventh probe tips being electrically interconnected with said first conductor and arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips and respectively co-locatable with probe pads of said test structure.

16. The probe of claim **8** further comprising:

(a) a first conductor overlaying an area of said second surface; and

(b) a second conductor extending from said second surface of said dielectric plate and electrically interconnecting said first conductor with a ground potential.

17. The probe of claim **8** wherein said dielectric plate is rigid.

18. The probe of claim **8** wherein said dielectric plate is flexible.

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