

[54] **ANIMATED DISPLAY AMUSEMENT
DEVICE**
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Hatboro, Pa.
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[51] Int. Cl. **A63f 9/14**
[58] Field of Search **273/86 R, 86 B;**
46/244 R, 244 A, 244 B; 180/2; 104/60, 149

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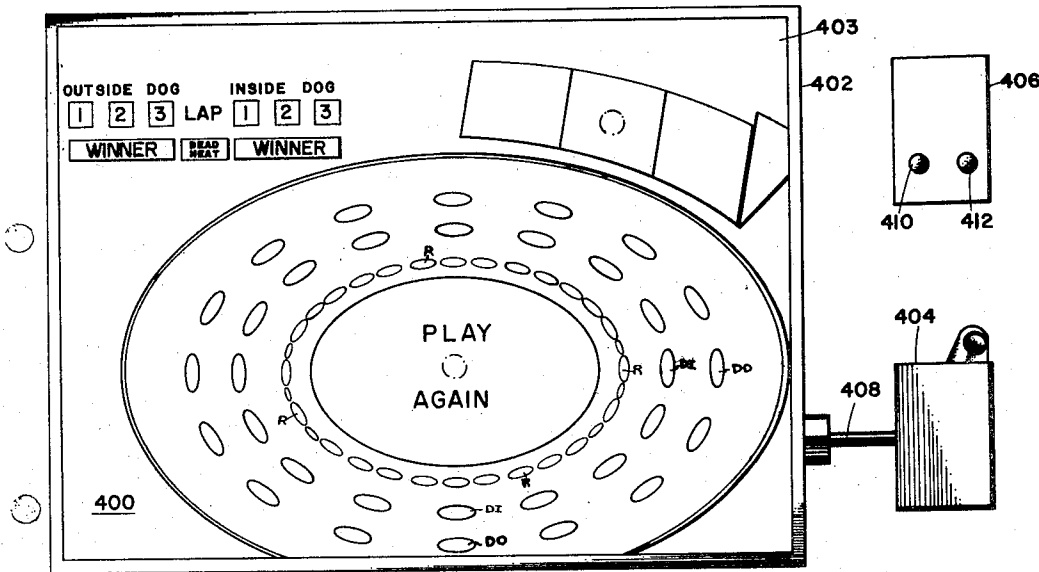
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323,304 1/1930 Great Britain **273/86 B**

Primary Examiner—Anton O. Oechsle
Attorney—A. D. Caesar et al.

[57] **ABSTRACT**

An animated amusement game having a board on which there is displayed a pair of dogs individually and sequentially advancing around the track. A rabbit is displayed as constantly circling the track and passing the dogs disposed thereon. A radio transmitter provides a multiplexed signal to electronic circuitry for controlling the individual advancement of the dogs in response to player actuated buttons on the transmitter which are associated with the respective dogs. Each dog advances a maximum distance if the player actuated button associated therewith is released at the moment that the rabbit passes the dog.

8 Claims, 16 Drawing Figures



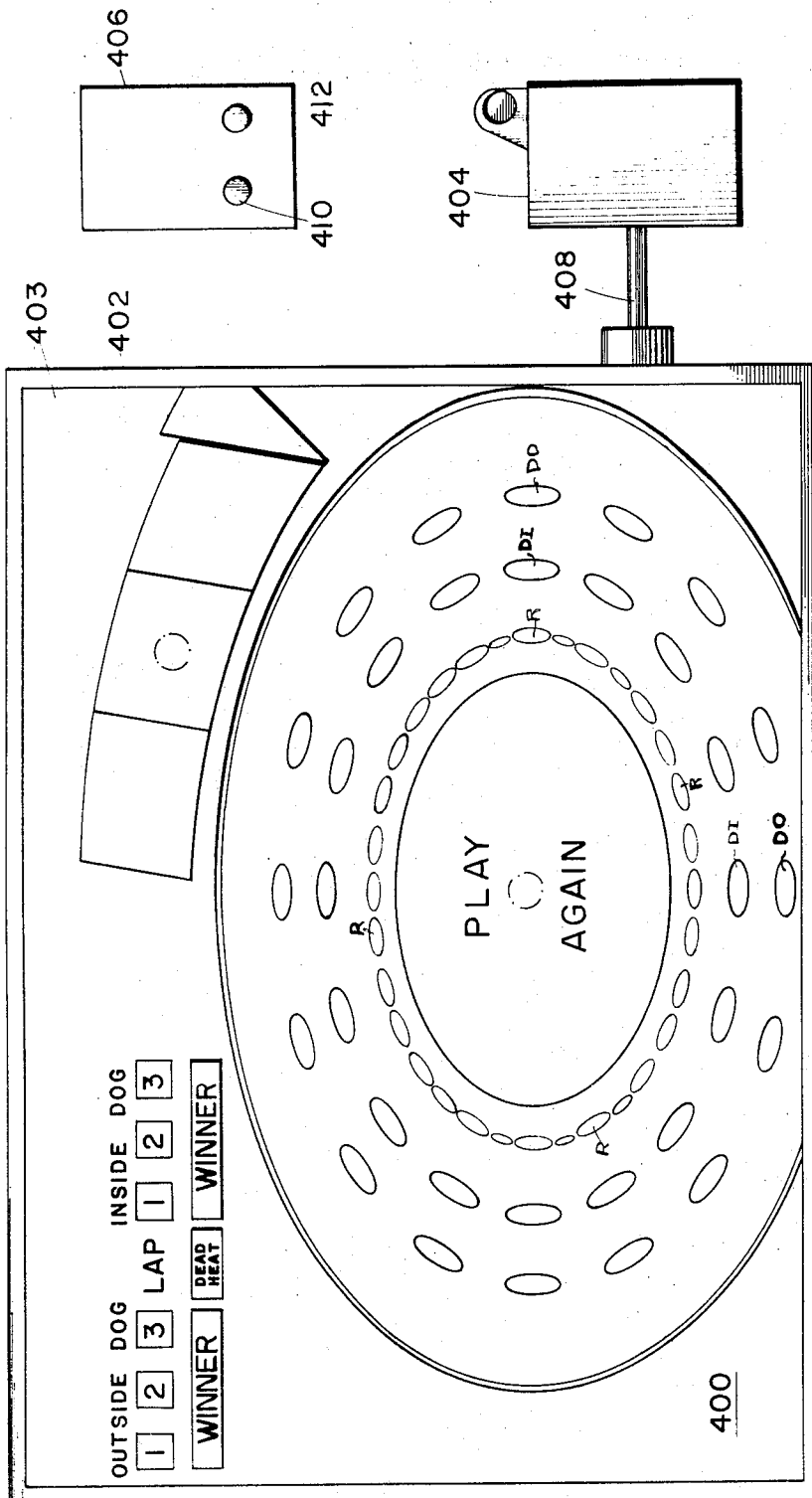
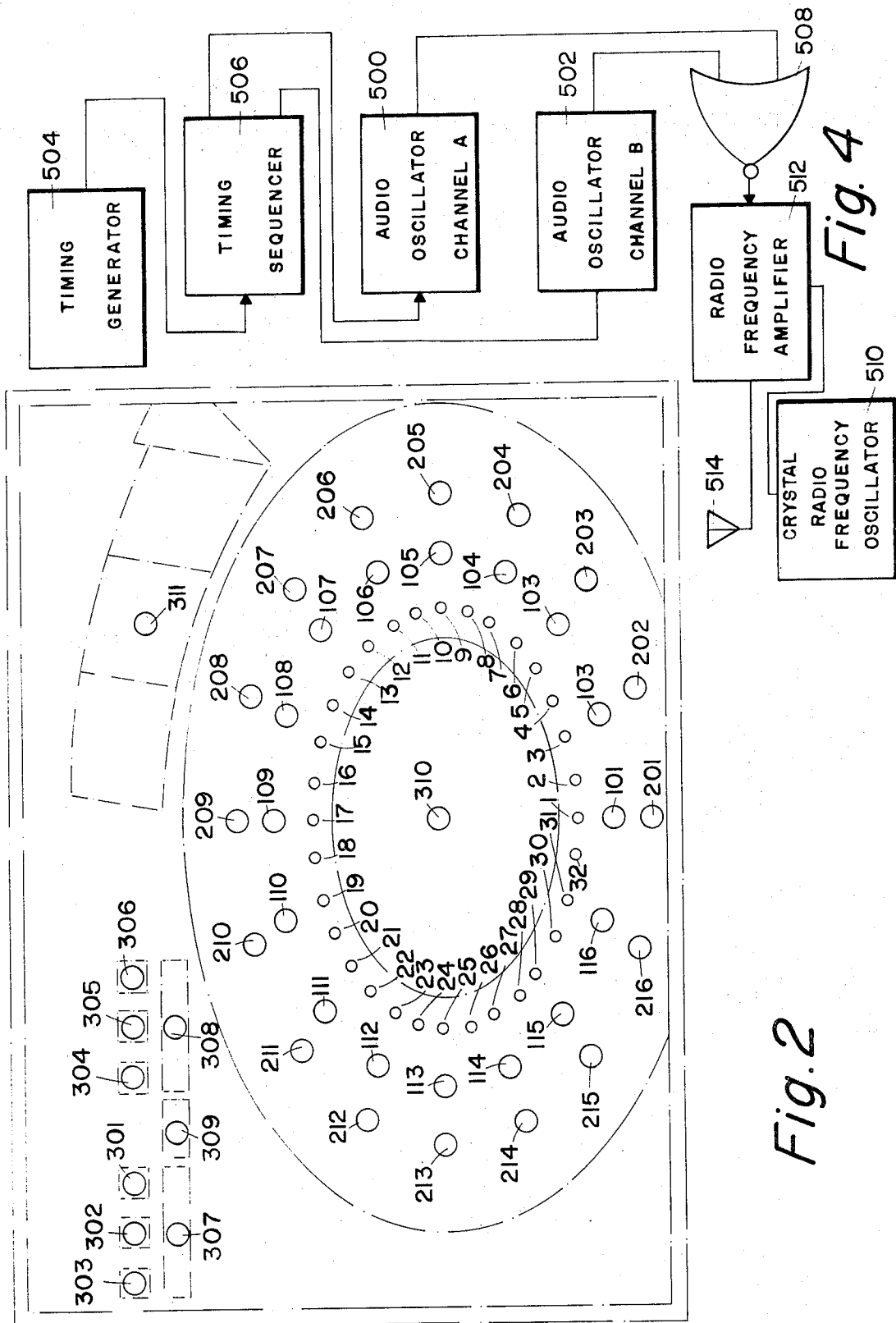
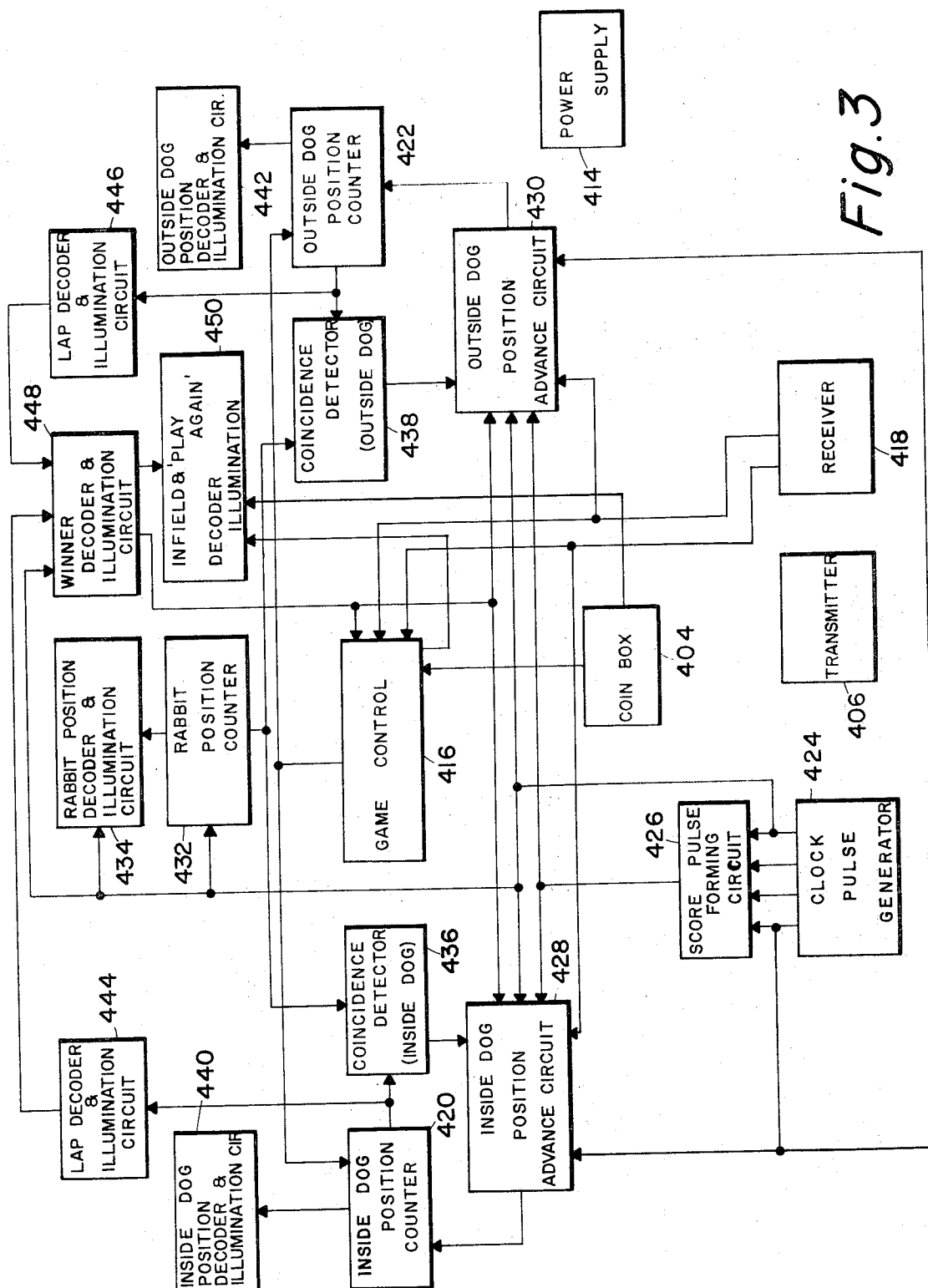


Fig. 1





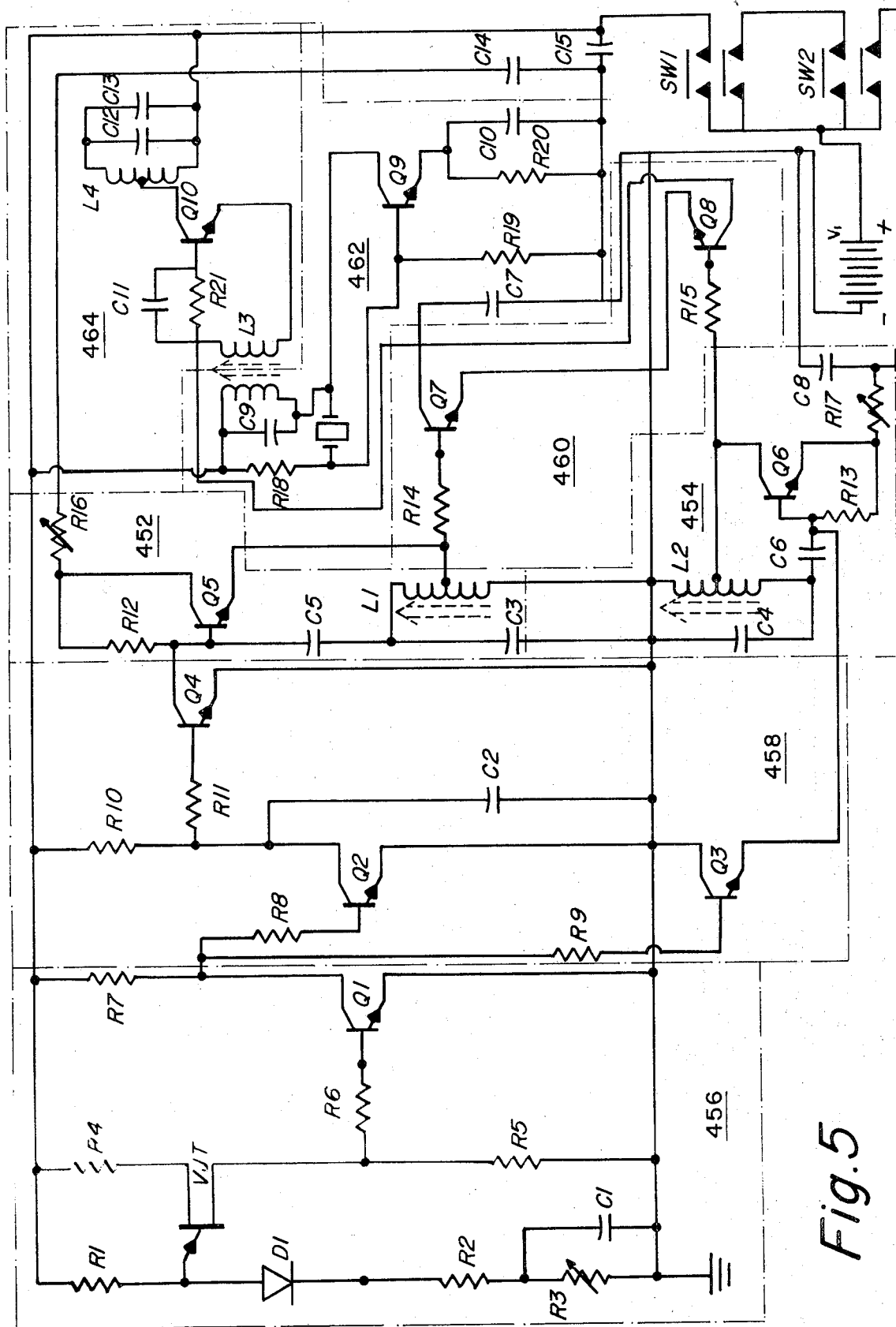


Fig.5

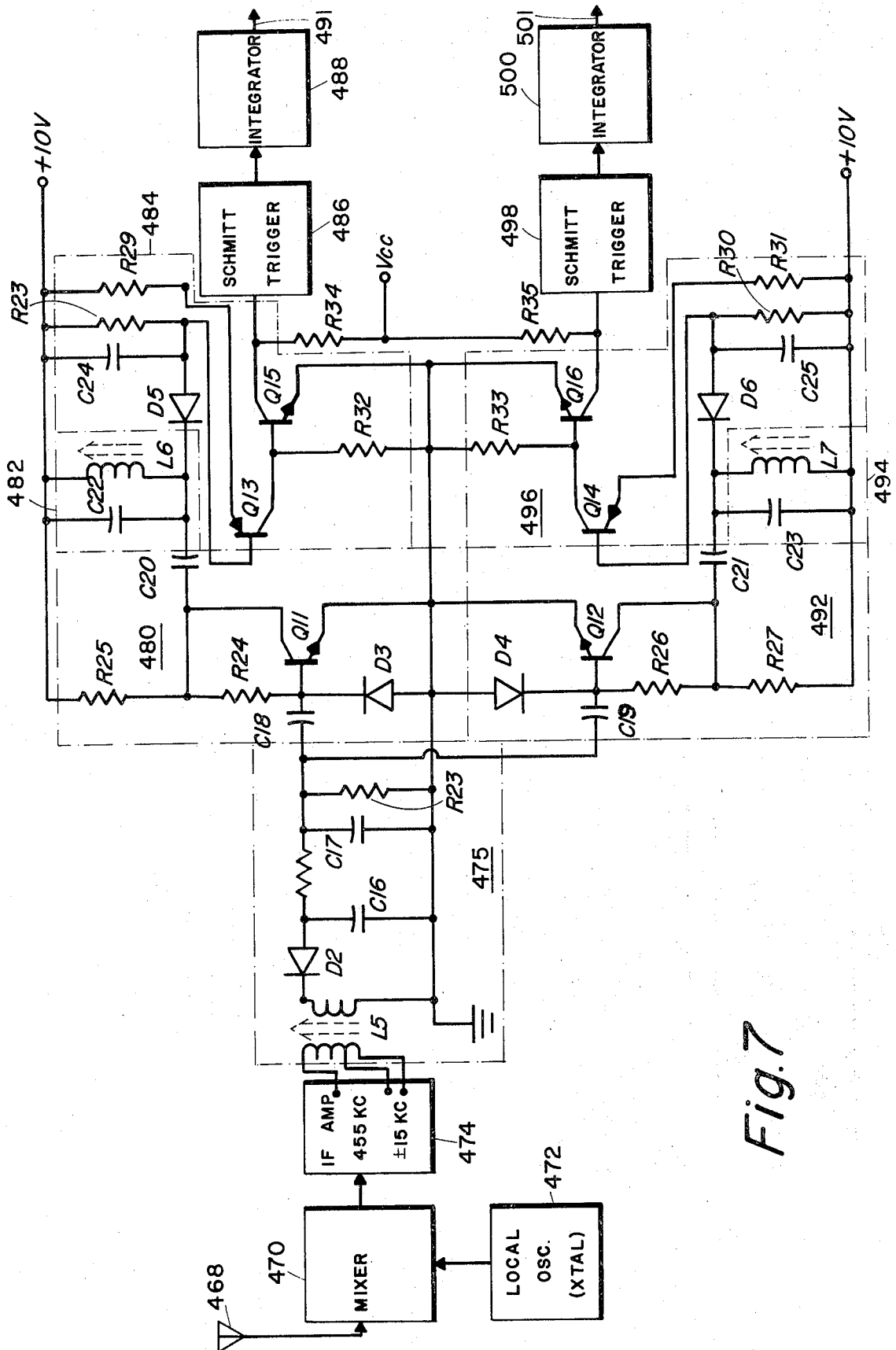


Fig. 7

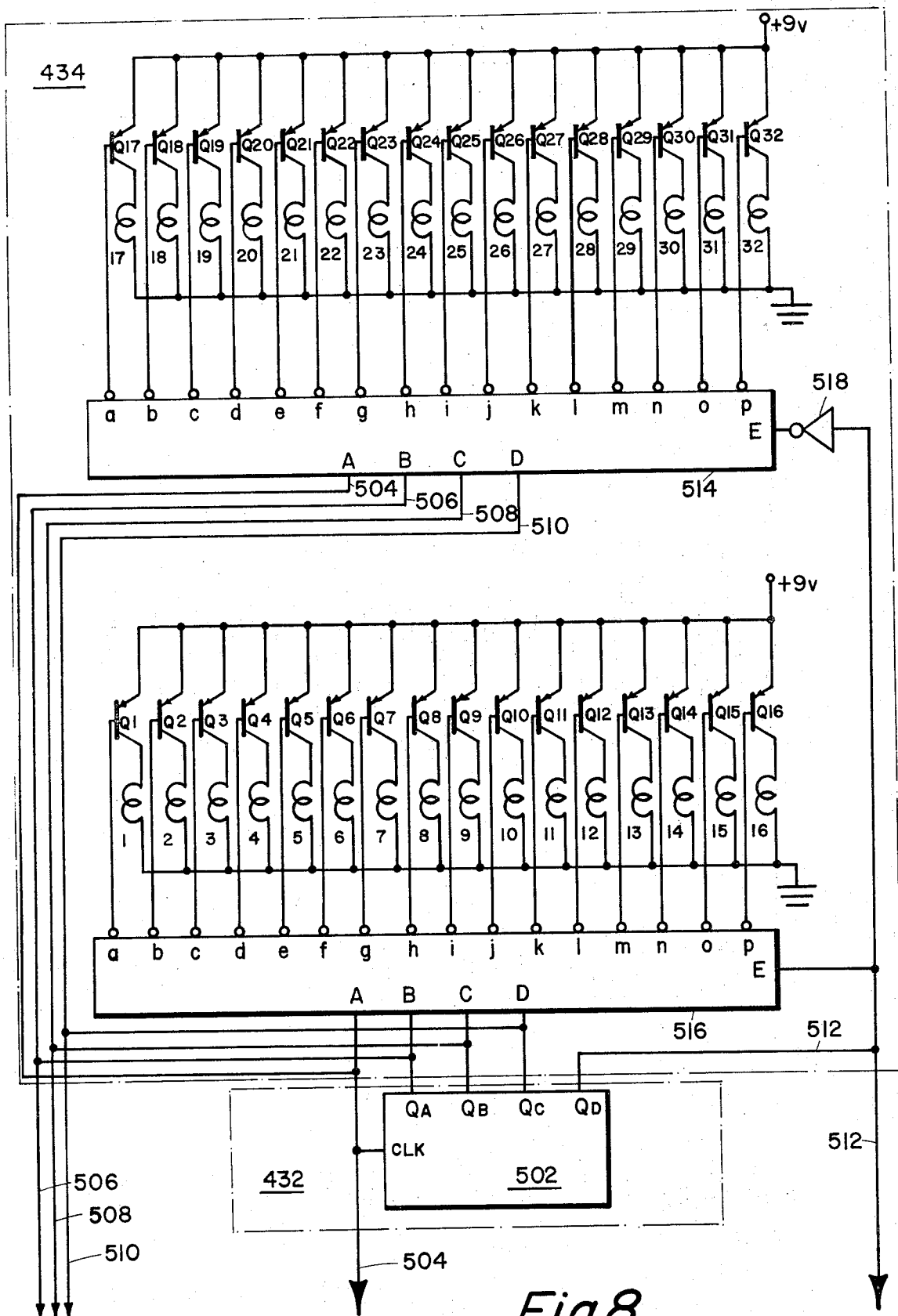


Fig. 8

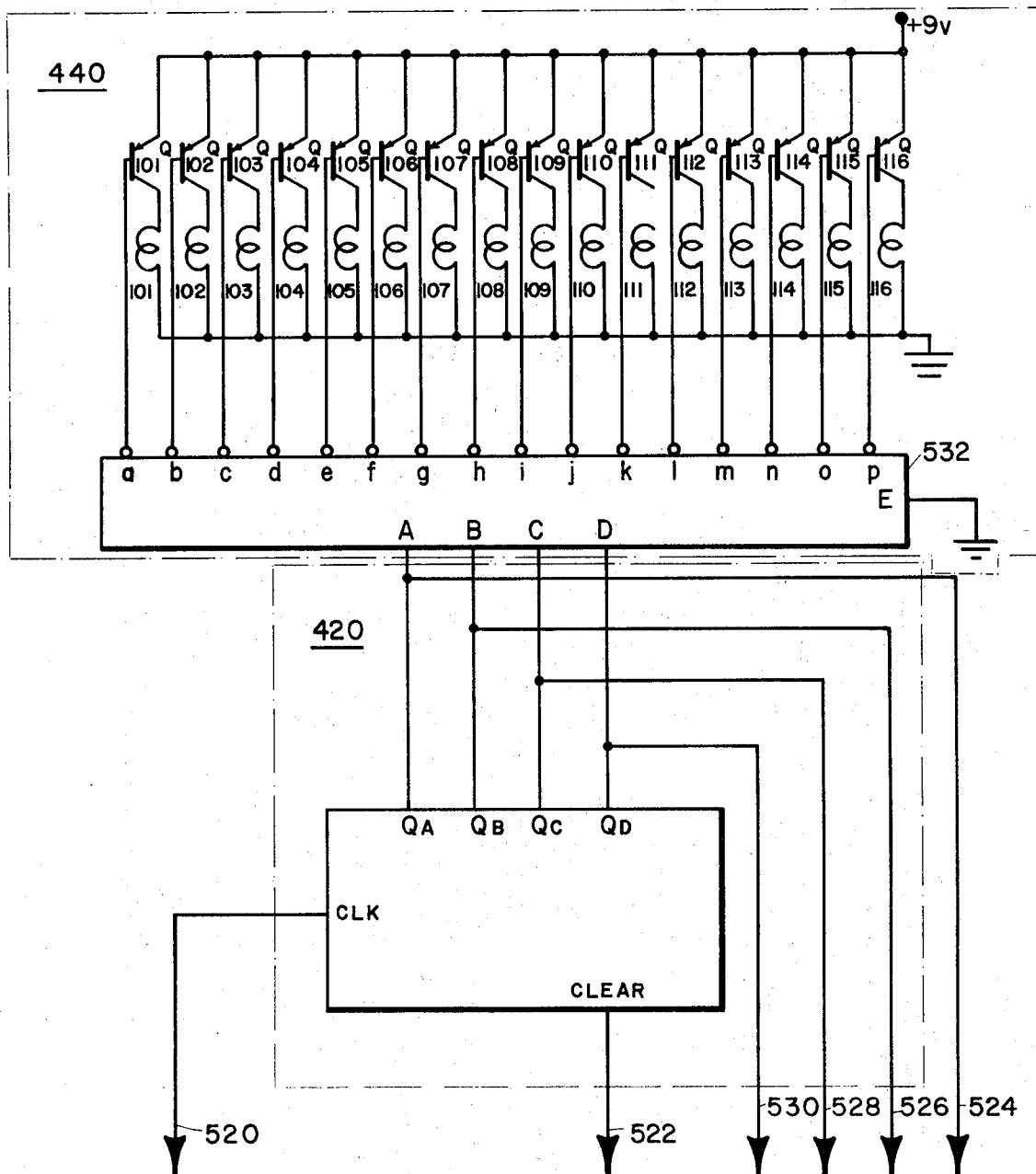


Fig. 9

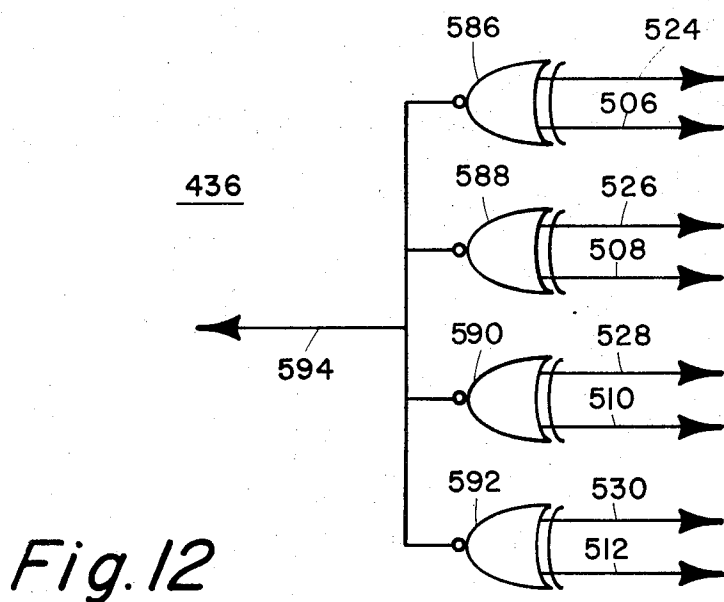


Fig. 12

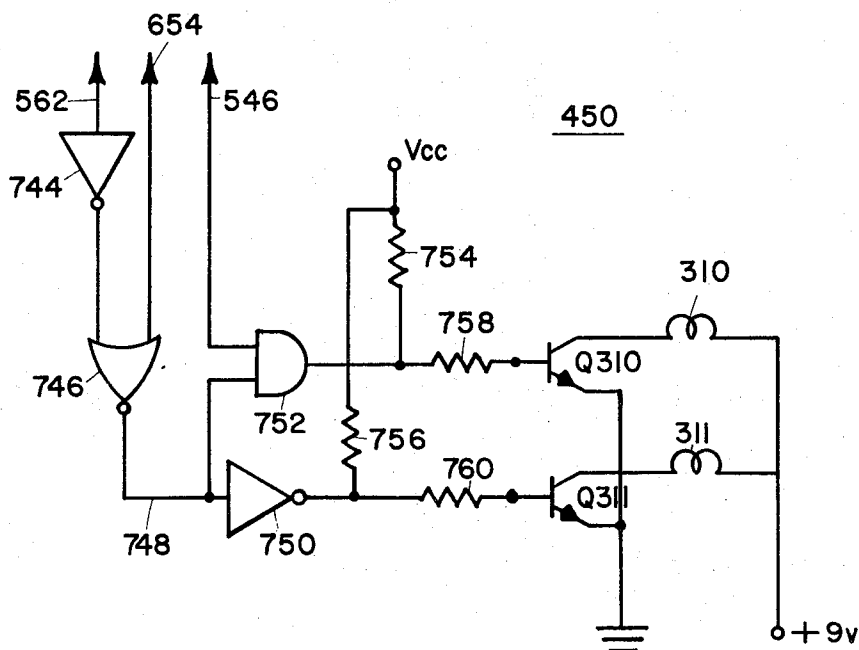


Fig. 16

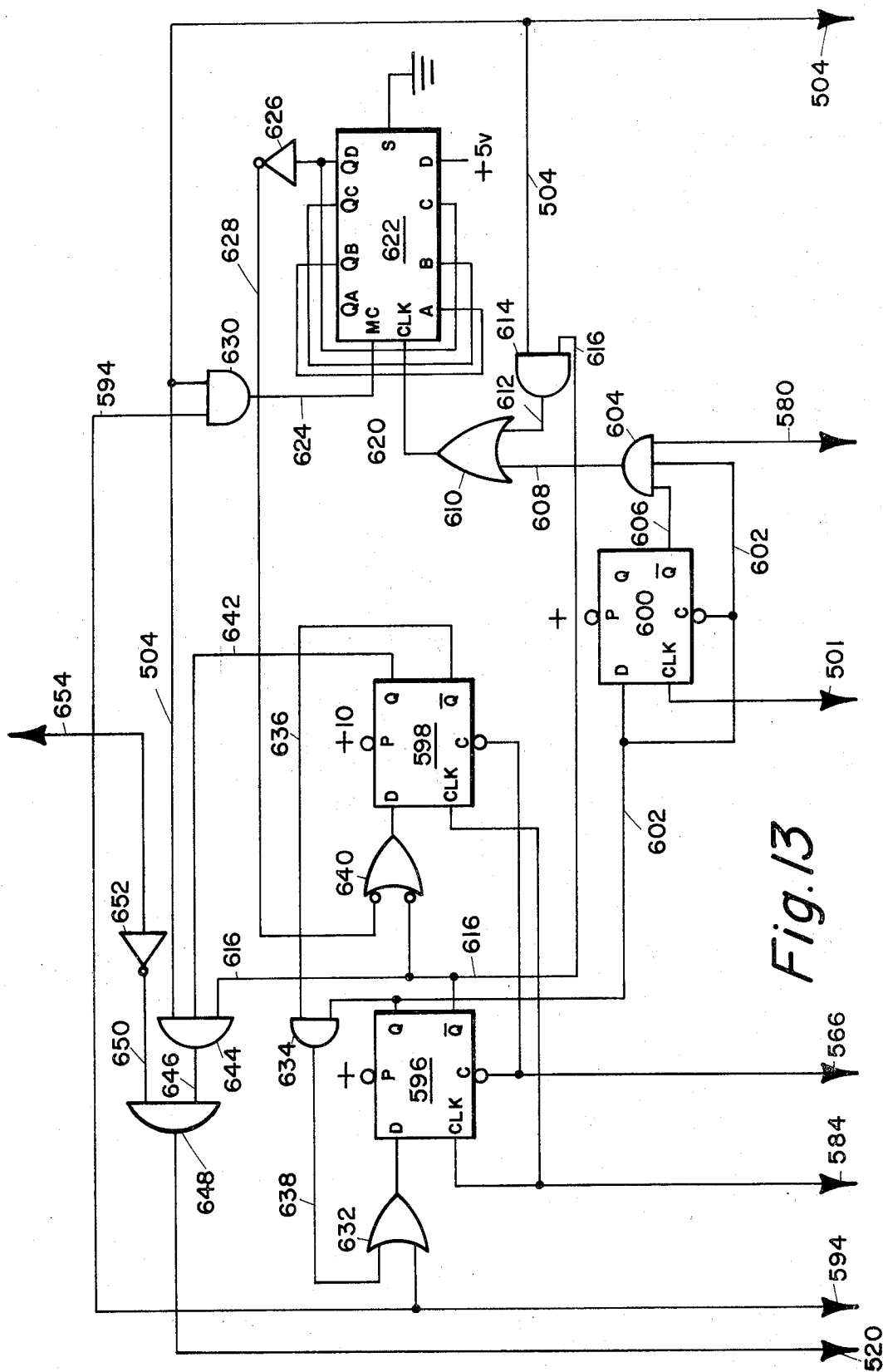


Fig. 13

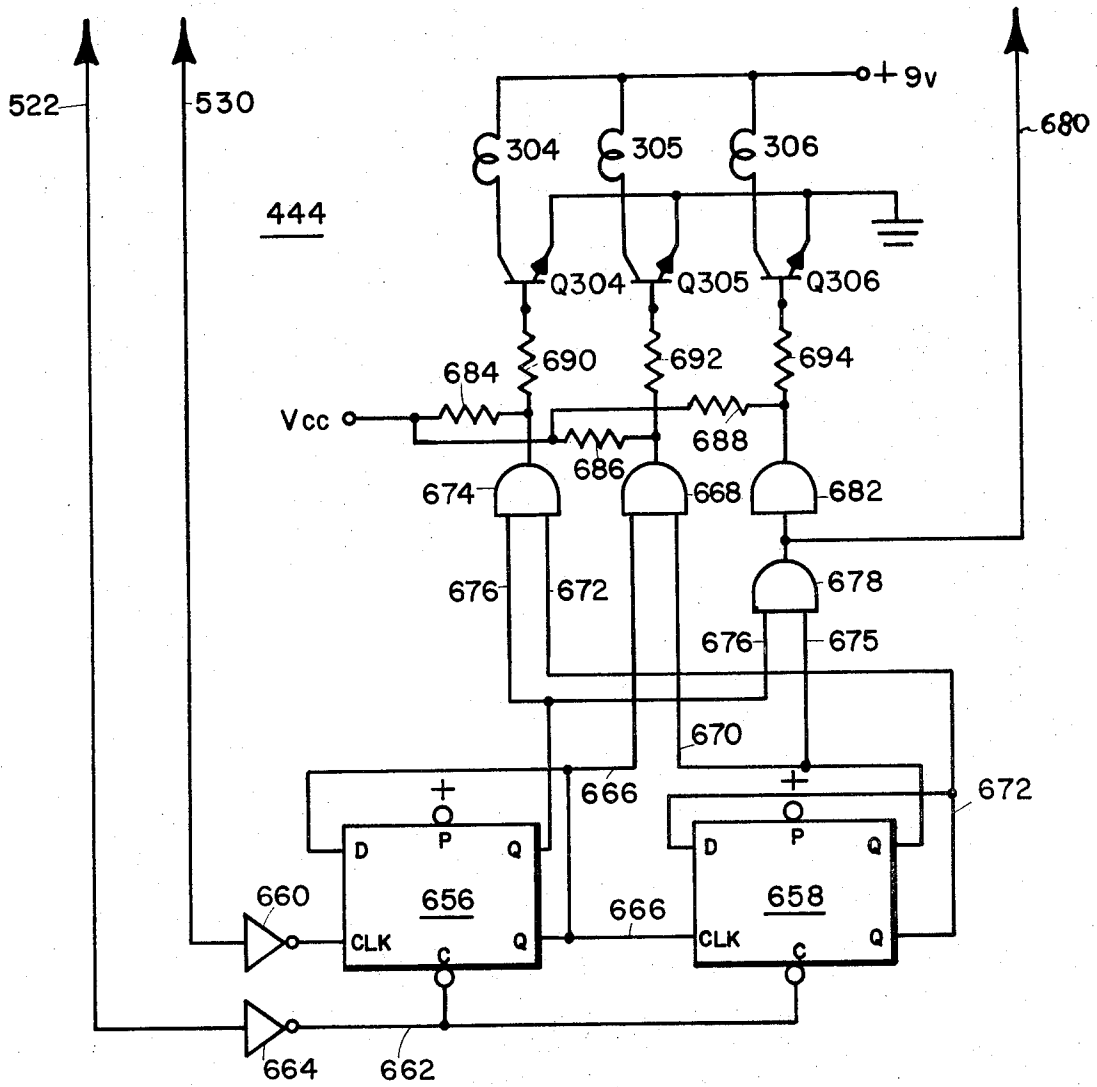
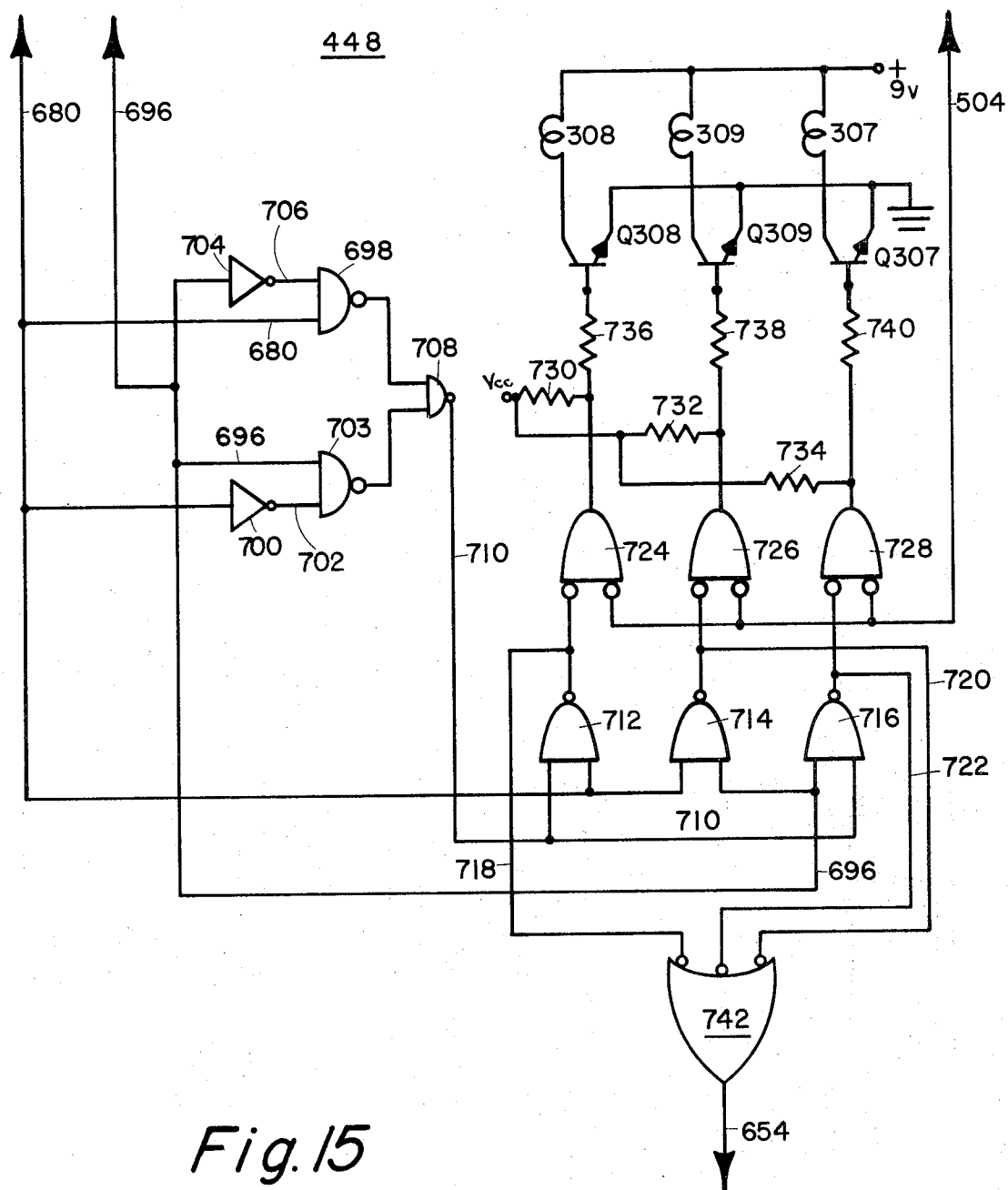


Fig.14



ANIMATED DISPLAY AMUSEMENT DEVICE

This invention relates generally to amusement devices and more particularly to animated display amusement games requiring player skill in responding to visual conditions.

With the increasing amount of leisure time enjoyed by people in today's society, there is a growing demand for amusement devices and games for recreational use.

To that end, various amusement devices and games, utilizing animated displays, are commercially available. Although many of such games are arranged to have players compete against one another for score, such games generally do not require much skill of the players to attain a high score and win.

In copending U.S. Pat. application Ser. No. 289,491 and filed on Sept. 25, 1972 which is assigned to the same assignee as this invention, there is disclosed and claimed an electronic game which requires a high degree of player skill in responding to visual condition to attain a high score and win. That game includes a board which displays in an animation sequence, two figures alternately taking turns cocking their arms and throwing a dart at a target. The point at which the figure releases his dart always occurs at the same point in the animation sequence. The game also includes electronic circuitry therein for effectuating the animation sequence and a transmitter which establishes a command signal in response to actuation by a player. If the player actuates the transmitter at the precise moment in the animation sequence that the figure is displayed releasing his dart, the dart impacts the bullseye of the target and a maximum score is attained. If the transmitter is actuated either before or after that moment, the dart will miss the bullseye and a lesser score will result, the longer the delay either before or after release of the dart that the player actuates the transmitter, the lower the score attained.

It is a general object of this invention to provide an amusement game having an animated sequence, which game tests the skill of a player to manually respond to a visual condition in the animation sequence.

It is a further object of this invention to provide an animated sequence amusement game which tests the skill of a player to manually respond to a visual condition in the animation sequence and which condition occurs at different points therein during consecutive sequences.

It is still a further object of this invention to provide an animated sequence amusement game which tests the skill of a player to manually respond to a visual condition in the animation sequence, which condition occurs at different points in the animation sequence depending upon the skill of the player in responding to the visual condition in the immediately prior sequence.

It is still a further object of this invention to provide an animated sequence amusement game utilizing a single channel radio signal to control the sequencing of two figures which are displayed racing against one another.

It is yet a further object of this invention to provide an animated amusement game wherein two figures are displayed racing against one another, the individual advancement of said figures being controlled by different players via a transmitted multiplexed radio signal.

The foregoing as well as other objects of the invention are achieved by providing an animated amusement

game including a display board, first means for establishing an animated display of a first object sequentially moving along a first path made up of plural positions on the board and second means for establishing an animated display of the second object sequentially moving along a second path made up of plural positions on the board. The second path is adjacent to the first path. The first means is arranged such that the first object overtakes and passes the second object. The second means is operative in response to first player actuated means wherein the second object advances a predetermined number of positions if the first player actuated means is operated at the moment that the first object overtakes the second object, whereas the second object advances a lesser number of positions if the first player actuated means is operated before or after said moment.

Other objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with accompanying drawing wherein:

FIG. 1 is a front elevational view of an amusement game in accordance with the preferred embodiment of this invention;

FIG. 2 is an enlarged elevational view of the arrangement of the illumination lamps for the board;

FIG. 3 is a functional schematic block diagram of the electronic circuitry forming the game shown in FIG. 1;

FIG. 4 is a functional schematic block diagram of the transmitter of the invention herein;

FIG. 5 is a schematic diagram of the transmitter;

FIG. 6 is a functional schematic block diagram of the receiver of the invention herein;

FIG. 7 is a schematic and functional block diagram of the receiver;

FIG. 8 is a schematic circuitry and block diagram of the rabbit advancing circuitry;

FIG. 9 is a schematic circuitry block diagram of one of the dog position counter and illumination circuit therein;

FIG. 10 is a schematic drawing of the logic of the game control circuitry;

FIG. 11 is a schematic drawing of logic of the scoring pulse forming circuit;

FIG. 12 is a schematic drawing of the logic coincidence detector circuits;

FIG. 13 is a schematic logic of the dog advancing circuits;

FIG. 14 is a schematic circuit block diagram of the lap decoder and illumination circuit;

FIG. 15 is a schematic logic diagram of the winner decoder and illumination circuit;

FIG. 16 is a schematic circuit block diagram of the infield and play again decoder and illumination circuits.

Referring now in greater detail to the various figures of the drawing wherein like reference characters refer to like parts, an animated display electronic amusement game embodying the present invention is shown at 400 in FIG. 1. As can be seen game 400 includes a board 402, a coin box 404 and a transmitter 406.

The board 402 includes a front face 403 upon which is graphically represented a race track. The race track is oval in shape and disposed about its inner rail are graphical representations 32 rabbits, each of said rabbits being represented by an oval R each of which being

equally spaced about the periphery of the inside rail of the track. A first set of 16 dogs are graphically represented by 16 ovals DI equally spaced around the track and adjacent to the rabbits. A second second set of 16 dogs are graphically represented by 16 ovals do spaced

around the track adjacent and outside of the first set of dogs. The two sets of dogs are arranged such that each dog of one set is substantially radially aligned with a corresponding dog of the second set and with two rabbits.

In the upper left hand corner of the board there is the legend "Outside Dog." Below this legend are numerals 1, 2 and 3. The legend "Winner" appears on the board immediately below said numerals. The upper left hand corner of the board also includes the legend "Inside Dog." Below this legend there appears numerals 1, 2 and 3. The legend "Winner" appears between the sets of numerals and the legend "Dead Heat" appear under the legend "Lap." In the upper right hand corner of the board a grandstand or infield is graphically represented.

In the center of the oval track there appears the legend "Play Again."

Board 402 includes a plurality of lamps which are disposed behind the front face 403 of the board at selected points. The lamps are shown schematically by circles on the face of the board.

The lamps are arranged to be illuminated in a sequence to result in animating the figures on the board such that a rabbit appears to be running around the track and that a dog immediately adjacent the rabbit, hereinafter called the inside dog, and a dog outside of the inside dog, hereinafter called the outside dog, also appears to be running around the track.

Logic circuitry is provided within the board 402 to establish the animation sequence, when enabled by the insertion of a coin in a coin slot in the coin box 404 and in response to signals received from the transmitter 406. An electrical cable connects the coin box to the circuitry inside board 402.

Transmitter 406 is a R. F. transmitter and includes a pair of buttons 410 and 412. The depression and release of button 410 controls the sequencing of the inside dog and depression and release of transmitter button 412 controls the sequencing of the outside dog.

The object of the game is to have one's dog (i.e. either the inside or outside dog) complete three laps of the track before the opponent's dog completes the three laps. The game is arranged such that the rabbit constantly encircles the track. If the transmitter button associated with a player's dog is released at the precise moment that the rabbit passes that dog, the dog will advance four positions, advancing one position at a time as as to appear as if it is running. If the player released the button either before or after the moment of coincidence, a lesser dog advance occurs, depending upon how early or how late the button is released. Even if the button is not released the dog will nevertheless advance one position. If the button is released it should be redressed after the dog advances to prepare the transmitter for the next pass of the rabbit. To that end when the rabbit has circled the track and is coincident with the dog in its advanced position, the transmitter button should again be released to effectuate the maximum advance of the dog around the track.

The transmitter is operative to provide the signals to both dogs, to effectuate their advance, over a single

radio channel, even if both buttons are released at the same time and irrespective of whether or not the dogs are beside one another.

Each time that a dog completes a lap of the track, the board lights up indicating the number of laps so completed. When a dog completes three laps the board lights up with the legend "Winner." If both dogs complete three laps at the same time the board lights up with the legend "Dead Heat." Upon either dog winning or upon a dead heat, the infield lights up for a preselected period of time and thereafter goes out at which time the legend "Play Again" in the center of the track lights up. The game is now reset for subsequent play.

As should be appreciated the game requires a high degree of player skill to coordinate the release of the button with the visual display of the coincidence of rabbit and a dog particularly so since the position at which the rabbit and the dog become coincident changes with each succeeding lap of the rabbit.

FIG. 2 shows the arrangement of the lamps with respect the board 402. As can be seen therein lamps 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, and 32 are respectively behind disposed the 32 graphically represented rabbits on the face of the board.

In a similar manner lamps 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, and 116 are respectively disposed behind the 16 graphically represented inside dogs and lamps, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215 and 216 are respectively disposed behind the sixteen graphically represented outside dogs.

Lamps 301, 302, 303 are disposed behind the numerals 1, 2 and 3 respectively, under the legend "Outside Dog" on the face of board 402. Lamps 304, 305 and 306 are disposed behind the numerals 1, 2 and 3, respectively, under the legend "Inside Dog" on the face of board 402. Lamp 307 is disposed behind the legend "Winner" and under the legend "Outside Dog" and lamp 308 is disposed behind the legend "Winner" and under the legend "Inside Dog." Lamp 309 is disposed behind the legend "Dead Heat." Lamp 310 is disposed behind the legend "Play Again" at the center of the oval track and lamp 311 is disposed behind the infield in the upper right hand corner of the board.

The rabbit lamps 1 through 32 are lit in sequential order, which order repeats continuously such that the rabbit constantly circles the track.

Lamp 101 through 116 are lit in sequential order such that the inside dog appears to run around the track. However, only up to four of said lamps are lit during any lap by the rabbit (the four lamps being sequentially lit when the transmitter button is released at the optimum time) such that the inside dog does not advance more than four positions during each lap of the track by the rabbit. The lamps 201 through 216, which define the animation sequence for the outside dog, are lit in a similar manner to the lamps 101 through 116 forming the animation sequence for the inside dog.

FIG. 3 is a functional block diagram of the logic and electrical circuitry for game 400. As can be seen therein, game 400 includes a power supply 414 which is suitably connected to the various components of the circuitry illumination power to the circuitry of the game.

The logic circuitry of the game includes Game Control Circuit 416. The Game Control Circuit includes one input connected to the output of the Coin Box 404 and another input connected to the output of Receiver 418. The output of the Game Control Circuit is connected as an input to Inside Dog Position Counter 420 and as an input to the Outside Dog Position Counter 422.

A clock pulse generator 424 is connected to and provides 30 hz clock pulses, 15 hz clock pulses, 7.5 hz clock pulses and 3.75 hz clock pulses inputs to the Scoring Pulse Forming Circuit 426. The 3.75 hz clock pulse output is also connected as an input to the Inside Dog Position Advance Circuit 428, the Outside Dog Position Advance Circuit 430, the Rabbit Position Counter 432, the Rabbit Position Decoder and Illumination Circuit 434 and the Winner Decoder and Illumination Circuit 448. The 30hz output is also connected to input terminals of the inside and outside dog advance circuits 428 and 430, respectively.

An output of Receiver 418 is connected to an input of the Inside Dog position Advance Circuit 428, another output of the Receiver is connected to an input the Outside Dog Position Advance Circuit 430.

The output of the Rabbit Position Counter Circuit 432 is connected to an input of the Coincidence Detector Circuit 436 and the Coincidence Detector Circuit 438. A second input to Coincidence Detector 436 is connected to an output of the Inside Dog Position Counter 420. A second input of the Coincidence Detector 438 is connected to an output of the Outside Dog Position Counter 422. The output of Coincidence Detector 436 is connected to an input of the Inside Dog Position Advance Circuit 428 and the output of the Coincidence Detector 438 is connected to an input of the Outside Dog Position Advance Circuit 430.

The output of Inside Dog Position Counter 420 is connected to the input of the Dog Position Decoder and Illumination Circuit 440 and the output of the Outside Dog Position Counter 422 is connected to the Inside Dog Position and Illumination Circuit 442. Another output of the Inside Dog Position Counter 420 is connected to an input of the Lap Decoder and Illumination Circuit 444 and a second output of the Outside Dog Position Counter 422 is connected to the Lap Decoder and Illumination Circuit 446. The output of the Lap Decoder and Illumination Circuit 444 and the Lap Decoder and Illumination Circuit 446 are connected to inputs of the Winner Decoder and Illumination Circuit 448. An output of Winner Decoder Illumination Circuit 448 is connected as an input to Game Control Circuit 416. Other outputs of the Winner Decode and Illumination Circuit 448 are connected to the Infield and Play Again Decoder and Illumination Circuit 450 and to the dog advance circuits 428 and 430. The Infield and Play again Decoder and Illumination circuit 450 includes a second input which is connected to an output of the Game Control Circuit 416 and a third input which is connected to the Coin Box 103.

Operation of the game is as follows: Upon the power supply 414 being energized, Inside and Outside Dog Position Advance Circuits 428 and 430 are cleared and enabled for operation. Upon receipt of a coin in the Coin Box, a signal is provided therefrom to Game Control Circuit 416. At this time circuit 416 is in its "Idle" condition wherein, in response to the signal from the coin box it provides a reset signal to the Inside Dog Po-

sition Counter 420 and to the Outside Dog Position Counter 422. This signal precludes any dog from advancing so long as the signal persists.

Upon either button 410 or 412 in the Transmitter being depressed, a multiplexed radio frequency signal is transmitted by the transmitter and is received by Receiver 418. The receiver provides a signal to the Game Control Circuit 416 which causes that circuit to switch from its "Idle" condition (wherein it supplies reset signals to the outside and inside dog position counters to disable them) to a "Play" condition (wherein it ceases providing reset signals thereto).

As soon as the power supply 414 is energized the Clock Pulse Generator 414 provides clock signals at its output terminals. The 3.75hz clock pulse output signals therefrom are provided as an input to the Rabbit Position Counter 432 and into the Rabbit Position Decoder and Illumination Circuit 434, whereupon lamps 1 through 32 therein light sequentially, such that rabbit appears to run around the track.

The output signal of the Inside Dog Position Counter 420 is provided to the Inside Dog Position Decoder and Illumination Circuit 440 to effectuate the illumination of lamp 101 which lights up the image of the inside dog at the start position. In a similar manner the output signal of the outside Dog Position Counter 422 is provided to the Outside Dog Position Decoder and Illumination Circuit 442 to effectuate the illumination of lamp 201 which lights up the image of the outside dog at the start position.

At the beginning of the game no laps will have been completed, thus the output of the Inside Dog Position Counter 420, as decoded by the decoder and circuit 444, results in all of the lamps in said latter circuit being out. In a similar manner decoder circuit 446 decodes the position of the Outside Dog Position Counter 422 such that all of the lamps in the circuit 446 are out.

Upon the Rabbit Position Counter completing one cycle, i.e., upon the rabbit completing one transversal of the track, the Coincidence Detectors 436 and 438 provide signals to the Inside Dog Position Advance Circuit 428 and the Outside Dog Position Advance Circuit 430, respectively. In response to the occurrence of the signals from the coincidence detectors, 30hz clock pulses are provided to registers within each of the dog advance circuits. The registers are four stage registers, which are adapted for either serial or parallel operation. In response to the signals from the coincidence detectors indicating that the rabbit is coincident with a dog, the register associated therewith switches to parallel operation wherein at the occurrence of the first 30hz clock pulse, a first stage therein goes high, at the occurrence of the second 30hz clock pulse the first and second stages go high, at the occurrence of the third 30hz clock pulse the first, second and third stages go high and at the occurrence of the fourth 30 hz clock pulse all of the stages are high, i.e., all stages are high at the point in time that the rabbit passes the dog. At the point in time that the rabbit passes the dogs the players controlling the inside and outside dogs should release their associated transmitter buttons to effectuate the maximum advance of their dogs.

Assuming that the player associated with the inside dog releases his button at the moment the rabbit passes his dog and that the player associated with the outside dog is very slow to react and fails to release his button at all, operation is as follows.

Insofar as the inside dog is concerned, the input signal received from receiver 418 causes a register within the Inside Dog Position Circuit 428 to begin shifting high signals therein in response to 30hz pulses from the clock pulse generator 424. At the precise moment that the rabbit just passes the dog, the register inside the dog position advance circuit is completely full, i.e., it contains four high signals therein.

Insofar as the outside dog is concerned it's associated advance circuit operates in the identical manner as the Inside Dog Position Advance Circuit, up until the moment the rabbit passes the outside dog.

Upon release of transmitter button 410, Receiver 418 provides a signal to the Inside Dog Position Advance Circuit which causes the register therein a stop counting (i.e., disables the register). The failure to release button 412 does not result in the disabling of the counter in the Outside Dog Position Advance.

At the end of the coincidence interval (i.e., when the rabbit passes a dog) both of the coincidence detectors 436 and 438 provide signals to their associated position advance circuits, which signals cause the registers therein to shift into a serial mode of operation wherein low signals are shifted into the register. Since Receiver 418 is providing signals to the position advance circuit 428 to preclude its register from shifting, the register remains full even though the signal from the coincidence detector 436 indicates the lack of coincidence. Insofar as the Outside Dog Position Advance Circuit is concerned, the Coincidence Detector, 438 provides a signal indicating that the outside dog and rabbit are not longer coincident. This signal, in conjunction with the 30hz clock pulses applied to the register, now in its serial mode of operation, causes the register to start emptying, i.e., to shift lows therein.

The dog position advance circuits are operative to provide clock pulses to the clock inputs of their associated dog position counters so long as a high input remains on the first stage output of their registers. The advance circuits are also operative (as will be explained later to provide a clock pulse to their associated dog counter even if their registers are empty at the occurrence of the first 3.75hz clock pulse after the rabbit passes the dogs associated therewith.

The Scoring Pulse Forming Circuit 426 enables every eighth 30hz pulse from the clock pulse generator to be provided to both the Inside Dog Position Advance Circuit and to the Outside Dog Position Advance Circuit 430. These signals called scoring pulses cause flip-flops in the Inside Dog Position Advance Circuit and the Outside Dog Position Advance Circuit to change states, whereupon during the second 3.75 hz interval after the rabbit passes the dog, a first 3.75 hz clock pulse is provided to the Inside Dog Position Counter and to the Outside Dog Position Counter. Accordingly, both the inside and Outside dogs advance one position.

The Inside Dog Position Decoder and Illumination Circuit 440 detects the counter position, such that lamp 102 illuminates. In a similar manner the Outside Dog Position Decoder and Illumination Circuit 442 detects the position of Outside Dog Counter 422 and illuminates lamp 202 in response thereto.

The second 3.75 hz clock pulse following the moment at which the rabbit passes the dogs, causes the last stage in the register of the Inside Dog Position Advance Circuit 428 to empty whereas, the register in the Outside Dog Position Counter will have completely emp-

tyed by this point in time (as a result of being clocked by the 30 hz pulses from the clock pulse generator from the time the register shifts into its serial mode of operation). The next successive 3.75 hz pulse (i.e. the third 3.75 hz pulse after the rabbit passes the dog), to appear at the output of the Inside Dog Position Advance Circuit clocks the Inside Dog Position Counter 420 to cause the counter to advance to a second position. The Inside Dog Position Decoder and illumination Circuit 440 decodes the counter position and illuminates lamp 103. At the same time the Outside Dog Position Advance Circuit 430 does not provide any 3.75 hz pulses to the Dog Position Counter 422 since the register in the advance circuit is empty. Accordingly, the dog position counter 422 remains its first position whereupon, the lamp 202 remains lit.

Upon the occurrence of the second clock pulse to the clock input of the Inside Dog Position Counter the fourth and third stages of the register in the Dog Position Advance Circuit 428 empty. Since the register still contains a high signal at its first stage upon the occurrence of the next consecutive 3.75 hz clock pulse (i.e., the fourth 3.75 clock pulse after the point at which the rabbit passes the dog), said pulse is provided by the Inside Dog Position Advance Circuit to the clock input of the Inside Dog Position Counter to advance the counter a third position. The Inside Dog Position Decoder and Illumination Circuit 440 thereby effectuates the illumination of lamp 104 (all the while lamp 202 of the outside dog remains lit).

Upon the passage of the third clock pulse to the clock input of the Inside Dog Position Counter the fourth, third and second stages of the register within the Inside Dog Position Advance Circuit empty, thereby leaving only a high signal on the first stage. Accordingly, upon the next successive 3.75 hz clock pulse from the clock pulse generator 424, i.e., the fifth consecutive clock pulse after the point at which the rabbit passes the dog, the Inside Dog Position Advance Circuit provides said clock pulse to the clock input of the Inside Dog Position Counter 420. This action advances the counter a fourth position. The Dog Position Decoder and Illumination Circuit decodes the counter 420 and illuminates lamp 105 in response thereto.

Upon the fourth clock pulse being applied to the Inside Dog Position Counter, the register within the Inside Dog Position Circuit 428 is completely empty; i.e., contains only lows. At this point in time the Inside Dog Position Advance Circuit, like the Outside Dog Position Advance Circuit, no longer provides clock pulses to its associated counter until the rabbit recircles the track and is again coincident with the dog, whereupon the above described sequence of operation can occur again.

When the Inside Dog Position Counter 420 reaches the end of its count cycle, the Lap Decoder and Illumination Circuit monitors such a condition and provides a signal indicating that the inside dog has completed one lap, i.e., lamp 304 is lit. The Lap Decoder and Illumination Circuit 444 provides a signal to light lamp 305 and indicate that a second lap has been completed when the Inside Dog Position Counter completes a second count sequence and provides a signal to illuminate lamp 306 when the Inside Dog Position Counter has completed a third count sequence.

Operation of the Lap Decoder and Illumination Circuit 446 is identical to that of Lap Decoder and Illumination Circuit 444.

When either Lap Decoder and Illumination Circuit indicate that three laps have been completed, the Winner Decoder and Illumination Circuit 448, illuminates either lamp 307 (if the outside dog wins), lamp 308 (if the inside dog wins), or lamp 309 (if it is a dead heat). Upon either a win or a dead heat, the Winner Decoder and Illumination Circuit provides a signal to the Infield and Play Again Decoder and Illumination Circuit 448. This action results in lamp 311 therein illuminating, to light up the infield on the face of the board 402. The infield remains lit for a predetermined period of time which period is established by the Game Control Circuit 416. After that period of time the Game Control Circuit provides a signal to the Infield and Play Again Decoder and Illumination Circuit to cause lamp 311 therein to go out and to cause lamp 310 to illuminate. This action results in the illumination of the "Play Again" legend.

The radio transmitter 406 provides a multiplexed signal to the receiver 418. That signal is produced by modulating a radio frequency carrier signal by two audio signals, depending upon whether or not an associated transmitter button is depressed. In FIG. 4 there is shown a block diagram of the radio transmitter.

As can be seen therein the transmitter includes a pair of audio oscillators, 452 and 454. Audio oscillator 452 is adapted for providing oscillations at a frequency of 5 KHZ and oscillator 454 is adapted for providing oscillations at a frequency of 7.5 KHZ.

The oscillators are provided during alternate intervals as will be described in detail hereinafter such that during one interval of time only oscillator 452 is providing oscillations and during the next succeeding interval oscillator 454 is providing oscillations. Either oscillator 452 or 454 can be disabled from providing oscillations in accordance with the condition of the transmitter button associated therewith.

The sequencing of oscillator operation is determined by a Timing Generator Circuit 456 and a Timing Sequencer Circuit 458.

The output of oscillator 452 is provided as one input to NOR gate 460 and the output of the other oscillator 454 is provided as another input to the NOR gate. The output of the NOR gate is provided as one input to a Radio Frequency Amplifier 464. A crystal controlled Radio Frequency Oscillator 462 is adapted for providing a main carrier signal to the Radio Frequency Amplifier 464. The radio frequency amplifier modulates the carrier signal and amplifies same in accordance with signals received from NOR gate 460 and provides the modulated and amplified signal to a tuned antenna 466. The antenna provides the modulated radio signals through the air to an antenna coupled to receiver.

FIG. 5 shows the details of the circuitry forming the transmitter 406. As can be seen therein a Battery VI is provided in the transmitter and is coupled to one side of a pair of dual-contact, ganged switches SW1 and SW2. Switch SW1 is connected to the transmitter button 410 and both of its pairs of contacts are closed when the transmitter button is depressed. Switch SW2 is connected to transmitter button 412 and both of its pairs of contacts are closed when switch SW2 is depressed.

Switch SW1 is adapted when closed for providing power to Timing Generator Circuit 456, the Timing Sequencer 458, the Audio Oscillator 452, the Crystal Oscillator 462 and the Radio Frequency Amplifier 464. Switch SW2 is adapted, when closed, for providing power to the Timing Generator Circuit 456 the Timing Sequencer 458, the Audio Oscillator 454, the Crystal Oscillator 462, and the Radio Frequency Amplifier 464.

The Timing Generator Circuit 456 includes a unijunction transistor, UJT, having a resistor R1 connected between contacts of switch 1 and the emitter of the unijunction transistor. The emitter of the unijunction transistor, is connected via a diode D1, and the parallel combination of a capacitor C1 and a resistor R2 and a series connected potentiometer R3, to ground. A resistor R4 is connected between the base of the unijunction transistor and one side of switches SW1 and SW2.

A transistor Q1 is coupled to the unijunction transistor. To that end a resistor R6 is coupled between the base 1 of the unijunction transistor and the base of transistor Q1. The emitter of transistor Q1 is connected to ground. The collector of transistor Q1 is connected, via a resistor R7, to the common connection of resistors R1 and R4.

As will be appreciated by those skilled in the art the voltage on the emitter of the unijunction transistor increases as the current through the path comprising resistor R1, diode D1, resistors R2 and R3 charges capacitor C1, the time constant of the charging path being the parallel resistance of R1 and R3 times the capacitance of C1. During the time that the unijunction transistor is off, the base of transistor Q1 is at ground potential and Q1 is off. Accordingly, the output on the collector of Q1 is high (some positive value).

When the unijunction transistor emitter reaches its peak-point voltage, the unijunction transistor conducts and capacitor C1 discharges through the resistors R2 and R3. During the discharge cycle of the unijunction the base of transistor Q1 is biased positive, whereupon transistor Q1 becomes conductive thereby lowering the collector voltage to ground potential. All during the time that the unijunction transistor is conducting the collector voltage of Q1 is at ground potential. When the unijunction transistor turns off and begins recharging again transistor Q1 turns off and the potential on its collector again begins to rise to said positive value.

The discharge time constant for the circuit 604 is established such that it is approximately of the same duration as the charging time constant. As should therefore be appreciated during the interval of time that the unijunction transistor is nonconductive, i.e., when it is charging, the output of the circuit 456 is a predetermined positive voltage and during the next successive interval, i.e., the interval during which the unijunction transistor is conducting the output of circuit 456 is at ground potential. The unijunction transistor is free running, such that during successive intervals of time positive voltage and ground potential alternately appear at the output of circuit 456.

The Timing Sequencer Circuit 458 includes a pair of Transistors Q2 and Q3 whose bases are coupled via resistors R8 and R9, respectively, to the collector of transistor Q1 of circuit 456. The collector of transistor Q2 is connected, via resistor R10, to one side of switch SW1 and to one side of switch SW2. The emitter of transistor Q2 is connected to ground.

In a similar manner, the emitter of transistor Q3 is connected to ground. The collector of transistor is connected, via resistors R13 and R17, to one side of switch SW2. A capacitor C2 is connected across the emitter-to-base junction of transistor Q2. A resistor R11 is connected from the collector of transistor Q2 to the base of a transistor Q4. The emitter of transistor Q4 is connected to ground and the collector thereof is connected to the base of a transistor Q5 in the Audio Oscillator 452. In a similar manner, the collector of transistor Q3 is connected to the base of a transistor Q6 in the Audio Oscillator 454.

Operation of the Timing Sequencer Circuit 458 is as follows, assuming that both switches SW1 and SW2 are closed. During the interval that the output of Timing Generator 456 is at ground potential both transistors Q2 and Q3 are biased off whereupon the base of transistor Q6 in Oscillator Circuit 454 is at some positive potential. When transistor Q2 is off, transistor Q4 is conductive. Accordingly, the base of transistor Q5 in Oscillator Circuit 452 is effectively at ground potential. During immediately succeeding interval in time (i.e., when the output of circuit 456 is at some positive potential) both transistor Q2 and Q3 are rendered conductive. Upon transistor Q3 conducting, the base of transistor Q6 is effectively at ground potential. Upon transistor Q2 conducting transistor Q4 is rendered non-conductive, whereupon some positive voltage appears at the base of transistor Q5, via resistor R12.

Each of the audio oscillators is of the "Hartley" type. For example, Oscillator 452 comprises a transistor Q5 and a resistor R12 connected between its collector and its base. A capacitor C5 is connected between the base of transistor Q5 and one end of an inductor L1. The other end of inductor L1 is connected to ground. A capacitor C3 is connected across inductor L1. Inductor L1 includes a center tap which is connected to the emitter of transistor Q5.

In a similar manner Oscillator 454 includes a transistor Q6 whose collector is connected to its base via resistor R13. A capacitor C6 is connected between the base of transistor Q6 and one end of an inductor L2. The other end of the inductor L2 is connected to ground. A capacitor C4 is connected across inductor L2. A center tap of inductor L2 is connected to the emitter of transistor Q6.

As can be seen, a variable potentiometer R16 is connected between the collector of transistor Q5 and one contact of switch SW1 and a variable potentiometer R17 is connected between the collector of transistor Q6 and one contact of switch SW2.

Oscillator 452 is adapted for providing 5 khz oscillations when enabled by the closure of switch SW1 and during the interval in time that the output of the Timing Generator Circuit 456 is at some positive potential. Oscillator 454 is adapted for providing 7.5 khz oscillations when enabled by the closure of switch SW2, during the next succeeding interval in time that output of the Timing Generator Circuit 456 is at ground potential.

The operation of either oscillator, when enabled and during their associated interval, proceeds in a similar manner. To that end only the operation of oscillator 454 will be described.

When the base of transistor Q6 in oscillator 454 is at some positive potential, transistor Q6 turns on, whereupon current flows therethrough and through a portion of the inductor L2 from the center tap to ground. The

current flowing through that portion of the inductor induces a flux in the core which results in an emf in the remaining portion of the coil. The emf is fed back to the base of transistor Q6 so that oscillations result therefrom. The oscillations are amplified by transistor Q6 and are provided at its emitter. The emitter of transistor Q6 serves as one input to Norgate 460. The emitter of transistor Q5 in oscillator 452 provides another input into the norgate.

As previously discussed, only one oscillator is enabled to oscillate during a conduction interval as defined by the Timing Generator Circuit and the Timing Sequencer, irrespective of whether or not both switches are closed. For example when switch SW1 is closed oscillator 452 operates during alternate intervals. During intermediate intervals oscillator 454 operates if switch 2 is also closed. If switch 2 is open no oscillations are produced during said intermediate interval. If switch 2 is closed and switch 1 is open, during the intermediate intervals, oscillator 454 provides oscillations during the alternate intervals.

The output of oscillator 452 is provided as one input to NOR gate 460 and the output of oscillator 454 is provided as another input of the Norgate. To that end the emitter of transistor Q5 is connected, via a resistor R14, to the base of transistor Q7 in the Norgate and the emitter of transistor Q6 is connected, via a resistor R15, to the base of transistor Q8 therein. The emitters of transistors Q7 and Q8 are connected together and to ground and the collectors thereof are connected together to form the output of the NOR gate.

Operation of the NOR gate is as follows, assuming that during one interval oscillations are provided to the base of transistor Q7 via oscillator 452. During the negative going half cycles of the oscillations, transistor Q7 is off and some positive voltage appears at the collector of transistor Q7. During the positive going half cycles of the oscillations, the transistor Q7 is on and its emitter is at ground potential. Accordingly, the oscillations from Oscillator Circuit 452 are converted in NOR gate 608 to a group of positive pulses at the frequency of the oscillations. In a similar manner, the NOR gate converts the oscillations from oscillator 454 into a group of pulses whose frequency is the frequency of the oscillations from circuit 454. Therefore, in the embodiment shown, during one interval pulses at a frequency of 7.5 khz appear at the output of the NOR gate and during the next successive interval pulses at a frequency of 6 khz appear at the output thereof (assuming of course that both switches SW1 and SW2 are closed).

The Crystal Oscillator 462 is of the "Pierce" type and comprises a transistor Q9 having a crystal, connected between its collector and its base. A resistor R18 is connected between the base of the transistor and one contact of switch SW1 and one contact of switch SW2. The emitter of transistor Q9 is connected to ground via a resistor R20. A resistor R19 is connected between the base of transistor Q9 and ground. A capacitor C8 is connected between ground and one side of switch SW2. A pair of capacitors C14 and C15 are connected between ground and respective contacts of switches SW1 and SW2.

The crystal oscillator 462 operates in a conventional manner and provides oscillations of a frequency approximately 27 megahertz via inductor L3 to the base of transistor Q10. The 27 megahertz oscillations act as the main carrier signal for the transmitter and receiver.

The Radio Frequency Amplifier 464 is operative for modulating the carrier signal with the signals received from the NOR gate 460 i.e., either the 7.5 khz pulses or the 5khz pulses, depending upon the conduction internal of Timing Generator Circuit 456. The Radio Frequency Amplifier 460 amplifies the modulated signal and provides the amplified signal to a tuned antenna 466 for transmission to the receiver.

The Radio Frequency Amplifier comprises a transistor Q10 whose emitter is connected to one side of another winding of inductor L3 and a resistor R21 is connected between the other side of that winding and the base of transistor Q10. A capacitor C11 is connected in parallel with resistor R21. The output of the NOR gate 460 (i.e., the collectors of transistors Q7 and Q8) is connected to the junction of resistor R21 and the other winding of L3. The collector of transistor Q10 is connected to the center tap of winding L4. A capacitor C12 and a tuning capacitor C13 are connected in parallel with each other and across L4 to form the tuned antenna 466.

Operation of the Radio Frequency Amplifier is as follows assuming that during a particular interval, oscillator 452 is operating whereupon pulses of a frequency of 5 khz are provided by the NOR gate 608 to a winding of L3. As will be appreciated by those skilled in the art, during the time between each 5 khz pulse the emitter of transistor Q10 will effectively be at ground potential and the 27 megahertz carrier signal will be amplified by transistor Q10 and be applied to the tuned antenna.

The antenna radiates the 27 megahertz carrier signal in a burst of 5 khz pulses during alternate intervals and the 27 megahertz carrier in bursts of 7.5 khz pulses during the intermediate intervals, assuming that both oscillators 452 and 454 are operating. If only switch SW1 is closed, oscillator 452 operates, thus the input to the receiver is the 27 megahertz carrier provided in a burst of 5 khz pulses during alternate intervals and no signal during the intermediate intervals. If, on the other hand, only switch SW2 is closed, oscillator 454 operates, thus the antenna radiates the 27 megahertz carrier in bursts of 7.5 khz pulses during the intermediate intervals and no signal during the alternate intervals.

FIG. 6 is a block diagram of the Receiver 418. As can be seen therein the receiver is of the superhetrodyne type in that the carrier signal is mixed with a local oscillation signal to provide an intermediate frequency (IF) signal. The IF signal is demodulated or detected to remove the carrier and to provide at its output the 5 khz pulses, if any, during the intermediate intervals. To that end the receiver includes an antenna 468 which provides the modulated 27 megahertz, carrier signal with the oscillation from a local oscillator 472. The local oscillator is tuned such that its output is 455 ± 15 lower than the 27 megahertz carrier. This results in 455 ± 15 khz oscillations appearing in either 5 khz pulses or 7.5 khz pulses, (depending upon the interval and the state of the switches SW1 and SW2 in the transmitter). The IF signal is provided to IF amplifier 472 which amplifies the input and feeds the amplified output to a detector circuit 475.

In the detector circuit the 455 ± 15 khz IF signal is rectified and filtered to remove the carrier and the remaining signal (i.e., the 5 or 7.5 khz pulses) is provided as an input into two detection channels, 476 and 478. Channel 476 is a channel for separating the 5 khz pulses from the carrier and for providing an output sig-

nal indicative of the presence of such pulses. Channel 478 is provided for separating the 7.5 khz pulses from the carrier and for providing an output signal indicative of the present of such pulses. To that end channel 476 comprises an Audio Frequency Amplifier 480, a 5 khz Band Pass Filter 482 a Detector 484, a Schmitt Trigger 486, and an Integrating Circuit 488. Channel 478 comprises an Audio Frequency Amplifier 492, a 7.5 khz Band Pass Filter 494 a Detector 496, a Schmitt Trigger 498 and an Integrating Circuit 500.

Operation of channel 476 is as follows. The Audio Frequency Amplifier 480 provides amplified oscillations at the frequency of the input signals provided thereto. The oscillations are provided to the 5 khz Band Pass Filter which filters out all signals other than the 5 khz oscillations (i.e., it filters out any 7.5 khz oscillations which may exist during the intermediate intervals). The 5 khz output of the Band Pass Filter is provided to Detector 484 which rectifies the oscillations and filters out the rectified signal to provide a positive signal during each interval in which the 5 khz oscillations appear. The output signal from the detector is shaped in Schmitt Trigger 486. The output of the Schmitt Trigger is fed into an Integrator 488 which provides a ground or logically low signal so long as the Schmitt Trigger provides it with positive output signals. As should thus be appreciated the output of the Integrator will be logically low whenever the transmitter button 410 is depressed and will be at a logical high whenever the transmitter button is released.

Channel 478 operates in a similar manner to channel 476 to provide a logically low signal whenever transmitter button 412 is depressed and a logically high signal when the transmitter button is released.

The details of a portion of the receiver are shown in FIG. 7. As can be seen therein the output of the IF amplifier 474 is provided to the Detector 475 via a winding of transformer L5 and is coupled via diode D2 across capacitor C16. One side of C16 is connected to ground. Capacitor C16 forms a side of a Pi arranged filter which includes another capacitor C17, one side of which is connected to ground and a resistor R22 connected between the non-grounded sides of both capacitors. A load resistor R23 is provided across capacitor C17 and forms the output of the detector. The output of the detector is coupled via a capacitor C18 to the input of the audio frequency amplifier 480 in channel 476 and via capacitor C19 to the audio frequency amplifier 492 in channel 478.

Audio frequency amplifier 480 comprises a transistor Q11 whose base serves as the input to the amplifier. A diode D3 is connected between ground and the base of Q11. A resistor R24 is connected between the collector and Q11 and the base thereof.

The 5 khz Band Pass Filter 482 is connected via a capacitor C20 and a resistor R25 to the collector of transistor Q11 and is also connected to a source of positive bias voltage such as 10 volts. The Band Pass Filter is formed of capacitor C22 and inductor L6, the values of which are selected so as to enable the passage 5 khz signals therethrough but to prevent 7.5 khz signals from passing therethrough.

Audio Amplifier 492 comprises a transistor Q12 whose base serves as the input to the amplifier. A diode D4 is connected between ground and the base of transistor Q12. A resistor R26 is connected between the collector of Q12 and the base thereof.

A 7.5 khz Band Pass Filter 494 is connected, via a capacitor C21 and a resistor R27, to the collector of transistor Q12 and is also connected to said positive bias voltage. The band pass Filter is formed of a capacitor C23 and L7, the values of which are selected so as to enable the passage of 7.5 khz signals therethrough but to preclude 5 khz signals from passing therethrough.

As will be appreciated by those skilled in the art, upon the appearance the 5khz signals and the 7.5 khz signals at the base of transistors Q11 and Q12 of amplifiers 480 and 492, respectively, oscillations at a frequency of 5 khz will appear at a frequency of 7.5 khz will appear at the output of Band Pass Filter 494, thereby effecting the separation of the input signals into channels 476 and 478.

The output signal from the band Pass Filter 482 is provided into detector 484 wherein it is rectified, filtered and amplified. To that end Detector 534 comprises a diode D5 which is connected to one side of inductor L6. A filter capacitor C24 is connected to the anode of diode D5 and to the other side of inductor L6 which in turn is connected to the positive bias voltage. A load resistor R28 is connected across capacitor C24. The base of transistor Q13 is connected to said one side L6 and the emitter is connected, via a resistor R29, to the positive bias voltage. The collector of transistor Q13 is connected via resistor R32 to ground and is also connected to the base of transistor Q15. The emitter of transistor Q15 is connected to ground and the collector thereof is connected via resistor R34 to a positive bias voltage VCC and serves as an input to the Schmitt Trigger Circuit 486.

In a similar manner the output signal from Band Pass Filter 494 is provided into Detector Circuit 496 where it is rectified, filtered and amplified. To that end Detector 496 comprises a diode D6 which is connected to one side of inductor L7. A filter capacitor C25 is connected to the anode of diode D6 and to the other side of inductor L7 which in turn is connected to the positive bias voltage. A load resistor R30 is connected across the capacitor C25. The base of a transistor Q14 is connected to one side of inductor L7 and the emitter is connected via resistors R31 to the positive bias voltage. The collector of transistor Q14 is connected via resistor R33 to ground and is also connected to the base of transistor Q16. The emitter of transistor Q16 is connected to ground and the collector thereof is connected via resistor R35 to the positive bias voltage VCC and serves as the input to schmitt Trigger Circuit 498.

Operation of the Detector 496 is similar to that of Detector 484 and only the operation of detector circuit 484 will be described. To that end, upon the appearance of 5 khz oscillations at diode D5, such oscillations are rectified thereby and the rectified oscillations are filtered by capacitor C24. The resulting signal is applied to load resistor R28, and thus at the base of transistor Q13. Transistor Q13 acts an emitter follower and upon conducting causes transistor Q15 to begin conducting. When transistor Q15 conducts, the collector thereof is at ground potential.

As should be appreciated during the intervals between the filtered rectified signals, the base of transistor Q13 is at ground potential whereupon transistor Q13 turns off and a positive voltage appears at its collector and as the input to the Schmitt Trigger Circuit 486. The Schmitt Trigger shapes the positive signals ap-

plied to its input and passes the shaped signals to the Integrator 488.

In a similar manner, Schmitt Trigger 498 shapes the output of Detector 496 and passes said shaped signals to the Integrator 500.

Each of the integrators integrate the input signal provided thereto to provide constant grounded (i.e. logically low) output signal so long as their input consists of positive signals. To that end each integrator includes a retriggerable monostable multi-vibrator whose $\bar{Q}$ output is set at a logically low state in response to the first positive signal provided at the monostable multi-vibrator's input by the associated Schmitt Trigger Circuit and which retriggers itself to said low state if a positive signal is in existence at the time it attempts to reset itself (i.e. it maintains its logically low state so long as positive signal appears at its input at a time when it would attempt to reset itself.)

The output of Integrator 488 is provided at line 491 and the output of Integrator 500 is provided at line 501.

In FIG. 8 the details of the Rabbit Position Counter 432 and Rabbit Position Decoder and Illumination Circuit 434 are shown.

As can be seen circuit 432 includes a four-stage counter 502 having four outputs QA, QB, QC, and QD. The clock input to the counter is provided by line 504 from the 3.75 hz output line of the clock pulse generator 424. The Q5 output of counter 502 is provided by line 506. The QB output of the counter is provided by line 510 and the QD output is provided by line 512.

The Rabbit Position Decoder and Illumination Circuit 434 includes a pair of decoders 514 and 516. Each of the decoders is operative for decoding a four line binary code into a sixteen position output. As can be seen the A input to both decoders is connected to line 504. The B input to both decoders is provided from the QA output of the rabbit counter via line 506. In a similar manner the QB output is provided to the C inputs of the decoders via line 508 and the QC output of the counter is provided to the D input of decoders via line 510.

Each of the decoders includes 16 output terminals *a, b, c, d, e, f, g, h, i, j, k, l, m, n, o* and *p*. The decoders also include an enable terminal E, which when a low signal is provided thereto enables the decoder to decode the input signals appearing at its input terminals. As can be seen, the enable terminal E of decoder 514 is connected via an inverter 518 to the QD output terminal of counter 502 that the enable terminal E of decoder 516 is provided from the QD output of the counter directly by line 512. Decoder 434 includes transistors Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31 and Q32. The bases of transistors Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15 and Q16 are connected to the decoder output terminals *a, b, c, d, e, f, g, h, i, j, k, l, m, n, o* and *p*, respectively and the bases of transistors Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31 and Q32 are connected to the decoder output terminals *a, b, c, d, e, f, g, h, i, j, k, l, m, n, o* and *p*, respectively. The emitters of transistors Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13 and Q16 are connected together to a source of positive voltage such as 9 volts. The collectors transistors Q1-Q15, inclusive, are connected to one side of lamps 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16, the other side of the lamps are con-

nected together to ground. In a similar manner, the collectors of transistors Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31 and Q32 are connected together to the nine volt source of bias voltage and the collectors of the transistors are connected to one side of lamps 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, and 32. The other side of the lamps are connected together and to ground.

Operation of the Rabbit Counter 502 and the Rabbit Decoder and Illumination Circuit is 434 as follows.

When the counter 502 is in its initially cleared state, the QD output thereof which is provided by line 512 is low thereby enabling the decoder 516 while disabling the decoder 514 via the high signal provided by inverter 518.

Each of the decoder output terminals provide inverted output signals and thus are high when the decoder is disabled. When enabled, the provides provides signals at its the output terminals in accordance with logic levels of the four input signals provided to its input terminals A, B, C and D.

During the interval in time before the first 3.75 hz clock pulse from the Clock Pulse Generator 424, the inputs to the enabled decoder 516 are low since the QB, QC and QD terminals of the counter 502 are low. With lows on the input terminals, the output terminal A of decoder 516 is low whereby transistor Q1 conducts to enable the illumination of lamp 1.

At the occurrence of first 3.75 hz clock pulse the A input to decoder 516 is high whereas the outputs QA, Qb and QC of counter remain low (since the counter can only be clocked by the trailing edge of an incoming signal). Accordingly, the B, C and D terminals of the decoder are low. This condition results in the B terminal of decoder 516 being low whereby transistor Q2 conducts to enable the illumination of lamp 2. At the trailing edge of the 3.75 hz clock pulse, counter 502 is clocked whereby its QA output goes high. At this point in time input A of the decoder 516 is low, input B is high and inputs C and D are low. This condition results in output C of decoder 516 being low whereby transistor Q3 conducts to enable the illumination of lamp 3.

Operation of the counter 502 and the decoder 516 continues in a similar manner for a total of sixteen counts i.e., until the trailing edge of the 8th 3.75 hz clock pulse. On the sixteenth count the P output terminal of decoder 516 is low whereby transistor Q16 conducts to enable the illumination of lamp 16.

At the end of the sixteenth count the QD output of counter 502 goes high whereupon the high signal applied to the E input terminal of decoder 516 disables that decoder. The high signals appearing on line 512 is inverted by inverter 518 and provided as an input to the enable terminal, E, of decoder 514 to enable the decoder to encode the signals appearing on its input lines 504, 506, 508 and 510. Operation of the Counter 502 and the Decoder 514 continues from the seventeenth count through the thirty second count in a manner similar to the operation of the counter 502 and the decoder 516 in counting the first through the sixteenth.

As should thus be appreciated, the rabbit traverses thirty two positions via the sequential illumination of 32 lamps during the period in time that the clockpulse generator provides sixteen 3.75 hz clock pulses.

In FIG. 9. there is shown the details of the Inside Dog Position Counter 420 and the Dog Position Decoder and Illumination Circuit 440.

The Outside Dog Position Counter 422 is identical to the Inside Dog Position Counter and is connected and arranged in a similar manner. Accordingly, the details of circuit 422 will not be considered herein. Similarly, the Dog Position Decoder and Illumination Circuit 422 is identical to the Dog Position Decoder and Illumination Circuit 440 and is connected and arranged in a similar manner thereto. Accordingly, circuit 442 will not as considered in detail herein.

Counter 420 is a four-stage counter having four output terminals QA, QB, QC and QD. The counter includes a clock input terminal clk which is provided from line 520 and a clear input terminal which is provided from line 522. The QA, QB, QC and QD terminals of counter 420 are provided at lines 524, 526, 528 and 530, respectively.

The Dog Position Decoder and Illumination Circuit 440 includes a decoder 532 which is similar to decoders 514 and 516 in circuit 434. As can be seen decoder 524 includes input terminals A, B, C, D. An enable terminal E is connected to ground so as to enable the decoder to operate at all times to provide a decoder output at terminals a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, and p.

Circuit 440 includes transistors Q101, Q102, Q103, Q104, Q105, Q106, Q107, Q108, Q109, Q110, Q111, Q112, Q113, Q114, Q115, and Q116. The base of transistors Q101, Q102, Q103, Q104, Q105, Q106, Q107, Q108, Q109, Q110, Q111, Q112, Q113, Q114, Q115 and Q116 are connected to decoder to output terminals a, b, c, d, e, f, g, h, i, j, k, l, m, n, o and p, respectively. The emitters of the transistors are connected together to a positive bias voltage of nine volts. The Collectors of transistors Q101, Q102, Q103, Q104, Q105, Q106, Q107, Q108, Q109, Q110, Q111, Q112, Q113, Q114, Q115, and Q116 are connected to one side of lamps 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, and 116 and the other side of the lamps are connected together to ground.

Operation of circuit 420 and circuit 440 is as follows: At the beginning of the game, the Control Circuit 416 provides a reset signal, which is a logically high signal, to the clear input terminal of counter 420. This causes the QA, QB, QC and QD outputs thereof to go low. During the game the Inside Dog Position Advance Circuit 428 provides either one, two, three or four clock signals along line 522 to the clock input of counter 420 depending upon the point at which the transmitter button 410 is released as the rabbit passes the inside dog.

Prior to the first clock signal being provided to the counter, all of its inputs are low and thus all of the decoder inputs are low. This results in a low signal appearing at the output terminal of the decoder, whereupon transistor Q101 turns on and lamp 101 illuminates. At the trailing edge of the first signal at the clock input of signal the counter 420, the QA output thereof goes high while the QB, QC, and QD outputs stay low, whereupon the Decoder 532 decodes those signals and provides a low signal at its output terminal B. This action results in transistor Q102 turning on and lamp 102 lighting, whereupon the inside dog advances one position around the track.

Operation of the counter and decoder continue in a similar manner to illuminate the lamps in sequential or-

der, one at a time as the counter counts clock signals applied thereto. This action establishes the animated display of the inside dog running around the track.

After being clocked sixteen times, the counter 420 is reset back in its original starting position and the dog returns to the starting position on the track and has completed one lap.

The game control circuit 416 is shown in logic diagram of FIG. 10. As can be seen therein, Circuit 416 includes a pair of flip-flops 532 and 534. The flip-flop 532 includes a D input provided by the output of an AND gate 536. One input to AND gate 536 is provided by line 538 and the other input thereto is provided by line 540. Line 540 is connected to the Q output of flip-flop 534. The $\bar{Q}$ output of flip-flop 532 is provided via line 542 to one input of AND gate 544. The other input and AND gate 544 is provided by line 546 which is connected to the $\bar{Q}$ output of flip-flop 534. The output of AND gate 544 is provided by line 522. The Flip-flop 534 includes a D input which is connected to the output of AND gate 548. One input to AND gate 548 is provided by line 542 and the other input thereto is provided by line 550. Line 550 serves as the output of OR gate 552. One input of OR gate 552 is provided by line 540 and another input thereto is provided by line 554. Line 554 is the output of AND gate 556. Gate 556 includes a pair of input terminals 558 and 560. Line 558 is provided at the output of gate 562. The inputs to gate 562 are provided by lines 491 and 501. The clock inputs to both flip-flops are provided by inverter 564 from line 512. The clear inputs to both flip-flops are connected to line 566. The preset inputs P of the flip-flops 532 and 534 are connected to a positive voltage.

Operation of the control circuit 416 is as follows. Upon the energization of power supply 414, a temporary low signal is provided at line 566 which effectuates the clearing of flip-flops 532 and 534 such that their $\bar{Q}$ outputs go high and the control circuit is in its "Idle" condition. As a result of both flip-flops being cleared, the gate 544 provides a high signal at line 522. This signal effectively resets both of the dogs' counters and holds those counters in the reset state so long as the high signal persists on line 522.

Line 560 is connected to the coin box 404 and is at a logically low level before a coin is inserted therein. Accordingly, before a coin is inserted AND gate 556 is disabled and a low signal appears on line 554 and one input to OR gate 552. The other input of OR gate 552 is provided by the Q output of flip-flop 534 and is also low since the flip-flop 534 is cleared. The output of OR gate 552 is thus low and disables the AND gate 546 whereupon a low signal is provided at the D input of flip-flop 534. At the same time the low signal appearing on the Q output of flip-flop 534 is provided via line 540 to AND gate 536. This signal disables the AND gate 536 whereupon a low signal is applied to the D input of flip-flop 532.

When a coin is inserted into the Coin Box 103 a high signal appears on line 560. The high signal is provided as one input to AND gate 556. If neither transmitter button is depressed at this time, the signals appearing on lines 491 and 501 are high, whereupon the output of gate 562 is low. The output of gate 562 is provided, via line 558 to the other input of AND gate 556. Accordingly, the output of gate 556 is low the control circuit remains in its "Idle" condition.

When either transmitter button is depressed the low signal appearing at the output of its associated integrator causes the output line 558 to go high. For example, if transmitter button 410 is depressed line 491 goes low such that output line 558 goes high. In a similar manner if transmitter button 412 is depressed the low signal appearing on line 501 causes the output line 558 of gate 562 to go high.

Upon the coincidence of high signals on line 558 and 560, the output of gate 556 goes high, whereupon input line 554 of OR gate 552 goes high. The high signal appearing on line 554 results in OR gate 552 providing a high signal, via line 550, to AND gate 548. Since the flip-flop 532 is in its cleared state the $\bar{Q}$ output thereof as provided by line 542 is also high. Accordingly, the output of gate 548 is high and is provided to the D input to flip-flop 534. At the same time the Q output of flip-flop 534 is low and the low signal provided via line 540 to one input of AND gate 536. Accordingly, AND gate 536 is disabled and a low signal is applied at the D input to flip-flop 532.

Upon the rabbit completing one lap of the track (such that the QD output of the counter is low) the low signal appearing on line 512 is inverted by inverter 564 to provide a high signal to the clock inputs of flip-flop 532 and 534. The action causes flip-flop 534 to set whereas flip-flop 532 remains in its cleared state due to the low signal on its D input.

Upon the setting of flip-flop 534 its $\bar{Q}$ output goes low, thereby disabling gate 544 such that a low signal appears on line 522. The low signal appearing on line 522 enables both of the dog counters to advance when clocked. The game control circuit is now in its "Play" condition.

The high signal appearing on the Q output of flip-flop 534 is provided as one input via line 540 to OR gate 552. The output of OR gate 552 is provided along line 550 and is therefore high. Accordingly, a high signal appears at one input to AND gate 548. The other input to AND gate 548 is provided by the $\bar{Q}$ output of the cleared flip-flop 532 via line 542. Accordingly, the D input on flip-flop 534 is maintained high.

The high signal appearing on line 540 from the Q output of the set flip-flop 534 is provided as one input to AND gate 536. The other input to AND gate 536 is provided by line 538 and is low so long as a game is in progress. Accordingly, the output of gate 536 is low and prevents flip-flop 532 from changing states until the game ends.

Assuming that one or both dogs complete three laps of the track such that the game has ended, a high signal is provided on line 538. Since line 540 is high, via the high Q output of flip-flop 534, the high signal appearing on line 538 when the game ends enables a high signal to be provided on the D input to flip-flop 532.

At the same time the high signal appearing on the $\bar{Q}$ output of flip-flop 532 is provided, via line 542 as one input to AND gate 548. The other input to AND gate 548 is provided by OR gate 552. Since flip-flop 534 is set at this time, its Q output is high which output is provided via line 540, into OR gate 552. Therefore, the output of OR gate 552 is high and is provided via line 550 to the other input of AND gate 548. The coincidence of high signals appearing on lines 542 and 550 results in AND gate 548 providing a high signal to the D input of flip-flop 534. When the rabbit next advances around the board such that the QD output of its

counter is low, the low signal applied via line 512 is inverted by inverter 564 and provided to clock flip-flops 532 and 534, whereupon flip-flop 532 sets and flip-flop 534 remains set. When flip-flop 532 sets, its $\bar{Q}$ output goes low, thereby disabling gate 548 which provides a low signal to the D input of flip-flop 534.

When flip-flop 532 and 534 are both set the game control circuit is in its "Game End" condition.

At the same time that the AND gate 548 provides a low signal to the D input of flip-flop 534, the AND gate 536 provides a high signal into the D input of flip-flop 532, via the high input signals provided to its input lines 540 and 538. Accordingly, the next time that the rabbit counter reaches the position where its QD output is low, the low signal appearing on line 512, as inverted by inverter 564, clocks flip-flops 532 and 534. This action results in the resetting of flip-flop 534 while flip-flop 532 remains in its set condition. When flip-flop 534 is in its reset condition and flip-flop 532 is in its set condition the game control circuit is in its "cycle condition."

When flip-flop 534 resets, the low signal appearing on its Q output is provided as one input to AND gate 536, whereby the gate provides a low signal to the D input of flip-flop 532. At the same time the low signal appearing on the $\bar{Q}$ output of flip-flop 532 is provided via line 542 to AND gate 548. This action results in AND gate 548 providing a low signal to the D input of flip-flop 534. The next time that the rabbit counter reaches the position where its QD output is low, the low signal appearing on line 512 is inverted by inverter 564 and provided to the clock inputs of flip-flops 532 and 534. This action results in resetting flip-flop 532 while flip-flop 534 remains reset. When this action occurs the infield lamp goes out and the lamp behind legend "Play Again" illuminates. The game control is now in its "Idle" condition and awaiting the insertion of a coin and the depression of the transmitter buttons to start a new game.

FIG. 11 is a logic diagram of the details of the Scoring Pulse Forming Circuit 426. As can be seen therein line 504 provides 3.75 hz clock pulses from the clock pulse generator circuit 424 to inverter 568. Line 570 provides 7.5 hz clock pulses from the clock pulse generator to inverter 572 and line 574 provides 15 hz clock pulses from the clock pulse generator to inverter 576. The outputs of inverters 568, 572 and 576 are connected together at line 578. Line 580 provides 30 hz clock pulses from the clock pulse generator to one input of AND gate 582. The other input of AND gate 582 is provided by line 578. The output of AND gate 582 is denoted as 584.

As will be appreciated by those skilled in the art, with the inputs arranged as shown in FIG. 11, a 30 hz positive going pulse will appear once every eighth 30 hz clock pulse appearing on line 580, starting with the first 30 hz clock pulse applied thereto. The output pulses appearing on line 584 are hereinafter referred to as scoring pulses.

The Coincidence Detector 436 is shown in the logic diagram of FIG. 12. The Coincident Detector 438 is constructed in an identical manner to Coincident Detector 436 and is connected to the Rabbit Position Counter in the same manner that the Rabbit Position Counter and is also connected to the outside Dog position Counter 422 in the same manner that the Coincident Detector 436 is connected to the Inside Dog Po-

sition Counter 420. Accordingly, Coincidence Detector 438 will not be described in detail.

As can be seen Coincidence Detector 426 includes four EXCLUSIVE NOR Gates, 586, 588, 590 and 592. The outputs of the EXCLUSIVE NOR Gates are connected together to line 594. The two inputs to EXCLUSIVE NOR Gate 586 are provided by lines 524 and 506, line 524 being the QA output of counter 420 and line 506 being the QA output of counter 502. The two inputs to EXCLUSIVE NOR Gate 588 are provided by lines 526 and 508, line 526 being the QB output of counter 420 and line 508 being the QB output of counter 502. The two inputs to EXCLUSIVE NOR Gate 590 are provided by lines 528 and 510, line 528 being the QC output of counter 420 and line 510 being the QC output of counter 502. The two inputs to EXCLUSIVE NOR Gate 592 are provided by lines 530, 512, line 530 being the QD output of counter 420 and line 512 being the QD output of counter 502.

As will be appreciated by those skilled in the art, the output of the EXCLUSIVE NOR gates will be high whenever the rabbit and the dog are coincident with one another. For example, assuming that the rabbit and the dog are both in the positions wherein the QA and QD outputs of their counters are high and the QB and QC outputs are low, therefore line, 524 and 506 are high, and lines 530 and 512 are high. Since gates 586, 588, 590, and 592 are EXCLUSIVE NOR gates, all of their outputs are high and line 594 is high. Line 594 serves as the output of the Coincidence Detector.

In FIG. 13 there is shown the logic details of the Inside Dog Position Advance Circuit 42. This circuit is identical in construction with the outside dog position advance circuit 430. The Outside Dog Position Advance Circuit is coupled to the Outside Dog Position Counter 422 in the same manner that the Inside Dog Position Advance Circuit 428 is connected to the Inside Dog Position Counter 420, the Outside Dog Position Advance Circuit 430 is coupled to the Coincidence Detector 438 is connected to the Coincidence Detector 436, the Outside Dog Position Advance Circuit 430 is connected to the 30 hz output of the Clock Pulse Generator in the same manner that the Inside Dog Position Advance Circuit 428 is connected thereto and the Outside Dog Position Advance Circuit 430 is connected to the 3.75 hz output of the clock pulse generator in the same manner that the Inside Dog Position Advance Circuit 428 is connected thereto, and the Outside Dog Position advance Circuit is connected to the Winner Decoder Circuit 448 in the same manner that the Inside Dog Position Advance Circuit is connected to the Winner Decoder Circuit. Furthermore, the outside Dog Position Advance Circuit 430 is connected to the output terminal 491 of the receiver in the same manner that the Inside Dog Position Advance Circuit 428 is connected to the output line 501 of the receiver. Accordingly, the details of the Outside Dog Position Advance Circuit 430 will not be described herein in detail.

As can be seen, the Inside Dog Position Advance Circuit 428 includes three flip-flops namely, flip-flops 596, 598 and 600. The Q output of flip-flop 596 is provided to the D input of flip-flop 600 to the inverting clear input of flip-flop 600 via line 602 and to one input of AND gate 604. Another input to AND gate 604 is provided by line 606 from the $\bar{Q}$ output of flip-flop 600.

The third input to AND gate 604 is provided by line 580 from the 30 hz output of the clock pulse generator. The output of gate 608 is provided into one input of an OR GATE 610. The other input thereto is provided by line 612 from an AND gate 614. One input to AND gate 614 is provided by the $\bar{Q}$ output via line 616. The other input to AND gate 614 is provided by line 504 from the 3.75 hz output of the clock pulse generator.

The output of OR gate 610 is provided by line 620 to the clock input of a register 622. Register 622 is adapted for shifting pulses either serially therethrough or parallelly therethrough depending upon the logic state of the signal applied to a mode control input MC thereof. The Signetics Corporation register model No. 54/7495 is particularly suited for use circuit 428. Register 622 includes four parallel inputs namely A, B, C, and D and four outputs namely QA, QB, QC and QD.

As can be seen the output QD is connected to the C input of the register, the output QC is connected to the B input thereof and the output QB is connected to the A input thereof. The D input is connected to a positive 5 volts. The register also includes a series input S which is connected to ground. The clock input of the register denoted as CLK serves to clock the register in either mode of operation. The mode control input MC of the register is provided by line 624. The QD output of the register 622 is provided by inverter 626 to line 628.

Line 624 is the output of AND gate 630. One input to AND gate 630 is provided by line 504 from the 3.75 hz output of the clock pulse generator and the other input to gate 630 is provided by line 594 which is provided from the output of the Coincidence Detector 436.

The line 594 from the coincidence detector also serves as one input to OR gate 632. The other input to the OR GATE is provided from line 638. Line 638 is the output of AND gate 634. One input of AND gate 634 is provided by line 602 from the Q output of flip-flop 596 and the other input to the AND gate is provided by line 636 from the $\bar{Q}$ output of flip-flop 598.

The $\bar{Q}$ is provided via line 616 to one input to gate 640. The other input to gate 640 is provided by line 628 from inverter 626. The output of gate 640 is provided to the D input of flip-flop 598. The Q output of flip-flop 598 is provided, via line 642, to one input to AND gate 644. Another input to AND gate 644 is provided by line 616 from the $\bar{Q}$ output of flip-flop 596 and a third input to gate 644 is provided via line 504 from the 3.75 hz output of the clock pulse generator. The output of AND gate 644 is provided via line 646 to one input of AND gate 648. The other input to AND gate 648 is provided by line 650. Line 650 is the output of an inverter 652 whose input is provided by line 654 from the Winner Decoder and Illumination Circuit 448.

The output of AND gate 648 is provided by line 520 to the clock input of the Dog Counter 420.

Operation of the Inside Dog Position Advance Circuit 428 is as follows. When the power supply is initially energized a short duration low going signal is provided along line 566. This effectively clears flip-flops 596 and 598. Upon flip-flop 596 clearing its Q input as provided by line 602 goes low whereupon the flip-flop 600 is cleared via low signal applied at its clear input terminal C. The low signal appearing at the clear input is provided by line 602 to one input of AND gate 604. The low signal appearing at this terminal disables the gate, whereupon the output along line 608 goes low. Line

608 serves as one input to OR gate 610. The other input to OR gate 610 is provided by line 612 from AND gate 614. One input to AND gate 614 is provided by line 616 from the high on the $\bar{Q}$ output of flip-flop 596. Accordingly, AND gate 614 is enabled and 3.75 hz clock pulses are provided from the clock pulse generator via line 504 through AND gate 614 to appear at output line 612. The 3.75 hz clock pulses pass through OR gate 610 and are applied, via line 620, to the clock input of register 622.

Assuming that the rabbit and the inside dog are not coincident, line 594 is low, thereby disabling AND gate 630 such that it provides a low signal via line 624 to the mode control input of register 622. The occurrence of a low signal on the mode control input of register 622 enables the register to operate in its series mode each time that it is clocked. In this series mode low signals are shifted into the register from ground via the S input thereof each time that the register is clocked. Accordingly, it should be appreciated that so long as the rabbit and the dog are not coincident the register is in its series mode of operation wherein its QA, QB, QC, and QD terminals are all low.

At the same time that the register is operating as described above, the high signal appearing on the $\bar{Q}$ output of cleared flip-flop 596 is provided at one input to gate 640. The other input of gate 640 is provided by line 628 which is high as a result of the low signal appearing on the QD output of register 622 being inverted by inverter 626. The two high signals appearing on the inputs of gate 640 to result in a low signal appearing at its output and at the D input terminal to flip-flop 596.

So long as flip-flop 598 remains cleared (in the state where its Q output as provided by line 642 b is low) AND gate 644 will be disabled, thereby disabling AND gate 648. As previously noted the output of AND gate 648 is provided via line 520 to the clock input to the inside dog counter 420. Accordingly, so long as flip-flop 598 is cleared, the inside dog position counter is precluded from advancing.

Assuming that the rabbit becomes coincident with the dog, operation is as follows. A high signal appears on line 594 and is provided to one input of AND gate 630. The other input of AND gate 630 is provided via line 504 from the 3.75 Hz clock pulses from the clock pulse generator. Accordingly, during the interval that line 504 is high, i.e., during one 3.75 hz clock pulse, the mode control input MC to register 622 is high and the register operates in its parallel mode of operation.

When operating in its parallel mode of operation, the register is operative upon a first clock pulse applied to its clock input to shift a high signal into the QD output thereof. Since the QD terminal is connected to the C input terminal and the QC terminal is connected to the B input terminal and the QB terminal is connected to the A input terminal, upon the occurrence of the next clock pulse high signals appear on both the QC and QD output terminals. Upon the next clock pulse, high signals appear on the QD, QC and QB output terminals and on the fourth clock pulse applied to the register all of the output terminals QD, QC, QB and QA are high.

If the clock signals to the clock input are suppressed, irrespective of the state of the mode control input MC, the output terminals of the register will remain in the same state as existing at the time of the suppression of the clock signals.

As the result of the coincidence of the rabbit and the inside dog, line 594, as previously noted is high. This high signal is provided via OR gate 632 to the D input of flip-flop 596. Upon the occurrence of the first scoring pulse from Scoring Pulse Forming Circuit 426, 5 which pulse occurs immediately after the commencement of the interval during which the rabbit and the dog are coincident, flip-flop 596 sets and flip-flop 598 remains in its cleared state.

Upon the setting of flip-flop 596 its Q output 10 goes high and this high signal is provided by line 602 to one input to AND gate 604. Another input to AND gate 604 is provided via line 606 from the $\bar{Q}$ output of flip-flop 600. As previously noted, this flip-flop is cleared such that line 606 is high. Accordingly, 30 hz 15 clock pulses as provided by line 580 from the clock pulse generator are enabled to pass through gate 604 via line 608 to one input of OR gate 610. The 30 hz clock pulses pass through OR gate 610 and are provided to the clock input to register 622. During the first 20 four 30 hz clock pulses provided to the clock input of register 622, the mode control input to the register is (i.e., the MC input is low until line 504 goes high upon the occurrence of a 3.75 hz clock pulse). The MC input to the register goes high during the second half of the 25 interval in which the dog and rabbit are coincident.

Upon the occurrence of the 3.75 hz clock pulse during the coincidence interval, AND gate 630 provides a high signal via line 624 to the mode control input of register 622. Accordingly, the 30 hz clock pulses appearing on line 620 effectuate the shifting of high signals into the register.

On the first 30 hz clock pulse following the commencement of parallel operation of the register, a high signal is clocked into the QD output terminal of register 35 622. On the next successive 30 hz clock pulse, another high signal is clocked into the register such that the QD and QC output terminals thereof are both high. On the next successive (third) 30 hz pulse another high signal is clocked into the register such that the QD, QC and QB output terminals thereof are high. On the next successive (fourth) 30hz clock pulse another high signal is clocked into the register such that all of the output terminals thereof are high.

As should be appreciated, the termination of the coincidence interval coincides with the termination of the fourth 30 hz clock pulse provided to register 622. Furthermore, at the termination of the coincidence interval, line 594 goes low whereupon gate 630 is disabled and a low signal is provided via line 624 to the mode control input to register 622. Accordingly, the register is enabled for serial operation.

When to QD output of the register goes high, i.e., when the register commences parallel operation, the high signal appearing on the QD output thereof is inverted by inverter 626 such that a low signal is provided along line 628 to one input of gate 640. The low signal appearing at that input to gate 640 results in a high signal appearing at that input to gate 640 which results in a high signal appearing at its output thereof and at the D input to flip-flop 598. Furthermore, since flip-flop 598 is at this time in its reset state, its $\bar{Q}$ output is high and is provided via line 636 to one input to gate 634. At the same time since flip-flop 596 is set its Q output as provided via line 602 to the other input of AND gate 634 results in a high signal appearing on line 638 from said AND gate. Line 638 serves as one input to OR gate

632. Accordingly, a high signal is maintained on the D input of flip-flop 596.

At the occurrence of the next successive scoring clock pulse from line 584, which clock pulse appears eight 30 hz clock pulses after the previous clock pulse, flip-flops 596 and 598 are clocked. As a result of being clocked flip-flop 596 remains in its set condition while flip-flop 598 switches to the set condition.

Assuming that the transmitter button is released at the optimum time, i.e., the point that the rabbit just passes the inside dog, operation is as follows. As previously noted when flip-flop 596 is set, its Q output as provided by line 602 is high. This high signal is provided at the D input to cleared flip-flop 600. Upon the release of the transmitter button associated with the inside dog line 501 from the receiver goes high thereby clocking flip-flop 600. This action results in flip-flop 600 setting whereupon its $\bar{Q}$ output as provided by line 606 goes low. Upon a low signal appearing on line 606, AND gate 604 is disabled and 30 hz clock pulses from the clock pulse generator provided via line 508 are precluded from passing therethrough. Accordingly, the output of AND gate 604, as provided by line 608, to one input to OR gate 610 is low. The other input to the OR gate, as provided by line 612, is also low since the set flip-flop 596 provides a low signal at its $\bar{Q}$ output, via line 616 to one input of AND gate 10, the clock input to register 622 provided by line 620 goes low.

As should thus be appreciated, upon the release of the transmitter button, the clock signals to the register 622 are suppressed.

Once the clock input to register 622 is low, the register is precluded from shifting out the high signals appearing on its output terminals even though the mode control input terminal MC goes low (thereby enabling serial operation) at the end of the interval that the rabbit and the dog are coincident with one another.

All of the output terminals of the register remain high until after the appearance of the next successive scoring pulse, i.e., the first scoring pulse after flip-flop 598 sets,

During the period of time after flip-flop 598 sets but before the occurrence of the first scoring pulse thereafter, the D input to flip-flop 596 is low and the D input to flip-flop 598 is high.

The low signal at the D input of flip-flop 596 is provided in the following manner: The $\bar{Q}$ output of the set flip-flop 598, being low, disables AND gate 634, which provides a low signal to OR gate 632. Since the rabbit and the dog are no longer coincident, the other input to OR gate 632, as provided by line 594, is also low. Thus a low signal appears at the output of the OR gate 532 and at the D input of flip-flop 596.

The high signal at the D input of flip-flop 598 is provided in the following manner: The high signal appearing at the QD output terminal of the register 622 is inverted by inverter 626 and provided as a low on line 628 to one input of gate 640. Since flip-flop 596 is set, its $\bar{Q}$ output thereof as provided along line 616 to the other input of gate 640 is also low. Accordingly, a high signal appears at the output of gate 640 and at the D input to flip-flop 598.

At the occurrence of the first scoring pulse after the flip-flop 598 sets, both flip-flops 596 and 598 are clocked via line 584, whereupon flip-flop 596 resets whereas flip-flop 598 remains set.

As a result of flip-flop 596 resetting, the Q output thereof goes low, thereby disabling gate 634 and providing a low signal into one input of OR gate 632. The other input of the OR gate 632 is also low since the rabbit is no longer coincident with the inside dog. Accordingly, the D input of flip-flop 596 has a low signal provided thereto.

The high signal appearing at the $\bar{Q}$ output of flip-flop 596 as a result of its resetting is applied to one input to gate 640. The other input to gate 640 is provided with a low signal via inverter 626 from the high QD output of register 622. Accordingly, a high signal appears on the D input to flip-flop 598.

At the same time, the high signal appearing on line 616 from the $\bar{Q}$ output of reset flip-flop 596 is provided to one input of AND gate 614 thereby enabling the gate. Accordingly, AND gate 14 is enabled to pass therethrough 3.75 hz clock pulses via line 504 from the clock pulse generator circuit. The 3.75 hz clock pulse signals pass through OR gate 610 and are supplied by supplied 620 to the clock input of the register 622.

The first 3.75 hz clock pulse is provided to the clock input terminal of register 622 before the appearance of the next consecutive scoring pulse from scoring pulse forming circuit 426. The 3.75 hz clock pulse is also enabled to pass through gates 644 and 648 and thus to appear at the clock input terminal 520 of the dog counter 420. That action occurs in the following manner. Since flip-flop 596 is cleared its Q output is high, which signal is provided via line 616 to one input of AND gate 644. At the same time since flip-flop 598 is set, its Q output is high and is provided by line 642 to another input to AND gate 644. The two high signals appearing on line 616 and 642 enable AND gate 644 to pass the 3.75 hz clock pulse appearing on line 504. Accordingly, the output line 646 of AND gate 644 goes high and is provided as one input to AND gate 648. The other input to AND gate 648 is provided by line 654, which is low since the game is in operation. The low signal on line 654 is inverted by inverter 652 to provide a high signal at line 650. The 3.75 hz clock pulse appearing on line 646 is enabled to pass through gate 648 by the high signal appearing on line 650.

Upon the trailing edge of the 3.75 hz clock pulse appearing at the clock input terminal of register 622 the register, now in its serial mode of operation (due to the low signal on its MC input terminal), shifts a low signal into itself, whereupon its QA output goes low. At this point in time the Q output of the reset flip-flop 596 disables AND gate 634 to thereby provide a low signal to one input of OR gate 632. Since the rabbit and the dog are no longer coincident, line 594 is also low whereupon the output of OR gate 632 as provided to the D input of flip-flop 596 is low.

Notwithstanding the fact that register 622 had shifted a low signal into its first position, i.e., QA being low, the QD output thereof remains high. This high signal is inverted by inverter 626 and provided to one input to gate 640. The low signal appearing on its input results in the gate 640 providing a high signal to the D input to flip-flop 598. Upon the next consecutive scoring pulse provided by line 584, i.e., the second scoring pulse after flip-flop 598 sets, flip-flops 596 and 598 are clocked but both remain in their previous states due to the input signals applied on their D inputs. Accordingly, AND gate 614 is enabled to pass another 3.75 hz clock pulse to the clock input of register 622 and the

AND gate 644 is enabled to pass the 3.75 hz clock pulse through enabled gate 648 to the clock input line 520 for the inside dog position counter 520.

Upon the occurrence of the trailing edge of the 3.75 hz clock pulse so provided, register 622 shifts another low signal into its serial input such that both the QA and QB outputs thereof go low. Notwithstanding this action, line 628 remains low whereupon gate 640 provides a high signal to the D input of flip-flop 598. At the same time, a low signal appears on the Q output of flip-flop 596 which disables gate 634 such that said gate provides a low signal to the input of OR gate 632. Since the dog and the rabbit are no longer coincident the other input to the OR gate as provided by line 594 is also low and a low signal continues to be provided at the D input of flip-flop 596.

Upon the occurrence of the next consecutive scoring pulse, i.e. the third scoring pulse after flip-flop 598 sets, flip-flops 596 and 598 are clocked but each remains in its previous state due to the signals appearing on their D input terminals.

As a result of the flip-flops remaining in their previous state, AND gate 614 remains enabled to pass another 3.75 hz clock pulse to OR gate 610 and into the clock input of the register 622. Furthermore, and AND gate 644 is enabled to pass said pulse therethrough to the input of enabled AND gate 648 such that the latter gate provides the pulse via line 520 to the clock pulse of dog counter 420.

Upon the trailing edge of the 3.75 hz clock pulse provided to the clock input of register 622, register 622 shifts a third low signal serially therein, whereupon the QA, QB, and QC outputs all are low. The high signal nevertheless remains on the QD output, which signal is inverted and provided along line 628 to the gate 640. Accordingly, the output of gate 640 remains low and this signal is provided to the input of flip-flop 598. A low signal appearing on the Q output of flip-flop 596 continues to disable gate 634, whereupon one input to OR gate 632 is low. The other input to the OR gate input is also low since the dog and rabbit are no longer coincident. Accordingly, a low signal continues to be provided to the D input to flip-flop 596.

Upon the occurrence of the next consecutive scoring pulse from line 584, i.e., the fourth scoring pulse after flip-flop 598 sets, flip-flops 596 and 598 are clocked but remain in their previous states due to the inputs appearing on their D input terminals. Accordingly, AND gate 10 is enabled to pass another 3.75 hz clock pulse therethrough and to the clock input of register 622. Furthermore the AND gate 644 is enabled to pass another 3.75 hz clock pulse therethrough and through enabled AND gate 648 to the clock input of the dog counter 420 via line 520. Upon the trailing edge of the 3.75 hz clock pulse passed through AND gate 614, register 622 is clocked whereupon a fourth low signal is shifted into the register such that all of the output terminals thereof are low.

The low signals thus appearing on the QD output terminal of register 622 is inverted by inverter 626 to provide a high signal which is provided, via line 628 to one input of gate 640. The other input to gate 640 is also high due to the reset flip-flop 596 providing a high signal at its $\bar{Q}$ output. Accordingly, the D input to flip-flop 598 provided by gate 640 is low.

As should thus be appreciated upon the occurrence of the next consecutive scoring pulse at line 584, i.e.,

the fifth scoring pulse after flip-flop 598 sets, flip-flops 596 and 598 are clocked whereupon flip-flop 596 stays reset and flip-flop 598 resets. Upon flip-flop 598 resetting its Q output as provided by line 642 goes low to thereby disable AND gate 644, thus preventing any further 3.75 hz clock pulses from passing therethrough.

Therefore, when the transmitter button associated with the inside dog is released at the precise moment that the rabbit passes the inside dog, four 3.75 hz clock pulses are enabled to pass to the clock input to the dog counter 420 to advance the dog positions.

As will be appreciated by those skilled in the art, if the transmitter button is released at a point in time that the QD, QC and QB terminals are high, which condition occurs slightly before or slightly after the point in which the rabbit passes the dog, three 3.75 hz clock pulses are enabled to pass to the clock input to the dog counter 420. If the transmitter button is released at a point in time when only the QD and QC output terminals of the register 622 are high, two 3.75 hz clock pulses are provided via line 520 to the clock input to the dog counter 420. If only the QD output terminal of register 622 is high when the transmitter button is released only one 3.75 clock pulse is provided by line 520 to the clock input of dog counter 420.

The Inside Dog Advance Circuit 428 is also arranged such that even if none of the output terminals of the register 622 are high at a point when the transmitter button is released or if the transmitter button is not released at all, one 3.75 hz clock pulse is nevertheless provided, via line 520, to the clock input of the Dog Counter 420.

Such operation is as follows, assuming that the transmitter button is not released at all. Circuit 428 operates in the identical manner to that previously described up until the time that flip-flop 598 sets. As will be remembered from the previous discussion at that time, AND gate 604 is enabled to pass 30 hz clock pulses therethrough. The 30 hz clock pulses are provided, via gate 610 to the clock input of register 622. At the end of the interval at which the rabbit and the dog are coincident, line 594 goes low whereupon gate 630 is disabled to cause a low signal to appear on line 624. This low signal causes the register to switch from parallel operation back into serial operation.

Under the assumption that the transmitter button is not released, flip-flop 600 remains cleared, whereupon the 30 hz clock pulses from the clock pulse generator continue to flow therethrough and into the clock input of the register 622. Upon the first 30 hz clock pulse appearing at the clock input of the register, the QA output of the register goes low. Upon the second 30 hz clock pulse provided to the clock input terminal the QB output terminal thereof goes low and the QA terminal remains low. Upon the third 30 hz clock pulse applied to register 622, the QC output terminal thereof goes low and the QB and QA terminals thereof remain low. Upon the fourth 30 hz clock pulse provided to the clock input of the register 622, the output terminal QC goes low and terminals QA, QB, and QC remain low. It should therefore be appreciated that four 30 hz clock pulses after flip-flop 598 sets, the register 422 is completely cleared.

Once the register is cleared the low signal provided at is QD output is inverted by inverter 626 to provide a high signal on line 628 and one input to gate 640. The other input to gate 640 is low since it is provided by the

$\bar{Q}$ output of set flip-flop 596. Accordingly, the D input of flip-flop 598 is provided with a high signal at this time. At the same time the $\bar{Q}$ output of set flip-flop 598 is low and disables gate 634 whereupon a low signal provided to one input of OR gate 632. The other input to the OR gate 632 is provided by line 594 and is low since the rabbit is no longer coincident with the dog. Accordingly, the D input to flip-flop 596 is low.

Upon the occurrence of the first scoring pulse after flip-flop 598 sets, flip-flops 596 and 598 are clocked, this action results in flip-flop 596 resetting whereas flip-flop 598 remains set.

As a result of flip-flop 596 resetting, its Q output goes high and is provided via line 616 to one input of AND gate 644. As a result of flip-flop 598 remaining set its Q output remains high and is provided via line 642 to another input of AND gate 644. The high signals appearing on line 616 and 642 enable gate 644 to pass a 3.75 clock pulse from line 504, therethrough and to one input to gate 648. Since the game is in progress a low signal appears on line 654 which is inverted by inverter 652 to provided a high signal on line 650 and thereby enable AND gate 648 to pass the 3.75 hz clock pulse appearing on line 646. Thus the 3.75 hz clock pulse passes through gate 648 via line 520, to the clock input terminal of the inside dog position counter 420.

Once flip-flop 596 resets its $\bar{Q}$ output thereof goes high and is provided to one input of gate 640. The other input of gate 640 is provided by line 628. This line is high at this time owing to the fact that the QD output of register 622 is low and is inverted to a high signal by inverter 626 and provided at line 628. The high signals appearing at the input terminals of gate 640 result in a low signal appearing at the output thereof and at the D input of flip-flop 598.

Upon the occurrence of the next consecutive scoring pulse, i.e. the second scoring pulse after flip-flop 598 sets, flip-flop 598 is clocked whereupon it resets. Once flip-flop 598 resets its Q output thereof goes low. The Q output of flip-flop 598 is provided by line 642 and disables gate 644 from passing any further 3.75 hz clock pulses therethrough.

Thus it should be appreciated that only a single 3.75 hz clock pulse is provided via line 520 to the dog position counter 420 by circuit 428 if the transmitter button associated with the inside dog is released at a time when the register 622 therein is empty.

The details of Lap Decoder and Illumination Circuit 444 are shown in FIG. 14. The Lap Decoder and Illumination Circuit 446 is of identical construction to Lap Decoder and Illumination Circuit 444 and is coupled to the Dog Counter 422 in the same manner that the Lap Decoder and Illumination Circuit 444 is coupled to the Dog Counter 420. Similarly, the Lap Decoder and Illumination Circuit 446 is coupled to the Winner Decoder and Illumination Circuit 448 in a similar manner that the Lap Decoder and Illumination Circuit 444 is coupled thereto. Accordingly, the details Lap Decoder and Illumination Circuit 446 will not be described herein.

As can be seen in FIG. 14 the Lap Decoder and Illumination Circuit 444 includes flip-flops 656, and 658. The clock input to flip-flop 656 is provided via inverter 660. The input to inverter 660 is provided by the QD output of the dog counter circuit 420 via line 530. The clear input terminals of the flip-flops are provided via line 662 from the output of inverter 664. The input to

inverter 664 is provided by line 522 from the Game Control Circuit 416.

The $\bar{Q}$ output of flip-flop 656 is connected via line 666, to the D input thereof and to one input to AND gate 668. Line 666 is also connected to the clock input of flip-flop 658. The other input to AND gate 668 is provided by the Q output of flip-flop 658 via line 670. The Q output of flip-flop 658 is connected to the D input thereof by line 672 and is provided as one input to AND gate 674. The other input to AND gate 674 is provided by line 676 which is connected to the Q output of flip-flop 656 and to one input of AND gate 678. The other input to AND gate 678 is provided by the line 670 connected to the Q output of flip-flop 658. The output of AND gate 678 is provided, via line 680, to the Winner Decoder and Illumination Circuit 448.

As can be seen the output of AND gate 674 is connected to one side of bias resistor 684. The other side of resistor 684 is connected to a positive voltage VCC. Voltage VCC is connected to one side of resistor 686, the other side of which is connected to the output of AND gate 668. The positive bias VCC is also connected to one side of resistor 688, the other side of which being connected to the output of isolating AND gate 682. The input of gate 682 is connected to line 680.

The output of AND gate 674 is also connected to one side of a current limiting resistor 690. Resistor 690 is in turn connected to the base of a transistor Q304. The output of AND gate 668 is connected to one side of resistor 692, the other side of which being connected to the base of transistor Q305. The output of gate 682 is connected to one side of resistor 694, the other side of which being connected to the base of a transistor Q306. The emitters of transistors Q304, Q305 and Q306 are connected together and to ground. The collector of transistor Q304 is connected to one side of a lamp 304, the collector of transistor Q305 is connected to one side of a lamp 305 and the collector of transistor Q306 is connected to one side of lamp 306. The other side of lamps 304, 305 and 306 are connected to a positive voltage such as 9 volts.

Lamp 304 when lit indicates that the inside dog has completed the first lap, lamp 305, when lit, indicates that the inside dog has completed the second lap and lamp 306, when lit, indicates that the inside dog has completed a third lap.

Operation of the circuit 444 is as follows. When the control circuit 416 is in its "Idle" state, it provides a reset or high signal on line 522. This signal is inverted by inverter 664 and provided as a low to the clear inputs to flip-flops 656 and 658 thereby clearing those flip-flops. When the game control circuit switches to its "Play" condition, the reset signal is removed and the clear signals thus disappear from the clear inputs to flip-flops 656 and 658.

When the inside dog completes one circuit of the track, the QD output of its counter goes low and the low signal is provided at line 530. This low signal is inverted by inverter 660 and effectuates the clocking of previously cleared flip-flop 656. This action causes flip-flop 656 to set (as a result of the high input signal fed from its $\bar{Q}$ output to its D input when the flip-flop was in its cleared state).

When flip-flop 656 sets, its Q output as provided by line 676 goes high. Accordingly, one input to AND gate 674 is high and one input to AND gate 678 is high. The

other input to gate 674 is provided by line 762 which is connected to the $\bar{Q}$ output of flip-flop 658. Flip-flop 658 is in its cleared state whereupon its $\bar{Q}$ output is high. Accordingly, a high signal appears at the output of AND gate 764. The high signal appearing at the output of the AND gate results in transistor Q304 becoming conductive whereupon lamp 304 is illuminated thereby indicating that the inside dog has completed one lap.

Upon the inside dog completing another lap of the track, the low signal appearing on line 530 is inverted by inverter 660 to clock flip-flop 656. Since theretofore flip-flop 656 was high, its $\bar{Q}$ output thereof was low, which low signal provided at is D input. Accordingly, when flip-flop 656 is clocked upon the dog completing the second lap, flip-flop 656 resets, whereupon its Q output goes high. The high signal appearing on the $\bar{Q}$ output of flip-flop 656 is provided via line 666 to one input to AND gate 668. The high signal appearing on line 666 also effectuates the clocking of flip-flop 658. Since the D input of flip-flop 658 theretofore had been high (flip-flop 658 was cleared), when flip-flop 658 is clocked by the high signal appearing on line 666, flip-flop 658 switches to its set condition, whereupon its Q output as provided by line 670, also goes high. Accordingly, both inputs to AND gate 668 are high whereby transistor Q305 turns on to result in the illumination of lamp 305 and indicate that the inside dog has completed a second lap.

Upon the inside dog completing another lap of the track, the low signal appearing on line 530 is inverted by inverter 660 and provided to the clock input of flip-flop 656. Prior to this time, flip-flop 656, having been reset, is providing a high signal at its D input via its $\bar{Q}$ output. Accordingly, when clocked, flip-flop 656 sets. Upon setting the Q output of flip-flop 656 goes high thereby providing a high signal to one input to AND gate 678. Flip-flop 658 does not change states since the low going signal which appears on the $\bar{Q}$ output of flip-flop 656 as it sets will not clock flip-flop 658. Accordingly, the Q output of flip-flop 658 remains high and is provided via line 670 as another input to AND gate 678. Accordingly, a high signal will appear on line 680 indicating that the inside dog has completed three laps. The high signal appearing at the output of line 678 is provided through isolating AND gate 682 and appears as a high at the output thereof. The high signal appearing at the output of AND gate 682 is provided to the base of transistor Q306 whereupon said transistor turns on to effectuate the illumination of lamp 306.

The details of the Winner Decoder and Illumination Circuit 448 are shown in FIG. 15. As can be seen therein, circuit 448 includes two input lines namely, line 680 which is provided by the Lap Decoder and Illumination Circuit 444 and by line 696 which is the comparable line from the Lap Decoder and Illumination circuit 446.

Another input to the Winner Decoder and Illumination Circuit 448 is provided by line 504 from the 3.75 hz clock output of the Clock Pulse Generator 424.

Input line 680 is connected to one input to NAND gate 698 and is also connected to inverter 700. The output of inverter 700 is connected, via line 702, to one input of NAND gate 703. Line 696 is provided to the other input to NAND gate 703 and is provided to inverter 704. The output of inverter 704 is provided by line 706 to the other input to NAND gate 698. The out-

put of NAND gate 698 is provided as one input to NAND gate 708 and the other input to NAND gate 708 is provided as one input to NAND gate 703. The output of NAND gate 708 is provided by line 710 to one input of NAND gate 712 and to one input of NAND gate 716. The other input to NAND gate 712 is provided by line 680. Line 680 also provides one input to NAND gate 714. The other input to NAND gate 716 is provided by line 696. Line 696 also provided the other input to NAND gate 714. The output of NAND gate 712 is provided by line 718, the output of NAND gate 714 is provided by line 720 and the output of NAND gate 716 is provided by line 722. Line 718 is provided as one input to gate 724, line 720 is provided as one input to gate 725 and line 722 is provided as one input to gate 728. The other input to gate 724, 726 and 728, respectively, are provided by line 504 which is the 3.75 hz clock output line of the Clock Pulse Generator. The output of gate 724 is provided to one side of register 730. The other side of resistor 730 is connected to a source of voltage VCC. Resistor 730 serves as a biasing resistor. The output of gate 726 is connected to one side of biasing resistor 732, the other side of which is also connected to voltage VCC. The output of gate 728 is provided to one side of biasing resistor 734, the other side of which is also connected to voltage VCC.

The output of gate 724 is also connected to one side of resistor 736, the other side of which being connected to the base of transistor Q308. The output of gate 726 is also connected to one side of resistor 738, the other side of which being connected to the base of transistor Q309. The output of gate 728 is also connected to one side of resistor 740, the other side of which is connected to the base of transistor Q307. The emitters of transistors Q308, Q309 and Q307 are connected together and to ground. The collector of transistor Q308 is connected to one side of lamp 308, the collector of transistor Q307 is connected to one side of lamp 307. The other side of lamps 308, 309 are connected together and to a source of positive voltage such as 9 volts.

Output Line 718 is also connected to one input to NOR gate 742. Output line 720 is connected a second input to said gate and output line 722 is connected to a third input to said gate. The output of gate 742 is provided to line 654 and serves as the "Game End" signal when it is logically high.

Operation of the circuit when the inside dog completes three laps before the outside dog is as follows. A high signal appears on line 680 indicating that the inside dog has completed three laps. A low signal appears on corresponding line 696 indicating that the outside dog has not completed three laps. The high signal appearing on line 680 is provided directly to one input of NAND gate 698. The low signal appearing on line 696 is inverted by inverter 704 and provided as a high at line 706 which is the other input to NAND gate 698. Accordingly, a low output appears at the output of NAND gate 698. The low signal appearing on line 696 is provided as one input to NAND gate 703. The high signal appearing on line 680 is inverted by inverter 700 and provided, via line 702, as a high to the other input to NAND gate 703. Accordingly, the output of NAND gate 703 will be high. The high and the low signal appearing on the inputs to NAND gate 708 result in a high signal appearing on the output thereof which signal is provided by line 710 as one input to NAND gate

712 and one input to NAND gate 716. The high signal appearing on line 680 is provided as the other input to NAND gate 712 and one input to NAND gate 714. Accordingly, the output of NAND gate 712 is low. The low signal appearing on line 696 is provided to the other input to NAND gate 716 and to the other input to NAND gate 714. Accordingly the high and low signal appearing on the inputs to NAND gate 714 result in a high signal appearing on its output. In a similar manner the high and the low signals appearing on the input to NAND gate 716 result in the NAND gate providing a high signal at its output thereof. A low signal appearing on the output of NAND gate 712 is provided as one input to gate 724. The other input to gate 724 is provided by line 504 which provided 3.75 hz clock pulses thereon. The output of gate 724 consists of inverted 3.75 hz clock pulses. The high signal appearing on the output of NAND gate 714 is provided as one input to gate 726 and effectively disables said gate and the high signal appearing on the output of NAND gate 716 is provided to one input of gate 728 which effectively disables that gate. The inverted pulse is provided at the output of gate 724 effectuates the repetitive conduction of transistor Q308 to thereby cause the repetitive illumination of lamp 308. This lamp, when flickering, indicates that the inside dog won the race.

Operation of the circuit 448 when the outside dog wins the race is in a similar manner to that which was previously discussed save for the fact that in such a condition transistor Q307 will be repetitively rendered conductive to thereby repetitively illuminate lamp 307.

Operation of the circuit 448 under a dead heat condition, i.e., when both inside and outside dogs complete three laps at the same moment, is as follows. The high signal appearing on line 680 is provided as one input to NAND gate 698 and the high signal appearing on line 696 is inverted by inverter 704 and provided as a low on line 696 is inverted by inverter 704 and provided as a low on line 706 which serves as the other input to NAND gate 698. Accordingly the output of NAND gate 698 is high. In a similar manner the high signal provided by line 696 is provided to one input of NAND gate 703. The high signal provided by line 680 is inverted by inverter 700 and provided as a low on line 702 which serves as the other input to NAND gate 703. Accordingly the output of NAND gate 703 will also be high.

The high outputs of NAND gate 698 and 703 are provided as inputs to NAND gate 708 and result in NAND gate 708 providing a low signal at line 710. The low signal appearing on line 710 is provided as one input to NAND gate 712 and as one input to NAND gate 714 thereby disabling said gate whereupon their output is high. The high signal appearing on line 780 is also provided as one input to NAND gate 714. The high signal appearing on line 696 is also provided as the second input to NAND gate 714. The two high signals appearing on the inputs of NAND gate 714 result in a low signal appearing at its output. The low signal appearing at the output of NAND gate 714 is provided as one input to gate 726. The other input to gate 726 is provided by 3.75 hz clock pulses along line 504. Accordingly the output of gate 726 will be inverted 3.75 hz clock pulses. These pulses effectuate the repetitive conduction of transistor Q309 and thereby enable lamp 309 to light repetitively to indicate the game ended in a dead heat.

As should be appreciated when the output of any of the NAND gate 712, 714 or 716 is low, thereby indicating that one or both dogs completed three laps of the track, the signals provided along lines 718, 720 and 722 cause NOR gate 742 to provide a high signal at its output terminal 654.

The high signal appearing on line 654 is provided to inverter 752 in circuit 428 to provide a low signal on line 650 to thereby disable gate 648 and preclude any pulses from going to the clock input to the Dog Counter 420. In a similar manner the signal 654 causes a corresponding NAND gate in the Outside Dog Position Advance Circuit to preclude the passage of clock signals to the clock input of the Dog Counter 422.

The details of the Infield and "Play Again" Decoder and Illumination Circuit 450 are shown in FIG. 16. As can be seen therein line 562 from the Coin Box 103 is provided as an input to an inverter 744. The output of the inverter is provided as one input to NOR gate 746. The other input of NOR gate 746 is provided by line 654 from the Winner Decoder and Illumination Circuit.

The output of NOR gate 746 is provided at line 748. Line 748 is connected as one input to inverter 750 and one input to AND gate 752. The other input to AND gate 752 is provided by line 546 which is the Q output of flip-flop 534 in the Game Control Circuit 416. The output of AND gate 752 is provided to one side of biasing resistor 754. The other side of biasing resistor 754 is connected to a positive voltage VCC. The output of inverter 750 is provided to one side of biasing resistor 756, the other side of which is also connected to voltage VCC. The output of AND gate 752 is provided to one side of current limiting resistor 758, the other side of which being connected to the base of transistor Q310. The output of inverter 750 is provided to one side of current limiting resistor 760, the other side of which being connected to the base of transistor Q311. The emitters of transistors Q310 and Q311 are connected together to ground. The collector of transistor Q310 is connected to one side of lamp 310 and the collector of transistor Q311 is connected to one side of lamp 311. The other side of lamps 310 and 311 are connected together to a positive voltage such as 9 volts.

Operation of the circuit 450 is as follows. A high signal is provided on line 562 by the Coin Box 103. This signal is inverted by inverter 744 and provided as a low at one input to NOR gate 746. When either dog completes three laps or when both of dogs complete three laps together, the Winner Detector Circuit provides a high signal via line 654 to NOR gate 746. Accordingly, the output of NOR gate 746, as provided along line 748, is low. The low signal is provided as one input to AND gate 752 and disables that AND gate. The low signal appearing on line 748 is inverted by inverter 750 to cause transistor Q311 to conduct, whereupon lamp 311 illuminates. Lamp 311, as previously noted, is behind the graphical representation of the infield on the track. Accordingly, when either dog wins or if a death heat results, the infield lights up.

As previously described, the game Control Circuit continues operation after a "Game Over" signal is provided. When the Game Control Circuit has recycled itself to the situation wherein both of its flip-flops are reset, a high or reset signal resets the counters in the dog position circuits 420 and 422 and also clears the flip-flops in the Lap Decoder and Illumination Circuits 444

and 446. As a result of this action, the "Game Over" signal appearing on line 654 terminates and line 654 goes low. As a result of line 654 going low, the output of NOR gate 746 goes high. This high signal is provided to one input to AND gate 752. The other input to AND gate 752 is provided by line 546 which is provided off the $\bar{Q}$ output of Game Control Circuit's flip-flop 534. As was previously noted during the condition wherein the Game Control Circuit 416 is providing a reset signal the $\bar{Q}$ output of flip-flop 534 is high. Accordingly, the output of AND gate 752 goes high and transistor Q310 is rendered conductive. Conduction of transistor 310 enables the illumination of lamp 310. This action illuminates legend "Play Again" at the center of the track.

When the game has recycled itself for renewed operation the infield lamp 311 is out and the lamp 310 is lit.

The rabbit, since its position is controlled by a free running counter, continues to circle the track via the sequential conduction of the lamps in its decoder circuit.

Without further elaboration, the foregoing will so fully illustrate my invention that others may, by applying current or future knowledge, readily adapt the same for use under various conditions of service.

What is claimed as the invention is:

1. An animated amusement game comprising, a display board, first means for establishing an animated display of a first object sequentially moving along a first path made up of plural positions on said board and second means for establishing an animated display of a second object sequentially moving along a second path made up of plural positions on said board, said second path being adjacent to said first path, said first means being arranged such that said first object overtakes and passes said second object, said second means being operative in response to first player actuated means wherein said second object advances a predetermined number of positions if said first player actuated means is operated at the moment that said first object overtakes said second object, whereas said second object advances a lesser number of positions if said first player actuated means is operated before or after said moment.

2. The game as specified in claim 1 wherein said second means comprises means for storing signals during a portion of the interval that said first object is beside said second object, said second means being arranged to cause said storage means to shift said signals thereout once said first object passes said second object unless said storage means is disabled, said storage means being disabled in response to said first player actuated means, said second means causing said second object to advance a predetermined number of positions in accordance with the number of signals in said storage means.

3. The game as specified in claim 1 wherein said first player actuated means provides a radio signal to said second means.

4. The game as specified in claim 1 additionally comprising third means for establishing an animated display of a third object sequentially moving along a third path made up of plural positions on said board, said third path being adjacent to said second path, said first means being arranged such that said first object overtakes and passes said third object, said third means being operative in response to second player actuated

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means, wherein said third object advances a predetermined number of positions if said first player actuated means is operated at the moment that said first object overtakes said third object, whereas said third object advances a lesser number of positions if said second player actuated means is operated before or after said moment.

5. The claim as specified in claim 4 wherein said first and said second player actuated means operate a radio transmitter to provide a radio signal to said first and second means.

6. The game as specified in claim 5 wherein said radio signal is a multiplexed signal having a main carrier signal which is modulated by alternating first and second subcarrier signals, said first subcarrier signal being provided in response to the first player actuated means and said second subcarrier being provided in response to said second player actuated means.

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7. The claim as specified in claim 6 wherein said radio transmitter includes means for enabling said first signal to modulate said main carrier during first alternate intervals in time if said first player actuated means is operative and for enabling said second signal to modulate said main carrier during second intermediate intervals in time if said second player actuated means is operated.

8. The game as specified in claim 7 wherein said game additionally comprises a radio receiver which is operative for separating said two subcarrier signals out of said multiplexed signal to enable said second means to advance said second object along said second path when said first player actuated means is operative and to enable said third means to advance said third object along said third path when said second player actuated means is operated.

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