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(54) Title: THERMAL DIODE FOR ENERGY CONVERSION

(57) Abstract: Solid state thermionic energy converter semiconductor diode implementation and method for conversion of thermal energy to electric energy, and electric energy to refrigeration. In embodiments of this invention a highly doped n^* region can serve as an emitter region, from which carriers can be injected into a gap region. The gap region can be p-type, intrinsic, or moderately doped n-type. A hot ohmic contact is connected to the n^*-type region. A cold ohmic contact serves as a collector and is connected to the other side of the gap region. The cold ohmic contact has a recombination region formed between the cold ohmic contact and the gap region and a blocking compensation layer that reduces the thermoelectric back flow component. The heated emitter relative to the collector generates an EMF which drives current through a series load. The inventive principle works for hole conductivity, as well as for electrons.

THERMAL DIODE FOR ENERGY CONVERSION

BACKGROUND MATERIAL

5 **1. Field of the Invention**

This invention relates to the conversion of thermal energy to electric energy, and electric energy to refrigeration, and more particularly to a solid state thermionic converter using semiconductor diode implementation.

2. Relevant Technology

10 Thermionic energy conversion is a method of converting heat energy directly into electric energy by thermionic emission. In this process, electrons are thermionically emitted from the surface of a metal by heating the metal and imparting sufficient energy to a portion of the electrons to overcome retarding forces at the surface of the metal in order to escape. Unlike most other conventional methods of generating electric energy, 15 thermionic conversion does not require either an intermediate form of energy or a working fluid, other than electric charges, in order to change heat into electricity.

In its most elementary form, a conventional thermionic energy converter consists of one electrode connected to a heat source, a second electrode connected to a heat sink and separated from the first electrode by an intervening space, leads connecting the 20 electrodes to the electric load, and an enclosure. The space in the enclosure is either highly evacuated or filled with a suitable rarefied vapor, such as cesium.

The essential process in a conventional thermionic converter is as follows. The heat source supplies heat at a sufficiently high temperature to one electrode, the emitter, from which electrons are thermionically evaporated into the evacuated or rarefied-vapor-25 filled interelectrode space. The electrons move through this space toward the other electrode, the collector, which is kept at a low temperature near that of the heat sink. There the electrons condense and return to the hot electrode via external electric leads and an electric load connected between the emitter and the collector.

An embodiment of a conventional thermionic converter 100 is schematically 30 illustrated in Fig. 1. These conventional devices typically comprise an emitter 110, or low electron-work-function cathode, a collector 112, or comparatively colder, high electron-work-function anode, an enclosure 114, suitable electric conductors 116, and an external load 118. Emitter 110 is exposed to heat flow 120 which causes this cathode to emit electrons 122, thus closing the electric circuit and providing an electric intensity to 35 load 118. As indicated above, interelectrode space 130 in conventional thermionic converters is an evacuated medium or a rarified-vapor-filled medium.

The flow of electrons through the electric load is sustained by the temperature difference between the electrodes. Thus, electric work is delivered to the load.

Thermionic energy conversion is based on the concept that a low electron work function cathode in contact with a heat source will emit electrons. These electrons are absorbed by a cold, high work function anode, and they can flow back to the cathode through an external load where they perform useful work. Practical thermionic generators are limited by the work function of available metals or other materials that are used for the cathodes. Another important limitation is the *space charge effect*. The presence of charged electrons in the space between the cathode and anode will create an extra potential barrier which reduces the thermionic current. These limitations detrimentally affect the maximum current density, and thus present a major problem in developing large-scale thermionic converters.

Conventional thermionic converters are typically classified as vacuum converters or gas-filled converters. Vacuum converters have an evacuated medium between the electrodes. These converters have limited practical applications.

Embodiments in a first class of gas-filled converters are provided with a vaporized substance in the interelectrode space that generates positive ions. This vaporized substance is commonly a vaporized alkali metal such as cesium, potassium and rubidium. Because of the presence of these positive ions, liberated electrons can more easily travel from the emitter to the collector. The emitter temperature in these types of conventional devices is in part determined by the vaporization temperature of the substance that generates the positive ions. Generally, the emitter temperature should be at least 3.5 times the temperature of the reservoir of the positive ion generating substance if efficient production of ions is to be achieved in these conventional devices.

Embodiments in a second class of gas-filled converters are provided with a third electrode to generate ions. The gas in the interelectrode space in these conventional devices is an inert gas such as neon, argon and xenon. Although these converters can operate at lower temperatures, such as about 1500 K, they are more complex.

Typical conventional thermionic emitters are operated at temperatures ranging from 1400 to 2200 K and collectors at temperatures ranging from 500 to 1200 K. Under optimum conditions of operation, overall efficiencies of energy conversion range from 5 to 40%, electric power densities are of the order of 1 to 100 watts/cm^2, and current densities are of the order of 5 to 100 A/cm^2. In general, the higher the emitter temperature, the higher the efficiency and the power and current densities with designs accounting for radiation losses. The voltage at which the power is delivered from one unit of a typical converter is 0.3 to 1.2 volts, i.e., about the same as that of an ordinary

electrolytic cell. Thermionic systems with a high power rating frequently consist of many thermionic converter units connected electrically in series. Each thermionic converter unit is typically rated at 10 to 500 watts.

The high-temperature attributes of thermionic converters are advantageous for certain applications, but they are restrictive for others. This is because the required emitter temperatures are generally beyond the practical capability of many conventional heat sources. In contrast, typical thermoelectric converters are operable at heat source temperatures ranging from 500 to 1500 K. However, even under optimum conditions, overall efficiencies of thermoelectric energy converters only range from 3 to 10%, electric power densities are normally less than a few watts/cm^2, and current densities are of the order of 1 to 100 A/cm^2.

From a physics standpoint, thermoelectric devices are similar to thermionic devices. In both cases a temperature gradient is placed upon a metal or semiconductor, and both cases are based upon the concept that electron motion is electricity. However, the electron motion also carries energy. A forced current transports energy for both thermionic and thermoelectric devices. The main difference between thermoelectric and thermionic devices is in the transport mechanism: ballistic and diffusive transport for thermionics and ohmic transport for thermoelectrics. Ohmic flow is microscopically diffusive, but not macroscopically so. The distinguishing feature is whether excess carriers are present. In thermoelectrics, the carriers normally present are responsible for current. In thermionics, the current is due to putting excess carriers in the gap. A thermionic device has a relatively high efficiency if the electrons ballistically go over and across the gap. For a thermionic device all of the kinetic energy is carried from one electrode to the other. The motion of electrons in a thermoelectric device is quasi-equilibrium and ohmic, and can be described in terms of a Seebeck coefficient, which is an equilibrium parameter.

In structures with narrow barriers, the electrons will not travel far enough to suffer collisions as they cross the barrier. Under these circumstances, the ballistic version of thermionic emission theory is a more accurate representation of the current transport. The current density is given by:

$j = A_0 T^2 e^{\frac{-e\varphi}{k_B T}}$, where A_0 is the Richardson's constant, φ is the barrier height (electron work function), e is the electron charge, k_B is Boltzmann's constant, and T is the temperature. Richardson's constant A_0 is given by $A_0 = (emk_B^2T^2)/(2\pi^2\hbar^2)$, where m is the effective electron mass and $\hbar$ is reduced Planck's constant.

The foregoing electron current density equation provides quantitative language for explaining some of the observations described above. For example, this equation for the emission current shows that the rate of emission increases rapidly with temperature, and it decreases exponentially with the work function.

5 Solutions to the foregoing problems have been sought according to the present state of the art by using vacuum converters or gas-filled converters. Attempts to reduce space-charge effects with vacuum converters have involved the reduction of the interelectrode separation to the order of micrometers. Attempts to reduce the same effects with gas-filled converters have led to the introduction of positive ions into the
10 cloud of electrons in front of the emitter. Nevertheless, these conventional devices still present shortcomings such as those related to limited maximum current densities and temperature regimes. Consequently, there remains a need to provide a more satisfactory solution to converting thermal energy to electric energy at lower temperature regimes with high efficiencies and high power densities.

15
SUMMARY OF THE INVENTION

The present invention was developed to fill a need for a device which efficiently converts thermal energy to electric energy at relatively low operating temperatures and with power densities and efficiencies high enough for commercial applications. The present invention also operates in reverse mode to provide efficient cooling.

20 The present invention seeks to resolve a number of the problems which have been experienced in the background art, as identified above. More specifically, the apparatus and method of this invention constitute an important advance in the art of thermionic power conversion, as evidenced by the characteristics of embodiments of this invention.

Briefly summarized, objects of the present invention are achieved by solid state
25 converter comprising an emitter having at least a region comprising a first donor at a concentration N_d^*, a collector and a gap region between the emitter and the collector in electric and thermal communication with the emitter and the collector. The gap region comprises a semiconductor with a second donor at a concentration N_d, which is selected so that the natural logarithm of the ratio N_d^* / N_d is between 0 and about 7.

30 Other embodiments of the present invention comprise a solid state thermionic converter utilizing semiconductor diode implementation comprising an emitter that comprises an n^*-type region; a gap region between the emitter and a collector, the gap region being adjacent to said n^*-type region; and a cold ohmic contact connected to said gap region, said cold ohmic contact having a recombination collector region formed
35 between said cold ohmic contact and said gap region. In some embodiments of this invention a collector provides a recombination element and such collector is in electric

communication with a cold ohmic contact. A hot ohmic contact is in electric communication with the emitter. The gap region may be n-type, p-type, or intrinsic. To use the electric current generated by embodiments of the converter of this invention, the electric circuit is typically closed externally with an electric load connected to the hot ohmic contact and the cold ohmic contact. It is understood that terms such as "electric communication", "electric connection" and "electric contact" refer to a relationship between elements whereby electric current can flow between such elements, whether such elements are in direct contact or the electric current flow is facilitated by at least one conductor linking such elements.

Still other embodiments of the present invention comprise a plurality of plates, each comprising an emitter and a collector with a gap region therebetween.

In refrigeration embodiments, carrier transport is assisted by an external electric field. A first ohmic contact on the emitter, comprising in one embodiment an n^*-type region, is connected to a thermal load that is cooled by heat flow from electrons leaving the emitter. As described in connection with embodiments of heat-to-electricity converters according to this invention, electrons in refrigeration embodiments circulate from the emitter, preferably from a hot ohmic contact on the n^*-type region, to the gap region. A gap region is in one embodiment adjacent to the emitter, and a second ohmic contact having a recombination collector region is formed between the second ohmic contact and the gap region. The gap region in embodiments of this invention may be n-type, p-type, or intrinsic. A heat exchanger dissipates the heat from hot electrons on the second ohmic contact connected to the gap region.

BRIEF DESCRIPTION OF DRAWINGS

In order to more fully understand the manner in which the above-recited advantages and objects of the invention are obtained, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope, the presently preferred embodiments and the presently understood best mode of the invention will be described with additional detail through use of the accompanying drawings in which:

FIG. 1 schematically shows an embodiment of a conventional thermionic converter.

FIG. 2 is a cross-sectional view of a thermal diode of the present invention.

FIG. 3 is a plot of the normalized conductivity parameter χ as a function of temperature for InSb, assuming that $N_D^* = 10^{20} cm^{-3}$.

FIG. 4 shows electron and hole concentrations for an n^*pn^* thermionic structure in InSb, where the donor concentration in the emitter and collector regions is 10^{20} cm^{-3}, and the acceptor concentration in the gap region is 10^{17} cm^{-3}.

5 FIG. 5A shows electron concentrations for an n^*nn^* thermionic structure in InSb, where the donor concentration in the emitter and collector regions is 10^{20} cm^{-3}, and the donor concentration in the gap region is 10^{14} cm^{-3}.

FIG. 5B shows the normalized conductivity χ as a function of temperature for several semiconductors.

10 FIG. 6 shows electron and hole concentrations for an n^*nn^* thermionic structure in InSb, where the donor concentration in the emitter and collector regions is 10^{20} cm^{-3}, and the donor concentration in the gap region is 8 x 10^{17} cm^{-3}.

FIG. 7 shows the normalized barrier height Δu as a function of the doping concentration.

15 FIG. 8 shows short circuit current as a function of normalized barrier height for the structures considered above with T_{max} = 600 K and $\Delta\tau = 0.5$.

FIG. 9 shows current and voltage characteristic for a 625 μ thick InSb design, with an emitter electron concentration of 10^{20} electrons/cm^3, an emitter temperature T_{max} = 600 K and a collector temperature T_{min} = 300 K.

20 FIG. 10 shows the load power per unit area for a 625 μ thick InSb design, with an emitter electron concentration 10^{20} electrons/cm^3, an emitter temperature T_{max} = 600 K and a collector temperature T_{min} = 300 K.

FIG. 11 shows the thermal power dissipated per unit area as a function of voltage for a 625 μ thick InSb design, with an emitter electron concentration 10^{20} electrons/cm^3, an emitter temperature T_{max} = 600 K and a collector temperature T_{min} = 300 K.

25 FIG. 12 shows the efficiency as a function of voltage for a InSb design. Calculations are shown for gap donor densities of 10^{17} (the lowest curve on the plot), 3 x 10^{17}, 5 x 10^{17} and 7 x 10^{17} (the highest curve on the plot) in units of cm^{-3}.

30 FIG. 13 shows the results of a numerical optimization of efficiency as a function of gap doping over a wide range of doping densities at a fixed emitter ionized dopant concentration of 10^{20} cm^{-3}.

FIG. 14 shows the results for the optimum efficiency as a function of emitter doping with fixed gap doping N_D = 7 x 10^{17} cm^{-3}.

FIG. 15 shows the thermal and load power per unit area for thermal diode designs.

35 FIG. 16 shows the efficiency of a design with an emitter electron concentration of 10^{20} electrons/cm^3 and a gap donor density of 7 x 10^{17} cm^{-3}.

FIG. 17 shows the optimized efficiency as a fraction of the thermodynamic limit.

FIG. 18 shows the thermal power flow under conditions of optimum energy conversion at different temperatures.

FIG. 19 is a cross-sectional view of a compensated thermal diode.

FIG. 20 shows the current as a function of gap doping for an InSb thermal diode
5 design.

FIG. 21 shows optimization of efficiency as a function of gap doping with *p*-type compensation using N_a^- concentrations of 7 x 10^{17}, 10^{18}, 2 x 10^{18} and 3 x 10^{18} cm^{-3}.

FIG. 22 shows a cross-sectional view of a single compensated thermal diode with increasing temperature indicated by the arrow labeled *T*.

10 FIG. 23A shows the efficiency under optimized conditions as a function of emitter temperature for different gap doping with perfect compensation. An InSb compensated thermal diode structure 625 μ thick is assumed, with an emitter electron density of 10^{20} cm^{-3} and a collector temperature of 300 K.

FIG. 23B shows the efficiency normalized to the thermodynamic limit under
15 optimized conditions as a function of emitter temperature for the different cases shown in Figure 23A.

FIG. 24 illustrates an embodiment having four stacked diodes.

FIG. 25 illustrates an embodiment having multiple stacked diodes having a curved boundary and forming a wedge-shaped geometry.

20 FIG. 26 illustrates an embodiment of stacked diodes wherein the stack boundary approximates an ideal curve as shown in Figure 25.

FIGS. 27A-27B show efficiency as a function of temperature for optimized embodiments of compensated thermal diodes wherein the collector temperature is about 300K according to this invention.

25 FIGS. 28 and 29 show the dose needed to create a compensated layer over a wide range of ion energies in an *n-type* InSb diode doped to a concentration *n*.

FIG. 30 shows the results for an ohmic contact implantation dose required to achieve a $10^{21}cm^{-3}$ shallow doping of Te for an InSb design.

FIG. 31 shows the ion range for FIG. 30.

30 FIG. 32 shows the results for Ag doping to achieve an ohmic contact.

FIG. 33 shows the results for Ag doping to achieve an ohmic contact.

FIG. 34 shows the temperature behavior of an InSb gap.

FIG. 35 shows the temperature dependence on barrier height for an interface layer doped with Te to $3x10^{19}cm^{-3}$ deposited on InSb doped with Te to $1x10^{18}cm^{-3}$ with an In
35 emitter.

FIG. 36A shows the surface states of a metal-semiconductor contact.

FIG. 36B schematically illustrates an embodiment of the present invention comprising a metal-semiconductor-interface-barrier reduction layer.

FIG. 37 shows the I-V curves for a single diode and a stack of three InSb diodes.

FIG. 38 shows a graph of one plate efficiency for InSb as a function of Ar ion implantation dose for a sample whose size is 0.50 x 1.0 x 1.5 mm^3.

FIG. 39 shows a graph of the ^4He ion implantation range as a function of ion energy for an InSb target.

FIG. 40 shows the results of a simulation for the number of vacancies per ion as a function of ^4He ion energy for the ion implantation referred to in FIG. 39.

FIG. 41 shows a graph of output current density for an embodiment comprising a $Hg_{0.86}Cd_{0.14}Te$ sample as a function of the hot side temperature for the sample with a Cu emitter layer and for the sample with an In-Ga emitter layer.

FIG. 42 shows a graph of output current density for an embodiment comprising a $Hg_{0.86}Cd_{0.14}Te$ sample as a function of the hot side temperature for the sample with an Al substrate and for the sample with an In-Ga substrate.

FIG. 43 shows a graph of the absolute efficiency as a function of temperature for an embodiment of a thermal diode without compensation comprising a $Hg_{0.86}Cd_{0.14}Te$ sample.

FIG. 44 shows a graph of the efficiency, expressed as a percentage of ideal Carnot cycle efficiency, as a function of temperature for the same embodiment referred to in FIG. 43.

FIG. 45 shows a graph of the absolute efficiency for an embodiment of a sandwich converter as a function of hot plate temperature.

FIG. 46 shows a graph of the efficiency, expressed as a percentage of ideal Carnot cycle efficiency, as a function of hot plate temperature for the same embodiment referred to in FIG. 45.

FIG. 47 shows a graph for the $Hg_{1-x}Cd_xTe$ normalized figure of merit relative to that of InSb as a function of x.

FIG. 48 illustrates a thermal diode for providing cooling.

FIG. 49 shows a compensated thermal diode for providing cooling.

FIG. 50 shows the coefficient of performance as a function of temperature for refrigeration embodiments.

DETAILED DESCRIPTION OF THE INVENTION

The present invention embodies a solid state thermionic energy converter 10, generally illustrated in Figure 2, and is directed to a method and apparatus for the conversion of energy. One embodiment of the inventive solid state thermionic energy

converter 10 comprises a semiconductor diode having an n^*-type region 14 as an emitter, a gap region 16 adjacent to the n^*-type region 14, a hot ohmic contact 12 connected to said n^*-type region 14, and a cold ohmic contact 20 being a collector and connected to said gap region 16. In one embodiment the cold ohmic contact 20 has a recombination
5 collector region 18 formed between said cold ohmic contact 20 and said gap region 16.

The recombination region in some embodiments of this invention comprises a distinct layer. In other embodiments of this invention the recombination region is obtained by treating and/or damaging the surface of an ohmic contact or collector. Forming a recombination region in the context of this invention thus includes procedures
10 for incorporating a recombination layer and procedures for treating and/or damaging the surface of an ohmic contact or collector.

The terms n^*-region are used herein to refer to an n-region which has a higher electron concentration than an n-region. Illustrative embodiments of materials comprised in n^*-regions are given below. A general characterization of the n^*-region and n-region
15 in terms of their relative donor number densities N_d^* and N_d is provided hereinbelow. Examples of n-type regions are provided by regions that include InSb doped with Te at a concentration from about 10^{16} cm^{-3} to about 10^{19} cm^{-3}. Concentrations in the order of 10^{20} cm^{-3} are also envisaged as characterizing the dopant concentration of materials in n-type regions in embodiments of this invention. Examples of n^*-type regions are
20 provided by regions that include InSb doped with Te at a concentration from about 10^{19} cm^{-3} to about $3 \cdot 10^{19}$ cm^{-3}. Concentrations of about $3 \cdot 10^{20}$ cm^{-3} are also envisaged as characterizing the dopant concentration of materials in n^*-type regions in embodiments of this invention. In addition to Te, dopants in some other embodiments of the present invention include at least one of S, Se, and Sn. Furthermore, the symbol n^{**} is used
25 herein to refer to an n-region which has a higher electron concentration than an n^*-region. Examples of n^{**}-type regions are provided by regions that include a material such as In, Te, Ga, and Fe.

An electric load R_L connected to hot ohmic contact 12 and to cold ohmic contact 20 is provided with the electric intensity generated by an embodiment of a converter
30 according to this invention. The emitter may be a metal. The gap region 16 may be either moderately doped n-type, p-type, or intrinsic. Electrons are collected in the recombination collector region 18. The heated emitter relative to the collector generates an EMF which drives current through a series load.

It is noted that the inventive principle works for hole conductivity, as well as for
35 electrons. Also, reference to metals herein includes alloys.

In contrast with conventional thermionic devices, embodiments of converters according to the present invention are solid-state devices. The prior art, however, teaches devices that rely on an evacuated interelectrode space or on a gas-filled interelectrode space. General characteristics of these conventional devices have been summarized above.

Instead of an evacuated or gas-filled space, embodiments of the present invention incorporate a semiconducting material. Semiconductors are valuable, not for their conductivity, but for two unusual properties. First, the concentration of free carriers, and consequently the conductivity, increases exponentially with temperature (approximately 5% per degree Celsius at ordinary temperatures). Second, the conductivity of a semiconductor can be increased greatly, and to a precisely controlled extent, by adding small amounts of impurities in the process called doping. Since there are two types of mobile charge carriers (electrons and holes), of opposite sign, extraordinary *distributions* of charge carriers can be created. The semiconductor diode utilizes this property. Semiconductors, pure or doped, p-type, or n-type, are bilateral; current flows in either direction with equal facility. If, however, a p-type region exists in close proximity to an n-type region, there is a carrier density gradient that is unilateral; current flows easily in one direction only. The resulting device, a *semiconductor diode*, exhibits a very useful control property of carrier transport that can be utilized for energy conversion.

The following written description and graphic material refer to models and/or simulations of phenomena that are associated with working embodiments of the present invention. References to these models and/or simulations are not meant to be limiting explanations of the present invention. It is understood that the present invention is not limited or restricted to any single explanation of its underlying physical processes. Models and/or simulations are intended to highlight relevant variables that can be used to design additional embodiments envisaged within the scope of the present invention, even though such embodiments are not explicitly referred to in the context of this written description. With these design tools, the teachings of this written description, and ordinary skill in the art, additional embodiments that are within the scope of the present invention and claims can be designed. Accordingly, the following written description and graphic material describe embodiments of the present invention and provide models that can be used for designing additional embodiments envisaged within the scope of the present invention.

It is understood that the headings in the following material are provided as guides for organization purposes and not as limiting or restrictive statements regarding this written description and figures, which are to be interpreted in their entirety as a whole.

Results for an InSb thermal diode are presented below because InSb is one of the semiconductor materials for embodiments of the present invention. The behavior of the InSb embodiment is shown to be consistent with the injection of carriers from the emitter into a gap region, with allowed transport across the gap to the collector. These results are consistent with the efficiency depending on gap doping, as the gap doping determines barrier height and current flow. These results also show that efficiency optimization of a thermal diode according to the present invention using InSb can reach 5.5% with a 600 K emitter and an emitter electron density of 10^{20} cm^{-3}.

The following written description and figures also disclose compensation as a technique to increase efficiency in embodiments of the present invention. Compensation includes return current suppression. Methods for forming ohmic contacts in embodiments of the present invention are subsequently described.

Examples of embodiments of the present invention that comprise InSb with a compensation layer include InSb wafers with a *n*-type dopant, such as Te, and an emitter layer of Te implanted by a technique such as magnetron sputtering. The compensation layer in these embodiments is formed by *p*-type impurity implantation. This *p*-type impurity comprises at least one type of ions such as Ar and He ions, which compensate for the *n*-type dopant.

Another material to build an n^*/n emitter according to this invention comprises $Hg_{1-x}Cd_xTe$. For example, a $Hg_{0.86}Cd_{0.14}Te$ wafer is used in embodiments of this invention to build a n^*/n emitter by reacting $Hg_{0.86}Cd_{0.14}Te$ with a *n*-type impurity substrate such as Al and In-Ga thus creating an electron injecting n^* region. One form of an In-Ga material for this purpose is $In_{0.75}Ga_{0.25}$. Embodiments with this emitter exhibit an output electric current density that increases as a function of the hot side temperature. It is shown below that these embodiments attain efficiencies that are above 30% of an ideal Carnot cycle efficiency.

$Hg_{1-x}Cd_xTe$ is part of a multi-plate, or sandwich configuration in other embodiments of this invention. For example, an embodiment of these sandwiches comprises an InSb plate doped with an *n*-type material such as Te and an emitter layer of InSb sputtered with Te and coated with a material such as In-Ga, more specifically, such as $In_{0.75}Ga_{0.25}$. A second plate in this sandwich material comprises $Hg_{1-x}Cd_xTe$, where x is in one embodiment 0.14.

Examples of embodiments according to the present invention include design parameters, uncompensated thermal diodes, compensated thermal diodes and Schottky diodes. Furthermore, converters according to the present invention include converters to convert thermal energy to electricity and refrigeration embodiments. As discussed

hereinbelow, two types of embodiments include the same main components, whether they operate as thermionic converters for refrigeration or as thermal diodes for converting thermal energy into electricity.

It has been found in the context of this invention that $Hg_{1-x}Cd_xTe$ with x being from about 0.08 to about 0.15 exhibits a high thermionic figure of merit while remaining semiconductor and allowing an n^* emitter layer/compensation layer design and behavior as described herein with respect to other materials. Furthermore, it has also been discovered in the context of this invention that $Hg_{0.92}Cd_{0.18}Te$ behaves as an excellent thermoelectric material.

1. The Solid State Thermionic Converter

A highly doped n^* region 14 in embodiments of the present invention can serve as an emitter region, from which carriers can be boiled off into gap region 16. The n^* region comprises a semiconductor doped with a high concentration of donor (providing electrons) impurity. For example, InSb can be doped with Te or S. It has been found in the context of the present invention that energy conversion is a function of the semiconductor normalized conductivity χ, which in turn is a function of the material parameters and peak emitter doping.

Relevant material parameters have been examined in the context of this invention to determine useful operational regimes for a number of semiconductors. This evaluation is presented hereinbelow to illustrate how relevant material parameters are selected for a number of materials and how this selection and evaluation can be extended within the scope of this invention to supplement the materials referred to hereinbelow.

Table 1 lists material parameters, including electron mobility and thermal conductivity, and the associated estimates of χ. Values for the normalized conductivity χ are estimated using $N_D^* = 10^{20}\,cm^{-3}$. One observes a wide range (almost four orders of magnitude) of possible values of the normalized conductivity χ. Data for the construction of this table were gathered from the *CRC Handbook of Chemistry and Physics*, 67th edition. Materials with small χ are more preferred. According to this criterion, a preferred material among the semiconductors listed in Table 1 is seen to be mercury selenide, with an associated value of χ = 0.014. With this normalized conductivity and a reduced potential of 5, the barrier optimized efficiency will reach about 13.3% and 23.8% for differences in emitter-collector temperatures relative to the emitter temperature ($\Delta\,\tau$) of 0.3 and 0.5, respectively. These efficiencies are close to half of the thermodynamic maximum values.

TABLE 1

Semiconductor	$\mu_e\left(\frac{cm^2}{V\sec}\right)$	$\kappa\left(\frac{W}{cm K}\right)$	χ
HgSe	20000	0.010	0.014
HgTe	25000	0.020	0.022
InSb	78000	0.160	0.057
CdSnAs2	22000	0.070	0.089
InAs	33000	0.290	0.25
PbTe	1600	0.023	0.40
PbSe	1000	0.017	0.47
ZnO	180	0.006	0.93
PbS	600	0.023	1.07
GaAs	8800	0.370	1.18
GaSb	4000	0.270	1.89
CdO	100	0.007	1.96
Ge	3800	0.640	4.72
InP	4600	0.800	4.87
Si	1900	1.240	18.3
GaP	300	1.100	103
$Bi_{0.9}Sb_{0.1}$	50,000	0.050	0.028
Se_xTe_{1-x}	10,000	0.035	0.097
Bi(‖trigon. axis)	35,000	0.053	0.042

Both the mobility and the thermal conductivity are, in general, functions of temperature. In InSb, both the mobility and the conductivity decrease with increasing temperature. The resulting temperature dependence of χ is illustrated in Figure 3. Figure 3 shows the normalized conductivity parameter χ (also referred to as "figure of merit") as a function of temperature for InSb, assuming that $N_D^* = 10^{20} cm^{-3}$. Results are shown for n-type gap regions with doping densities $N_D = 10^{15}$, 10^{16}, 10^{17}, 10^{18} in units of cm^{-3}. The normalized conductivity is seen to decrease at higher temperature. In addition, the normalized conductivity decreases in the presence of background carriers, since the

mobility of electrons in InSb decreases with increasing doping density. More generally, Figure 5B shows the normalized conductivity χ for a number of semiconductors.

Semiconductors listed in Table 1 are examples that include materials that can be used in embodiments of the present invention. InSb is one material among these semiconductors. As it will be shown hereinbelow, $Hg_{1-x}Cd_x Te$ is another semiconductor and it exhibits a normalized conductivity parameter of about half the value of the same parameter for HgSe.

It has been found in the context of this invention that concentrations in the emitter and gap regions can be related to the emitter-gap potential barrier. More specifically, the potential barrier between the emitter and a p-type gap relative doping concentrations was found to be

$$\Delta u = \ln\left[\frac{N_d^+ N_a^-}{n_i^2(T_{\max})}\right],$$

where Δu is the emitter-gap potential barrier, N_d^+ and N_a^- are the ionized donor and acceptor concentrations, n_i is the intrinsic carrier density, and $T_{\max}$ is the maximum emitter temperature.

The barrier in embodiments of this invention is up to about 7, preferably in the range from about 1.5 to about 7, and more preferably from about 3 to about 7. Unfortunately, it is not possible to achieve this for InSb in the absence of an independent gap bias for a p-type gap region in the vicinity of room temperature.

In the case of an n^* emitter to n-type gap region, the barrier height was determined to be

$$\Delta u = \ln\left[\frac{N_d^*}{N_d}\right].$$

A normalized barrier height of 5-7 corresponds to a doping ratio of e^5 - e^7, which evaluates numerically to 150 - 1100. If the n^* region is doped to a level of 10^{20} cm^{-3}, then the gap region doping should be in the range of 9 x 10^{16} cm^{-3} to 7 x 10^{17} cm^{-3}.

2. Results for the InSb Thermal Diode

a. Carrier injection

Referring to Figure 2, the emitter is the hot n^* region 14 to the left. The gap region 16 is a thick region in the center, which may be either n-type or p-type (although it was found that the efficiency is higher if the gap is n-type). The collector is depicted here as a recombination collector region 18 and metal contact 20 that is cold. A premise of designs of the present invention is that carriers are boiled off from a hot emitter region 14 into the gap region 16, where they transport to the collector region 18 and contact 20.

This section focuses on the issue of carrier injection from emitter into gap region, with three different choices of gap region type (*p*-type, intrinsic, and *n*-type). Electron injection into a *p*-type gap region would result in a much simpler problem to analyze, but there exists a significant barrier which occurs in the depletion region. The optimum efficiency occurs when the barrier is on the order of $4\ k_BT$. The barrier between an n^* emitter and a *p*-type gap is closer to 8-9 k_BT. Consequently, to inject a larger number of carriers, a lower barrier is needed. Lower barriers occur with moderate *n*-type gap regions, but then one must understand carrier injection of a majority carrier.

In the case of thermal electron ejection into a *p*-type gap region, the analysis of the *npn* bipolar junction transistor has been used in the context of this invention to show that these characterizations of carrier injection are basically correct. Figure 4 illustrates numerical solutions for charge emission from a hot n^*-type emitter into a *p*-type gap region. It is seen that electrons are emitted into the gap region and screened by the majority carrier holes, and the minority carrier transport occurs primarily through diffusion. The holes act to screen the field in the gap region.

A significant reduction in the barrier height occurs when the gap region is intrinsic. As the injected carrier densities can be significant, a lightly doped *n*-type gap region is utilized with 10^{14} cm^{-3} donors that will simulate an intrinsic gap region. This simulated intrinsic gap region will have a lower potential barrier than a pure intrinsic gap region. Results for carrier injection in this case are illustrated in Figure 4. Figure 4 shows electron and hole concentrations for an n^*pn^* thermionic structure in InSb. The donor concentration in the emitter and collector regions is 10^{20} cm^{-3}, and the acceptor concentration in the gap region is 10^{17} cm^{-3}. The emitter is at 600 K, and the collector is at 300 K. Three cases are illustrated: open circuit $i = 0$ (equilibrium) with no carrier injection; short circuit $v = 0$ with maximum current; and an intermediate case with v equal to half the open circuit voltage. It is seen that the electron and hole densities become very nearly equal, which implies that charge neutrality holds in the gap region to within what can be discerned on a graph of this type. It is thus verified numerically that charge injection into an intrinsic region is possible and that electrons injected into the gap region appear to be able to transport to the collector region.

Results for carrier injection in this case are further illustrated in Figure 5. Figure 5 shows electron concentrations for an n^*nn^* thermionic structure in InSb. The donor concentration in the emitter and collector regions is 10^{20} cm^{-3}, and the donor concentration in the gap region is 10^{14} cm^{-3}. The emitter is at 600 K, and the collector is at 300 K. Three cases are illustrated: open circuit $i = 0$ (equilibrium) with no carrier injection; short circuit $v = 0$ with maximum current; and an intermediate case with v

equal to half the open circuit voltage. It is seen that the electron and hole densities become very nearly equal, which implies that charge neutrality holds in the gap region to within what can be discerned on a graph of this type. It is thus verified numerically that charge injection into an intrinsic region is possible and that electrons injected into
5 the gap region appear to be able to transport to the collector region without difficulty.

The case where carriers are injected from an n^*-type emitter region into a moderately-doped n-type gap region is now examined. The numerical results are illustrated in Figure 6. Figure 6 shows electron and hole concentrations for an n^*nn^* thermionic structure in InSb. The donor concentration in the emitter and collector
10 regions is 10^{20} cm^{-3}, and the donor concentration in the gap region is 8 x 10^{17} cm^{-3}. The emitter is at 600 K, and the collector is at 300 K. Three cases are illustrated: open circuit $i = 0$ (equilibrium) with no carrier injection; short circuit v with maximum current; and an intermediate case with v equal to half the open circuit voltage. It is observed that electron injection occurs, and that the transport still looks more or less diffusive.

15 The results presented above show that electron injection from an n^* emitter region into the gap region occurs as expected in the case of a p-type gap, and also in both intrinsic and in n-type gap regions. Injection into a p-type gap region would be expected to follow a diode law. Heating the emitter region relative to the collector leads to a thermally-generated EMF. The collector in this configuration plays the same role as a
20 metallized contact in a diode. Consequently, the current could be calculated directly from a diode law. However, electron injection into intrinsic and n-type gap regions is now considered, for which there would be no reason *a priori* to expect a diode law to be satisfied. It is therefore of interest to investigate whether diode-type behavior extends into the new regimes, and what kinds of modifications might be expected.

25 To carry out such a study, current versus voltage characteristics are required, except that in the thermal energy converter there does not appear to be an adjustable voltage. The barrier height may be adjusted through a selection of the doping characteristic of the gap region. Figure 7 illustrates the normalized barrier height for the example considered above as a function of the gap doping. Figure 7 shows the
30 normalized barrier height Δu as a function of the doping concentration. The emitter is assumed to be doped to have 10^{20} electrons/cm^3. The donors and acceptors in the gap are assumed to be completely ionized. Using this result as a mapping between doping and barrier height, the short circuit current as a function of gap doping was simulated, and the results shown as a plot of the magnitude of the current as a function of barrier height.
35 This is illustrated in Figure 8. Figure 8 shows short circuit current as a function of normalized barrier height for the structures considered above with T_{max} = 600 K and an

emitter-collector temperature difference relative to the emitter temperature of 0.5. It is observed that the diode law is obeyed in the p-type regime away from intrinsic. It is also seen that, qualitatively, generic diode-type law behavior persists well into n-type regime. Such behavior is consistent with the postulated injection of carriers from emitter into gap
5 region, with allowed transport across the gap to the collector. This provides a numerical verification that modeling developed for this system based on diode-law behavior should be relevant.

b. The Current-Voltage Relation, Power and Efficiency

Having established the basic thermionic effect, attention now turns to the basic
10 issue of the optimization of the efficiency.

Illustrated in Figure 9 are representative curves showing computed current and voltage characteristics for the 625 μ thick InSb example considered above, with an emitter electron concentration of 10^{20} electrons/cm^3, an emitter temperature $T_{max} = 600$ K and a collector temperature $T_{min} = 300$ K. Results are shown for gap donor densities
15 of 10^{17} (the lowest curve on the plot), 3×10^{17}, 5×10^{17} and 8×10^{17} (the highest curve on the plot) in units of cm^{-3}. It is shown that to within an excellent approximation, the current and voltage relations are linear. It is also noted that as defined above, electrons boiled off of the emitter will give rise to a negative current, as well as a negative open circuit voltage. Figure 9 plots the magnitude of both current and voltage.
20 Figure 10 shows the computed load power per unit area for the 625 μ thick InSb example considered above, with an emitter electron concentration 10^{20} electrons/cm^3, an emitter temperature $T_{max} = 600$ K and a collector temperature $T_{min} = 300$ K. Results are shown for gap donor densities of 10^{17} (the lowest curve on the plot), 3×10^{17}, 5×10^{17} and 7×10^{17} (the highest curve on the plot) in units of cm^{-3}.
25 The thermal power per unit area dissipated by the device for the conditions used in the previous examples is illustrated in Figure 11. Figure 11 shows the computed thermal power dissipated per unit area for the 625 μ thick InSb example considered above, with an emitter electron concentration 10^{20} electrons/cm^3, an emitter temperature $T_{max} = 600$ K and a collector temperature $T_{min} = 300$ K. Results are shown for gap donor
30 densities of 10^{17} (the lowest curve on the plot), 3×10^{17}, 5×10^{17} and 7×10^{17} (the highest curve on the plot) in units of cm^{-3}. It is seen that the power is composed of a constant Fick's Law contribution at zero current (at the open circuit voltage), and a term linear in the current (and hence linear in the voltage).

Figure 12 shows the efficiency as a function of voltage for the InSb example
35 considered above. Calculations are shown for gap donor densities of 10^{17} (the lowest

curve on the plot), 3 x 10^{17}, 5 x 10^{17} and 7 x 10^{17} (the highest curve on the plot) in units of cm^{-3}. The dots are the efficiencies at the optimum points.

The results presented above show that the efficiency depends on the gap doping, as the gap doping determines the barrier height and corresponding current flow. A gap 5 donor doping near 7 x 10^{17} cm^{-3} appears to be near the optimum. To explore this optimization further, Figure 13 shows the results of a numerical optimization of efficiency as a function of gap doping over a wide range of doping densities at a fixed emitter ionized dopant concentration of 10^{20} cm^{-3}. If the gap doping is near intrinsic, the efficiency is low. This is ultimately because the associated emitter-gap barrier is high. 10 Accordingly, embodiments with near intrinsic gap doping that have a high emitter-gap barrier have a lower efficiency. If the gap doping gets to be too high, the beneficial effects of the low emitter-gap barrier is counter-balanced by the deleterious effect of the ohmic return current. This issue is examined further below.

c. Examination of scaling

15 The efficiency of the thermal diode design is a function of the emitter doping. The thickness is assumed to be 625 μ, the gap doping is maintained at 7 x 10^{17} cm^{-3}, and the emitter and collector temperatures are assumed to be 600 K and 300 K, respectively. The results are shown in Figure 14 for the optimum efficiency as a function of emitter doping with fixed gap doping N_D = 7 x 10^{17} cm^{-3}. It is seen that the efficiency increases 20 monotonically with the emitter electron concentration, but the scaling is less than linear. This is due to two interesting effects: the emitter-gap barrier increases at higher emitter doping since the gap doping was kept fixed; and the electron mobility decreases at higher carrier concentration. Both of these effects combine to reduce the beneficial impact of a larger emitter doping.

25 It is possible to implant Te (which is the lowest ionization energy donor) in the emitter at concentrations on the order of 10^{20} cm^{-3}. Simulation by utilizing the TRIM-91 code indicates that such a high dopant density will lead to the development of an amorphous emitter layer. Such a layer will have a different band gap, effective mass, and mobility than what we have modeled. In addition, one would expect that the 30 recombination rate would be very high. Some consequences of this can be anticipated. Electron injection into the gap will be limited to emitter densities that are available on the order of one recombination length into the emitter as measured from the gap side. This will be the case down to spatial scales that are on the mean free path of the electron.

The consequence of this is that a large amorphous emitter region with a gentle 35 scale length that is on the order of a micron will very likely present an effective doping density to the gap that is much less than the peak density achieved at the semiconductor

edge. On the other hand, a sharp n^* profile might allow free streaming of the electrons from the highly-doped amorphous region into a crystalline intermediate region. This latter picture would correspond more closely to the assumptions built into the model under discussion here.

Another important issue is that the ionization of the donor levels in the emitter will likely be incomplete. If the emitter region were crystalline at high doping levels, then the associated conduction band density of states would not be particularly large, so that the ionization balance of the donors will likely favor significant occupation of the donors. Data for the donor ionization energy is available (Te appears to have a donor ionization energy of 50 meV in InSb), so that the ionization fraction can be estimated. The use of a metal contact with a low work function at the emitter may circumvent associated problems, as the thermionic injection from a metal can be quite large.

Depending on the model used to simulate the efficiency of embodiments of the present invention, it is concluded that the optimum efficiency should be independent of the gap length or that this independence is nearly maintained for a gap thickness ranging between 200 μ and 2 mm. The thermal power is found to be proportional to the inverse gap thickness in any of the models considered in the context of this invention, as illustrated in Figure 15 for a thermal diode.

The previous discussion has focused on a total InSb wafer thickness of 625 μ. In the absence of recombination effects, thick layers would be preferred for large T_{max} applications, since the associated thermal flux would be correspondingly less. The recombination length of electrons in bulk n-type crystalline InSb for the gap densities that have been considered is at least 10 times the wafer thickness that has been examined. In addition, the total recombination rate is dominated by radiative recombination, which is likely to be strongly radiation trapped in large crystals such as considered here. Consequently, structures on the order of 1-2 mm should be interesting for energy conversion applications.

The effects of recombination on the device efficiency under conditions where recombination becomes important has not been addressed. While recombination effects might generally be assumed to be universally deleterious for thermionic energy conversion, this should probably not be second guessed in the absence of modeling results. The reason for this is that recombination increases the injected current over the diffusive limit considered here. While the thermal loss is inversely proportional to the gap length, the current would be inversely proportional to the recombination length. One might imagine that in this limit, the net result would be a net increase in the efficiency. This would be mitigated by the fact that the hole current required to support the

recombination would come with an associated potential drop. As the hole mobility is low in InSb, the associated potential drop is likely to be large.

Figure 16 shows the efficiency of a design with an emitter electron concentration of 10^{20} electrons/cm^3 and a gap donor density of 7 x 10^{17} cm^{-3}. The results are plotted as a function of the emitter temperature assuming that the collector temperature is 300 K. The results in the two cases are very nearly the same. The optimized efficiency as a fraction of the thermodynamic limit is illustrated in Figure 17. One observes that the design works more or less equally as well compared to the thermodynamic limit at all temperatures shown.

When the temperature difference is lower, the thermal power flow is less for a given design. Figure 18 shows the thermal power flow under conditions of optimum energy conversion for 626 μ and 1250 μ designs at different temperatures. The thermal power flow is in the range of a few hundred W/cm^2 under the optimum operating conditions of interest.

d. Summary

The previous discussion considered a model for a thermal "diode" based on an illustrative InSb implementation. This device uses a highly doped emitter region, a gap region which can be either *p*-type or *n*-type, and an ohmic metal collector with a sufficiently large work function arranged so as to have a negligible thermionic injection current above the ohmic contribution due to carrier equilibrium at the collector contact.

The results reported above show that to obtain the largest thermionic injection current, an emitter to gap barrier is required that is preferably on the order of 4-5 k_BT_{max}, which implies that the gap needs to be preferably an *n*-type semiconductor. Therefore, this invention envisages embodiments whose emitter to gap barrier is preferably in the range from about 4 k_BT_{max} to about 5 k_BT_{max}, as well as other embodiments in which this barrier is outside this range but that can be designed with the teachings provided herein.

As shown above, an n* region can inject electrons into an *n*-type gap region, and the transport is more or less diffusive in the gap region. Furthermore, it is also shown above that the thermal diode is capable of operation as an energy converter based on thermionic emission from the emitter into the gap, and subsequent transport to the collector. It has also been shown above how to optimize embodiments of the present invention as a function of gap donor concentration. The optimum efficiency of the thermal diode can be as high as 5.5% with a 600 K emitter, assuming that an electron density of 10^{20} cm^{-3} can be developed in the emitter. These parameters are characteristics of embodiments of this invention, although embodiments with other characteristics that

depart from this particular optimization and which are designed according to the teachings provided herein are also envisaged within the scope of this invention.

3. Results for the InSb Compensated Thermal Diode

Thermionic energy conversion efficiency in embodiments such as those
5 schematically illustrated in Figure 2 is ultimately limited by the presence of an ohmic return current due to the thermoelectric response of the semiconductor. If this return current could be suppressed, then a substantial increase in efficiency would be obtained. This section shows that it is possible to increase the efficiency by roughly a factor of 2 when the return current is reduced.

10 One scheme for reducing the return current involves compensating the *n*-type substrate with *p*-type doping to produce a nearly intrinsic layer in front of the collector contact in embodiments of the present invention, thus reducing dramatically the supply of available electrons that would initiate an ohmic return current. A trade-off is apparent in this approach because too much *p*-type compensation can restrict the flow of
15 thermionic current to the collector.

Work performed in the context of this invention shows that there is a small window within parameter space in which a compensated layer can be matched with the gap doping so as to simultaneously allow for nearly free thermionic current flow and nearly zero ohmic return current flow. The resulting designs have a very high predicted
20 efficiency for energy conversion, and may be competitive with the best of the thermoelectrics. As there exists other semiconductors with better mobility to thermal conduction ratios (such as HgSe and HgTe), the compensated diode scheme may have the potential to develop conversion efficiencies well in excess of the best thermoelectrics. As will be shown hereinbelow, —see for example the discussion regarding Figure 38—
25 compensation layers developed in the context of this invention showed a significantly improved performance for materials such as InSb. This improvement was quantified in an increase in efficiency by a factor of about 2. For $Hg_{1-x}Cd_xTe$, this improvement translates into efficiencies that approach the absolute limit of 50% of an ideal Carnot cycle efficiency.

30 Because these and other embodiments of compensated diodes, with such semiconductors that exhibit high mobility to thermal conduction ratios, can be designed by one with ordinary skill in the art in light of the teachings and examples provided herein, they are envisaged within the scope of the present invention.

A basic thermal diode structure implementation in InSb was considered as an
35 energy converter. The efficiency of the device was found to be limited to somewhat over 10% of the thermodynamic limit. A compensation is implemented as follows. As noted

above, it might be possible to increase the efficiency by suppressing the ohmic return current of opposite sign to the thermionic current. One way to do this is to use p-type doping to produce a compensated layer on the inside of the collector contact, which would prevent injection of electrons from the collector side of the device (see Figure 19).
5 Figure 19 schematically shows an embodiment of a compensated thermal diode according to this invention. The emitter is the hot n^* region 14 to the left. The gap region 16 is a thick region in the center, which is n-type. The collector is depicted here as a metal contact 20 that is cold. The hot ohmic contact 12 is adjacent to the hot n^* region 14. On the inside of the metal contact is a compensated region 19 created through the addition
10 of p-type doping that suppresses the electronic return current. The addition of p-type doping can produce a layer of p-type semiconductor if not precisely matched to the substrate doping, which can inhibit the thermionic electron current from reaching the collector. A small region is found to exist in parameter space around perfect compensation in which design numbers can be chosen that allow simultaneous collection
15 of the thermionic current and rejection of the ohmic return current. The efficiency computed for such a device was found to be substantially increased over that of the basic diode structure. This section considers this device and associated issues.

a. The return current

Before proceeding, the existence of the return current needs to be established in
20 the basic thermal diode. One way to do this is to plot the current, including the sign, as a function of the gap donor concentration. The result is illustrated in Figure 20. Figure 20 shows the current as a function of gap doping for the illustrative InSb thermal diode design considered in the last section. For the thermionic regime, which corresponds to a negative current (electrons moving from left to right), the current is computed under
25 conditions of optimum efficiency. For the thermoelectric regime, which corresponds to positive current (electrons moving from the collector to the emitter), the current is taken under conditions where the voltage is half of the thermally induced EMF, which is roughly where the optimum is in the thermionic regime. The thermally induced current is observed to change sign. At low gap doping, there is not enough conductivity for the
30 gap to sustain an ohmic component large enough to compete with the thermionic injection. When the gap doping increases, at some point the ohmic current surpasses the thermionic current in magnitude, and thermionic energy conversion is no longer possible. This ohmic return current is made up of electrons that originate on the collector side of the device, and transport primarily by drift to the emitter.

35

b. Optimization of the efficiency with a blocking layer

We now consider the predicted operation of the compensated thermal diode, which includes an intrinsic blocking layer. In the simulation, we model the compensation layer using Gaussian *p*-type doping with a characteristic length of 5 μ. Results for
5 different acceptor densities are shown in Figure 21. Figure 21 shows optimization of efficiency as a function of gap doping with *p*-type compensation using N_a^- concentrations of 7×10^{17}, 10^{18}, 2×10^{18} and 3×10^{18} cm^{-3}. The dotted line indicates the efficiency obtained in the absence of a blocking layer. The maximum efficiency is obtained when the acceptor concentration of the compensation layer is adjusted to match
10 the substrate donor concentration. A substantial increase in the optimum efficiency is obtained over the uncompensated case.

The shape of the efficiency curves shown in Figure 21 can be understood qualitatively from simple considerations. The efficiency is maximized under conditions where the blocking layer is intrinsic, which simultaneously allows transmission of the
15 thermionic current from the emitter, while producing a minimal return current. At lower gap donor concentration, the compensation layer produces a *p*-type region, which in this application behaves more or less as a reverse biased diode in rejecting the thermionic current. At higher gap donor concentration, the compensation is insufficient to eliminate excess electrons. A return current is initiated, with a magnitude that is roughly linear in
20 the electron concentration in the blocking layer. Consequently, a linear decrease is seen in the efficiency on the high side of the optimum.

From a practical standpoint, the capacity of the electrical current leads limits the current densities to 10^2 - 10^3 A/cm^2. Otherwise, the voltage drop in the wires becomes unacceptable. Moreover, there is a temperature drop across the diode of 200-300°C. For
25 the given thermal conductivity of InSb, this translates into a gap thickness of about 1cm. This thickness presents challenges such as the recombination length being comparable with the gap thickness and technological problems with polishing thick wafers. For example, most wafer processing equipment is designed for a thickness less than 1mm.

A typical approach to achieving thick gaps is to stack the diodes. Because the
30 current through the diodes stacked in series is the same, this means that stacked diodes should be current matched. One diode producing a larger current results in a voltage drop across the other diodes and reduced performance due to additional potential barriers.

The following discusses approaches to achieving current matching that can be implemented in the context of the present invention.

(1) **Gap doping concentration current matching**

The following example assumes an InSb diode material with all diodes having the same geometry and with a heat source temperature of 530 K and a heat sink temperature of 460 K. A single diode configuration is shown in Figure 22. The arrow in Figure 22 indicates that the temperature T of the hot ohmic contact 12 is higher than the temperature of collector 20. From the plot illustrated in Figure 23A and setting an efficiency level at 6%, four diodes may be stacked as shown in Figure 24, where the first diode (D_1) has a gap dopant concentration of $5 \cdot 10^{17}$ cm^{-3}, $D_2 \sim 7 \cdot 10^{17}$ cm^{-3}, $D_3 \sim 10^{18}$ cm^{-3}, and $D_4 \sim 2 \cdot 10^{18}$ cm^{-3}. In this embodiment all four diodes are producing the same current, and the overall efficiency stays at 6%. Although some embodiments of stacked diodes according to the present invention comprise diodes whose respective elements are manufactured with the same materials for each diode, it is understood that embodiments of stacked diodes in the context of this invention are not limited to such stacks. Some embodiments of stacked diodes according to the present invention comprise diodes whose respective elements are manufactured with different materials. For example, in some embodiments of stacked diodes the emitters in different diodes comprise different materials, and/or the gap regions in different stacked diodes comprise different materials, and/or the collectors in different stacked diodes comprise different materials.

(2) **Current matching by geometry**

The following example assumes the highest efficiency line on Figure 23A, corresponding to a gap donor concentration of $2 \cdot 10^{18}$ cm^{-3}. A thin diode in a series stack at 500 K produces a current that is approximately two times greater than the current produced in a non-stacked diode. Current matching will be achieved if the diode is at a temperature of 400 K and has an area that is twice as large as the area of a non-stacked diode. The results of this embodiment are shown in Figure 25, where the area change is in the form of a wedge-shaped collection of diodes. The boundary of a stack is actually not a straight line, but rather a curve that takes into account non-linear behavior of the efficiency curve on Figure 23A. The stack shown in Figure 26 shows another embodiment, where the stack boundary approximates an ideal curve as shown in Figure 25. The arrows in Figures 25-26 indicate increasing temperature, T, from T_{COLD} to T_{HOT}.

The compensated thermal diode design has been optimized to operate with maximum efficiency with a hot emitter at 600 K. It is of interest to determine the efficiency of the device at other emitter temperatures. Numerical results for the efficiency are illustrated in Figure 23A for different substrate dopings assuming perfect compensation. Figure 23A shows the efficiency under optimized conditions as a function of emitter temperature for different gap doping with perfect compensation. An InSb

compensated thermal diode structure 625 μ thick is assumed, with an emitter electron density of 10^{20} cm^{-3} and a collector temperature of 300 K. Gap donor concentrations and matched acceptor concentrations are (in order of increasing efficiency as plotted) 7 x 10^{17}, 10^{18}, 2 x 10^{18} and 3 x 10^{18} cm^{-3}. The dotted line indicates the efficiency obtained in the
5 absence of a blocking layer. Results for the efficiency normalized to the thermodynamic limit are shown in Figure 23B. Figure 23B shows the efficiency normalized to the thermodynamic limit under optimized conditions as a function of emitter temperature for the different cases shown in Figure 23A. One observes that the compensation layer is effective at high emitter temperature. In addition, optimization at high temperature
10 appears to produce relative optima at other temperatures such that separate designs optimized for different temperature regimes is not required. More advanced designs that work best around their design temperature, and not as well at other temperatures, will be discussed below.

c. Examples

15 Figures 27A-27B show efficiency as a function of temperature for optimized embodiments of compensated thermal diodes according to this invention. The curves in Figures 27A-27B are labeled according to the gap material, and numbers within brackets represent the carrier concentration. The efficiency shown in Figure 27B is given relative to that of a Carnot cycle.

20 A compensated layer in an *n-type* semiconductor can be made by, including but not limited to, introducing acceptors. For InSb doped with Te (donor impurity), the donor ionization energy is 50 meV. The same ionization energy is characteristic for acceptors created by vacancies. A compensated layer exists if the number of vacancies matches the initial donor concentration (n).

25 The number of vacancies is defined by the ion dose per unit area D (ions/cm^2) and the number of vacancies created by a single ion V, if vacancies are induced by ion implantation of an inert gas. V is a function of the ion energy E, $V = V(E)$. The number of vacancies is $N_v(E) = D \cdot V(E)$. In this case, the vacancy concentration c depends on the ion range in the material R, which is also a function of the ion energy $R = R(E)$. Thus,
30 for a given ion type, the vacancy concentration as a function of the ion energy is

$$C(E) = \frac{D\ V(E)}{R(E)}$$

for a compensated layer C(E) = n, or

35

$$D = \frac{n\ R(E)}{V(E)}$$

$R(E)$ and $V(E)$ were modeled using the TRIM-91 computer code for InSb and Ne, Ar and Xe ions. The modeling results are shown in Figures 28 and 29. The dose needed to create a compensated layer over a wide range of ion energies in an *n-type* InSb diode doped to a concentration n can be determined utilizing Figures 28 and 29 and the
5 equation for D given above. Lines 32 and 38 represent the curves for Argon, lines 34 and 36 for Neon, and lines 30 and 40 for Xenon in Figures 34 and 35, respectively.

Ion implantation creates a vacancy concentration profile which is more pronounced at the last 20-30% of the ion range. This 20-30% of the ion range can be decreased to less than the tunneling distance in InSb, which is typically between 100-150
10 Å, to avoid the formation of additional barriers.

Which ion is utilized requires a balancing of the pros and cons, such as the number of shallow levels that are created versus the damage to the solid structure. For example, Xe creates more shallow layers; however, it inflicts more damage and the crystal is semi-amorphous.

15 **d. Summary**

A modification of the basic thermal diode design introduced in the last section has been set forth which seeks to reduce the ohmic return current that limits the maximum efficiency of the device. It was demonstrated that an ohmic return current is present in the computations, and that it dominates the thermionic current at high gap doping.
20 Including a compensated layer on the inside of the collector is shown to reduce the return current, leading to a higher optimum efficiency. The results of the modeling indicate that perfect compensation produces the highest efficiencies for a given gap donor concentration. This conclusion is consistent with what could have been reasoned *a priori* from simple physical arguments. Therefore preferred embodiments of compensated
25 thermal diodes according to the present invention are characterized by high efficiencies, such that a larger compensation extent leads to a higher efficiency. The peak efficiency computed for the compensated thermal diode is competitive with the best thermoelectrics.

4. Ohmic Contact

An ohmic contact is defined as a metal-semiconductor contact that has a
30 negligible contact resistance relative to the bulk or spreading resistance of the semiconductor. (*See* Sze, S.M., *Physics of Semiconductor Devices*. N.Y., John Wiley & Sons, 1981, pp. 304-311, the contents of which are specifically incorporated herein.) This section describes ohmic contacts and methods for making such contacts according to this invention.

35 Metal-semiconductor interfaces introduce local potential barriers, which are known under the generic name of Schottky barriers. In its simplified form, the height of

a Schottky barrier ϕ_b measured relative to the Fermi level can be written as $\phi_b = \phi_m - \chi_s$, where ϕ_m is the metal electron work function and χ_s is the semiconductor electron affinity. Examples of the Schottky barrier values are 0.70 eV for GaAs and 0.18 eV for InSb.

5 For a solid state metal-semiconductor thermionic converter, the operating voltage range is lower than the Schottky barrier height. This will destroy the effect or at least bring down operating currents.

The typical operating voltage of the present invention is 10-100 mV and the power is 1-10 W. This results in an operating current of I_o = 100-1000 A. The power
10 loss on a Schottky barrier is $W_{loss} = I_o\phi_b$. For W_{loss} to be less than 1% of the total power, ϕ_b must be less than 1meV. The barrier is often expressed in terms of a contact resistance. Therefore, at the stated currents, the contact resistance must be less than 10^{-5}-10^{-6} ohm.

The references Chang et. al., *Specific Contact Resistance of Metal-Semiconductor*
15 *Barriers. Solid-State Electronics*, Vol. 14 (1971), pp. 541-550, and Shannon, J.M., *Control of Schottky Barrier Height Using Highly Doped Surface Layers. Solid-State Electronics*. Vol. 19 (1976), pp. 537-543, which are incorporated herein by reference, set forth a method of forming an ohmic contact. An electric field at the metal-semiconductor interface creates a carrier depleted region in the semiconductor. As the
20 concentration of ionized impurity increases, the depletion width becomes narrower. This in turn causes the transmission coefficient for tunneling to increase. Hence, even a high barrier contact can become ohmic if the barrier is thin enough such that tunneling dominates the carrier transport process. A dopant level corresponding to 10^{-6}ohm/cm^2 is 10^{20}-10^{21} (Te in InSb) at 300°C. The electron effective mass for tunneling increases
25 with temperature, and at 500°C the required concentration is 10^{21} rather than 10^{20}. A high dopant concentration layer must be sufficiently thin so it does not introduce its own barrier on the contacting semiconductor interface. The *Shannon* reference cited above estimates this thickness as less than 150 Å. This approach applies to both *n*-type and *p*-type doping, while keeping in mind that the current sign is reversed when going from an
30 *n*-type region to a *p*-type region.

The implantation dose required to achieve a 10^{21} cm^{-3} shallow doping was calculated by using the TRIM-91 computer code (G. Ziegler, G. Biersack. IBM (1991)). The ion range and required dose were calculated separately for In and Sb. The calculation results were averaged to approximate InSb. The difference between In and
35 Sb in this energy range was no more than 20%. Te was utilized as an *n*-type dopant

because Te has the lowest known ionization energy (50 meV). Figure 30 shows the calculation results for this dose, while Figure 31 shows the ion range.

For *p*-type doping, the known materials for InSb include Ge (9 meV ionization energy) and Ag (E_i = 30 meV). Ag is evidently a preferred ion since it is heavier than Ge and has a shorter range for the same ion energies, which allows for a smaller depleted region width. The calculations for Ag doping are shown in Figures 32 and 33. The ion implantation process creates vacancies which subsequently must be annealed.

Another method for forming an ohmic contact is through diffusion annealing. For example, an ohmic contact for a diode comprising InSb may be formed by annealing indium layers on InSb wafers. The following procedure was performed in an acid cleaned quartz ampule. The ampule was baked for more than one hour in a high vacuum at 800°C. The InSb samples having an indium coating were loaded into the quartz ampules, which was pumped down and filled with 10-100 torr of helium. Helium, which has a high thermal conductivity, provides for quick cooling. After annealing at various temperatures, I vs. V curves were measured on the samples to confirm that ohmic contacts existed. Positive results were obtained in the temperature range of 250-400°C with an annealing time of 10-60 minutes. At temperatures exceeding 500°C the indium dissolved completely rendering the samples unusable, even though the samples showed ohmic behavior.

5. Examples

a. Design parameters

Referring to Figure 2, intermediate, thermally conducting layers may be placed in other embodiments of this invention between the ohmic contacts (12, 20) and heat sinks to ensure thermal contact. For example, a deposited layer of In or the like may be used on the hot side and a deposited layer of In-Ga eutectic or the like may be used on the cold side. These materials are sufficiently malleable to ensure adequate thermal contact at low compression (0.1 - 1.0 MPa).

Accordingly, materials that can be used for these layers according to this invention are malleable thermal conductors, although other materials can be used in other embodiments. *Another method of providing thermal contact is the application of paste,* glue, a low temperature soldering alloy, or equivalents thereof. An electrically and thermally conducting layer is then added to serve as a diffusion barrier between a thermally conducting layer and a semiconductor. In this embodiment, the thermally and electrically conducting layer is used as an emitter without an additional semiconductor emitting layer. The characteristics and functions of this layer include, but are not limited to, the following: (1) conducts heat; (2) conducts electricity; (3) emits electrons; (4)

creates a Schottky barrier at the metal-semiconductor interface; (5) creates a diffusion barrier; (6) prevents a chemical reaction of a semiconductor with a subsequent layer; (7) matches the thermal expansion of a semiconductor to prevent delamination; (8) is thermally stable within the range of operation of the thermal diode; and (9) has a high
5 resistance to oxidation if not vacuum encapsulated or encased in an inert environment.

InSb, for example, has a thermal expansion coefficient of $5.2 - 5.4 \times 10^{-6}\ K^{-1}$ in the temperature range of 300-500 K. Other possible materials include, but are not limited to, Mo, Cr, W, Ta, Re, Os, Ir, lanthanoids and nickel alloys, Pt and soft metals such as In, Au, Cu or the like. From this list, Ta and the lanthanoids are prone to oxidation, and
10 In has a low melting temperature.

Highly doped semiconductors and semi-metals may also be used. For example, a thin layer of Si has a sufficiently high thermal and electric conductivity. However, certain precautions should be observed, and, in particular, it should be noted that a large forbidden gap when compared to InSb ensures the formation of an internal barrier which
15 impedes current transport.

The thickness of embodiments of the thermally and electrically conducting layer is designed as follows. The thermal conductivity is preferably higher than that of a semiconductor gap. With a gap thickness of 100-1000 microns, the thickness of the layer is preferably less than about a few microns since it will increase thermal losses. On the
20 thin side, there are a few considerations that define the layer thickness. For example, metal layers are preferably thicker than the electron mean free path in order to maintain its bulk properties. Since the layer is in close proximity to another metal (intermediate layer), it can affect its Fermi level position and change the electron emission into the semiconductor. This effect is known to be significant at metal layer thicknesses below
25 1000 Å. This number is at least a few electron mean free path lengths and can be regarded as a low practical limit in order to avoid unnecessary complications. Similar thickness considerations apply to the semiconductor emitter region n^*.

A preferred situation for the emitter-gap interface is when the region has matched crystallography, i.e., when the emitter region is grown epitaxially on top of the gap
30 region. For InSb this can be achieved by maintaining the deposition temperature above 150°C (PVD). For other gap materials, such as $Hg_{1-x}Cd_xTe$, the epitaxial growth is more complex. Scattering and decreased converter performance occurs when the emitter-gap interface is mismatched.

One skilled in the art of electric and thermal contacts recognizes there are
35 numerous methods of providing an adequate electric and thermal contact, and the scope

of this invention is not limited to the examples cited above, but it also envisages other embodiments designed according to different criteria.

b. Uncompensated thermal diodes

The following examples are intended to be illustrative of select embodiments of the present invention and not restrictive. The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The dopant concentration in the following examples (1)-(9) are given in units of cm^{-3}.

(1) **$metal_1$/*n*/$metal_2$**: InGa eutectic (bulk)/Cr or Ni (1000-4000 Å)/InSb (360 microns; doped with $1.1x10^{18}$ Te, orientation 100)/Pt (1500 Å)/ In (bulk). The thickness of *$metal_1$* cannot be less than the mean free path of electrons for the specific metal at a specific temperature, e.g., for Ag the mean free path is about 400 Å.

(2) **$metal_1$/*n**/*n*/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/InSb (400 Å; doped with $3.0x10^{19}$ Te)/InSb (360 microns; doped with $1.1x10^{18}$ Te)/Pt (1500 Å)/ In (bulk).

(3) ***$metal_1$/n**/n*/n/n***/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/InSb (400 Å; doped with $3.0x10^{19}$ Te)/InSb (360 microns; doped with $1.1x10^{18}$ Te)/In (100Å)/Pt (1500 Å)/ In (bulk).

(4) ***$metal_1$/n**/n*/n/n***/$metal_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $3.0x10^{20}$ Te)/InSb (360 microns; doped with $1.1x10^{18}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(5) ***$metal_1$/n**/n/n***/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (360 microns; doped with $1.1x10^{18}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(6) ***$metal_1$/n**/n/n***/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/In (100Å)/InSb (500 microns; doped with $1.1x10^{18}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(7) ***$metal_1$/n**/n*/n/n***/$metal_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $3.0x10^{20}$ Te)/InSb (500 microns; doped with $1.1x10^{18}$ Te)/In (100 Å)/Ni (1500 Å)/ In (bulk).

(8) ***$metal_1$/n**/n/n***/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (500 microns; doped with $1.9x10^{17}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(9) ***$metal_1$/n**/n/n***/$metal_2$** : InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (500 microns; doped with $1.9x10^{17}$ Te)/In (100 Å)/Ni (1500 Å)/ In (bulk).

c. **Compensated thermal diodes**

The following examples are intended to be illustrative of select embodiments of the present invention and not restrictive. The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. Layers referred to as having a low doping (p) may also be n-type. The dopant concentration in the following examples (1)-(5) are given in units of cm^{-3}.

(1) **metal$_1$/*n***/*n**/*n*/*p*/*n***/metal$_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $3.0x10^{19}$ Te)/InSb (500 microns; doped with $1x10^{18}$ Te; 2° from (100))/p-InSb (400 Å; doped with $3.1x10^{14}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(2) **metal$_1$/*n***/*n**/*n*/*p*/*n***/metal$_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $3.0x10^{19}$ Te)/InSb (500 microns; doped with $1x10^{20}$ Te; 2° from (100))/p-InSb (400 Å; doped with $3.1x10^{14}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(3) **metal$_1$/*n***/*n*/*p*/*n***/metal$_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (500 microns; doped with $1x10^{18}$ Te; 2° from (100))/p-InSb (400 Å; doped with $3.1x10^{14}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(4) **metal$_1$/*n***/*n**/*n*/*p*/*n***/metal$_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $3.0x10^{19}$ Te)/InSb (500 microns; doped with $1x10^{20}$ Te; 2° from (100))/p-InSb (2000 Å; doped with $3.1x10^{14}$ Te)/In (100 Å)/Pt (1500 Å)/ In (bulk).

(5) **metal$_1$/*n***/*n**/*n*/*p*/*n***/metal$_2$**: InGa eutectic (bulk)/Cr (1500 Å)/In (100 Å)/InSb (400 Å; doped with $1.0x10^{20}$ Te)/InSb (500 microns; doped with $1x10^{18}$ Te)/p-InSb (400 Å; where p-type region is ion implanted with Ar or Ne)/In (100Å)/Pt (1500 Å).

6. **Distributed Schottky Diode**

The formation of a Schottky barrier on a metal-semiconductor interface is well described in Rhoderick, E.H. and Williams, R.H., *Metal-Semiconductor Contacts*. Oxford, Clarendon Press (1988), which is incorporated herein by reference. Two major models of a Schottky barrier exist. For the Schottky-Mott model the barrier, ϕ_B, is considered to be the difference of a metal work function, ϕ_m, and semiconductor electron affinity, χ_s: $\phi_B = \phi_m - \chi_s$. In reality, ϕ_B is almost independent on the metal work function ϕ_m. The explanation by J. Bardeen is that the barrier is affected by surface states. Compensation of this charge is affected by the charge in the surface states Q_{ss}. And the electroneutrality condition is $Q_m + Q_d + Q_{ss} = 0$, where Q_m is the negative charge on the

surface of the metal and Q_d is the positive charge of uncompensated donors. The compensation ϕ_o barrier (neutral level) properties depends on the relative position of ϕ_o and the Fermi level E_F. If ϕ_o is measured relative to the top of the valence band, the Schottky barrier is as follows: $\phi_B \approx E_g - \phi_o$.

5 The gap energy E_g is a function of the temperature, and to some extent the dopant concentration. The accumulation of impurities on the surface affects ϕ_B as described in Section 4 regarding ohmic contacts. A partial impurity accumulation on the interface also affects the barrier height.

Figure 34 shows the temperature behavior of the InSb gap (*see* Landolt-Börnstein, 10 *Numerical Data and Functional Relationships in Science and Technology, Group III: Crystal and Solid State Physics*, (1983) Vol. 22b, the contents of which are specifically incorporated herein).

Schottky barrier values can be determined by the slope change of the curve taken from external I vs. V curve measurements. At room temperature the barrier height was 15 175-180 meV, irrespective of the dopant concentration (Te) in InSb up to 10^{20} cm^{-3} (in contact). Figure 35 shows the barrier height as a function of temperature for a 2000 Å interface layer doped with Te to $3x10^{19}$ cm^{-3} deposited on InSb doped with Te to $1x10^{18}$ cm^{-3} (500 μ) for an In emitter. Since the barrier height decreases with temperature at a faster rate than E_g, it means that the neutral level ϕ_o is higher than E_F, and the surface 20 density of states increases with temperature. Figures 34 and 35 provide for ϕ_o to be estimated at 15-20 meV at around 300°C. This type of barrier is illustrated in Figure 36A. The insulating film (oxide) shown in Figure 36A is so thin that carriers tunnel through without giving an appearance of an actual barrier, even if it is present. It has been found in the context of this invention that the implementation of this type of diode 25 increases operating temperatures of embodiments of this invention.

a. Experimental results

Samples were manufactured on the basis of InSb wafers doped with Te to $1x10^{18}$ cm^{-3}. The wafer thickness was about 500 microns and polished on both sides. After standard cleaning, an emitter layer of 2000 Å of InSb doped with Te to $3x10^{19}$ cm^{-3} 30 concentration was deposited on a wafer by magnetron sputtering. The sample size ranged from 1x1 to 3x3 mm^2 squares that were painted with InGa eutectic (T_m = 35°C) on both sides. The painting process involved the application of some pressure to destroy any surface oxide layer.

Figure 36B schematically illustrates an embodiment of the present invention 35 comprising a hot ohmic contact 12, an emitter 14, a gap region 16, a compensated region 19, and a collector 20. Region 15 is formed in some embodiments on the emitter side

that faces hot ohmic contact 12 to reduce the metal-semiconductor interface barrier. This metal-semiconductor-interface-barrier-reduction layer is formed in some embodiments by magnetron sputtering. Region 17 is formed in some embodiments on the gap region side that faces the collector cold metal contact 20, and its effect is to reduce the metal-semiconductor interface barrier. This region is formed by techniques analogous to those employed to form region 15. Other embodiments of the present invention comprise only region 15, and still other embodiments of the present invention comprise only region 17. As indicated above, the presence of at least one of regions 15 and 17 in embodiments of the present invention, including compensated and uncompensated embodiments, increases their operating temperatures.

The test apparatus included a cartridge heater rated at 400 W in a massive silverized copper block, and a water cooled cold plate (silverized copper) mounted on a micrometric linear stage. The electric leads were massive flexible copper strands ($<10^{-4}$ ohms). The temperature was controlled with Omega RTD's with a Keithly 2001 display. A custom made resistor bank was provided for loads from 10^{-4} ohms and higher. The voltage was measured with 0.01% accuracy, and the current with 1% accuracy. The samples were installed on a hot plate and compressed with the cold plate on a linear positioning stage. Argon gas was introduced between the plates to prevent oxidation of the materials at elevated temperatures. The hot side was thermally insulated from the mounting plate and ambient air.

Figure 37 illustrates an example output I vs. V curve for a single sample indicated by line 42 and a stack of three samples indicated by line 44 for an emitter temperature of 200°C. At the point of maximum extracted power, the output difference is less than 20% when the decrease in the heat flow is at least three times. This means that the efficiency in a stack configuration increases dramatically. Furthermore, each interface introduces thermal resistance due to the non-ideal contact and the phonon mismatch effect. The minimal numbers for phonon mismatch are around 4% (See Swartz, E.T., *Thermal Boundary Resistance*, Vol. 61, No. 3 (July 1989), which is incorporated herein by reference). Each sample introduces two additional boundaries.

Replacing the sample orientation in a stack, such as the emitter layer on the cold side, reduces the output in a stack of 5 samples by approximately 5 times at 200°C, and approximately 2 times at 300°C, compared with a stack built correctly. At 300°C and recalculated on the basis of InSb thermal conductivity and electric output, in some instances the efficiency was better than 25% of ideal Carnot cycle with an output power density of 3-8 W/cm^2.

7. Additional Examples

This section describes testing device characteristics, sample preparation techniques, and more specific results regarding embodiments that contain InSb and/or an Hg-Cd-Te-based material.

5

a. Test Apparatus and Sample Preparation.

Testing devices were designed on the basis of standard mechanical parts for laser applications, including a Coherent® stainless steel bread board. Micrometric linear stage and laser optical stands allowed for 100 mm of vertical linear travel.

The hot side was mounted with a Macor ceramic ring on the linear stage and
10 consisted of a massive copper block with a 400 W Ogden Scientific cartridge heater. The copper block was thermally insulated with porous ZrO_2 ceramics and fiberglass fabric. Interchangeable copper rods made of oxygen-free copper that had a 2-micron coating of silver were used to deliver heat to the sample. Each rod had at least two holes configured for receiving temperature sensors. By measuring temperature at two points along the rod
15 and knowing the thermal conductivity and cross-section of the rod, the heat flow to the sample was determined.

A silver coated water-cooled cold plate was mounted on the top of the optical stand with a Newport three axis "Ball and Socket" stage, which allowed the parallel alignment of the cold and hot plates.

20 The electric current lead comprised silver coated braided copper wires having a resistance of about 10^{-4} ohm. Load resistors in the range of about 10^{-5} ohm to about 10^{-1} ohm were made of copper and stainless steel and were connected to the current leads by massive bolts.

Power to the heater was supplied by a Xantrex 300-3.5 DC power supply.
25 Voltage across the load and sample resistance were measured with a HP34420A NIST-traceable nanovolt/microohmeter in a 4-wire configuration. Keithley 2001 multimeters were used as readouts for Omega thermocouples and RTD temperature sensors. Electric current was measured by an Amprobe® A-1000 transducer. Load and leads resistance allowed independent current determination. On all measured parameters except currents
30 below 1A, the accuracy was better than 1%.

To prevent oxidation of the sample and contacts at elevated temperatures, argon gas was introduced between the hot and cold plates using a Capton foil skirt.

Material for the sample preparation comprised InSb wafers (WaferTech, U.K.) of about 2" in diameter and 500μ in thickness. The wafers were polished to about 20 Å
35 RMS (root mean square) on both sides. Standard dopant (Te) concentration was about 10^{18} cm^{-3}. The emitter layer was deposited by magnetron sputtering. An InSb target

doped with $3x10^{19}cm^{-3}$ Te was also used. The emitter layer thickness was in the range from about 400 Å to about 15000 Å. Emitter thickness in embodiments of the present invention was at least about 400 Å. Furthermore, principles in the context of this invention do not impose any limitation to the emitter thickness and therefore
5 embodiments of this invention are not limited by constraints in an upper bound for such thickness.

To create a compensation layer, about 10^{18} cm^{-3} *p*-type impurity was placed in the semiconductor to compensate the already existing *n*-type dopant (Te) at a concentration of about 10^{18} cm^{-3}. Vacancies in InSb form *p*-type carriers with ionization energy of
10 about 60 meV (*see*, *e.g.*, Landolt-Bornstein), which is roughly the same as the ionization energy of Te. The implantation doses were recalculated by using TRIM-91 software to form a compensation layer.

The samples were then cleaned and cleaved to fit the implanter. The samples were implanted with 40keV Ar ions (Core Systems, Inc., Santa Clara, California) at
15 different doses. Each sample was tested in a conversion mode at about 200° C. Test results are shown in Figure 38, together with calculated doses required for the compensated diode. The doses were varied because the dopant concentration in wafers was known to about 10% accuracy. An implantation dose of zero in Fig. 38 corresponds to a non-compensated sample, and implantation doses greater than zero in Fig. 38 refer
20 to compensated samples. As shown in Fig. 38, comparison of the maximum efficiency for the compensated samples shown therein with the efficiency of the non-compensated sample reveals that the compensation layer leads to about 80% performance improvement. For comparison, Fig. 38 also shows the computed efficiency that is predicted at a given implantation dose.

25 The range for Ar^+ at 40 keV in InSb is approximately 400 Å, which is sufficient for creating a compensation layer. A 400 Å layer is prone to fast diffusion loss of vacancies at elevated temperatures. To avoid such diffusion loss, He ion implantation is performed in other embodiments. The He ion layer thickness in these embodiments is of the order of a few microns, which increases the effective life of the implantation
30 layer. For example, the estimated diffusion half life of vacancies in InSb at 1 micron thickness is approximately 1 year at 200°C. Because the compensation layer is located on the cold side of embodiments of this invention, diffusion problems are typically avoided when the compensation layer is a few microns thick. Computed ion ranges and vacancy formation for ^4He ions in InSb are shown in Figs. 39-40.

b. Embodiments with $Hg_{1-x}Cd_xTe$

$Hg_{1-x}Cd_xTe$ semiconductors (herein referred to as "MCT") have very good thermionic figure-of-merit values when $0.08 \leq x \leq 0.15$, where the upper and lower bounds are given approximately. A preferred value of x is about 0.14. Embodiments of 5 this invention comprised a 500 micron thick $Hg_{0.86}Cd_{0.14}Te$ wafer (Lockheed Martin IR Imaging Systems). MCT reacts with various substrates, creating heavily doped donor (reacting with metals such as In, Fe, Ga and Al) or acceptor (reacting with metals such as Ag, Au, and Bi) layers, with the reaction rate depending on the material and temperature. *See*, P. Caper, *Properties of Narrow Gap Cadmium-based Compounds*, 10 INSPEC, 1994, which is incorporated herein by reference.

The reactivity of MCT allows to build n^*/n emitter layers more easily than with InSb because InSb is less reactive and requires the implementation of a more complex technique for creating an n^* region. Furthermore, InSb is limited to dopant concentrations of about 2-3x10^{19} cm^{-3}.

15 The performance of embodiments of the present invention shows that substrates that form donor impurities are preferred because they generate higher current densities. As shown in Fig. 41, a thermoelectric response without a carrier injection layer generates a current density that exhibits little or no change with respect to temperature. For example, copper forms an acceptor impurity and should not form an n^* region. In 20 contrast, substrates such as Al, In and Ga form n-type impurities in MCT and they create electron-injecting n^* regions. Figure 41 shows electric current density as a function of temperature for $Hg_{0.86}Cd_{0.14}Te$ samples, one of them with a Cu emitter layer and another with an In-Ga emitter layer with substrate composition $In_{0.75}Ga_{0.25}$. Contact resistance was monitored in both cases to ensure that oxide layers do not play a significant role in 25 the observed results. In particular, it was found that In-Ga makes a slightly better contact than copper (about 92 mΩ for In-Ga compared to about 103 mΩ for copper). As shown in Fig. 41, the electric current density as a function of temperature for the sample with copper flattens out. The MCT sample was allowed to cool down and a layer of In-Ga about 20-50 micron thick was placed on top of the copper substrate. As shown in Fig. 30 41, the electric current density exhibited a change with temperature that was similar to that exhibited by the sample with copper only at temperatures up to about 70°C. The same figure shows that above this point the electric current density clearly increased with temperature. This is attributed to the acceptor-type impurity being swamped by n-type impurity, thus causing the sample to exhibit a carrier injection mode with many times 35 higher current output. Output voltage in both cases was approximately the same, from

about 290 to about 350 μV/K, and is consistent with the known thermoelectric Zeebeck coefficient for MCT.

Different donor materials lead to different electric current densities. Figure 42 shows the electric current density as a function of temperature for two $Hg_{0.86}Cd_{0.14}Te$ samples, one of them with an Al substrate and the other sample with an In-Ga substrate. A preferred composition of this substrate is embodied by $In_{0.75}Ga_{0.25}$. The In-Ga substrate forms a better emitter than Al because the electric current density as a function of *temperature is consistently higher for the sample with In-Ga over the entire temperature* range. Although not shown in the form of electric current density vs. temperature graphs, In forms a better emitter than Ga, particularly with pure In substrate. Substrates such as Al, In and Ga are examples of substrates that form *n*-type impurities in MCT that create electron injecting *n** regions.

Figure 43 shows the absolute efficiency exhibited by an embodiment of a MCT converter according to the present invention in which the *n** emitter layer was formed by reacting MCT with $In_{0.75}G_{0.25}$ eutectic. Absolute efficiency is defined as the ratio of an electric power output to the heat flow through the sample. The same data shown in Fig. 43 was recalculated in terms of a percentage of an ideal Carnot cycle efficiency, which are shown in Fig. 44. Ideal Carnot cycle efficiency η_c is defined as $\eta_c = (T_{hot} - T_{cold}) / T_{hot}$. It is accepted that more than 30% of an ideal Carnot cycle efficiency is beyond the capabilities of any conventional thermoelectric device, and that conventional thermoelectric devices can hardly reach 20% of an ideal Carnot cycle efficiency. In contrast, Fig. 44 shows that embodiments of the present invention consistently generate over 20% of an ideal Carnot cycle efficiency in the temperature range from about 100°C to about 175°C with $T_{cold} = 20.5°C$, and that the efficiency is over 30% of an ideal Carnot cycle efficiency at temperatures from about 150°C to about 160°C.

Declining converter performance beyond 150-160°C could be attributed to emitter layer dissolution and/or injected carrier recombination. To avoid this declining converter performance, embodiments of the present invention comprise a diffusion barrier. An ytterbium layer of up to about 10 Å is an example of such diffusion barrier. A thickness of up to about 10 Å is preferred because such metal layer does not significantly affect electron transport properties. For additional ways to make diffusion barriers, *see, e.g.*, A. Raisanen *et al.*, in Properties of II-VI Semiconductors, MRS Society Symposium Proceedings, vol. 161, pp. 297-302, 1990, which is incorporated herein by reference.

c. **Embodiments with a InSb/$Hg_{1-x}Cd_xTe$ Sandwich.**

As shown above, embodiments of this invention that comprise stacked InSb plates with an emitter on a hot side configuration, display a significantly enhanced efficiency. Efficiency for these types of embodiments was determined as follows.

5 InSb and MCT exhibit best performances at different temperatures: from about 300°C to about 350°C for InSb and about 150°C for MCT. By taking into consideration these different temperatures, embodiments of converters according to this invention are optimized for both materials.

The small thermal conductivity of MCT makes the direct measurement of heat 10 flow difficult, especially when the measurements have to be taken with small samples. Furthermore, the dimensions of some of the samples used in embodiments of the present invention were at most a few square millimeters and, because of these reduced dimensions, were not suitable for contact temperature measurements with available temperature sensors. In addition, the small size of these samples did not permit the use 15 of standard IR imaging cameras because of the limited spacial resolution of such IR imaging cameras. A methodology that relies on custom optics IR cameras avoids this problem.

Another methodology, which was adopted in these experiments, implies the following assumptions. Plates with the same thickness exhibit the same heat flow with 20 substantially no heat loss. The total temperature drop across the stack is written as $\Delta T = \Delta T_1 + \Delta T_2$, where ΔT_1 is the temperature drop across the first plate and ΔT_2 is the temperature drop across second plate. The temperature-dependent thermal conductivities of InSb and MCT are, respectively, λ_1 (T) and λ_2 (T). The following system of equations is set forth with these variables:

25

$$-\lambda_1(T)\,\Delta T_1 = -\lambda_2(T)\,\Delta T_2$$

$$\Delta T = \Delta T_1 + \Delta T_2$$

ΔT can be measured as a temperature difference between the cold and the hot plates, and the first equation can be iterated using ΔT_1, λ_1 (T) and λ_2 (T) values. The heat flow 30 and the temperature drop across each plate are estimated according to this iterative procedure. As indicated above, the converter efficiency is computed by taking the ratio of the electric power output to the heat flow through the device. The thickness of the InSb plate was adjusted to vary the converter operating temperature range from less than 150°C to more than 300°C with substantially the same fraction of Carnot cycle efficiency 35 at over 30%. Direct measurements with infrared imaging equipment showed slightly lower heat flow through the converter, probably due to non-ideal contacts, resulting in

3%-4% higher efficiency. Maximum observed efficiency in embodiments of this invention exceeds 40% of an ideal Carnot cycle. In contrast, conventional energy converters available at present typically exhibit a fraction of Carnot cycle efficiency of about 16% in a narrow temperature range.

5 Figure 45 shows the efficiency of an embodiment of a sandwich converter according to the present invention. An about 1-mm thick InSb plate was used in this embodiment and the dopant (Te) concentration was about 10^{18} cm^{-3}. The emitter layer was about 2000 Å and it comprised a sputtered InSb layer with about $3x10^{19}$ cm^{-3} Te. The plate was coated with a layer containing In-Ga. A preferred composition of this In-
10 Ga material is embodied by $In_{0.75}Ga_{0.25}$. The thickness of this layer was from about 30 microns to about 50 microns. A second plate was made of $Hg_{1-x}Cd_xTe$, with x preferably satisfying $0.08 \leq x \leq 0.15$, with the upper and lower bounds given approximately. A more preferred form of this compound has an approximate stoichiometry given by $Hg_{0.86}Cd_{0.14}Te$, with a thickness of about 0.51 mm. The average stack cross section was
15 about 1.70x1.52 mm^2. The fraction of an ideal Carnot cycle efficiency as a function of the hot plate temperature for this embodiment is shown in Fig. 46. T_{cold} regarding Fig. 45-46 was 20°C. As shown in Fig. 46, the percentage of an ideal Carnot cycle efficiency for this embodiment at maximum performance is about the same as that displayed in Fig. 44, but this embodiment exhibits it at a significantly higher temperature.

20 **d. $Hg_{1-x}Cd_xTe$ Figure of Merit.**

As shown in Table 1, the figure of merit for the HgTe is about 2.5 times better than that for InSb. Addition of Cd to HgTe improves carrier mobility and reduces thermal conductivity. Figure 47 shows the normalized thermionic figure of merit for $Hg_{1-x}Cd_xTe$ relative to that of InSb as a function of x. For x = 0.08, the figure of merit for
25 $Hg_{0.92}Cd_{0.08}Te$ is about 0.0065, which is better than the figure of merit for HgTe by a factor of about 2. In other embodiments of this invention, the figure of merit is envisaged to be as low as about 0.001.

It was also found in the context of this invention that preferred embodiments of $Hg_{1-x}Cd_xTe$ have x-values in the range from about 0.08 to about 0.15 and that it is in
30 this region that this material exhibits the highest value for its thermionic figure of merit while the material still exhibits semiconductor properties. This supports the relationship between the *n** emitter layer and the gap and the compensation layer and the gap that has been described hereinabove.

8. Refrigeration Embodiments

35 The main components of a thermionic converter 50 for providing refrigeration (see Figures 48 and 49) are essentially the same as those of a thermal diode 10 for

converting heat to electricity, as set forth above (see Figures 1 and 19). Accordingly, the terms "solid state thermionic converter of thermal energy" generically refer herein to embodiments of converters of thermal energy into electricity according to this invention, and to refrigeration embodiments according to this invention.

5 Figure 48 illustrates the uncompensated thermal diode and Figure 49 the compensated thermal diode. The essential difference between the heat to electricity and refrigeration embodiments is that carrier transport is assisted by an external electric field, E_{Ext}, and the n^*-type region 14 is connected to a thermal load that is cooled by heat flow to the first ohmic contact 52 on the n^*-type region 14. The n^*-type region 14 is thermally
10 insulated by means of an insulating material 54. Rather than a heated n^*-type region 14, as is the case in the heat to electricity embodiment, a thermal load is cooled by heat flow, Q_{Load}, to the n^*-type region 14 in the thermal diode 50 illustrated in Figure 48. A gap 16 region is adjacent to the n^*-type region 14, and a second ohmic contact 53 having a recombination collector region 56 is formed between the second ohmic contact 53 and
15 the gap region 16. The gap region 16 may be n-type, p-type or intrinsic. For the case of the compensated thermal diode as shown in Figure 49, a compensated region 19 is on the inside of the metal contact, which is created through the addition of p-type doping that suppresses the electronic return current. The back surface of the second ohmic contact 53 acts as a heat exchanger, and heat flow $Q_{Exchange}$ dissipates the heat from hot electrons.

20 Figure 50 shows the coefficient of performance (CoP, relative to a reversed Carnot cycle) as a function of temperature for compensated diodes as refrigeration embodiments of the present invention. The coefficient-of-performance curves in Figure 50 are labeled with the different gap materials in each embodiment. In addition to the significantly improved coefficients of performance with respect to conventional devices,
25 Figure 50 also shows that embodiments of the present invention are operational at temperatures well below 200 K, in contrast with conventional devices that generally cannot operate at temperatures below about 200 K.

One skilled in the art of heat exchangers recognizes there are many means for accomplishing heat exchange including, but not limited to, air and liquid cooling, or
30 equivalents thereof.

9. Applications

Since energy conversion is the basis of modern civilization, an efficient energy converter has numerous applications, such as existing utility power plants, solar power plants, residential electricity supplies, residential/solar electricity supply, automotive,
35 maritime, solar/maritime, portable electronics, environmental heat pump, refrigeration (cooling, air conditioning, etc.), aerospace, and so forth.

Power plants have a tremendous amount of waste heat with a potential of 300°C and lower. Converting the waste heat at 20-40% of Carnot efficiency by using embodiments of the present invention is expected to give an additional 10-20% overall plant efficiency with equivalent savings on fuel.

5 The proliferation of low-cost energy converters according to the present invention is expected to lower the capital costs of solar concentrator power plants with a higher efficiency than current steam/electricity cycles. Lower operating temperatures will also lower maintenance costs.

Residential electric supplies based on direct heat to electric energy conversion are 10 ideal for remote areas, where it is difficult or inconvenient to install power lines. The heat source may either be in the form of fossil fuel or solar concentrators. Solar concentrators can also be in the form of solar heated water pools, utilizing day/night temperature differences. A few hundred cubic meters of water with a hundred square meters of surface in conjunction with embodiments of the present invention could 15 provide the electricity supply for a house in areas with a temperature differential of about 10°C.

A thermal diode according to the present invention in combination with a conventional engine driving an electric generator and an electric motor would substantially increase mileage.

20 Direct energy conversion has tremendous application in electric cars. One application involves using thermionic devices according to the present invention with operating temperatures up to about 150 to 200°C as overall efficiency boosters. Another application is an automobile with an electric drive and a conventional engine coupled with an electric generator having a converter array according to the present invention as 25 an intermediate radiator.

Automotive and propulsion applications are also applicable to maritime applications. In addition, solar concentrators may be used in a sail-type fashion. A combination of light and inexpensive plastic Fresnel lenses with thermal diode converters according to the present invention may be incorporated into modern rigid wing-type sails, 30 providing for the use of wind and sun energy to propel a boat with about 100-200 W/m^2 of the sail solar component.

Since embodiments of the converter according to the present invention can utilize very small temperature gradients in a self-sustaining mode, a temperature gradient between the heat sinks will be created with asymmetric heat exchange on the surface 35 (e.g., one heat sink can be thermally insulated). Also, the system will run until something malfunctions, cooling the environment and producing electricity. In summary, the

method and apparatus disclosed herein is a significant improvement from the present state of the art of energy conversion.

The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in
5 all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed is:

1. A solid state thermionic converter, comprising:

an emitter having at least a region comprising a first donor having a concentration N_d^*;

a collector; and

5 a gap region between said emitter and said collector in electric and thermal communication with said emitter and said collector, said gap region comprising a semiconductor, said semiconductor comprising a second donor having a concentration N_d, said concentration of said second donor being selected such that the natural logarithm of the ratio N_d^* / N_d is between a numerical value

10 greater than 0 and about 7.

2. A converter as recited in claim 1, further comprising a compensated region disposed between said gap region and said collector, said compensated region being configured to suppress electric current from said collector to said gap region.

3. A converter as recited in claim 1, wherein said natural logarithm of the

15 ratio N_d^* / N_d is in a range between about 3 and about 7.

4. A converter as recited in claim 1, wherein the temperature of said emitter is higher than the temperature of said collector when an electric current flows from said emitter to said collector.

5. A converter as recited in claim 1, wherein said emitter comprises a metal.

20 6. A converter as recited in claim 1, wherein said gap region comprises an *n*-type semiconductor.

7. A converter as recited in claim 1, further comprising a recombination region either disposed in electric communication between said gap region and said collector or comprising a portion of said collector in electric communication with said

25 gap region.

8. A converter as recited in claim 1, wherein said emitter comprises InSb.

9. A converter as recited in claim 1, wherein said emitter comprises InSb doped with Te.

10. A converter as recited in claim 1, wherein said gap region comprises InSb

30 doped with Te at a concentration in the range from about 10^{16} cm^{-3} to about $3 \cdot 10^{19}$ cm^{-3}.

11. A converter as recited in claim 1, wherein said emitter comprises InSb doped with Te at a concentration in the range from about 10^{18} cm^{-3} to about $3 \cdot 10^{19}$ cm^{-3}.

12. A converter as recited in claim 1, wherein said gap region comprises InSb doped with Te at a concentration of about 10^{18} cm^{-3}.

35 13. A converter as recited in claim 1, wherein the thickness of said emitter is at least about 400 Å.

14. A converter as recited in claim 1, wherein said gap region comprises a semiconductor whose dimensionless normalized conductivity χ is within the range from about 1 to about 0.001.

15. A converter as recited in claim 1, wherein said gap region comprises HgSe.

16. A converter as recited in claim 1, wherein said gap region comprises HgTe.

17. A converter as recited in claim 1, wherein said gap region comprises $Bi_{1-y}Sb_y$, wherein y is within the range from about 0.05 to about 0.2.

18. A converter as recited in claim 1, wherein said gap region comprises Se_zTe_{1-z}, wherein z satisfies $0 \leq z \leq 1$.

19. A converter as recited in claim 1, wherein said gap region comprises $Hg_{1-x}Cd_xTe$, wherein x is within the range from about 0.08 to about 0.2.

20. A converter as recited in claim 1, wherein said gap region comprises $Hg_{1-x}Cd_xTe$, wherein x is about 0.08.

21. A converter as recited in claim 1, wherein said gap region comprises a doped semiconductor with a dopant concentration in the range from about 10^{15} cm^{-3} to about 10^{20} cm^{-3}.

22. A converter as recited in claim 1, wherein said gap region comprises a *p*-type semiconductor.

23. A converter as recited in claim 1, wherein said gap region comprises an intrinsic semiconductor.

24. A converter as recited in claim 1, wherein the energy barrier for electron injection from said emitter to said gap region is in the range from about $4k_BT$ to about $5k_BT$, where k_B is the Boltzman constant and T is the absolute temperature at which the electron injection takes place.

25. A converter as recited in claim 1, wherein said emitter is thermally insulated.

26. A converter as recited in claim 1, further comprising:

a first ohmic contact in electric and thermal communication with said emitter;

a metal-semiconductor-interface-barrier-reduction layer between said first ohmic contact and said emitter; and

a second ohmic contact in electric communication with said collector.

27. A converter as recited in claim 26, wherein said collector is formed on said second ohmic contact.

28. A converter as recited in claim 26, further comprising a thermally conducting layer deposited on at least one of said first and second ohmic contacts.

29. A converter as recited in claim 1, further comprising:

a cold ohmic contact in electric and thermal communication with said gap region, wherein said cold ohmic contact comprises said collector next to said gap region, wherein said collector includes a recombination collector region; and

a compensated region disposed between said gap region and said collector, said compensated region being configured to suppress electric current from said collector to said gap region; and

30. A converter as recited in claim 29, wherein said recombination collector region is formed on said cold ohmic contact.

31. A converter as recited in claim 1, further comprising:

a compensated region such that said gap region is located between said emitter and said compensated region, and wherein said collector is in electric and thermal contact with said compensated region, said compensated region having *p*-type doping such that electric current from said collector to said gap region can be substantially suppressed while allowing thermionic current from said gap region to said collector.

32. A converter as recited in claim 31, wherein the temperature of said emitter is higher than the temperature of said collector when an electric current flows between said emitter and said collector.

33. A solid state thermionic converter comprising a plurality of individual converters arranged in series, wherein each of said individual converters is configured as recited in claim 31.

34. A converter as recited in claim 31, wherein said compensated region is formed by ion implantation into said gap region.

35. A converter as recited in claim 31, wherein said compensated region comprises vacancies created by ion implantation.

36. A converter as recited in claim 31, wherein said emitter is thermally insulated.

37. A solid state thermionic converter of thermal energy, comprising:

an emitter having at least a reaction product of $Hg_{1-x}Cd_xTe$ with a substrate comprising In;

a collector; and

a gap region between said emitter and said collector in electric and thermal communication with said emitter and said collector, said gap region

comprising a semiconductor selected from the group consisting of *n*-type, *p*-type and intrinsic semiconductors.

38. A converter as recited in claim 37, further comprising a compensated region disposed between said gap region and said collector, said compensated region being configured to suppress electric current from said collector to said gap region.

39. A converter as recited in claim 37, wherein said substrate comprises In-Ga.

40. A converter as recited in claim 37, wherein x is within the range from about 0.08 to about 0.25.

41. A converter as recited in claim 37, wherein x is within the range from about 0.08 to about 0.09.

42. A converter as recited in claim 37, wherein said substrate comprises $In_{1-w}Ga_w$, wherein w is within the range from about 0.1 to about 0.3.

43. A converter as recited in claim 37, wherein said emitter is provided with a diffusion barrier.

44. A converter as recited in claim 37, wherein said emitter is provided with a diffusion barrier comprising ytterbium.

45. A converter as recited in claim 37, wherein said emitter is thermally insulated.

46. A solid state thermionic converter of thermal energy, comprising:

a plurality of plates P_i, with $1 \le i \le m$, where m is the total number of said plates, each one of said plates P_i having

an emitter E_i having at least a region comprising a first donor having a concentration N_d^*;

a collector C_i; and

a gap region G_i between said emitter E_i and said collector C_i in electric and thermal communication with said emitter E_i and said collector C_i, said gap region G_i comprising a semiconductor, said semiconductor comprising a second donor having a concentration N_d, said concentration of said second donor being selected such that the natural logarithm of the ratio N_d^* / N_d is between a numerical value greater than 0 and about 7, and such that $1 \le i \le m$;

wherein each plate P_j having an emitter E_{j+1}, a gap region G_{j+1}, and a collector C_{j+1}, so configured is connected in series with a group of an emitter E_j, a gap region G_j, and a collector C_j, for $1 \le j \le (m-1)$, the indexes i and j being integers, and such that collector C_j is in electric communication with emitter E_{j+1} for each j satisfying $1 \le j \le (m-1)$.

47. A converter as recited in claim 46, wherein said natural logarithm of the ratio N_d^* / N_d is in a range from about 3 to about 7.

48. A converter as recited in claim 46, further comprising a compensated region disposed between said gap region G_i and said collector C_i, said compensated region R_i being configured to suppress electric current from said collector to said gap region, wherein each plate P_j having an emitter E_{j+1}, a gap region G_{j+1}, a compensated region R_{j+1}, and a collector C_{j+1}, so configured is connected in series with a group of an emitter E_j, a gap region G_j, a compensated region R_{j+1}, and a collector C_j, for $1 \leq j \leq (m-1)$.

49. A converter as recited in claim 48, wherein emitters E_i and E_j comprise substantially the same materials, collectors C_i and C_j comprise substantially the same materials, and compensated regions R_i and R_j comprise substantially the same materials, for $i \neq j$, and $1 \leq i \leq m$, $1 \leq j \leq m$.

50. A converter as recited in claim 46, such that the temperature of each of said emitter E_i is higher than the temperature of each of said collector C_i when an electric current flows between said emitter E_i and said collector C_i.

51. A converter as recited in claim 46, wherein said first plate P_1 comprises InSb.

52. A converter as recited in claim 46, wherein said first plate P_1 comprises InSb doped with Te.

53. A converter as recited in claim 46, wherein said first plate P_1 comprises InSb doped with Te at a concentration of about 10^{18} cm^{-3}.

54. A converter as recited in claim 46, wherein at least said first plate emitter E_1 comprises InSb doped with Te.

55. A converter as recited in claim 46, wherein at least said first plate emitter E_1 comprises InSb doped with Te at a concentration of about $3 \cdot 10^{19}$ cm^{-3}.

56. A converter as recited in claim 46, wherein said first plate P_1 is coated with a material comprising In-Ga.

57. A converter as recited in claim 46, wherein at least said first plate P_1 is coated with a material having $In_{1-u}Ga_u$, wherein u is in a range from about 0 to about 0.3.

58. A converter as recited in claim 46, wherein at least said first plate P_1 is coated with a material having $In_{1-u}Ga_u$, wherein u is about 0.25.

59. A converter as recited in claim 46, wherein at least one of said plates comprises $Hg_{1-x}Cd_xTe$, with x being in the range from about 0.08 to about 0.2.

60. A converter as recited in claim 46, wherein at least one of said plates comprises $Hg_{1-x}Cd_xTe$, with x being in a range from about 0.08 to about 0.14.

61. A converter as recited in claim 46, wherein said first emitter E_1 is thermally insulated.

62. A method for converting thermal energy into electricity by using a solid state thermionic converter, comprising:

5 electrically coupling a thermionic converter to an external load, said thermionic converter having

an emitter;

a collector; and

a gap region between said emitter and said collector in electric

10 and thermal communication with said emitter and said collector;

and

delivering thermal energy to said emitter of said thermionic converter such that a temperature gradient is established between said emitter and said collector, and an electric potential difference is established between said emitter

15 and said collector when said thermal energy is delivered to said emitter, said thermionic converter converting said thermal energy into electric energy with an efficiency of at least 25% of an ideal Carnot cycle efficiency.

63. The method recited in claim 62, wherein the temperature of said emitter is in a range from about 20°C to about 400°C.

20 64. A method for refrigeration by using a solid state thermionic converter, comprising:

establishing externally an electric potential difference across a thermionic converter having

a thermally insulated emitter having at least a region having a first

25 donor concentration N_d^*;

a collector;

a gap region between said emitter and said collector in electric and thermal communication with said emitter and said collector, said gap region comprising a semiconductor, said semiconductor comprising a

30 second donor having a concentration N_d, said concentration of said second donor being selected such that the natural logarithm of the ratio N_d^* / N_d is between a numerical value greater than 0 and about 7; and

delivering a thermal load to said emitter such that said thermal load is cooled by heat flow as said externally established electric potential difference

35 causes the flow of electric current between said emitter and said collector.

65. A method as recited in claim 64, wherein said natural logarithm of the ratio N_d^* / N_d is in a range between about 3 and bout 7.

66. A method as recited in claim 64, with said thermionic converter further having a compensated region disposed between said gap region and said collector, said
5 compensated region being configured to suppress electric current from said collector to said gap region.

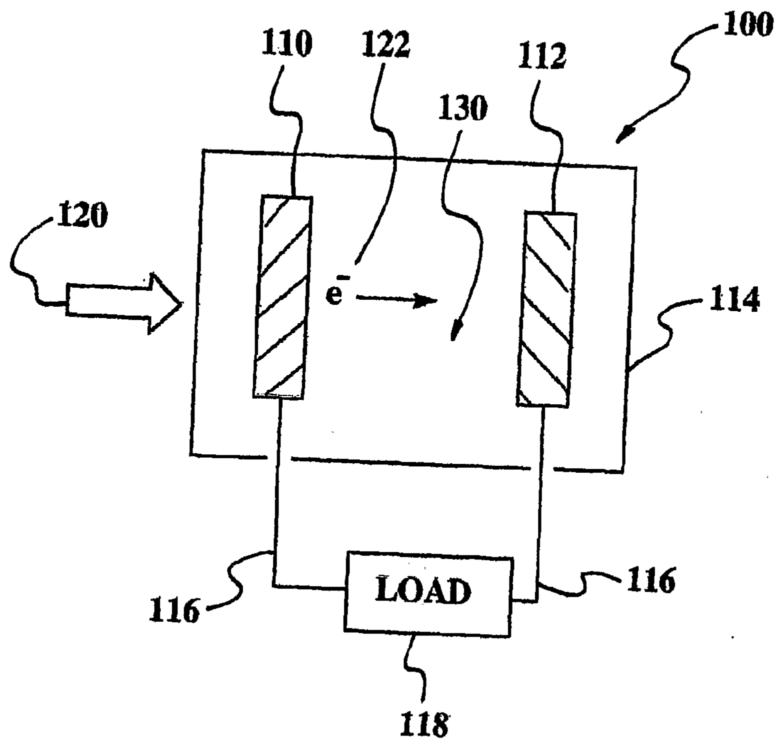


Figure 1
(PRIOR ART)

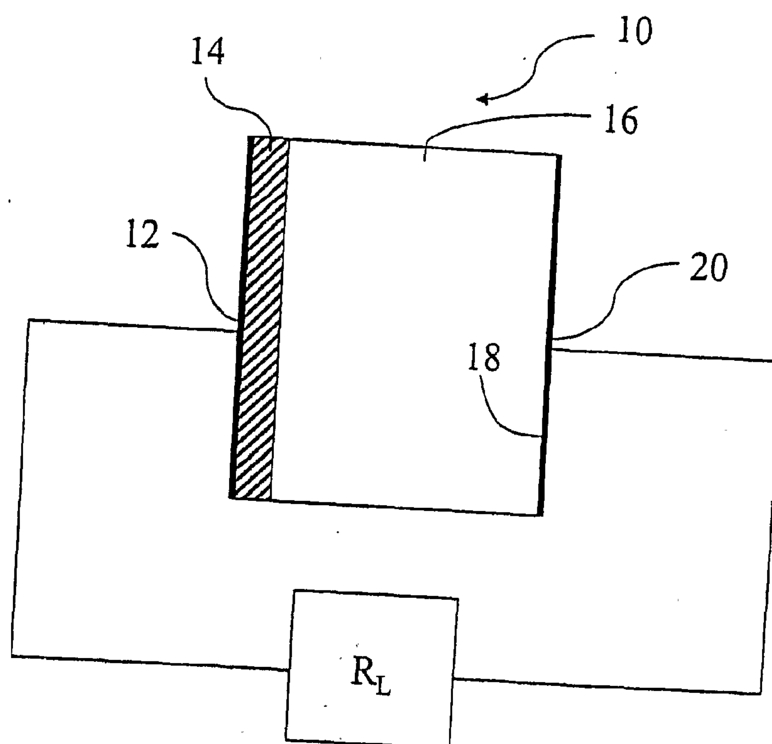


FIG. 2

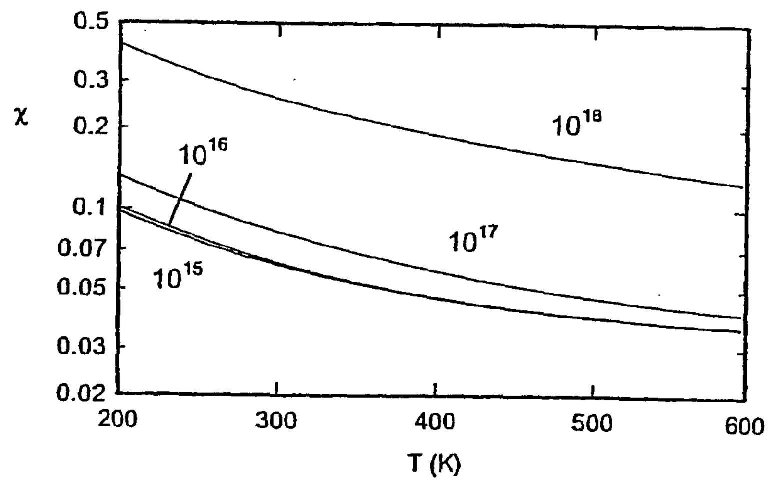


Figure 3

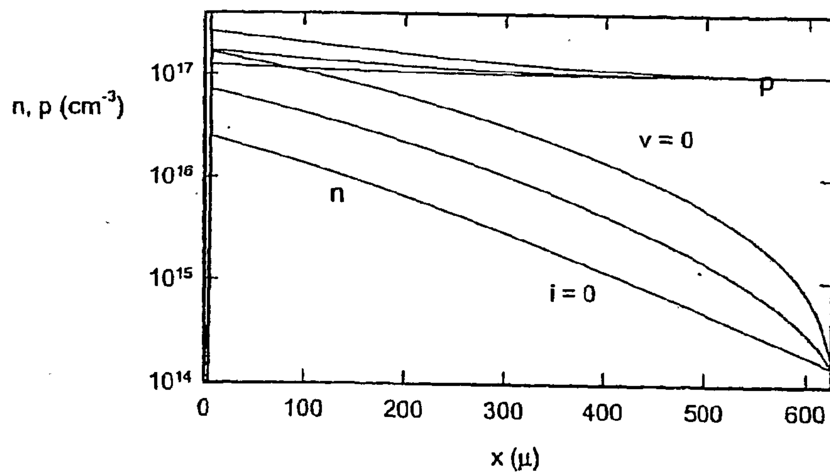


Figure 4

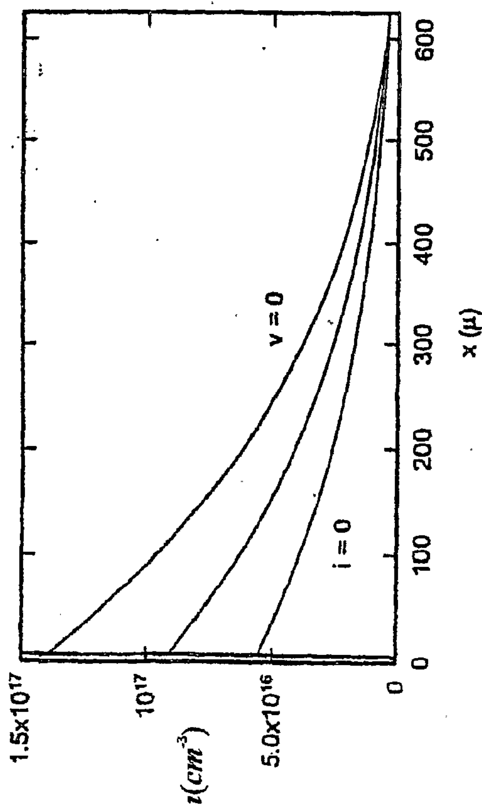


Figure 5A

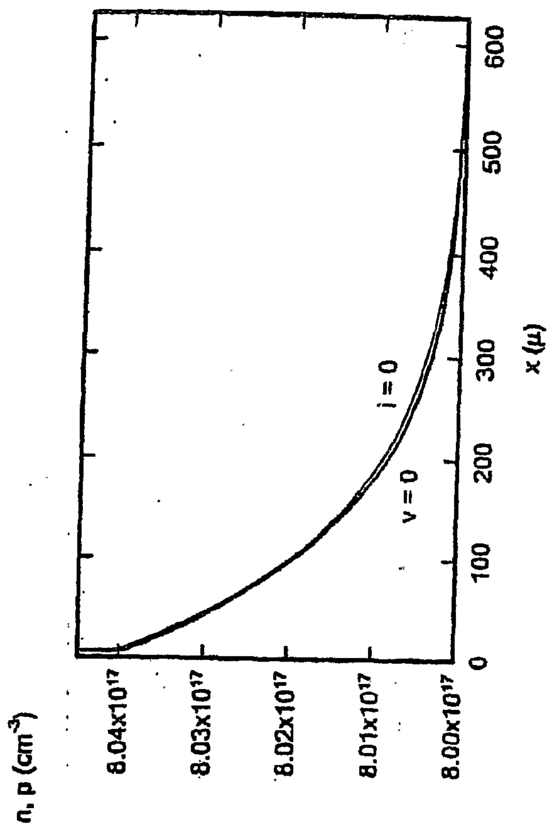
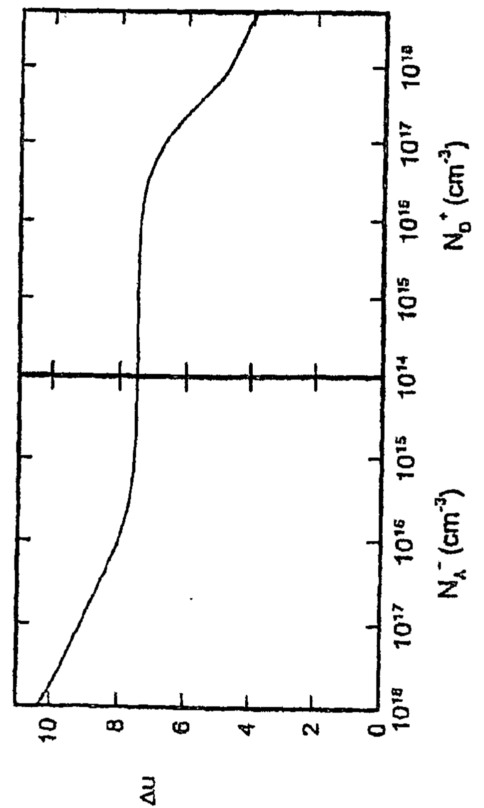
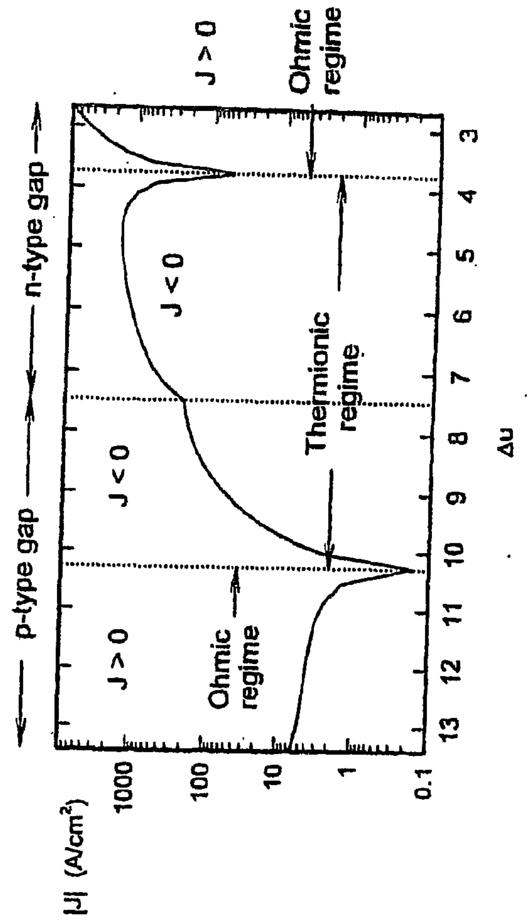


Figure 6





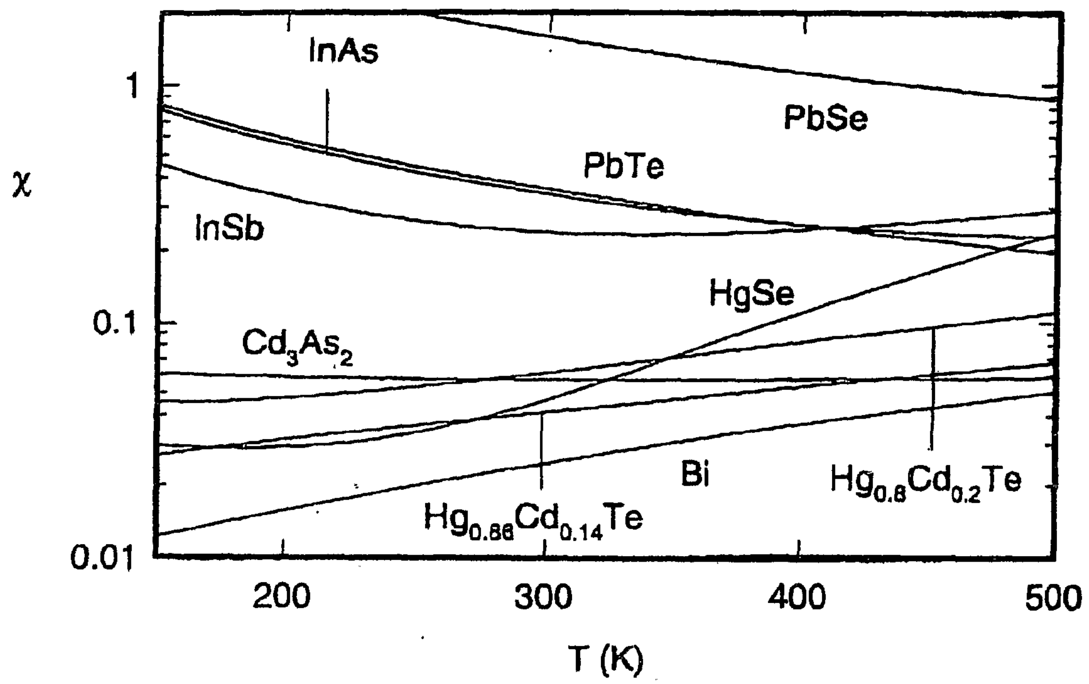


Figure 5B

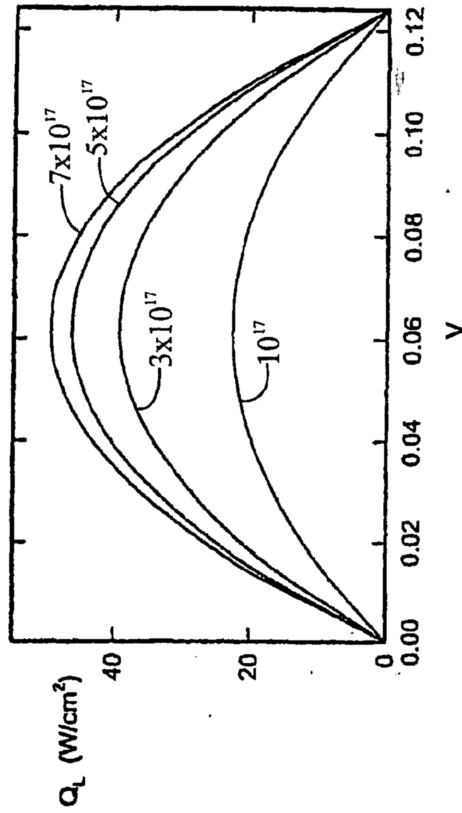


Figure 10

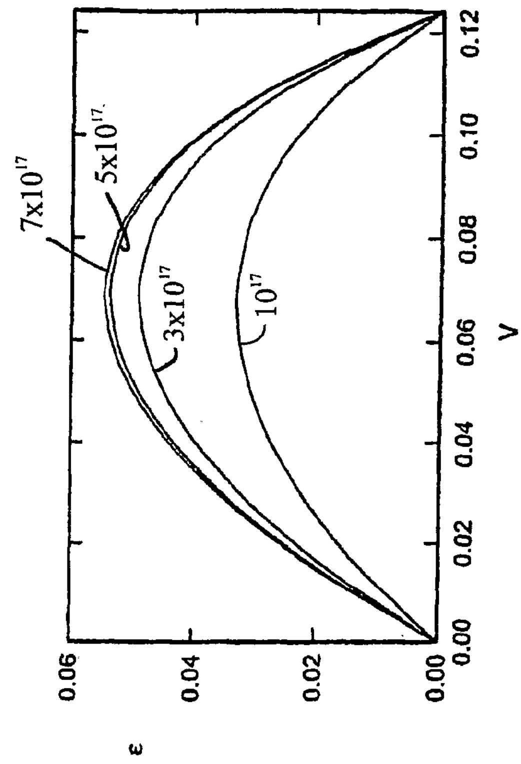
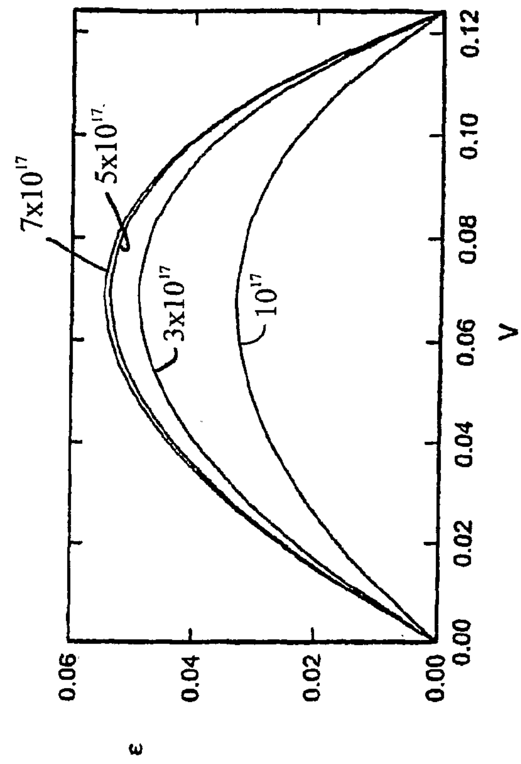


Figure 12



(A/cm^2)

0
500
1000
1500
0.00
0.02
0.04
0.06
0.08
0.10
0.12
V
7 x 10^{17}
5 x 10^{17}
3 x 10^{17}
10^{17}

Figure 9

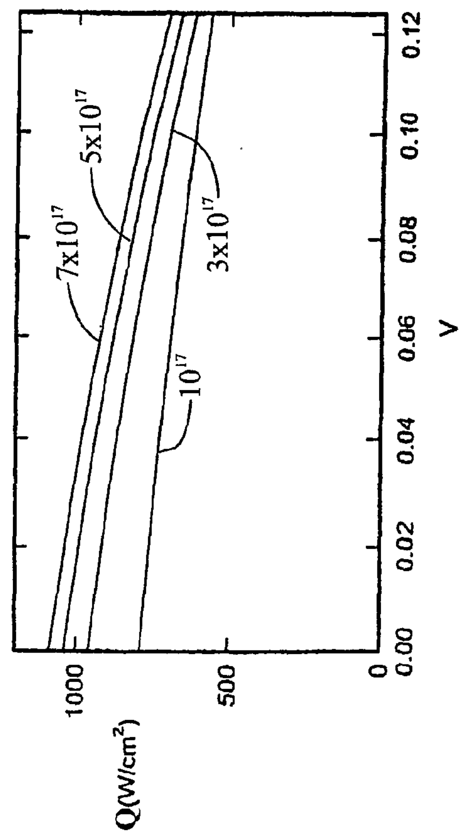


Figure 11

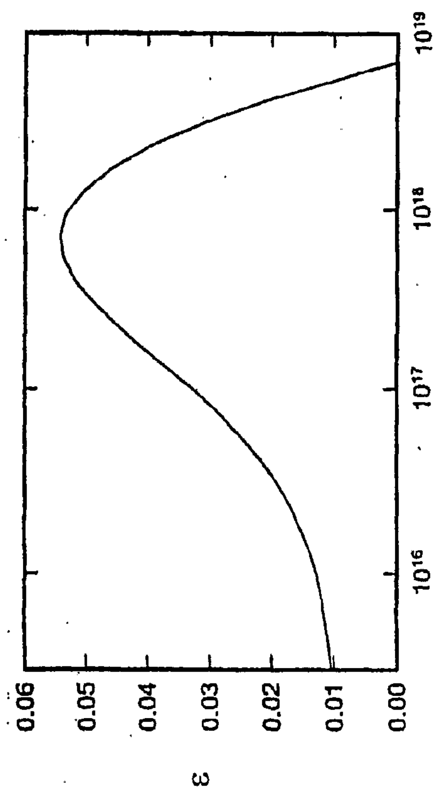


Figure 13

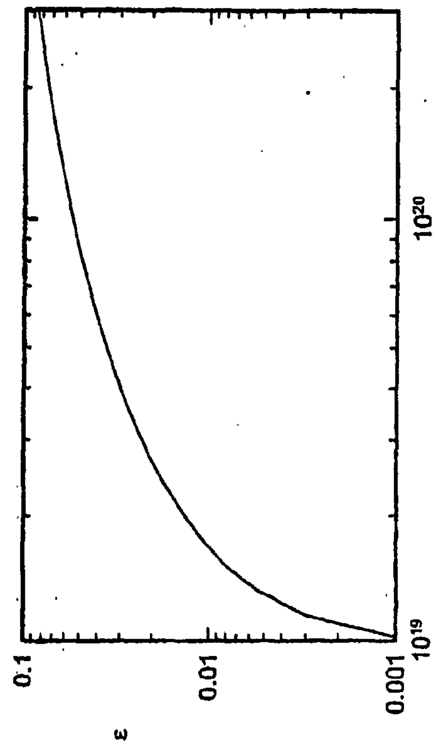


Figure 14

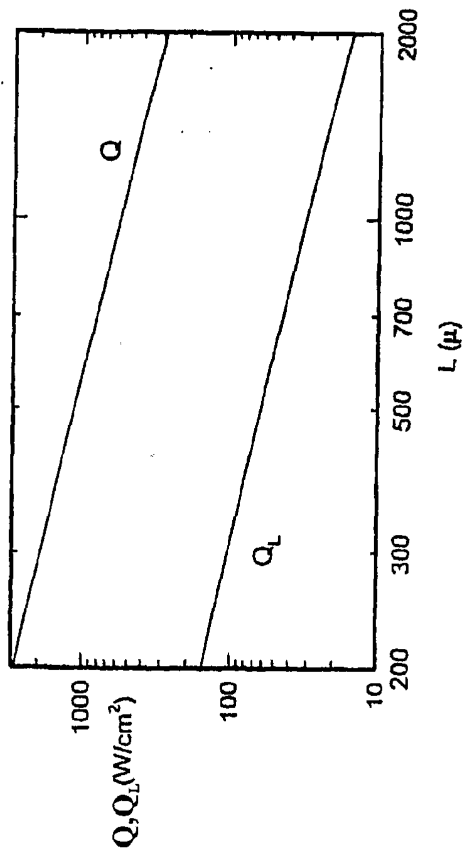


Figure 15

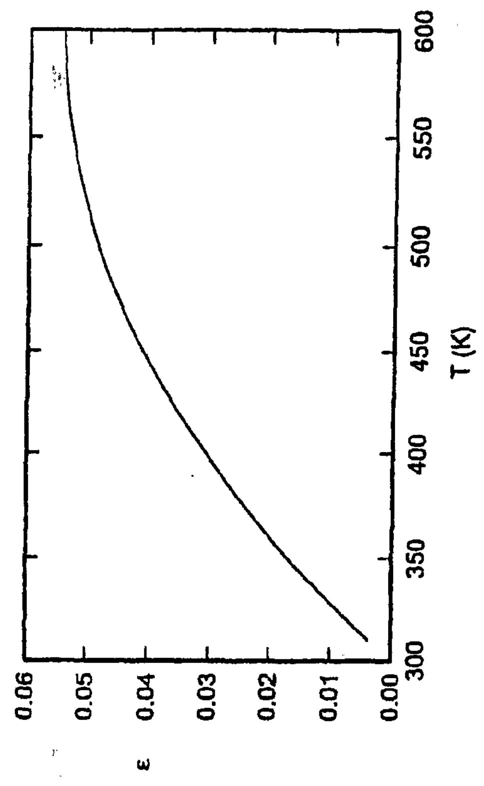


Figure 16

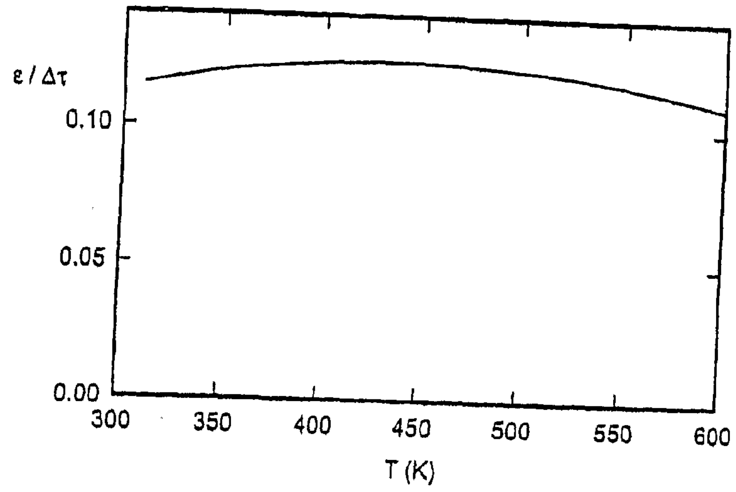


Figure 17

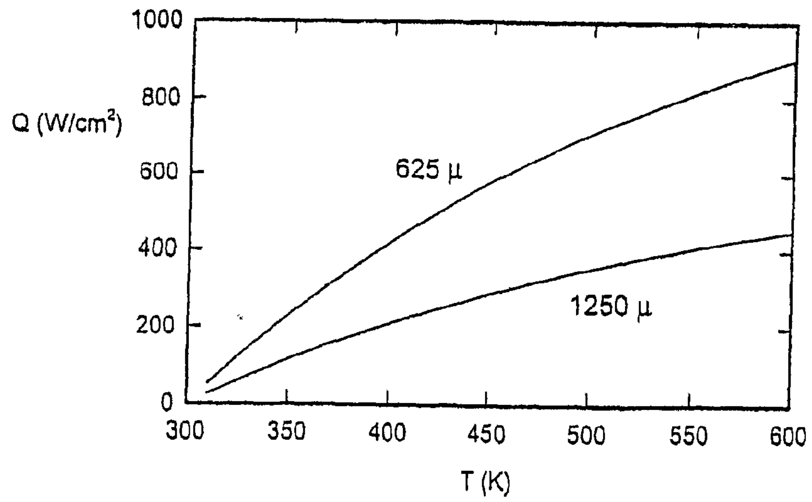


Figure 18

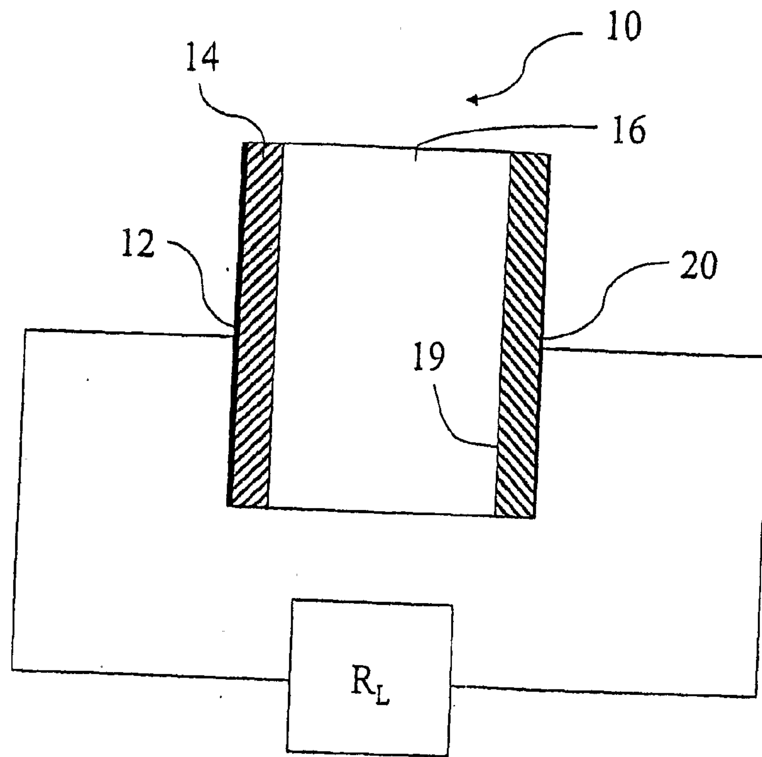


Figure 19

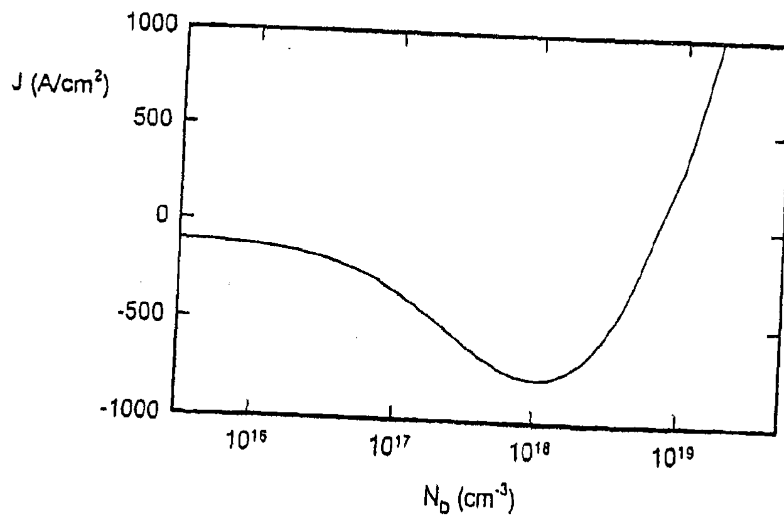


Figure 20

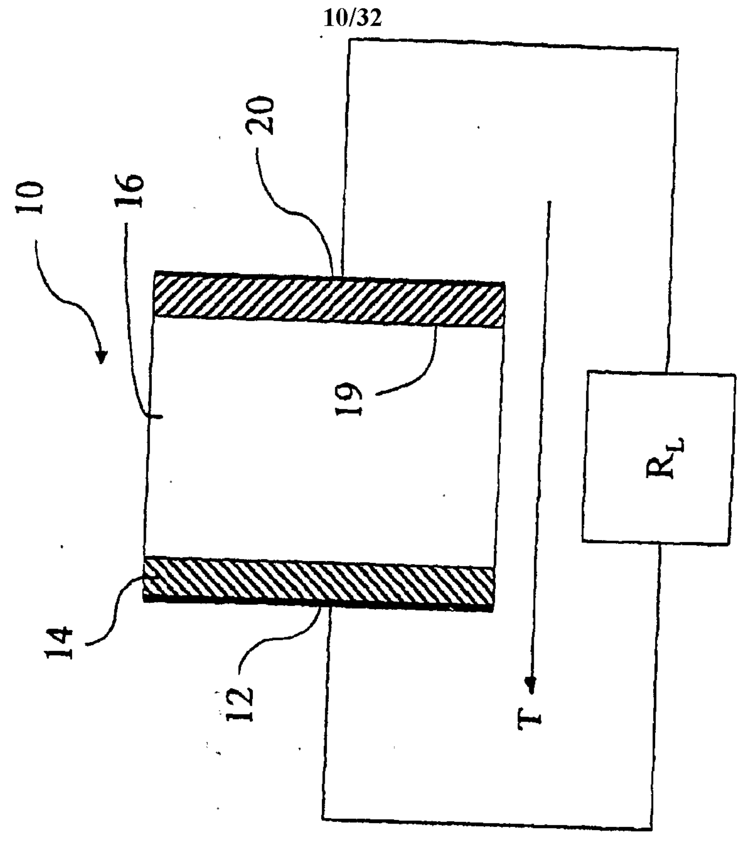


Figure 22

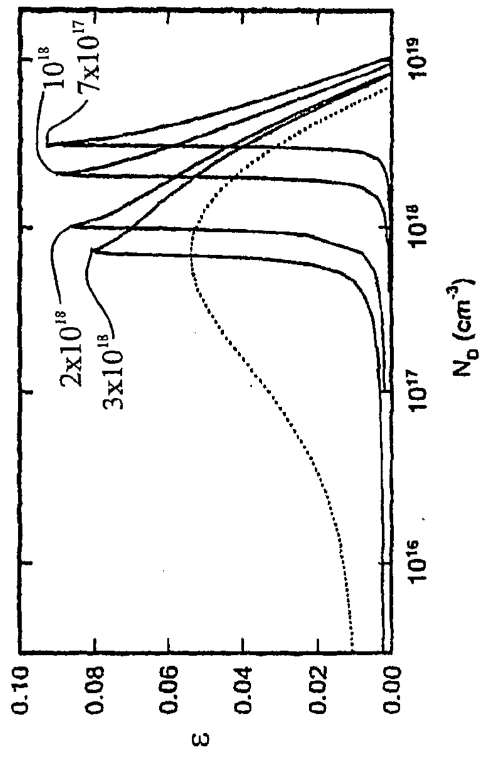


Figure 21

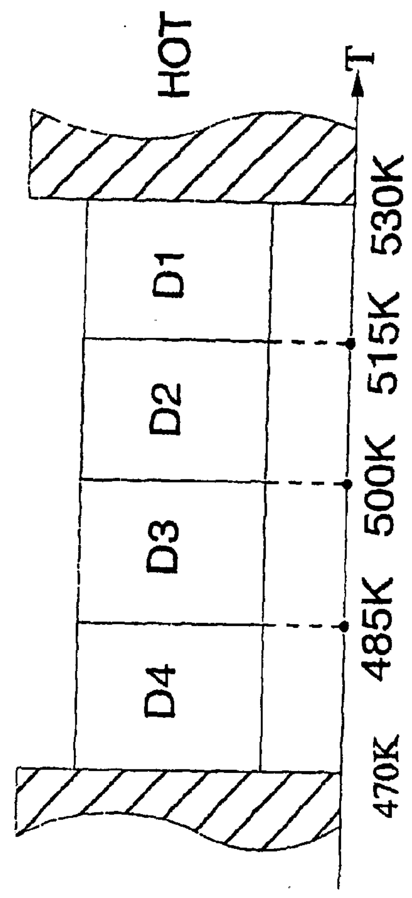


Figure 24

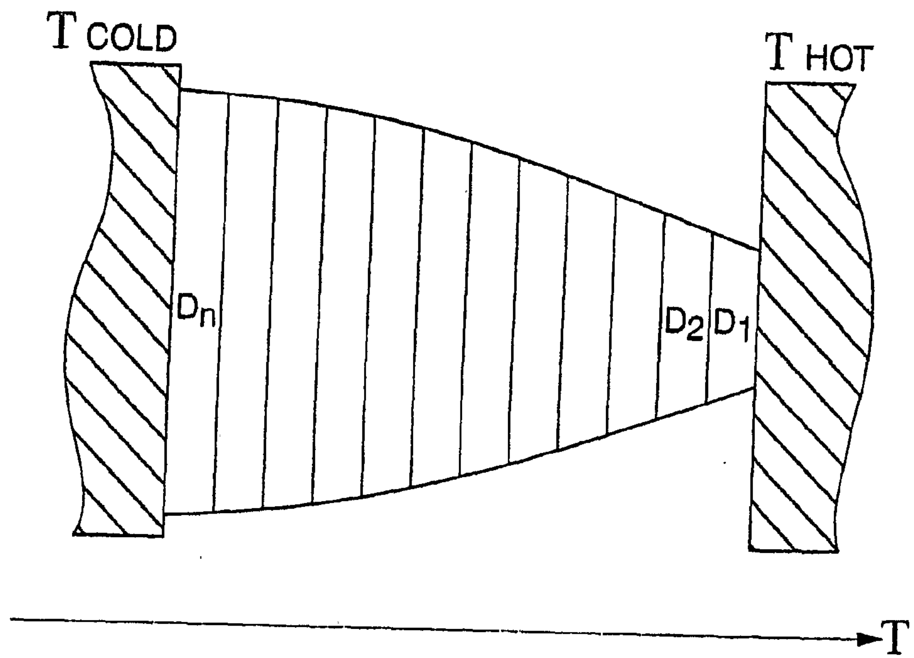


Figure 25

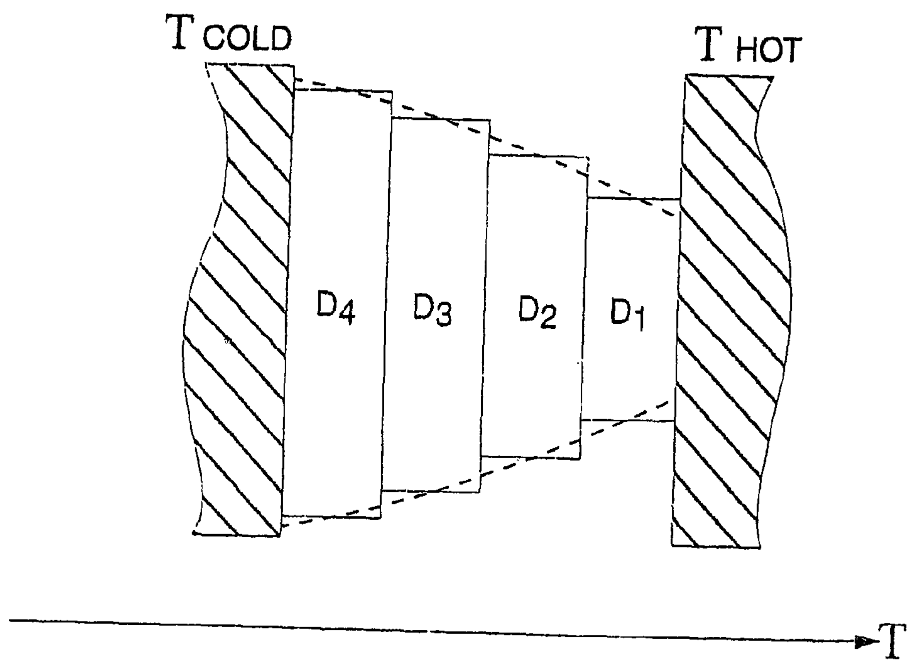


Figure 26

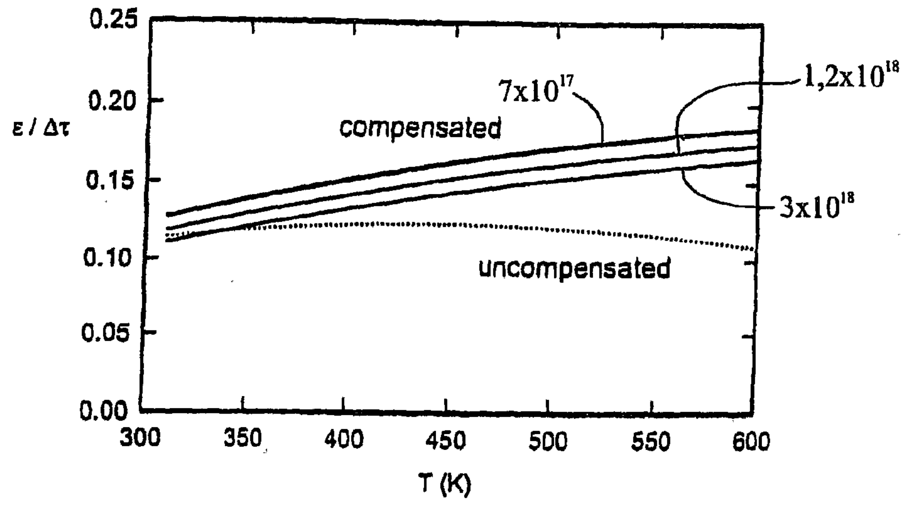


Figure 23A

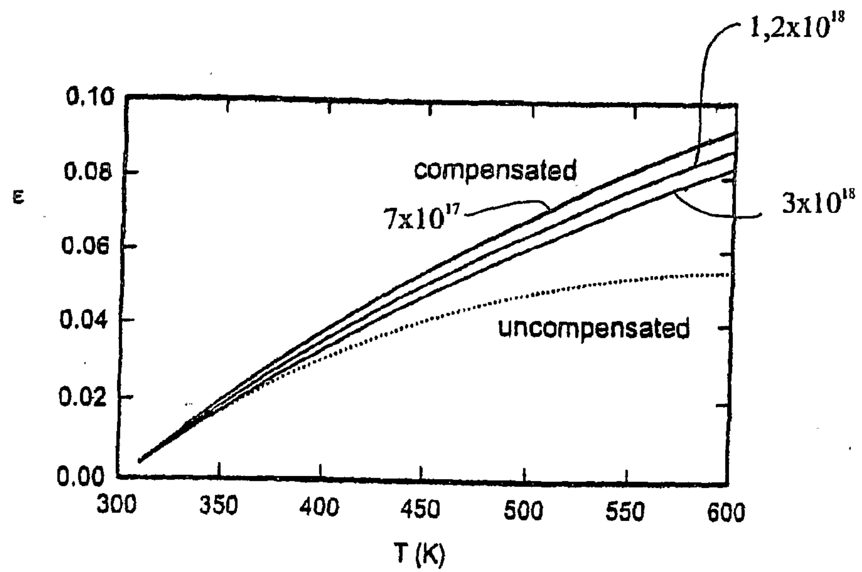


Figure 23B

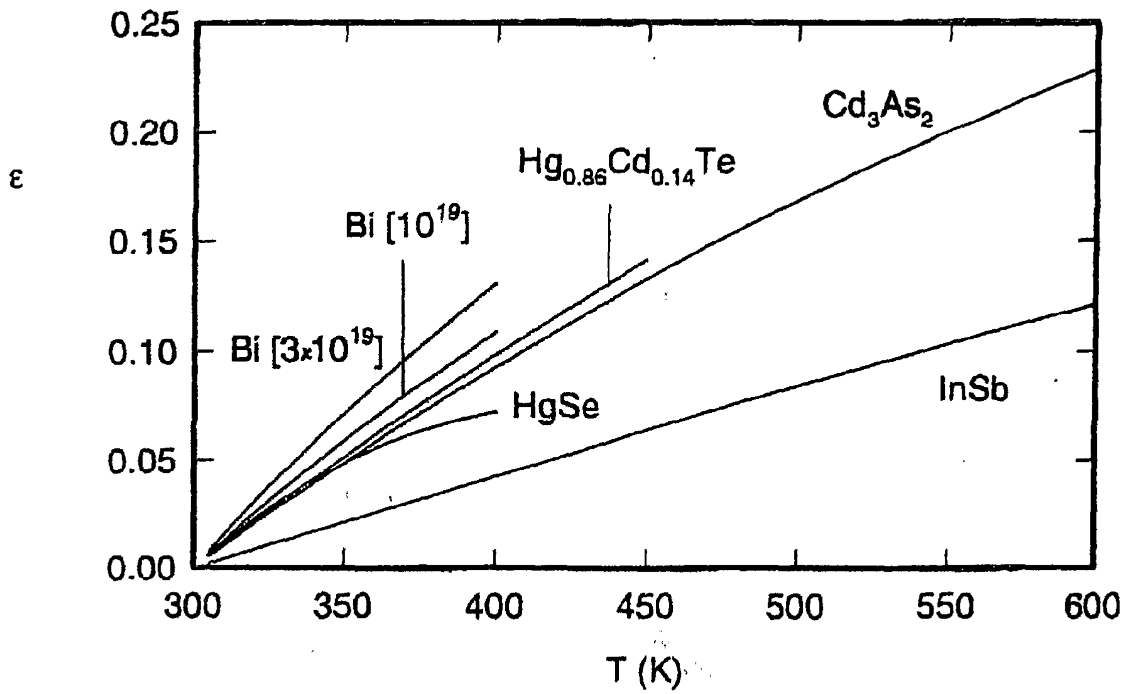


Figure 27A

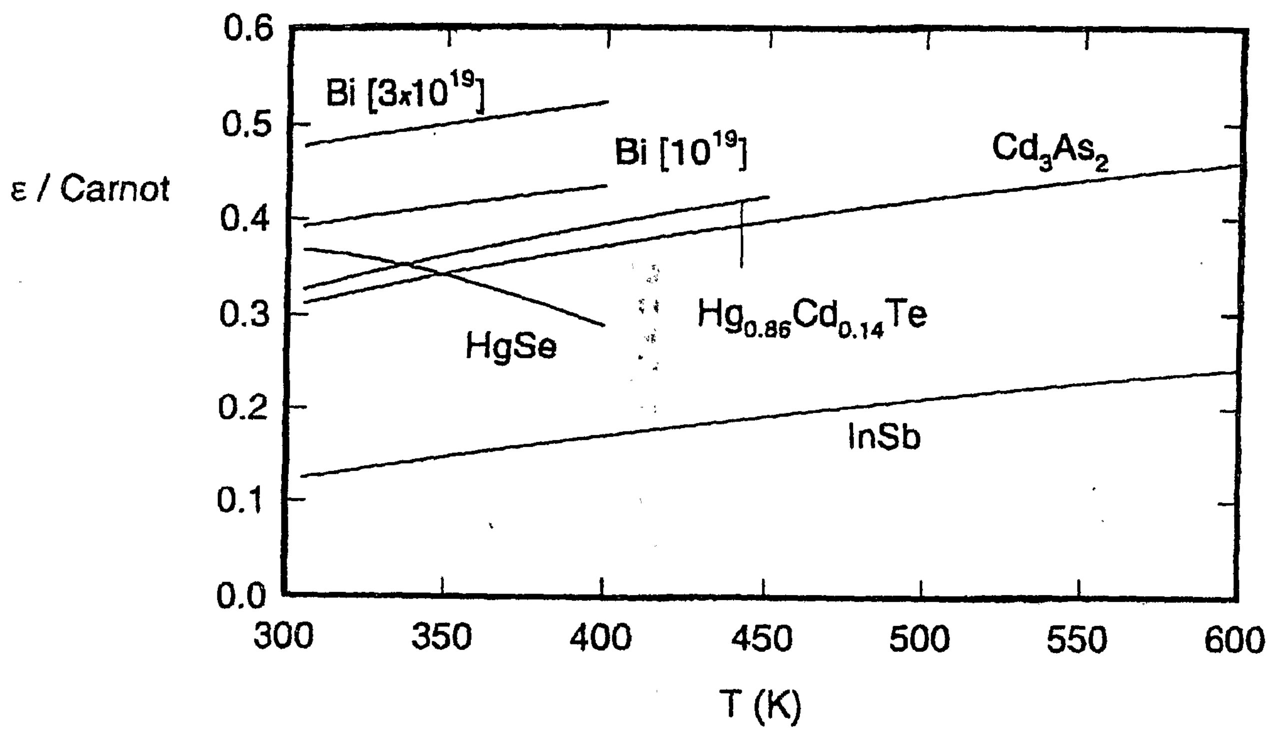


Figure 27B

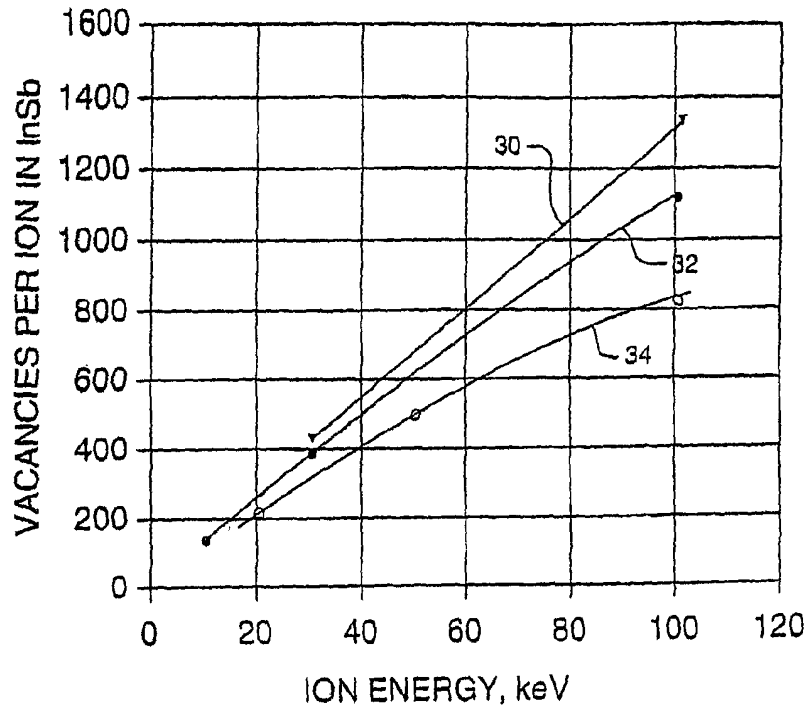


Figure 28

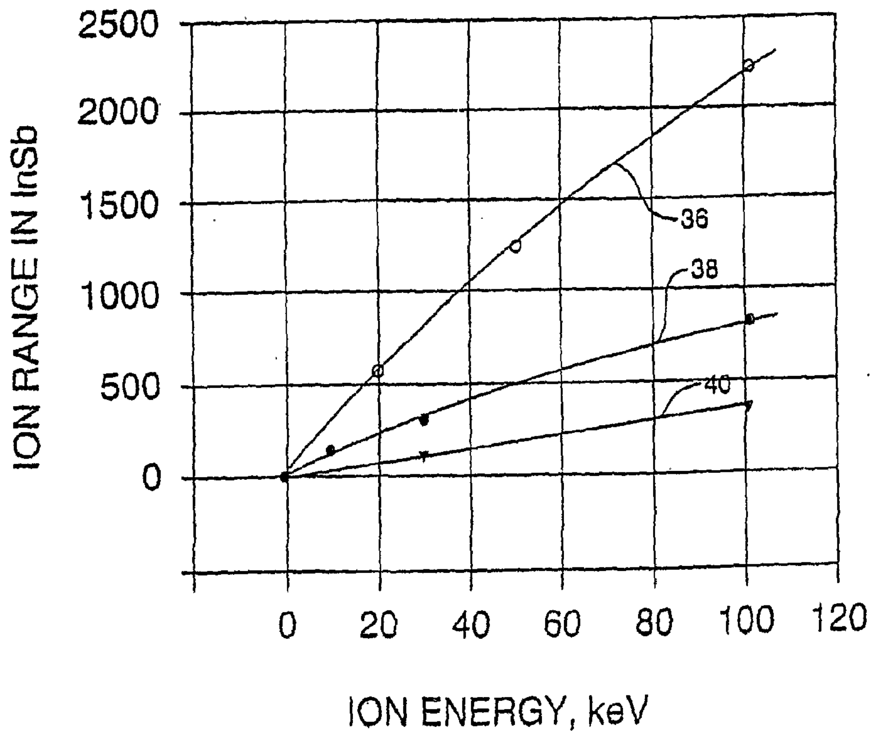


Figure 29

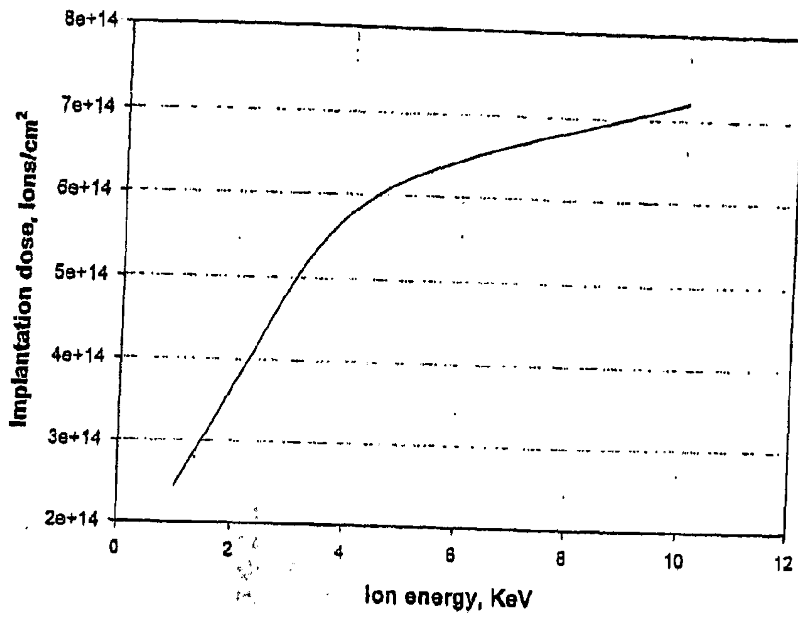


Figure 30

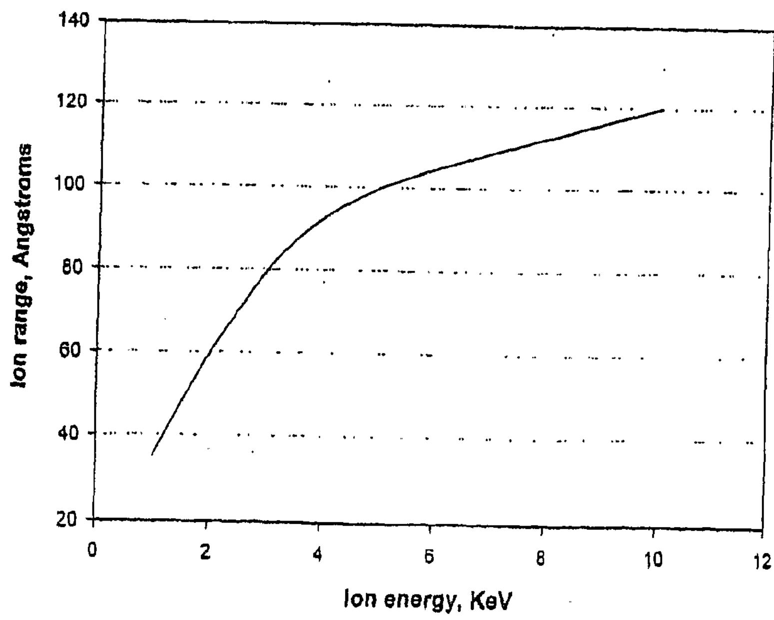


Figure 31

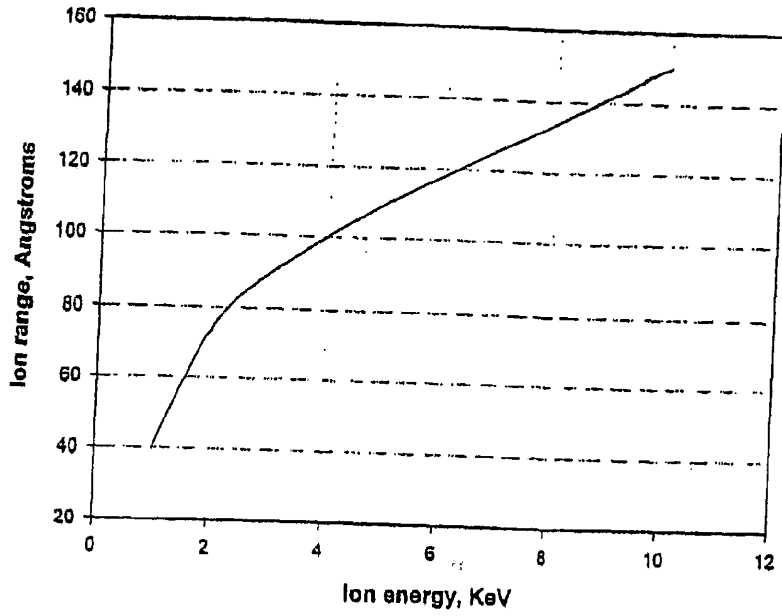


Figure 32

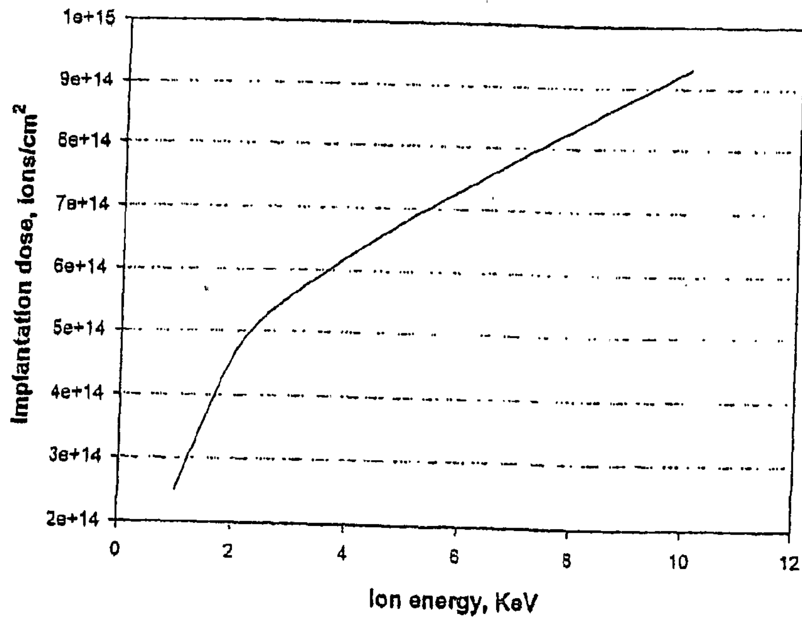


Figure 33

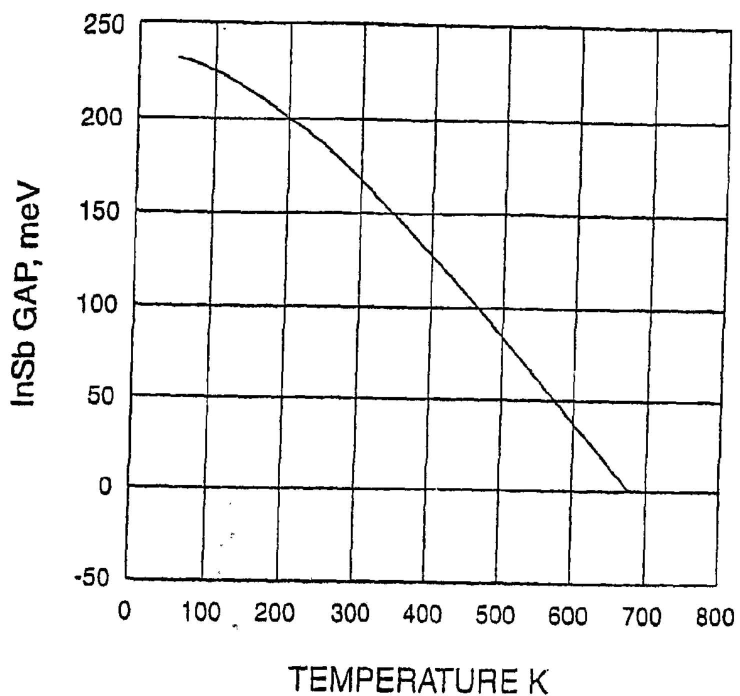


Figure 34

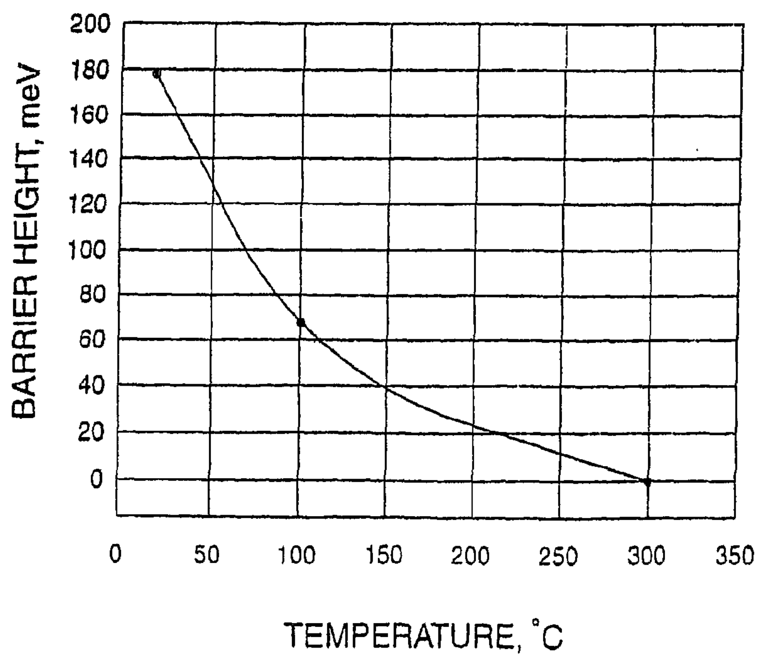


Figure 35

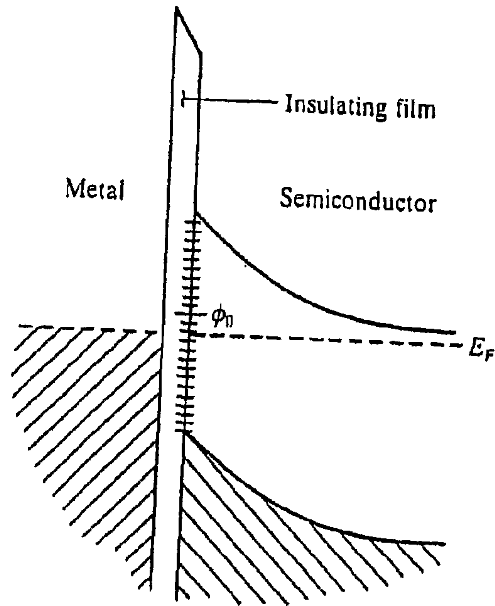


Figure 36A

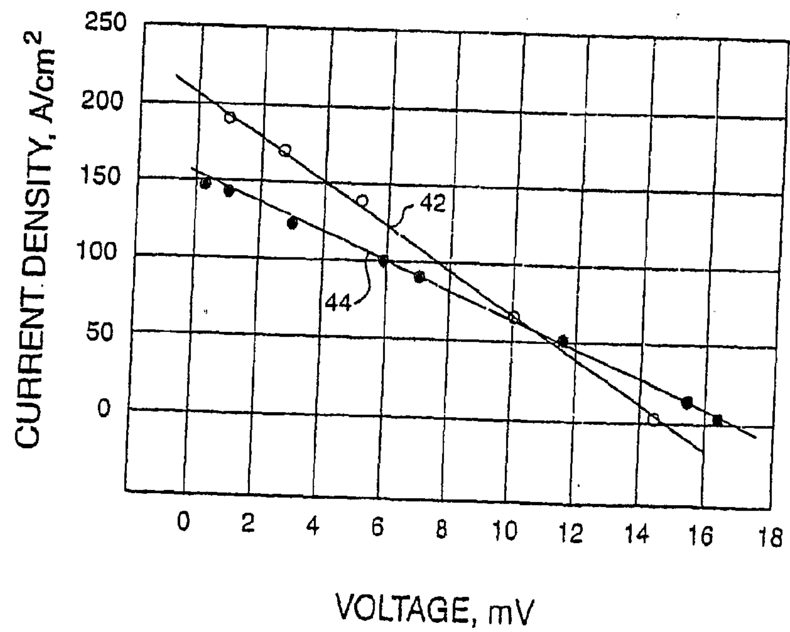


Figure 37

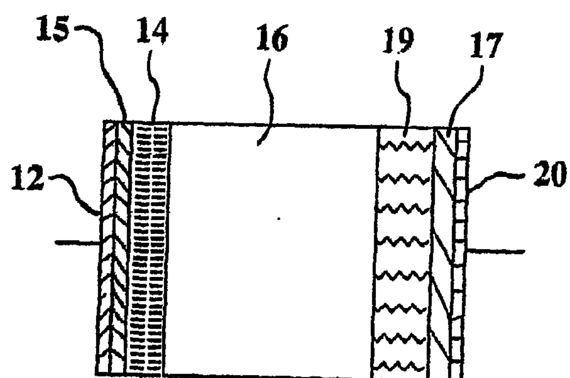


Figure 36B

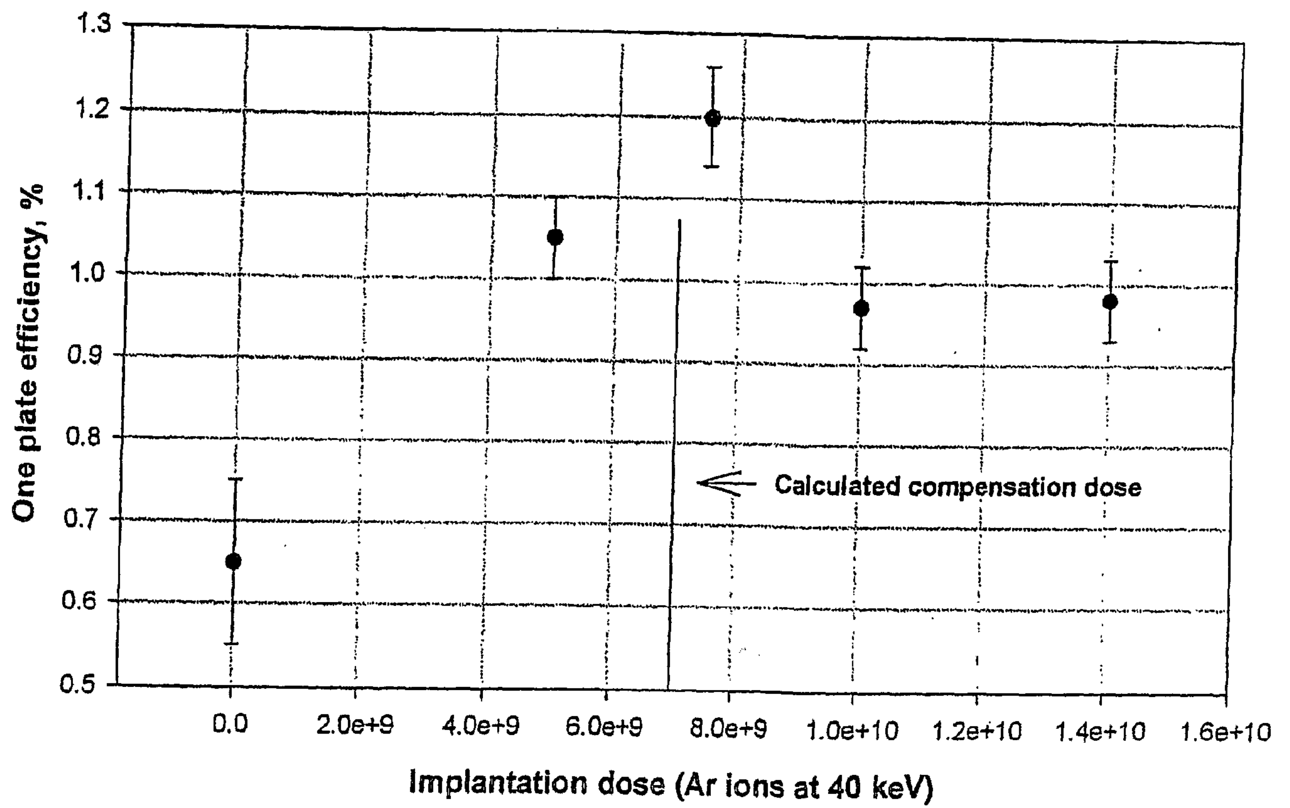


Figure 38

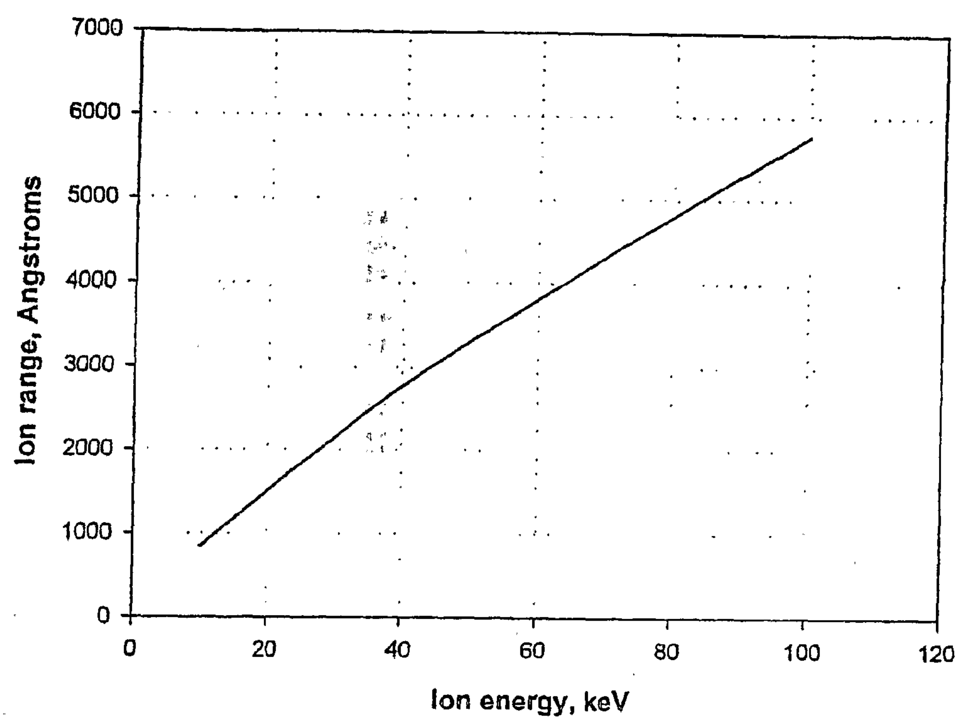
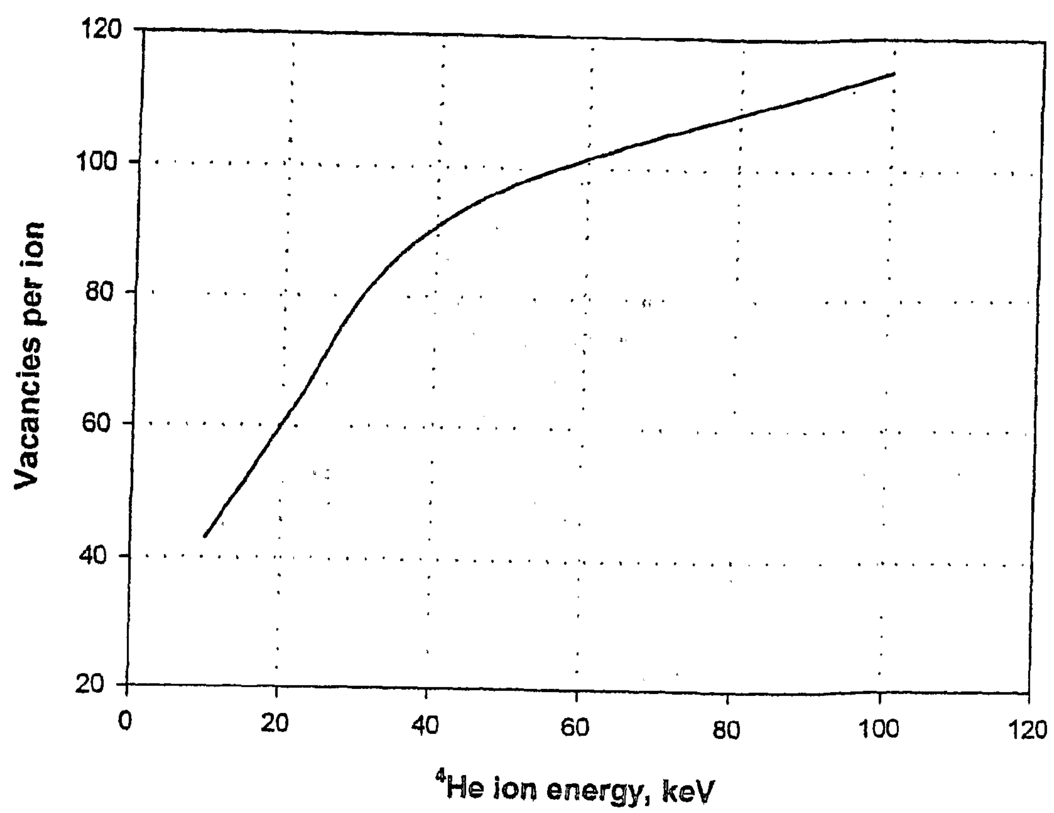


Figure 39



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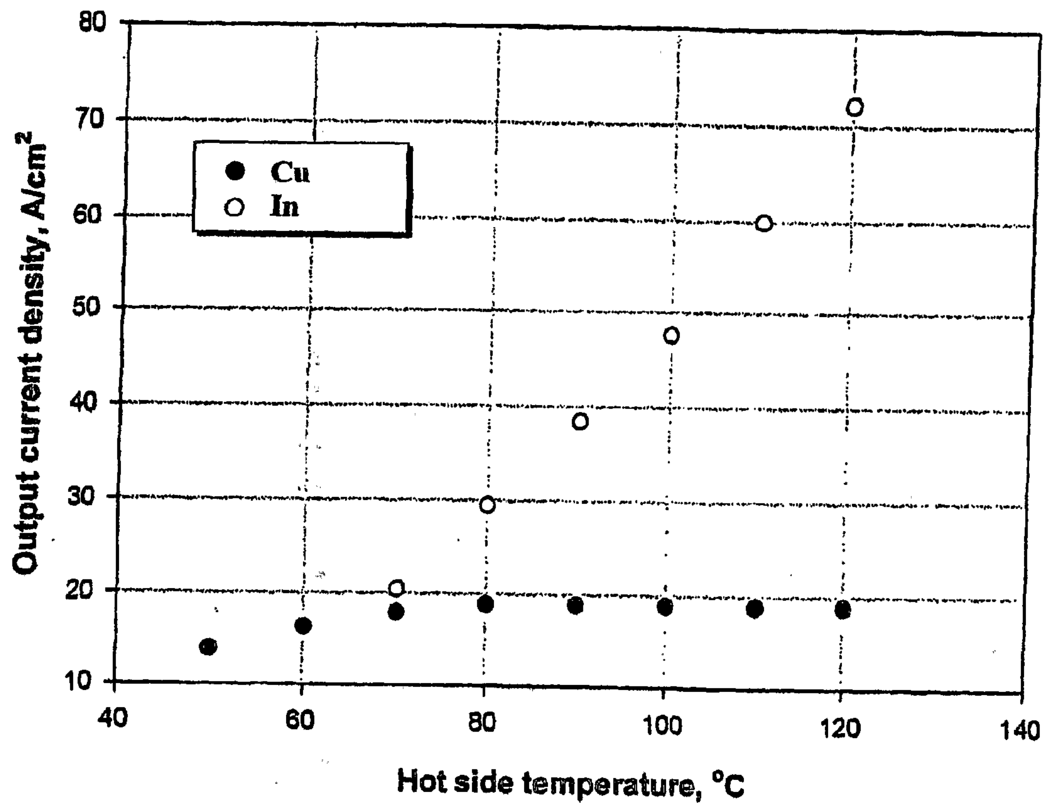


Figure 41

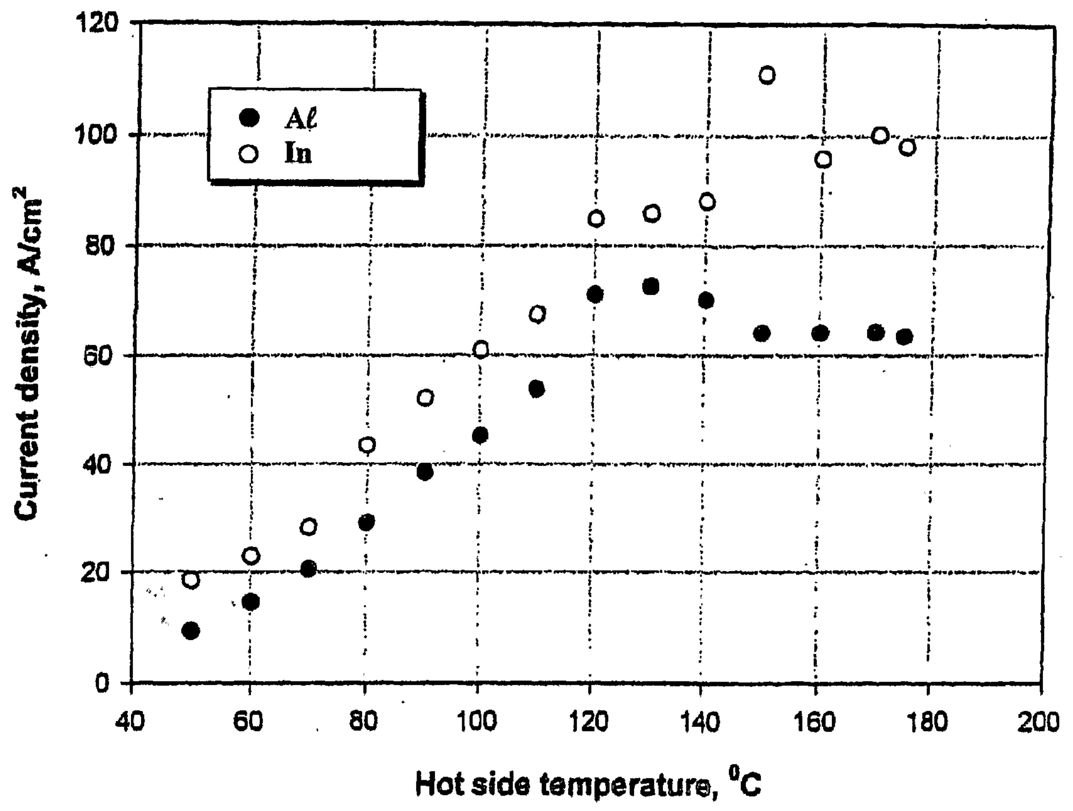


Figure 42

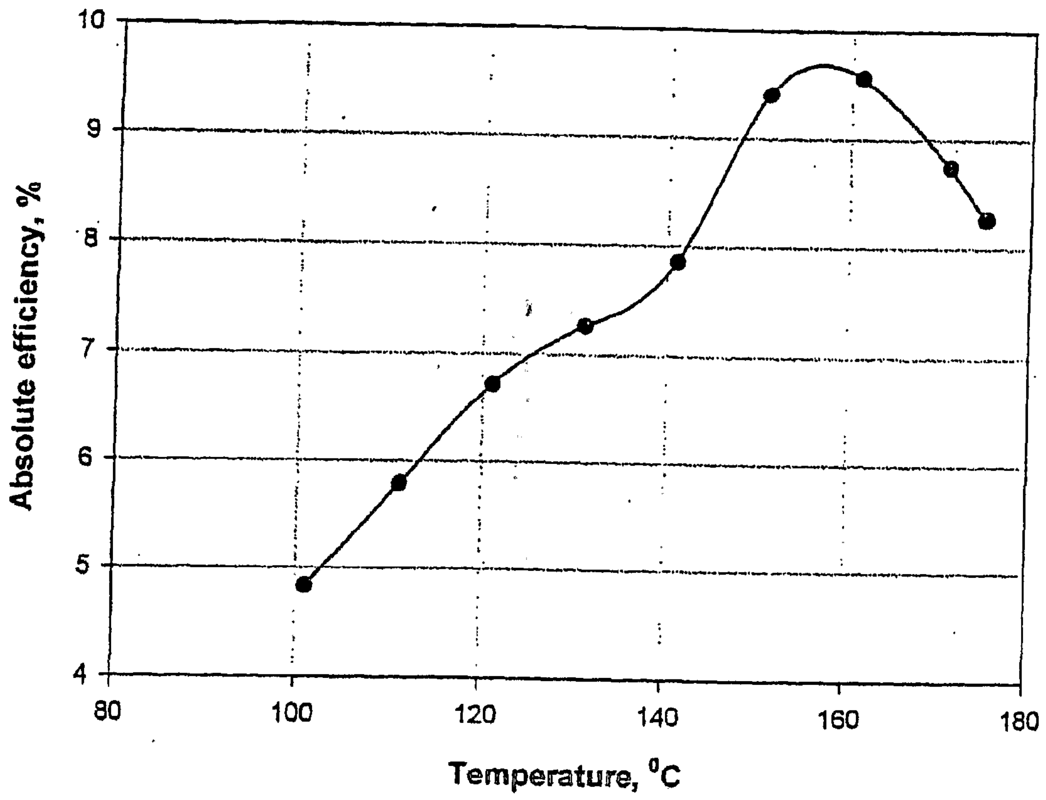


Figure 43

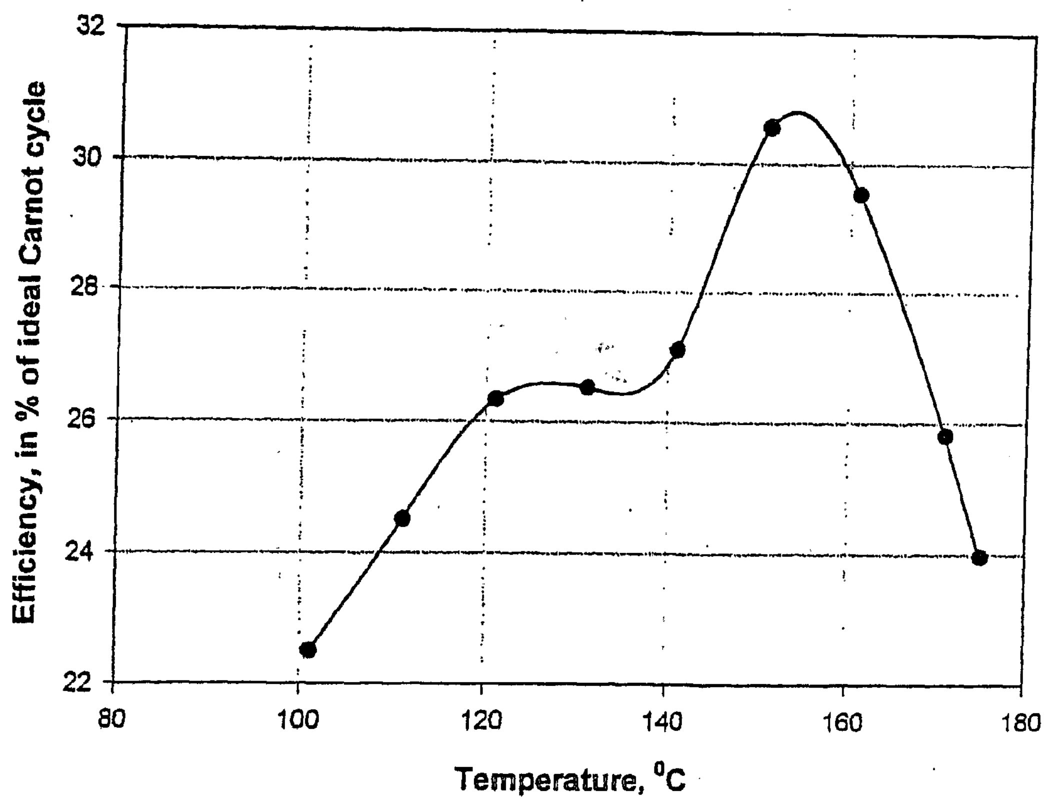
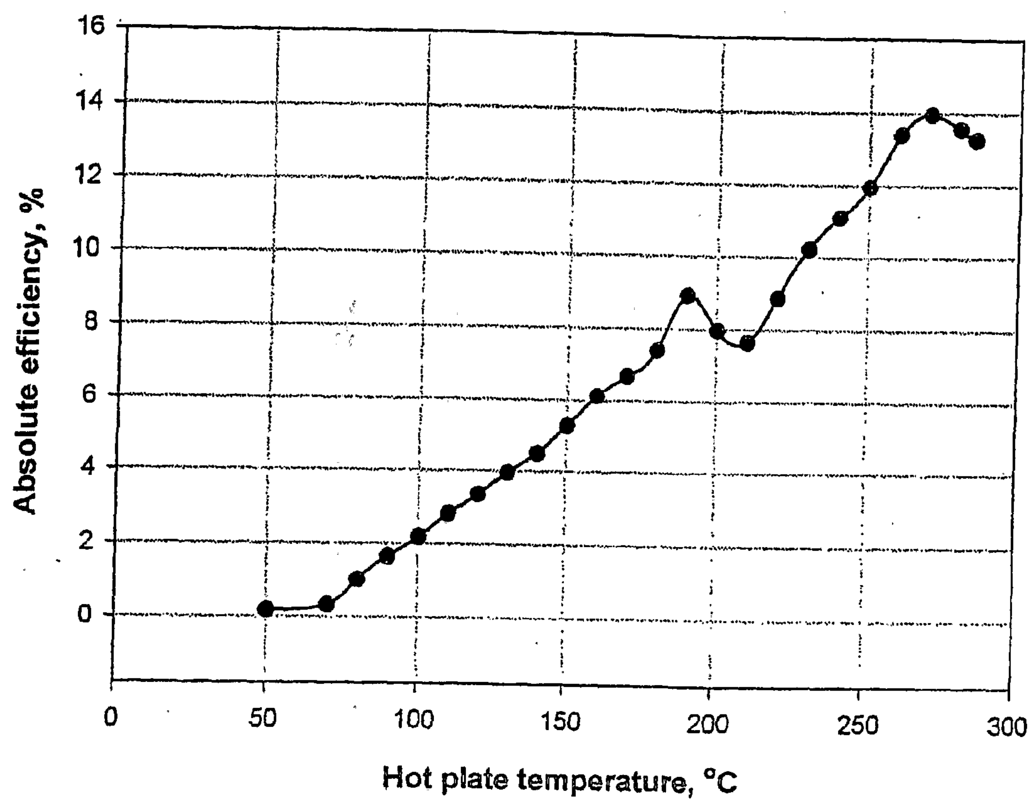


Figure 44



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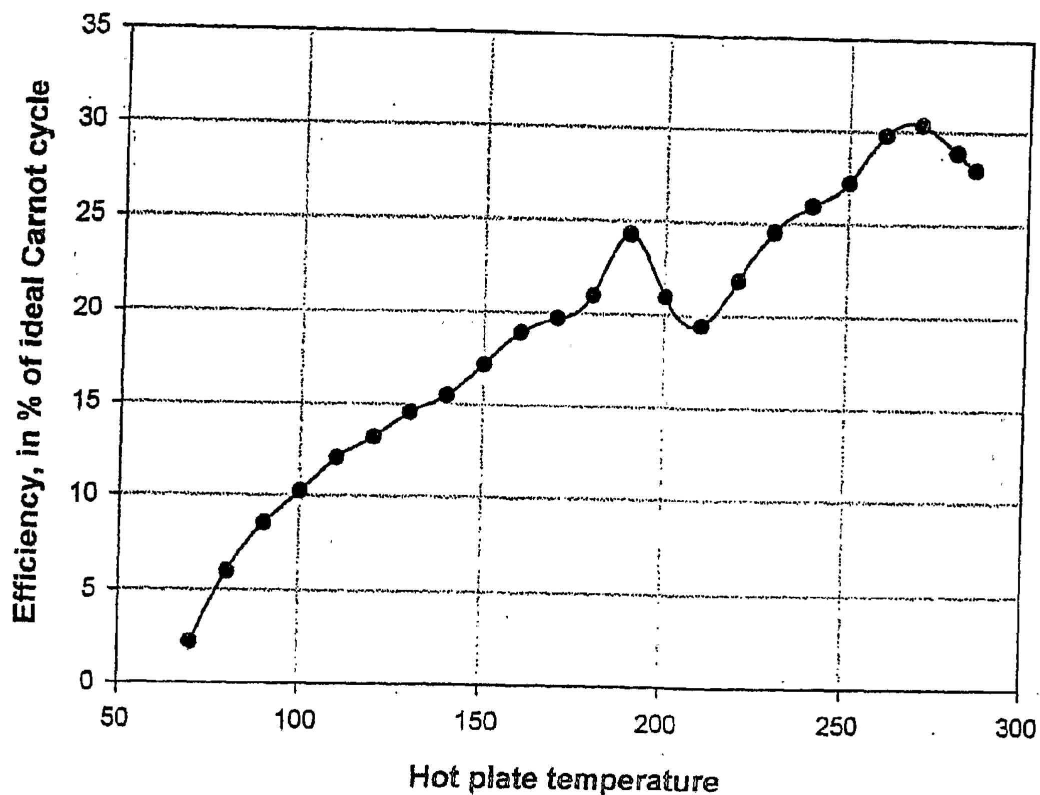

Figure 46

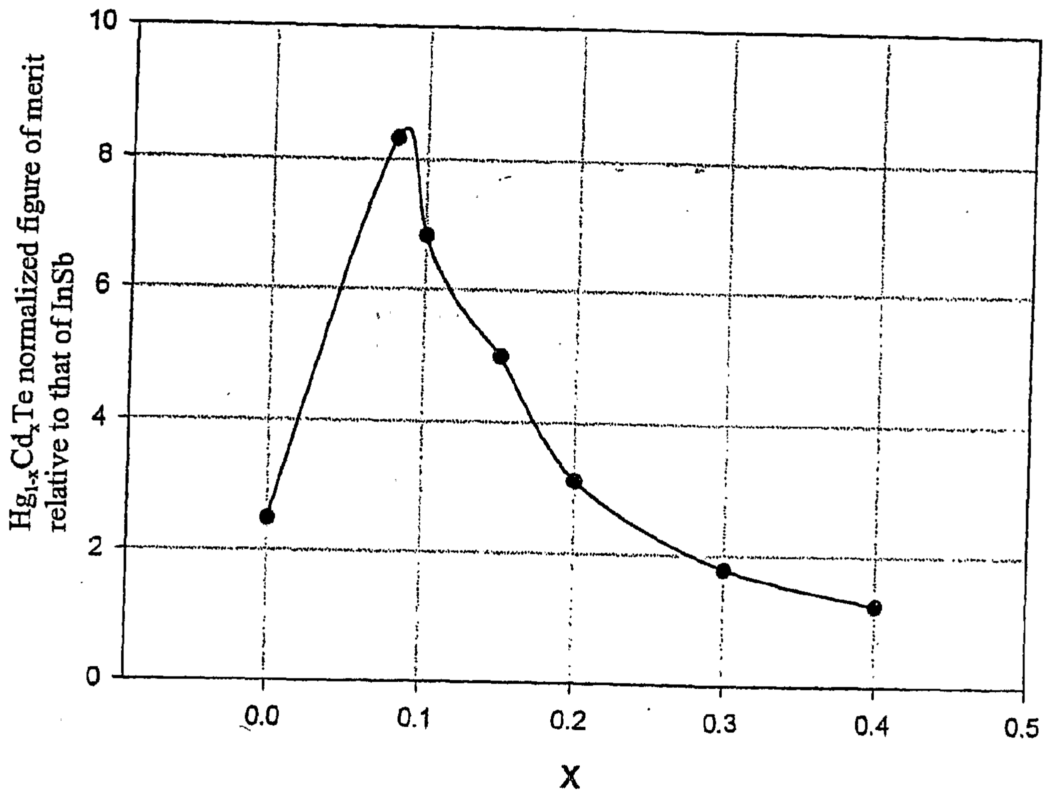

Figure 47

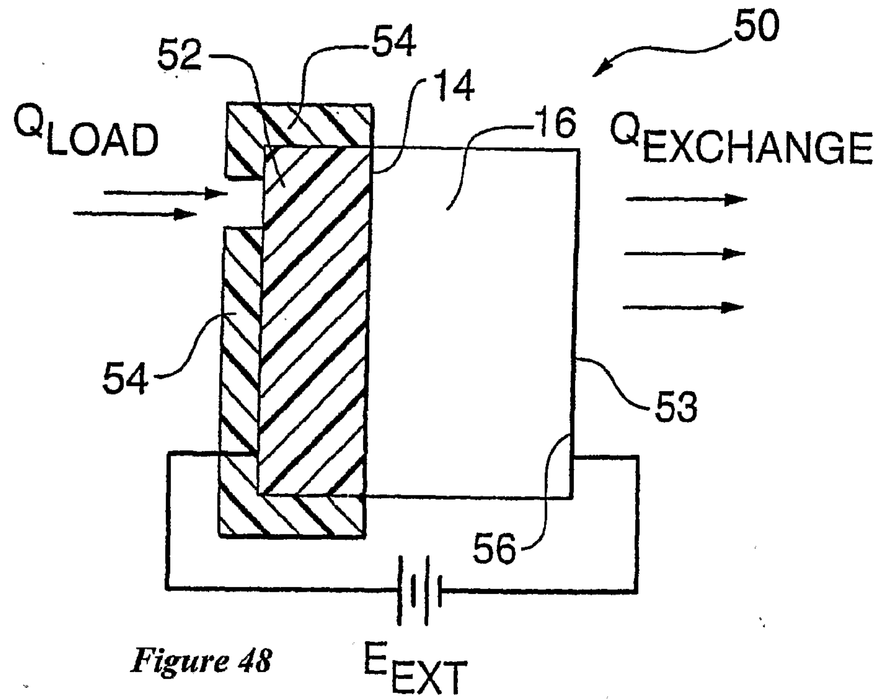

Figure 48

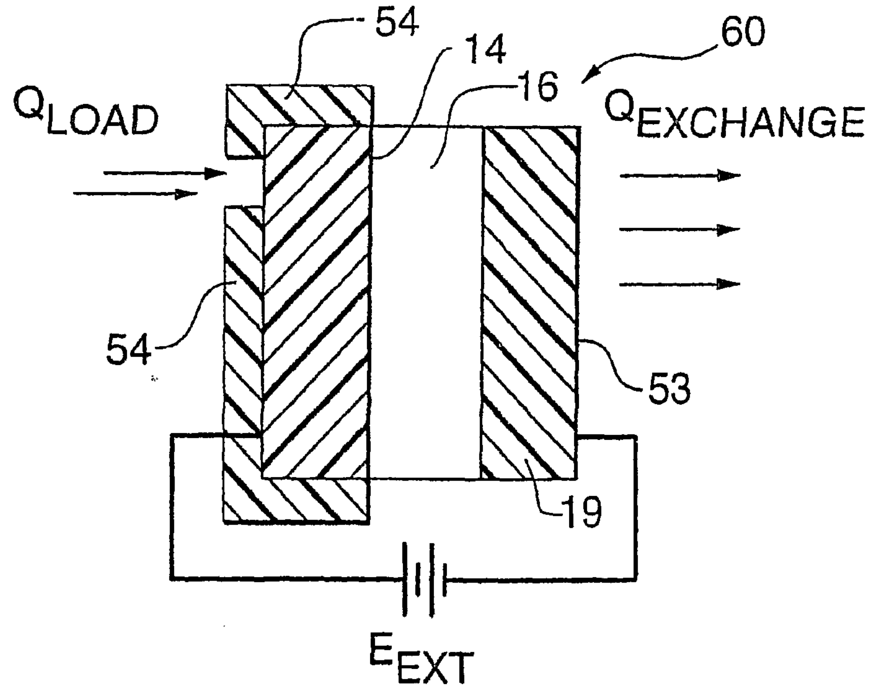

Figure 49

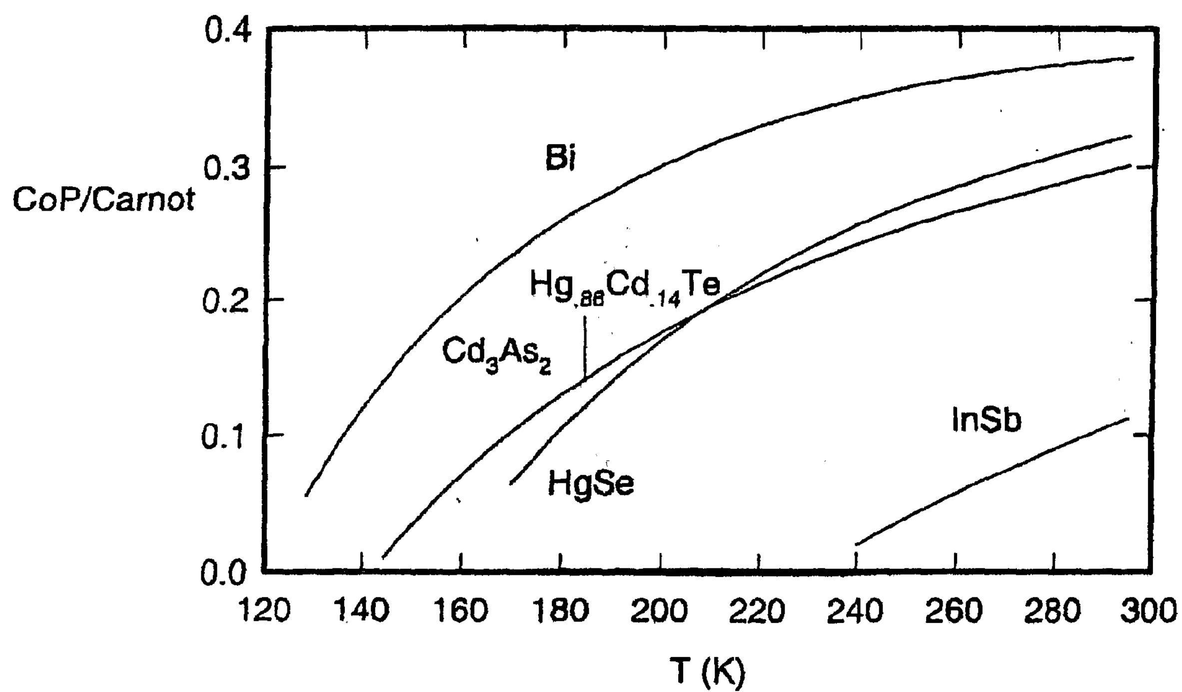

Figure 50