United States Patent

Rogers

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[54] ELECTRONIC VALIDATOR SYSTEM FOR MAGNETIC CREDIT CARDS AND THE LIKE

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[52] **U.S. Cl.** .....**235/61.7 B,** 340/149 A
[51] **Int. Cl.** **G06k 7/00**
[58] **Field of Search** .....235/61.11 D, 61.12 M, 61.12, 235/61.7 B; 340/149 A, 174 SP, 174 PM

[56] **References Cited**

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3,401,830	9/1968	Mathews	340/149 A UX
3,080,550	3/1963	Kuhrt	340/174 PM
3,513,298	5/1970	Riddle et al.	235/61.11 D UX
3,588,449	6/1971	Paterson	235/61.7 B

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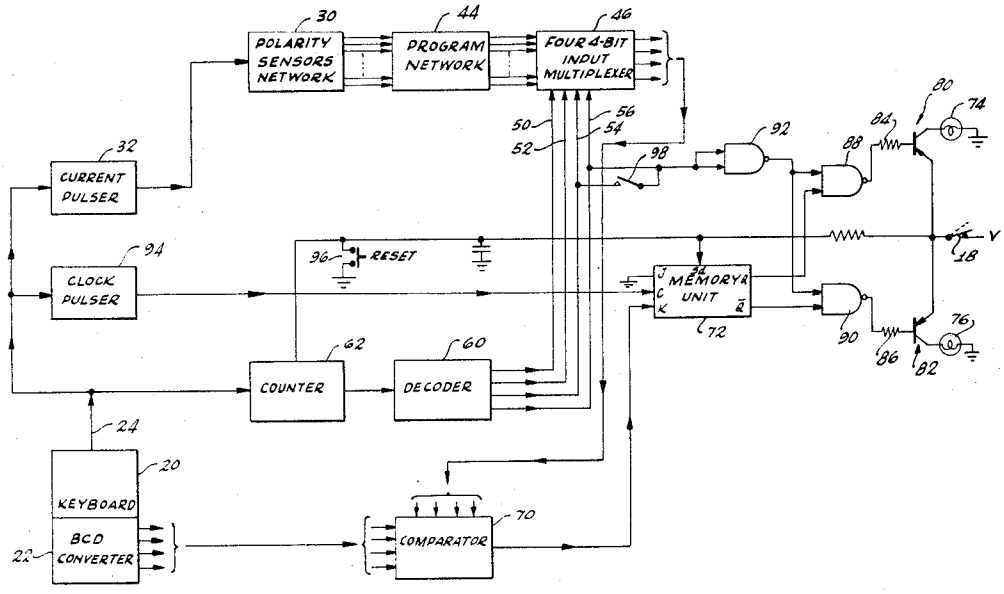
[57] **ABSTRACT**

A plurality of resistive elements, each adapted to exhibit the Hall effect, are arranged in a plane. A magnetic card with a plurality of portions magnetized along lines perpendicular to the card faces is adapted to be placed adjacent such plane with each magnetized portion aligned with a respective element. From each element a voltage is developed which represents the polarity of the adjacent end of the magnetized card portion aligned therewith, and via a program network such voltages are applied to a multiplexer. A keyboard is provided with keys or pushbuttons to be operated by a customer in a predetermined sequence. Via a counter and decoder, successive key operations enable different portions of the multiplexer to provide successive BCD outputs therefrom, and simultaneously a converter establishes a BCD output corresponding to the number or location of each key that is operated. The pairs of BCD signals are applied to a comparator which is connected to a memory unit. A clock pulse established upon each key operation is also applied to the memory unit, and an output for the memory unit is established coincidentally with the occurrence of the clock pulse generated upon operation of the last key in the predetermined sequence. The output of the memory unit is true if the successive comparisons matched, whereupon a lamp is operated to signify that the card is good. The memory unit output is false if all comparisons did not match, whereupon a lamp is operated that signifies the card is bad.

5 Claims, 4 Drawing Figures



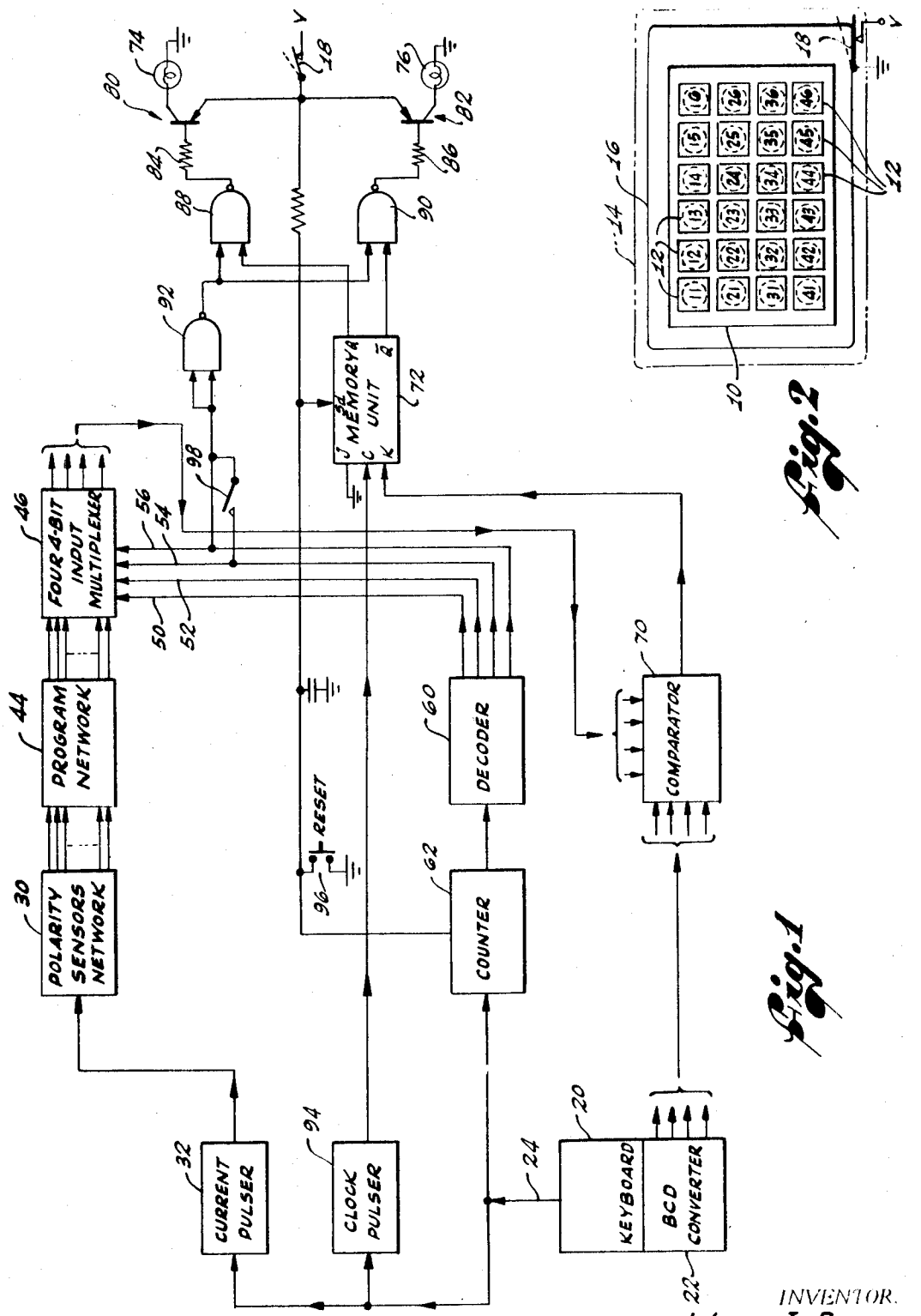


Fig. 1

Fig. 2

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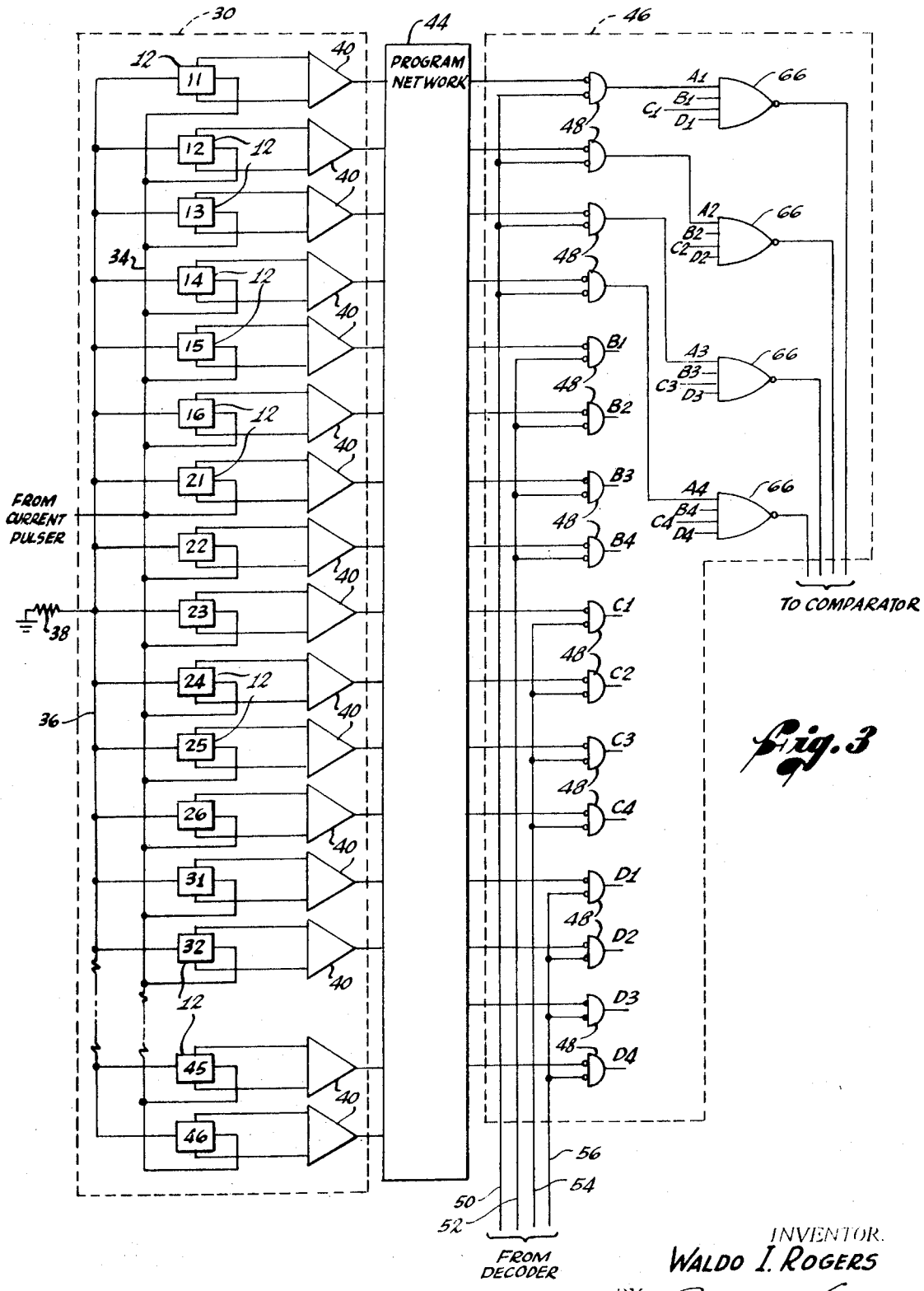

Fig. 3

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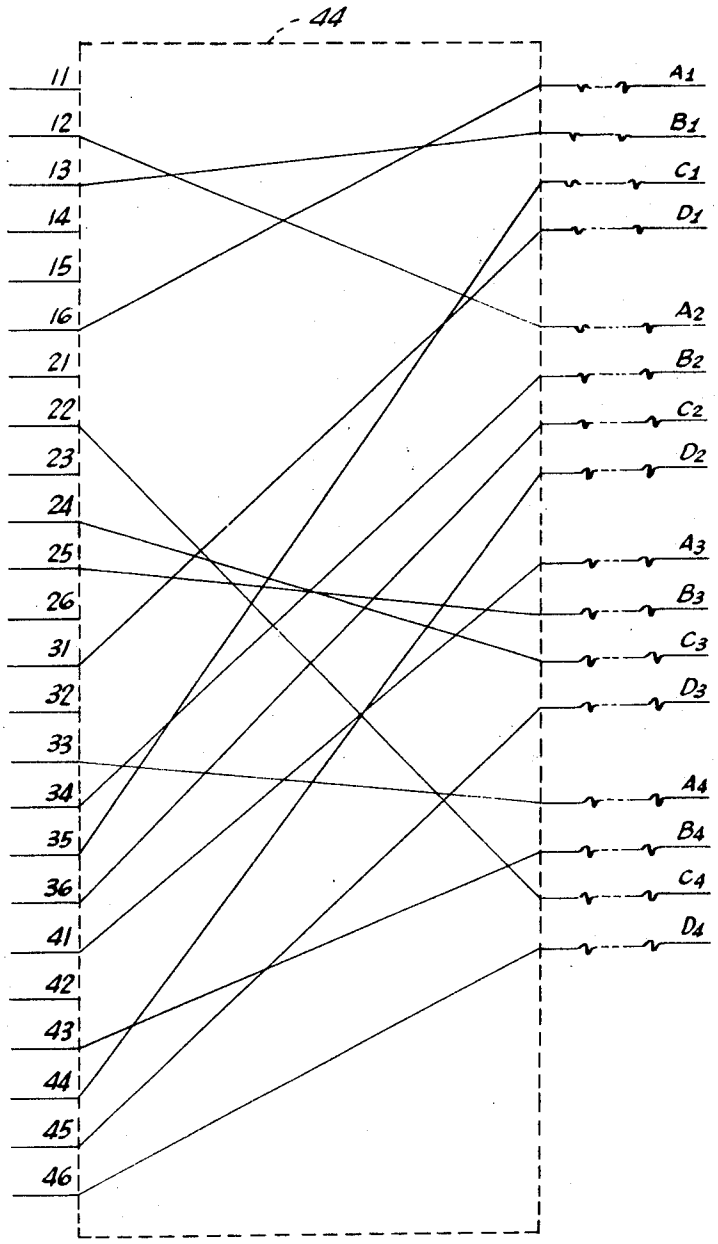

Fig. 4

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ELECTRONIC VALIDATOR SYSTEM FOR MAGNETIC CREDIT CARDS AND THE LIKE

CROSS-REFERENCE TO COPENDING APPLICATION

See application entitled, "Electronic Reader Means for Magnetic Credit Cards and the Like," Ser. No. 842,190, filed July 16, 1969, by Louis M. Ballard and Waldo I. Rogers, and assigned to the same assignee as the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to electronic validator apparatus for magnetic credit cards and the like.

2. Description of the Prior Art

Validator systems to which this invention relates are the type disclosed in U.S. Pat. No. 3,401,830, for "Vending Machine For Credit Card Purchasing," issued Sept. 17, 1968. In said patent, a customer has a memorized decimal or alphanumeric code which he enters into the system via a keyboard or the like. A BCD converter translates each decimal value to its BCD equivalent, and a register effects further translation to a straight binary number. Also, the customer has a credit card that is coded in bits that represent a binary number. The card is inserted in a card reader that has bit sensors from which the straight binary number is obtained. The two straight binary numbers are applied to respective registers of a comparator, which generates a "vend" signal only if the two numbers are identical, i.e., if the contents of the registers in the comparator are equal.

Unfortunately, such a system can be operated by one who has a lost or stolen card. In this connection, the binary number for the card is automatically placed in the appropriate comparator register when the card is put in the card reader. A person having a lost or stolen card can place it in the card reader and then operate the manual selectors by trial and error until he gets a "vend" signal.

SUMMARY OF THE INVENTION

This invention embraces a magnetic card validator system having polarity sensor devices in a circuit to develop logic level signals representing coded portions of a magnetic card, manual selectors operable in a predetermined sequence for a customer code associated with the card code, circuit means to develop logic level signals representing the selector operations, logic network means to code the respective sets of logic level signals, and means operable upon the last selector operation to indicate whether the coded signals correspond.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a combined block and schematic diagram of a magnetic card validator system in accordance with my invention;

FIG. **2** is a plan view of a card bearing a plurality of resistive elements adapted to exhibit the Hall effect for polarity sensing and a magnetic card adjacent thereto wherein the ends of magnetized card portions are aligned with the respective resistive elements;

FIG. **3** is a schematic diagram for the polarity sensors network and the multiplexer of FIG. **1**; and

FIG. **4** is a schematic wiring diagram for the program network of FIG. **1**, to illustrate a coded arrangement of connections between outputs of the polarity sensors network and the inputs of the multiplexer.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENT

Referring to FIG. **2**, there is shown a card **10** supporting a plurality of resistive elements or chips **12**, which in this example are shown as 24 elements arranged in four rows and six columns. To aid in identifying the positions of the respective chips **12**, the individual chips are numbered, with the chips in the first row numbered 11–16, the first digit indicating the row and the second digit indicating the column. This same numbering scheme is provided for the remaining chips, those in the second row being numbered 21–26, those in the third row being numbered 31–36, and those in the fourth row being numbered 41–46. The card **10** is held in a stationary support, indicated in phantom at **14**, which preferably is a housing provided with a slot to receive a magnetic card **16**.

The magnetic card **16** preferably is of the type having a sheet of homogeneous material that has a plurality of portions magnetized along lines perpendicular to the card faces. The positions of the magnetized portions are shown as dotted circles superimposed on the chips **12**, i.e., the card **16** is magnetized at portions such that when the card is inserted in the housing **14**, each magnetized portion is aligned with a respective chip **12**. Such card portions are magnetized in accordance with a code, e.g., the polarities of the magnetized portions adjacent the chips **12** are distributed in accordance with a master pattern, with predetermined ones of the poles representing a code for the particular card. In this connection, the customer to whom such a card is issued does not know the polarity distribution of the magnetized portions of his card. When the card **16** is inserted in the housing **14**, it closes a switch **18** for connecting a power supply to the system.

Referring to FIG. **1**, a keyboard unit **20** has an associated BCD converter **22** which is adapted to provide a binary coded output representing the magnitude of the decimal for each key that is depressed. For purposes of simplifying the description of the system, it will be assumed that the keyboard has 10 keys numbered "**0**," "**1**," . . . . . "**9**." The keyboard also has a switch circuit in common with each key, so that each key when depressed will operate the common switch circuit and establish a voltage output, as on the line indicated at **24**. Keyboards of this type, with binary coded decimal output means and a common switch circuit, include those having a telephone-type pushbutton keyset, such as described in "-Product News" (1969, Automatic Electric, North Lake, Illinois).

The chips **12** are adapted to exhibit the Hall effect, which is manifested as a DC voltage that is positive or negative depending upon the direction of current flow through the chip. In this connection, each chip is characterized in that during current flow through it, a potential is established across it in a direction at right angles to the current flow when a pole of a magnet is placed in proximity to the chip. Further, the potential developed across such a chip in the presence of a south pole is the reverse of that developed across it in the presence of a north pole.

Thus, the chips **12** are polarity sensors, and are included in a polarity sensors network **30** which is coupled to a current source. The current source is illustrated as a pulser **32** which is operated upon each actuation of a pushbutton of the keyboard **20**, i.e., upon each operation of the common switch circuit, to supply a pulse of current to the chips **12** in the network **30**. In this connection, and referring to FIG. **3** along with FIG. **1**, each of the chips **12** is shown connected to the current pulser **32** so that current flows therethrough from right to left. To this end, leads from the right edges of the chips are connected to a bus **34** to which current is supplied from the current pulser **32**. Leads from the left edges of the chips **12** are connected to a bus **36** which is connected to ground through a current-limiting resistor **38**.

Leads from the top and bottom edges of each of the chips **12** are connected to a respective amplifier **40**, which preferably are DC amplifiers adapted to amplify small potentials developed between such leads to a desired level, e.g., by a factor of 1,000. The DC output voltage from each amplifier **40** is positive or negative, depending upon whether the pole of a magnetized card portion aligned with the associated chip is a north pole or a south pole. The outputs of the amplifiers **40** are connected, as shown, to a program network **44**.

The program network **44** has output connections to respective elements in a network designated as a four 4-bit input multiplexer **46**, such elements being shown in FIG. **3** as gates

48. In the arrangement shown, the gates 48 are enabled in groups of four, as via a lead 50 to enabling terminals of the top four gates, the outputs of such gates being labeled A1, A2, A3, A4; via a lead 52 to the enabling terminals of the next four gates, the outputs of which are labeled B1, B2, B3, B4; via a lead 54 to the enabling terminals of the next group of four gates, the outputs of which are labeled C1, C2, C3, C4; and via a lead 56 to the enabling terminals of the bottom four gates, the outputs of which are labeled D1, D2, D3, D4.

As indicated in FIG. 3, the leads 50, 52, 54, 56 are from a decoder, shown in FIG. 1 at 60. To the decoder 60 is connected a counter 62 which is operated in response to each pushbutton operation, i.e., in response to each operation of the common switch circuit. In the example to be described, a pushbutton code is composed of four pushbuttons to be actuated by the card customer. That is, when the customer's magnetic card 16 is inserted in the housing 14, the customer actuates four pushbuttons of the keyboard 20 in a predetermined sequence. That is, the customer's complete code includes a card code which he does not known and a keyboard code which he does know.

When the power supply is off, i.e., before the magnetic card 16 is inserted in the housing to close the switch 18, the counter 62 is set at zero. When the card is inserted and power is applied, the counter 62 and decoder 60 respond to the four successive pushbutton operations so that the leads 50, 52, 54, 56 are energized in succession. For purposes of illustration, it will be assumed that for a chip 12 with which a north pole of a magnetized card portion is aligned, the output of the associated amplifier 40 is positive, and the input to the gate 48 with which that amplifier is connected is true, e.g., "1." Similarly, for a chip 12 with which the south pole of a magnetized card portion is aligned, the output of the associated amplifier 40 is negative, and a false or "0" input appears at the input lead of the gate 48 with which that amplifier is connected.

As shown in FIG. 3, the outputs of the gates 48 having "A" outputs are connected to inputs of respective NOR gates 66. The top gate 66 is shown to have input leads A1, B1, C1, D1, and the remaining gates have respective input leads A2–D2, A3–D3, and A4–D4. These leads are connected to correspondingly labeled output leads of gates 48.

Considering the operations of the first group of four gates 48, which are simultaneously enabled via lead 50, the outputs of the gates 66 are true or false depending upon whether their inputs are false or true, and therefore correspond to the logic levels of the inputs to the gates 48. Further in this connection, the decoder functions so that when the lead 50 is energized, the enabling leads of the top four gates 48 are false. Thus, if the input to any of these gates from the program network 44 is true, the gate output is false, and the output of the associated NOR-gate 66 is true. If the input to any such gate 48 from the program network 44 is false, the output of such gate is true, and the output of the corresponding NOR-gate 66 is false. In similar fashion, through each of the leads 52, 54, 56, the enabling leads of the associated gates 48 is made false, whereupon the same logic operations of the gates 48 and 66 occur.

The outputs of the NOR-gates 66 constitute the outputs of the multiplexer 46, and are applied to a comparator 70. As shown in FIG. 1, the outputs of the BCD converter 22 are also applied to the comparator 70. With this arrangement, the comparator 70 functions to compare two sets of binary coded decimal inputs, and is a 4-bit comparator in this illustration. Further in this connection, let it be assumed that the BCD converter 22 has four output leads on which bits appear which represent the conventional binary code for pushbuttons numbered "0"–"9." Thus, for four successive pushbuttons "8," "1," "7," "5," the outputs from the BCD converter 22, and hence the inputs therefrom to the comparator 70, are successively 1000, 0001, 0111, and 0101. The binary coded inputs to the comparator 70 from the multiplexer 46 will match those from the BCD converter 22 for a properly coded magnetic card.

The output of the comparator 70 is applied to a memory unit 72. In the event of a complete match of the four sets of binary coded inputs to the comparator 70 from the converter 22 and multiplexer 46, the memory unit 72 effects operation of a lamp 74, e.g., a green lamp, to signify that the card is good. On the other hand, if there is any discrepancy in any bit comparison, the memory unit 72 effects operation of another lamp 76, e.g., a red lamp, to signify that the card is bad.

Neither of the lamps 74, 76 is operated unless and until the last key of the pushbutton code is operated. If it were otherwise, i.e., if one or the other of the lamps operated each time a pushbutton was depressed, a person in possession of a lost or stolen card, and who was therefore unaware of the pushbutton code for the particular card, could by trial and error determine the code sequence for the keyboard operation. To inhibit lamp operation until the last pushbutton operation, FIG. 1 illustrates an example of logic level control circuitry wherein the base electrodes of PNP transistors 80, 82 are coupled via resistors 84, 86 to the outputs of respective gates 88, 90. The lead 56 through which the last set of gates 48 in the multiplexer 46 are enabled, i.e., upon operation of the fourth pushbutton in the example described, is connected to an inverter 92, the output of which is connected to respective input leads for both gates 88, 90. In the context of the previously described logic levels established through the leads from the decoder 60, the operation of the fourth of any sequence of pushbuttons causes the input to the inverter 92 to be false, and hence its output, and the inputs to the gates 88, 90 connected thereto, to be true.

The memory unit 72 has a pair of complementary outputs, Q and $\overline{Q}$, which are shown respectively connected to the remaining inputs of gates 88, 90. The memory unit is of the type adapted to be pulsed, and is shown with a clock input terminal, C, to which a clock pulser network 94 is connected. The clock pulser 94 responds to each operation of the common switch circuit, i.e., to each pushbutton operation, to apply a pulse to the C terminal of the memory unit 72. Further in this regard, clock pulser 94 is operable to generate a pulse which is shorter than the pulse applied to the polarity sensors from the current pulser 32, and which further is initiated and terminated during the occurrence of each pulse from the current pulser 32. By way of example, each pulse from the current pulser 32 may be a 400-microsecond pulse, and each pulse from the clock pulser 94 may be a 200-microsecond pulse which occurs 100 microseconds following the leading edge of the pulse from the current pulser, and which terminates 100 microseconds ahead of the pulse from the current pulser.

The memory unit 72 is shown to be of the dual input type, commonly known as a J-K flip-flop, the two input terminals being designated J and K, with the J terminal in this example being connected to ground and the K terminal being connected to the output of the comparator 70. The unit also has a DC set terminal, S_d, by which, upon closure of the switch 18 to connect such terminal to the power supply, the unit is initially set to a state wherein one of its outputs is true and the other is false, e.g., the Q output is true or "1" and its $\overline{Q}$ output is false or "0." The grounded J input terminal is always false, and the outputs of the unit will or will not change depending upon the logic level of the signal at the K terminal. For a detailed schematic and description of operation of such a memory unit, reference can be made to "Signetics Utilogic II Handbook" (1969, Signetics Corporation, Sunnyvale, California).

Initially, there is of course no output from the comparator 70, and the K input to the memory unit 72 is false or "0." Further, the comparator 70 functions so that its output after each bit comparison is false if the binary coded signals applied thereto from the multiplexer 46 and the BCD converter 22 are identical. If such identities exist for each of the four comparisons, the K input remains false and the Q and $\overline{Q}$ outputs remain true and false respectively. Accordingly, upon the operation of the inverter 92 following the operation of the last pushbutton, the inputs to the gate 88 are "1" and "0," and the inputs to the gate 90 are both "0."

With gates **88**, **90** functioning as NAND-gates in the example just described, the output of the gate **88** is "0" and the output of the gate **90** is "1." The lower output level of the gate **88** effectively establishes a sufficient emitter-base potential difference for the transistor **80** to effect emitter-collector flow from the power supply through the lamp **74**, causing the lamp to be illuminated to signify that the card is good, i.e., the pushbutton sequence is the correct one for the particular card sensed by the network **30**. The higher output level of gate **90**, however, maintains the emitter-base potential difference for the transistor **82** too small for its conduction, whereby the lamp **76** is not operated.

On the other hand, any mismatch of the binary coded inputs to the comparator **70** causes the K input to the memory unit **72** to change to "1," and thereby causes the Q and $\overline{Q}$ outputs to change to "0" and "1," respectively. Upon the operation of the inverter **92** following the actuation of the last of four pushbuttons, the inputs to the gate **88** are "1" and "0," and the inputs to the gate **90** are both "1." Accordingly, the outputs of the gates **88**, **90** are "1" and "0," respectively. Therefore, the higher level output of the gate **88** inhibits operation of the transistor **80**—preventing illumination of the "good" indicator lamp **74**—and effects operation of the transistor **82** to cause operation of the "bad" indicator lamp **76**.

It is possible that a customer having a valid card and knowing his pushbutton code may inadvertently depress the wrong key. If this happens, it is not necessary to remove the card and reinsert it in order to reset the counter **62**. A normally open reset switch **96** is provided which can momentarily be depressed to connect the reset terminal of the counter **62** to ground, and thereby reset the output of the counter to zero, and also to reset the memory unit so that its Q and $\overline{Q}$ outputs are "1" and "0." The customer can then proceed to operate the pushbuttons in the correct sequence, thus permitting the system to function in the normal manner to effect operation of the "good" indicator lamp **74** as above described.

FIGS. **3** and **4** illustrate aspects of the invention for frustrating attempts to "break" the card code. In the example chosen for illustration, the multiplexer **46** has four groups of four gates **48**, i.e., a total of 16 output connections from the program network **44**. The program network **44** has a greater number of inputs, here shown as connections to the outputs of each of 24 amplifiers **40**. Further, the card **16** is provided with 24 magnetized portions, and the card **10** supports 24 chips **12** connected to the respective amplifiers **40**.

The program network **44** effects apparent random connections among the amplifiers **40** and the gates **48**. In FIG. **4**, the program network is illustrated as a simple connector board, through which gate leads A1, B1, C1, D1 are connected to the amplifiers associated with chips at locations **16**, **13**, **35** and **31**; gate leads A2, B2, C2, D2 are connected to the amplifiers associated with chips at locations **12**, **34**, **36** and **44**; gates leads A3, B3, C3, D3 are connected to the amplifiers associated with chips at locations **41**, **25**, **24** and **45**; and gate leads A4, B4, C4, D4 are connected to the amplifiers associated with chips at locations **33**, **43**, **22**, and **46**.

There are many hundreds of thousands of combinations of 16-polarity distributions of magnetized card portions which can be made up from 24 magnetized portions. Further, for any combination of 16, there are many millions of possibilities of code schemes for magnetized cards and program connections. Still further, the number of magnetized card portions and Hall effect chips can be markedly increased, whereby the combinations of 16 which can be made run into many millions. Also, security is provided against counterfeit cards by randomly magnetizing those card portions for which there will be no connections between the associated amplifiers and any of the gates connected to the program board. Preferably, such program boards are adapted for ready replacement, e.g., as in the manner of circuit boards with edge terminals adapted to be frictionally engaged by mating terminals for the leads from the amplifiers and gate leads to be connected. A plurality of program boards with different connection schemes may be employed to further enhance security.

While a simple wiring board is shown for the program network **44**, this invention embraces program networks which also incorporate logic circuits therein, e.g., integrated circuits. For example, leads from amplifiers associated with chips at locations **16** and **26** may be connected to the inputs of an AND-gate, the output of which is connected to the A1 gate lead, such AND-gate functioning to make the A1 lead false if neither chip or only one chip is confronted by a north pole, and to make such A1 lead true if both chips are confronted by a north pole.

Still further, the invention embraces arrangements wherein a customer's keyboard code involves a plurality of pushbutton operations, and also arrangements wherein one customer may have a longer pushbutton code than another. For example, customers may be provided with six-key pushbutton codes. So that the customer can easily remember it, an alpha-numeric code may be employed, e.g., three letters followed by three numerals. In such case, six enabling leads would be provided between the decoders **60** and the multiplexer **46**, which would be a six 4-bit input multiplexer, e.g., the program network **44** would have 24 output leads and the multiplexer would have six sets of four gates as previously described, and there would be six leads from each of the converter **22** and multiplexer **46** to the comparator **70**. In that case, the inverter **92** would be connected to the sixth enabling lead from the decoder **60**. With such an arrangement, the obstacles become even more insurmountable for one attempting to use a counterfeit card and/or learning a pushbutton code by trial and error with a lost or stolen card.

For the situation where one customer has a longer keyboard code than another, let it be assumed that some customers are provided with pushbutton codes requiring the operation of three keys on the keyboard **20**. This requires that the multiplexer **46** be converted to a three 4-bit multiplexer. This is accomplished by closing a normally open switch **98** connected between the enabling lead **54** from the decoder **60** and the inverter **92**. On closing the switch **98**, the last comparison effected occurs upon operating the third pushbutton on the keyboard. Thus, when a customer with a three-key pushbutton code seeks validation, the switch **98** is closed. When a customer with a four-key pushbutton code seeks validation, the switch **98** is open.

In like manner, this invention is adapted to validate cards wherein there are more than two pushbutton code lengths. Thus, if a system is arranged so that the multiplexer **46** has a maximum of six 4-bit inputs, and wherein different customers are provided with cards which have three-key, four-key, five-key and six-key pushbutton codes, there may be a separate switch **98** connected between the inverter **92** and each of the enabling leads from the decoder which corresponds in number to the last place pushbutton to be operated. Alternatively, one rotary switch may be employed for this purpose.

It should be mentioned that the current pulser **32** is not essential to the operation of this system, but is preferred where a battery is used for the power supply. In this connection, the power supply may be connected so as to continuously apply power to the polarity sensors network **30** upon operation of the switch **18**. However, because such a continuous flow of current through the chips would require cooling means to be employed to prolong their operating life, and would shorten the life of the power supply where a battery is used, it is preferable to use the current pulser.

While the validator system has been described with reference to polarity sensor devices in the form of resistive elements which exhibit the Hall effect, it should be noted that this invention embraces the use of other current-carrying devices adapted to exhibit potentials of opposite sense in the presence of oppositely directed magnetic fields. For example, the chips **12** may be replaced with transistors or other solid-state devices which exhibit a potential difference of one sense in the presence of a north pole and a potential difference of opposite sense in the presence of a south pole.

I claim:

1. Validator apparatus for magnetic cards each having a plurality of portions magnetized along lines perpendicular to the card faces, wherein each card has a respective code determined by the polarity distributions of the magnetized portions thereof, comprising:

selector means including a plurality of manual selectors,

each card having an associated manual selector code in which a predetermined number of selectors are operated in a predetermined sequence;

a plurality of stationary polarity sensors;

means supporting said sensors and a card so that magnetized portions of the card are aligned with respective sensors;

means for coupling said sensors to a power source,

each sensor so connected exhibiting an electrical characteristic that represents whether the adjacent pole of the card portion aligned therewith is a north pole or a south pole;

first means for reading the code represented by the sequence of operation of said selectors;

second means for reading the card code;

comparing means coupled to said first and second reading means;

indicating means operable from said comparing means to signify that the codes read by said first and second reading means are associated or are not associated;

and control means operable by said selector means to prevent operation of said indicating means until the last of said predetermined number of selectors is operated,

said control means including means for enabling said second reading means from said selector means.

2. The combination of claim 1, wherein said sensor coupling means includes means operable by each selector to apply a pulse to said sensors.

3. The combination of claim 1, including means coupled to said enabling means and indicating means and operable to effect operation of said indicating means only upon operation of the last selector of the predetermined number of selectors.

4. The combination of claim 3, wherein said enabling means is effective to enable said second reading means upon each selector operation.

5. The combination of claim 3, wherein, for different cards for which the predetermined number of selector operations is different, said enabling means is selectively settable for each card to enable said second reading means for the number of selector operations therefor.

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