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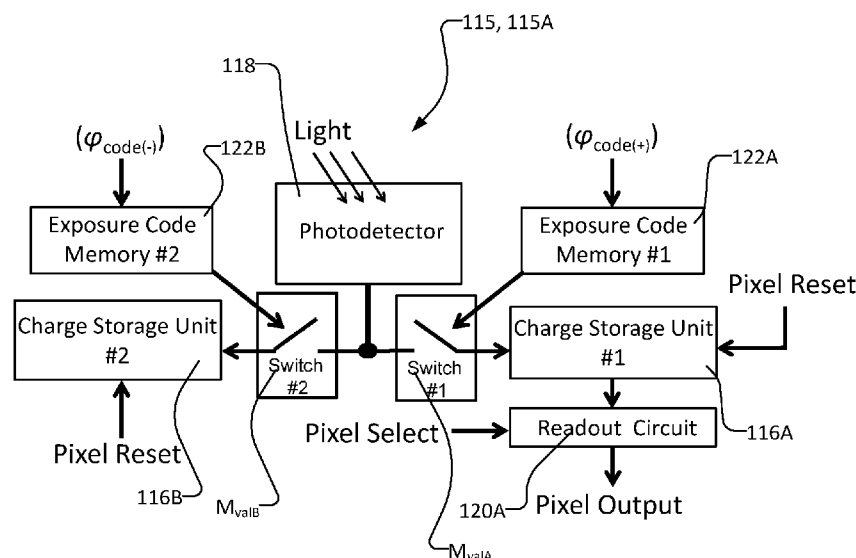


FIGURE 4B

(57) Abstract: A pixel for an image sensor comprises: a photodetector for emitting charge in response to light incident thereon; and a plurality of charge-storage devices and a corresponding plurality of valve switches, each charge-storage device selectively connectable to receive charge from the photodetector by control of a switching state of its corresponding valve switch. The switching state of each valve switch is responsive to a corresponding exposure code signal ϕ_{code} received at a control input of the valve switch.

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CMOS IMAGE SENSORS WITH PIXEL-WISE PROGRAMMABLE EXPOSURE ENCODING AND METHODS FOR USE OF SAME

Cross-Reference to Related Applications

[0001] This application claims priority from application No. 62/500376, filed 2 May 2017 and entitled METHODS, APPARATUS AND SYSTEMS FOR OPERATING AN IMAGE SENSOR. For purposes of the United States, this application claims the benefit under 35 U.S.C. §119 of application No. 62/500376, filed 2 May 2017, and entitled METHODS, APPARATUS AND SYSTEMS FOR OPERATING AN IMAGE SENSOR. All previously filed applications referred to in this paragraph are hereby incorporated herein by reference for all purposes.

Field

[0002] This disclosure relates to CMOS image sensors. Particular embodiments of the invention provide CMOS image sensors which encode or modulate input (scene) light during the process of image capture.

Background

[0003] Computational imaging is an emerging field of technology where input light to an image sensor (e.g. light from a scene that is being directed to the image sensor) is encoded or modulated during the process of image capture and then, after capture, computationally decoded or demodulated to generate one or more images of interest. Computational imaging can be used, without limitation, to capture scene details and/or other scene characteristics or scene features that are not perceptible to the human eye. By way of non-limiting example, computational imaging can be used for applications such as: high-speed motion de-blurring (see R. Raskar, A. Agrawal, and J. Tumblin, "Coded exposure photography: Motion deblurring using fluttered shutter," *Proc. ACM SIGGRAPH*, pp. 795-804, 2006); compressive sensing (see "Flutter shutter video camera for compressive sensing of videos," *Proc. IEEE International Conference on Computational Photography (ICCP)*, pp. 1-9, 2012); and focal-stack photography (see X. Lin, J. Suo, G. Wetzstein, Q. Dai, and R. Raskar, "Coded focal stack photography," *Proc. IEEE International Conference on Computational Photography (ICCP)*, pp.1-9, 2013).

[0004] Figure 1 schematically shows the notional idea behind a computational

imaging system 10 which involves the use of a computational-image-capture emulator 18. Light 8A from scene 8 is directed through suitable input optics 12 (typically comprising one or more lenses 12A and/or other optical components) to computational-image-capture emulator 18. Computational-image-capture emulator 18 is typically implemented using controllable discrete optical components (not shown), such as a liquid crystal display (LCD) mask, liquid crystal on silicon (LCoS), digital micro-mirror device (DMD), other forms of spatial light modulators (SLMs) and/or the like. In some cases, computational-image capture emulators 18 also comprise a number of additional discrete optical components (e.g. lenses, beam splitters, mirrors and/or the like). In some implementations, computational-image-capture emulator 18 may be located to receive light 8A from scene 8 directly and may pass light to input optics 12 (i.e. the order of input optics 12 and computational-image-capture emulator 18 shown in Figure 1 may be switched). The output of computational-image-capture emulator 18 is computationally encoded light 18A which is directed to CMOS image sensor (CIS) 14. CIS 14 captures images in the conventional (continuous exposure or non-intermittent exposure) manner. The images captured by CIS 14 are subsequently stored in memory 18. Since the light impinging on CIS 14 is computationally encoded by emulator 18, the images stored in memory 18 represent computationally encoded image data. A computational-image decoder (typically implemented in the form of a suitably configured central processing unit (CPU)/graphics processing unit (GPU) or some other form of digital processor) 20 (typically embodied by a suitably programmed computer that is separate from the image-capture device and from CIS 14) processes (decodes) the encoded images to produce decoded image data which may be restored in memory 18, output to display 22 or output to some other suitable device (not shown).

[0005] Two types of image-capture encoding include: temporal image-capture encoding and spatial-temporal image-capture encoding (also referred to as spatial image-capture encoding, for brevity). Figures 2A-2C schematically depict conventional (continuous or non-intermittent) image capture, temporal image-capture encoding and spatial-temporal image-capture encoding. Figure 2A schematically depicts a single exposure cycle 24 for a CIS pixel array 26 of CIS 14 with conventional continuous or non-intermittent exposure. Continuous exposure image capture is the technique typically used by current imaging devices and does not involve encoding the input image. Exposure cycle 24 starts by resetting the pixels

(schematically depicted as squares in Figure 2A) during time period 28A. Then, during time period 28B, CIS 14 is continuously exposed to input light. Time period 28B may be referred to as the exposure period or integration period 28B for CIS 14 and is the period during which the photodiode (not shown) associated with each pixel converts photons into electronic charge. At the conclusion of the exposure period 28B, exposure cycle 24 enters a readout period 28C, during which the output signal of each pixel is “read” (typically line by line of pixel array 26) to determine a pixel value corresponding to the charge accumulated during its exposure period. After readout period 28C, the pixels may enter reset period 28A again, where the pixels are reset for capturing new image data.

[0006] Figure 2B schematically depicts a single exposure cycle 34 for a CIS pixel array 26 of CIS 14 during temporally encoded image capture. Reset period 38A and readout period 38C may be substantially similar to reset period 28A and readout period 28C of the continuous exposure image-capture example shown in Figure 2A. However, during exposure period 38B, a sequence of temporal exposure codes is applied to pixel array 26 such that at a number of sub-periods during exposure period 38B, pixel array 26 is not exposed to input light. Sub-periods of an exposure period (e.g. exposure period 38B) may also be referred to as “chops” of the exposure period. Pixel array 26 is shown schematically in Figure 2B as being black for the sub-periods of exposure period 38B during which exposure is off and white for the sub-periods of exposure period 38B during which exposure is on and charge is accumulated. Because charge is accumulated (the corresponding photodiodes are exposed to light) during some sub-periods of exposure period 38B and exposure is off during some sub-periods of exposure period 38B, the Figure 2B exposure scheme may be referred to as intermittent exposure. As can be seen from Figure 2B, the entire pixel array 26 is either white (exposure on) or black (exposure off). A bit can be assigned to the exposure-on and exposure-off states of pixel array 26 (e.g. a bit value of 0 for the exposure-on state and a bit value of 1 for the exposure-off state). It will be appreciated, with such a bit assignment, a temporal encoding or temporal modulation scheme can be imparted on the captured image by encoding each sub-period of exposure period 38B with a corresponding bit value. Accordingly, the Figure 2B process is known as temporal image-capture encoding.

[0007] Figure 2C schematically depicts a single exposure cycle 44 for a CIS pixel

array 26 of CIS 14 during spatial-temporal encoded image capture. Reset period 48A and readout period 48C may be substantially similar to reset period 28A and readout period 28C of the continuous exposure example shown in Figure 2A. However, during exposure period 48B of the Figure 2C example, a spatial-temporal code is applied to pixel array 26, such that for each sub-period (chop) during exposure period 48B, a number of exposure codes are applied pixel-wise to the pixels 26A in pixel array 26, whereby each pixel 26A of pixel array 26 is either permitted to be exposed (shown as being white (exposure on) in the schematic Figure 2C illustration) or is prevented from being exposed (shown as being black (exposure off) in the schematic Figure 2C illustration). The spatial-temporal encoding scheme of Figure 2C is similar to the temporal encoding scheme of Figure 2B in the sense that exposure period 48B is temporally divided into sub-periods (chops), but differs from the temporal encoding scheme of Figure 2B in the sense that rather than having a single code bit for each sub-period, the spatial-temporal scheme of Figure 2C permits different code-bits to be assigned to each pixel 26A in pixel array 26 on a pixel-wise (i.e. spatial) basis for each sub-period. It will be appreciated that with the Figure 2C scheme, the image data captured by pixel array 26 of CIS 14 is both spatially (pixel-wise) and temporally encoded. Accordingly, the Figure 2C process is known as spatial-temporal exposure image-capture.

[0008] For computational image-capture emulator 18 of the Figure 1 system 10, temporal image-capture encoding (modulation) may be implemented for example by a controllable LCD mask which may be used like a rapidly switchable shutter to switch between the accumulating and non-accumulating states. Figure 2D shows such an example of a temporal image-capture modulation emulator 18 that may be used with the Figure 1 system 10. Image-capture emulator 18 shown in Figure 2D comprises a transmissive LCD 51 that is located in the light path between input optics 12 and CIS 14. LCD works as a rapidly-switching electrical shutter under the influence of a control signal 56 from an emulator controller (not shown) to either pass light or block light entirely from CIS 14 to thereby expose CIS 14 to temporally encoded light.

[0009] Figure 2E shows a LCoS-based implementation of a computational image-capture emulator 18 that may be used with the Figure 1 system 10 to emulate pixel-wise spatial-temporal image-capture modulation. Image-capture emulator 18 shown in Figure 2E comprises a number of discrete lenses 50A, 50B, 50C, a polarizing

beam splitter 52 and a controllable LCoS unit 54. Input light 8A from scene 8 is provided to lens 50A, then lens 50B and then impinges on beam splitter 52. Beam splitter 52 splits the input light, some of which is transmitted to controllable LCoS unit 54 in the form of S-polarized light. LCoS unit 54 may be suitably programmed by signal(s) 56 from an emulator controller (not shown) to cause pixels to selectively reflect P-polarized light and to thereby implement a pixel-wise spatial-temporal encoding scheme. P-polarized light reflected from LCoS unit 54, which may be spatially and temporally encoded, passes through lense 50C and is reflected at beam splitter 52 toward input optics 12, which in turn focus the spatially and temporally encoded light onto CIS 14. CIS 14 is thereby exposed by the spatially and temporally encoded light.

[0010] Referring to Figures 2D and 2E and back to Figure 1, it will be appreciated that the image-capture encoding implemented by system 10 is not implemented at the sensor level (i.e. by CIS 14), but rather is implemented by emulator 18 and its controllable discrete optical components. The image-capture encoding implemented by emulator 18 in system 10 actually occurs optically upstream (in the optical path of input light) from the pixels of CIS 14. Thus, while the Figure 1 system 10 may be referred to as computational “image-capture” encoding, the Figure 1 system 10 does not implement true electronic “exposure” encoding in the sense that the encoding by the Figure 1 system 10 does not occur electronically at the sensor level. There is a general desire to implement electronic exposure encoding at the sensor level.

[0011] Further, the controllable discrete optical components used for implementing the system 10 emulator 18 have a large size (when compared to CIS 14, for example), consume large amounts of power, require synchronization between emulator 18 and CIS 14. Also, the limitations of the controllable discrete optical components limit the operational characteristics of such emulators 18 and their corresponding imaging systems 10. For example, in the case of emulator 18 shown in Figure 2E, the physical limitations of LCoS unit 54 limit the resolution of any system 10 using this emulator 18. For emulators 18 that use beam splitters, like beam splitter 52 of the Figure 2E emulator 18, the beam splitter results in a loss of input light and corresponding loss of light efficiency. There is a general desire to implement image-capture encoding and/or exposure encoding that at least ameliorates some of these drawbacks with prior art emulator-based systems.

[0012] Still further, there is a general desire to implement image-capture encoding and/or exposure encoding, to the extent possible, on the same CIS chip as the individual CMOS pixel sensors are located.

[0013] Figure 3A is a circuit diagram of a conventional prior art 4-transistor (4T) CMOS active-pixel sensor (APS) circuit 60 which may be used for a pixel 12A of pixel array 12 in CIS 14 of the Figure 1 system 10. Figure 3B is a corresponding timing diagram for circuit 60 and a plot of the voltage (V) at node 62 (corresponding to the voltage across photodiode 64). For circuit 60, the voltage (V) at node 62 is reset to V_{rst} during T_{Reset} , when the Reset and Trans signals go high. The time T_{Reset} during which the Reset and Trans signals are high corresponds to reset period 28A in Figure 2A. When the Reset and Trans signals transition to low, the exposure period (see period 28B in Figure 2A) begins. The exposure period lasts for a time $T_{Exposure}$, during which photodiode 64 is exposed to photons and corresponding charge begins to accumulate at node 62. This charge accumulation is shown (in the case of the illustrated embodiment) as the voltage signal V decreasing over the exposure period (see Figure 3B). At the conclusion of the exposure period, the Trans and Select signals transition to high and the accumulated voltage is transferred from node 62 to a floating diffusion (FD) and read out by a source follower to output node 66, and this voltage (V_{out}) is read from output node 66. The readout period T_{Read} shown in Figure 3B corresponds to the readout period 28C shown in Figure 2A. Another cycle may begin at the conclusion of the readout period.

[0014] A characteristic of APS circuit 60 is that the charge generated by photodiode 64 is “locked” at node 62, while the Trans signal is low and the corresponding transistor 68 is non-conducting (i.e. for the entire exposure period $T_{Exposure}$). This characteristic of APS circuit 60 makes it challenging to implement intermittent exposure encoding using existing APS circuitry 60. Other types of existing CIS technology exhibit similar characteristics – i.e. that the exposure of the light sensing element (e.g. photodiode, photogate or photo-transistor) is continuous during the exposure period and is not programmable or otherwise controllable.

Brief Description of the Drawings

[0015] The accompanying drawings illustrate non-limiting example embodiments of

the invention.

[0016] Figure 1 is a schematic illustration of a computational imaging system which involves the use of a computational-image-capture emulator.

[0017] Figure 2A is a schematic illustration of a single exposure cycle for a CIS pixel array during conventional continuous or non-intermittent exposure. Figure 2B is a schematic illustration of a single exposure cycle for a CIS pixel array during temporal image-capture encoding. Figure 2C is a schematic illustration of a single exposure cycle for a CIS pixel array during spatial-temporal image-capture encoding. Figure 2D shows a LCD mask-based implementation of a computational image-capture emulator that may be used with the Figure 1 system. Figure 2E shows a LCoS-based implementation of a computational image-capture emulator that may be used with the Figure 1 system.

[0018] Figure 3A is a circuit diagram of a conventional CMOS APS circuit. Figure 3B is a corresponding timing diagram for the Figure 3A circuit.

[0019] Figure 4A is a schematic illustration of a computational imaging system which involves exposure encoding according to a particular embodiment. Figure 4B is a block diagram illustration of an exposure encoder for a particular pixel that can be used as part of the CIS-based exposure encoder of the Figure 4A system according to a particular embodiment. Figure 4C is a block diagram illustration of an exposure encoder for a particular pixel that can be used as part of the CIS-based exposure encoder of the Figure 4A system according to a particular embodiment. Figures 4A, 4B and 4C may be referred to collectively herein as Figure 4.

[0020] Figure 5A is a diagram of a circuit for implementing the Figure 4B exposure encoder for a particular pixel in an APS implementation according to a particular embodiment. Figure 5B is a diagram of a circuit for implementing the Figure 4C exposure encoder for a particular pixel in an APS implementation according to a particular embodiment. Figure 5C is a timing diagram which describes the operation of the Figure 5A or Figure 5B exposure encoder circuit for temporal exposure encoding in one frame cycle according to a particular embodiment. Figure 5D is a timing diagram which describes the operation of the Figure 5A or Figure 5B exposure encoder circuit for spatial-temporal exposure encoding in one frame cycle according to a particular embodiment. Figures 5A, 5B, 5C and 5D may be referred to collectively

herein as Figure 5.

[0021] Figure 6A is a diagram of a circuit for implementing the Figure 4B exposure encoder for a particular pixel in a Capacitive Trans-Impedance Amplifier (CTIA) implementation according to a particular embodiment. Figure 6B is a diagram of a circuit for implementing the Figure 4C exposure encoder for a particular pixel in a CTIA implementation according to a particular embodiment. Figure 6C is a timing diagram which describes the operation of the Figure 6A or Figure 6B exposure encoder circuit for temporal exposure encoding in one frame cycle according to a particular embodiment. Figure 6D is a timing diagram which describes the operation of the Figure 6A or Figure 6B exposure encoder circuit for spatial-temporal exposure encoding in one frame cycle according to a particular embodiment. Figures 6A, 6B, 6C and 6D may be referred to collectively herein as Figure 6.

[0022] Figure 7A is a circuit diagram of a dynamic random access memory (DRAM) unit which may be used as the code-memory unit for any of the pixels of Figure 4, 5 and/or 6 according to a particular embodiment. Figure 7B is a circuit diagram of a static random access memory (SRAM) unit which may be used the code-memory unit for any of the pixels of Figures 4, 5 and/or 6 according to a particular embodiment. Figures 7A and 7B may be referred to collectively herein as Figure 7.

[0023] Figure 8 is a schematic depiction of a CIS system architecture according to a particular embodiment, which shows a CIS pixel array, each pixel of which may be implemented according to any of the pixel (exposure encoder) embodiments described herein (e.g. Figures 4, 5 and 6).

[0024] Figure 9A is a flow chart schematically illustrating a method for operating the Figure 8 CIS system according to a particular embodiment. Figure 9B is a flow chart schematically illustrating a method for performing the temporal exposure encoding procedure of the Figure 9A method according to a particular embodiment. Figure 9C is a flow chart schematically illustrating a method for performing the spatial-temporal exposure encoding procedure of the Figure 9A method according to a particular embodiment. Figures 9A, 9B and 9C may be referred to collectively herein as Figure 9.

Detailed Description

[0025] Throughout the following description, specific details are set forth in order to

provide a more thorough understanding of the invention. However, the invention may be practiced without these particulars. In other instances, well known elements have not been shown or described in detail to avoid unnecessarily obscuring the invention. Accordingly, the specification and drawings are to be regarded in an illustrative, rather than a restrictive sense.

[0026] Figure 4A is a schematic illustration of a computational imaging system 110 which involves exposure encoding using a CIS-based exposure encoder 114 according to a particular embodiment. Aside from CIS-based exposure encoder 114 (which takes the place of emulator 18 and CIS 14), the other components of system 100 may be similar to corresponding components of computational imaging system 10 described above and are referred to herein using similar reference numbers. Aspects of the invention provide a CIS-based (or sensor-based) pixel-wise exposure encoder 114 which may be used in a computational imaging system 110 of the type shown in Figure 4A.

[0027] Figure 4B is a block diagram illustration of an exposure encoder 115 for a particular pixel 115A that can be used as part of the CIS-based exposure encoder 114 of the Figure 4A system 110 according to a particular embodiment. Exposure encoder 115 of the Figure 4B embodiment comprises a plurality (a pair in the case of the illustrated embodiment) of charge-storage devices 116A, 116B which are switchably connectable to photodetector 118 by a pair of controllable (e.g. electronically controllable) switches M_{valA} and M_{valB} (also referred to herein as valve switches). The general scheme implemented by exposure encoder 115 is that, for each sub-period (chop) of an exposure period (see exposure periods 38B, 48B of Figures 2B, 2C), charge resulting from the exposure of photodetector (e.g. photodiode, phototransistor, photogate or some other type of photo-sensitive element) 118 to input light is selectively delivered (by suitably controlling switches M_{valA} , M_{valB}) to either one of charge-storage devices 116A, 116B in accordance with an exposure encoding scheme, but, in the case of the illustrated Figure 4B embodiment, charge is only read out (by readout circuit 120A) from one of the charge-storage devices (charge-storage device 116A in the case of the Figure 4B illustration). Charge directed to the other one of the charge-storage devices (charge-storage device 116B in the case of the Figure 4B illustration) may be discarded when pixel 115A is reset. Thus, any exposure sub-period (chop) when charge from

photodetector 118 is directed to charge-storage device 116A (by switch M_{valA}), is equivalent to pixel 115A being exposed (exposure on) for that sub-period. Conversely, any sub-period when charge from photodetector 118 is directed to charge-storage device 116B (by switch M_{valB}), is equivalent to pixel 115A being not exposed (exposure off) for that sub-period. In some embodiments, a suitable readout circuit (not shown in Figure 4B) could be used to read out charge from charge storage device 116B. At the conclusion of the entire exposure period (comprising a plurality of exposure sub-periods), the accumulated (and encoded) charge stored in charge-storage device 116A may be read out by readout circuit 120A.

[0028] Exposure encoder 115 may optionally incorporate a plurality (a pair in the case of the illustrated embodiment) of code-memory units 122A, 122B, each of which is associated with a corresponding one of charge-storage units 116A, 116B. Code-memory units 122A, 122B may be used for implementing temporal exposure encoding and/or spatial-temporal exposure encoding. In the illustrated Figure 4B embodiment, where there are two code signals/bits (denoted $\phi_{code(+)}$ and $\phi_{code(-)}$), these two exposure code signals $\phi_{code(+)}$ and $\phi_{code(-)}$ can be respectively provided to code-memory units 122A, 122B, which may in turn be used, for each exposure sub-period, to control valve switches M_{valA} and M_{valB} to thereby select whether charge from photodetector 118 is directed to charge-storage unit 116A or charge-storage unit 116B. In the illustrated embodiment, the exposure codes ($\phi_{code(+)}$, $\phi_{code(-)}$) provided to code-memory units 122A, 122B are complementary to one another and this complementary nature of the codes may be denoted herein using the symbols “(+)” and “(-)”. Where the exposure codes ($\phi_{code(+)}$, $\phi_{code(-)}$) are complementary to one another, it will be appreciated that the on/off state of valve switches M_{valA} and M_{valB} are opposite to one another – i.e. if switch M_{valA} is conducting charge from photodetector 116 to charge storage unit 116A, then switch M_{valB} is in a non-conducting state and if switch M_{valB} is conducting charge from photodetector 116 to charge storage unit 116B, then switch M_{valA} is in a non-conducting state. In some embodiments, where the exposure codes ($\phi_{code(+)}$ and $\phi_{code(-)}$) are complementary to one another, it may be possible to implement exposure encoder 115 using a single code-memory unit and a suitable circuit to invert the content of the single code-memory unit. It will be appreciated that for temporal exposure encoding (see Figure 2B), where pixel 115A is controlled by two complementary code signals ($\phi_{code(+)}$, $\phi_{code(-)}$), code-memory units 122A, 122B are not required, since the intermittent

exposure of the entire pixel array (not shown in Figure 4B) is gated simultaneously and suitable control signals may be sent directly to valve switches M_{valA} , M_{valB} . In some embodiments, a readout circuit 120B similar to readout circuit 120A (not shown in Figure 4B) may be provided as a part of exposure encoder 115 and may be connected to charge-storage device 116B for reading charge stored in charge-storage device 116B in manner similar to how readout circuit 120A reads out charge from charge-storage device 116A.

[0029] The components of the Figure 4B pixel 115A (including, for example, photodetector 118, charge-storage devices 116, valve switches M_{val} , code-memory units 122 and/or readout circuits 120) may be fabricated on the same microelectronic chip (or wafer) or on a pair of stacked microelectronic chips (not shown). In some embodiments, photodetector 118 may be fabricated on a first microelectronic chip and the other components of the Figure 4B pixel 115A (including, for example, charge-storage devices 116, valve switches M_{val} , code-memory units 122 and/or readout circuits 120) may be fabricated on a second stacked microelectronic chip that is stacked with the first microelectronic chip.

[0030] In the illustrated embodiment of Figure 4B, exposure encoder 115 of pixel 115A comprises a pair of charge-storage devices 116A, 116B, a corresponding pair of controllable valve switches M_{valA} , M_{valB} and a corresponding pair of code-memory units 122A, 122B controlled by a corresponding pair of exposure code signals $((\Phi_{code(+)}, \Phi_{code(-)}))$. In some embodiments, exposure encoders may comprise a plurality of more than two charge-storage units and a corresponding plurality of more than two switch valves and code-memory units controlled by a corresponding plurality of more than two exposure code signals. A block diagram example of an exposure encoder 215 for a particular pixel 215A of such an embodiment is shown in Figure 4C. The Figure 4C exposure encoder 215 for particular pixel 215A can be used as part of the CIS-based exposure encoder 114 of the Figure 4A system 110 according to a particular embodiment. The Figure 4C exposure encoder 215 is similar in many respects to, and is a generalization in many respects of, the exposure encoder of Figure 4B and similar reference numerals are used to describe features and components of the Figure 4C exposure encoder 215 that are similar to or correspond with the features and components of the Figure 4B exposure encoder 115.

[0031] The Figure 4C exposure encoder 215 for pixel 215A comprises a plurality of N

(where N may be greater than 2) charge-storage devices 116A, 116B ... 116N (collectively, charge-storage devices 116), N corresponding switches M_{valA} , M_{valB} , ... M_{valN} (collectively, switches M_{val} or valve switches M_{val}) and N corresponding code-memory units 122A, 122B, ... 122N (collectively, code-memory units 122) used to control switches M_{val} . In the illustrated embodiment, the Figure 4C exposure encoder 215 also comprises N corresponding readout circuits 120A, 120B, ... 120N (collectively readout circuits 120), although exposure encoder 215 may be implemented with as few as one readout circuit 120. The Figure 4C exposure encoder 215 is programmed (modulated) by a plurality of N exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}), each of which may be stored in a corresponding one of code-memory units 122 and each of which may be used to control a corresponding one of switches M_{val} to thereby gate a corresponding charge storage device 116 (as explained in more detail below). In the Figure 4C exposure encoder 215, the plurality of exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) may be independent of one another, such that, during any exposure sub-period, switches M_{val} may be conducting in any combination or sub-combination so that charge may be selectively accumulated in any combination or sub-combination of charge-storage devices 116. It may be desirable, in some embodiments, to select the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) to ensure that charge is accumulated in at least one charge storage unit 116 (i.e. at least on switch M_{val} is conducting) during each exposure sub-period (chop). In the case where N=2, the Figure 4C exposure encoder 215 may be substantially similar to the Figure 4B exposure encoder 115.

[0032] The components of the Figure 4B pixel 215A (including, for example, photodetector 118, charge-storage devices 116, valve switches M_{val} , code-memory units 122 and/or readout circuits 120) may be fabricated on the same microelectronic chip (or wafer) or on a pair of stacked microelectronic chips (not shown). In some embodiments, photodetector 118 may be fabricated on a first microelectronic chip and the other components of the Figure 4B pixel 115A (including, for example, charge-storage devices 116, valve switches M_{val} , code-memory units 122 and/or readout circuits 120) may be fabricated on a second stacked microelectronic chip that is stacked with the first microelectronic chip.

[0033] Figure 5A is a circuit diagram of a circuit 121 for implementing the Figure 4B exposure encoder 115 for a particular pixel 115A in an APS implementation according

to a particular embodiment. Circuit 121 may be used for a particular pixel 115A of the Figure 4A CIS exposure encoder 114. Circuit 121 may be suitably modified to provide any of the modifications discussed herein in connection with the Figure 4B exposure encoder 115. In circuit 121 of the Figure 5A embodiment, charge-storage devices 116A, 116B (collectively, charge-storage devices 116) are respectively implemented by charge-storage capacitors C_1 , C_2 (collectively, charge-storage capacitors C). Charge-storage capacitors C act as charge-storage devices 116 to store charge transferred from photodetector 118 through valve transistors M_{val1} , M_{val2} (collectively, valve transistors or valve switches or, for brevity, switches M_{val}), where valve transistors M_{val1} , M_{val2} act as switches to selectively switch charge accumulation between charge-storage capacitors C_1 , C_2 during each exposure sub-period. In Figure 5A and the description below, exposure code signals $\phi_{code(+)}$, $\phi_{code(-)}$ may be generalized and referred to as exposure code signals ϕ_{code1} , ϕ_{code2} .

[0034] In circuit 121 of the Figure 5A embodiment, code-memory units 122A, 122B (collectively, code-memory units 122) may be respectively implemented by any suitable memory units. In some embodiments, code-memory units 122 may each be implemented by a corresponding DRAM unit 126. Figure 7A depicts a DRAM unit 126 which may be used to implement a corresponding one of code-memory units 122 in the Figure 5A exposure encoder 115. In the Figure 7A embodiment, DRAM unit 126 comprises a transistor-based switch (M_{dram}) controlled by a corresponding signal (ϕ_{ctrl}) and a corresponding capacitor (C_{dram}). DRAM unit 126 may be connected between a corresponding exposure code signal ϕ_{code} (e.g. one of exposure code signals ϕ_{code1} , ϕ_{code2} shown in Figure 5A) and a corresponding valve transistor M_{val} (e.g. one of valve transistors M_{val1} , M_{val2} shown in Figure 5A). When the control signal ϕ_{ctrl} turns on switch M_{dram} , the exposure code signal ϕ_{code} will appear at node 127 and will be stored by capacitor C_{dram} . This signal at node 127 is also on the gate of valve transistor M_{val} and, consequently, turns valve transistor M_{val} on or off.

[0035] In some embodiments, code-memory units 122 may each be implemented by a corresponding SRAM unit 131. Figure 7B depicts a SRAM unit 131 which may be used to implement a corresponding one of code-memory units 122 in the Figure 5A exposure encoder 115. In the Figure 7B embodiment, SRAM unit 131 comprises a pair of control switches (M_{ctrl1} and M_{ctrl2}) controlled by a corresponding signal (ϕ_{ctrl}). SRAM unit 131 may be connected between a corresponding exposure code signal

ϕ_{code} (e.g. one of exposure code signals ϕ_{code1} , ϕ_{code2} shown in Figure 5A) and a corresponding valve transistor M_{val} (e.g. one of valve transistors M_{val1} , M_{val2} shown in Figure 5A). When the control signal ϕ_{ctrl} is low, control transistors M_{ctrl1} and M_{ctrl2} are non-conducting and the node 133A output of SRAM unit 131 cannot be changed. However, when the control signal ϕ_{ctrl} is high, control transistors M_{ctrl1} and M_{ctrl2} turn on and the node 133A output of SRAM unit 131 tracks the exposure code signal ϕ_{code} . Once writing to SRAM unit 131 is finished, control signal ϕ_{ctrl} is pulled low again, so that output node 133A is no longer accessible. The signal at node 133A of SRAM unit 131 is also on the gate of valve transistor M_{val} and, consequently, may be used to turn valve transistor M_{val} on or off. At the potential cost of more circuit components, SRAM unit 131 may have the advantage (relative to DRAM unit 126) that SRAM unit 131 does not exhibit leakage and consequently, does not have to be regularly refreshed.

[0036] Code-memory units 122 are not limited to the DRAM or SRAM embodiments shown in Figures 7A and 7B. In some embodiments, other forms of memory units could be additionally or alternatively be used to implement code-memory units 122.

[0037] Referring back to Figure 5A, when pixel 115A is being exposed to light, and photodetector 118 is implemented by a photodiode, electron-hole pairs are generated in the pn -junction region of photodiode 118 once the incident photon energy is greater than the photodetector's bandgap. If photodiode 118 is reverse-biased with a voltage V , the photocurrent I_{PD} in diode 118 can be modelled by the following equation:

$$I_{\text{PD}} = R_{\text{PD}}LA + qA \left(\frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0} \right) \left[1 - \exp \left(\frac{qV}{nKT_A} \right) \right] \quad (1)$$

where R_{PD} is the photodiode sensitivity, K is Boltzmann's constant, L indicates the illumination at the photodiode surface, A is the cross-section area of the photodiode, T_A is the absolute temperature, $D_{n,p}$, $L_{n,p}$, n_{p0} and p_{n0} respectively denote the diffusion coefficient, diffusion length, minority carrier concentration in the p -type region, and the minority carrier concentration in n -type region.

[0038] Exposure code signals ϕ_{code1} , ϕ_{code2} , as gated by gating signal ϕ_{ctrl} , switch on/off valve transistors M_{val1} , M_{val2} . When the exposure code ϕ_{code1} is high and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (charge-storage capacitor C_1). Where exposure codes signals ϕ_{code1} , ϕ_{code2} are complementary to one

another, ϕ_{code1} being high corresponds to ϕ_{code2} being low. Accordingly, at the same time as valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (charge-storage capacitor C_1), ϕ_{ctrl} also causes code-memory unit 122B to transfer its complementary (low) exposure code ϕ_{code2} to the gate of valve transistor M_{val2} , so that valve transistor M_{val2} switches off and charge is prevented from flowing from photodetector 118 to charge-storage device 116B (charge-storage capacitor C_2). Conversely, when the exposure code ϕ_{code1} is low and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches off to prevent charge from flowing from photodetector 118 to charge-storage device 116A (charge-storage capacitor C_1). Where exposure codes signals ϕ_{code1} , ϕ_{code2} are complementary, this will correspond to ϕ_{code2} being high, turning on valve transistor M_{val2} , so that charge flows from photodetector 118 to charge-storage device 116B (charge-storage capacitor C_2).

[0039] At the conclusion of the exposure period (e.g. exposure period 38B of Figure 2B or exposure period 48B of Figure 2C), the signal ϕ_{tran} is used to turn on transfer transistors M_{tran} and to thereby transfer charges out from charge storage units 116 (charge-storage capacitors C) for readout by corresponding readout circuits 120A, 120B. In the illustrated embodiment of Figure 5A, each readout circuit 120A, 120B comprises a source follower formed by transistor M_{sf} when switch M_{sel} is on. In the specific case of the Figure 4B embodiment (where there is only one readout circuit 120A), charges from charge-storage capacitor C_2 (which may not be of interest) may be neglected and discarded when reset transistors M_{rst} switch on.

[0040] Code-memory units 122A, 122B may act to buffer their respective exposure code signals ϕ_{code1} , ϕ_{code2} . When ϕ_{ctrl} is pulled low, valve transistors M_{val1} , M_{val2} operate according to the voltage levels that are stored in the respective code-memory units 122A, 122B (e.g. in the respective capacitors C_{dram} of DRAM units 126 (Figure 7A)), regardless of the status of exposure code signals ϕ_{code1} , ϕ_{code2} . Due to the potential for leakage current I_{leak} in DRAM memory cells, it may be desirable in some embodiments to have a DRAM refresh period that is less than $T_{\text{refresh,max}}$, where $T_{\text{refresh,max}}$ is given by:

$$T_{\text{refresh,max}} = \frac{(V_{DD} - V_{th} - V_H)(C_{\text{DRAM}} + C_{\text{gate}} + C_{\text{drain}})}{I_{\text{leak}}} \quad (2)$$

where C_{DRAM} refers to C_{dram} of DRAM circuit 126 shown in Figure 7A, C_{gate} is the gate capacitance of valve transistors M_{val1} , M_{val2} (Figure 5A), V_{th} is the transistor threshold voltage, V_{H} is the essential voltage level to maintain logic high, and C_{drain} is the drain capacitance of the reset transistor M_{rst} .

[0041] Figure 5B is a circuit diagram of a circuit 124 for implementing the Figure 4C exposure encoder 215 for a particular pixel 215A in an APS implementation according to a particular embodiment. Circuit 124 may be used for a particular pixel 215A of the Figure 4A CIS exposure encoder 114. Circuit 124 may be suitably modified to provide any of the modifications discussed herein in connection with the Figure 4C exposure encoder 215. As discussed above in connection with Figures 4C and 4B, the Figure 5B circuit 124 differs from the Figure 5A circuit 121 because the Figure 5B circuit 124 is generalized to incorporate any suitable number N of exposure codes. In circuit 124 of the Figure 5B embodiment, charge-storage devices 116A, 116B, ... 116N (collectively, charge-storage devices 116) are respectively implemented by charge-storage capacitors C_1 , C_2 , ... C_N (collectively charge storages capacitors C). Charge-storage capacitors C act as charge-storage devices 116 to store charge transferred from photodetector 118 through valve transistors M_{val1} , M_{val2} , ... M_{valN} (collectively valve transistors, valve switches or, for brevity, switches M_{val}), where valve transistors M_{val1} , M_{val2} , ... M_{valN} act as switches to selectively switch charge accumulation between charge-storage capacitors C_1 , C_2 , ... C_N during each exposure sub-period.

[0042] In circuit 124 of the Figure 5B embodiment, code-memory units 122A, 122B, ... 122N may be respectively implemented by any suitable memory units. In some embodiments, code-memory units 122 may each be implemented by a corresponding DRAM unit 126 of the type shown in Figure 7A and described above in connection with circuit 121 of the Figure 5A embodiment. In some embodiments, code-memory units 122 may each be implemented by a corresponding SRAM unit 131 of the type shown in Figure 7B and described above in connection with circuit 121 of the Figure 5A embodiment. Code-memory units 122 are not limited to the DRAM or SRAM embodiments shown in Figures 7A and 7B. In some embodiments, other forms of memory units could be additionally or alternatively be used to implement code-memory units 122.

[0043] Photodetector 118 of the Figure 5B embodiment may operate in a manner substantially similar to photodetector 118 of the Figure 5A embodiment described

above. Exposure code signals $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$, as gated by gating signal ϕ_{ctrl} , switch on/off valve transistors $M_{\text{val1}}, M_{\text{val2}}, \dots M_{\text{valN}}$. When the exposure code ϕ_{code1} is high and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (charge-storage capacitor C_1). Conversely, if the exposure code ϕ_{code1} is low and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches off and charge does not flow from photodetector 118 to charge-storage device 116A (charge-storage capacitor C_1).

[0044] Similarly, if ϕ_{ctrl} causes a code-memory unit 122B, ... 122N to transfer its corresponding exposure code $\phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ to the gate of its corresponding valve transistor $M_{\text{val2}}, \dots M_{\text{valN}}$ and any of the corresponding exposure codes $\phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ is high, the corresponding valve transistor $M_{\text{val2}}, \dots M_{\text{valN}}$ switches on to let charges from photodetector 118 accumulate at the corresponding charge-storage device 116B, ... 116N (the corresponding charge-storage capacitor $C_2, \dots C_N$). Conversely, if ϕ_{ctrl} causes code-memory unit 122B, ... 122N to transfer its corresponding exposure code $\phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ to the gate of its corresponding valve transistor $M_{\text{val2}}, \dots M_{\text{valN}}$ and any of the corresponding exposure code $\phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ is low, then the corresponding valve transistor $M_{\text{val2}}, \dots M_{\text{valN}}$ switches off and charge does not flow from photodetector 118 to the corresponding charge-storage device 116B, ... 116N (the corresponding charge-storage capacitor $C_2, \dots C_N$).

[0045] As discussed above, the plurality of exposure codes ($\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$) may be independent of one another, such that, during any exposure sub-period, charge may be selectively accumulated in any combination of sub-combination of charge-storage devices 116 (charge-storage capacitors C). It may be desirable, in some embodiments, to select the exposure codes ($\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$) to ensure that charge is accumulated in at least one charge storage unit 116 (charge-storage capacitor C) during each exposure sub-period (chop). This may be done, for example, by using a dummy exposure code which is complementary to another exposure code. This dummy exposure code may not be of interest and may not be read out by any readout circuit 120.

[0046] At the conclusion of the exposure period (e.g. exposure period 38B of Figure 2B or exposure period 48B of Figure 2C), the signal ϕ_{tran} is used to turn on transfer

transistors M_{tran} and to thereby transfer charges out from charge storage units 116 (charge-storage capacitors C) for readout by corresponding readout circuits 120A, 120B, ... 120N (collectively, readout circuits 120), each of which may be the same as readout circuits 120A, 120B described above in connection with circuit 121 of Figure 5A. Charges accumulated in any charge-storage capacitor C that are not of interest may be neglected and discarded when reset transistors M_{rst} switch on.

[0047] Code-memory units 122A, 122B, ... 122N may act to buffer their corresponding exposure code signals ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} in a manner that is similar to code-memory units 122A, 122B of circuit 121 described above.

[0048] Figure 5C is a timing diagram which describes the operation of the Figure 5B exposure encoder circuit 124 for temporal exposure encoding over one frame cycle T_{frame} according to a particular embodiment. It will be appreciated that the Figure 5C timing diagram is also applicable to exposure encoder circuit 121 of Figure 5A, by selecting $N=2$. Figure 5C also shows a plot of the voltage (V) at node 128A of charge-storage device 116A (charge-storage capacitor C_1) over the frame cycle T_{frame} . The temporal exposure encoding starts with a reset period T_{rst} , during which the signals ϕ_{rst} and ϕ_{tran} are both high to reset the voltage level in charge-storage units 116 (charge-storage capacitors C) to V_{rst} . For the case of temporal exposure encoding shown in Figure 5C, during the exposure period T_{expo} , ϕ_{ctrl} stays high to pass exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} directly to valve transistors M_{val} .

[0049] Considering now, the plot of the voltage (V) at node 128A of charge-storage capacitor C_1 , during T_{expo} , for exposure sub-periods when ϕ_{code1} is high, valve-transistor M_{val1} is on, resulting in charge transfer from photodetector 118 to charge-storage capacitor C_1 (charge-storage device 116A) and a corresponding decrease in the voltage (V) at node 128A during the exposure sub-period. Conversely, during T_{expo} , for exposure sub-periods when ϕ_{code1} is low, valve transistor M_{val1} is off, there is no transfer of charge to node 128A and, consequently, the voltage (V) at node 128A remains constant during the exposure sub-period. Exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} may be synchronized at a rate of $(1/T_{\text{chop}})$, which may in turn set an allowable bit length of the exposure code sequence to be $(T_{\text{expo}}/T_{\text{chop}})$. When T_{expo} ends, exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} stop updating and ϕ_{tran} and ϕ_{sel} pull high, so that the node 128A voltage (V) is transferred, via transfer transistor M_{tran} , to readout circuit 120A, where this voltage is amplified by source follower M_{sf} and read out as the

accumulated output voltage V_{out1} . The signal ϕ_{sel} may pull high on a row-by-row basis in some embodiments, as described in more detail below.

[0050] Figure 5D is a timing diagram which describes the operation of the Figure 5A or Figure 5B exposure encoder circuit 124 for spatial-temporal exposure encoding in one frame cycle T_{frame} according to a particular embodiment. It will be appreciated that the Figure 5D timing diagram is also application to exposure encoder circuit 121 of Figure 5A, by selecting $N=2$. Figure 5D also shows a plot of the voltage (V) at node 128A of charge-storage device 116A (charge-storage capacitor C_1) over the frame cycle T_{frame} . In the Figure 5D embodiment, it is assumed that the array of pixels in CIS 114 includes M rows of pixels ($row_1, row_2, \dots, row_M$). For spatial-temporal exposure encoding, within T_{expo} , every row of pixels ($row_1, row_2, \dots, row_M$) is assigned a specific encoding period T_{code} within each exposure sub-period (T_{chop}) for its unique exposure code update. During each encoding period T_{code} , the control signal $\phi_{ctrl,row1}, \phi_{ctrl,row2}, \dots, \phi_{ctrl,rowM}$ for one corresponding row of pixels pulls high to allow the unique exposure codes $\phi_{code1}, \phi_{code2}, \dots, \phi_{codeN}$ for each pixel in that row to update/refresh the exposure codes $\phi_{code1}, \phi_{code2}, \dots, \phi_{codeN}$ stored in the corresponding code-memory units 122 of each pixel in the corresponding row. For example, in the illustrated embodiment of Figure 5D, in the first T_{code} , the signal $\phi_{ctrl,row1}$ pulls high, thereby updating the unique exposure codes $\phi_{code1}, \phi_{code2}, \dots, \phi_{codeN}$ for each pixel in row_1 . It should be realized that the exposure codes $\phi_{code1}, \phi_{code2}, \dots, \phi_{codeN}$ are unique for each pixel. However, because the exposure codes of the pixel array are updated on a row by row basis, each column of pixels may share the same exposure code bus (as will be explained in more detail below). Even where each column of pixels shares the same exposure code bus, a unique pixel may be addressed using control signals $\phi_{ctrl,row1}, \phi_{ctrl,row2}, \dots, \phi_{ctrl,rowM}$ for each row in the array. Figure 5D only depicts the exposure codes for a single column ($\phi_{code1, column1}, \phi_{code2, column1}, \dots, \phi_{codeN, column1}$), but it will be appreciated that each column bus will have a corresponding set of exposure codes $\{\phi_{code1}, \dots, \phi_{codeN}\}_{col_i}$ where $i=1, \dots, P$ and P is the number of columns in the array.

[0051] In this manner, within each exposure sub-period (i.e. within each T_{chop}), all pixels accomplish their exposure code update during a time period equal to the number of rows (M) times T_{code} . This exposure code update for each pixel is equivalent to applying a spatial exposure mask to the pixel array. Until the next exposure sub-period (T_{chop}) starts, the pixel array exposure for each pixel is

programmed by the applied exposure mask (i.e. each pixel 215A in the pixel array is programmed by its corresponding exposure codes φ_{code1} , φ_{code2} , ... φ_{codeN} (stored in its corresponding code-memory units 122)).

[0052] In some embodiments, during T_{expo} , when other rows of pixels are being processed, each individual pixel may operate according to its own stored exposure codes (i.e. exposure codes φ_{code1} , φ_{code2} , ... φ_{codeN} stored in its corresponding code-memory units 122) regardless of any changes in the signals $\varphi_{code1, column1}$, $\varphi_{code2, column1}$, ... $\varphi_{codeN, column1}$. The time period during which each pixel may operate according its own unique exposure codes (as stored in its code-memory units 122) may be referred to as T_{memory} . In the Figure 5D embodiment, it can be observed that each row has a T_{memory} of a slightly different duration (i.e. $T_{memory, row1}$, $T_{memory, row2}$, ... $T_{memory, rowM}$) and that the maximum time-length difference (i.e. between $T_{memory, row1}$ and $T_{memory, rowM}$) is $(M-1)T_{code}$. This is a suitable implementation, for many applications, such as global shuttering applications and/or where the smallest T_{memory} ($T_{memory, rowM}$) is significantly greater than the number of rows (M) times T_{code} (i.e. $T_{memory, rowM} \gg M(T_{code})$). In some embodiments (not shown in Figure 5D), T_{memory} may be made equal for each row by permitting T_{memory} for rows 2, 3, ...M to extend into the next exposure sub-period/chop (e.g. until the exposure codes for the corresponding row are updated at the time T_{code} for the corresponding row in the next exposure sub-period (T_{chop})). In such embodiments, the start and end times of T_{memory} are offset for each row by a duration T_{code} for each pair of adjacent rows between row_1 and row_M . This is a suitable implementation for many applications, such as rolling shutter schemes, where the exposure is row-by-row based, for example.

[0053] The maximum number of spatial exposure masks that can be applied during one T_{expo} and in one frame cycle T_{frame} is thus T_{expo}/T_{chop} . Other than for the independent programming of each pixel, during each exposure sub-period, the exposure, readout and reset of pixel 115A shown in Figure 5D works in a manner similar to that described above for Figure 5C. In some embodiments, such as global shuttering embodiments for example, where the T_{memory} times for the second and subsequent rows are permitted to extend into subsequent exposure sub-periods (chops), it may be desirable to have the codes applied in the last exposure sub-period T_{chop} of each exposure period T_{expo} be dummy codes (or padded codes), so that all rows have equal T_{memory} times for all exposure masks of interest. For example, all

exposure codes $\phi_{\text{code}1}$, $\phi_{\text{code}2}$, ... $\phi_{\text{code}N}$ (except, possibly, for one exposure code per pixel which is not of interest) for all pixels may be set to have exposure off (dummy codes) during the last exposure sub-period T_{chop} of each exposure period T_{expo} . In some such embodiments, the one exposure code per pixel which is not of interest, may be a dummy exposure code which is set to exposure on and which is used to sink charge from photodetector 118, when all of the exposure codes for the exposure codes of interest are set to exposure off, thereby preventing charge from being “locked” in photodetector 118. In rolling shutter embodiments, these dummy codes in the last sub-period may not be required, since pixels may be exposed and/or read on a row-by-row basis.

[0054] Figure 6A is a circuit diagram of a circuit 131 for implementing the Figure 4B exposure encoder 115 for a particular pixel 115A in a CTIA implementation according to a particular embodiment. Circuit 131 may be used for a particular pixel 215A of the Figure 4A CIS exposure encoder 114. Circuit 134 may be suitably modified to provide any of the modifications discussed herein in connection with the Figure 4C exposure encoder 215. In circuit 131 of the Figure 6A embodiment, charge-storage devices 116A, 116B, (collectively, charge-storage devices 116) are implemented by charge-storage capacitors C_1 , C_2 (collectively, charge-storage capacitors C), Charge-storage capacitors C act as charge-storage devices 116 to store charge transferred from photodiode 118 through valve transistors $M_{\text{val}1}$, $M_{\text{val}2}$ (collectively valve transistors, valve switches or, for brevity, switches M_{val}), where valve transistors $M_{\text{val}1}$, $M_{\text{val}2}$ act as switches to selectively switch charge accumulation between charge-storage capacitors C_1 , C_2 during each exposure sub-period. In Figure 6A and the description below, exposure code signals $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$ may be generalized and referred to as exposure code signals $\phi_{\text{code}1}$, $\phi_{\text{code}2}$.

[0055] In circuit 131 of the Figure 6A embodiment, code-memory units 122A, 122B (collectively, code-memory units 122) may be respectively implemented by any suitable memory units. In some embodiments, code-memory units 122 may each be implemented by a corresponding DRAM unit 126 of the type shown in Figure 7A and described above in connection with circuit 121 of the Figure 5A embodiment. In some embodiments, code-memory units 122 may each be implemented by a corresponding SRAM unit 131 of the type shown in Figure 7B and described above in connection with circuit 121 of the Figure 5A embodiment. Code-memory units 122 are not limited

to the DRAM or SRAM embodiments shown in Figures 7A and 7B. In some embodiments, other forms of memory units could be additionally or alternatively be used to implement code-memory units 122.

[0056] Circuit 131 of the Figure 6A embodiment, also comprises CTIA units 135A, 135B, (collectively, CTIA units 135), each of which comprises a corresponding TIA amplifier 136A, 136B (collectively, TIA amplifiers 136) for amplifying the charge across its corresponding charge-storage capacitor C_1 , C_2 . In the illustrated embodiment, photodetector 118 is connected to each charge storage capacitor C_1 , C_2 via corresponding valve transistors M_{val1} , M_{val2} . Charge storage capacitors C_1 , C_2 may be used for charge integration and may be reset using reset switches M_{rst} under the control of reset signal ϕ_{rst} .

[0057] The pixel exposure period T_{expo} may be divided into exposure sub-periods (chops) with temporal duration T_{chop} . In each exposure sub-period (T_{chop}), charges generated by photodetector 118 are selectively transferred to charge storage capacitors C_1 , C_2 depending on whether their corresponding valve transistors M_{val1} , M_{val2} are on. Exposure code signals ϕ_{code1} , ϕ_{code2} , as gated by gating signal ϕ_{ctrl} , switch on/off valve transistors M_{val1} , M_{val2} . When exposure code ϕ_{code1} is high and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (i.e. charge-storage capacitor C_1). Where exposure codes signals ϕ_{code1} , ϕ_{code2} are complementary to one another, ϕ_{code1} being high corresponds to ϕ_{code2} being low. Accordingly, at the same time as valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (charge-storage capacitor C_1), ϕ_{ctrl} also causes code-memory unit 122B to transfer its complementary (low) exposure code ϕ_{code2} to the gate of valve transistor M_{val2} , so that valve transistor M_{val2} switches off and charge is prevented from flowing from photodetector 118 to charge-storage device 116B (charge-storage capacitor C_2). Conversely, when the exposure code ϕ_{code1} is low and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches off to prevent charge from flowing from photodetector 118 to charge-storage device 116A (charge-storage capacitor C_1). Where exposure codes signals ϕ_{code1} , ϕ_{code2} are complementary, this will correspond to ϕ_{code2} being high, turning on valve

transistor M_{val2} , so that charge flows from photodetector 118 to charge-storage device 116B (charge-storage capacitor C_2).

[0058] Each trans-impedance amplifier (TIA) 136A, 136B, biased by V_{bp} and V_{bn} , controls the transfer speed at its input node 140A, 140B to ensure that charge accumulated in photodetector 118 is fully transferred to TIA amplifiers 136A, 136B. Consequently, charge generated by photodetector 118 accumulates solely in charge-storage devices 116A, 116B (i.e. on charge-storage capacitors C_1 , C_2) during the exposure period T_{exp} . For amplifiers 136A, 136B to settle (i.e. to ensure that charge is fully transferred to CTIA 135A, 135B) within T_{chop} , their gain-bandwidth product may preferably be greater than:

$$GBW = \frac{5}{\pi T_{chop}} \cdot \frac{C_{int} + C_{pd}}{C_{int}} \quad (3)$$

where C_{int} represents the charge-storage capacitor (C_1 , C_2) and C_{pd} is the self-capacitance of photodetector 118. To read out the pixel, pixel select switches M_{sel} may be closed when signal ϕ_{sel} is pulled up. Output signals, V_{out1} , V_{out2} reflect the voltage levels across charge storage capacitors C_1 , C_2 and can be calculated, for the $N=2$ case, according to:

$$V_{out(1,2)} = \frac{I_{ph}}{C_{int}(1 - \frac{C_{int} - C_{pd}}{A_g C_{int}})} + V_{off} \quad (4)$$

where V_{th} , A_g , and V_{off} denote the NMOS threshold voltage, the amplifier gain, and the offset voltage, respectively. With a constant load capacitance C_{load} , the pixel read noise can be estimated as:

$$V_{read,noise}^2 = \frac{\alpha K T}{(\frac{1}{r_{out} g_m} + \frac{C_{int}}{C_{int} + C_{pd}})(C_{load} + \frac{C_{int} C_{pd}}{C_{int} + C_{pd}})} \quad (5)$$

where α , r_{out} and g_m are the amplifier fitting coefficient (ranging from 2/3 to 2), the amplifier output resistance, and the amplifier transconductance, respectively.

[0059] For the $N=2$ case, the switching operation of valve transistors M_{val1} and M_{val2} is controlled by exposure code signals ϕ_{code1} and ϕ_{code2} (which may, but need not necessarily, be complementary to one another). As summarized in Table I for the case of complementary exposure code signals, different ϕ_{code1} and ϕ_{code2} combinations turn valve transistors M_{val1} and M_{val2} on/off accordingly and control the

charge transfer direction (to C_1 or to C_2) during the temporal exposure encoding.

Table I

THE EXPOSURE CODE ARRANGEMENTS FOR M_1 AND M_2 OPERATIONS						
	Φ_{code1}	Φ_{code2}	Φ_{code1}	Φ_{code2}	Φ_{code1}	Φ_{code2}
Exposure code	1	0	0	1	X	X
Φ_{ctrl}	1		1		0	
M_{val1}	Close		Open		Determined by code-memory unit 122A	
M_{val2}	Open		Close		Determined by code-memory unit 122B	

For spatial-temporal exposure encoding in the $N=2$ situation illustrated in Table 1, as each pixel stores its unique exposure codes, two code-memory units 122A, 122B may be used to store Φ_{code1} and Φ_{code2} signals. In the illustrated Figure 6A embodiment, when the control signal Φ_{ctrl} is low, valve transistors M_{val1} and M_{val2} maintain their on/off status according to the signals buffered in code-memory units 122A, 122B, irrespective of the status of Φ_{code1} and Φ_{code2} .

[0060] Where code-memory units 122 are implemented by DRAM units 126A, 126B (see DRAM 126 of Figure 7A), due to potential leakage current I_{leak} , charges stored in DRAM units 126A, 126B may leak and cause potentially problematic logic shift. It is therefore desirable in some circumstances to refresh DRAM units 126A, 126B to maintain their stored logic level. In some embodiments, DRAM units 126A, 126B may be refreshed with a period less than $T_{refresh,max}$ defined as in equation (1) above, where C_{gate} , and C_{drain} represent gate capacitance of valve transistors M_{val1} , M_{val2} and drain capacitance of the transistor M_{dram} (Figure 7A). During spatial-temporal exposure encoding, T_{chop} may be selected to be smaller than $T_{refresh,max}$ to ensure effective (e.g. leak-free) storage of exposure codes.

[0061] Figure 6B is a circuit diagram of a circuit 134 for implementing the Figure 4C exposure encoder 215 for a particular pixel 215A in a CTIA implementation according

to a particular embodiment. Circuit 134 may be used for a particular pixel 215A of the Figure 4A CIS exposure encoder 114. Circuit 134 may be suitably modified to provide any of the modifications discussed herein in connection with the Figure 4C exposure encoder 215. As discussed above in connection with Figures 4C and 4B, the Figure 6B circuit 134 differs from the Figure 6A circuit 131 because the Figure 6B circuit 134 is generalized to incorporate any suitable number N of exposure codes. In circuit 134 of the Figure 6B embodiment, charge-storage devices 116A, 116B, ... 116N (collectively, charge-storage devices 116) are implemented by charge-storage capacitors $C_1, C_2, \dots C_N$ (collectively, charge-storage capacitors C). Charge-storage capacitors C act as charge-storage devices 116 to store charge transferred from photodiode 118 through valve transistors $M_{val1}, M_{val2}, \dots M_{valN}$ (collectively valve transistors, valve switches or, for brevity, switches M_{val}), where valve transistors $M_{val1}, M_{val2}, \dots M_{valN}$ act as switches to selectively switch charge accumulation between charge-storage capacitors $C_1, C_2, \dots C_N$ during each exposure sub-period.

[0062] In circuit 134 of the Figure 6B embodiment, code-memory units 122A, 122B, ... 122N may be respectively implemented by any suitable memory units. In some embodiments, code-memory units 122 may each be implemented by a corresponding DRAM unit 126 of the type shown in Figure 7A and described above in connection with circuit 121 of the Figure 5A embodiment. In some embodiments, code-memory units 122 may each be implemented by a corresponding SRAM unit 131 of the type shown in Figure 7B and described above in connection with circuit 121 of the Figure 5A embodiment. Code-memory units 122 are not limited to the DRAM or SRAM embodiments shown in Figures 7A and 7B. In some embodiments, other forms of memory units could be additionally or alternatively be used to implement code-memory units 122.

[0063] Circuit 134 of the Figure 6B embodiment, also comprises CTIA units 135A, 135B, ... 135N (collectively, CTIA units 135), each of which comprises a corresponding TIA amplifier 136A, 136B, ... 136N (collectively, amplifiers 136) for amplifying the charge across its corresponding charge-storage capacitor $C_1, C_2, \dots C_N$. In the illustrated embodiment, photodetector 118 is connected to each charge storage capacitor $C_1, C_2, \dots C_N$ via corresponding valve transistors $M_{val1}, M_{val2}, \dots M_{valN}$. Charge storage capacitors $C_1, C_2, \dots C_N$ may be used for charge integration and may be reset using reset switches M_{rst} under the control of reset signal ϕ_{rst} .

[0064] The pixel exposure period T_{expo} may be divided into exposure sub-periods (chops) with temporal duration T_{chop} . In each exposure sub-period (T_{chop}), charges generated by photodetector 118 are transferred to charge storage capacitors C_1 , C_2 , ... C_N depending on whether their corresponding valve transistors M_{val1} , M_{val2} , ... M_{valN} are on. Exposure code signals ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} , as gated by gating signal ϕ_{ctrl} , switch valve transistors M_{val1} , M_{val2} , ... M_{valN} on/off. When exposure code ϕ_{code1} is high and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches on to let charges from photodetector 118 accumulate at charge-storage device 116A (charge-storage capacitor C_1). Conversely, if the exposure code ϕ_{code1} is low and ϕ_{ctrl} causes code-memory unit 122A to transfer its corresponding exposure code ϕ_{code1} to the gate of valve transistor M_{val1} , valve transistor M_{val1} switches off and charge does not flow from photodetector 118 to charge-storage device 116A (charge-storage capacitor C_1).

[0065] Similarly, if ϕ_{ctrl} causes a code-memory unit 122B, ... 122N to transfer its corresponding exposure code ϕ_{code2} , ... ϕ_{codeN} to the gate of its corresponding valve transistor M_{val2} , ... M_{valN} and any of the corresponding exposure codes ϕ_{code2} , ... ϕ_{codeN} is high, the corresponding valve transistor M_{val2} , ... M_{valN} switches on to let charges from photodetector 118 accumulate at the corresponding charge-storage device 116B, ... 116N (the corresponding charge-storage capacitor C_2 , ... C_N). However, if ϕ_{ctrl} causes code-memory unit 122B, ... 122N to transfer its corresponding exposure code ϕ_{code2} , ... ϕ_{codeN} to the gate of its corresponding valve transistor M_{val2} , ... M_{valN} and any of the corresponding exposure code ϕ_{code2} , ... ϕ_{codeN} is low, then the corresponding valve transistor M_{val2} , ... M_{valN} switches off and charge does not flow from photodetector 118 to the corresponding charge-storage device 116B, ... 116N (the corresponding charge-storage capacitor C_2 , ... C_N).

[0066] As discussed above, the plurality of exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) may be independent of one another, such that, during any exposure sub-period, charge may be selectively accumulated in any combination of sub-combination of charge-storage devices 116 (charge-storage capacitors C). It may be desirable, in some embodiments, to select the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) to ensure that charge is accumulated in at least one charge storage unit 116 (charge-storage capacitor C) during each exposure sub-period (chop). This may be done, for example,

by using a dummy exposure code which is complementary to another exposure code. This dummy exposure code may not be of interest and may not be read out by any readout circuit 120.

[0067] Figure 6C is a timing diagram which describes the operation of the Figure 6B exposure encoder circuit 134 for temporal exposure encoding over one frame cycle T_{frame} according to a particular embodiment. It will be appreciated that the Figure 6C timing diagram is also applicable to exposure encoder circuit 131 of Figure 6A, by selecting $N=2$. Figure 6C also shows a plot of the voltage (V) at node 138A (the output of TIA 136A – see Figure 6B) over the frame cycle T_{frame} . In temporal exposure encoding, all pixels are guided by the same exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} . Starting with pixel reset (T_{rst}), the voltage level in photodetector 118, charge-storage units 116 (charge-storage capacitors C) and nodes 138A, 138B, ... 138N are reset to V_{rst} . During the exposure period (T_{expo}), ϕ_{ctrl} stays high, in the case of temporal exposure encoding, to pass exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} directly to valve transistors M_{val1} , M_{val2} , ... M_{valN} , thereby turning valve transistors M_{val1} , M_{val2} , ... M_{valN} on/off.

[0068] Considering now, the plot of the node 138A voltage (V), during T_{expo} , for exposure sub-periods when ϕ_{code1} is high, valve transistor M_{val1} is on, resulting in charge transfer from photodetector 118 to charge-storage capacitor C_1 (charge-storage device 116A), a corresponding decrease in the voltage at node 140A and a corresponding increase in the voltage (V) at node 138A due to the inverting amplification effect of TIA 136A. Conversely, during T_{expo} , for exposure sub-periods when ϕ_{code1} is low, valve transistor M_{val1} is off, and so there is no transfer of charge to node 138A and the voltage (V) at node 138A remains constant during the exposure sub-period. Exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} may be synchronized at a rate of $(1/T_{\text{chop}})$, which may in turn set the length of each exposure code to be $(T_{\text{expo}}/T_{\text{chop}})$. As charges are distributed into CTIA units 135A, 135B, ... 135N, the voltage levels at nodes 138A, 138B, ... 138N increase. Once T_{expo} ends, exposure codes ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN} stop updating. The pixel selection signal (ϕ_{sel}) is then pulled up to read out the final output V_{out1} , V_{out2} , ... V_{outN} . Within the readout period (T_{read}), the voltages at nodes 138A, 138B, ... 138N remain unchanged until ϕ_{rst} is pulled up again to start the next frame.

[0069] Figure 6D is a timing diagram which describes the operation of the Figure 6B

exposure encoder circuit 134 for spatial-temporal exposure encoding in one frame cycle T_{frame} according to a particular embodiment. . It will be appreciated that the Figure 6D timing diagram is also application to exposure encoder circuit 131 of Figure 6A, by selecting $N=2$. Figure 6D also shows a plot of the voltage (V) at node 138A (Figure 6B) of charge-storage device 116A (charge storage capacitor C_1) over the frame cycle T_{frame} . In the Figure 6D embodiment, it is assumed that the array of pixels in CIS 114 includes M rows of pixels ($\text{row}_1, \text{row}_2, \dots \text{row}_M$). For spatial-temporal exposure encoding, within T_{expo} , each row of pixels ($\text{row}_1, \text{row}_2, \dots \text{row}_M$) is assigned a specific encoding period T_{code} within each exposure sub-period (T_{chop}) for its unique exposure code update. During each encoding period T_{code} , the control signal $\phi_{\text{ctrl,row1}}, \phi_{\text{ctrl,row2}}, \dots \phi_{\text{ctrl,rowM}}$ for one corresponding row of pixels pulls high to allow the unique exposure codes $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ for each pixel in that row to update/refresh the exposure codes $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ stored in the corresponding code-memory units 122 of each pixel in the corresponding row. For example, in the illustrated embodiment of Figure 6D, in the first T_{code} , the signal $\phi_{\text{ctrl,row1}}$ pulls high, thereby updating the unique exposure codes $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ for each pixel in row_1 . It should be realized that the exposure codes $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ are unique for each pixel. However, because the exposure codes of the pixel array are updated on a row by row basis, each column of pixels may share the same exposure code bus (as will be explained in more detail below). Even where each column of pixels shares the same exposure code bus, a unique pixel may be addressed using control signals $\phi_{\text{ctrl,row1}}, \phi_{\text{ctrl,row2}}, \dots \phi_{\text{ctrl,rowM}}$ for each row in the array. Figure 6D only depicts the exposure codes for a single column ($\phi_{\text{code1, column1}}, \phi_{\text{code2, column1}}, \dots \phi_{\text{codeN, column1}}$), but it will be appreciated that each column bus will have a corresponding set of exposure codes $\{\phi_{\text{code1}}, \dots \phi_{\text{codeN}}\}_{\text{col}i}$ where $i=1, \dots P$ and P is the number of columns in the array.

[0070] In this manner, within each exposure sub-period (i.e. within each T_{chop}), all pixels accomplish their exposure codes update during a time period equal to the number of rows (M) times T_{code} . This exposure code update for each pixel is equivalent to applying a spatial exposure mask to the pixel array. Until the next exposure sub-period (T_{chop}) starts, the pixel array exposure for each pixel is exposed based on the applied exposure mask (i.e. each pixel 215A in the pixel array is programmed by its corresponding exposure codes $\phi_{\text{code1}}, \phi_{\text{code2}}, \dots \phi_{\text{codeN}}$ (stored in its corresponding code-memory units 122)).

[0071] In some embodiments, during T_{expo} , when other rows of pixels are being processed, each individual pixel may operate according to its own stored exposure codes (i.e. exposure codes φ_{code1} , φ_{code2} , ... φ_{codeN} stored in its corresponding code-memory units 122) regardless of any changes in the signals $\varphi_{\text{code1, column1}}$, $\varphi_{\text{code2, column1}}$, ... $\varphi_{\text{codeN, column1}}$. The time period during which each pixel may operate according its own unique exposure codes (as stored in its code-memory unit 122) may be referred to as T_{memory} . In the Figure 6D embodiment, it can be observed that each row has a T_{memory} of a slightly different duration (i.e. $T_{\text{memory, row1}}$, $T_{\text{memory, row2}}$, ... $T_{\text{memory, rowM}}$) and that the maximum time-length difference (i.e. between $T_{\text{memory, row1}}$ and $T_{\text{memory, rowM}}$) is $(M-1)T_{\text{code}}$. This is a suitable implementation, for many applications, such as global shuttering applications and/or where the smallest T_{memory} ($T_{\text{memory, rowM}}$) is significantly greater than the number of rows (M) times T_{code} (i.e. $T_{\text{memory, rowM}} \gg M(T_{\text{code}})$). In some embodiments (not shown in Figure 6D), T_{memory} may be made equal for each row by permitting T_{memory} for rows 2, 3, ...M to extend into the next exposure sub-period/chop (e.g. until the exposure codes for the corresponding row are updated at the time T_{code} for the corresponding row in the next exposure sub-period (T_{chop})). In such embodiments, the start and end times of T_{memory} are offset for each row by a duration T_{code} for each pair of adjacent rows between row₁ and row_M. This is a suitable implementation for many applications, such as rolling shutter schemes, where exposure is row-by-row based, for example.

[0072] The maximum number of spatial exposure masks that can be applied during one T_{expo} and in one frame cycle T_{frame} is thus $T_{\text{expo}}/T_{\text{chop}}$. Other than for the independent programming of each pixel, during each exposure sub-period, the exposure, readout and reset of pixel 215A shown in Figure 6D works in a manner similar to that described above for Figure 6C. In some embodiments, such as global shuttering embodiments for example, where the T_{memory} times for the second and subsequent rows are permitted to extend into subsequent exposure sub-periods (chops), it may be desirable to have the codes applied in the last exposure sub-period T_{chop} of each exposure period T_{expo} be dummy codes (or padded codes), so that all rows have equal T_{memory} times for all exposure masks of interest. For example, all exposure codes φ_{code1} , φ_{code2} , ... φ_{codeN} (except, possibly, for one exposure code per pixel which is not of interest) for all pixels may be set to have exposure off (dummy codes) during the last exposure sub-period T_{chop} of each exposure period T_{expo} . In some such embodiments, the one exposure code per pixel which is not of interest,

may be a dummy exposure code which is set to exposure on and which is used to sink charge from photodetector 118, when all of the exposure codes for the exposure codes of interest are set to exposure off, thereby preventing charge from being “locked” in photodetector 118. In rolling shutter embodiments, these dummy codes in the last sub-period may not be required, since pixels may be exposed and/or read on a row-by-row basis.

[0073] Figure 8 is a schematic depiction of a CIS system architecture 300 according to a particular embodiment, which shows a CIS pixel array 314. Each pixel 324 of CIS system 300 may be implemented according to any of the pixel (exposure encoder) embodiments described herein (e.g. Figures 4, 5 and 6). Pixels 324 may be individually referred to by their row and column number – e.g. any particular pixel 324 may be referred to as pixel $324_{i,j}$ where $1 \leq i \leq M$ is the pixel row number and $1 \leq j \leq P$ is the pixel column number. CIS system 300 of the illustrated embodiment comprises a number of notional controllers, comprising exposure code controller 310, image signal processing controller 312, code memory controller 316 and row scanner 318 and code memory controller 316. In practice, one or more of controllers 310, 312, 316, 318 may be implemented by the same physical or logical digital (data) processor which may be operating under the control of suitable software.

[0074] Exposure code controller 310 is connected to pixel array 314 via a series of column busses 310A. Exposure code controller 310 may operate under the control of suitable exposure control software (e.g. application software) 308 to deliver the various exposure codes $\varphi_{code1}, \varphi_{code2}, \dots, \varphi_{codeN}$ to each pixel 324. Specifically, each column bus 310A connected to exposure code controller 310 carries a series of exposure codes $\varphi_{code1}, \varphi_{code2}, \dots, \varphi_{codeN}$ during each T_{code} , where the exposure codes $\varphi_{code1}, \varphi_{code2}, \dots, \varphi_{codeN}$ for each column bus 310A are specific to a particular pixel 314. In Figure 5D and 6D, the notation that is used for the exposure codes on each column bus is exposure codes $\varphi_{code1,coli}, \varphi_{code2,coli}, \dots, \varphi_{codeN,coli}$ where $1 \leq i \leq P$ is the index of column bus 310A. The particular pixel that is selected to be programmed in each T_{code} is selected by a control signal $\varphi_{ctrl,rowj}$ output on row-select lines 316A by code memory controller 316, where $1 \leq j \leq M$ is the index of row-select lines 316A. As discussed above, the rows of pixels 324 in array 314 are programmed with exposure codes on a row by row basis during successive T_{codes} during each sub-period T_{chop} .

[0075] Once all of the pixels 324 of array 314 are coded with their corresponding

unique exposure codes φ_{code1} , φ_{code2} , ... φ_{codeN} , in each sub-period (chop), exposure takes place for that sub-period (possibly extending into a subsequent chop as discussed above). At the conclusion of all of the sub-periods corresponding to an exposure period T_{expo} , the individual pixels are read out. This occurs in a manner similar to that of programming the pixels with column busses 312A that are connected to each pixel 324 in a corresponding column and row scanner 318, which outputs row-select signals $\varphi_{\text{sel,rowj}}$ onto row-select lines 318A, where $1 \leq j \leq M$ is the index of row-select lines 318A. For each successive row $1 \leq j \leq M$, the N output voltages V_{out1} , V_{out2} , ... V_{outN} of each pixel 324 in the row are output onto a corresponding column bus 312A and provided to image signal processor 312 and thereafter to image memory 320 (which may be accessible to a CPU, GPU or display (not shown in Figure 8)).

[0076] Figure 9A is a flow chart schematically illustrating a method 400 for operating the Figure 8 CIS system 300 according to a particular embodiment. Method 400 begins in block 402 which involves initiating the pixel of the CIS sensor 114. This CIS sensor initiation may comprise a standard CIS initiation as is known in the art. Method 400 then enters a frame loop which is performed once every T_{frame} (see Figures 5 and 6). The first procedure of the frame loop in the illustrated embodiment is the block 404 reset procedure, where φ_{rst} (for each pixel) is pulled high (see Figures 5 and 6) and the voltages at photodetector 118, charge-storage units 116 (charge-storage capacitors C) and the corresponding nodes of the exposure encoder circuit are reset to V_{rst} . Method 400 then proceeds to block 406 which involves an inquiry into whether the current frame is to be a non-intermittent (continuous) exposure frame. If the block 406 inquiry is positive, then method 400 proceeds to block 408 where a continuous exposure operation is performed. The block 408 continuous exposure, an example of which is shown in Figure 2A, is well known in the art.

[0077] However, if the block 406 inquiry is negative, then method 400 proceeds to block 410, where an inquiry is made as to whether the intermittent exposure is to be a temporal exposure encoding (block 412) or a spatial-temporal exposure encoding (block 414). Each of temporal encoding block 412 and spatial-temporal encoding block 414 is explained in more detail in Figures 9B and 9C. At the conclusion of the exposure in 408, 412 or 414, the block 416 inquiry is positive and method 400 proceeds to block 418, where a read operation is performed at the end of the frame.

The block 418 read operation may involve using the ϕ_{sel} signal for each row the pixel array to read the output voltages that have accumulated in the charge-storage devices during the frame. These output voltages may be read onto the read column busses 412A (Figure 8) on a row-by-row basis, as discussed above. At the conclusion of the block 418 read operation, method 400 proceeds to block 420, where method 400 either loops back to block 404 to image another frame or ends at block 422.

[0078] Figure 9B is a flow chart schematically illustrating a method 450 for performing the block 412 temporal exposure encoding procedure of the Figure 9A method 400 according to a particular embodiment. Method 450 starts in block 452 and then proceeds to perform a pair of procedures 454, 456 for each sub-period (chop) during the exposure period T_{expo} . The first exposure sub-period involves performing blocks 454A and 456A. In block 454A, exposure code controller 310 (Figure 8) updates the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) for the first chop for each column a1, b1, c1 ... (for all P columns in the array). For temporal exposure encoding, the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) for each pixel (i.e. in each column and each row) are the same in each chop. Consequently, the ϕ_{ctrl} signal may be used to program all rows (and all columns) in the pixel array at the same time in block 454A – i.e. it is not necessary to use ϕ_{ctrl} on a row-by-row basis for temporal encoding. At the conclusion of block 454A, the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) are programmed into the code-memory units 122 of each pixel. Method 450 then proceeds to block 456A, which involves exposure under the the exposure codes (ϕ_{code1} , ϕ_{code2} , ... ϕ_{codeN}) programmed in block 454A for the current exposure sub-period (chop). For the second and subsequent exposure sub-periods (chops) in the method 450 frame, the procedures of blocks 454B, ... 454n and blocks 456B, ... 456n are the substantially the same as blocks 454A and 456A for the first exposure sub-period (chop). In the illustrated embodiment, there are n chops (exposure sub-periods) in the frame. At the conclusion of the n exposure sub-periods, method 450 ends in block 458.

[0079] Figure 9C is a flow chart schematically illustrating a method 480 for performing the block 414 spatial-temporal exposure encoding procedure of the Figure 9A method 400 according to a particular embodiment. Method 480 starts in block 482 and then proceeds to perform a number of procedures 484, 486, 488, 490 for each sub-period (chop) during the exposure period T_{expo} . The first exposure sub-period involves performing blocks 484A, 486A, 488A, 490A. In block 484A, pixel memory

controller 316 (Figure 8) selects a row j of pixels and sets the signal $\varphi_{ctrl,rowj}$ to be high for the selected row j of pixels. In block 486A, exposure code controller 310 (Figure 8) updates the exposure codes (φ_{code1} , φ_{code2} , ... φ_{codeN}) for the first chop for each column $a1$, $b1$, $c1$... (for all P columns in the array) in the currently select row j . For spatial-temporal encoding, the exposure codes (φ_{code1} , φ_{code2} , ... φ_{codeN}) are unique for each individual column in each block 486A. This results in unique exposure codes (φ_{code1} , φ_{code2} , ... φ_{codeN}) for each pixel in the CIS array. After block 486A, method 480 proceeds to block 488A, where an inquiry is performed as to whether the currently selected row j is the last row to have its exposure codes (φ_{code1} , φ_{code2} , ... φ_{codeN}) updated. If the block 488A inquiry is negative, then method 480 loops back to block 486A to select another row for programming. If the block 488A inquiry is positive, then the mask M_1 corresponding to the first exposure sub-period (chop) is complete and method 480 proceeds to block 490A which involves exposure for the first exposure sub-period (chop) under the exposure codes of the first mask M_1 . For the second and subsequent exposure sub-periods (chops) in the method 480 frame, the procedures of blocks 484B, ... 484n, blocks 486B,... 486n, blocks 488B, ... 488n and blocks 490B, ... 490n are the substantially the same as blocks 484A, 486A, 488A, 490A for the first exposure sub-period (chop). In the illustrated embodiment, there are n chops (exposure sub-periods) in the frame. At the conclusion of the n exposure sub-periods, method 480 ends in block 492.

Interpretation of Terms

[0080] Unless the context clearly requires otherwise, throughout the description and the claims:

- “comprise”, “comprising”, and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to”;
- “connected”, “coupled”, or any variant thereof, means any connection or coupling, either direct or indirect, between two or more elements; the coupling or connection between the elements can be physical, logical, or a combination thereof;
- “herein”, “above”, “below”, and words of similar import, when used to describe this specification, shall refer to this specification as a whole, and not to any particular portions of this specification;

- “or”, in reference to a list of two or more items, covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list;
- the singular forms “a”, “an”, and “the” also include the meaning of any appropriate plural forms;
- components are described or recited herein as being selectively connectable to one another. Such selective connections may refer to selectively conducting connections where in one state, electric conductivity is possible between the components, and in another state, electric conductivity is possible between the components. Such selective connections may be made, for example, by semiconductor switches (e.g. transistor-based switches or other semiconductor-based switches), where the components may maintain physical connection (via the semiconductor switch), but may or may not be conductively connected depending on the state of the switch.

[0081] Embodiments of the invention may be implemented using specifically designed hardware, configurable hardware, programmable data processors configured by the provision of software (which may optionally comprise “firmware”) capable of executing on the data processors, special purpose computers or data processors that are specifically programmed, configured, or constructed to perform one or more steps in a method as explained in detail herein and/or combinations of two or more of these. Examples of specifically designed hardware are: logic circuits, application-specific integrated circuits (“ASICs”), large scale integrated circuits (“LSIs”), very large scale integrated circuits (“VLSIs”), and the like. Examples of configurable hardware are: one or more programmable logic devices such as programmable array logic (“PALs”), programmable logic arrays (“PLAs”), and field programmable gate arrays (“FPGAs”). Examples of programmable data processors are: microprocessors, digital signal processors (“DSPs”), embedded processors, graphics processors, math co-processors, general purpose computers, server computers, cloud computers, mainframe computers, computer workstations, and the like. For example, one or more data processors in a control circuit for a device may implement methods as described herein by executing software instructions in a program memory accessible to the processors.

[0082] Processing may be centralized or distributed. Where processing is distributed,

information including software and/or data may be kept centrally or distributed. Such information may be exchanged between different functional units by way of a communications network, such as a Local Area Network (LAN), Wide Area Network (WAN), or the Internet, wired or wireless data links, electromagnetic signals, or other data communication channel.

[0083] For example, while processes or blocks are presented in a given order, alternative examples may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified to provide alternative or subcombinations. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0084] In addition, while elements are at times shown as being performed sequentially, they may instead be performed simultaneously or in different sequences. It is therefore intended that the following claims are interpreted to include all such variations as are within their intended scope.

[0085] Software and other modules may reside on servers, workstations, personal computers, tablet computers, image data encoders, image data decoders, PDAs, color-grading tools, video projectors, audio-visual receivers, displays (such as televisions), digital cinema projectors, media players, and other devices suitable for the purposes described herein. Those skilled in the relevant art will appreciate that aspects of the system can be practised with other communications, data processing, or computer system configurations, including: Internet appliances, hand-held devices (including personal digital assistants (PDAs)), wearable computers, all manner of cellular or mobile phones, multi-processor systems, microprocessor-based or programmable consumer electronics (e.g., video projectors, audio-visual receivers, displays, such as televisions, and the like), set-top boxes, color-grading tools, network PCs, mini-computers, mainframe computers, and the like.

[0086] The invention may also be provided in the form of a program product. The program product may comprise any non-transitory medium which carries a set of computer-readable instructions which, when executed by a data processor, cause the data processor to execute a method of the invention. Program products according to

the invention may be in any of a wide variety of forms. The program product may comprise, for example, non-transitory media such as magnetic data storage media including floppy diskettes, hard disk drives, optical data storage media including CD ROMs, DVDs, electronic data storage media including ROMs, flash RAM, EPROMs, hardwired or preprogrammed chips (e.g., EEPROM semiconductor chips), nanotechnology memory, or the like. The computer-readable signals on the program product may optionally be compressed or encrypted.

[0087] In some embodiments, the invention may be implemented in software. For greater clarity, “software” includes any instructions executed on a processor, and may include (but is not limited to) firmware, resident software, microcode, and the like. Both processing hardware and software may be centralized or distributed (or a combination thereof), in whole or in part, as known to those skilled in the art. For example, software and other modules may be accessible via local memory, via a network, via a browser or other application in a distributed computing context, or via other means suitable for the purposes described above.

[0088] Where a component (e.g. a software module, processor, assembly, device, circuit, etc.) is referred to above, unless otherwise indicated, reference to that component (including a reference to a “means”) should be interpreted as including as equivalents of that component any component which performs the function of the described component (i.e., that is functionally equivalent), including components which are not structurally equivalent to the disclosed structure which performs the function in the illustrated exemplary embodiments of the invention.

[0089] Specific examples of systems, methods and apparatus have been described herein for purposes of illustration. These are only examples. The technology provided herein can be applied to systems other than the example systems described above. Many alterations, modifications, additions, omissions, and permutations are possible within the practice of this invention. This invention includes variations on described embodiments that would be apparent to the skilled addressee, including variations obtained by: replacing features, elements and/or acts with equivalent features, elements and/or acts; mixing and matching of features, elements and/or acts from different embodiments; combining features, elements and/or acts from embodiments as described herein with features, elements and/or acts of other technology; and/or omitting combining features, elements and/or acts from described

embodiments. For example:

- The embodiments described elsewhere herein comprise a photodiode as the light sensitive (photodetector) element. This is not necessary. The photodiode may additionally or alternatively comprise any suitable photo-sensing element, such as a phototransistor, photogate and/or the like.
- In some embodiments, the Figure 7A DRAM unit 126 may comprise an inverter (not shown), which may be connected to node 127 and may invert the exposure code signal ϕ_{code} present at node 127 to output the complement of exposure code signal ϕ_{code} . After writing to DRAM unit 126 by temporarily activating the control signal ϕ_{ctrl} , this will result in a pair of complementary exposure codes $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$ being present on node 127 and at the output of the inverter. For the particular case of two complementary exposure codes $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$, node 127 of DRAM unit 126 may be connected to the gate of a first valve transistor (e.g. to the gate of M_{val1} in circuit 121 of Figure 5A or circuit 131 of Figure 6A) and the output of the inverter may be connected to the gate of a second valve transistor (e.g. to the gate of M_{val2} in circuit 121 of Figure 5A or circuit 131 of Figure 6A), which may allow the Figure 5A circuit 121 or the Figure 6A circuit to be configured with a single DRAM cell which may store both complementary exposure codes $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$.
- In some embodiments, the Figure 7B SRAM unit 131 may comprise an inverter 137, which may invert exposure code signal ϕ_{code} and may result in the complement of exposure code signal ϕ_{code} being present at node 139. In some embodiments, node 139 of SRAM unit 131 may be connected directly to the complement of exposure code signal ϕ_{code} . After writing to SRAM unit 131 by temporarily activating the control signal ϕ_{ctrl} , this will result in a pair of complementary exposure codes $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$ being present on nodes 133A, 133B of the Figure 7B SRAM unit 131. For the particular case of two complementary exposure codes $\phi_{\text{code}(+)}$, $\phi_{\text{code}(-)}$, node 133A of SRAM unit 131 may be connected to the gate of a first valve transistor (e.g. to the gate of M_{val1} in circuit 121 of Figure 5A or circuit 131 of Figure 6A) and node 133B of SRAM unit 131 may be connected to the gate of a second valve transistor (e.g. to the gate of M_{val2} in circuit 121 of Figure 5A or circuit 131 of Figure 6A), which may allow the Figure 5A circuit 121 or the Figure 6A circuit to be configured with a single SRAM cell which may store both complementary exposure codes

$\Phi_{\text{code}(+)}, \Phi_{\text{code}(-)}$.

- In the embodiments described above, a valve switch M_{val} is provided for each charge storage unit 116 to selectively connect each charge-storage unit 116 to the photodetector 118 or disconnect each charge-storage unit 116 from photodetector 118. In some embodiments, where $N=2$, a pixel may be provided with a single switch (controllable by a single exposure code $\Phi_{\text{code}(+)}$) may be provided which may connect photodetector 118 alternatively to either one of charge storage units 116A, 116B. In other respects, such a pixel may be similar to the embodiments described elsewhere herein where $N=2$.

[0090] It is therefore intended that the following appended claims and claims hereafter introduced are interpreted to include all such modifications, permutations, additions, omissions, and sub-combinations as may reasonably be inferred. The scope of the claims should not be limited by the preferred embodiments set forth in the examples, but should be given the broadest interpretation consistent with the description as a whole.

WHAT IS CLAIMED IS:

1. A pixel for an image sensor comprising:
 - a photodetector for emitting charge in response to light incident thereon;
 - a plurality of charge-storage devices and a corresponding plurality of valve switches, each charge-storage device selectively connectable to receive charge from the photodetector by control of a switching state of its corresponding valve switch;
 - wherein the switching state of each valve switch is responsive to a corresponding exposure code signal ϕ_{code} received at a control input of the valve switch.
2. A pixel according to claim 1 or any other claim herein wherein the exposure code signal ϕ_{code} received at the control input of each valve switch comprises a binary signal having binary values capable of changing in each of a plurality of exposure sub-periods of a single exposure period T_{expo} during which the pixel is exposed to incident light.
3. A pixel according to any one of claims 1 to 2 or any other claim herein comprising a plurality of code-memory units, each code-memory unit connected to receive a corresponding input exposure code signal and selectively connectable to provide a corresponding exposure code signal ϕ_{code} to the control input of a corresponding one of the plurality of valve switches to thereby control the switching state of the corresponding one of the valve switches.
4. A pixel according to claim 3 or any other claim herein wherein the input exposure code signal received at each code-memory unit comprises a binary signal having binary values capable of changing in each of a plurality of exposure sub-periods of a single exposure period T_{expo} during which the pixel is exposed to incident light.
5. A pixel according to any one of claims 3 to 4 or any other claim herein wherein

each code-memory unit comprises a memory for maintaining the corresponding exposure code signal at the control input of the corresponding one of the valve switches.

6. A pixel according to claim 5 or any other claim herein wherein, for each code-memory unit, the memory comprises a memory capacitor.
7. A pixel according to any one of claims 3 to 6 or any other claim herein wherein each code-memory unit comprises a dynamic random access (DRAM) cell.
8. A pixel according to any one of claims 3 to 5 or any other claim herein wherein each code-memory unit comprises a static random access (SRAM) cell.
9. A pixel according to any one of claims 3 to 8 or any other claim herein wherein each code-memory unit is selectively connectable to provide the corresponding exposure code signal to the control input of the corresponding one of the plurality of valve switches in response to a control signal ϕ_{ctrl} .
10. A pixel according to any one of claims 3 to 9 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the plurality of code-memory units are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip..
11. A pixel according to any one of claims 1 to 10 or any other claim herein comprising one or more readout circuits, each readout circuit associated with a corresponding one of the plurality of charge-storage devices and selectively connectable to the corresponding one of the charge-storage devices to output a corresponding output signal, the corresponding output signals dependent on an amount of charge stored in the corresponding one of the charge-storage devices.
12. A pixel according to claim 11 or any other claim herein wherein each readout circuit comprises a source follower transistor.

13. A pixel according to claim 11 or any other claim herein wherein each readout circuit comprises a trans-impedance amplifier (TIA).
14. A pixel according to any one of claims 11 to 13 or any other claim herein wherein each readout circuit is selectively connectable to the corresponding one of the charge storage units to output the corresponding output signal in response to a pixel select signal ϕ_{sel} .
15. A pixel according to any one of claims 11 to 13 or any other claim herein wherein each readout circuit is selectively connectable to the corresponding one of the charge storage units to output the corresponding output signal in response to a combination of an output transfer signal ϕ_{tran} and a pixel select signal ϕ_{sel} .
16. A pixel according to any one of claims 11 to 15 or any other claim herein wherein each readout circuit is selectively connectable to the corresponding one of the charge-storage units once per exposure period T_{expo} during which the pixel is exposed to light at the conclusion of the exposure period T_{expo} and prior to any next exposure period.
17. A pixel according to any one of claims 11 to 16 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the one or more readout circuits are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip..
18. A pixel according to any one of claims 1 to 17 or any other claim herein wherein each charge-storage device comprises a charge-storage capacitor.
19. A pixel according to any one of claims 1 to 18 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the plurality of charge-storage devices are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips

stacked with the first microelectronic chip..

20. A pixel according to any one of claims 1 to 19 or any other claim herein wherein each valve switch comprises a CMOS transistor, the gate of the CMOS transistor providing the control input of the valve switch and the source of the CMOS transistor connected to one of the photodetector and the corresponding charge-storage device and the drain of the CMOS transistor connected to the other one of the photodetector and the corresponding charge-storage device.
21. A pixel according to any one of claims 1 to 20 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the plurality of valve switches are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip.
22. A pixel according to any one of claims 1 to 21 or any other claim herein comprising a plurality of reset switches, each reset switch selectively connectable to a corresponding one of the charge-storage devices to reset a voltage level at the corresponding one of the charge-storage devices.
23. A pixel according to claim 22 or any other claim herein wherein each reset switch is selectively connectable to the corresponding one of the charge-storage devices in response to a pixel reset signal ϕ_{rst} .
24. A pixel according to any one of claims 22 to 23 or any other claim herein wherein each reset switch is selectively connectable to the corresponding one of the charge-storage devices once per exposure period T_{expo} during which the pixel is exposed to light immediately prior to the exposure period T_{expo} .
25. A pixel according to any one of claims 1 to 24 or any other claim herein wherein one of the exposure code signals is complementary to at least one other one of the exposure code signals such that the switching states of valve switches that receive the one of the exposure code signals and the other one

of the exposure code signals are opposite to one another.

26. A pixel according to any one of claims 1 to 25 or any other claim herein wherein the plurality of charge-storage devices comprises two charge-storage devices and the corresponding plurality of valve switches comprise two corresponding valve switches.
27. A pixel according to claim 26 or any other claim herein comprising a code memory unit connected to receive a corresponding input exposure code signal and selectively connectable to provide a corresponding exposure code signal $\phi_{\text{code}(+)}$ to the control input of a first one of the two valve switches to thereby control the switching state of the first one of the two valve switches.
28. A pixel according to claim 27 or any other claim herein comprising a digital inverter connected to receive corresponding exposure code signal $\phi_{\text{code}(+)}$ from the code-memory unit and to output a complementary exposure code signal $\phi_{\text{code}(-)}$ to the control input of a second one of the two valve switches to thereby control the switching state of the second one of the two valve switches, the switching state of the second one of the two valve switches being opposite to the switching state of the first one of the two valve switches.
29. A pixel according to claim 27 or any other claim herein wherein the code memory unit comprises a static random access (SRAM) cell which receives the input exposure code signal and stores the exposure code signal $\phi_{\text{code}(+)}$ and a complementary exposure code signal $\phi_{\text{code}(-)}$ and which is selectively connectable to provide the complementary exposure code signal $\phi_{\text{code}(-)}$ to the control input of a second one of the two valve switches to thereby control the switching state of the second one of the two valve switches, the switching state of the second one of the two valve switches being opposite to the switching state of the first one of the two valve switches.
30. A pixel for an image sensor comprising:
 - a photodetector for emitting charge in response to light incident thereon;
 - first and second charge-storage devices and a valve switch, each of the

first and second charge-storage devices selectively connectable to receive charge from the photodetector by control of a switching state of the valve switch between the photodetector and either one of the first and second charge-storage devices;

wherein the switching state of the valve switch is responsive to a corresponding exposure code signal ϕ_{code} received at a control input of the valve switch.

31. A pixel according to claim 30 or any other claim herein comprising any features, combinations of features and/or sub-combinations of features of claims 1 to 29.
32. An image-capture device for capturing exposure encoded images on a pixel array, the image-capture device comprising:
 - a pixel array, each pixel of the array comprising:
 - a photodetector for emitting charge in response to light incident thereon;
 - a plurality of charge-storage devices and a corresponding plurality of valve switches, each charge-storage device selectively connectable to receive charge from the photodetector by control of a switching state of its corresponding valve switch;
 - wherein the switching state of each valve switch is responsive to a corresponding exposure code signal ϕ_{code} received at a control input of the valve switch;
 - a digital processor connected to provide control signals, the control signals comprising the exposure code signals, to the pixel array and configured to provide the control signals in a manner which causes the pixel array to capture an exposure encoded image wherein, for an exposure period T_{expo} associated with the exposure encoded image during which the pixel array is exposed to light and for each pixel, the selective connection of the photodetector to each charge-storage device is temporally intermittent.
33. An image-capture device according to claim 32 or any other claim herein wherein each exposure code signal provided by the processor to the pixel

array and received at the control input of a corresponding valve switch is a binary signal having binary values capable of changing in each of a plurality of exposure sub-periods during the exposure period T_{expo} .

34. An image-capture device according to claim 33 or any other claim herein wherein the processor is configured to provide updated exposure code signals to each pixel in the array once for each exposure sub-period during the exposure period T_{expo} .
35. An image-capture device according to claim 34 or any other claim herein wherein the processor is connected to provide the exposure code signals to the pixels over a plurality of column busses and, in each exposure sub-period during the exposure period T_{expo} , is configured to provide the updated exposure code signals to the pixels on a row-by-row basis, the provision of updated exposure code signals to each row of pixels gated by a corresponding row control signal ϕ_{row} .
36. An image-capture device according to any one of claims 33 to 35 or any other claim herein wherein, after the updated exposure codes are provided to each pixel in the array, each pixel in the array operates according to the updated exposure codes for a remainder of the exposure period T_{expo} .
37. An image-capture device according to any one of claims 33 to 36 or any other claim herein wherein the exposure period T_{expo} may be offset for different pixels (e.g. for different individual pixels or different rows of pixels) in the array.
38. An image-capture device according to any one of claims 32 to 37 or any other claim herein wherein each pixel comprises one or more readout circuits, each readout circuit associated with a corresponding one of the plurality of charge-storage devices and selectively connectable to the corresponding one of the charge-storage devices to output a corresponding output signal, the corresponding output signals dependent on an amount of charge stored in the corresponding one of the charge-storage devices.

39. An image-capture device according to claim 38 or any other claim herein wherein the processor is configured to provide pixel select signals ϕ_{sel} to the array to thereby selectively connect each readout circuit to the corresponding one of the charge storage units to output the corresponding output signal once per exposure period T_{expo} at the conclusion of the exposure period T_{expo} and prior to any next exposure period.
40. An image-capture device according to claim 38 or any other claim herein wherein the processor is configured to provide pixel select signals ϕ_{sel} and output transfer signals ϕ_{tran} to the array to thereby selectively connect each readout circuit to the corresponding one of the charge storage units to output the corresponding output signal once per exposure period T_{expo} at the conclusion of the exposure period T_{expo} and prior to any next exposure period.
41. An image-capture device according to any one of claims 32 to 40 or any other claim herein wherein each pixel comprises a plurality of reset switches, each reset switch selectively connectable to a corresponding one of the charge-storage devices to reset a voltage level at the corresponding one of the charge-storage devices.
42. An image-capture device according to claim 41 or any other claim herein wherein the processor is configured to provide pixel reset signals ϕ_{rst} to the array to thereby reset each charge-storage device once per exposure period T_{expo} immediately prior to the exposure period T_{expo} .
43. An image-capture device according to any one of claims 32 to 42 or any other claim herein comprising any of the features, combinations of features or sub-combinations of features of any of claims 1 to 31.
44. A method for facilitating intermittent exposure of a pixel in an image sensor, the method comprising:
providing a pixel comprising: a photodetector for emitting charge in response to light incident thereon, a plurality of charge-storage devices and a corresponding plurality of valve switches, each charge-storage device

selectively connectable to receive charge from the photodetector by control of a switching state of its corresponding valve switch;

for each of a plurality of exposure sub-periods in an exposure period T_{expo} during which the pixel is exposed to light, providing an exposure code signal ϕ_{code} at a control input of each valve switch, to thereby control the switching state of the valve switch.

45. A method according to claim 44 or any other claim herein wherein, for each of a plurality of exposure sub-periods in an exposure period T_{expo} during which the pixel is exposed to light, providing an exposure code signal ϕ_{code} at a control input of each valve switch, comprises providing a binary exposure code signal ϕ_{code} .
46. A method according to any one of claims 44 to 45 or any other claim herein comprising providing each exposure code signal to a corresponding code-memory unit which is selectively connectable to provide the exposure code signal ϕ_{code} to the control input of a corresponding one of the plurality of valve switches to thereby control the switching state of the corresponding one of the valve switches.
47. A method according to claim 46 or any other claim herein wherein each code-memory unit comprises a memory for maintaining the corresponding exposure code signal at the control input of the corresponding one of the valve switches.
48. A method according to any one of claims 46 to 47 or any other claim herein comprising providing a control signal ϕ_{ctrl} which causes the selective connection of each code-memory unit to provide the corresponding exposure code signal to the control input of the corresponding one of the plurality of valve switches.
49. A method according to any one of claims 46 to 48 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the plurality of code-memory units are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the

first microelectronic chip.

50. A method according to any one of claims 44 to 49 or any other claim herein comprising selectively connecting one or more of the plurality of charge-storage devices to one or more corresponding readout circuits to output one or more corresponding output signals, each corresponding output signal dependent on an amount of charge stored in a corresponding one of the charge-storage devices.
51. A method according to claim 50 or any other claim herein comprising providing a pixel select signal ϕ_{sel} which causes the selective connection of the one or more charge-storage devices to the one or more corresponding readout circuits.
52. A method according to claim 50 or any other claim herein comprising providing a combination of an output transfer signal ϕ_{tran} and a pixel select signal ϕ_{sel} which causes the selective connection of the one or more charge-storage devices to the one or more corresponding readout circuits.
53. A method according to any one of claims 50 to 52 or any other claim herein comprising selectively connecting the one or more readout circuits to the one or more the charge-storage units once per exposure period T_{expo} at the conclusion of the exposure period T_{expo} and prior to any next exposure period.
54. A method according to any one of claims 50 to 53 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the one or more readout circuits are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip.
55. A method according to any one of claims 44 to 54 or any other claim herein wherein each charge-storage device comprises a charge-storage capacitor.
56. A method according to any one of claims 44 to 55 or any other claim herein

wherein the photodetector is fabricated on a first microelectronic chip and the plurality of charge-storage devices are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip.

57. A method according to any one of claims 44 to 56 or any other claim herein wherein each valve switch comprises a CMOS transistor, the gate of the CMOS transistor providing the control input of the valve switch and the source of the CMOS transistor connected to one of the photodetector and the corresponding charge-storage device and the drain of the CMOS transistor connected to the other one of the photodetector and the corresponding charge-storage device.
58. A method according to any one of claims 44 to 57 or any other claim herein wherein the photodetector is fabricated on a first microelectronic chip and the plurality of valve switches are fabricated on the same first microelectronic chip or on one or more second stacked microelectronic chips stacked with the first microelectronic chip.
59. A method according to any one of claims 44 to 58 or any other claim herein comprising selectively connecting each of a plurality of reset switches to a corresponding one of the charge-storage devices to reset a voltage level at the corresponding one of the charge-storage devices.
60. A method according to claim 59 or any other claim herein comprising providing a pixel reset signals ϕ_{rst} which cause the selective connection of each reset switch to the corresponding one of the charge-storage devices.
61. A method according to any one of claims 59 to 60 or any other claim herein comprising selectively connecting each reset switch to the corresponding one of the charge-storage devices once per exposure period T_{expo} immediately prior to the exposure period T_{expo} .
62. A method according to any one of claims 44 to 61 or any other claim herein

wherein one of the exposure code signals is complementary to at least one other one of the exposure code signals such that the switching states of valve switches that receive the one of the exposure code signals and the other one of the exposure code signals are opposite to one another.

63. A method according to any one of claims 44 to 62 or any other claim herein wherein the plurality of charge-storage devices comprises two charge-storage devices and the corresponding plurality of valve switches comprise two corresponding valve switches.
64. A method according to claim 63 or any other claim herein comprising providing a code memory unit connected to receive a corresponding input exposure code signal and selectively connectable to provide a corresponding exposure code signal $\phi_{\text{code}(+)}$ to the control input of a first one of the two valve switches to thereby control the switching state of the first one of the two valve switches.
65. A method according to claim 64 or any other claim herein comprising connecting a digital inverter to receive corresponding exposure code signal $\phi_{\text{code}(+)}$ from the code-memory unit and to output a complementary exposure code signal $\phi_{\text{code}(-)}$ to the control input of a second one of the two valve switches to thereby control the switching state of the second one of the two valve switches, the switching state of the second one of the two valve switches being opposite to the switching state of the first one of the two valve switches.
66. A method according to claim 64 or any other claim herein wherein the code memory unit comprises a static random access (SRAM) cell which receives the input exposure code signal and stores the exposure code signal $\phi_{\text{code}(+)}$ and a complementary exposure code signal $\phi_{\text{code}(-)}$ and which is selectively connectable to provide the complementary exposure code signal $\phi_{\text{code}(-)}$ to the control input of a second one of the two valve switches to thereby control the switching state of the second one of the two valve switches, the switching state of the second one of the two valve switches being opposite to the switching state of the first one of the two valve switches.

67. A method according to any one of claims 44 to 66 or any other claim herein comprising any of the features, combinations of features or sub-combinations of features of any of claims 1 to 43.
68. A method for facilitating intermittent exposure of a pixel in an image sensor the method comprising
 providing a pixel comprising: a photodetector for emitting charge in response to light incident thereon; first and second charge-storage devices and a valve switch, each of the first and second charge-storage devices selectively connectable to receive charge from the photodetector by control of a switching state of the valve switch between the photodetector and either one of the first and second charge-storage devices;
 for each of a plurality of exposure sub-periods in an exposure period T_{expo} during which the pixel is exposed to light, providing an exposure code signal ϕ_{code} at a control input of the valve switch, to thereby control the switching state of the valve switch.
69. A method according to claim 68 or any other claim herein comprising any of the features, combinations of features or sub-combinations of features of any of claims 1 to 67.
70. A method for operating an image-capture device to capture exposure encoded images on a pixel array, the method comprising:
 providing a pixel array, each pixel of the array comprising: a photodetector for emitting charge in response to light incident thereon; a plurality of charge-storage devices and a corresponding plurality of valve switches, each charge-storage device selectively connectable to receive charge from the photodetector by control of a switching state of its corresponding valve switch;
 for each valve switch of each pixel and for each of a plurality of exposure sub-periods in an exposure period T_{expo} during which the pixel is exposed to light, providing an exposure code signal ϕ_{code} at a control input of the valve switch to thereby control the switching state of the valve switch;
 providing control signals, the control signals comprising the exposure code signals, to the pixel array in a manner which causes the pixel array to capture

an exposure encoded image wherein, for the exposure period T_{expo} , the selective connection of the photodetector to each charge-storage device is temporally intermittent.

71. A method according to claim 70 or any other claim herein comprising any of the features, combinations of features or sub-combinations of features of any of claims 1 to 69.
72. Apparatus having any new and inventive feature, combination of features, or sub-combination of features as described herein.
73. Methods having any new and inventive steps, acts, combination of steps and/or acts or sub-combination of steps and/or acts as described herein.

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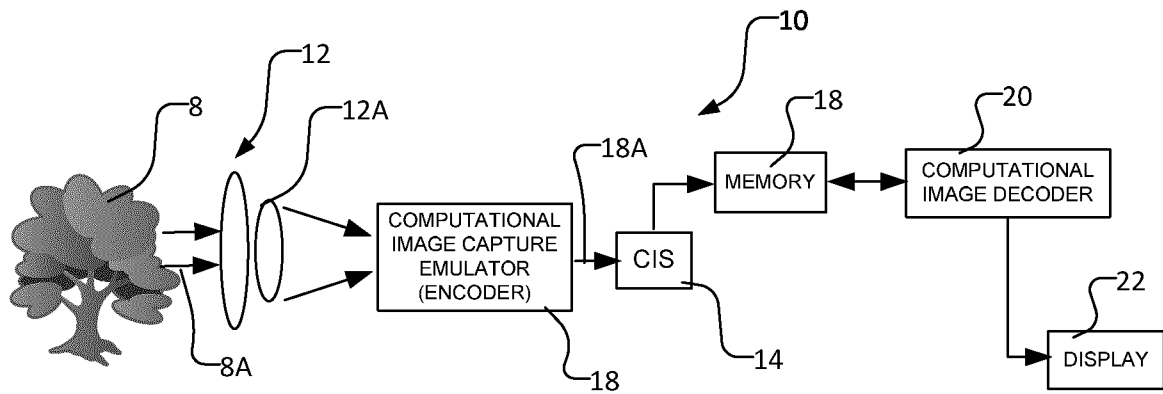
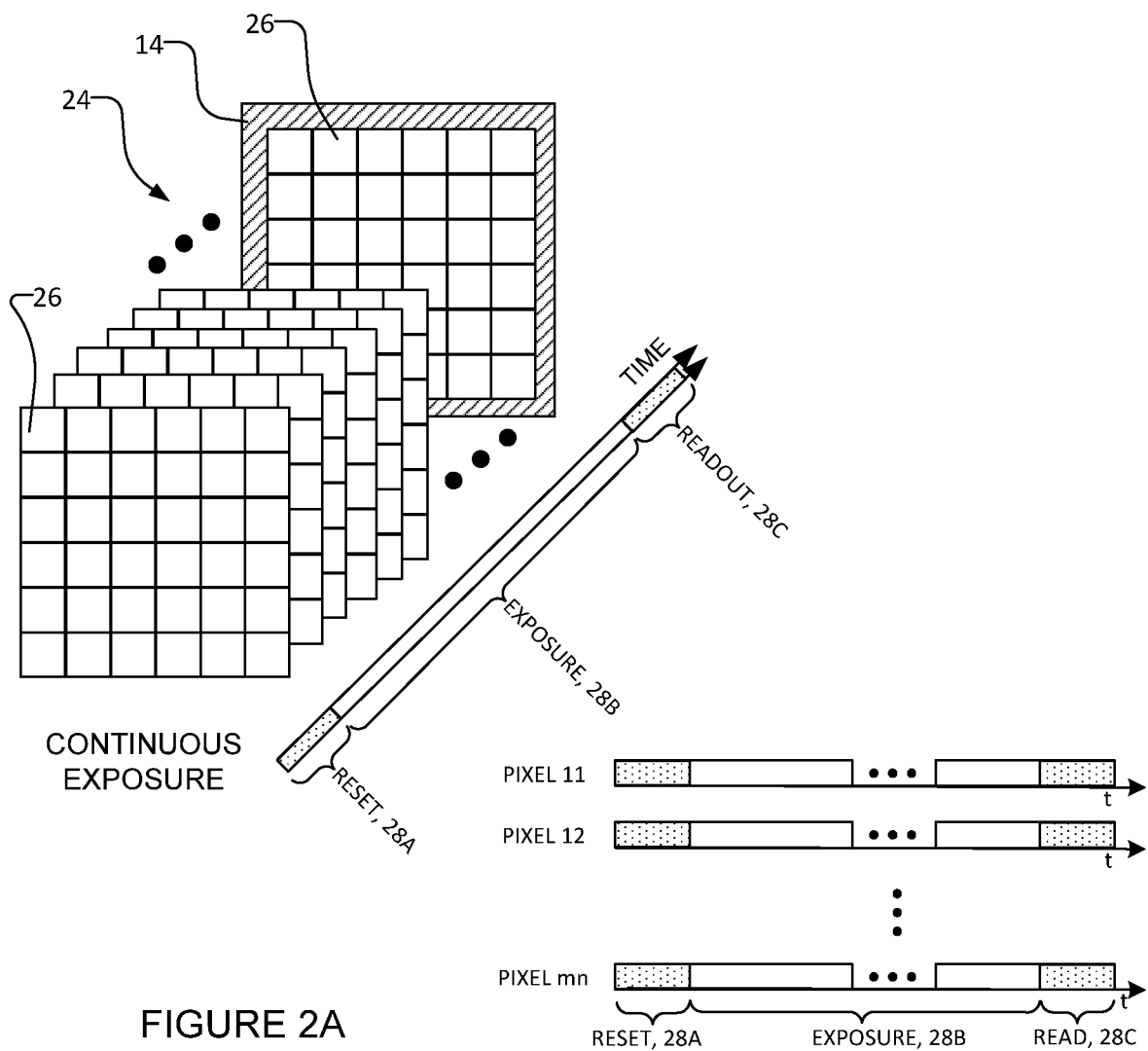


FIGURE 1



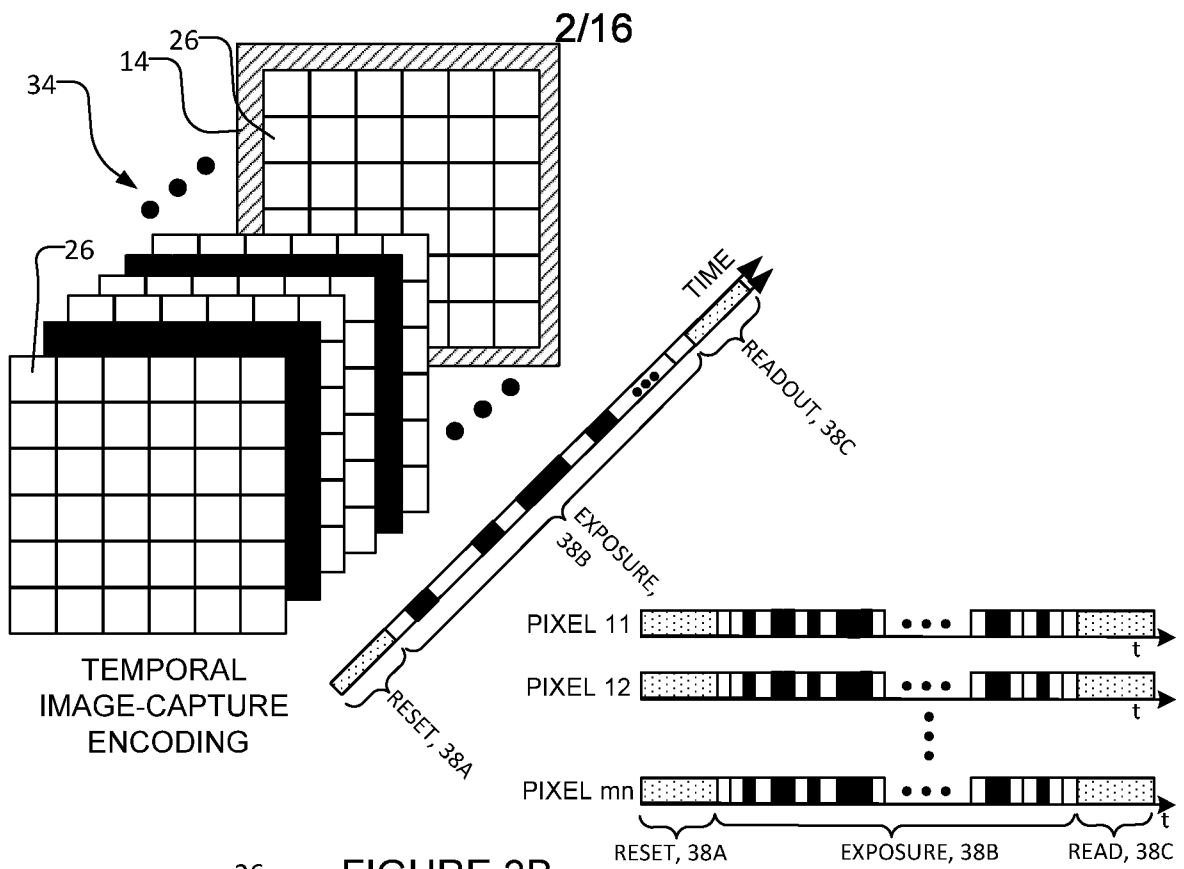


FIGURE 2B

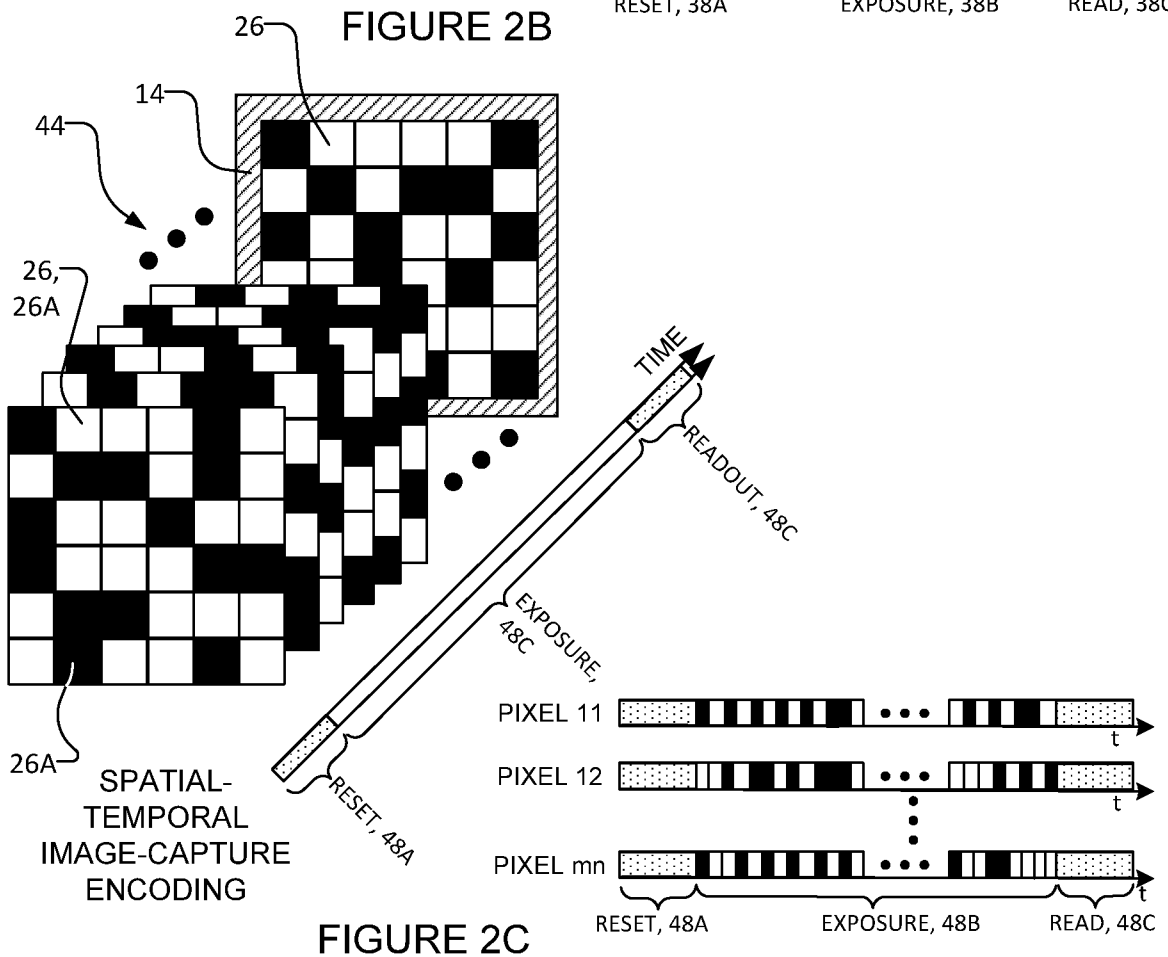


FIGURE 2C

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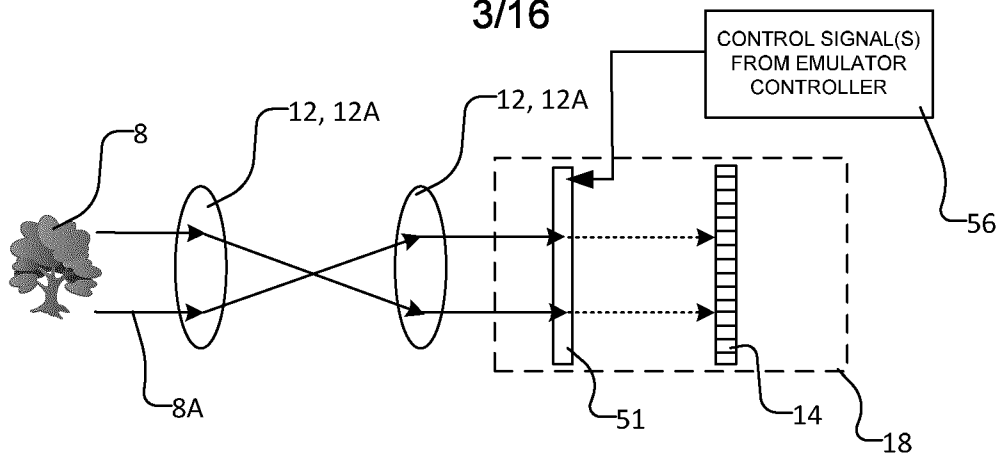


FIGURE 2D

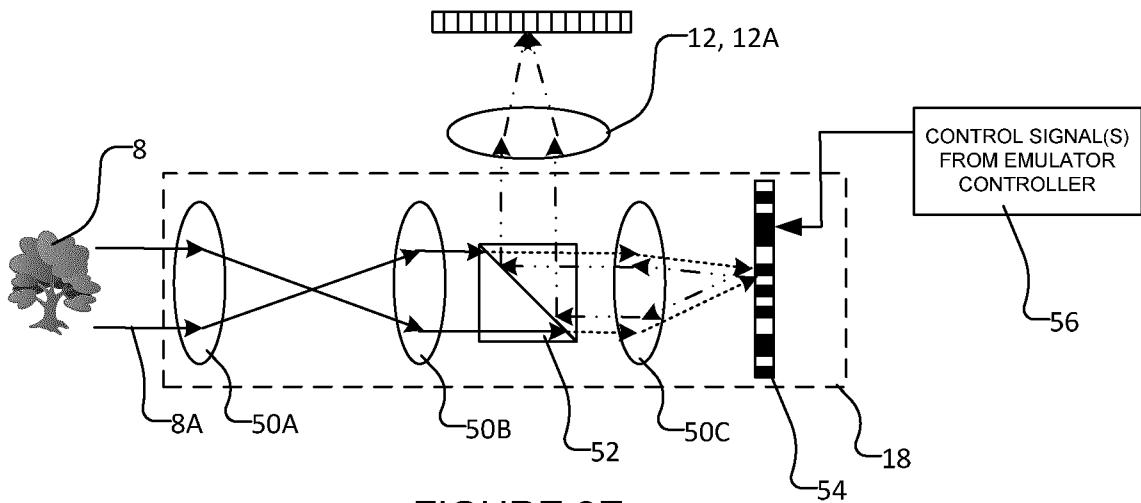


FIGURE 2E

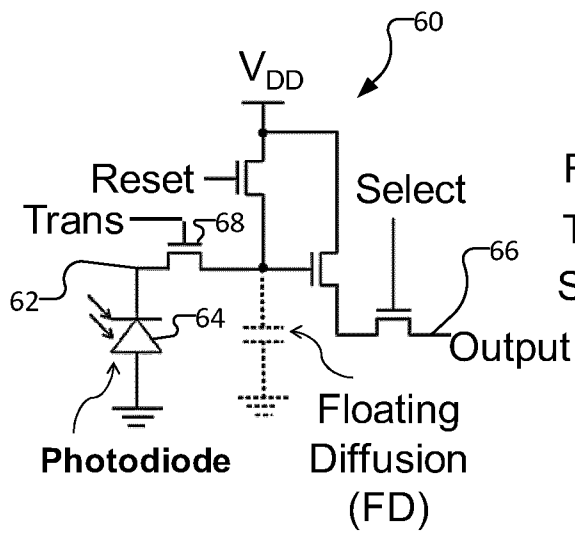


FIGURE 3A

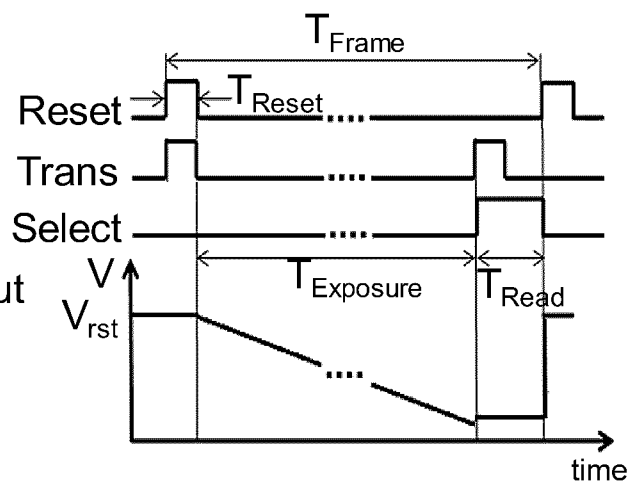


FIGURE 3B

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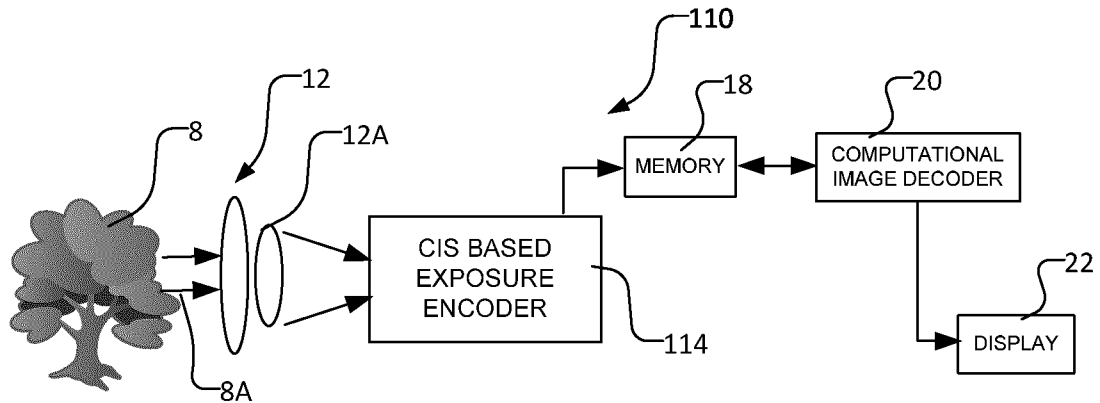


FIGURE 4A

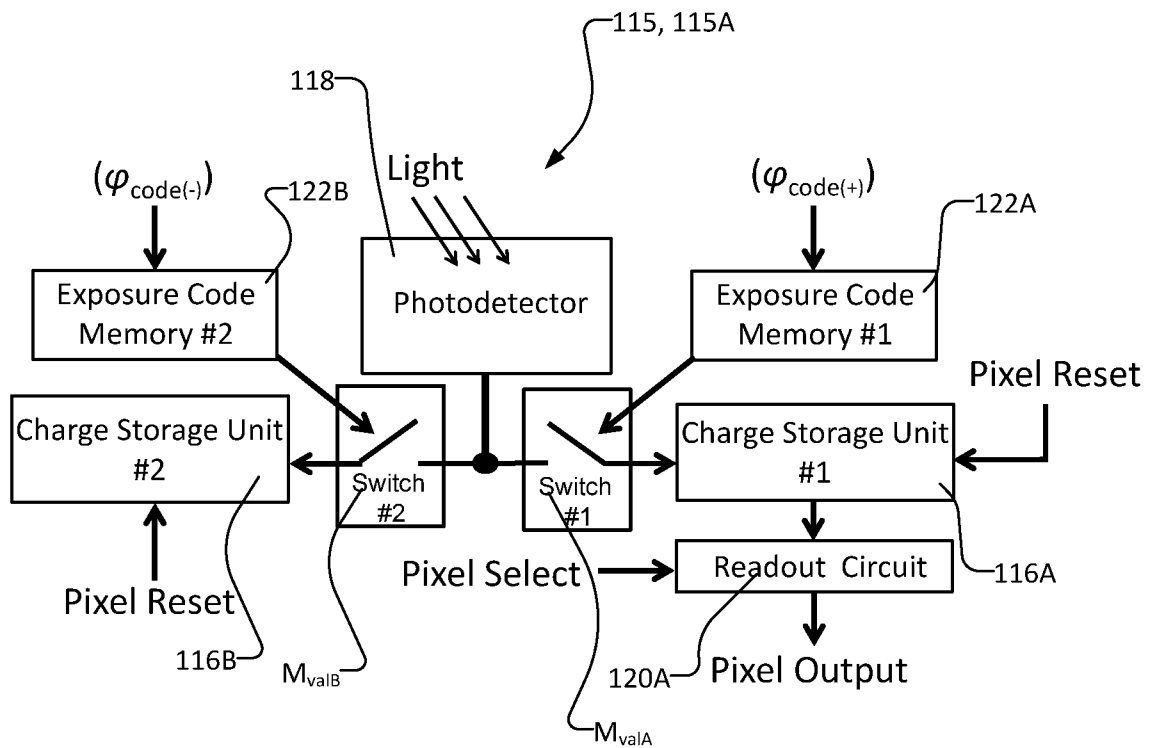


FIGURE 4B

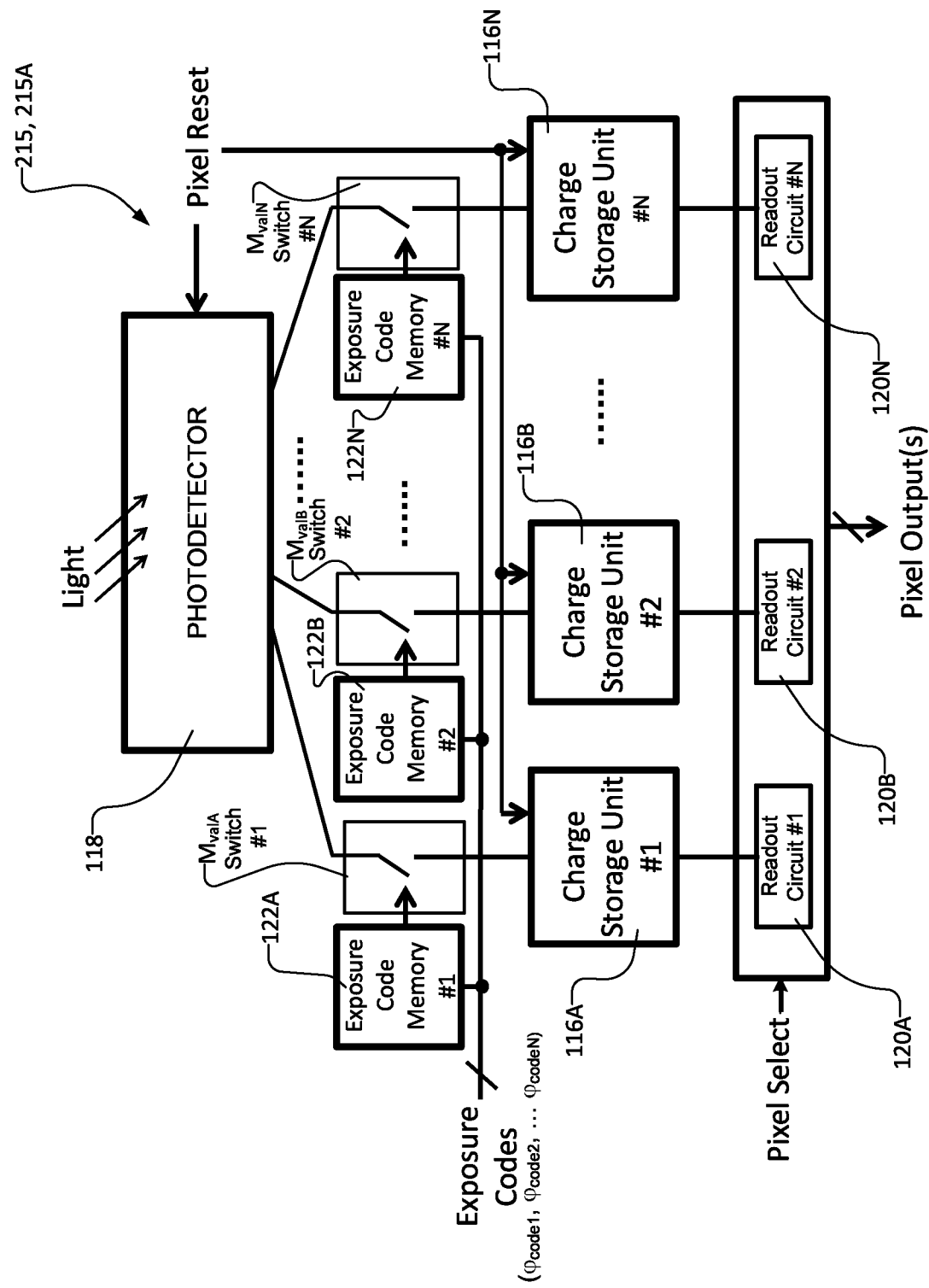


FIGURE 4C

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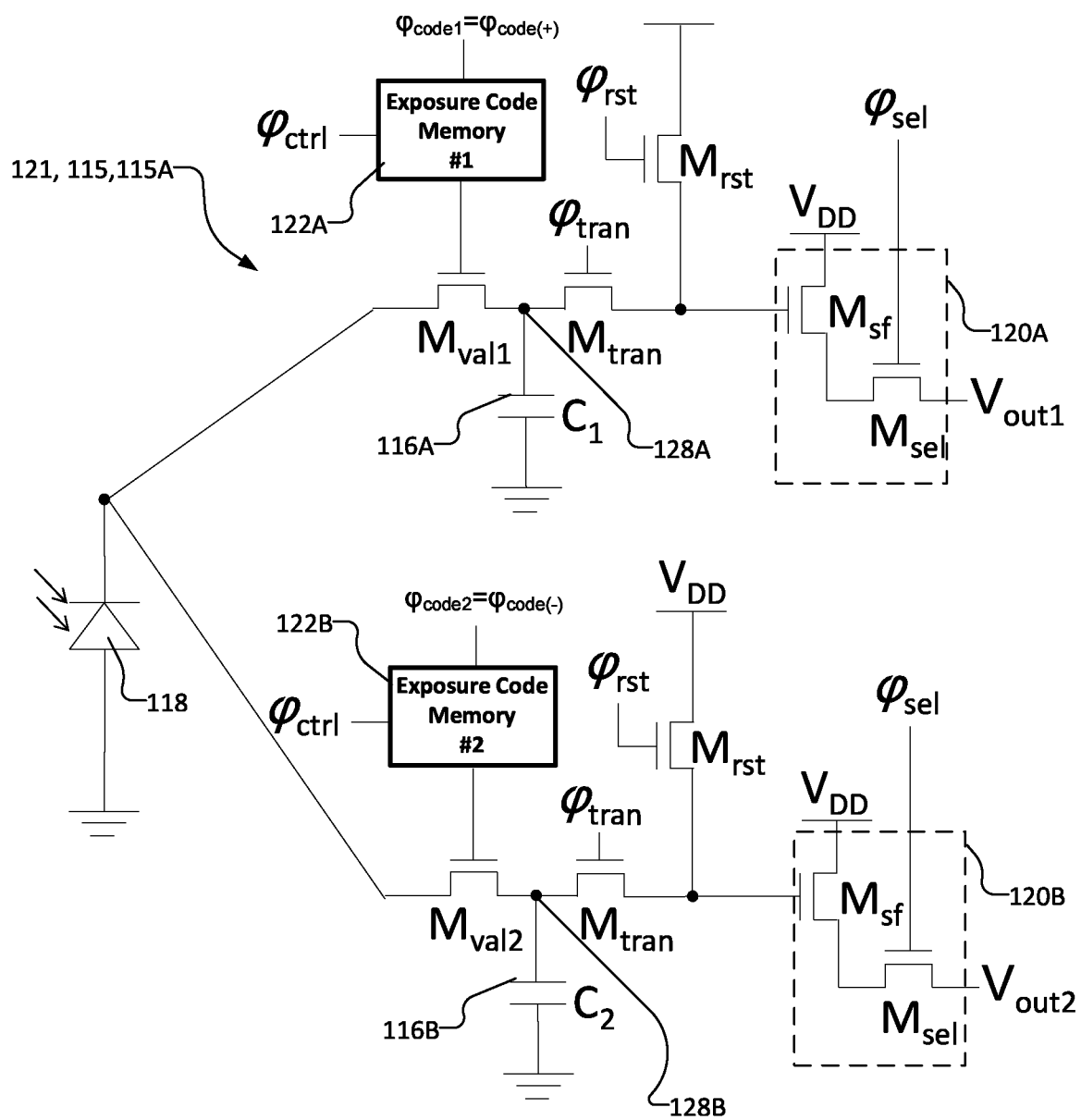


FIGURE 5A

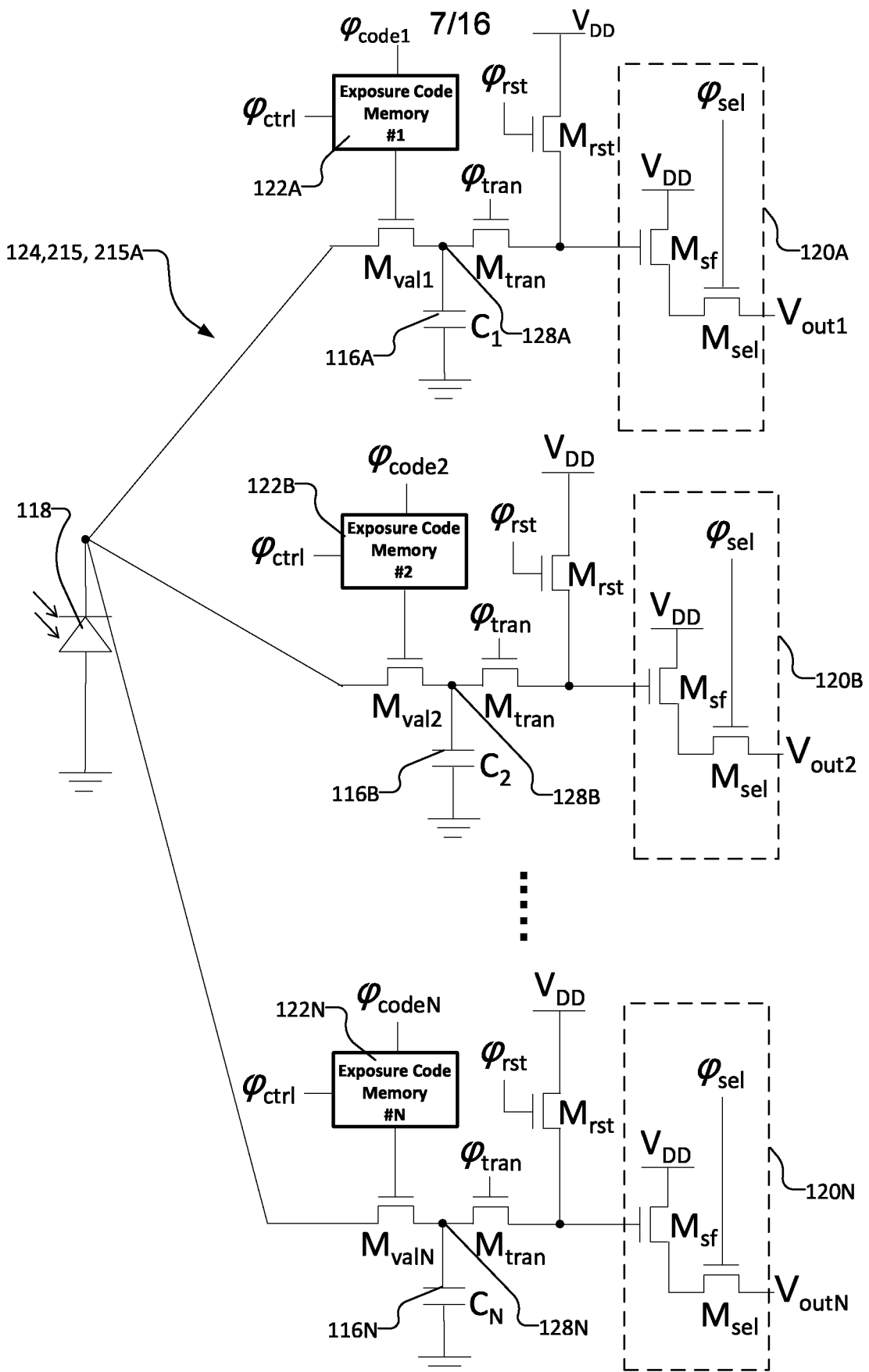


FIGURE 5B

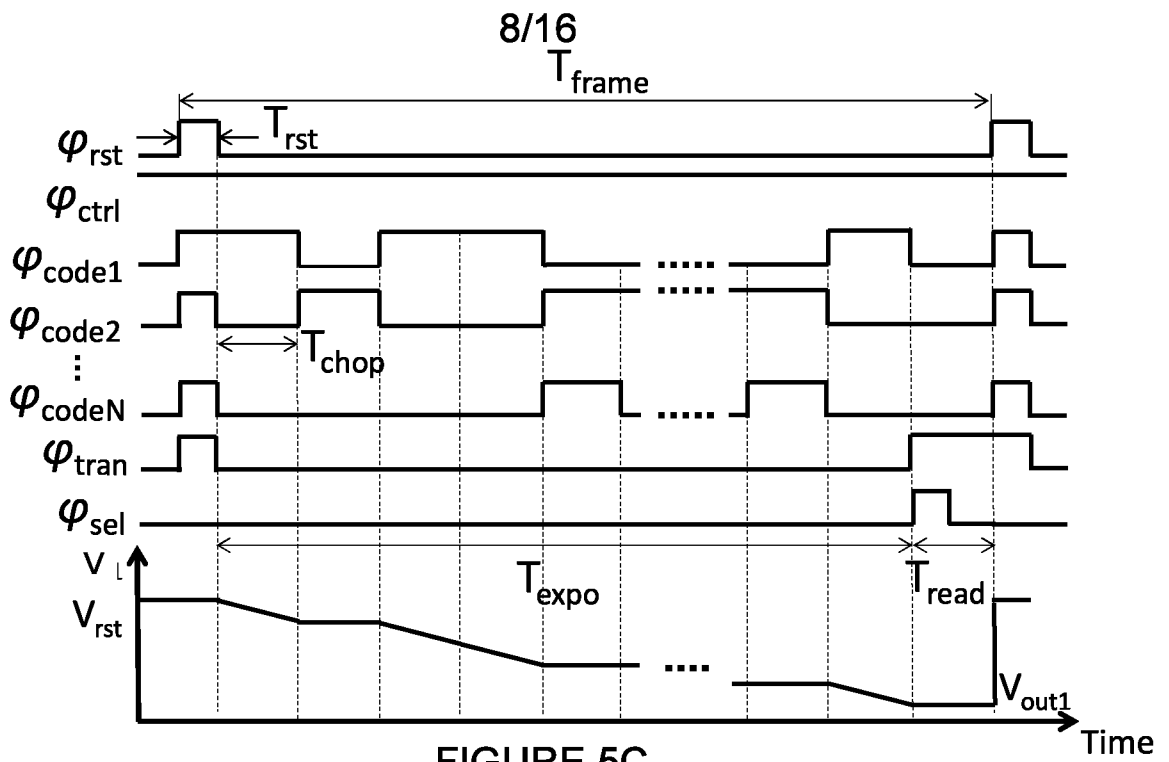


FIGURE 5C

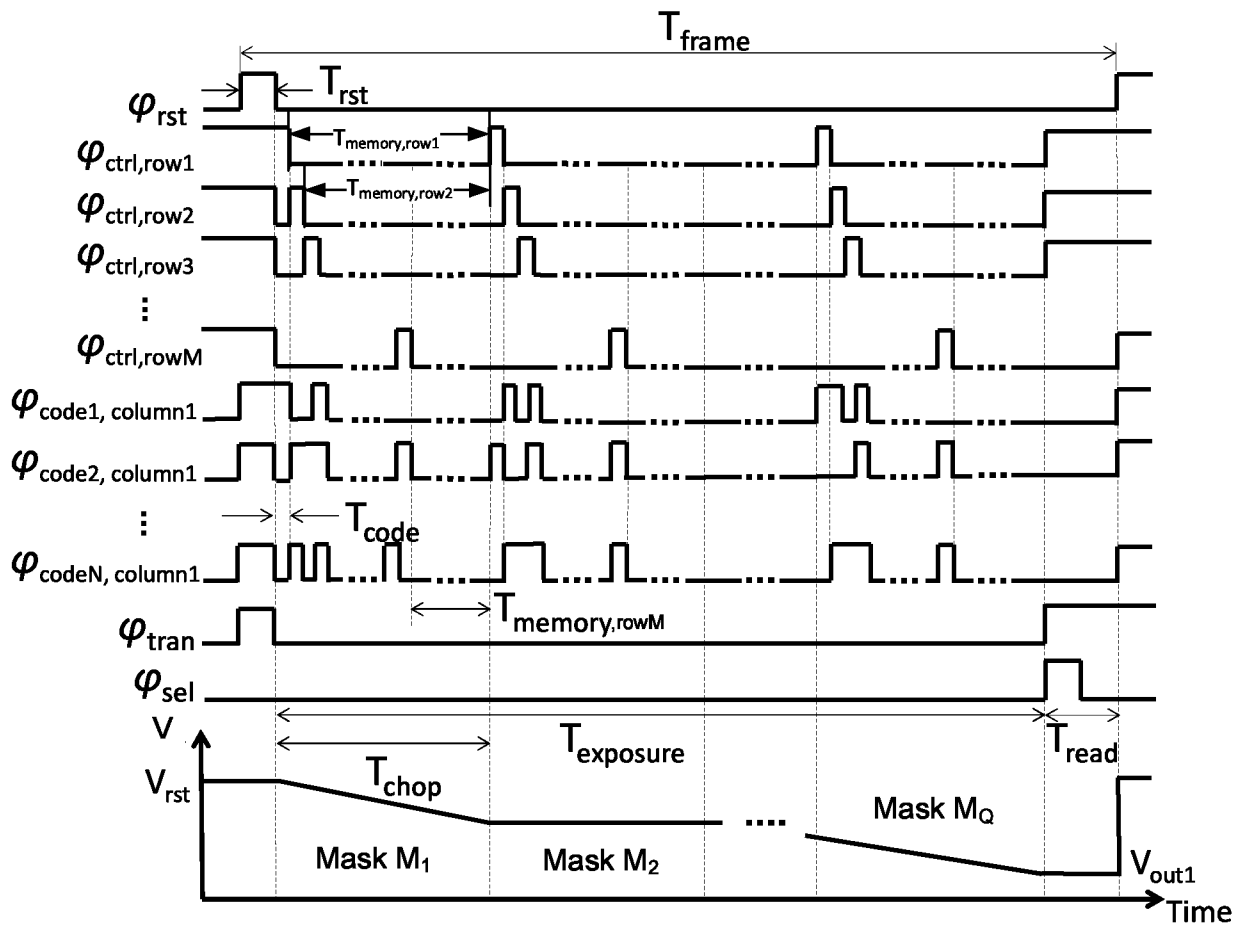


FIGURE 5D

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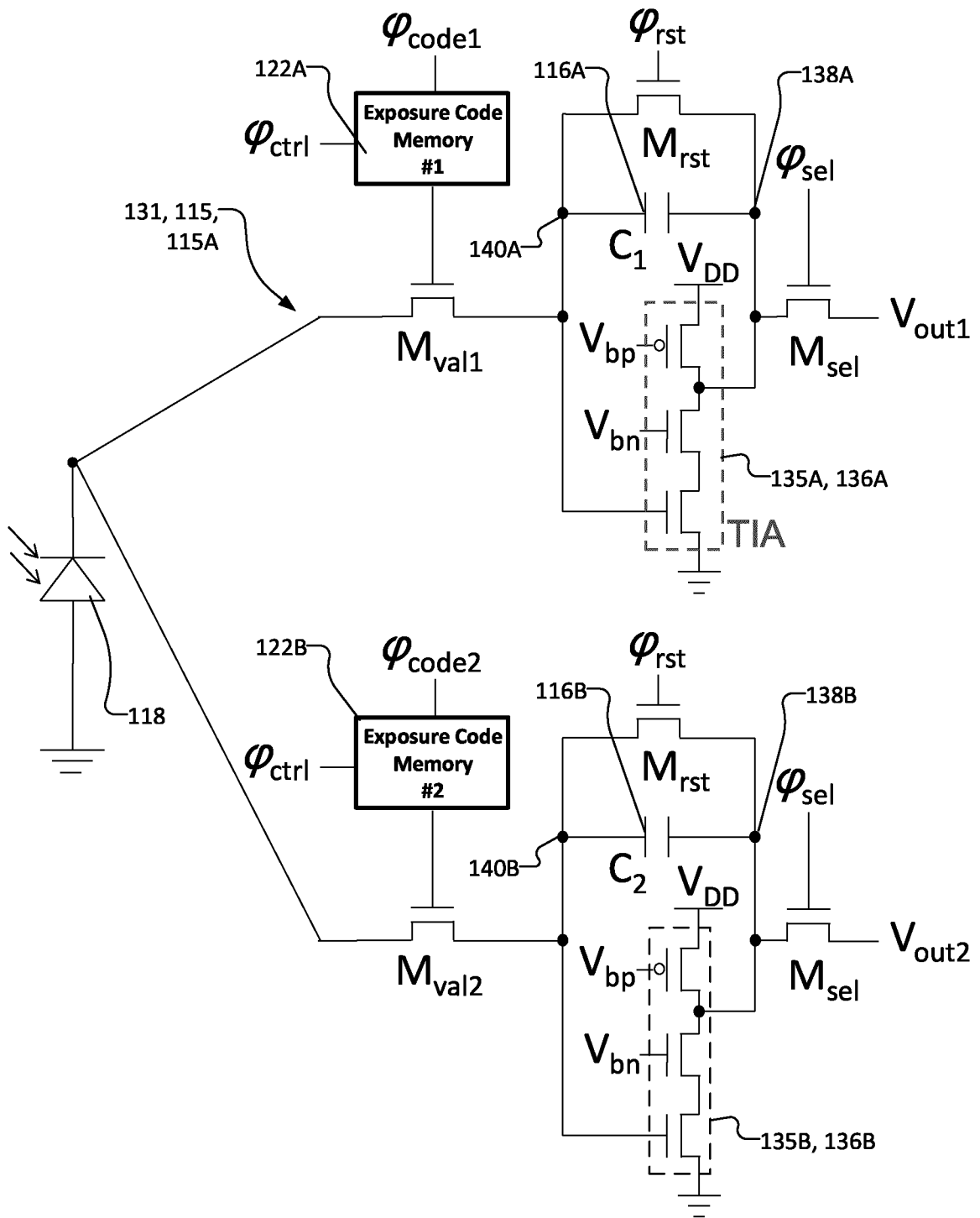


FIGURE 6A

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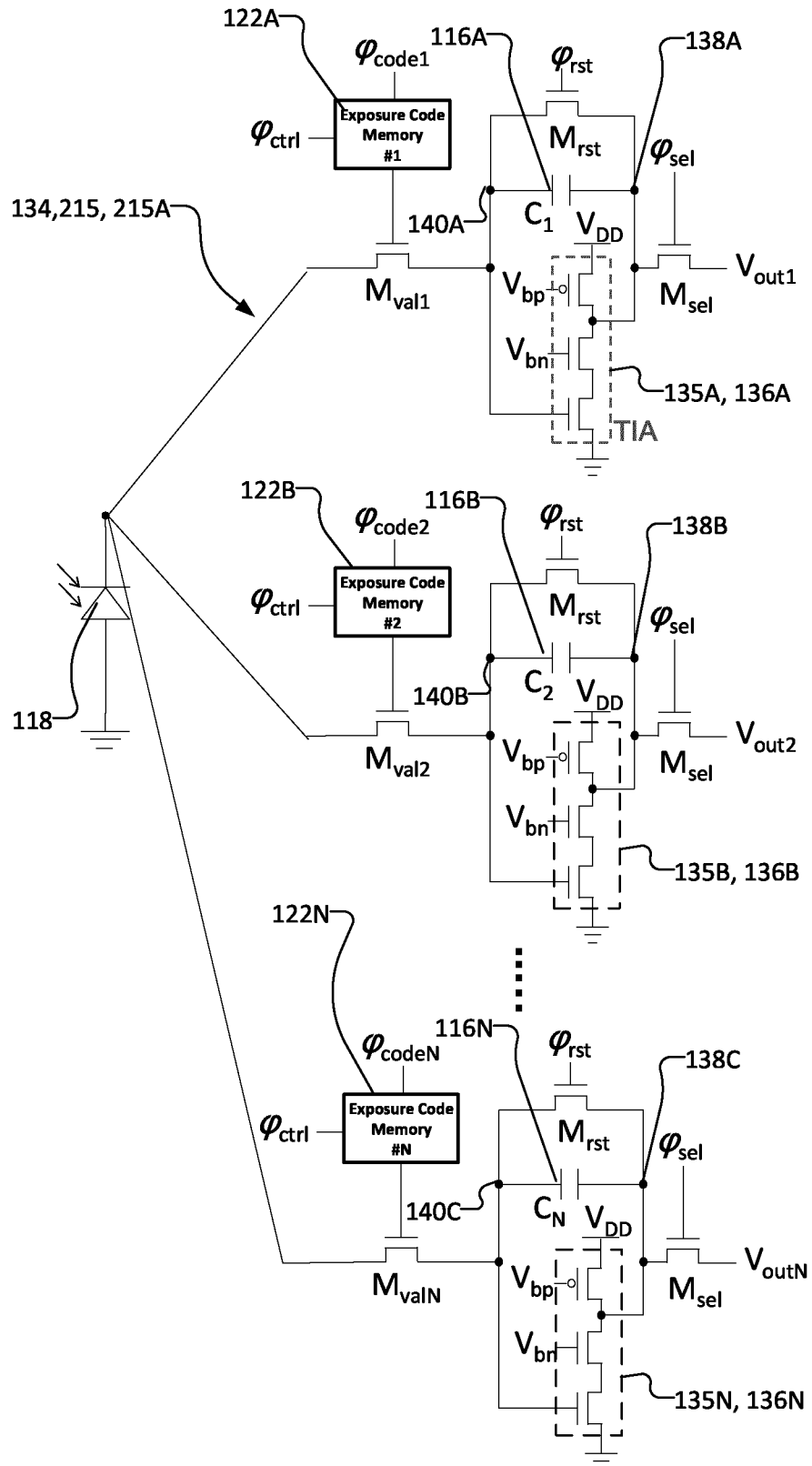


FIGURE 6B

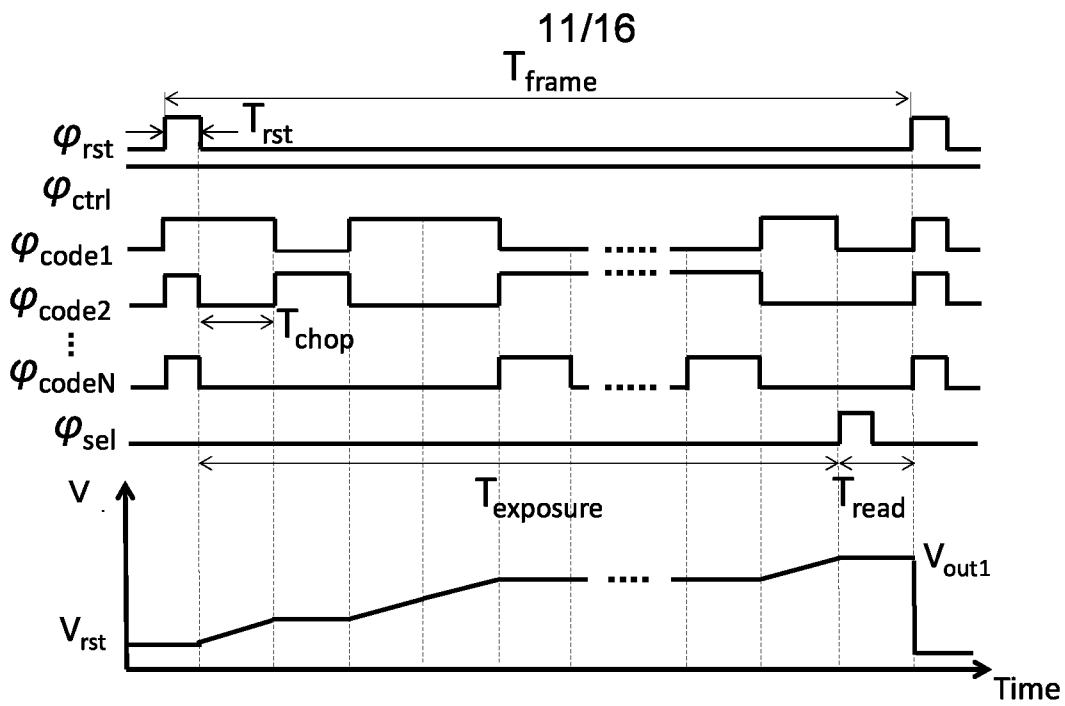


FIGURE 6C

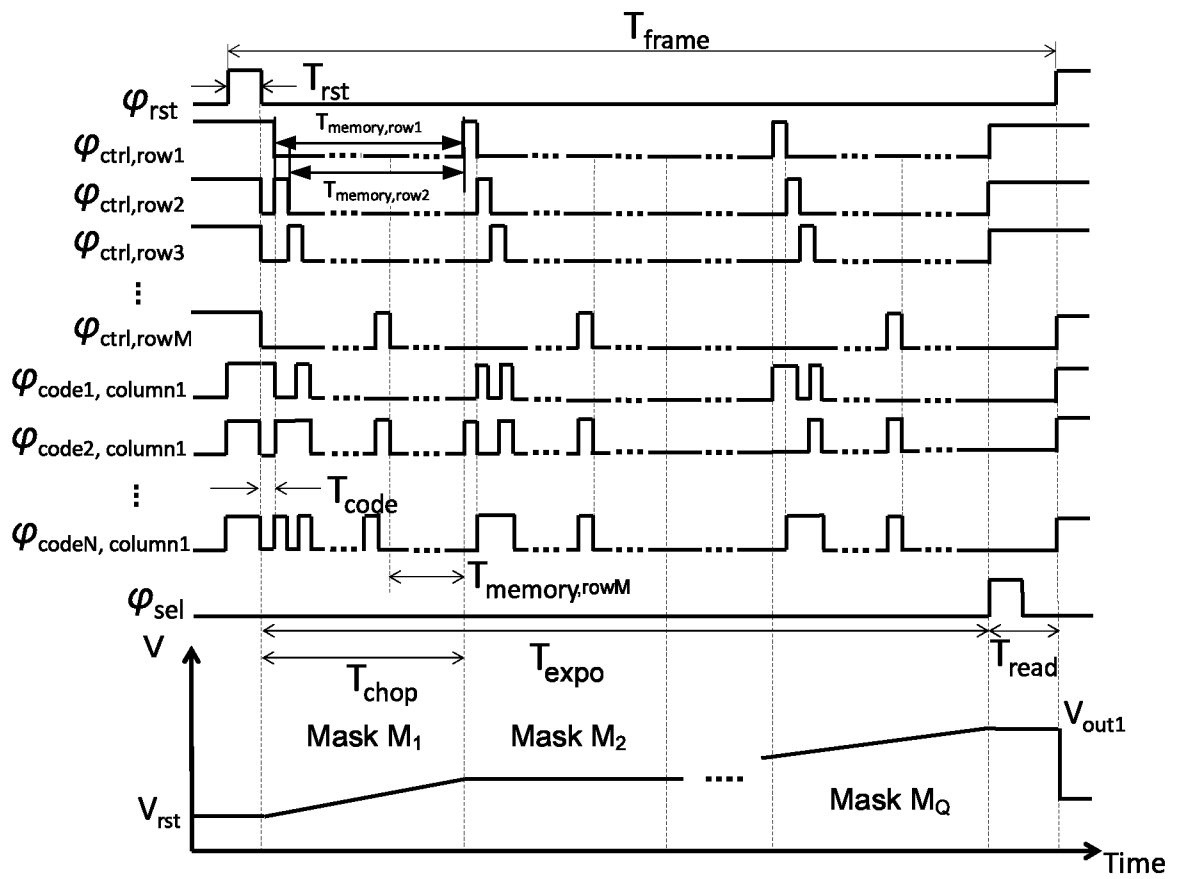


FIGURE 6D

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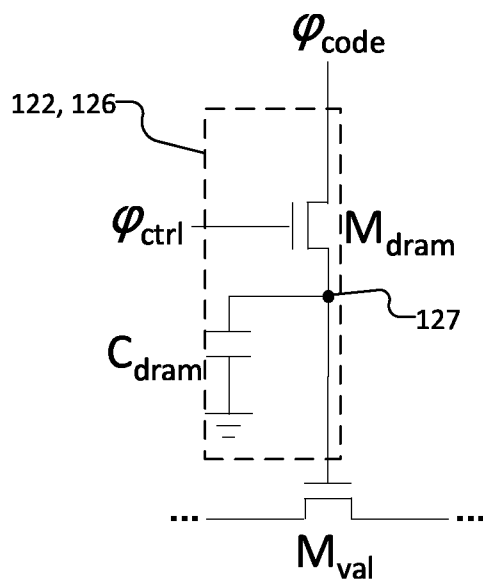


FIGURE 7A

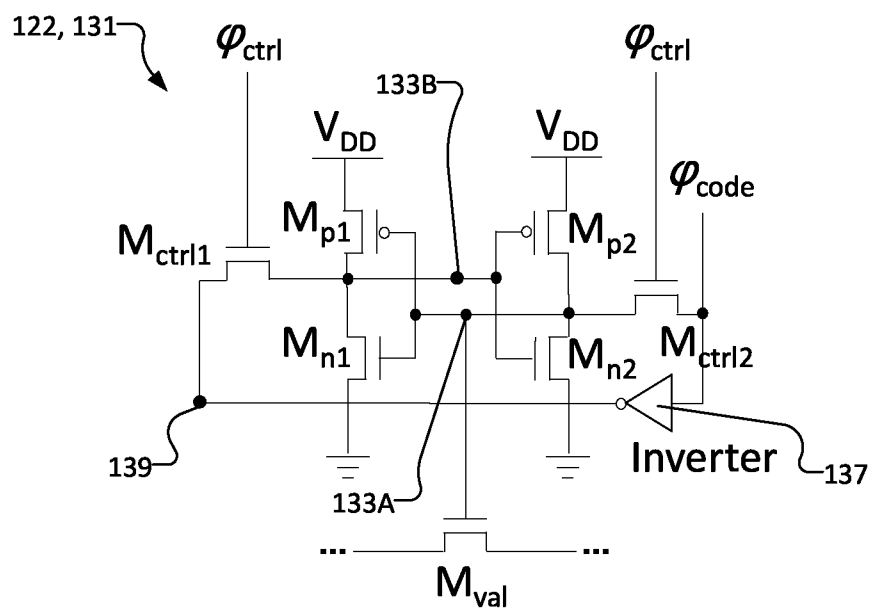


FIGURE 7B

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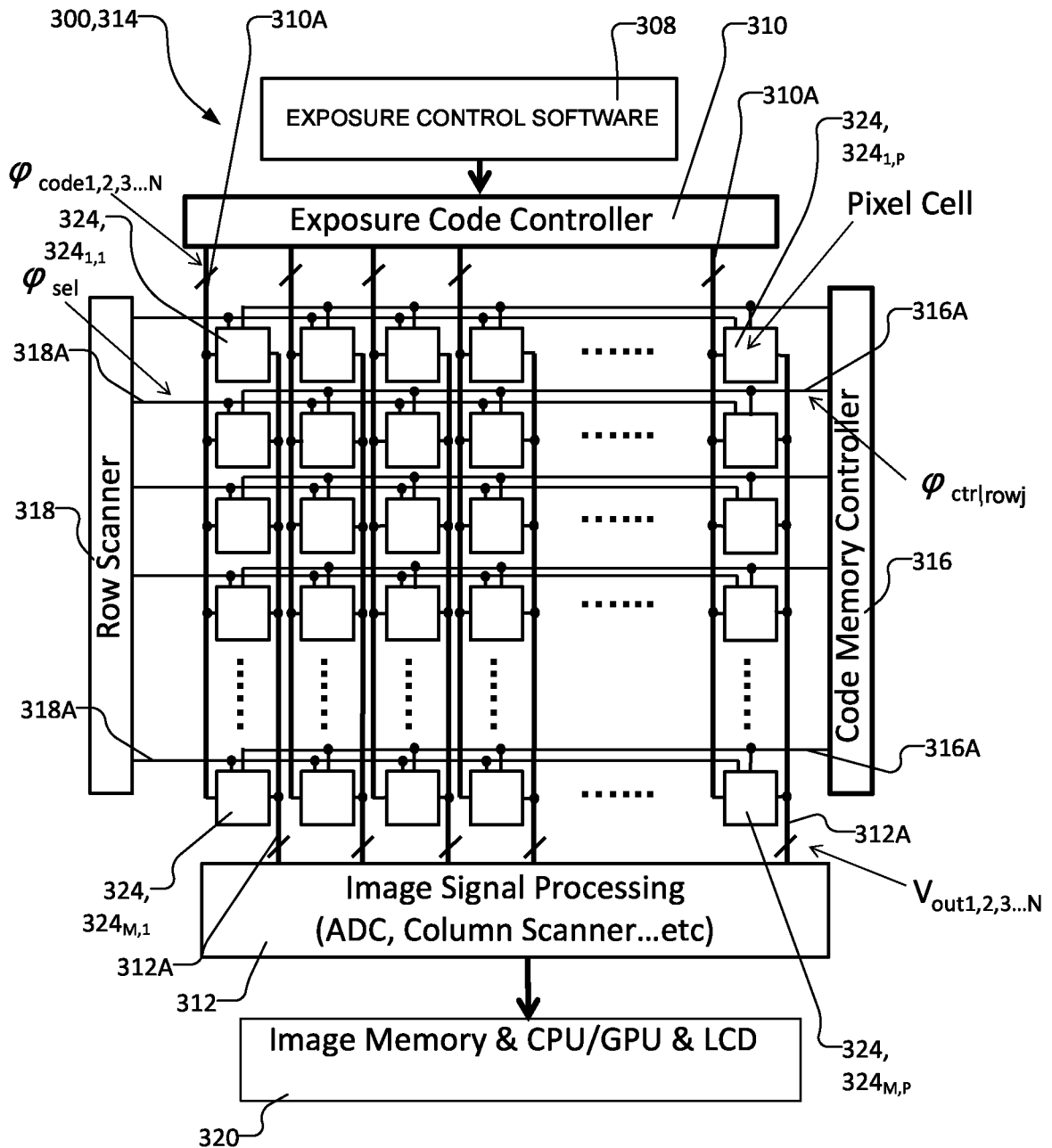


FIGURE 8

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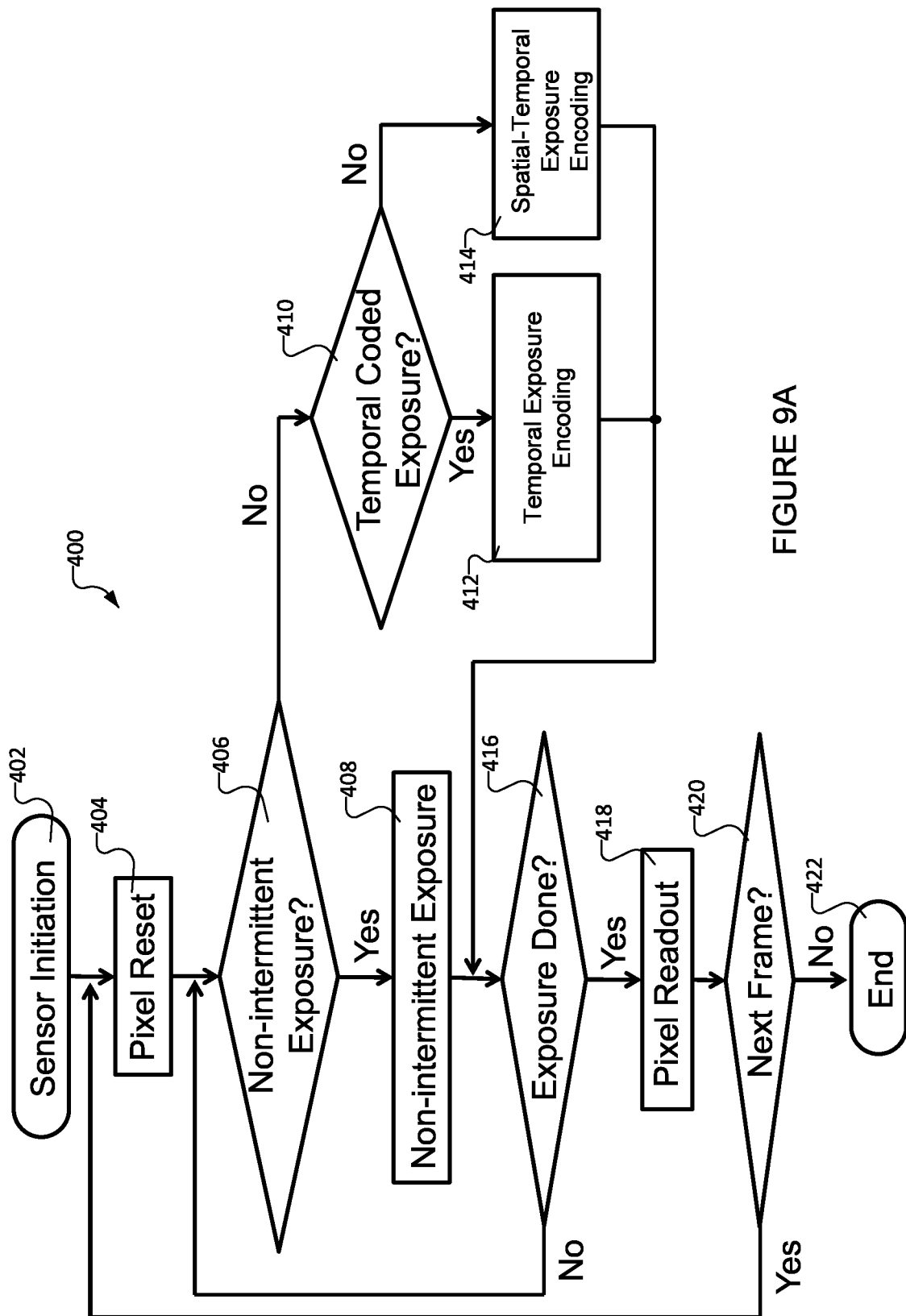


FIGURE 9A

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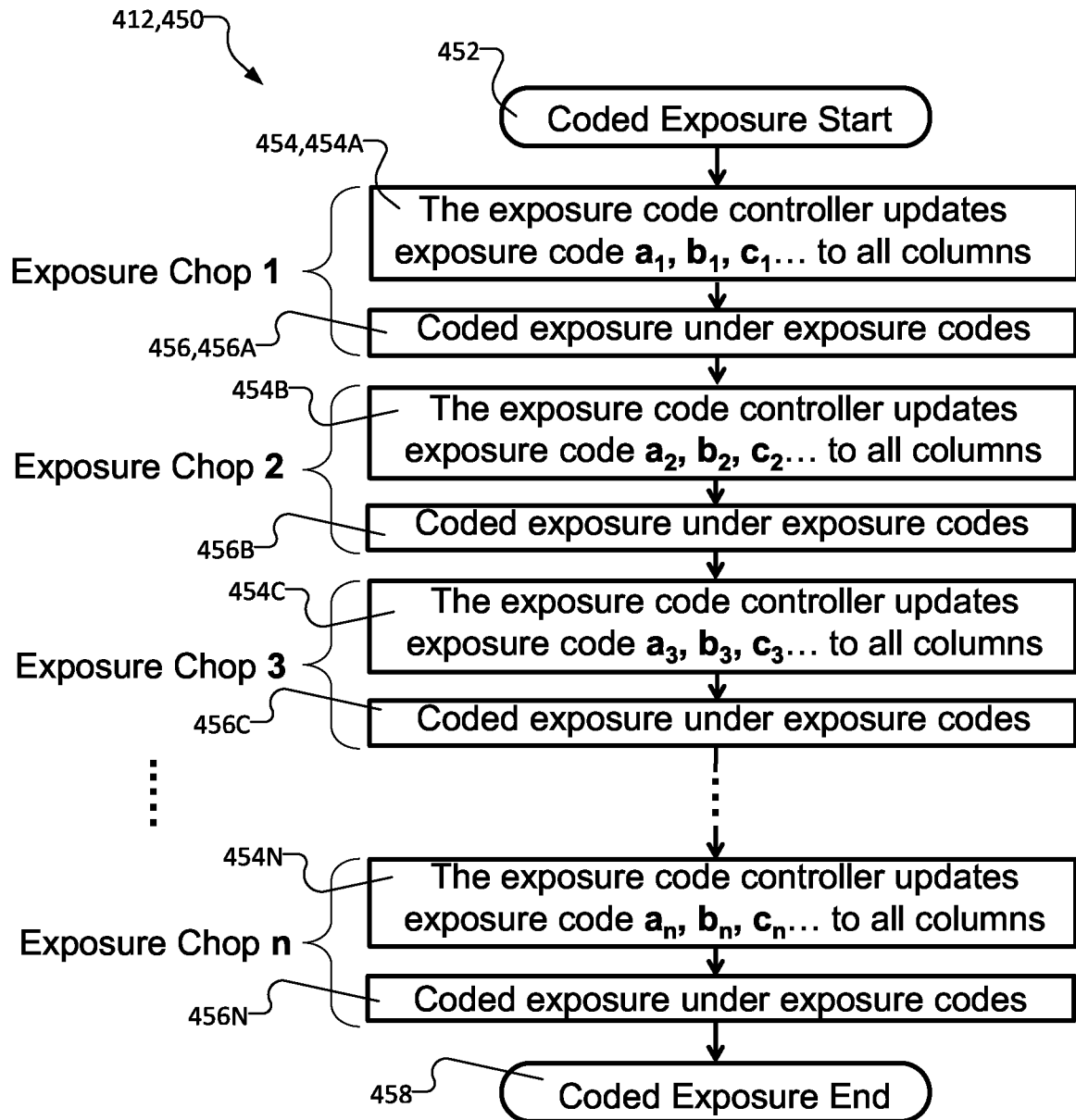


FIGURE 9B

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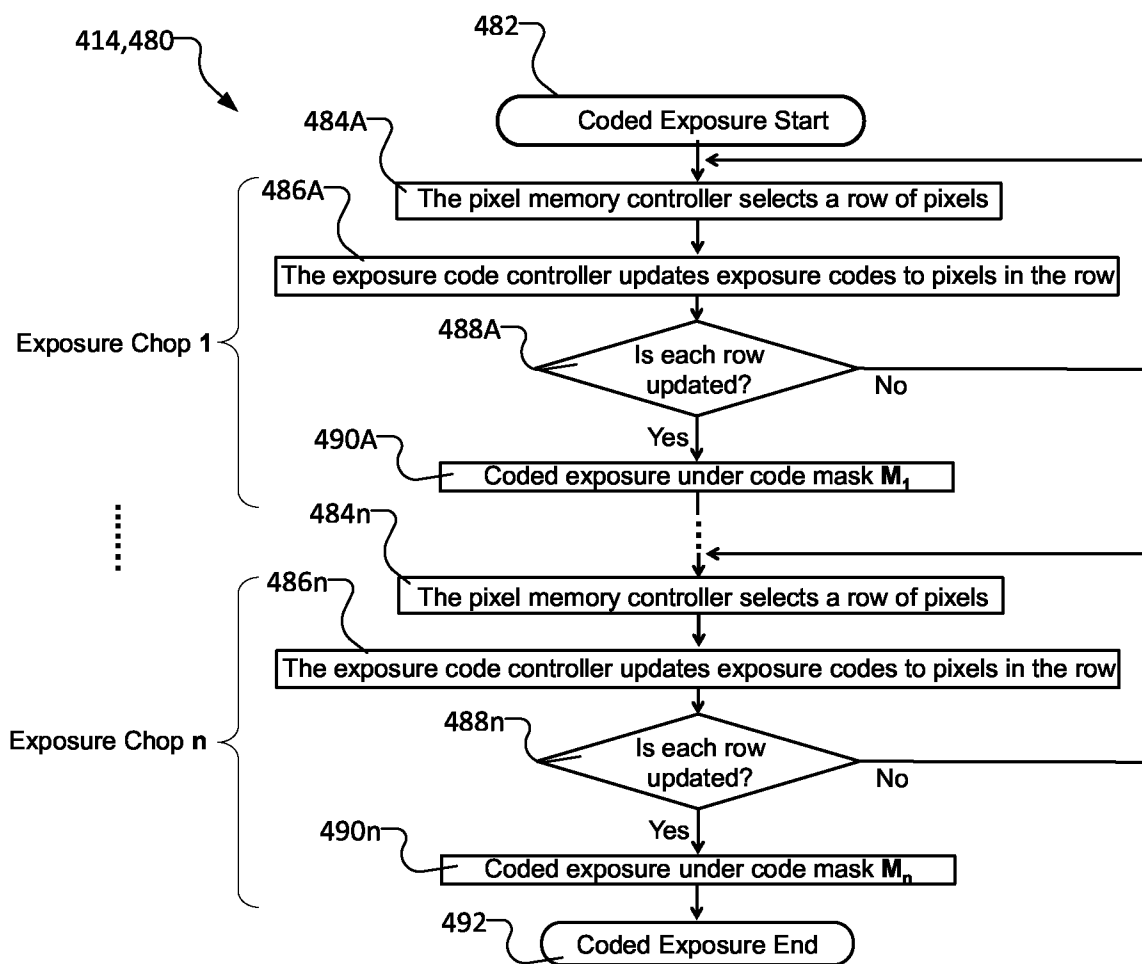


FIGURE 9C

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CA2017/050926

A. CLASSIFICATION OF SUBJECT MATTER

IPC: *H04N 5/353* (2011.01), *H01L 25/16* (2006.01), *H01L 27/105* (2006.01), *H01L 27/146* (2006.01),*H04N 5/372* (2011.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: ALL (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

Questal-Orbit, Intellect and keywords: cmos; sensor; photodetector; light; pixel/pixels; computation/computational; image/images/imaging; exposure; code; signal; charge/charges; storage; memory; time; temporal; switch; valve; gate; "APS"; active; Luo Li; Mirabbasi shahriar; University British Columbia

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/0117690 A1 (<i>Rhodes</i>) – 29 August 2002 (29-08-2002) * the whole document *	ALL
A	US 7,199,405 B2 (<i>Rhodes</i>) – 3 April 2007 (03-04-2007) * the whole document *	ALL
A	US 2001/0002045A1 (<i>Fossum et al.</i>) – 31 May 2001 (31-05-2001) * the whole document *	ALL
A	WO 97/08647 A1 (<i>Olmstead et al.</i>) – 6 March 1997 (06-03-1997) * the whole document *	ALL

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* "A" "E" "L" "O" "P"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance earlier application or patent but published on or after the international filing date document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) document referring to an oral disclosure, use, exhibition or other means document published prior to the international filing date but later than the priority date claimed	"T" "X" "Y" "&"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art document member of the same patent family
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Date of the actual completion of the international search
19 December 2017 (19-12-2017)Date of mailing of the international search report
12 January 2018 (12-01-2018)Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
Place du Portage I, C114 - 1st Floor, Box PCT
50 Victoria Street
Gatineau, Quebec K1A 0C9
Facsimile No.: 819-953-2476

Authorized officer

Reginald Linco (819) 639-8198

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CA2017/050926**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of the first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claim Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claim Nos.: 72 and 73
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

The claims attempt to claim material which is so broadly defined that this material cannot be properly searched.

3. ☐ Claim Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claim Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2017/050926

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/CA2017/050926

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