United States Patent

Braaten

[15] **3,696,409**

[45] **Oct. 3, 1972**

[54] **FINGER-TOUCH FACEPLATE**

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[22] Filed: **Dec. 28, 1970**

[21] Appl. No.: **101,752**

[52] **U.S. Cl.** .....**340/365,** 178/19, 340/324 A
[51] **Int. Cl.** **G08c 9/02**
[58] **Field of Search**.....340/365 C; 178/19

[56] **References Cited**

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Primary Examiner—Thomas B. Habecker
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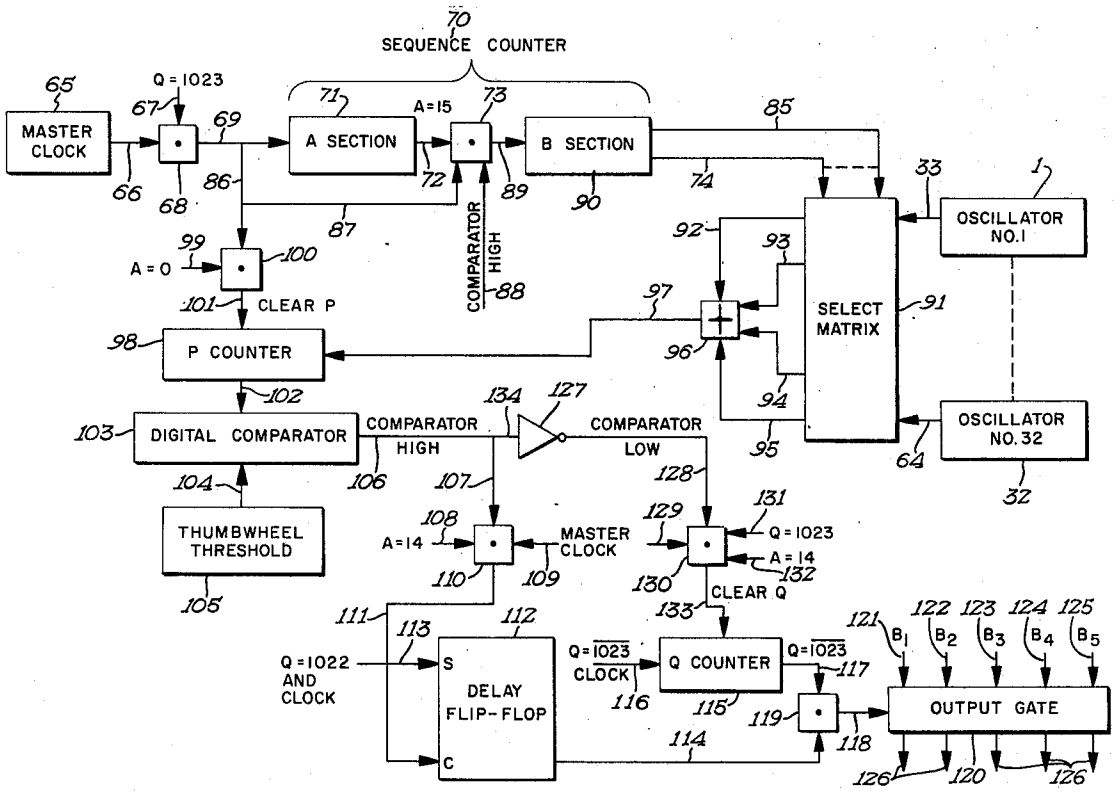
[57] **ABSTRACT**

A system for identifying a particular position on the face of a display device by simply touching the area with the finger. The area is a conductive pad connected to a relaxation oscillator whose frequency is lowered by the touch. The oscillator is therefore identifiable and a digital computer is enabled to perform a prescribed act such as new information transferred to the display device, dependent upon the location of the area touched.

6 Claims, 13 Drawing Figures



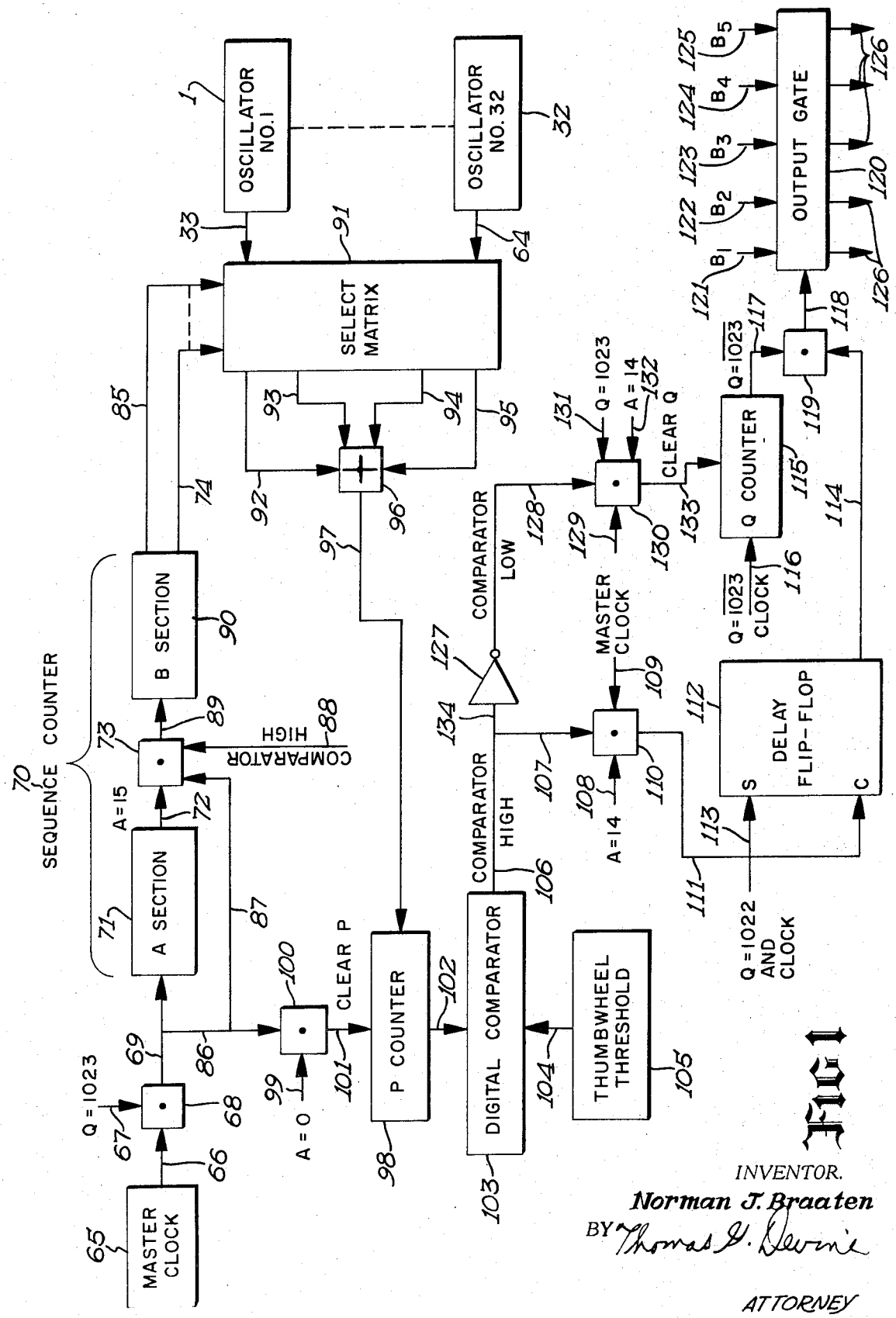


FIG. 1

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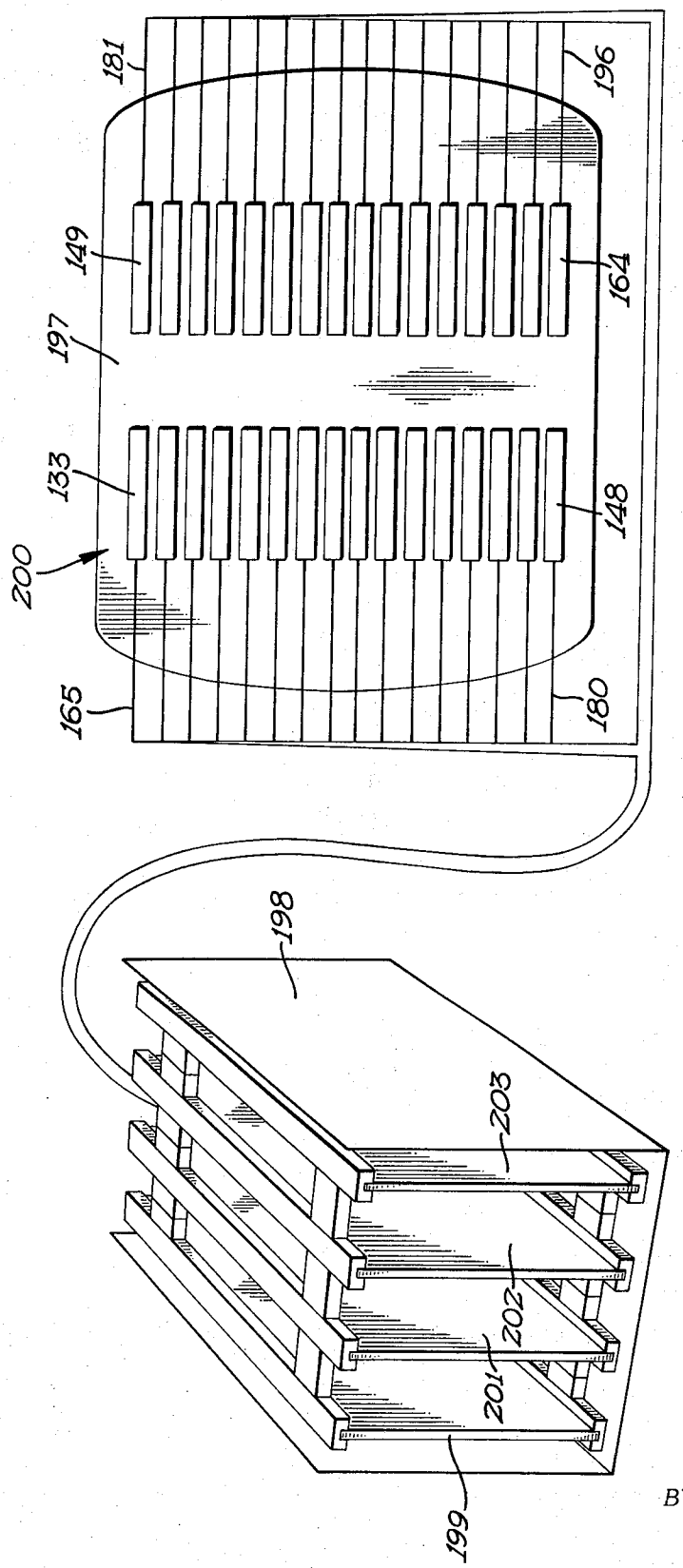

FIG 2

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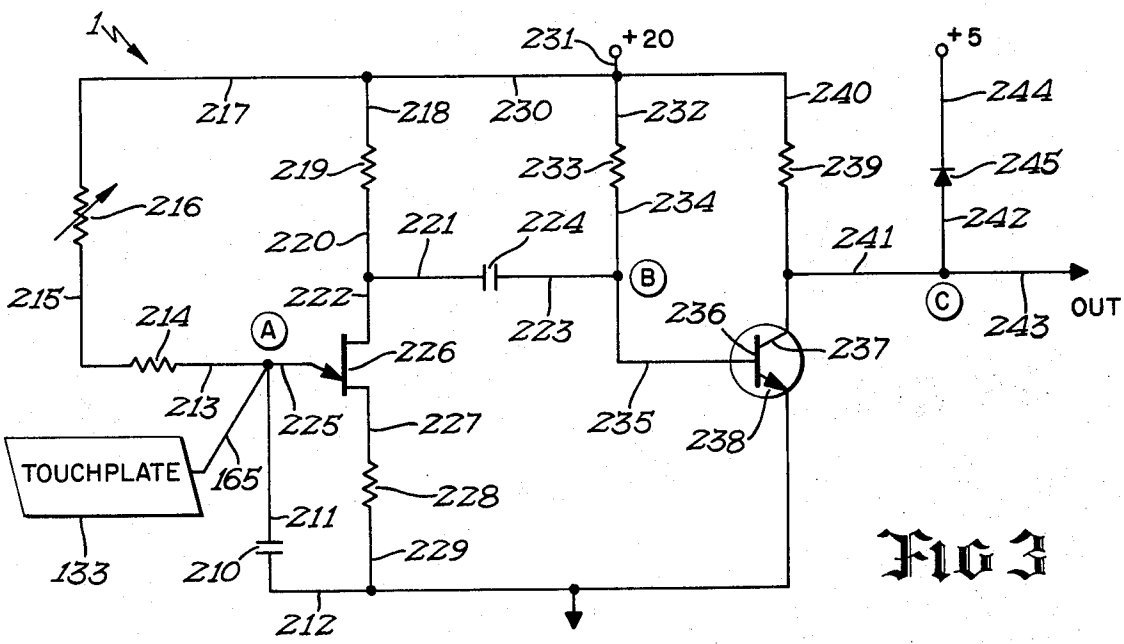

Fig 3

Fig 3A

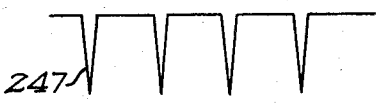

Fig 3B

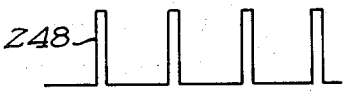

Fig 3C

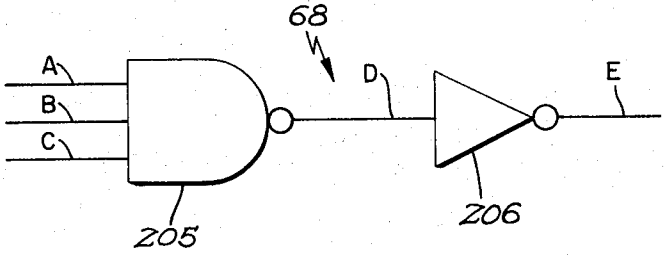

Fig 4

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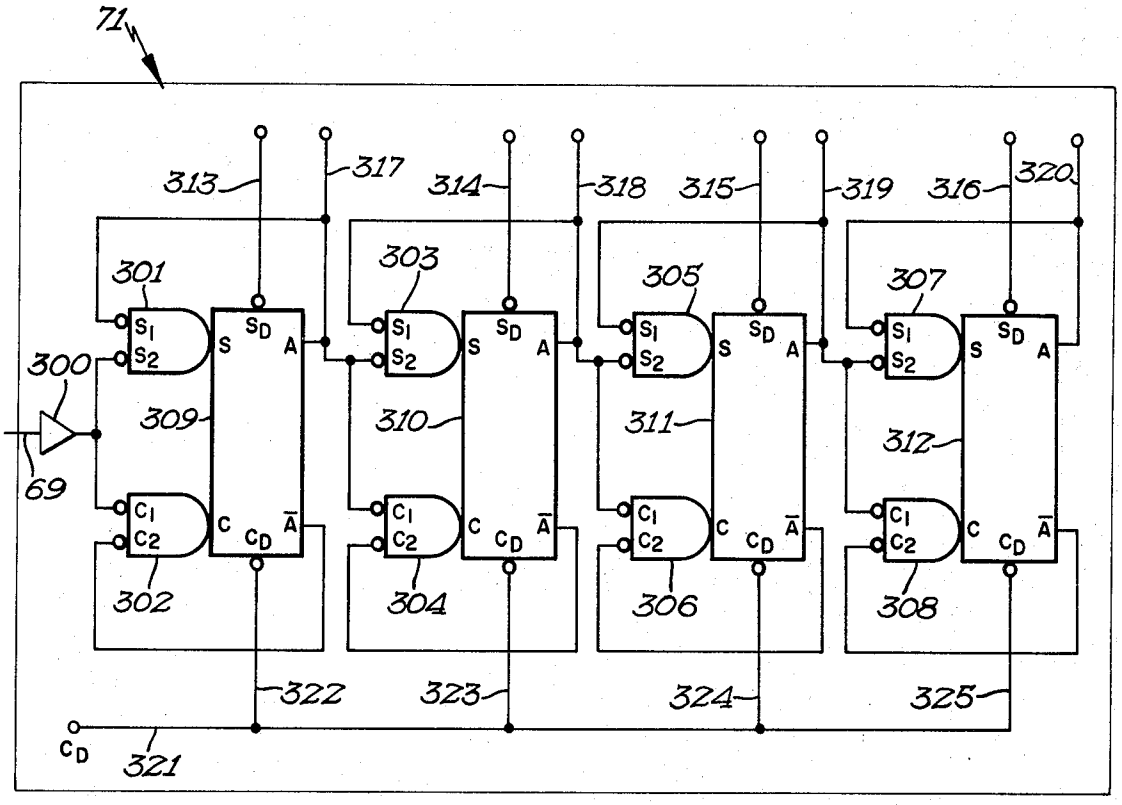

FIG 5

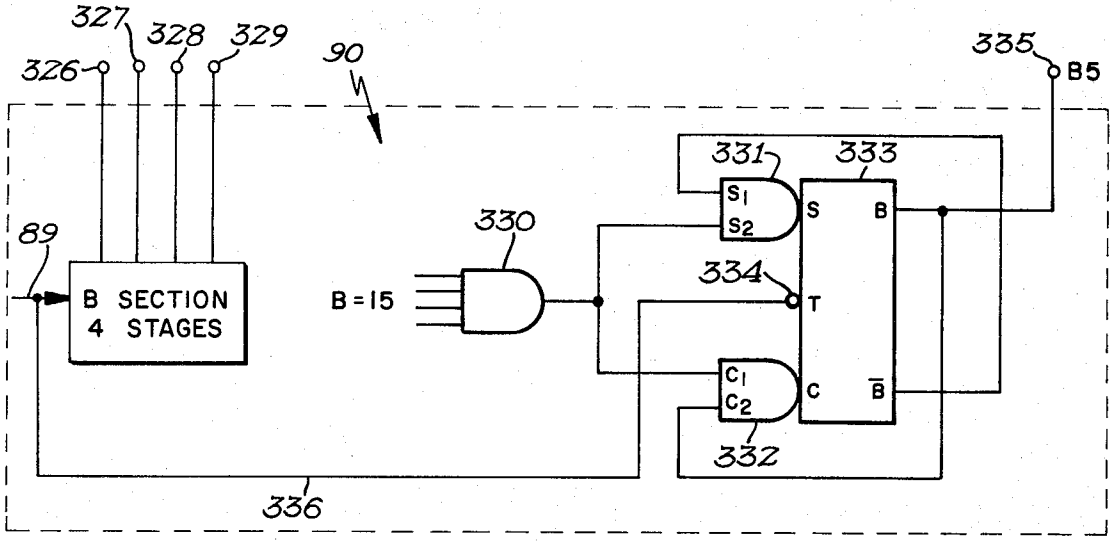

FIG 6

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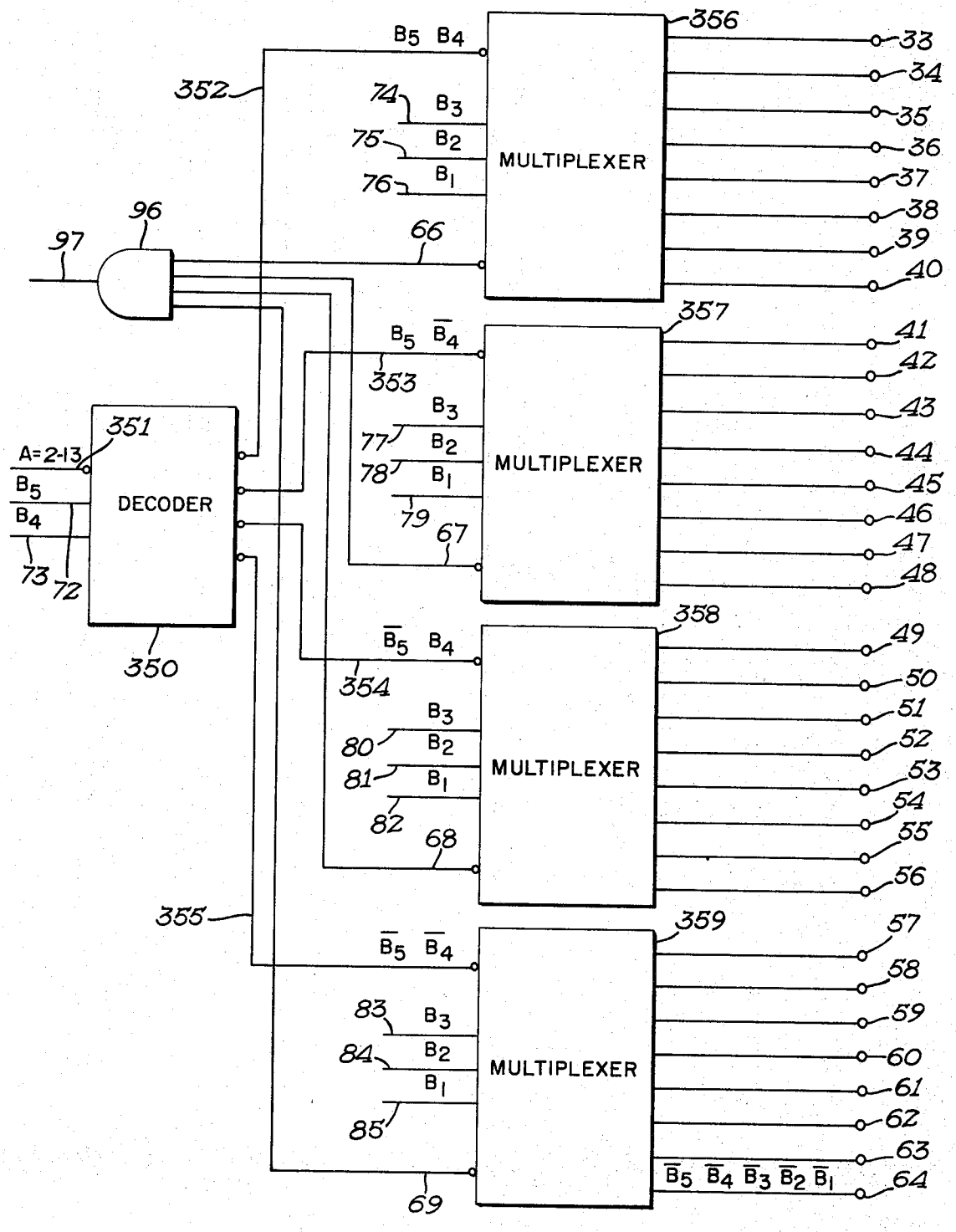

FIG 7

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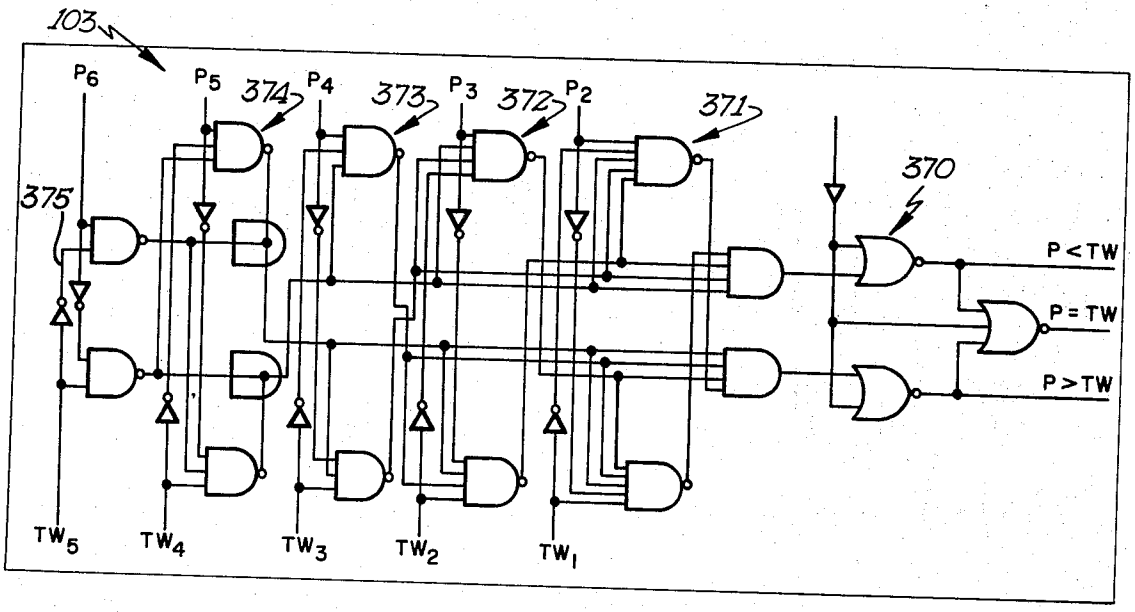
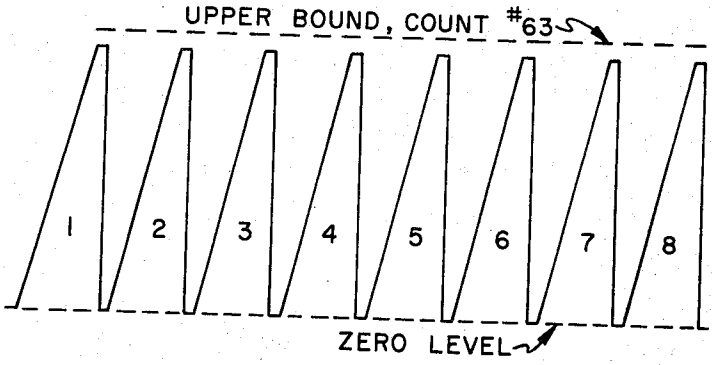
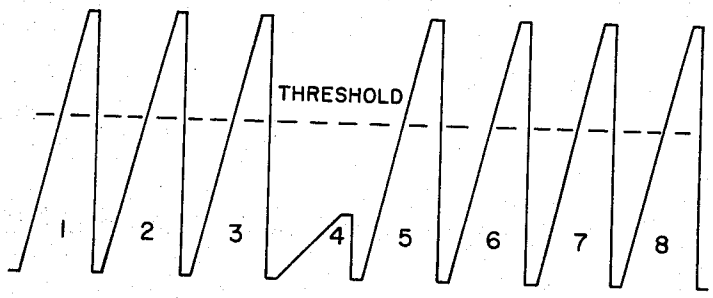


FIG 8



SCAN OF 8 OSCILLATORS (NO PAD TOUCHED) FIG 9A



SCAN OF 8 OSCILLATORS (# 4 PAD TOUCHED)

FIG 9B

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FINGER-TOUCH FACEPLATE

BACKGROUND OF THE INVENTION

Management systems and teaching systems utilizing a digital computer lend themselves very well to the use of a finger-touch faceplate. It is an excellent, simple manner of communicating with a digital computer where the interface between the operator and the computer has been the subject of much effort over the years to be made simpler.

In the prior art, there have been many efforts made to recognize a particular area on the face of a cathode ray tube display for example by touching the selected area with a conductor, with a "light pen" and with the finger. Using only the finger as a pointer has presented problems which have been successfully overcome in this invention. In prior art devices, the circuitry has been extensive and complex, but most important has not been as reliable as desired. Efforts have been made to detect a position by wire grids over the face of a display device which indicate a position when intersecting wires are pressed together to contact each other. There have also been light grids used to attempt to locate where the operator's finger is placed by interrupting the circuit of a photosensitive device. Another interesting prior art approach to solving the problem is found in U.S. Pat. No. 3,382,588 in which one or more capacitors are made a part of the faceplate of the display and are intentionally of a high leakage character. When the leakage field is interrupted by the operator's finger, the capacitive reactance is changed and a bridge circuit is upset. Another prior art approach is one where, in essence, a transmitter is placed in the area of the faceplate of the display device and the finger acts as an antenna. These devices are all highly complex. Additionally, it has been found that in many of the prior art devices which utilize cathode ray tubes as the display device, that the electron beam of the cathode ray tube causes an undesirable static charge on the areas of the faceplate to be touched.

It will be seen that the invention described herein substantially reduces or eliminates these problems.

SUMMARY OF THE INVENTION

A plurality of conductive pads are attached to the face of a display device forming a finger-touch faceplate. Each pad is electrically connected to an oscillator. It has been determined that the human body is basically capacitive. Therefore when a person touches one of the conductive pads, capacity is added in parallel to the capacitance in the RC charge path of a relaxation oscillator. The frequency of the oscillator output is therefore lowered. A recognition of the fact that the frequency has been lowered and of the indentity of the oscillator with which the touched pad is associated results in an exact identification of the pad and the fact that it has been touched by the operator. This knowledge in the form of electric signals can then be transmitted to a digital computer which will respond in a prescribed way. In the preferred embodiment it is ordinarily expected that new information will be presented on the face of the display device replacing that which the operator pointed to through the transparent conductive pad.

In the preferred embodiment, the capacitor in the charge path discharges through a unijunction transistor and then charges again. Electric charge collected on the pad as a result of the electron beam of a cathode ray tube, if a cathode ray tube is used, will be conducted from the pad and discharged through the unijunction transistor, thus keeping the faceplate free of charge.

An object of this invention is to provide an economical and reliable means for selecting a given area on the face of a display device.

Another object is to electronically identify a pad that has been touched by a person.

Another object is to permit a person to touch a desired word or symbol appearing on the face of a display device and have a change in the information displayed as a result of the touch.

Still another object is to prevent the buildup of electric charge on the face of the display device.

These and other objects will become more apparent in the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the system.

FIG. 2 is a perspective view of the conductive pads installed on a display device and the electronics package.

FIG. 3 is a schematic diagram of the relaxation oscillators used in the invention.

FIG. 3A, FIG. 3B and FIG. 3C illustrate waveforms as seen on the face of an oscilloscope at various points within the oscillator of FIG. 3.

FIG. 4 is a logic diagram of an AND circuit made up of a NAND circuit and an inverter.

FIG. 5 is a logic diagram of a typical counter used in this invention.

FIG. 6 illustrates the use of a flip-flop circuit in conjunction with a counter, as typically used throughout this invention.

FIG. 7 is a logic diagram of the select matrix of FIG. 1.

FIG. 8 is a logic diagram of the digital comparator of FIG. 1.

FIG. 9 is an analog representation of the output of eight oscillators with none of the associated pads touched and of the output of eight oscillators with one of the pads touched.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a block diagram of the system. The preferred embodiment has **32** touchplates and therefore **32** oscillators. Oscillator **1** and oscillator **32** are shown with respective outputs **33** and **64** connected to select matrix **91**. Oscillators **2** through **31** and connections **34** through **63** are not shown to avoid confusion. The select matrix **91** has outputs **92**, **93**, **94** and **95** which terminate in AND circuit **96**.

The system has a master clock **65** whose output **66** is connected to AND circuit **68** which has additional input line **67** and output line **69** which is an input to the A section **71** of the sequence counter **70**. An output **72** of the A section **71** is an input to AND circuit **73**, which has additional inputs **87** and **88**. The output **89** of AND circuit **73** is an input to B section **90** of sequence counter **70**. Output lines **74** and **85** from the B section **90** serving as inputs to select matrix **91** are shown. Output lines **75** through **84** from the B section **90** are not shown for the sake of simplicity.

Referring again to AND circuit **68**, it can be seen that an additional output line **86** terminates in AND circuit **100** which has additional input line **99**. AND circuit **100** has an output line **101** which is connected to P counter **98**. The output of AND circuit **96** is line **97** which serves as an input to the P counter **98**. Digital comparator **103** has an input **102** from P counter **98** and an input **104** from thumb-wheel threshold **105**. Digital comparator **103** has an output **106** connected to output line **107** which serves as one input to AND circuit **110**, the other inputs being line **108** and line **109**. The output **111** of AND circuit **110** serves as the "-clear" input of delay flip-flop **112**.

Referring back to digital comparator **103**, it can be seen that its output **106** also is connected to input line **134** of inverter **127** whose output line **128** is connected to AND circuit **130**. AND circuit **130** has additional inputs **129**, **131** and **132**, and has an output line **133** which is a "clear" input to Q counter **115** which has an additional input **116**.

With reference to delay flip-flop **112**, it is apparent that the "clear" output line **114** terminates at AND circuit **119** which has another input line **117** which is an output of Q counter **115**. AND circuit **119** has an output line **118** that terminates in the output gate **120** which has inputs **121** through **125** and output lines **126**.

FIG. **2** illustrates a typical display device **200** having a screen **197**. Attached to screen **197** are transparent, conductive touchplates **133** through **164**. The touchplates are typically comprised of metal oxide, well-known in the art and cemented to the face of the display device with transparent cement, also well known. To each of the touchplates is connected a conductor. For example, conductor **165** is connected to touchplate **133**, conductor **180** is connected to touchplate **148**, conductor **181** is connected to touchplate **149**, and conductor **196** is connected to touchplate **164**. There is a conductor attached to each of the other touchplates which are not shown. Each conductor is connected to a separate oscillator. For example, conductor **165** is connected to oscillator **1**, conductor **180** is connected to oscillator **32**. Conductors **165** through **196** are shown generally as entering chassis **198**. Chassis **198** contains printed circuit boards **199**, **201**, **202** and **203**. All of the oscillators and other components (not shown) are mounted on the printed circuit boards **199**, **201**, **202** and **203**. The chassis **198** need not be remote from the display device **200**.

FIG. **3** is the schematic diagram of oscillator **1** of FIG. **1**. It is identical to the other **31** oscillators of the preferred embodiment. Except for the value of capacitor **210** and the deletion of touchplate **133** and conductor **165**, it is also identical to master clock **65** of FIG. **1**. The transparent, conductive touchplate **133** is connected to the oscillator through conductor **165** at point A. Delaying capacitor **210** is connected through conductor **211** to point A and from its other plate connected to ground through conductor **212**. Unijunction transistor **226** has its emitter connected through conductor **225** to paint A. Its base **2** is connected to a positive voltage source through conductor **222**, conductor **220**, resistor **219**, conductor **218**, conductor **230** and conductor **231**. Its base **2** is also connected to coupling capacitor **224** through conductor **221**. Its base **1** is connected to ground through conductor **227**, resistor **228** and conductor **229**. Variable resistor **216** is connected to the positive voltage source at one side through conductors **217**, **230** and **231**. At its other end, resistor **216** is connected to resistor **214** through conductor **215**. The other side of resistor **214** is connected to point A through conductor **213**. The combination of resistors **216** and **214**, together with capacitor **210** form the delay circuit for the oscillator.

The other plate of capacitor **224** is connected through conductor **223** to point B. The base of transistor **236** is connected to the positive voltage source through conductors **235** and **234**, and through resistor **233** and conductors **232** and **231**. The emitter of transistor **236** is connected through conductor **238** to ground. The collector of transistor **236** is connected to the positive voltage source through conductor **237**, resistor **239**, conductor **240** and conductor **231**. The output from transistor **238** is taken from its collector through conductor **241** to point C and out on conductor **243**. Point C is kept at a specified positive voltage by diode **245** connected at its anode to point C through conductor **242** and at its cathode through conductor **244** to a positive voltage source.

FIG. **3A** is a representation of the voltage waveform at point A of FIG. **3**. The waveform **246** is a plot of voltage in the Y direction versus time in the X direction.

FIG. **3B** is a representation of the voltage waveform at point B of FIG. **3**. Waveform **247** is representative of voltage in the Y direction and time in the X direction.

FIG. **3C** is representative of the voltage at point C of FIG. **3**. Wave **248** represents voltage in the Y direction and time in the X direction, illustrating the pulse output of the relaxation oscillator of FIG. **3**.

Throughout this discussion, the AND circuit is discussed. In practice the NAND circuit is more readily available in integrated circuits. FIG. **4** illustrates AND circuit **68** having NAND circuit **205** with inputs A, B and C and output D. When A, B and C are all "up", D is "down", mathematically expressed as a Boolean equation:

$$D=\bar{A}\cdot\bar{B}\cdot\bar{C}$$

A simple inverter **206** whose input is D and whose output is E is connected to the NAND circuit **205** in series. When D is "up", E is "down" and vice versa. Expressed mathematically in Boolean form:

$$E=\bar{D}$$

$$E=A\cdot B\cdot C$$

This is readily understood to be a design choice in the use of integrated circuits. FIG. **4** shows a simple AND circuit which is comprised of a NAND circuit and an inverter. All of the AND circuits referred to herein are of similar configuration.

FIG. **5** is a logic diagram of a well-known counter, old in the art. Flip-flops **309**, **310**, **311** and **312** have set inputs from circuits **301**, **303**, **305** and **307** respectively. They have "clear" inputs from circuits **302**, **304**, **306** and **308** respectively. This counter is indicated generally as A section **71** of FIG. **1**. Outputs are indicated at **317**, **318**, **319** and **320** in ascending order. The flip-flops are provided with force-set inputs indicated as **313**, **314**, **315** and **316**. The flip-flops also have force-clear inputs indicated at **322**, **323**, **324** and **325**. The input signal coming from AND circuit **67** of FIG. **1** enters through amplifier **300**.

FIG. 6 is a logic diagram showing the B section **90** (FIG. 1) of the sequence counter **70**. The lower four stages of the B section are configured exactly the same as the four stages of the A section **71** shown in detail in FIG. 5. The uppermost stage of the B section is comprised of AND circuit **330**, whose inputs are the lower section outputs **326**, **327**, **328** and **329**, and flip-flop **333**, whose inputs are AND circuit **331** and on the "-set" side, AND circuit **332** on the "clear" side and terminal **334** which conditions flip-flop **333**. The set output of flip-flop **333** is shown at terminal **335**.,

Referring now to FIG. 7, the select matrix **91** of FIG. **1** is shown in logic form. Decoder **350** has as its inputs the highest order bit (B_5) on line **72** and the next highest bit (B_4) on line **73** and an "enable" on line **351** which permits the decoder to operate when the A section of the sequence counter **70** of FIG. **1** is $\overline{0}$, $\overline{1}$, $\overline{14}$ or $\overline{15}$. Decoder **350** has four outputs, line **352** which is connected to multiplexer **356**, line **353** which is connected to multiplexer **357**, line **354** which is connected to multiplexer **358**, and line **355** which is connected to multiplexer **359**. The three remaining lower order bits of the B section (B_3, B_2 and B_1) are connected to each of the four multiplexers. The inputs are shown at lines **74**, **75** and **76** of multiplexer **356**; lines **77**, **78** and **79** of multiplexer **357**; lines **80**, **81** and **82** of multiplexer **358**; lines **83**, **84** and **85** of multiplexer **359**. The output line from each of the oscillators **1** through **32** of FIG. **1** are shown as lines **33** through **64**, eight being an input to each of the four multiplexers.

Each of the multiplexers has an output through which the output of a selected oscillator passes. The operation will be described later. Multiplexer **356** has an output **66**, multiplexer **357** has an output **67**, multiplexer **358** has an output **68** and multiplexer **359** has an output **69**. The outputs are connected as the inputs to OR circuit **96** of FIG. **1** whose output is line **97**. An OR circuit is simply one that is responsive to any one of a multiplicity of inputs.

The P counter **98** of FIG. **1** is made the of a pair of counters in identical configuration with the sequence counter **70** except that not as many counter stages are used. The operation will be fully described later.

The thumb-wheel threshold **105** of FIG. **1** is a simple rotary thumb-wheel switch, old in the art. In the preferred embodiment, the thumb-wheel threshold **105** has five outputs each of which is adjustable to ground or an open circuit. Line **104** of FIG. **1** represents the five outputs of thumb-wheel threshold **105**. In similar fashion, line **102** of FIG. **1** represents five outputs from P counter **98**.

FIG. **8** is a detailed logic diagram of digital comparator **103** of FIG. **1**. It is well-known in the art and therefore will not be described in detail. Its inputs from the P counter **98** are shown as P_6, P_5, P_4, P_3 and P_2. The lowest stage of P is not used in this application. Its inputs from the thumb-wheel threshold **105** and shown as TW_5, TW_4, TW_3, TW_2 and TW_1. The stages are shown generally as **375**, **374**, **373**, **372** and **371**. In each stage the inputs are compared to each other and at the output **370** it can be determined whether P is less than TW, whether P equals TW or whether P is greater than TW. In the preferred embodiment, only the output indicated as P is greater than TW is used.

FIG. **9** is of interest only as a graphic illustration of an analog representation of eight of the oscillators. The output of the P counter **98** is run into a digital-to-analog converter (not shown) and the pulse train from each of the eight pads shown scanned may then be viewed on an oscilloscope as an amplitude rather than a frequency. This is old in the art and is only for purposes of illustration.

FIG. 9A shows the resultant amplitude output of eight oscillators with no touchplate (referred to as "-pad" in this figure) being touched. FIG. 9B shows the pad for oscillator No. **4** being touched and its representation of frequency now as an amplitude is shown being quite low and below a threshold frequency set by the thumb-wheel threshold switches of thumb-wheel threshold **105**.

The delay flip-flop **112** of FIG. **1** is identical to the flip-flop **333** of FIG. **6**. It also is old in the art and need not be shown in detail. The Q counter **115** of FIG. **1** is made up of counters identical to the configuration of the sequence counter **70** and therefore need not be described in detail.

The output gate **120** of FIG. **1** is simply five AND circuits which have been described in FIG. **4**. Outputs **126** of output gate **120** are available as inputs to any desired device. Typically, the application is to the buffer register of a digital computer. The output is of course not limited to such an application.

MODE OF OPERATION

FIG. **3** is a detailed schematic diagram of the oscillators **1** through **32** of FIG. **1** as well as master clock oscillator **65** of FIG. **1**. As indicated earlier, the difference between the master clock oscillator **65** and all other oscillators **1** through **32** is that the capacitor **210** is of a higher capacitance and there is no touchplate **133** or conductor **165**. The relaxation oscillator here shown is of itself old in the art, particularly with reference to the master clock oscillator **65**.

Simply stated, in the case of the master clock oscillator **65**, adjustable resistor **216**, resistor **214** and capacitor **210** form a charging path for capacitor **210**. When capacitor **210** is charged to a critical value, the potential thereby appearing at paint A causes the unijunction transistor **226** to conduct providing a discharge path through the unijunction transistor **226**, resistor **228**, back to the other plate of capacitor **210**. The discharge is rapid, dropping the potential at point A resulting in the cutoff of unijunction transistor **226**. The charge cycle starts again, resulting in capacitor **210** again becoming charged to cause the conduction of unijunction transistor **226** permitting a discharge path through resistor **228**. This is a typical relaxation oscillator. The charge and discharge of capacitor **210** results in the waveform of point A shown in FIG. 3A.

The output of base **2** of unijunction transistor **226** is coupled to point B via capacitor **224** and is shown in FIG. 3B as it appears at point B of FIG. 3. That waveform is inverted and amplified in NPN transistor **236**. The output waveform is shown at FIG. 3C which is the collector output at point C of transistor **236**. The diode **245** conducts when point C tends to go beyond +5 volts, resulting in a shaped waveform of FIG. 3C. The frequency of the pulses of FIG. 3C may be varied by varying the charge path of capacitor **210** by changing the resistance of variable resistor **216**.

The oscillators **1** through **32** are each provided with a touchplate and a conductor as an input. In FIG. **3** the touchplate **133** is connected to the circuit through conductor **165**.

It has been determined that the human body is basically capacitive. The capacitance varies with the size of the body but not significantly. When a person touches touchplate **133**, capacitance is added in parallel with capacitor **210**. This added capacitance results in a larger RC time constant in the charge path. A preselected frequency of output pulses as shown in FIG. **3C** is thereby lowered with the addition of capacitance at touchplate **133**. The operation as described above for the master clock oscillator **65** is identical to that of oscillators **1** through **32** except that the frequency is lowered by adding capacitance in the latter case. Recognizing the oscillator (and therefore the touchplate) and the fact that its frequency is lowered, is at the heart of this invention.

Referring to FIG. **1**, sequence counter **70**, P counter **98**, and Q counter **115** are shown. In the preferred embodiment, the A section **71** of sequence counter **70** has four binary stages and the B section **90** of sequence counter **70** has five binary stages. The P counter **98** has six binary stages and the Q counter **115** has nine binary stages. As is well-known in the art, each binary stage can be represented by two different voltage amplitudes. An arbitrary selection can be made assigning, for example, a "one" to a voltage and a "zero" to a ground potential. If all four stages are "one" the binary number represented is 1111, but for simplicity it will be referred to in its decimal equivalent as 15. Likewise the B section when filled is 31, the P counter when filled is 63 and the Q counter when filled is 1023. The Q counter **115** is ordinarily set at 1023 because its input **116** depends upon an output from the master clock **65** and the fact that $Q=\overline{1023}$.

The master clock **65** produces pulses as shown in FIG. **3C** in a manner described above at a rate of 4×10^3 PPS in this preferred embodiment. These pulses are transmitted over output line **66** to the AND circuit **68**. AND circuit **68** is shown in FIG. **4** with the Boolean expressions set out above. When there is a pulse out of master clock **65** on line **66** and when Q=1023 on line **67** the output of the AND circuit **68** on line **69** is active only when both of such inputs are present. Determining that Q=1023 is simply done by appropriate AND circuits logically arrayed in one of a variety of possible configurations, well known in the prior art. Another output **86** of AND circuit **68** goes to AND circuit **100** which has another input **99** requiring that A=0 in order for the output line **101** to be activated which is a "clear input" to P counter **98**.

FIG. **5** shows the A section **71** of sequence counter **70** in logic detail. The signal coming in on line **69** is amplified through amplifier **300** and sets the first stage of the counter, defined as circuits **301** and **302**, to receive the inputs and flip-flop **309** whose output "A_1" is shown at **317**. The reception of another pulse through amplifier **300** toggles the first stage and sets the second stage whose output "A_2" is shown at **318**. Another input pulse sets the first stage so that output A_1 is again A_1. Another pulse toggles the first and second stage and sets the third stage whose "one output" at "A_3" is shown at **319**. In like manner the stages are toggled back and forth until all four are "1's". When A=15 (filled) line **72** is activated. AND circuit **73** receives an input from AND circuit **68** and a signal that the digital comparator **103** is "high" as shown on line **88**. This will be explained later. Assuming that line **88** has a signal present and assuming that line **87** has a clock pulse, then AND circuit **73** passes a pulse on line **89** to the B section **90** of sequence counter **70**. This is merely an extension of the A section **71**.

The B section **90** is shown is greater detail in FIG. **6**. The four lower order bits of the B section are identical to the configuration of the A section **71** of FIG. **5** and need not be shown. A fifth stage is supplied by a flip-flop **333**. The flip-flop **333** is well-known in the prior art. It is conditioned at terminal **334** from line **336** when the lower four stages of the B section **90** are filled (B=15), then the four inputs to AND circuit **330** are activated and the last stage **333** is toggled to a "1" state.

However, prior to the toggling of any of the stages in the B section **90**, when B=0, output lines **74** through **85** convey that fact to select matrix **91**.

Select matrix **91** is shown in logical detail in FIG. **7**. Decoder **350** is a device well-known in the prior art which simply provides the four possible combinations for two binary signals. When B=0, then B_5 on input line **72** equals **0** and B_4 on input line **73** equals **0**. The four possible outputs are $B_5 \cdot B_4$, $B_5 \cdot \overline{B_4}$, $\overline{B_5} \cdot B_4$ and $\overline{B_5} \cdot \overline{B_4}$. With $B_5=0$ and $B_4=0$ then line **355** is activated as an enable input to multiplexer **359**. Multiplexer **359** has inputs B_3, B_2 and B_1 on input lines **83**, **84** and **85** respectively. The multiplexer **359** is a device well known in the prior art which takes three control inputs and combines those three inputs in the eight possible gating combinations to gate as an output one of the eight inputs. Additionally, the enable input on line **355** is also placed on all eight outputs **57** through **64**. The eight possible combinations of B_1, B_2 and B_3 are as follows:

$B_3 \cdot B_2 \cdot B_1$	$B_3\ B_2\ B_1$
$B_3 \cdot B_2 \cdot B_1$	$B_3\ B_2\ B_1$
$B_3 \cdot B_2\ B_1$	$B_3 \cdot B_2\ B_1$
$B_3 \cdot B_2\ B_1$	$B_3 \cdot B_2 \cdot B_1$

When B=0 output **64** carrying the function $B_5 \cdot B_4 \cdot B_3 \cdot B_2 B_1$ is activated. This permits the oscillator connected to line **64** to send its pulses through the multiplexer and on line **69** to OR circuit **96**, out on line **97**. The selection of line **64** has been shown for illustrative purposes. Multiplexers **356** through **359** operate in identical fashion on each of the eight input lines except that the conditioning signals from decoder **350** are different. In each case, one line of any one multiplexer can be selected thereby selecting a specific oscillator.

Referring to FIG. **1**, P counter **98** accepts the pulses from the selected oscillator from line **97** to P counter and begins counting the pulses from the selected oscillator. The time period during which the pulses are counted is measured by the counting of the clock pulses by the A section **71**.

It has been determined that approximately 60 pulses counted in the P curve **98** (high count capacity = 63) is very workable in the preferred embodiment. The master clock **65** operates at 4×10^3 PPS those pulses being transmitted into the A section **71**. However, various counts of A are not available for measuring the

time of counting in the P counter **98**. When A=0, the P counter **98** is cleared. When A=14, the output of digital comparator **103** is gated out at AND circuit **110** and AND circuit **130**. When A=15, AND circuit **73** is enabled, permitting a pulse to go through line **89** into the B section **90**. Therefore, the time period measured by the A section **71** is from A=2 to A=13, a count of 12 clock pulses.

$T = 1/f$

Where

T = period

F = frequency

$T = (1\times10^{-3}/4$

$T = 0.25\times10^{-3}$

Total time (12 pulses)	= 12T
Total time	= $12\times0.25\times10^{-3}$
Total time	= 3×10^{-3}

Since 60 pulses is a good number for counting in the P counter, a minimum frequency is required to provide at least 60 pulses within the count period time of 3×10^{-3} seconds. The period (T) of one of 60 pulses equals the total time available divided by the number of pulses; therefore:

$T = (3\times10^{-3}/60)$

$T = 5\times10^{-5}$

$F = (1/5)\times10^{5} = 20\times10^{3}$ PPS.

The oscillators must be able to provide a minimum of 20,000 pulses per second to meet the design requirements of this system.

As stated before, the oscillators **1** through **32** have been designed to produce 20×10^{3} PPS in this preferred embodiment.

Keeping in mind that the A section **71** counts 16 pulses, the actual time spent for counting the pulses of each oscillator is 3×10^{-3} for the actual count and 1×10^{-3} seconds for housekeeping details between counts.

Actual scan time = $32\times4\times10^{-3} = 128\times10^{-3}$ seconds

System Frequency = $(1\times10^{3}/128)$ = 7.8 cycles per second

As those skilled in the art well know, these parameters are merely indicative of the preferred embodiment but are subject to wide variation dependent upon the components and specific circuit embodied.

Referring again to FIG. **1**, the thumb-wheel threshold is set to represent 40 pulses. In the preferred embodiment, thumb-wheel threshold **105** has only five bits and therefore the binary equivalent of **40** cannot be set but the lowest order bit of the binary equivalent of **40** is ignored and the other bits are transmitted into digital comparator **103**. Digital comparator **103** is shown in FIG. **8** and the signals from thumb-wheel threshold **105** come in at TW_5, TW_4, TW_3, TW_2 and TW_1.

As the pulses from the selected oscillator are being counted in P counter **98**, the count from the P counter is continually transmitted to digital comparator **103**. The P counter has six bits, but only the upper five are used because of the five-bit digital comparator **103**. The inputs from the P counter enter the digital comparator **103** as P_6, P_5, P_4, P_3 and P_2. In FIG. **8** it can be seen that three outputs are available:

$P<TW$

$P=TW$

$P>TW$

In the preferred embodiment, only the P>TW output is used. That is, when the count of the P counter, when A=14, is greater than the count of the thumb-wheel threshold **105**, line **106** has a positive pulse present. Assuming that the selected oscillator had not been touched and its frequency remained therefore at 20×10^{3} PPS, 60 pulses would have been counted in the prescribed time in the P counter, such a count being higher than the thumb-wheel threshold **105** setting of 40 resulting in a "comparator high" signal out on line **106**. This condition would result in a signal present on line **107** to AND gate **110** enabled by the master clock at **109** and by A=14 at **108**. The output of AND circuit **110** is **111** and is a "clear" input to delay flip-flop **112** resulting in a "clear" output on line **114** into AND circuit **119**.

Referring again to output **106** of digital comparator **103**, when the comparator is "high", a signal is presented through line **134** to inverter **127** which then presents a ground level to line **128** which does not permit enabling of AND circuit **130** and therefore Q counter **115** is not "clear" but remains at a count 1023. The output **117** of Q counter **115** is enabled only when $Q=\overline{1023}$ and therefore is not enabled in this situation. Therefore AND circuit **119** does not present a signal to output gate **120** over line **118**. As a result, there are no output signals permitted through the output lines **126**.

Now assume a person touches the touchplate of the selected oscillator. The operation is identical to that described above except that now the capacitance of the body of the person touching the touchplate is added in parallel to the capacitance **210** of FIG. **3**. As described earlier, this results in a reduced frequency output from the selected oscillator. Under such circumstances, when A=14, the count from the P counter will be less than 40 which has been set into the digital comparator **103** from the thumb-wheel threshold **105**. When that occurs, the output on line **106** from digital comparator **103** will be grounded and the ground will be present on line **107** to AND circuit **110** thereby disenabling that AND circuit. However, the ground voltage presents itself on line **134** to inverter **127** which inverts that signal to a positive voltage. The positive pulse presents itself to AND circuit **130** which is further conditioned by the master clock at input **129**, A=14 at input **132** and Q=1023 at input **131**. Therefore, AND circuit **130** is enabled and the "clear" Q output **133** is enabled clearing the Q counter **115**. The delay flip-flop **112** is still cleared at this time and therefore line **114** has a positive voltage present. Line **117** now has a positive voltage present and Q=0. Output gate **120** is enabled through line **118** and the appropriate location as indicated by the B section **90** of sequence counter **70** is transmitted to a buffer through output lines **126**. The appropriate location or address from the B section **90** comes in through B_1, B_2, B_3, B_4 and B_5 on input lines **121, 122, 123, 124** and **125** of output gate **120**.

Q counter **115** immediately begins to count back to **1023** as a result of input **116** which requires only a pulse from master clock **65** and $Q=\overline{1023}$. When Q=1022, delay flip-flop **112** is set through input **113**. The clear output **114** is disabled, disabling AND circuit **119**. If the person touching the touchplate does not remove his finger after the cycle has been completed, it is assumed that he did not intend touching the same

touchplate twice. The preferred embodiment is designed to preclude the possibility of sending the same information through output lines **126** in a successive cycle. Referring to FIG. **1**, AND circuit **73** is disabled because the comparator is "low" and therefore input **88** to AND circuit **73** is disabled. Therefore, the B section **90** count remains the same. As the finger is kept on the touchplate for another cycle, the digital comparator remains "low" and Q counter **115** is again cleared as described earlier. However, output line **111** from AND circuit **110** is not enabled and therefore "clear" output **114** remains disabled, AND circuit **119** remains disabled and output gate **120** remains disabled. When the operator's finger is removed and A=14, then once again the output of digital comparator **103** on line **106** will be "high", AND circuit **110** will be enabled, line **111** will be enabled clearing delay flip-flop **112**. "Clear" output line **114** will be enabled conditioning AND circuit **119** to be enabled when $Q=\overline{1023}$. When this happens, output gate **120** is once more enabled permitting information to pass through output lines **126** to the buffer.

There are many ways to implement this invention. For example, discrete components could be used throughout rather than the integrated circuits used in the preferred embodiment. There are many, many possible select matrixes available. There are also many different kinds of counters which could be used. This invention is not reliant on any one design choice.

What is claimed is:

1. A touchplate identification system for identifying one of a plurality of touchplates which has been touched by a human being, comprising:

a. a plurality of oscillators, each having a frequency of oscillation controlled by capacitance and resistance connected to the oscillator;

b. a plurality of conductors, each separately connected to the capacitance of an associated oscillator at one end and to an associated touchplate at the other end, the touchplate being adapted to be touched by a human being to change the frequency of oscillation by changing the capacitance;

c. means for sequentially generating an address signal for each of said oscillators;

d. a select matrix operatively connected to said oscillators and said address signal means for selecting one of said oscillators in response to a particular address signal;

e. a counter, for counting the oscillations of said selected oscillator;

f. threshold means for indicating a specified number of oscillations;

g. comparator means, electrically connected to the counter and to the threshold means for comparing the count of oscillations from the counter with the threshold count for a specified time and indicating which is higher;

h. timing means, connected to the comparator means for setting a specified time period; and

i. output means responsive to the comparator means for providing the address signal as an output signal when the oscillation count of the counter is lower than the threshold count.

2. A digital computer input-output system including a display device, having a faceplate, connected to the digital computer, comprising:

a. a plurality of transparent, conductive touchplates attached to the faceplate of the display device;

b. a plurality of oscillators, each having a frequency of oscillation controlled by capacitance and resistance connected to the oscillator;

c. a plurality of conductors, each separately connected to the capacitance of an associated oscillator at one end and to an associated touchplate at the other end, the touchplate being adapted to be touched by a human being to change the frequency of oscillation by changing the capacitance;

d. means for sequentially generating an address signal for each of said oscillators;

e. a select matrix operatively connected to said oscillators and said address signal means for selecting one of said oscillators in response to a particular address signal;

f. a counter, for counting the oscillations of said selected oscillator;

g. threshold means for indicating a specified number of oscillations;

h. comparator means, electrically connected to the counter and to the threshold means for comparing the count of oscillations from the counter with the threshold count for a specified time and indicating which is higher;

i. timing means, connected to the comparator means for setting a specified time period; and

j. output means responsive to the comparator means for providing the address signal as an output signal when the oscillation count of the counter is lower than the threshold count.

3. The system of claim **1**, wherein the touchplates are transparent and conductive.

4. The system of claim **1**, wherein the oscillators are relaxation oscillators each having a capacitor in an RC charge circuit at the input stage and wherein the associated conductor is connected to the input of the oscillator so that any added capacitance is added in parallel to the input capacitor.

5. The system of claim **1**, further including a display device having a faceplate wherein the touchplates are transparent and conductive and are attached to the faceplate of the display device.

6. The system of claim **1** wherein each of the plurality of oscillators has essentially the same free-run frequency.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,696,409 Dated October 3, 1972

Inventor(s) Norman J. Braaten

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

ASSIGNEE: "Linquist & Vennum" should be --Lindquist & Vennum--.

Column 3, Line 61 "paint" should be --point--.
Column 5, Line 17, "FIG 1" should be --FIG 1--.

Column 5, Line 41 "made the" should be --made up--.
Column 6, Line 44 "paint" should be --point--.

Column 8, Line 41 "$B_3 \cdot B_2 \cdot B_1 \quad B_3\ B_2\ B_1$" should be --$B_3 \cdot B_2 \cdot B_1 \quad B_3\ \overline{B}_2\ \overline{B}_1$--.
Column 8, Line 42 "$B_3 \cdot B_2 \cdot B_1 \quad B_3\ B_2\ B_1$" should be --$B_3 \cdot \overline{B}_2 \cdot \overline{B}_1 \quad \overline{B}_3\ \overline{B}_2\ \overline{B}_1$--.
Column 8, Line 43 "$B_3 \cdot B_2\ B_1 \quad B_3 \cdot B_2\ B_1$" should be --$\overline{B}_3 \cdot \overline{B}_2\ B_1 \quad \overline{B}_3 \cdot \overline{B}_2\ \overline{B}_1$--.
Column 8, Line 44 "$B_3 \cdot B_2\ B_1 \quad B_3 \cdot B_2 \cdot B_1$" should be --$\overline{B}_3 \cdot B_2\ B_1 \quad \overline{B}_3 \cdot \overline{B}_2 \cdot \overline{B}_1$--.

Column 8, Line 47 "$B_5 \cdot B_4$" should be --$\overline{B}_5 \cdot \overline{B}_4$--.

Column 8, Line 48 "$B_3 \cdot B_2\ B_1$" should be --$\overline{B}_3 \cdot \overline{B}_2 \cdot \overline{B}_1$--.

Column 9, Line 13 "$(1x10^{-3}/4$" should be --$1x10^{-3}/4$--.
Column 9, Line 28 "$(3x10^{-3}/60$" should be --$3x10^{-3}/60$--.
Column 9, Line 30 "$(1/5)x10^{5}$" should be --$1/5x10^{5}$--.
Column 9, Line 42 "$(1x10^{3}/128)$" should be --$1x10^{3}/128$--.

Column 11, Line 12 "disabled," should be --disabled.--.

Signed and sealed this 8th day of May 1973.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents