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ABNORMAL PACKET PROCESSING SYSTEM

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(57) Claim

1. An abnormal packet processing system in a data processing system including a plurality of processing units connected through an interconnection, characterized in that a transmitting processor is equipped with abnormality detection means for detecting any abnormality when such abnormality occurs in a data packet which is under transmission from said transmitting processor to a receiving processor, and with an abnormality report data addition means for adding abnormality report data containing the occurrence of said abnormality and the classification of said abnormality to said data packet during transmission and sending it to said receiving processor.

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COMPLETE SPECIFICATION

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INVENTION TITLE:

Abnormal packet processing system

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to an abnormal packet processing system. More particularly, it relates to an abnormal packet processing system for use in communications between processing units in a parallel computer system including I/O apparatuses and central processing units.

2. Description of the Related Art

When any abnormality occurs during packet communication between processing units of a data processing system employing an abnormal packet processing system according to the prior art, an instruction processing portion in a transmitting processor reports this abnormality to a receiving processor by allowing a packet, different from the packet under transmission, to contain control data and abnormality data and transmitting it to the receiving processor.

According to the prior art in the system described above, the abnormal data packet has already been received at the point of time when the different packet containing the abnormality report data arrives at the receiving processor, and there is the possibility that processing has been done on the abnormal packet. In other words, unnecessary processing is carried out on the abnormal packet.

SUMMARY OF THE INVENTION

In accordance with the present invention there is provided an abnormal packet processing system in a data processing system including a plurality of processing units connected through an interconnection, characterized in that a transmitting processor is equipped with abnormality detection means for detecting any abnormality when such abnormality occurs in a data packet which is under transmission from said transmitting processor to a receiving processor, and with an abnormality report data addition means for adding abnormality report data containing the occurrence of said abnormality and the classification of said abnormality to said data packet during transmission and sending it

to said receiving processor.

The present invention also provides an abnormal packet processing system in a data processing system including a plurality of processing units connected through an interconnection, characterized in that a transmitting processing unit is equipped with an abnormality detection means for detecting any abnormality when such abnormality occurs in a data packet which is being transmitted from said transmitting processor to a receiving processor, and with packet transfer inhibition means for inhibiting transfer of said data packet from said transmitting processor when said abnormality is detected.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other novel features of the present invention will become more apparent from the following description, by way of example only, of preferred embodiments of the present invention when taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a block diagram useful for explaining the principle of an embodiment of the present invention;

Fig. 2 is a block diagram useful for explaining the principle of another embodiment of the present invention;

Fig. 3 is a block diagram showing the construction of a data processing system applied to an embodiment of the present invention;

Fig. 4 is a block diagram showing one construction of a processing unit according to the embodiment of the present invention;

Fig. 5 is a block diagram showing the construction of a transfer processing unit in one embodiment of the present invention;

Fig. 6 is a flowchart useful for explaining the operation of the transfer processing unit shown in Fig. 5;

Fig. 7 is a diagram showing the construction of a packet according to the embodiment of the present invention;

Fig. 8 is a diagram showing the content displayed on a display according to the embodiment of the present

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invention;

Fig. 9 is a block diagram showing the construction of a transfer processing unit according to another embodiment of the present invention; and

Fig. 10 is a flowchart useful for explaining the operation of the transfer processing unit shown in Fig. 9.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to the description of the preferred embodiments of the present invention, the principle of the invention will be explained with reference to the associated drawings.

Fig. 1 is a block diagram useful for explaining the principle of one embodiment of the present invention. The drawing shows a data processor equipped with a plurality of processing units 1-1, 1-2, ..., 1-n, and these processing units 1-1, 1-2, ..., 1-n are connected with one another through an interconnection 2. According to the present invention, the transmitting processor 1-1 is equipped with an abnormality detection means 3 for detecting any abnormality when such abnormality occurs in a data packet which is being transmitted from the transmitting processor 1-1 to the receiving processor 1-2, and with an abnormality report data addition means 4 for adding abnormality report data to indicate the occurrence of this abnormality and its classification to the data packet during transmission and transmitting the data packet to the receiving processor 1-2.

The receiving processor 1-2 is equipped with an abnormality indication means 5 for holding the received abnormality report data.

Fig. 2 is a block diagram useful for explaining the principle of another embodiment of the present invention.

A plurality of processing units 1-1, 1-2, ..., 1-n are shown connected through an interconnection 2 in Fig. 2 in the same way as in Fig. 1. According to this

embodiment, the transmitting processor 1-1 is equipped with an abnormality detection means 3 for detecting any abnormality when such abnormality occurs in a data packet during transmission from the transmitting processor 1-1 to the receiving processor 1-2, and with a packet transmission inhibition means 6 for inhibiting the transmission of the data packet from the transmitting processor 1-1 when such abnormality is detected.

The transmitting processor 1-1 is equipped with an indication means 7 for indicating that transmission of the data packet is inhibited when the transmission of the data packet is inhibited.

According to the first embodiment of the invention shown in Fig. 1, the abnormality report data is added to the data packet during transmission and then the data packet is transmitted to the receiving processor 1-2. The receiving processor 1-2 displays the abnormality report data thus received. Accordingly, the report of the abnormal data arrives earlier at the reception processing unit and hence, abnormality processing becomes easier.

According to the second embodiment of the invention shown in Fig. 2, the transmission of the data packet from the transmitting processor 1-1 is inhibited when any abnormality occurs in the data packet during transmission from the transmitting processor 1-1 to the receiving processor 1-2. Accordingly, the processing of abnormal data becomes unnecessary in the receiving processor.

Fig. 3 is a block diagram showing a data processing system to which the abnormal packet processing system according to the embodiment of the present invention is applied. In the drawing, a plurality of processing units 3-1 to 3-n are shown connected through a network 32. These processing units are, for example, vector operation circuits or scalar operations circuits of a parallel computer system, and constitute a multi-processor.

The network 32 may be either a switching network having a switching function, or a bus.

A packet is transmitted from one of the processing units to others. When any abnormality occurs in this packet during transmission, this abnormality is reported to the processing unit on the receiving side, or the transmission of the packet itself is inhibited by the transmitting processor, by the means of the embodiments of the present invention which will be described next.

Fig. 4 is a block diagram showing one construction of the processing unit according to the embodiment of the present invention. In the drawing, the processing unit 3-1 includes a main storage 40 for storing instructions (that is, a program) and data, an instruction processing unit 41 for retrieving the instructions from the main storage 40 and executing them, a transfer processing unit 42 to transfer a packet between the main storage 40 and a network 32, and an abnormality detection circuit 43 for detecting the occurrence of any abnormality when such abnormality occurs in any of the main storage 40, the instruction processing unit 41 and the transfer processing unit 42 during transmission of the packet.

Fig. 5 is a block diagram showing the construction of the transfer processing unit 42 in the embodiment of the present invention. In the drawing, the transfer processing unit 42 includes a main storage access control unit 50 for controlling access to the main storage 40, a data buffer 51 for storing the data read out from the main storage 40 and accumulating the data to be stored in the main storage 40 under the control of the main storage access control unit 50, a network transfer control unit 52, a network interface 53 and an abnormality indication device 54 for indicating that an abnormality exists in the received packet.

Fig. 6 is a flowchart useful for explaining the operation of the transfer processing unit 42 shown in

Fig. 5.

Fig. 7 is a diagram showing the construction of the packet according to the embodiment of the present invention. As shown in the drawing, the packet comprises address data for designating a receiving processor, other control data and abnormality data which is added in accordance with the present invention. The control data includes memory access attributes in the transmitting processor, data relating to designation of the processing in the receiving processor, and so forth.

Fig. 8 shows the content of the abnormality data held by the indication device inside the processing unit on the receiving side or the transmitting side according to the present invention. As shown in the drawing, the indication device indicates that the transmission data is designated incorrectly, indicates that a multiple-bit error occurred in the transmission data, or indicates that hardware errors occurred inside the transfer processing unit.

The operation of the embodiment of the present invention will be explained with reference to Figs. 3 to 6.

The main storage access control unit 50 accesses the main storage 40 under instruction from the network transfer control unit 52, and controls the transfer of data between the main storage 40 and the data buffer 51. The data buffer 51 temporarily stores the data when data transfer is carried out between the main storage 40 and the network 32, and also temporarily stores the data when a data write request is made by the data transfer unit 42 and by the main storage access control unit 50 to the main storage 40.

The network transfer control unit 52 inside the transfer processing unit 42 is activated by the control data in the transfer packet generated by the instruction processing unit 41, and issues a main storage access request to the main storage access control unit 50 so as

to read out the control data from the transfer packet. The data is read out from the main storage 40 in response to this access request, and is stored in the buffer 51 (Step 61 in Fig. 6). The network transfer control unit 52 controls the network interface 53, and sends the control data from the data buffer 51 to the network 32 (Step 62 in Fig. 6). When any abnormality occurs in the main storage 40, the instruction processing unit 41 or the transfer processing unit 42 during the transfer of the control data from the transfer processing unit 42 (in the case of Y at Step 63 in Fig. 6), the abnormality detection circuit 43 detects this abnormality and reports it to the network transfer control unit 52. Upon receiving this report, the transmission abnormality data addition device 55 inside the network control unit 52 adds the abnormality data to the data packet during the transmission (Step 64 in Fig. 6).

When no abnormality is detected, the data from the data buffer 51 is delivered to the network 32 (Step 65 in Fig. 6).

Upon receiving the packet having the abnormality data added thereto, the processing unit on the receiving side allows the abnormality indication device 54 to hold details of the abnormality. The abnormality indication device 54 is a register to which reference can be made from the instruction processing unit. This abnormality can also be held in the abnormality indication device 54 on the transmitting side.

Fig. 9 is a block diagram showing the construction of the transfer processing unit according to another embodiment of the present invention. The same reference numerals will be used in this drawing to represent the same circuit elements as in Fig. 5 and a suffix a will be added to the reference numeral to represent the circuit element which is analogous to the one shown in Fig. 5.

In Fig. 9, delivery of the normal data packet is carried out in the same way as in Fig. 5. When any

abnormality occurs in the main storage 40, the instruction processing unit 41 or the transfer processing unit 42a during the transfer of the data packet, the abnormality detection circuit 43 detects this abnormality and reports it to the network transfer control unit 52a. Upon receiving this report, the abnormality packet transfer inhibition device 55a inside the network transfer control unit 52a inhibits the transmission of the abnormal data packet.

The abnormality indication device 54 inside the processing unit on the transmission side indicates the inhibition of the transmission of the packet as well as the content of this abnormality.

Fig. 10 is a flowchart useful for explaining the operation of the transfer processing unit 42a shown in Fig. 9. In this drawing, the control data of the packet is first read out from the main storage 40 at Step 101 in the same way as in Fig. 6, and is stored in the data buffer 51. When the abnormality report from the abnormality detection circuit 43 arrives during the storage of this control data (in the case of Y at Step 102), the abnormality data is sent to the abnormality indication device 54 at Step 103, the control data in the data buffer 51 is made invalid at Step 104, and the packet transfer is inhibited at Step 105.

When the abnormality report does not exist at Step 102, the control data is read out from the data buffer 51 at Step 106 and is sent to the network 32, and the data is then read out from the data buffer 51 at Step 107 and is sent to the network 32. After the data representing that no abnormality exists is added to the packet at Step 108, the packet transfer is completed.

Examples of abnormality in Figs. 5 and 9 are multiple-bit errors in the main storage 40 and hardware errors inside the transfer processing unit.

Although the foregoing embodiments illustrate the case where the transmission abnormality data addition

device and the abnormal packet transfer inhibition device are constituted by the hardware, they may also be accomplished by software.

As can be clearly understood from the explanation given above, one of the embodiments of the present invention adds the abnormality report data to the data packet when any abnormality exists on the transmission side during the data transfer between the processing units of the data processing system. For this reason, transfer of another packet for notifying this abnormality to the reception processing unit becomes unnecessary, and the abnormality report arrives up in the receiving processing unit, so that the abnormality processing becomes more simple. According to another embodiment of the present invention, the transmission of the data packet itself is inhibited when any abnormality exists on the transmission side. Accordingly, processing to cope with abnormality becomes unnecessary at the receiving processing unit.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated integer or group of integers but not the exclusion of any other integer or group of integers.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. An abnormal packet processing system in a data processing system including a plurality of processing units connected through an interconnection, characterized in that a transmitting processor is equipped with abnormality detection means for detecting any abnormality when such abnormality occurs in a data packet which is under transmission from said transmitting processor to a receiving processor, and with an abnormality report data addition means for adding abnormality report data containing the occurrence of said abnormality and the classification of said abnormality to said data packet during transmission and sending it to said receiving processor.

2. An abnormal packet processing system according to claim 1, wherein said receiving processor is equipped with abnormality indication means for displaying said abnormality report data.

3. An abnormal packet processing system according to claim 2, wherein said processing unit includes a main storage for storing instructions and data, an instruction processing unit for retrieving said instructions from said main storage and executing them, a transfer processing unit to transfer said packet between said main storage and a network, and an abnormality detection circuit for detecting abnormality when any abnormality occurs in said main storage, said instruction processing unit and said transfer processing unit during transfer of said packet.

4. An abnormal packet processing system according to claim 3, wherein said transfer processing unit includes a main storage access control unit for controlling an access to said main storage, a data buffer for storing data read out from said main storage and accumulating data to be stored in said main storage under control of said main storage access control unit, network transfer control unit, a network interface, and a receiving abnormality indication device for displaying the occurrence of any abnormality in said received packet.

5. An abnormal packet processing system according to claim 4, wherein said network

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transfer control unit includes a transmitting abnormality data addition device for adding abnormality data to said data packet being transmitted by the report from said abnormality detection circuit.

6. An abnormal packet processing system in a data processing system including a plurality of processing units connected through an interconnection, characterized in that a transmitting processing unit is equipped with an abnormality detection means for detecting any abnormality when such abnormality occurs in a data packet which is being transmitted from said transmitting processor to a receiving processor, and with packet transfer inhibition means for inhibiting transfer of said data packet from said transmitting processor when said abnormality is detected.

7. An abnormal packet processing system according to claim 6, wherein said transmitting processor includes an indications means for effecting a display to the effect that the transfer of said data packet is inhibited when the transmission of said data packet is inhibited.

8. An abnormal packet processing system according to claim 7, wherein said processing unit includes a main storage for storing instructions and data, an instruction processing unit for retrieving said instructions from said main storage and executing them, a transfer processing unit to transfer said packet between said main storage and said network, and an abnormality detection circuit for detecting abnormality when any abnormality occurs in said main storage, said instruction processing unit and said transfer processing unit during the transfer of said packet.

9. An abnormal packet processing system according to claim 8, wherein said transfer processing unit includes a main storage access control unit for controlling an access to said main storage, a data buffer for storing data read out from said main storage and accumulating data to be stored in said main storage under control of said main storage control unit, a network transfer control unit, a network interface and an abnormality display device for effecting display to the effect that any abnormality occurred for said packet received.

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10. An abnormal packet processing system according to claim 9, wherein said network transfer control unit includes an abnormal packet transfer inhibition device for inhibiting the transmission of an abnormal data packet during transmission by a report from said abnormality detection circuit.

11. An abnormal packet processing system substantially as hereinbefore described with reference to the accompanying drawings.

DATED this 8th day of February, 1994

FUJITSU LIMITED
By its Patent Attorneys
DAVIES COLLISON CAVE

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ABNORMAL PACKET PROCESSING SYSTEM

ABSTRACT OF THE DISCLOSURE

This invention relates to an abnormal packet processing system, and is directed to minimize processing of an abnormal packet during communication between a plurality of processing units by a receiving processor. In a data processing system including a plurality of processing units (1-1, 1-2, ..., 1-n) connected through an interconnection (2), a transmitting processor (1-1) includes means (3) for detecting abnormality of a data packet during transmission to a receiving processor (1-2) and means (4, 7) for adding abnormality report data to the data packet being transmitted and sending it to the receiving processor (1-2), or inhibiting transmission of the abnormal packet.

Fig.1

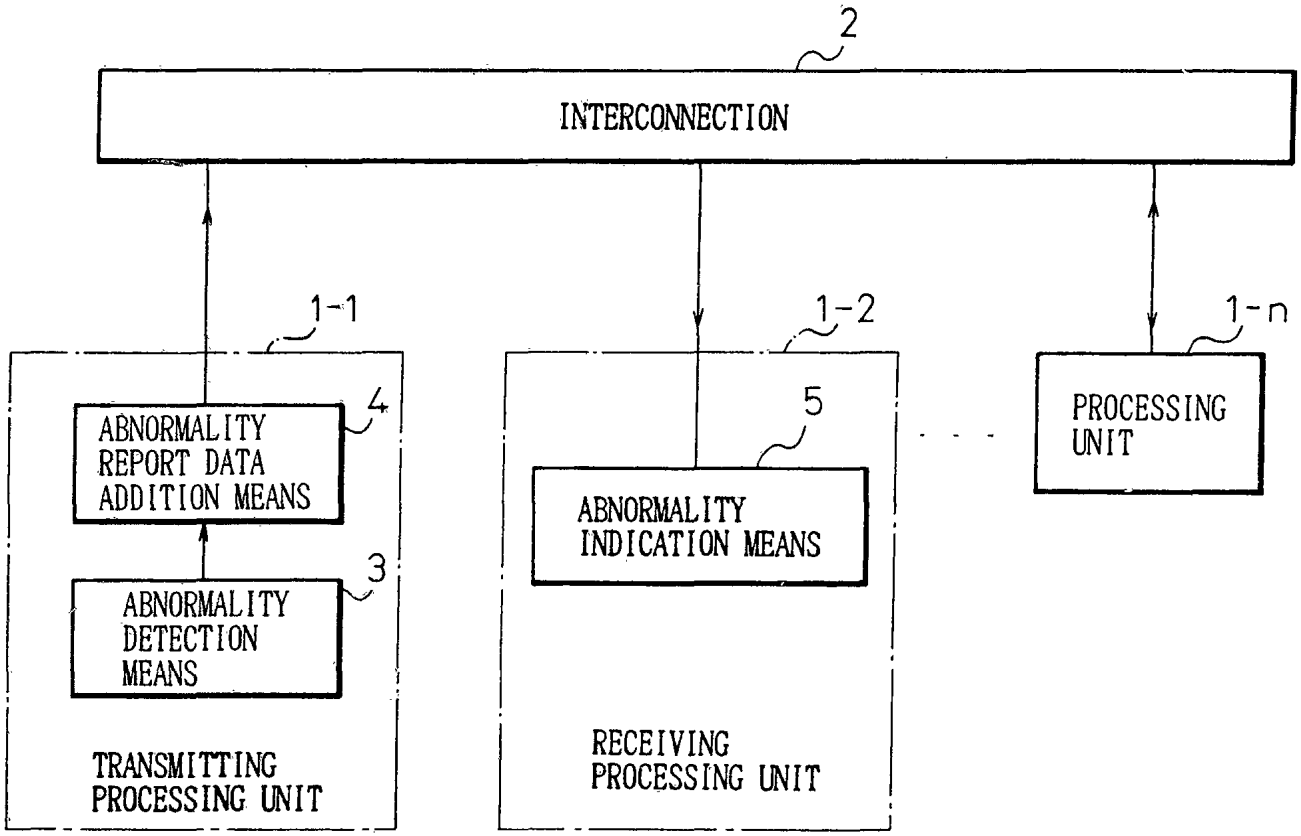

2
INTERCONNECTION
1-1
1-2
1-n
4
ABNORMALITY REPORT DATA ADDITION MEANS
3
ABNORMALITY DETECTION MEANS
TRANSMITTING PROCESSING UNIT
5
ABNORMALITY INDICATION MEANS
RECEIVING PROCESSING UNIT
PROCESSING UNIT

Fig.2

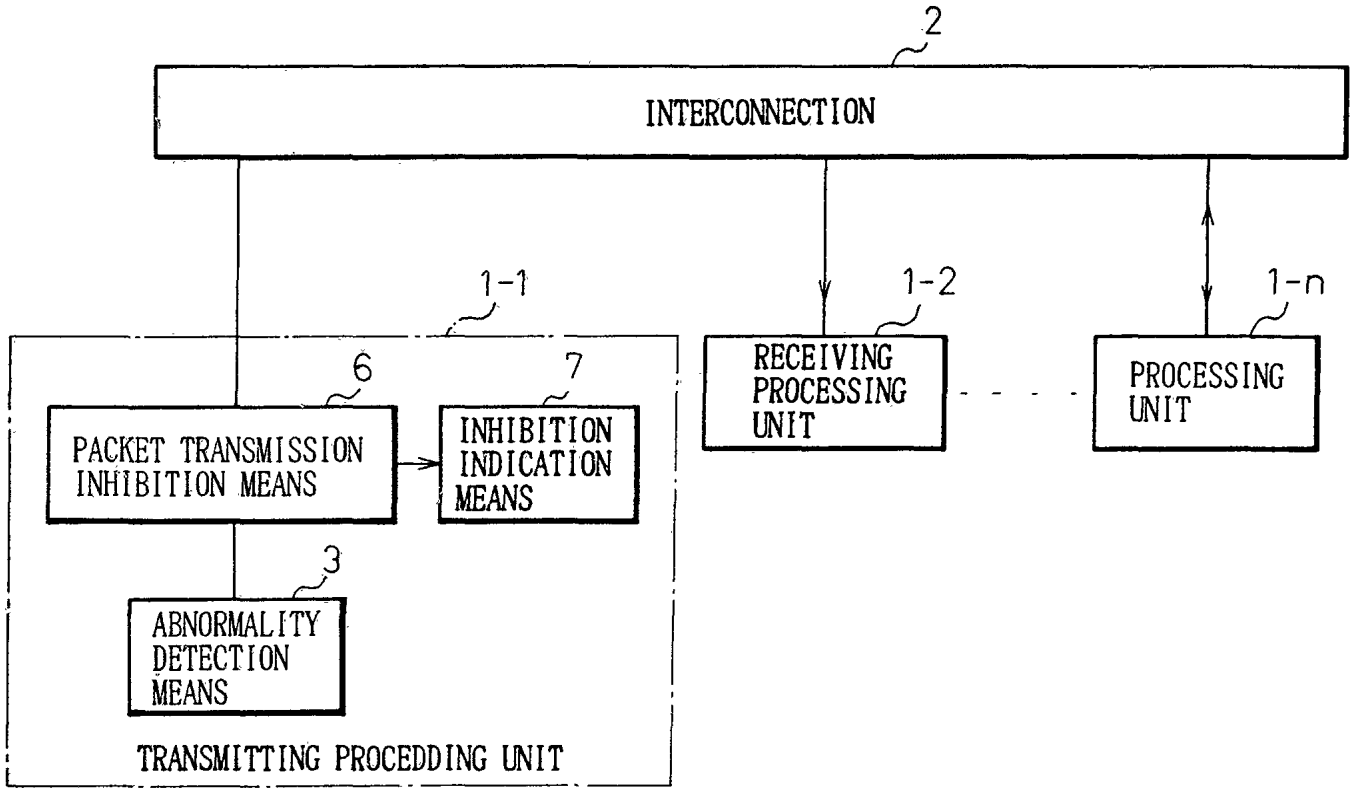

2
INTERCONNECTION
1-1
1-2
1-n
6
7
PACKET TRANSMISSION INHIBITION MEANS
INHIBITION INDICATION MEANS
RECEIVING PROCESSING UNIT
PROCESSING UNIT
3
ABNORMALITY DETECTION MEANS
TRANSMITTING PROCEDDING UNIT

Fig.3

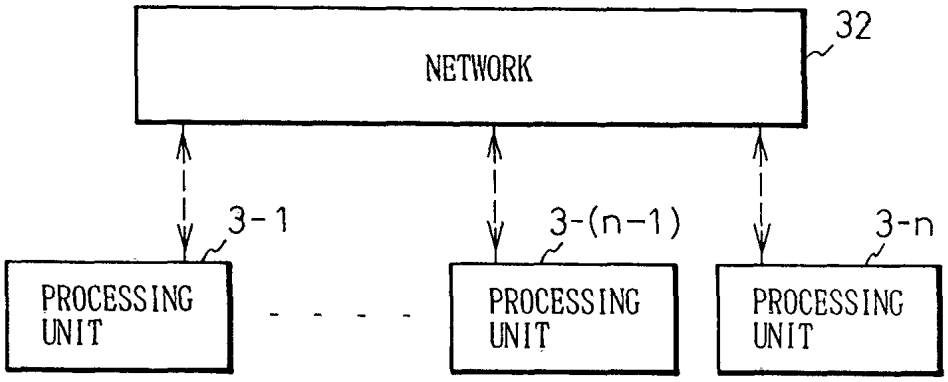

NETWORK
32
3-1
3-(n-1)
3-n
PROCESSING UNIT
PROCESSING UNIT
PROCESSING UNIT

Fig.4

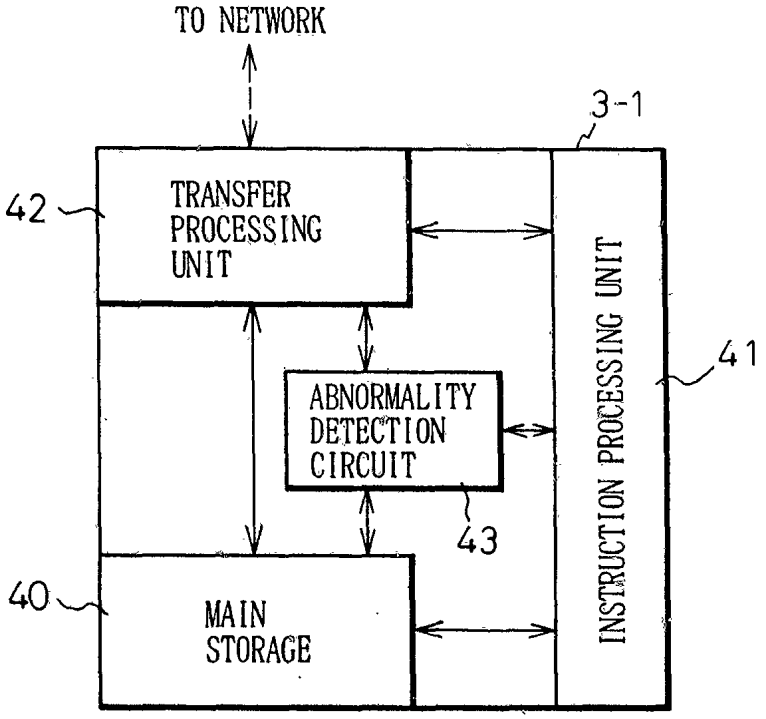

TO NETWORK
3-1
42
TRANSFER PROCESSING UNIT
ABNORMALITY DETECTION CIRCUIT
43
41
INSTRUCTION PROCESSING UNIT
40
MAIN STORAGE

Fig.5

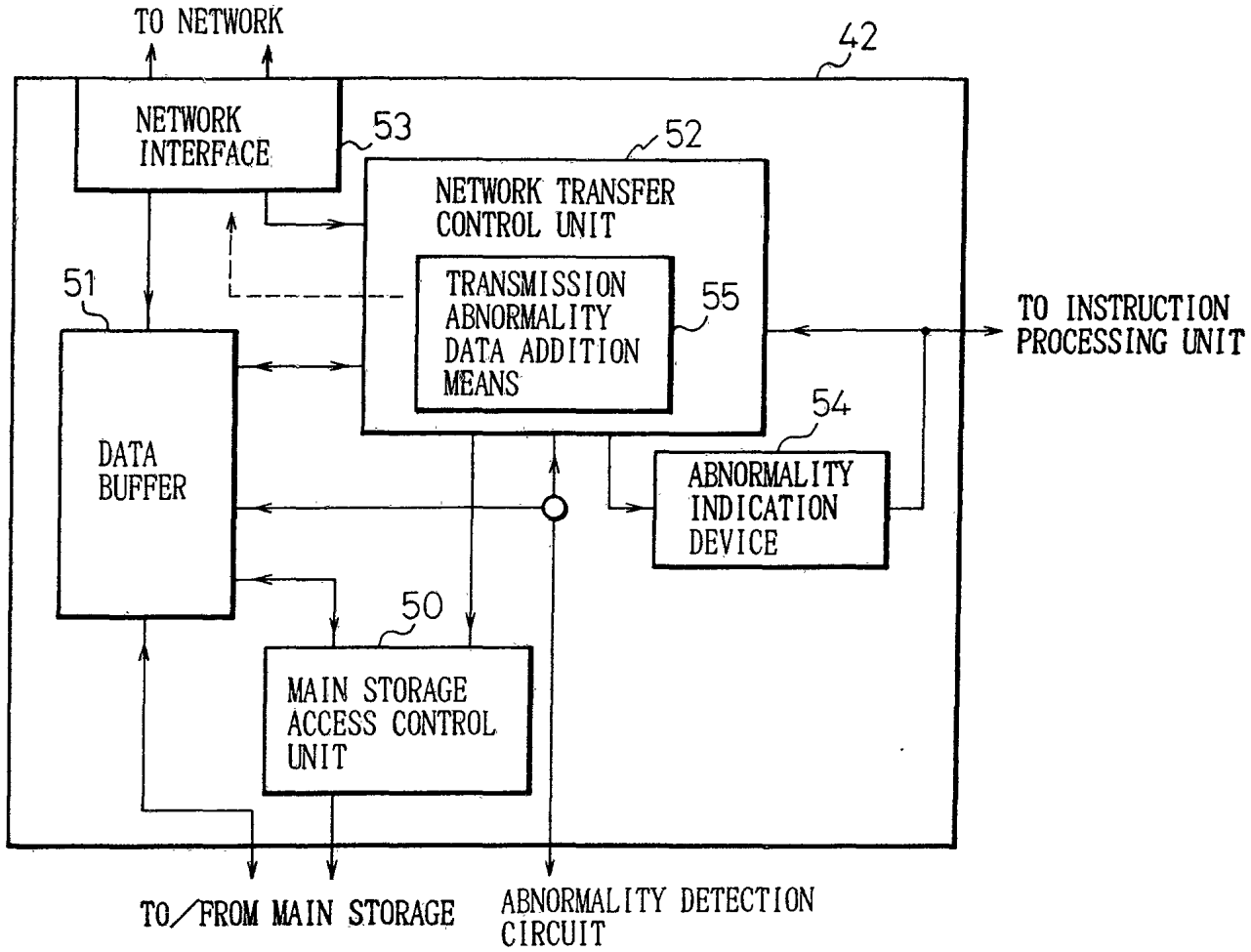

TO NETWORK
42
NETWORK INTERFACE
53
52
NETWORK TRANSFER CONTROL UNIT
TRANSMISSION ABNORMALITY DATA ADDITION MEANS
55
51
TO INSTRUCTION PROCESSING UNIT
DATA BUFFER
54
ABNORMALITY INDICATION DEVICE
50
MAIN STORAGE ACCESS CONTROL UNIT
TO/FROM MAIN STORAGE
ABNORMALITY DETECTION CIRCUIT

Fig.6

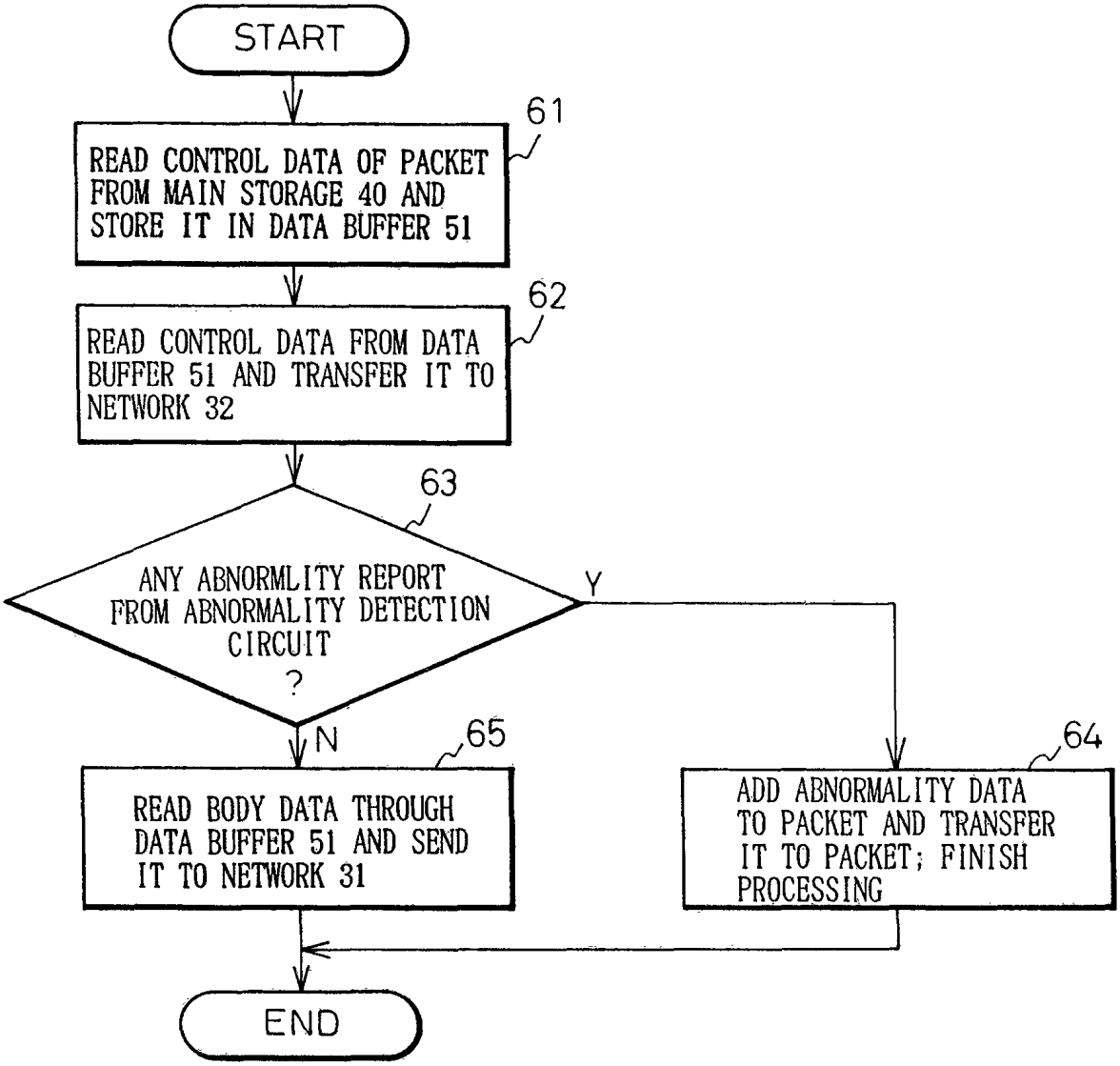

START
61
READ CONTROL DATA OF PACKET FROM MAIN STORAGE 40 AND STORE IT IN DATA BUFFER 51
62
READ CONTROL DATA FROM DATA BUFFER 51 AND TRANSFER IT TO NETWORK 32
63
ANY ABNORMLITY REPORT FROM ABNORMALITY DETECTION CIRCUIT ?
Y
N
65
READ BODY DATA THROUGH DATA BUFFER 51 AND SEND IT TO NETWORK 31
64
ADD ABNORMALITY DATA TO PACKET AND TRANSFER IT TO PACKET; FINISH PROCESSING
END

Fig.7

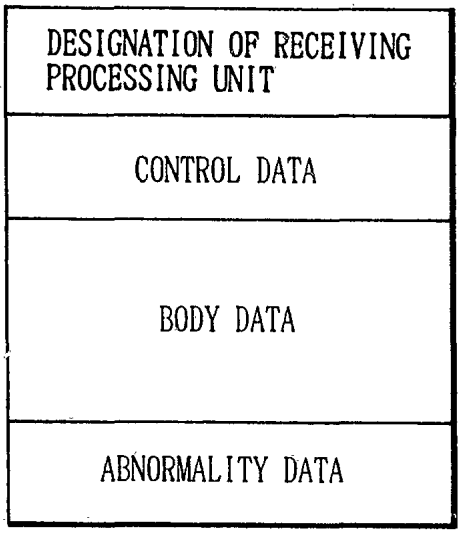


Fig.8

TRANSMISSION DATA DESIGNATION ERROR	MULTIPLE-BIT ERROR IN TRANSMISSION DATA	MALFUNCTION IN TRANSFER PROCESSING UNIT (MARDWARE ERROR)

Fig.9

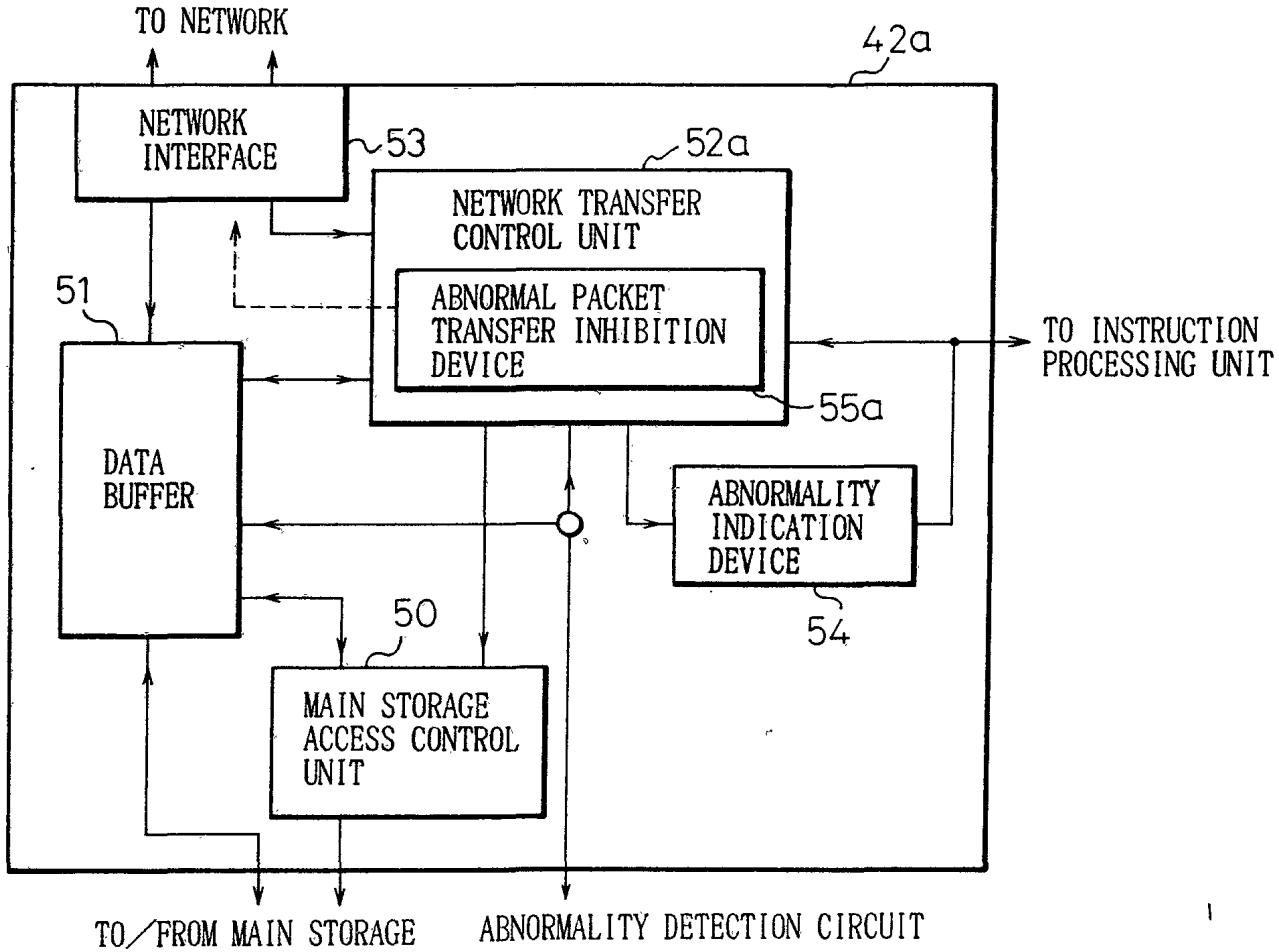
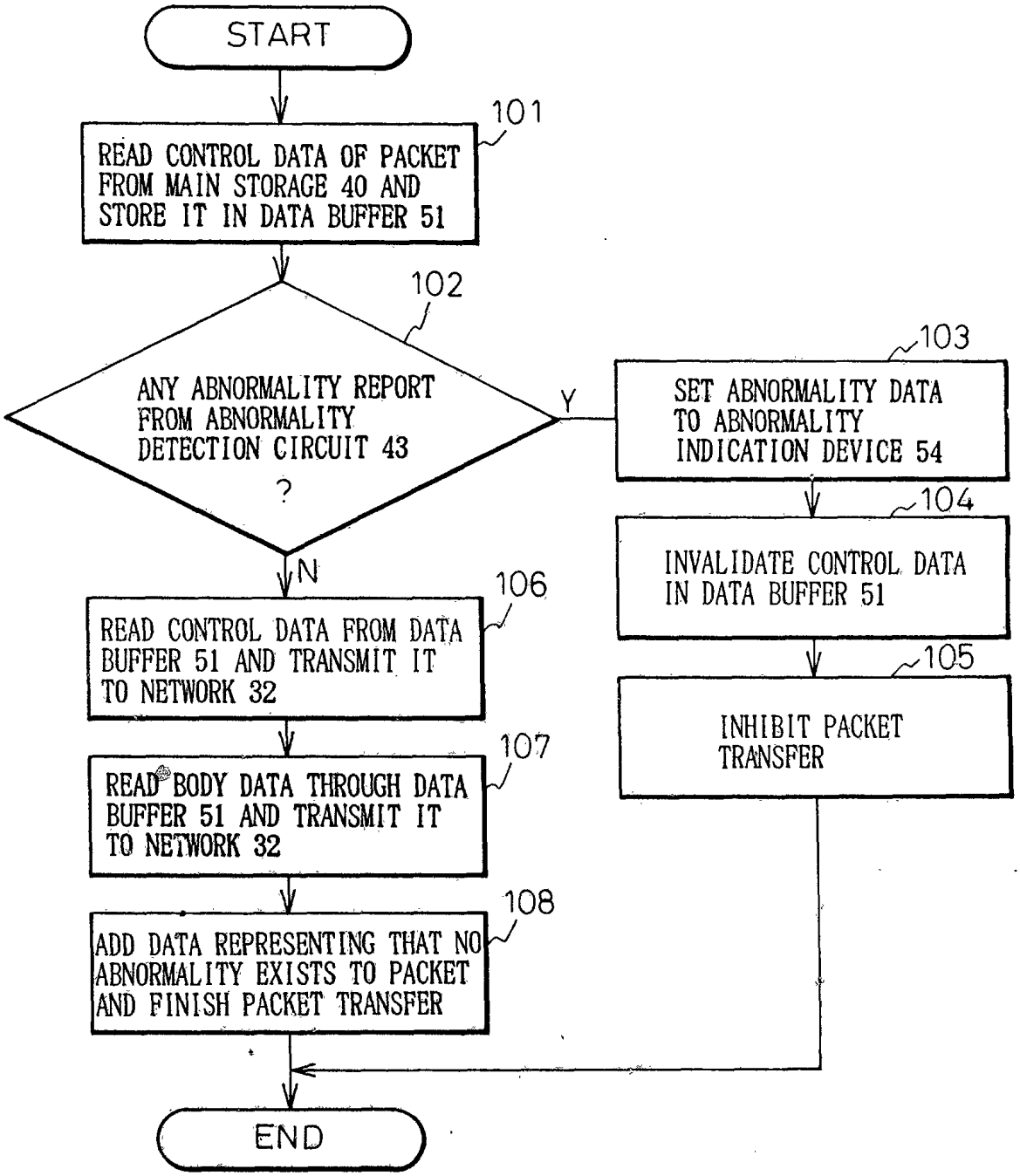

TO NETWORK
42a
NETWORK INTERFACE
53
52a
NETWORK TRANSFER CONTROL UNIT
ABNORMAL PACKET TRANSFER INHIBITION DEVICE
55a
51
DATA BUFFER
TO INSTRUCTION PROCESSING UNIT
ABNORMALITY INDICATION DEVICE
54
50
MAIN STORAGE ACCESS CONTROL UNIT
TO/FROM MAIN STORAGE
ABNORMALITY DETECTION CIRCUIT

Fig.10


START
101
READ CONTROL DATA OF PACKET FROM MAIN STORAGE 40 AND STORE IT IN DATA BUFFER 51
102
ANY ABNORMALITY REPORT FROM ABNORMALITY DETECTION CIRCUIT 43 ?
Y
103
SET ABNORMALITY DATA TO ABNORMALITY INDICATION DEVICE 54
104
INVALIDATE CONTROL DATA IN DATA BUFFER 51
105
INHIBIT PACKET TRANSFER
N
106
READ CONTROL DATA FROM DATA BUFFER 51 AND TRANSMIT IT TO NETWORK 32
107
READ BODY DATA THROUGH DATA BUFFER 51 AND TRANSMIT IT TO NETWORK 32
108
ADD DATA REPRESENTING THAT NO ABNORMALITY EXISTS TO PACKET AND FINISH PACKET TRANSFER
END