(54) Title: AUTOMATIC FAULT RECOVERY IN A PACKET NETWORK

(57) Abstract

An arrangement is disclosed for recovering from faults in transmission equipment or facilities forming so-called virtual circuits for transmitting packets in a network. Faults are detected in transmission paths associated with a network node and a fault indication is generated for any virtual circuits passing through the node that are affected by the fault. The fault indications are then transmitted on corresponding ones of the affected virtual circuits or on other designated virtual circuits. If any of the affected virtual circuits are determinated in the node, no fault indications are generated for them and they are switched to alternate virtual circuits. Otherwise, the fault indications are transmitted on corresponding virtual circuits or on other designated virtual circuits over facilities connected to the node to other unknown nodes. A node receiving a fault indication message determines whether the corresponding virtual circuit is terminated at the node, has one or more alternate virtual links in the node, or passes through it to some other unknown node. If an affected virtual circuit is terminated in the node, or has one or more alternate virtual links in the node, it is switched to an alternate virtual link. If the affected virtual circuit is not terminated in the node, and has no alternate virtual link present, the corresponding fault indication message is passed, i.e., switched, through it on that virtual circuit over a facility to some other unknown node.
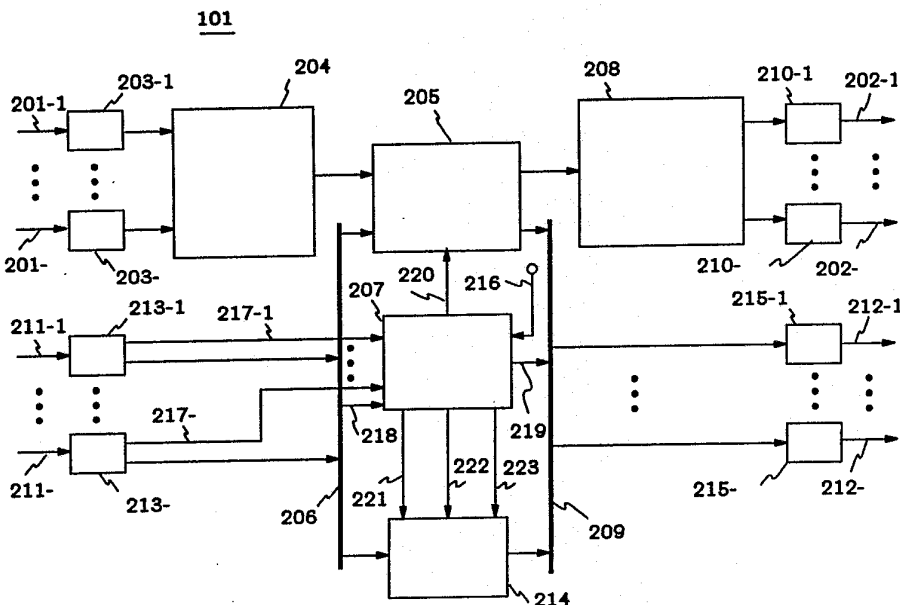
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AUTOMATIC FAULT RECOVERY IN A PACKET NETWORK

Technical Field

      This invention relates to packet transmission systems and/or networks and, more particularly, to automatic recovery from faults in the system and/or

5   network.

Background of the Invention

      Prior packet transmission and switching systems and/or networks included fault recovery arrangements. One such prior arrangement required a so-called centralized network management function to analyze reported faults and to

10 reconfigure the network as required. Consequently, the centralized network management function required knowledge of the entire network and connectivity to each node in the network. Such arrangements are slow to respond to faults and are also susceptible to faults in the network and in the management function itself.

      In another prior fault recovery arrangement, each node in the network

15 required knowledge of the network configuration and knowledge of faults occurring in the network. In such an arrangement, each node must store additional network configuration data other than that needed for transmission of packets in the particular node. Any change in the network configuration may require a change in the information being stored in the node. Both the storing and updating of the

20 configuration information in the node is cumbersome and expensive to implement.

      More recently, recovery from faults in a packet network has been realized by detecting faults in the transmission path associated with a network node and transmitting a fault indication message blindly for each virtual link that is affected by the fault.

25   Although these arrangements function satisfactorily in many applications, they may not function satisfactorily in others. Indeed, a problem with such arrangements occurs in complex networks that contain a large diversity of paths and/or uni-directional routing. For example, the previous arrangements may not properly respond to multiple faults in the network since the entire virtual circuit

30 affected by the fault is switched to an alternate path even though only a portion or portions of the circuit are actually faulted. Furthermore, if the fault affects a uni-directional virtual circuit, the fault indication messages in the previous arrangements may not reach the originating node.

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Summary of the Invention

These and other problems and limitations of prior automatic packet fault recover arrangements are overcome, in accordance with an aspect of the invention, by detecting faults in transmission paths associated with a network node and, then,
5 generating a fault indication message for virtual circuits passing, (i.e., switched) through the node representative that the virtual circuit has been affected by a detected fault. The fault indication message includes the identity of at least one virtual circuit which is affected by the fault and is transmitted in-band on the affected virtual circuit or on another specified affected virtual circuit to another
10 unknown node. If the affected virtual circuit is terminated in the node or if one or more alternate virtual circuits are present in the node for the affected virtual circuit no such fault indication message is generated for it and it is switched to an at least one alternate virtual circuit in the node. Any generated fault indication message is sent from the node that is affected by the detected fault toward an unknown node. If
15 a node that receives such a fault indication message has one or more alternate virtual links for any virtual circuit identified by the fault indication message, that node switches the at least one virtual circuit identified in the fault indication message to one of the alternate virtual links. If the node receiving the fault indication message does not have any alternate virtual links assigned to the affected virtual circuit
20 identified in the fault indication message, the fault indication is passed, i.e., switched through the node, on the affected virtual circuit or some other designated affected virtual circuit to some other unknown node.

In one embodiment of the invention, fault indication messages are generated for each affected virtual circuit and transmitted from the node affected by
25 the detected fault in a direction away from the fault and in a direction towards the fault.

In another embodiment of the invention, a node receiving the fault indication message(s) may have more than one alternate virtual link assigned to the virtual circuit(s) identified in the fault indication message(s). Such a node switches
30 the virtual circuit identified in the fault indication message to a selected one of the assigned alternate virtual links. The selection of the alternate virtual link may be realized by employing any one of a number of selection techniques, for example, by using a priority scheme or by considering the available capacity on each of the routes taken by the alternate virtual links. In one embodiment, the alternate virtual link on
35 the route with the most available capacity (i.e., the least congestion) is chosen.

Brief Description of the Drawings

In the drawings:

FIG. 1 shows, in simplified form, a packet transmission system and/or network including an embodiment of the invention;

5   FIG. 2 depicts, in simplified block diagram form, details of a packet node used in the system and/or network of FIG. 1;

FIG. 3 shows, in simplified block diagram form, details of the fault recovery unit employed in the node of FIG. 2;

FIG. 4 is a flow chart of a sequence of operations effected by the fault

10   indication message receiver of FIG. 3;

FIGs. 5 , 6 and 7 when connected as shown, form a flow chart illustrating a sequence of operations effected by the fault indication message generator of FIG. 3;

FIG. 8 is a flow chart illustrating a sequence of operations effected by

15   the access circuit mapping unit of FIG. 2;

FIG. 9 is a flow chart showing a sequence of operations effected by the frame mapping unit of FIG. 2;

FIG. 10 is a graphic representation of a LAPD frame; and

FIGs. 11 and 12 are graphic illustrations of fault indication messages

20   employed in this embodiment of the invention.

Detailed Description

FIG. 1 shows, in simplified form, details of transmission system and/or network 100 employing an embodiment of the invention. Accordingly, shown are a plurality of system and/or network nodes, namely, nodes 101-1 through 101-N.

25   Hereinafter all references will be made to network nodes, etc. Also shown are a number of network facilities (NFs) connecting nodes 101 and access facilities (AFs) connected to particular ones of nodes 101. Network facilities carry virtual links (VLs) between nodes inside the network. It is noted that some virtual links are designated alternate virtual lines (AVLs) and are shown in dot-dashed outline.

30   Access facilities carry access circuits from the network to outside of the network and, conversely, from outside of the network to the network. In this example, some of nodes 101 are identical and others are not depending on their particular function in the network. That is, some of nodes 101 have access facilities connected to them while others do not. It will also be apparent that particular ones of nodes 101 may

35   have a plurality of access facilities. Similarly, particular ones of nodes 101 may interface with a plurality of network facilities connecting them to one or more other

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nodes. In this specific example, it is assumed that the network facilities are either
T1, CEPT1, or T3 transmission facilities using non-channelized ISDN packet mode
framing formats, e.g., LAPD, protocols, and procedures. In some different
applications, other facilities may be employed, for example, local area networks,
5   wide area networks, RS232 and the like. Each network facility carries a set of
virtual links or alternate virtual links. The access facilities are assumed to be T1 or
ISDN basic rate interface (BRI) facilities. Each access facility carries one or more
access circuits. In a network node, an access circuit may be connected to a virtual
link or a virtual link may be connected to another virtual link. A virtual circuit for a
10   call comprises a local access circuit, one or more virtual links connected through one
or more nodes and at least one remote access circuit. It will be apparent to those
skilled in the art that other transmission facilities and other packet protocols may
equally be employed in practicing the invention.

For the purposes of illustrating the fault recovery operation of network
15   100, in accordance with an aspect of the invention, it is assumed that a primary
virtual circuit, shown in dashed outline, is provisioned between an access circuit
carried on the access facility (AF) shown connected to originating node 101-1 and an
access circuit carried on the access facility (AF) shown connected to destination
node 101-N. The primary virtual circuit is carried from originating node 101-1 to
20   destination node 101-N through a primary path including nodes 101-2, 101-3 and
101-4 and virtual links (VLs) carried on the associated network facilities (NFs).
Additionally, two alternate virtual links (AVLs), shown in dot-dashed outline, are
provisioned from node 101-2 to node 101-5 and destination node 101-N, and one
alternate virtual link is provisioned from originating node 101-1 to node 101-5.
25   Although only one primary virtual circuit and three alternate virtual links are shown,
there may be a plurality of such virtual circuits and links in the network. Moreover,
it is important to note that none of nodes 101 in network 100 has knowledge of any
other node in the network. Each of nodes 101, only knows its own mappings of
access circuits to virtual links and virtual links to virtual links. These mappings
30   include access circuits to alternate virtual links, virtual links to alternate virtual links
and alternate virtual links to alternate virtual links. It is further noted that a fault can
occur in the node equipment itself or in one or more network facilities connecting
nodes. In this example, it is assumed that a fault occurs somewhere in the
transmission path between nodes 101-3 and 101-4.

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When the fault occurs, the primary virtual circuit is disrupted along the primary path between originating node 101-1 and destination node 101-N. Upon detecting the fault, each of nodes 101-3 and 101-4 determines that a particular virtual circuit, among others, is affected by the fault. Node 101-3 generates a fault

5   indication message and supplies it as an output on the affected virtual circuit to node 101-2. Node 101-3 also generates a fault indication message and supplies it as an output on the affected virtual circuit toward node 101-4. If the fault is uni-directional, this fault indication message may reach node 101-4. In this example, the fault indication message is a LAPD frame (FIGs. 11 and 12) using a XID format

10   (See CCITT Recommendation Q.921, pages 42-48, and a Committee T1 Contribution, "Explicit Congestion avoidance indication as part of Link Layer management", T1S1.1-89/339, T1S1.2-89/240, July 17-19, 1989, pages 1-14 for an explanation of the LAPD frame and XID format). Similarly, node 101-4 generates a fault indication message and supplies it as an output on the affected virtual circuit to

15   node 101-N. Also, node 101-4 supplies as an output a fault indication message on the affected virtual circuit to node 101-3. Again, it is noted that neither node 101-3 nor node 101-4 has knowledge of other nodes in the path or of the end points of the affected virtual circuit. Nodes 101-3 and 101-4 include information relating only to the virtual link to virtual link mapping of the virtual circuit. Upon receiving the fault

20   indication message, node 101-2 determines whether one or more alternate virtual links are present at this node for the affected virtual circuit. Since node 101-2 includes two alternate virtual links for the affected virtual circuit, node 101-2 switches the virtual link between node 101-2 and node 101-3 to one of the two alternate virtual links. The choice of which alternate virtual link to use may be made

25   by determining which alternate virtual link is on the least congested network facility, where congestion is measured in a manner know to the art (see for example, United States Patent 4,703,477, issued October 27, 1987 for a congestion control arrangement). Alternatively, a priority scheme may be used to select the alternate virtual link. To this end, a pre-provisioned priority exists for each alternate virtual

30   link and an alternate virtual link not affected by any fault with the highest priority is chosen. It will be apparent to those skilled in the art that other techniques for choosing an alternative virtual link may also be used. Once an alternate virtual link is chosen, the virtual circuit is switched to use that alternate virtual link instead of the affected virtual link. Thus, it is seen that, in accordance with an aspect of the

35   invention, the network has recovered from the fault on the affected virtual circuit. Furthermore, it can be seen that, in accordance with an aspect of the invention, this

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recovery is accomplished without any node having information relating to the
network topology other than for the network facilities that terminate at individual
ones of nodes 101. Moreover, switching from the affected virtual links to the
alternate virtual links is accomplished at an intermediate node, not at the endpoint of
5   the virtual circuit.

FIG. 2 shows, in simplified block diagram form, the general architecture
of nodes 101. It is to be noted that the configuration of specific ones of nodes 101
may include an interface to at least one network facility and may not include any
access facilities. However, a typical one of nodes 101 includes one or more receive
10   access facilities 201-1 through 201-M, and a corresponding number of transmit
access facilities 202-1 through 202-M. It is noted that pairs of receive access
facilities 201-1 through 201-M and transmit access facilities 202-1 through 202-M,
respectively, form the access facilities (AFs) shown in FIG. 1. As indicated above,
the signals received and transmitted on the access links may take any desired form.
15   In this example, it is assumed that the access facility signals are non-packetized T-
carrier in the known DS1 format. Thus, in this example, an access facility carries up
to 24 access circuits. Signals obtained from receive access facilities 201-1 through
201-M are supplied via digital line interface (DLI) units 203-1 through 203-M,
respectively, to packetizer 204. Each of digital line interfaces 203 are of a type well
20   known in the art for interfacing the DS1 signals being supplied via the receive access
facilities 201. Packetizer 204 forms incoming voice or data information into a
packet format. Such packetizers are known in the art. In this example, the LAPD
format is used for packetization. The LAPD layer 2 data unit is known as a frame,
and the layer 3 data unit is known as a packet. Thus, throughout this example, the
25   term "frame" is used instead of "packet". The LAPD frames (FIG. 10) generated in
packetizer 204 are supplied to access circuit mapping unit 205. Access circuit
mapping unit 205 also obtains received frames from receive frame bus 206.
Additionally, access circuit remap control signals are supplied to access circuit
mapping unit 205 via circuit path 220 from fault recovery unit 207. The access
30   circuit remap control signals control remapping of access circuits carried on receive
access facilities 201 to virtual links carried on transmit network facilities 212, and
the remapping of virtual links carried on receive network facilities 211 to the
original access circuits carried on transmit access facilities 202. Access circuit
mapping unit 205 yields so-called terminated frames which are supplied to
35   depacketizer 208, and so-called transmit frames which are supplied to transmit frame
bus 209. Operation of access circuit mapping unit 205 is described below in

conjunction with FIG. 8. Depacketizer 208 reconstructs the voice or data digital signals from the terminated LAPD frames. These signals are supplied via digital line interface (DLI) units 210-1 through 210-M to transmit access facilities 202-1 through 202-M, respectively. Again, such digital line interface units and such
5 depacketizers are known in the art.

Received LAPD frames from receive network facilities 211-1 through 211-Y are supplied to digital line interface (DLI) units 213-1 through 213-Y, respectively. Each of digital line interface units 213 is of a type well known in the art for interfacing DS1 digital signals. In this example, each of digital line interface
10 (DLI) units 213 generates a facility failure signal in well known fashion. The facility failure signals from digital line interfaces 213-1 through 213-Y each indicate whether a red, yellow, blue, or performance alarm has occurred and are supplied via circuit paths 217-1 through 217-Y, respectively, to fault recovery unit 207. Each of digital line interface units (DLIs) 213-1 through 213-Y supplies the received LAPD
15 frames to receive frame bus 206. The received frames can be of many types, including received fault indication messages as shown in FIGs. 11 and 12. Fault recovery unit 207 obtains the received fault indication messages from receive frame bus 206 via circuit path 218, in well known fashion. An equipment failure signal indicating the failure of any unit in this node in the path of any virtual circuit is
20 supplied via circuit path 216 to fault recovery unit 207. Fault recovery unit 207 generates transmit fault indication messages which are supplied via circuit path 219 to transmit frame bus 209 and receive fault indication messages which are supplied via circuit path 221 to frame mapping unit 214. Fault recovery unit 207 supplies a frame relay remap control signal via circuit path 222 and an alternate virtual link ID
25 via circuit path 223 to frame mapping unit 214. Frame mapping unit 214 obtains the received frames from receive frame bus 206. Additionally, frame mapping unit 214 relays transmit frames from receive frame bus 206 to transmit frame bus 209. To this end, frame mapping unit 214 employs the known frame relay procedure to remap these incoming frames into transmit frames that are supplied to transmit
30 frame bus 209. The relayed frames include appropriate address mapping for each virtual circuit. That is to say, LAPD frames that are passing through this node are frame relayed from receive frame bus 206 to transmit frame bus 209. The operation of frame mapping unit 214 is described below in conjunction with FIG. 9. In turn, the appropriate transmit frames are obtained from transmit frame bus 209 by digital
35 line interface units 215-1 through 215-Y and, then, supplied to transmit network facilities 212-1 through 212-Y, respectively. Pairs of receive network facilities

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211-1 through 211-Y and transmit network facilities 212-1 through 212-Y form the
network facilities (NFs) shown in FIG. 1.

       Fault recovery unit 207 monitors for fault indication messages (FIGs. 11
and 12) on receive frame bus 206. This is achieved by monitoring received frames

5   for those that match a prescribed format. To this end, control fields in the received
frames are monitored to determine if the frames include a fault indication message.
In this example, the prescribed format is the so-called LAPD XID frame format
denoting fault indication messages for either a fault condition or a clear condition, as
shown in FIG. 11 and FIG. 12, respectively. As shown in both FIG. 11 and FIG. 12

10 the affected virtual circuit ID (DLCI) is included in the DLCI fields, an indication (in
this example, 10101111) that the LAPD frame is an XID frame is included in the
XID field, an indication that this XID frame is a fault indication message, in
accordance with an aspect of the invention, is included in the FI field and an
indication, in accordance with another aspect of the invention, of whether the fault

15 indication message denotes a fault or a clear condition is included in the GI field.
Thus, in this example, as shown in FIG. 11, the indication 11111010 in the GI field
denotes a fault condition and, as shown in FIG. 12, the indication 11110000 in the
GI field denotes a clear condition. It will be apparent to those skilled in the art that
other signaling arrangements may equally be employed to indicate the presence of a

20 fault indication message. Upon obtaining a fault indication message, fault recovery
unit 207 either sends an access circuit remap control signal to access circuit mapping
unit 205 causing it to switch a corresponding access circuit to an alternate virtual
link, in accordance with an aspect of the invention, or it sends a frame relay remap
control signal via circuit path 222 and an alternate virtual link ID via circuit path 223

25 to frame mapping unit 214 causing it to switch the corresponding virtual link to an
alternate virtual link, in accordance with an aspect of the invention, or it sends a
corresponding receive fault indication message via circuit path 221 to frame
mapping unit 214. In turn, frame mapping unit 214 supplies the fault indication
message to another node on a virtual link included in the primary virtual circuit.

30 Additionally, fault recovery unit 207 monitors for facility or equipment failures, and
either orders access circuit mapping unit 205 via access circuit remap control signal
or frame mapping unit 214 via frame relay remap control signals to switch the
affected access circuits or virtual links to alternate virtual links and/or generates
transmit fault indication messages to be passed via transmit frame bus 209 and

35 appropriate ones digital line interface (DLI) units 215-1 through 215-Y and transmit
network facilities 212-1 through 212-Y, respectively, to other ones of nodes 101 in

network 100 (FIG.1). Further details regarding operation of fault recovery unit 207 are discussed below in conjunction with FIGs. 3 through 6.

FIG. 3 depicts, in simplified block diagram form, details of fault recovery unit 207 of FIG. 2. Accordingly, shown are fault indication message

5   receiver 301 and fault indication message generator 302. Fault indication message receiver 301 obtains received fault indication messages via circuit path 218 from receive frame bus 206. If the received fault indication message is for an access circuit in this node, the access circuit remap control signal for that access circuit is activated and supplied via circuit path 220 to access circuit mapping unit 205. If the

10   received fault indication message is on a virtual link that has one or more alternate virtual links in this node, the frame relay remap control signal and the alternate virtual link ID (DLCI) are supplied via circuit paths 222 and 223, respectively, to frame mapping unit 214. If a received fault indication message is not for an access circuit in this node and if it is not on a virtual link that has one or more alternate

15   virtual links in this node, it is supplied unchanged via circuit path 221 to frame mapping unit 214. The operation of fault indication message receiver 301 is shown in the flow chart of FIG. 4 and described below. Fault indication message generator 302 is responsive to either a facility failure signal or an equipment failure signal becoming active or inactive. When either failure signal becomes active, fault

20   indication message generator 302 determines if the failure affects an access circuit terminated in this node or if it affects a virtual link that has one or more alternate virtual links in this node. If an access circuit terminated in this node is affected, an access circuit remap control signal for the access circuit is activated. If a virtual link that has one or more alternate virtual links in this node is affected, a frame relay

25   remap control signal for the virtual link is activated. If the affected virtual circuit is not terminated in this node and if no alternate virtual links exist for the affected virtual link, in this example, two fault indication messages including a fault indication (FIG. 11) are generated for the affected virtual circuit. One fault indication message is sent on the virtual circuit in the direction of the fault and the

30   other one is sent in the direction away from the fault. Similarly, when the fault is cleared, either the access circuit remap control signal or the frame relay remap control signal is deactivated, or two fault indication messages including a clear indication (FIG. 12) are generated. Operation of fault indication message generator 302 is described below in conjunction with the flow chart shown in FIGs. 5, 6 and 7.

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FIG. 4 is a flow chart showing a sequence of operations effected in fault indication message receiver 301 of FIG. 3. Accordingly, the sequence is entered via step 401. Thereafter, conditional branch point 402 tests to determine if there is a received fault indication message on receive frame bus 206 (FIG. 2). If the test

5   result is NO, the sequence is exited via step 403. If the test result in step 402 is YES, operational block 404 determines the virtual link identification corresponding to the obtained fault indication message. In the LAPD format this identification (ID) is known as the DLCI. Then, conditional branch point 405 tests to determine if the determined virtual link ID (DLCI) is mapped to an access circuit in this node. If the

10 test result in step 405 is NO, conditional branch point 406 tests to determine if the determined virtual link ID (DLCI) has one or more alternate virtual links in this node. If the test result in step 406 is YES, conditional branch point 407 tests to determine if the fault indication message indicates a fault. As indicated above, a fault indication message indicates a fault, in this example, when field GI includes

15 1111010, as shown in FIG. 11. If the test result in step 407 is YES, operational block 408 selects one of the alternate virtual link IDs and supplies it as an output from fault recovery unit 207 via circuit path 223 to frame mapping unit 214. This selection may be done in many ways, including measuring congestion in the network facilities and choosing an alternate virtual link on the least congested network

20 facility. Operational block 409 then supplies as an output an activated frame relay remap control signal for this virtual link via circuit path 222 to the frame mapping unit 214. The sequence is then exited via step 403. If the test result in step 407 is a NO, the fault indication message indicates a clear condition and operational block 410 supplies as an output a deactivated frame relay remap control signal via circuit

25 path 222 to frame mapping unit 214. A fault indication indicates a clear condition, in this example, when field GI includes 11110000, as shown in FIG. 11. The sequence is then exited via step 403. If the test result of 406 is NO, the virtual link denoted by this DLCI is frame relayed via frame mapping unit 214 (FIG. 2) through this node. To this end, operational block 411 supplies as an output the received fault

30 indication message to frame mapping unit 214 (FIG. 2). Thereafter, the sequence is exited via step 403. If the test result in step 405 is YES, the virtual link denoted by this DLCI is mapped to an appropriate access circuit in this node, i.e., the virtual circuit is terminated at this node. Conditional branch point 412 tests to determine whether the received fault indication message indicates the activating of a fault or

35 the clearing of a fault (FIG. 11 or FIG. 12, respectively). If the test result in step 412 is YES, indicating the activation of a fault, operational block 413 supplies as an

output an activated access circuit remap control signal for this virtual link ID (DLCI) to access circuit mapping unit 205 (FIG. 2). Thereafter, the sequence is exited via step 403. If the test result in step 412 is NO, indicating clearing of a fault, operational block 409 supplies as an output a deactivated access circuit remap

5   control signal for this virtual link ID (DLCI) to access circuit mapping unit 205 (FIG. 2). Thereafter, the sequence is exited via step 403. Alternatively, the operations of steps 402, 404 and 405 could be reversed in order, such that steps 404 and 405 are performed for all received frames and if the test result in step 405 is YES, then step 402 is performed to determine if the received frame includes a fault

10   indication message.

FIGs. 5, 6 and 7, when connected as shown, form a flow chart of a sequence of operations effected by fault indication message generator 302 of FIG. 3. Accordingly, the sequence is entered via step 501. Thereafter, conditional branch point 502 tests changes in the state of either the facility failure signal or equipment

15   failure signal. The active state indicates that a fault has occurred and the inactive state indicates that no fault is present, i.e., a clear condition. If there is no change in the state of these failure signals, the sequence is exited via step 503. If there is a change in the state of either of the failure signals, conditional branch point 504 tests to determine if the change of state in either of the failure signals affects any virtual

20   link that is mapped to an access circuit at this node. If the test result in step 504 is NO, control is supplied to conditional branch point 505 (FIG. 6). If the test result in step 504 is YES, operational block 506 determines which access circuits are affected. It is noted that more than one access circuit may be affected. Then, operational block 507 determines the virtual link ID (DLCI) for each affected access circuit.

25   Conditional branch point 508 tests to determine if the change in state of either failure signal is from inactive to active. If the test result in step 508 is YES, operational block 509 activates the access circuit remap control signal for this virtual link ID (DLCI). Then, control is supplied to conditional branch point 505 (FIG. 6) If the test result in step 508 is NO, operational block 510 deactivates the access circuit remap

30   control signal for this virtual link ID (DLCI). Thereafter, control is supplied to conditional branch point 505 (FIG. 6). Conditional branch point 505 tests to determine if the change in state of either failure signal in step 502 affects any virtual links for which one or more alternate virtual links are present in this node. If the test result in step 505 is NO, control is supplied to conditional branch point 511 (FIG. 7).

35   If the test result in step 505 is YES, operational block 512 determines the virtual link IDs (DLCIs) of the virtual links that have alternate virtual links present in this node.

Then, conditional branch point 513 tests to determine if the change in state in step 502 was from inactive to active, indicating a fault has occurred. If the test result in step 513 is YES, indicating a fault, operational block 514 selects an alternate virtual link for each determined virtual link ID (DLCI) from step 512 and supplies the

5   alternate virtual link ID to frame mapping unit 214. This selection may be done by considering network facility congestion, by using a priority scheme or in some other manner. Operational block 515 then activates the frame relay remap control signal for the determined virtual link IDs and supplies it as an output to frame mapping unit 214. Control is then passed to conditional branch point 511 (FIG.7). If the test

10   result in step 513 is NO, indicating a clear condition, operational block 516 supplies as an output a deactivated frame relay remap control signal to frame mapping unit 214 for the virtual link IDs determined in step 512. Control is then passed to conditional branch point 511 (FIG. 7). Conditional branch point 511 tests to determine if the change in state of either failure signal in step 502 affects any so-

15   called frame relay connection, i.e., virtual link to virtual link connection for which no alternate virtual links are present in this node. It is noted that an affected frame relay connection includes a faulted or cleared virtual link and a connected virtual link. If the test result in step 511 is NO, the sequence is exited via step 503 (FIG. 5). If the test result in step 511 is YES, operational block 517 determines which frame

20   relay connections are affected by the fault. Operational block 518 determines the virtual link ID (DLCI) and the network facility of the connected virtual link for each affected virtual link. Operational block 519 generates, in this example, two fault indication messages for each affected frame relay connection. The virtual link ID (DLCI) that was determined in step 518 is used as the address for one of the fault

25   indication messages and the affected virtual link ID is used for the address of the other fault indication message. Conditional branch point 520 tests to determine whether the change in state of either failure signal in step 502 is from inactive to active. If the test result in step 520 is YES, operational block 521 causes the fault indication messages generated in block 519 to indicate "fault" (GI field includes

30   1111010, FIG. 11). If the test result in step 520 is NO, operational block 522 causes the fault indication messages generated in block 519 to indicate "clear" (GI field includes 11110000, FIG. 12). Thereafter, operational block 523 supplies as an output the fault indication messages to transmit frame bus 209 (FIG. 2). Then, the sequence is exited via step 503 (FIG. 5).

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FIG. 8 is a flow chart of a sequence of operations effected by access circuit mapping unit 205 of FIG. 2. Accordingly, the sequence is entered via step 801. Thereafter, conditional branch point 802 tests to determine if a received frame is present on receive frame bus 206 (FIG. 2). If the test result in step 802 is YES,

5 operational block 803 determines the virtual link ID (DLCI) for the received frame. Conditional Branch point 804 tests to determine if the access circuit remap control signal is active for this virtual link ID (DLCI). If the test result in 804 is YES, operational block 805 causes the virtual link ID (DLCI) determined in step 803 to be modified to a DLCI for the appropriate virtual link ID of the primary virtual circuit.

10 If the test result in step 804 is NO, no action is taken to change the virtual link ID (DLCI) and operational block 806 supplies the received frame to depacketizer 208 (FIG. 2). Thereafter, the sequence is exited via step 807. Returning to step 802, if the test result is NO, conditional branch point 808 tests to determine if there is a generated frame from packetizer 204 (FIG. 2). If the test result in step 808 is NO,

15 the sequence is exited via step 807. If the test result in step 808 is YES, operational block 809 determines the virtual link ID (DLCI) for the generated frame. Then, conditional branch point 810 tests to determine if the access circuit remap control signal is active for this virtual link ID (DLCI). If the test result in step 810 is YES, operational block 811 changes the virtual link ID (DLCI) in the generated frame to

20 the alternate virtual link ID (DLCI) for the appropriate alternate virtual link. Then, operational block 812 supplies as an output the generated frame to transmit frame bus 209 (FIG. 2). Thereafter, the sequence is exited via step 807. Returning to step 810, if the test result is NO, the generated frame DLCI is not changed and steps 812 and 807 are iterated.

25 FIG. 9 is a flow chart of a sequence of operations effected in frame mapping unit 214 of FIG. 2. This flow chart does not completely describe the LAPD frame relay function known to the art but only those functions necessary to this embodiment of the invention. Accordingly, the sequence is entered via step 901. Then, conditional branch point 902 tests to determine if there is a received frame on

30 receive frame bus 206 (FIG. 2). If the test result in step 902 is NO, conditional branch point 903 tests to determine if there is a receive fault indication message on receive frame bus 206 (FIG. 2). If the result in step 903 is NO, the sequence is exited via step 904. If the test result in either step 902 or step 903 is YES, operational block 905 determines the virtual link ID (DLCI) for the received frame.

35 Operational block 906 determines the virtual link ID (DLCI) for the connected virtual link, i.e., the frame relay connection. Conditional branch point 907 tests to

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determine if the frame relay remap control signal from fault recovery unit 207 is
active for the virtual link ID (DLCI) determined in block 906. If the test result in
step 907 is YES, operational block 908 determines the alternate virtual link ID
(DLCI) as supplied from fault recovery unit 207 (FIG. 2). Operational block 909
5   then changes the virtual link ID (DLCI) of the received frame to the alternate virtual
link ID (DLCI) determined in step 908. Control is then passed to operational block
911. If the test result in step 907 is NO, operational block 910 changes the virtual
link ID (DLCI) of the received frame to the virtual link ID (DLCI) for the connected
virtual link. Operational block 911 supplies as an output the modified "received"
10   frame to the transmit frame bus 209 (FIG. 2). Thereafter, the sequence is exited by
step 904.

         Although this embodiment of the invention has been described in terms
of so-called provisioned virtual circuits and frame-relay, it will be apparent to those
skilled in the art that the invention is equally applicable to switched virtual circuits
15   and to frame switching arrangements. Additionally, it will also be apparent that the
fault indications, i.e., fault or clear, may be transported in other ways than individual
faults indication messages for each affected virtual circuit. Indeed, fault indication
messages including the identification of all virtual circuits being transported on a
network facility could be employed. See co-pending application Serial No.
20   (F. D. Fite Case 2) for an arrangement using such fault indication messages.
Moreover, it will be apparent to those skilled in the art that still other transport
techniques may be employed to transport the fault indication message to the
unknown nodes to effect the fault recovery in accordance with the principles of the
invention.

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Claims:

1. Apparatus in a packet node for recovering from faults in transmission paths including at least one virtual circuit in a network including a plurality of packet nodes, comprising,

5   means for detecting faults in at least one transmission path associated with the node,

the first being CHARACTERIZED BY,

first means for determining if any virtual circuit affected by a detected fault is terminated in the node,

10   second means for determining if any virtual circuit affected by the fault has at least one alternate virtual circuit present in the node,

means for generating fault indication messages for virtual circuits affected by the detected fault that are not terminated in the node and have no alternate virtual circuit present in the node,

15   first means for transmitting each of said generated fault indication messages on associated virtual circuits to some other node in the network, and

means for switching any affected virtual circuits determined to be terminated in the node or determined to have at least one alternate virtual link present in the node to associated alternate virtual circuits for transmission toward a

20 destination node.

2. The apparatus as defined in claim 1 being CHARACTERIZED BY

means for receiving fault indication messages including third means for determining if a virtual circuit identified in a received fault indication message is terminated in the node and fourth means for determining if a virtual circuit identified

25 in a received fault indication message has at least one alternate virtual link present in the node, and

second means for transmitting any of said received fault indication messages not associated with a virtual circuit terminated in the node or not having at least one alternate virtual circuit present in the node on associated virtual circuits to

30 some other node in the network.

3. The apparatus as defined in claim 2 CHARACTERIZED IN THAT each of said virtual circuits comprises a first access circuit at an originating node, a second access circuit at a destination node and at least one virtual link.

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4. The apparatus as defined in claim 3 CHARACTERIZED IN THAT said first means for transmitting includes means for transmitting said fault indication messages in a direction away from the detected fault and towards the detected fault on said associated virtual circuits.

5. The apparatus as defined in claim 3 CHARACTERIZED BY said received fault indication message including an identity of an affected virtual link of a virtual circuit, and CHARACTERIZED IN THAT said third means for determining includes means for generating a first control signal representative of whether said virtual link identified in the received fault indication message is mapped to an access circuit in the node, said fourth means for determining includes means for generating a second control signal representative that at least one alternate virtual link is present in the node for said virtual link identified in said received fault indication message, and said means for switching includes first switching means being responsive to said first control signal for changing the identity of said identified virtual link to an alternate virtual link identity when said first control signal indicates that said virtual link is mapped to an access circuit in the node, wherein said access circuit is mapped to an alternate virtual circuit for transmission to said access circuit in said destination node and second switching means being responsive to said second control signal for selecting and identifying said at least one alternate virtual link so that said identified affected virtual link is mapped to said selected at least one alternate virtual link for transmission to said access circuit at said destination node.

6. The apparatus as defined in claim 3 CHARACTERIZED IN THAT said first means for determining includes means for identifying access circuits in the node that are affected by the detected fault, means for identifying an associated virtual link for each access circuit in the node which is affected by the detected fault and means for generating an access circuit control signal representative that a corresponding access circuit is mapped to a virtual link that is affected by the detected fault, said second means for determining includes means for selecting and identifying an at least one alternate virtual link present in the node for each virtual link associated with the node that is affected by the fault and not terminated in the node and means for generating a frame relay control signal representative that an identified alternate virtual link is to be mapped to said identified affected virtual link, and wherein said means for switching includes means responsive to said access circuit control signal for changing the identity of said virtual link associated with the

identified access circuit to an alternate virtual link identity, wherein said access circuit is mapped to an alternate virtual circuit and means responsive to said frame relay control signal for mapping said identified affected virtual link to said identified alternate virtual link.

5   7. The apparatus as defined in claim 3 CHARACTERIZED BY said virtual circuit may include a virtual link being mapped to another virtual link in a node, and CHARACTERIZED IN THAT said means for generating a fault indication message includes means for identifying a virtual link to which a virtual link affected by the detected fault is mapped to and means for including the identity

10 of the identified virtual link as an address for the fault indication message being generated for the affected virtual circuit, and wherein said first means for transmitting supplies said generated fault indication message as an output on an associated affected virtual circuit.

    8. The apparatus as defined in claim 3 CHARACTERIZED IN THAT

15 said second means for transmitting includes means for determining an identity of a virtual link in said received fault indication message, means for determining an identity of an associated virtual link to which said identified virtual link is to be connected to, means for changing the virtual link identification in the fault indication message to that of the associated virtual link and means for supplying the fault

20 indication message including the associated virtual link identity as an output on an associated affected virtual circuit.

    9. The apparatus as defined in claim 3 CHARACTERIZED BY said fault indication message comprises a frame including a plurality of fields, a predetermined field including an identity of a virtual link of a virtual circuit affected by the detected

25 fault and a field including an indication of whether a fault condition exists.

    10. The apparatus as defined in claim 9 CHARACTERIZED BY a field in said frame includes an indication representative that the frame is a fault indication message.

    11. The apparatus as defined in claim 10 CHARACTERIZED BY said

30 frame being a LAPD XID frame having a field including an indication that the frame is an XID frame.

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12. A method for recovering from faults in transmission paths including at least one virtual circuit associated with a packet node in a network including a plurality of packet nodes, comprising the step of,

detecting faults in at least one transmission path associated with the

5   node,

the method being CHARACTERIZED BY

determining if any virtual circuit affected by a detected fault is terminated in the node,

determining if any virtual circuit affected by the fault has at least one

10   alternate virtual circuit present in the node,

generating fault indication messages for virtual circuits affected by the detected fault that are not terminated in the node and have no alternate virtual circuit present in the node,

transmitting each of said generated fault indication messages on

15   associated virtual circuits to some other node in the network, and

switching any affected virtual circuits determined to be terminated in the node or determined to have at least one alternate virtual link present in the node to associated alternate virtual circuits for transmission toward a destination node.

13. The method as defined in claim 12 CHARACTERIZED BY the steps

20   of

receiving fault indication messages including the steps of determining if a virtual circuit identified in a received fault indication message is terminated in the node and determining if a virtual circuit identified in a received fault indication message has at least one alternate virtual link present in the node, and

25   transmitting any of said received fault indication messages not associated with a virtual circuit terminated in the node or not having at least one alternate virtual circuit present in the node on associated virtual circuits to some other node in the network.

14. The method as defined in claim 13 CHARACTERIZED BY each of

30   said virtual circuits comprises a first access circuit at an originating node, a second access circuit at a destination node and at least one virtual link.

15. The method as defined in claim 14 CHARACTERIZED BY a field in said frame includes an indication representative that the frame is a fault indication

message.

16. The method as defined in claim 15 CHARACTERIZED BY said frame being a LAPD XID frame having a field including an indication that the frame is an XID frame.
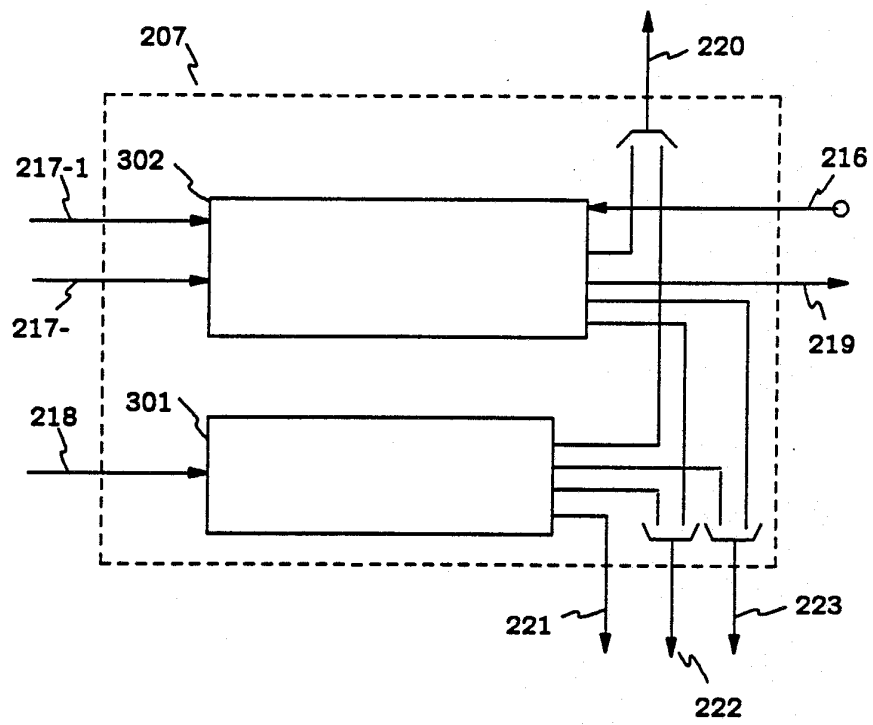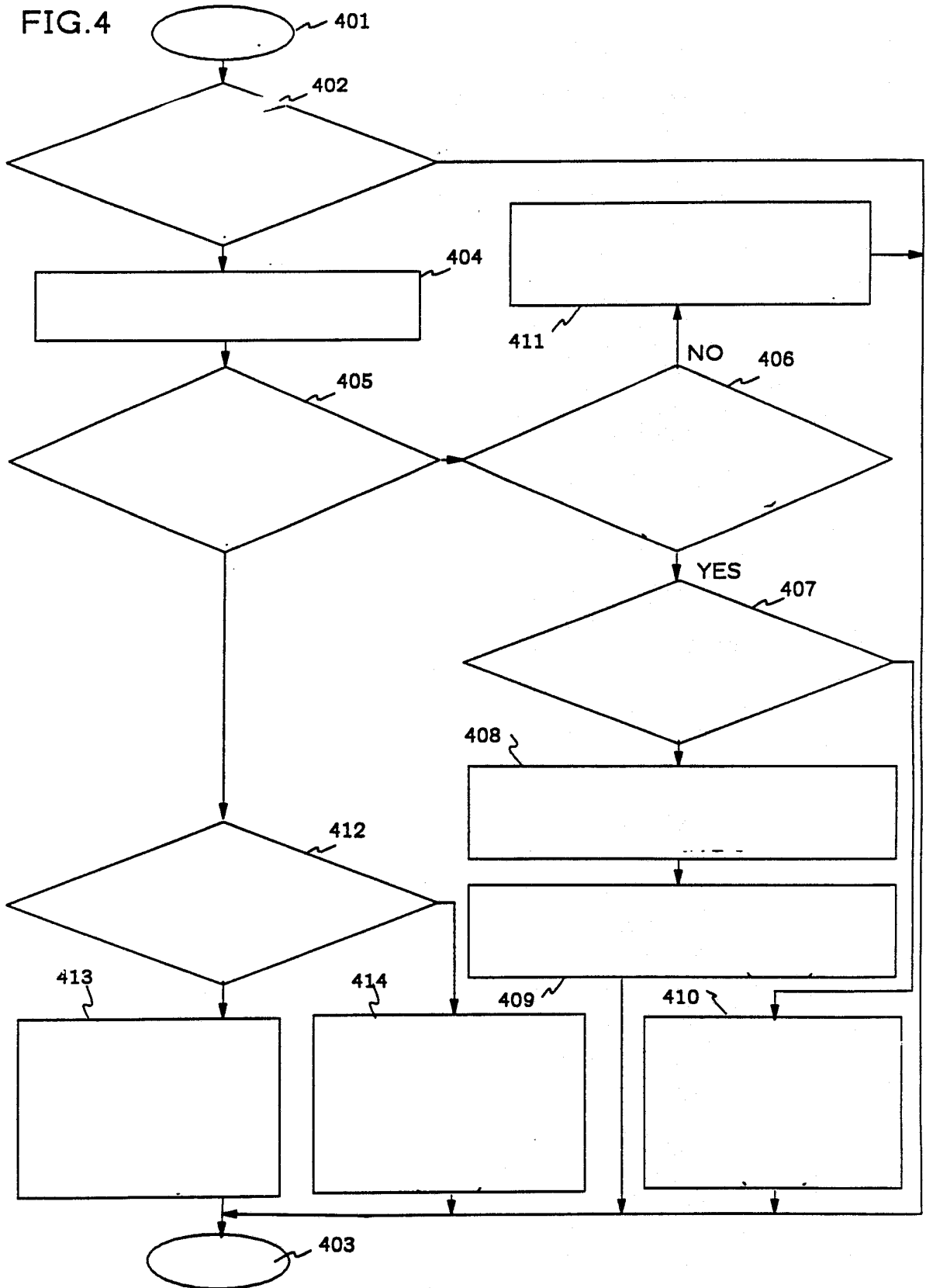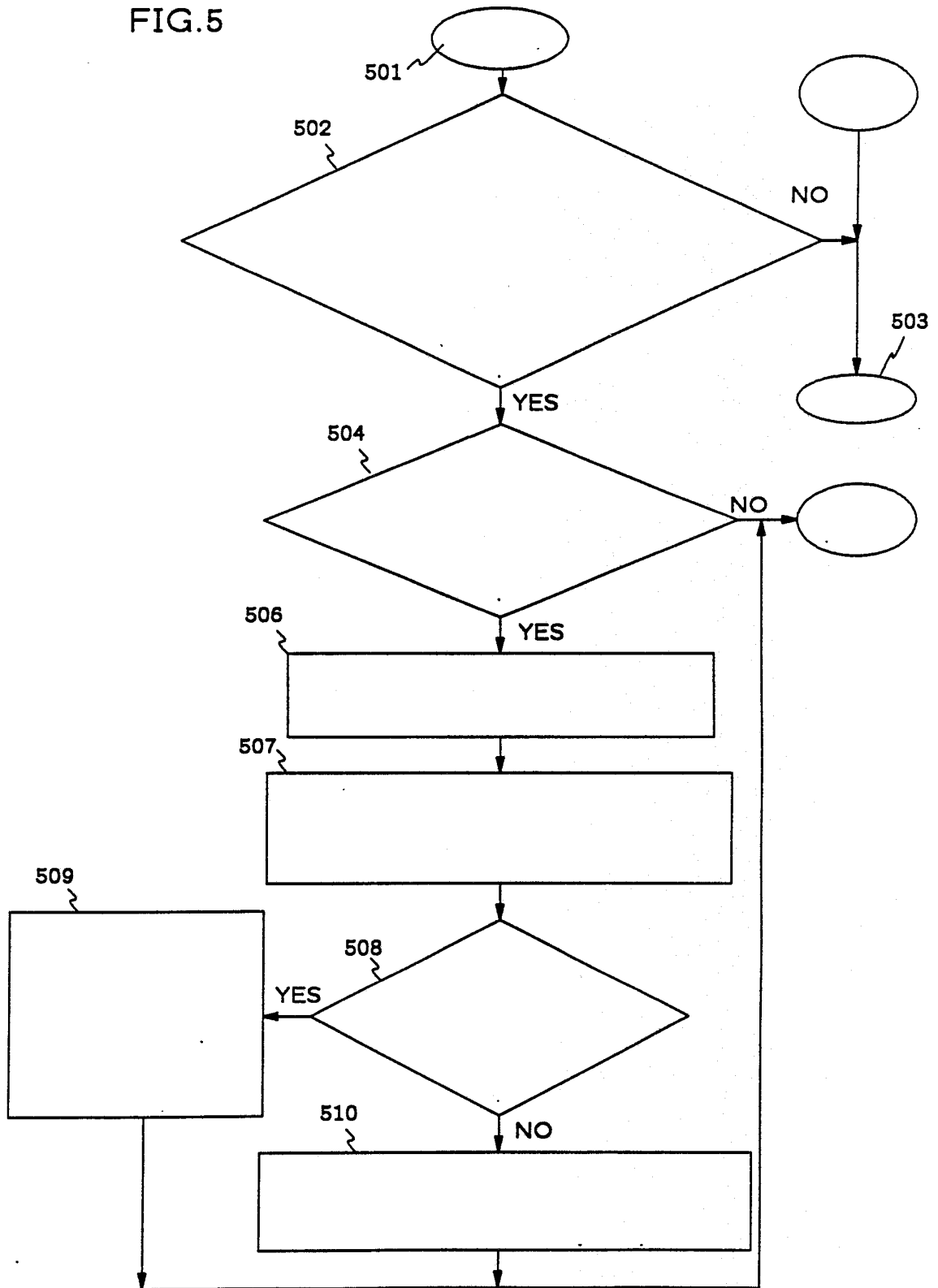
FIG.1

100
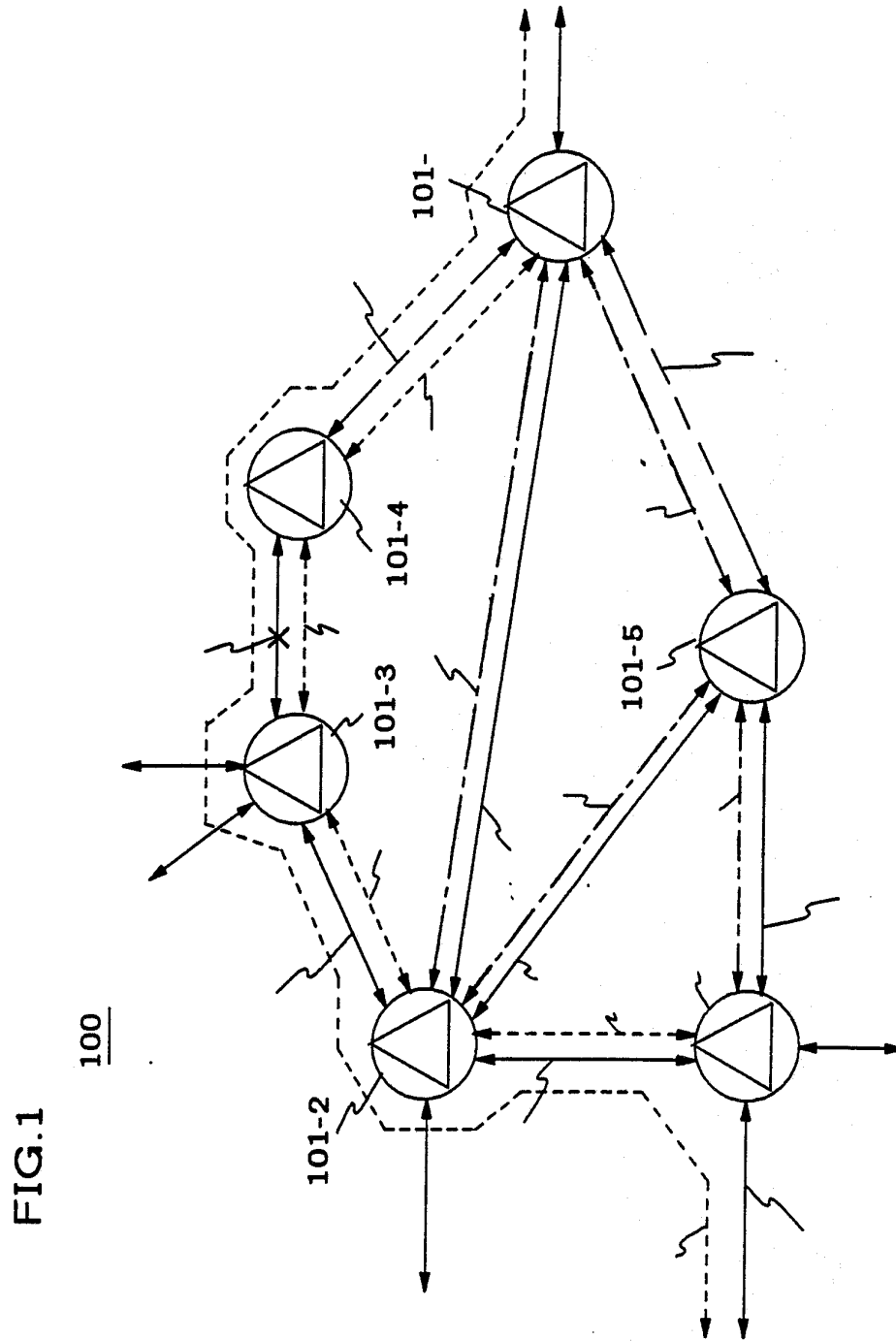
FIG.2

101
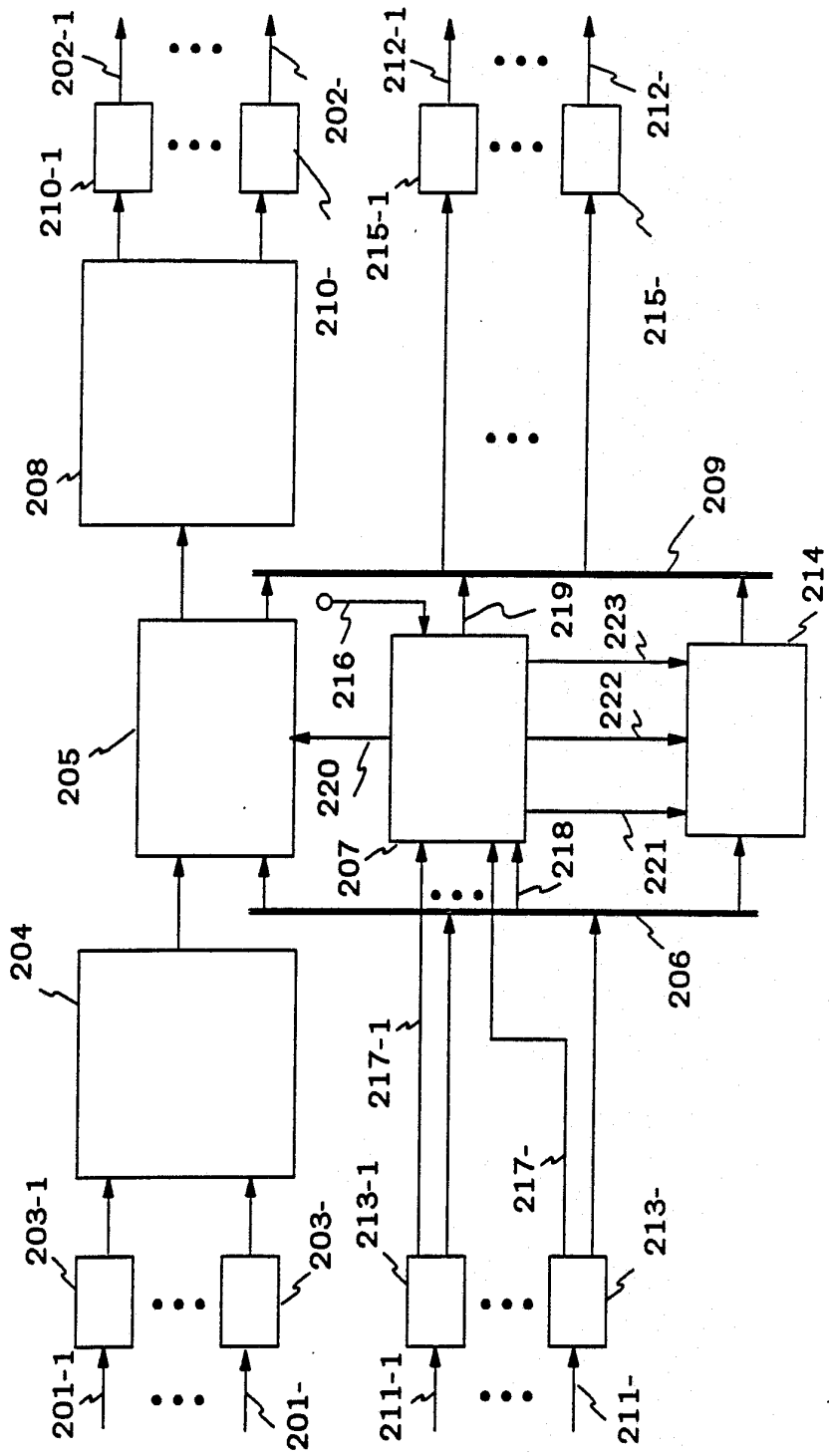
FIG.3

FIG.4

FIG.5

FIG.6
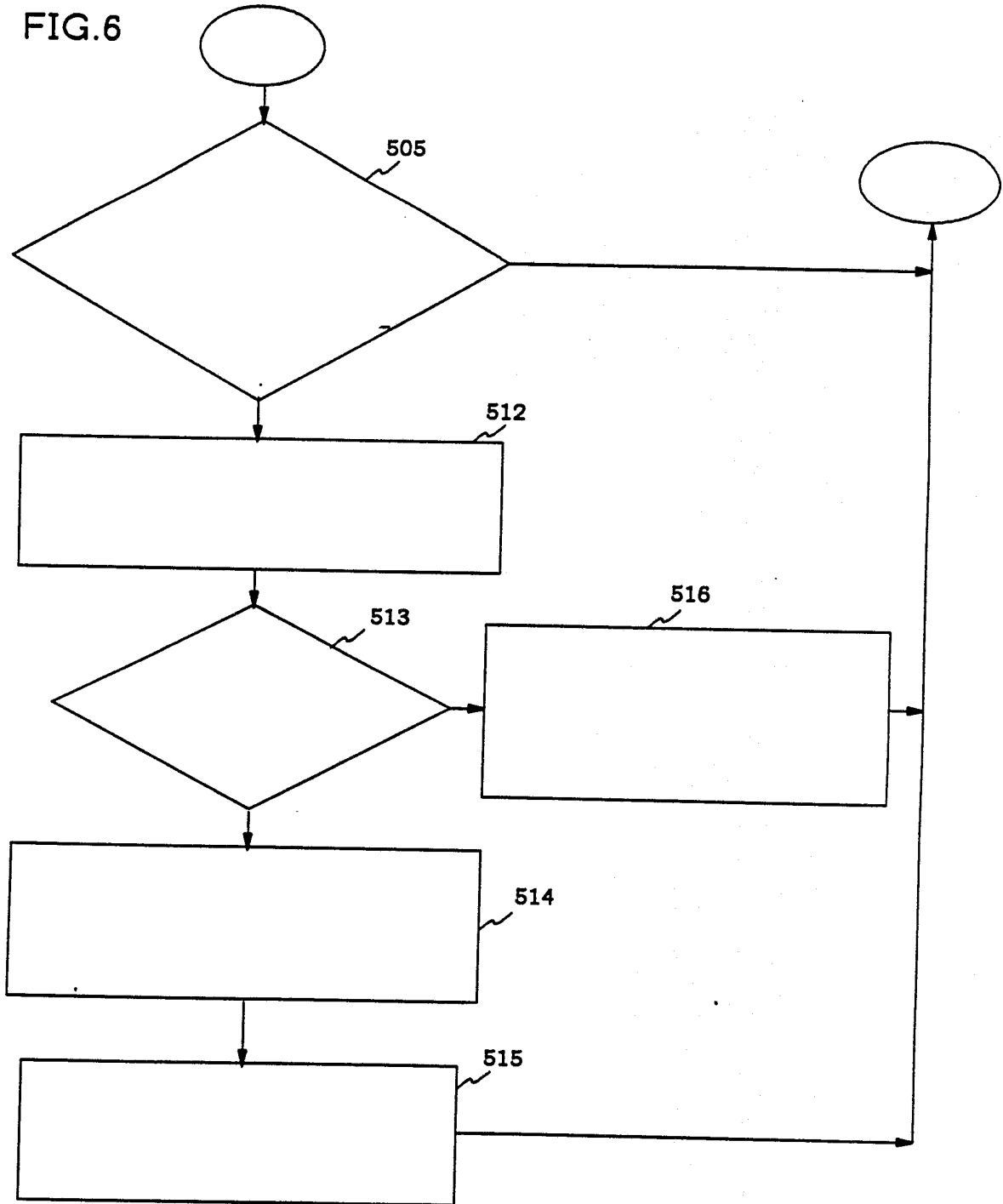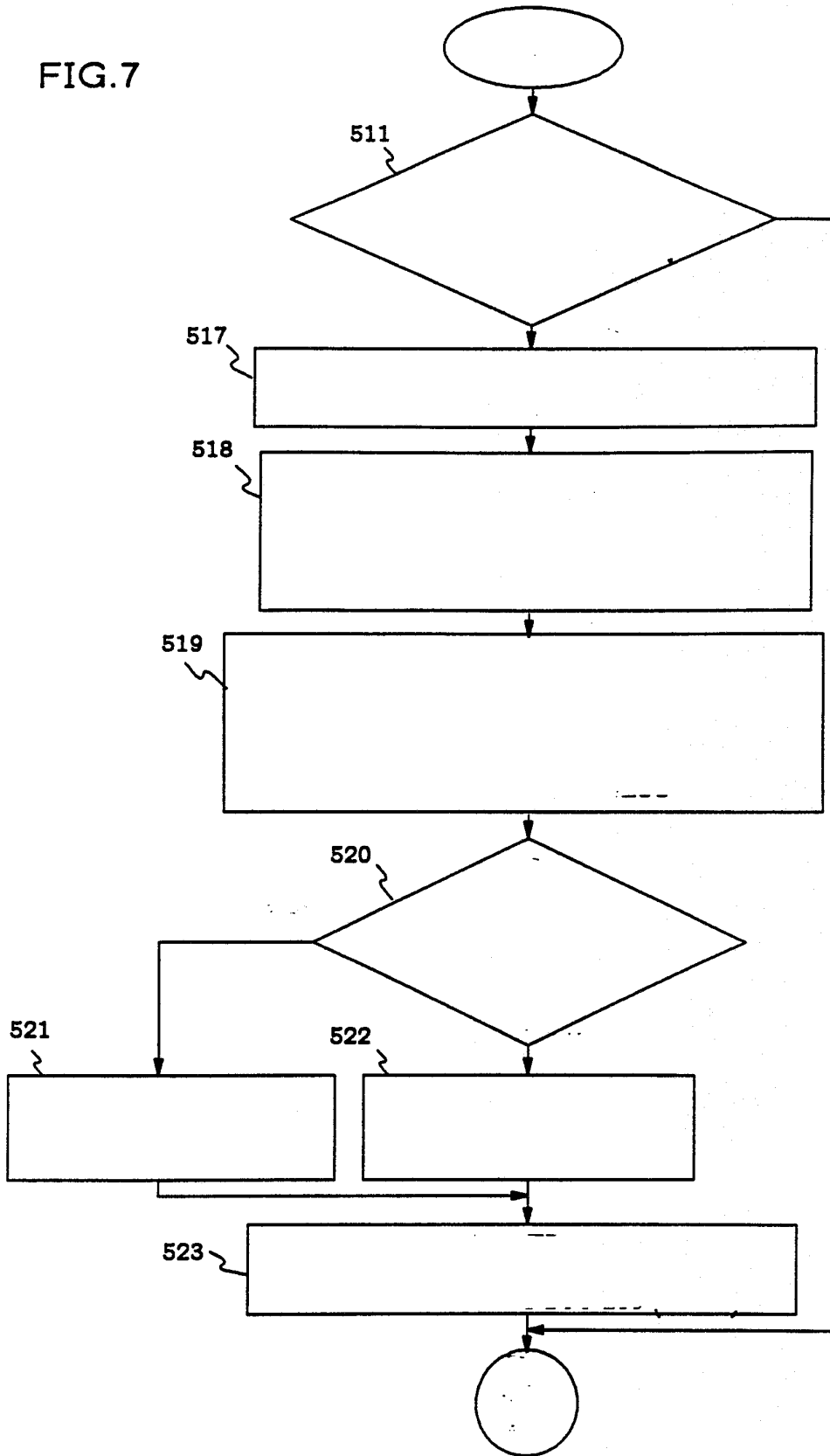
FIG.7

FIG.8

FIG.9

FIG.10

FIG.11

0111110	10101111	1000011	1111010

FIG.12
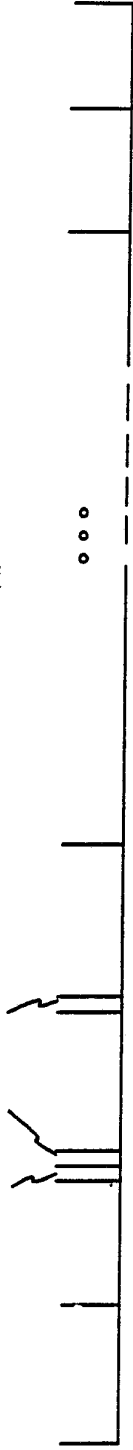
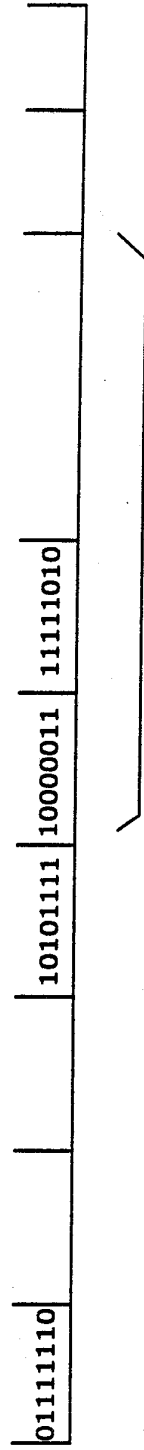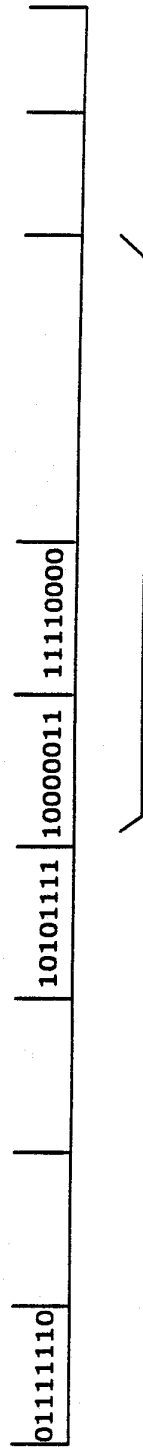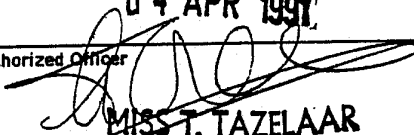| 0111110	10101111	1000011	1110000
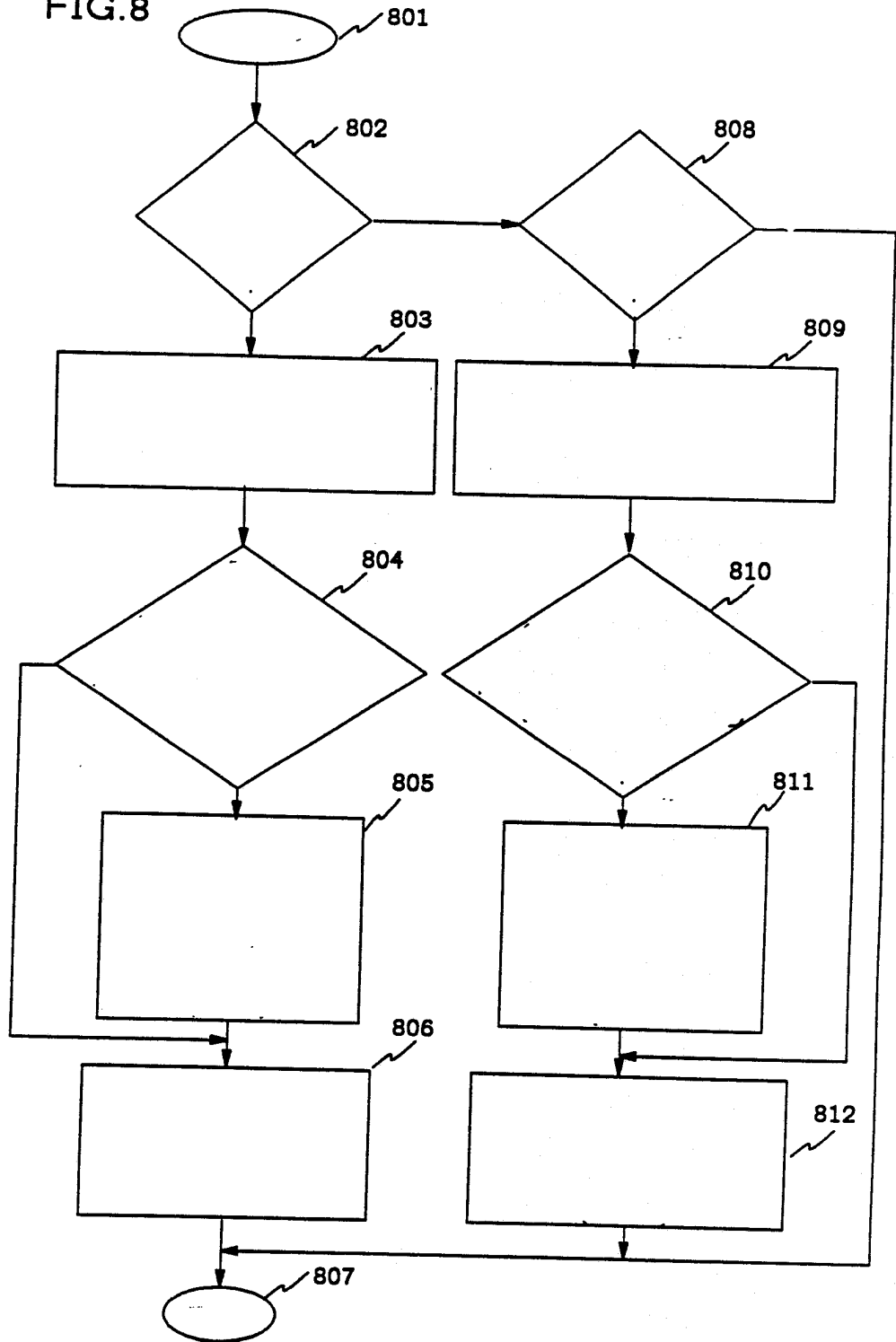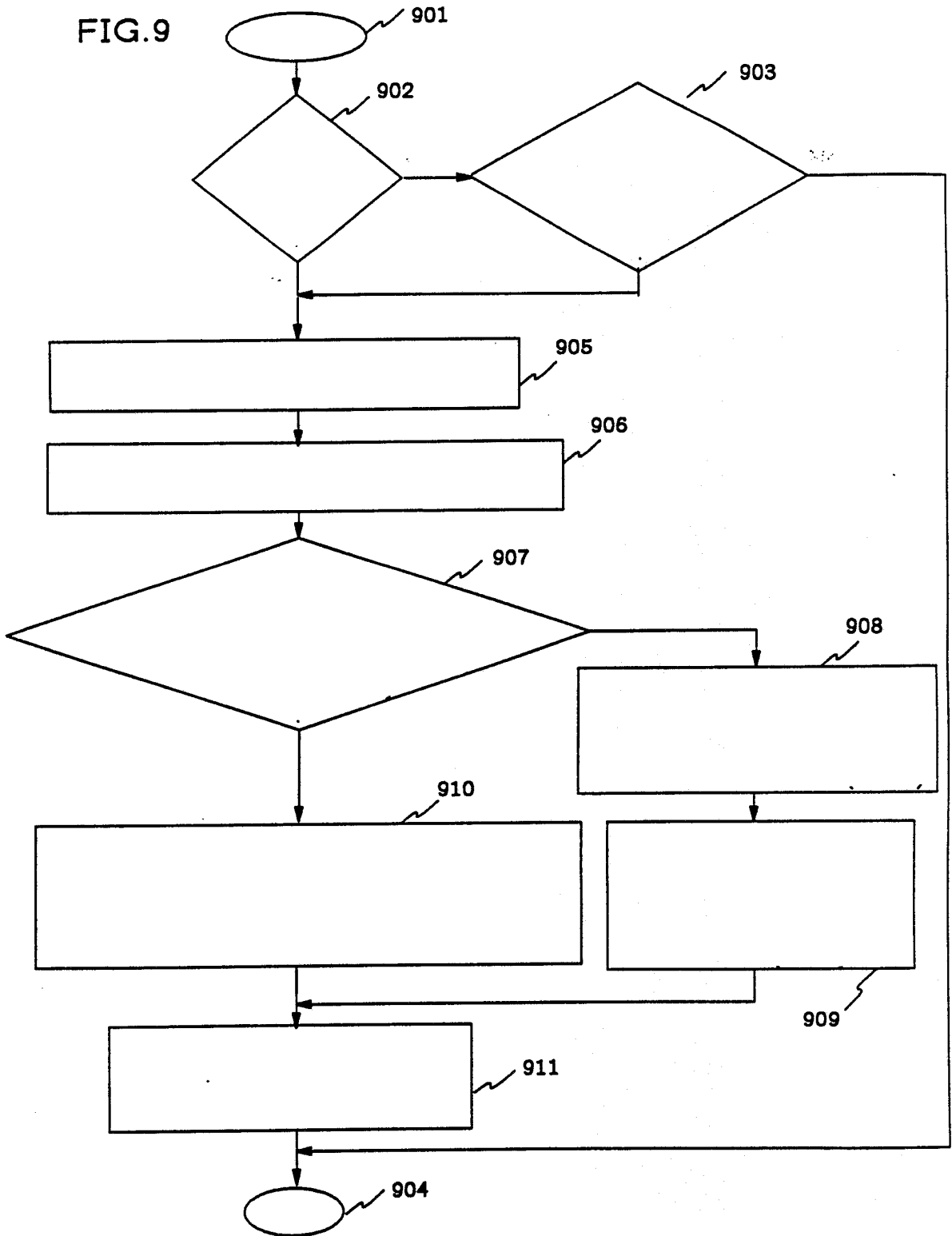
INTERNATIONAL SEARCH REPORT

International Application No **PCT/US 90/06549**

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: H 04 L 1/22

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	H 04 J, H 04 L, G 06 F

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category*	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	US, A, 4855993 (T HAMADA ET AL) 8 August 1989, see the whole document	1-16
	--	
A	US, A, 4679186 (C-T A LEA) 7 July 1987, see the whole document	1-16
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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
14th March 1991	0 4 APR 1991

International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	MISS T. TAZELAAR

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The members are as contained in the European Patent Office EDP file on   31/01/91
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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4855993	08/08/89	EP-A-	0280231	31/08/88
		JP-A-	63206045	25/08/88
US-A- 4679136	07/07/87	CA-A-	1234206	15/03/83
		CH-A-B-	669293	28/02/89
		DE-A-	3533846	03/04/86
		DE-A-	3534355	17/04/86
		FR-A-B-	2570914	28/03/86
		GB-A-	2168221	11/06/86
		JP-A-	61084942	30/04/86
		NL-A-	8502633	16/04/86

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