

(51) International Patent Classification:
H02M 3/335 (2006.01)(21) International Application Number:
PCT/US2008/083588(22) International Filing Date:
14 November 2008 (14.11.2008)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US): **SEMI-CONDUCTOR COMPONENTS INDUSTRIES, L.L.C.** [US/US]; 5005 E. McDowell Road - A700, Phoenix, Arizona 85008 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **LIDAK, Petr** [CZ/CZ]; Stachovicka 312, 74247 Hladke Zivotice (CZ). **BASSO, Christophe** [FR/FR]; 95, route de Leguevin, F-31820 Pibrac (FR). **CONSEIL, Stephanie** [FR/FR]; Res. Le Bois de Cabirol - Apt. C76, 6 avenue des Marots, F-31770 Colomiers (FR). **SUKUP, Frantisek** [CZ/CZ]; Zasova 715, 75661 Roznov P. R. (CZ).(74) Agents: **HIGHTOWER, Robert F.** et al.; Semiconductor Components Industries, L.L.C., Patent Administration - A700, P.O. Box 62890, Phoenix, AZ 85082-2890 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: QUASI-RESONANT POWER SUPPLY CONTROLLER AND METHOD THEREFOR

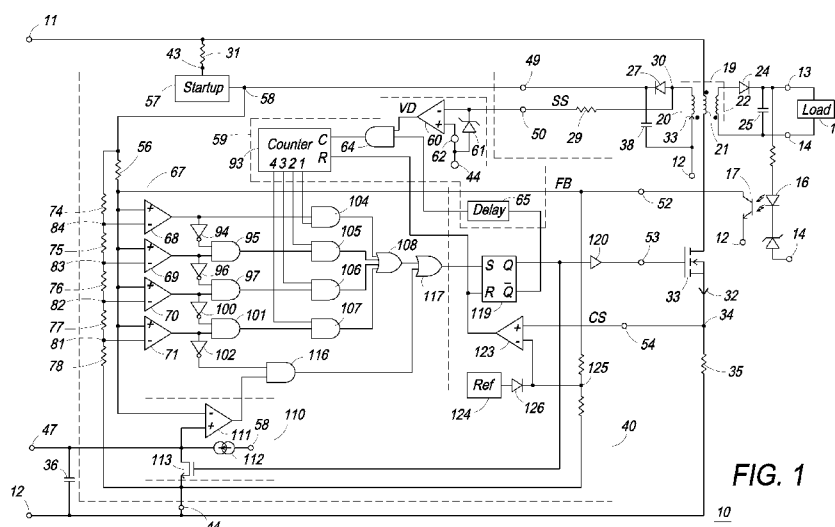


FIG. 1

(57) Abstract: In one embodiment, a quasi-resonant power supply controller is configured to select particular valley values of a switch voltage to determine a time to enable a power switch. The valleys values are selected responsively to a range of values of a feedback signal.

QUASI-RESONANT POWER SUPPLY CONTROLLER AND METHOD THEREFOR

Background of the Invention

5

The present invention relates, in general, to electronics, and more particularly, to semiconductors, structures thereof, and methods of forming semiconductor devices.

10

In the past, the semiconductor industry utilized various methods and structures to build switching power supply controllers that could be utilized in a power supply system such as in a flyback switching power supply system. In some applications, the switching power supply controllers were designed to operate in a discontinuous conduction mode and to use a value of the drain-to-source voltage across the switch transistor to determine the proper time for enabling the switch transistor. This was often referred to as a quasi-resonant operation or valley switching operation. During the operation of these power supply controllers, the switching frequency varied because the circuit kept the switch transistor disabled for a variable amount of time based on the voltage across the switch transistor. Because the frequency varied, prior controllers used different techniques to determine the proper time to re-enable the switch transistor. One particular technique sampled the frequency of oscillations there were formed by the voltage on the drain of the switch transistor and used the frequency to determine the proper time for re-enabling the switch transistor. However, this technique required complex circuitry which increased the cost of the power supply controller.

Accordingly, it is desirable to have a power supply controller that utilizes less complex circuitry, and that has a lower cost.

5

Brief Description of the Drawings

FIG. 1 schematically illustrates an embodiment of a portion of a system FIG. 1 schematically illustrates a
10 portion of an embodiment of flyback power supply system that also illustrates a portion of an exemplary embodiment of a power supply controller that is configured to operate in a quasi-resonant mode in accordance with the present invention;

15 FIG. 2 is a graph having plots that illustrate some of the signals formed by the power supply controller of FIG. 1 in accordance with the present invention; and

FIG. 3 illustrates an enlarged plan view of a semiconductor device that includes the power supply
20 controller of FIG. 1 in accordance with the present invention.

For simplicity and clarity of the illustration, elements in the figures are not necessarily to scale, and
25 the same reference numbers in different figures denote the same elements. Additionally, descriptions and details of well-known steps and elements are omitted for simplicity of the description. As used herein current carrying electrode means an element of a device that carries
30 current through the device such as a source or a drain of an MOS transistor or an emitter or a collector of a bipolar transistor or a cathode or anode of a diode, and a control electrode means an element of the device that controls current through the device such as a gate of an
35 MOS transistor or a base of a bipolar transistor.

Although the devices are explained herein as certain N-channel or P-Channel devices, or certain N-type or P-type

doped regions, a person of ordinary skill in the art will appreciate that complementary devices are also possible in accordance with the present invention. It will be appreciated by those skilled in the art that the words
5 during, while, and when as used herein relating to circuit operation are not exact terms that mean an action takes place instantly upon an initiating action but that there may be some small but reasonable delay, such as a propagation delay, between the reaction that is initiated
10 by the initial action. The use of the word approximately or substantially means that a value of an element has a parameter that is expected to be very close to a stated value or position. However, as is well known in the art there are always minor variances that prevent the values
15 or positions from being exactly as stated. It is well established in the art that variances of up to at least ten per cent (10%) (and up to twenty per cent (20%) for semiconductor doping concentrations) are reasonable variances from the ideal goal of exactly as described.

20

Detailed Description of the Drawings

FIG. 1 schematically illustrates a portion of an
25 embodiment of flyback power supply system 10 that also illustrates a portion of an exemplary embodiment of a power supply controller 40 that is configured to operate in a quasi-resonant mode. System 10 receives an input voltage between a power input terminal 11 and a power
30 return terminal 12, and regulates a value of an output voltage between a voltage output 13 and a voltage return 14. The output voltage usually is regulated to a target value within a range of values around the target value. For example, the target value may be five volts (5v) and
35 the range of values may be plus or minus five percent (5%) around the five volts. A load 15 is connected between

output 13 and return 14 to receive the output voltage and an output current in order to operate load 15. System 10 typically includes a transformer 19 that has a primary inductor or primary winding 21 that is connected to a switch, such as a power transistor 33. Controller 40 forms a switching drive signal that is used to operate transistor 33 and control a switch current 32 that flows through both transistor 33 and the primary or winding 21 in order to regulate the value of the output voltage. A sense resistor 35 typically is connected to transistor 33 in order to form a current sense (CS) signal that is representative of current 32. A secondary inductor or secondary winding 22 of transformer 19 is connected to supply a secondary voltage that is utilized to form the output voltage. In order to assist in forming the output voltage, a rectifier diode 24 typically is connected to winding 22 and a filter capacitor 25 typically is connected in parallel with output 13 and return 14. An auxiliary inductor or auxiliary winding 20 of transformer 19 is utilized to form an auxiliary voltage across winding 20 that is used to form an operating voltage for operating controller 40. A diode 27 and a capacitor 38 assist in forming the operating voltage. As will be seen further hereinafter, the switching of transistor 33 forms oscillations of a switch voltage. Controller 40 is configured to use a sense signal that is representative of the output voltage and to enable transistor 33 during one valley value, of a plurality of valley values that occur during the oscillations, responsively to a value of the sense signal.

Controller 40 is connected to receive a startup voltage for the initial startup operation of controller 40 through a high voltage input 43 and a common return 44. High-voltage input 43 generally is connected to terminal 11 through a resistor 31 so that controller 40 may receive

the input voltage (Vin) from terminal 11. Controller 40 includes an operating voltage input 49, a switch voltage sense (SS) input 50, a feedback (FB) input 52, a drive output 53, a current sense input 54, and a frequency control input 47. Controller 40 also includes a control circuit 67, a detector circuit or detector 59, a variable frequency oscillator (VCO) 110, and a switching control circuit that includes a PWM latch 119, a current sense (CS) comparator 123, and a high current driver 120.

Control circuit 67 includes comparators 68-71, AND gates 95, 97, 101, 104-107, and 116, inverters 94, 96, 100, and 102, OR gates 108 and 117, and a reference generator that includes voltage divider connected resistors 74-78. Detector 59 includes a valley comparator 60, a reference generator or reference 62, a clamp diode 61, an AND gate 64, a delay circuit 65, and a counter 93. VCO 110 includes a current source 112, a switch transistor 113, and a comparator 111. Such VCO circuits are well known to those skilled in the art.

Controller 40 also typically includes a startup circuit 57 that receives the input voltage from high voltage input 43 and assists in forming an operating voltage for operating controller 40. When power is first applied between terminals 11 and 12, startup circuit 57 receives an input current from terminal 11 through resistor 31. Circuit 57 uses this input current to supply a startup current through input 49 and charge capacitor 38. When the value of the voltage across capacitor 38 reaches a desired value of the operating voltage for operating controller 40, startup circuit 57 inhibits forming the startup current and typically supplies a signal (not shown) to other circuits of controller 40 that allows controller 40 to begin operating. As controller 40 begins operating and switching transistor 33, a voltage is formed across auxiliary winding 20 and a current is

applied through diode 27 to maintain capacitor 38 charged at the desired operating voltage for operating controller 40. During normal operation, the current from auxiliary winding 20 maintains capacitor 38 charged at the desired
5 operating voltage and startup circuit 57 no longer supplies the startup current to capacitor 38. Such startup circuits and auxiliary winding configurations are well known to those skilled in the art.

The switching drive signal formed by controller 40
10 enables transistor 33 in order to allow current 32 to flow through winding 21 and store energy within transformer 19. Current 32 flowing through resistor 35 forms the current sense (CS) signal, at a node 34, that is representative of the value of current 32. Comparator 123 compares the CS
15 signal to a signal from a node 125 that is representative of the FB signal and that is higher than the voltage from a reference generator or ref 124. When the value of the current sense signal is approximately equal to the value of the voltage from node 125, the output of comparator 123
20 goes high to reset latch 119 and negate the switching drive signal. Negating the switching drive signal disables transistor 33 and terminates the flow of current 32. As can be seen, the peak value of current 32 is a function of the value of the output voltage (through the
25 FB signal). Disabling transistor 33 causes transformer 19 to transfer the stored energy to windings 20 and 21 thereby transferring power to charge capacitor 25 and operate load 15, and also to regulate the operating voltage on input 49. Disabling transistor 33 also causes
30 the voltage formed between the drain of transistor 33 and terminal 12, the switch voltage, to increase.

FIG. 2 is a graph having plots that illustrate a portion of one switching cycle that is formed by controller 40. The abscissa indicates time and the
35 ordinate indicates increasing value of the illustrated

signal. A plot 130 illustrates the switch voltage formed between the drain of transistor 33 and return 12, a plot 132 illustrates a valley detected (VD) signal formed by valley comparator 60, and a plot 135 illustrates a portion of one cycle of the switching drive signal. Prior to a time T0 the switching drive signal is asserted as illustrated by plot 135 therefore transistor 33 is enabled and the value of the switch voltage is less than the value of the input voltage (V_{in}). Since latch 119 is set, the Q-bar output is low which forces the output of gate 64 low to ensure that counter 93 is not affected by noise (such that of the leakage inductor ringing) or other signals received on input 50. At time T0, comparator 123 resets latch 119 and negates the switching drive signal to disable transistor 33. The inductance of winding 21 pulls the drain of transistor 33 high to a voltage that is greater than the input voltage (V_{in}) which usually causes some ringing of the switch signal. This causes the switch voltage to increase until rectifier diode 24 conducts. At this point, the value of the switch voltage reaches the voltage of terminal 11 plus the so-called flyback voltage from transformer 19. This voltage level lasts as long as the energy stored in transformer 19 is fully transferred to the secondary side. When this period of time has elapsed, diode 24 blocks and the switch voltage returns to the voltage of terminal 11 via a series of N number of damped periodic oscillations as illustrated at times T2-TN. Note that resetting latch 119 forces the Q-bar output of latch high which triggers delay circuit 65 to keep the output of circuit 65 low for a time period after the Q-bar output goes high. This insures that the ringing of the switch signal at time T0 does not affect counter 93. Additionally, the high from comparator 123 resets counter 93 to prepare it for counting the valley values of the switch signal. Energy is transferred to the secondary

side of transformer 19 and the switch voltage remains relatively constant as shown by plot 130 after time T0 to just prior to a time T1 when the energy transfer is completed and the flux within transformer 19 is
5 collapsing. Because of the parasitic capacitance of transistor 33, the rapid change in voltage resulting from the demagnetizing of transformer 19 causes oscillations in the switch voltage as illustrated by plot 130 beginning just prior to time T1 and continuing thereafter. The
10 oscillations of the switch voltage form peak values and valley values or minimum values of the switch voltage. Because the energy transfer to the secondary is complete, it is time to re-enable transistor 33. However, it is desirable to re-enable transistor 33 when the value of the
15 switch voltage is at a minimum value or valley value. Enabling transistor 33 when the switch voltage is a minimum value improves the efficiency of system 10.

Detector 59 and control circuit 67 are configured to detect the valley values of the switch voltage, such as
20 the plurality of valley values illustrated as valley values V1-Vn, and to cause transistor 33 to be enabled during one valley value of these plurality of valley values. Controller 40 selects one of the valley values (V1-Vn) responsively to the value of the feedback signal.
25 Circuit 67 receives the feedback (FB) signal and forms a plurality of value ranges of the feedback signal around a plurality of values of the feedback signal so that a different value range of the plurality of ranges is formed around different values of the feedback signal.
30 Comparators 68-71 assist in forming the range of values around the different values of the feedback signal. The resistor divider formed by resistors 74-78 functions as a reference generator that forms a plurality of reference voltage values. The resistor divider forms a first
35 reference voltage at a node 84 that has a first value,

forms a second reference voltage at a node 83 that has a value that is less than the first reference voltage, forms a third reference voltage at a node 82 that has a value that is less than the second reference voltage, and forms
5 a fourth reference voltage at a node 81 that has a value that is less than the third reference voltage.

Detector 59 is configured to detect the plurality of valley values during a cycle of the switching drive signal and responsively form a plurality of valley detection
10 signals wherein a first valley detection signal is representative of detecting a first valley value, such as valley value V1, of the plurality of valley values and a second valley detection signal is representative of detecting a second valley value, such as valley value V2,
15 of the plurality of valley values that is different from the first valley value, etc. Detector 59 is configured to assert a separate control signal for each valley value upon detecting the occurrence of that particular valley value. The auxiliary voltage formed across the inductance
20 of auxiliary winding 20 causes current 32 to flow through winding 20, through a resistor 29, and form a switch sense signal at a node 30 that has a voltage that is representative of the value of the switch voltage. However, the value of the switch sense signal is
25 referenced to the value of return 12, therefore, the switch sense signal at node 30 is representative of the switch voltage and forms the switch voltage sense (SS) at input 50 that is also representative of the switch voltage. Valley comparator 60 receives the switch voltage
30 signal from input 50 and compares the switch sense signal to a reference signal from reference 62. As the switch voltage oscillates, the valley values that are formed cause the value of the switch sense signal to decrease below the value of the reference voltage from reference
35 62. Since counter 93 was previously reset by comparator

123, each time the switch voltage reaches a valley value, such as values V1-VN, the output of comparator 60 goes high as illustrated by plot 132 thereby forcing the valley detected (VD) signal high. Since counter 93 was
5 previously reset by comparator 123, the high from comparator 60 increments counter 93 which forces the first output (output one) of counter 93 high. Thus, the first valley value, V1, causes counter 93 to increment and assert the first valley detection signal at output one of
10 counter 93. The second valley value, V2, causes counter 93 to increment again and assert the second valley detection signal at output two of counter 93 in addition to keeping the first valley detection signal asserted. The third valley value, V3, causes counter 93 to increment
15 again and assert the third valley detection signal at output three of counter 93 in addition to keeping the first and second valley detection signals asserted. This incrementing of counter 93 continues for subsequent occurrences of the valley values during this cycle of the
20 switching drive signal.

Circuit 67 is configured to select one of the valley detection signals of the plurality of valley detection signals responsively to one value range of the plurality of value ranges of the output voltage (as represented by
25 the feedback signal). If the value of the feedback signal is within the first range of values, such as greater than the first reference voltage at node 84, the output of all of comparators 68-71 are high. However, the logic circuit formed by inverters 94, 96, and 100 and gates 95, 97, and
30 101 inhibit the output of comparators 69, 70, and 71 from affecting the control of the switching drive signal. The high from the output of comparator 68 forces the output of inverter 94 low which forces the output of gate 95 low and prevents comparator 69 from affecting the switching drive
35 signal. The low from gate 95 also forces the output of

gate 105 low which inhibits output two of counter 93 from affecting the switching drive signal. Similarly, the high from comparator 69 forces the output of inverter 96 low which forces the output of gate 97 low and the output of gate and 106 low thereby preventing the output of comparator 70 and also prevents comparator 70 and output three of counter 93 from affecting the switching drive signal. Similarly, the high from comparator 70 forces the output of inverter 100 low which in turn forces the output of gate 101 low and the output of gate 107 low thereby inhibiting the output of comparator 71 and output four of counter 93 from affecting the switching drive signal. Thus, it can be seen that as long as the value of the feedback signal is within the first range of values of the feedback signal, controller 40 selects the first valley detection signal from output one of counter 93 to set latch 119 and enable transistor 33 at the first valley value V1 as illustrated by the dashed portion of plot 135 at time T1. Enabling transistor 33 approximately at the first valley value could possibly cause the off-time of the cycle of the switching drive signal to be greater than the off-time for the maximum discontinuous mode operating frequency. Thus, the additional off-time could decrease the operating frequency. Consequently, this increased off-time may also cause an increase in the value of the feedback signal. However, as long the value of the feedback signal remains within the first range of values, controller 40 continues to enable transistor 33 for each cycle of the switching drive signal approximately at the first valley value.

If the value of the feedback signal decreases to a value that is not within the first range of values, such as within the second range of values that is less than the reference voltage on node 84 but greater than the value of the voltage on node 83, controller 40 enables transistor

33 approximately at the second valley value responsively to the feedback signal being within the second range of values. If the feedback signal is within the second range of values, the output of comparator 68 is low, thus gate 5 95 is enabled to be controlled by the output of comparator 69. The output of comparator 69 is high for the second range of values. When comparator 60 detects the first valley value, counter 93 is incremented to force output one high. Since comparator 68 is low, controller 40 is 10 inhibited from selecting the first valley detection signal, thus, controller 40 does not enable transistor 33. When comparator 60 detects the second valley value, counter 93 is incremented to force output two high. Since comparator 69 is high, controller 40 selects the second 15 valley detection signal and sets latch 119 to enable transistor 33 responsively to the feedback signal being within the second range of values. Enabling transistor 33 approximately at the second valley value may decrease the operating frequency; however, as long the value of the 20 feedback signal remains within the second range of values, controller 40 continues to enable transistor 33 for each cycle of the switching drive signal approximately at the second valley value. Those skilled in the art will appreciate that if the value of the feedback voltage 25 subsequently increases to a value that is within the first range of values, controller 40 will revert back to enabling transistor 33 approximately at the first valley value responsively to the feedback signal again being within the first range of values.

30 Similarly, if the value of the feedback signal decreases to a third range of values that is not within the first or the second range of values, such as within the range of values that is greater than the reference voltage on node 82 but less than the value of the voltage 35 on node 83, controller 40 enables transistor 33

approximately at the third valley value responsively to the feedback signal being within the third range of values. If the feedback signal is within the third range of values, the output of comparators 68 and 69 are low which forces the output of respective gates 104 and 105 low to inhibit controller 40 from selecting either of the first or second valley detection signals. Since the output of comparator 69 is low, gate 97 is enabled to be controlled by the output of comparator 70. The output of comparator 70 is high for the third range of values. When comparator 60 detects the first valley value, counter 93 is incremented to force output number one high. Since comparator 68 is low, controller 40 does not enable transistor 33. When comparator 60 detects the second valley value, counter 93 is again incremented to force output two high. Since comparator 69 is low, controller 40 does not enable transistor 33. When comparator 60 detects the third valley value, counter 93 is again incremented to force output three high. Since comparator 70 is high, controller 40 selects the third valley detection signal and sets latch 119 to enable transistor 33 responsively to the feedback signal being within the third range of values. Even though enabling transistor 33 approximately at the third valley value may decrease the operating frequency, as long the value of the feedback signal remains within the third range of values, controller 40 continues to enable transistor 33 for each cycle of the switching drive signal approximately at the third valley value.

Those skilled in the art will appreciate that controller 40 may be configured to detect N number of valley values by choosing the proper size of counter 93 in addition to choosing the corresponding number of comparators and reference voltage values for circuit 67.

If the value of the feedback voltage is less than a selected lower value or first value, controller 40 uses the oscillating frequency from VCO 110 to control the frequency at which transistor 133 is operated and inhibits
5 using the valley values to operate transistor 33. If the value of the feedback voltage is less than a reference voltage on node 81 but greater than the voltage on return 44, the output of comparators 68-71 are low. The low from comparator 71 force the output of inverter 102 high
10 thereby enabling gate 116 to be controlled by voltage controlled oscillator (VCO) 110. The oscillations from VCO 110 are used to set latch 119 and control the frequency at which transistor 133 is operated by the frequency of VCO 110. When operating in this mode, the
15 peak value of current 32 is substantially constant and is set by the value of the reference voltage from ref 124.

In the preferred embodiment, comparators 68-71 have hysteresis, thus, the limits of each of the range of values in affected by the values of the hysteresis voltage
20 of comparators 68-71. For example, in one embodiment comparators 68-71 had approximately 0.8 volts of hysteresis that was symmetrical to the center point of the hysteresis. In this embodiment, the value of the reference voltages on nodes 81-84 were 1.4 volts, 1.6
25 volts, 2.2 volts, and 2.8 volts respectively. Thus, comparators 71-68 received respective reference voltages of 1.4 volts, 1.6 volts, 2.2 volts, and 2.8 volts. Since comparators 68-71 had hysteresis, the upper and lower limits of the range of values depended on whether the
30 value of the feedback voltage was increasing or decreasing. For increasing values of the feedback voltage, the output of comparator 71 was high from FB values that were greater than 1.6 volts, the output of comparator 70 was high from FB values that were greater
35 than 2.0 volts, the output of comparator 69 was high from

FB values that were greater than 2.6 volts, and the output of comparator 68 was high from FB values that were greater than 3.2 volts. For decreasing values of the FB signal, the output of comparator 68 remained high until the FB
5 signal was less than 2.4 volts, the output of comparator 69 remained high until the FB signal was less than 1.8 volts, the output of comparator 70 remained high until the FB signal was less than 1.2 volts, and the output of comparator 71 remained high until the FB signal was less
10 than 0.8 volts.

In order to facilitate this functionality for controller 40, startup circuit 57 is connected between input 43 and return 44 in order to receive the input voltage and form an operating voltage on an output 58. A
15 first terminal of resistor 74 is connected to output 58 of circuit 57 and to input 49 of controller 40. A second terminal of resistor 74 is commonly connected to a first terminal of resistor 75, node 84, and an inverting input of comparator 68. A second terminal of resistor 75 is
20 commonly connected to node 83, an inverting input of comparator 69, and a first terminal of resistor 76. A second terminal of resistor 76 is commonly connected to node 82, an inverting input of comparator 70, and a first terminal of resistor 77. A second terminal of resistor 77
25 is commonly connected to node 81, an inverting input of comparator 71, and a first terminal of resistor 78. A second terminal of resistor 78 is connected to return 44. A first terminal of pull-up resistor 56 is connected to output 58 of circuit 57. A second terminal of resistor 56
30 is commonly connected to input 52, an inverting input of comparator 111, and a non-inverting input of comparators 68-71. The output of comparator 68 is commonly connected to a first input of gate 104 and an input of inverter 94. The output of inverter 94 is connected to a first input of
35 gate 95. The output of comparator 69 is commonly

connected to an input of inverter 96 and a second input of gate 95. The output inverter 96 is connected to a first input of gate 97. The output of comparator 70 is connected to a second input of gate 97 and a first input of inverter 100. The output of inverter 100 is connected to a first input of gate 101. The output of comparator 71 is commonly connected to a second input of gate 101 and to an input of inverter 102. The output of inverter 102 is connected to a first input of gate 116. The output of gate 101 is connected to a first input of gate 107 which has an output connected to a first input of gate 108. The output of gate 97 is connected to a first input of gate 106 which has an output connected to a second input of gate 108. The output of gate 95 is connected to a first input of gate 105 which has an output connected to a third input of gate 108. The output of gate 104 is connected to a fourth input of gate 108. An output of gate 108 is connected to a first input of gate 117. A second input of gate 108 is connected to a first output of counter 93. A second output of counter 93 is connected to a second input of gate 105. A third output of counter 93 is connected to a second input of gate 106, and a fourth output of counter 93 is connected to a second input of gate 107. An output of gate 117 is connected to a set input of latch 119. The Q output of latch 119 is commonly connected to an input of driver 120 and to a gate of transistor 113. The output of driver 120 is connected to output 53. The Q bar output of latch 119 is connected to an input of delay circuit 65 which has an output connected to a first input of gate 64. A second input of gate 64 is connected to the output of comparator 60. An inverting input of comparator 60 is commonly connected to input 50 and to a cathode of diode 61. An anode of diode 61 is connected to return 44 and to a first terminal of reference 62. A second terminal of reference 62 is connected to a non-inverting input of

comparator 60. Input 54 is connected to a non-inverting input of comparator 123 which has an inverting input commonly connected to node 125 and to an output of reference 124 through a diode 126. The output of
5 comparator 123 is commonly connected to the reset input of latch 119 and to a reset input of counter 93. A clock input of counter 93 is connected to an output of gate 64. Input 47 of controller 40 is commonly connected to a non-inverting input of comparator 111, a first terminal of
10 current source 112, and to a drain of transistor 113. A source of transistor 113 is connected to return 44. A second terminal of current source 112 is connected to output 58 of startup circuit 57. An output of comparator 111 is connected to a second input of gate 116 which has
15 an output connected to a second input of gate 117.

FIG. 3 schematically illustrates an enlarged plan view of a portion of an embodiment of a semiconductor device or integrated circuit 140 that is formed on a semiconductor die 141. Controller 40 is formed on die
20 141. Die 141 may also include other circuits that are not shown in FIG. 3 for simplicity of the drawing. Controller 40 and device or integrated circuit 140 are formed on die 141 by semiconductor manufacturing techniques that are well known to those skilled in the art.

25 In view of all of the above, it is evident that a novel device and method is disclosed. Included, among other features, is forming a power supply controller to enable the power switch during one valley value of a plurality of valley values responsively to a value of the
30 sense signal that is representative of an output voltage controlled by the power supply controller, or responsively to a range of values of the sense signal. Using one valley value for a range of values of the sense signal more accurately selects the proper time to enable the
35 switch transistor. It also utilizes less complex

circuitry than other methods of enabling the switch thereby lowering the costs.

For clarity of the explanation, the operation of the preferred embodiment is explained, however, it is evident
5 that many alternatives and variations will be apparent to those skilled in the semiconductor arts. For example, various circuits and methods may be used to form the range of values of the feedback signal in addition to the particular implementation illustrated by circuit 67.
10 Additionally, other circuits may be used to detect and count the valley values as long as they accurately detect the minimum value of the valley as accomplished by detector 59. Although transistor 33 and the current sense element of resistor 35 are illustrated to be external to
15 controller, transistor 33 and a current sense element may be formed as a part of controller 40. The word "connected" is used throughout for clarity of the description, however, it is intended to have the same meaning as the word "coupled". Accordingly, "connected"
20 should be interpreted as including either a direct connection or an indirect connection. Although the subject matter of the invention is described using an exemplary embodiment of a buck power supply controller, the invention is applicable to other power supply
25 configurations.

CLAIMS

1. A switching power supply controller comprising:
a first output configured to control a switch current
5 through both a switch and an inductor in order to regulate
an output voltage to a desired value wherein the switching
power supply controller is configured to form a switching
drive signal in order to enable and disable the switch
responsively to the switching drive signal and wherein
10 disabling the switch creates oscillations of a switch
voltage across the switch, the oscillations forming a
plurality of peak values and a plurality of valley values
of the switch voltage;
a first input configured to receive a sense signal
15 that is representative of a value of the output voltage;
a detector configured to detect the plurality of
valley values and form a plurality of valley detection
signals responsively to the plurality of valley values
wherein a first valley detection signal is representative
20 of detecting a first valley value of the plurality of
valley values and a second valley detection signal is
representative of detecting a second valley value of the
plurality of valley values that is different from the
first valley value; and
25 a first circuit configured to use a first value of
the sense signal and the first valley detection signal to
selectively enable the switch during the first valley
value that occurs during a first switching cycle of the
switching drive signal, the first circuit configured to
30 selectively enable the switch during the first valley
value responsively to a second value of the sense signal
and the first valley detection signal during a second
switching cycle of the switching drive signal which is
different from the first switching cycle, the second value
35 of the sense signal being within a first range around the
first value of the sense signal.

2. The switching power supply controller of claim 1 wherein the first circuit is configured to selectively enable the switch during the second valley value responsively to a third value of the sense signal and the second valley detection signal during a third switching cycle of the switching drive signal, the third value of the sense signal being outside the first range around the first value.

3. The switching power supply controller of claim 1 wherein the first circuit includes a plurality of comparators coupled to receive the sense signal and each comparator coupled to receive a different valley detection signal of the plurality of valley detection signals wherein successive comparators of the plurality of comparators are coupled to receive successively larger values of a reference voltage.

4. The switching power supply controller of claim 3 wherein a first comparator of the plurality of comparators is coupled to receive a first reference voltage and the first valley detection signal and form a first output signal, a second comparator of the plurality of comparators is coupled to receive a second reference voltage the second valley detection signal and form a second output signal wherein the first reference voltage is greater than the second reference voltage, and wherein the first circuit is configured to inhibit using the second output to selectively enable the switch if the first output is asserted.

5. The switching power supply controller of claim 4 wherein the first circuit includes a first AND gate having a first input coupled to receive the first output signal from the first comparator, a second input coupled to receive the first valley detection signal, and an output

coupled to cause an assertion of the switching drive signal;

5 a first inverter having an input coupled to receive the first output signal from the first comparator and having an output;

a second AND gate having a first input coupled to receive the second output signal from the second comparator, a second input coupled to the output of the first inverter, and an output; and

10 a third AND gate having a first input coupled to the output of the second AND gate, a second input coupled to receive the second valley detection signal, and an output coupled to cause an assertion of the switching drive signal.

15

6. The switching power supply controller of claim 1 wherein the switching power supply controller includes a second input coupled to receive a switch signal that is representative of the switch voltage and wherein the
20 detector includes a counter coupled to count successive occurrences of the plurality of valley values and form the plurality of valley detection signals.

7. The switching power supply controller of claim 6
25 wherein the detector includes a valley comparator coupled to receive the switch signal and form a clock signal to clock the counter responsively to any of the plurality of valley values.

30 8. The switching power supply controller of claim 1 further including a voltage controlled oscillator coupled to selectively control a frequency of the switching drive signal responsively to the first circuit wherein the first circuit is configured to inhibit the voltage controlled
35 oscillator from controlling the switching drive signal until the output voltage is less than a first value that

is representative of a minimum power consumption by a load that is coupled to receive the output voltage.

9. A method of forming a power supply controller
5 comprising:

configuring the power supply controller to form a plurality of switching cycles to control a switch current through a switch in order to regulate an output voltage to a desired value wherein disabling the switch during a
10 switching cycle of the plurality of switching cycles creates oscillations of a switch voltage across the switch, the oscillations forming a plurality of valley values of the switch voltage;

configuring a first circuit of the power supply
15 controller to detect the plurality of valley values and responsively form a plurality of valley detection signals;

configuring a second circuit of the power supply controller to form a plurality of value ranges around a plurality of values of a sense signal that is
20 representative of the output voltage wherein a different value range of the plurality of value ranges is formed around different values of the plurality of values of the sense signal;

configuring the second circuit to select one valley
25 detection signal of the plurality of valley detection signals responsively to one value range of the plurality of value ranges; and

configuring the power supply controller to enable the switch responsively to the selected one of the plurality
30 of valley detection signals.

10. The method of claim 9 wherein configuring the first circuit of the power supply controller to detect the plurality of valley values and responsively form the
35 plurality of valley detection signals includes configuring the first circuit to detect successive valley values after

disabling the switch during a first switching cycle of the plurality of switching cycles.

11. The method of claim 9 wherein configuring the
5 second circuit to select one valley detection signal
includes configuring the second circuit to form a first
range of values around a first value of the sense signal
and to select a first valley detection signal of the
plurality of valley detection signals responsively to the
10 sense signal being within the first range of values.

12. The method of claim 11 further including
configuring the second circuit to form a second range of
values around a second value of the sense signal and to
15 select a second valley detection signal of the plurality
of valley detection signals responsively to the sense
signal being within the second range of values.

13. The method of claim 12 further including
20 configuring the second circuit to form a third range of
values around a third value of the sense signal and to
select a third valley detection signal of the plurality of
valley detection signals responsively to the sense signal
being within the third range of values.

25
14. The method of claim 9 further including
configuring the power supply controller to control the
switch responsively to a frequency of a VCO circuit for
values of the sense signal that are less than the
30 plurality of value ranges of the sense signal and not to
enable the switch responsively to the selected one of the
plurality of valley detection signals.

15. The method of claim 9 wherein configuring the
35 first circuit of the power supply controller to detect the
plurality of valley values and responsively form the

plurality of valley detection signals includes configuring the first circuit to form a separate control signal for each valley value that is detected.

5 16. A method of forming a power supply controller comprising:

 configuring the power supply controller to form a plurality of switching cycles to control a switch current through a switch in order to regulate an output voltage to
10 a desired value wherein disabling the switch during a switching cycle of the plurality of switching cycles creates oscillations of a switch voltage across the switch, the oscillations forming a plurality of valley values of the switch voltage;

15 configuring the power supply controller to use a sense signal that is representative of the output voltage; and

 configuring the power supply controller to enable the switch during one valley value of the plurality of valley
20 values responsively to a value of the sense signal.

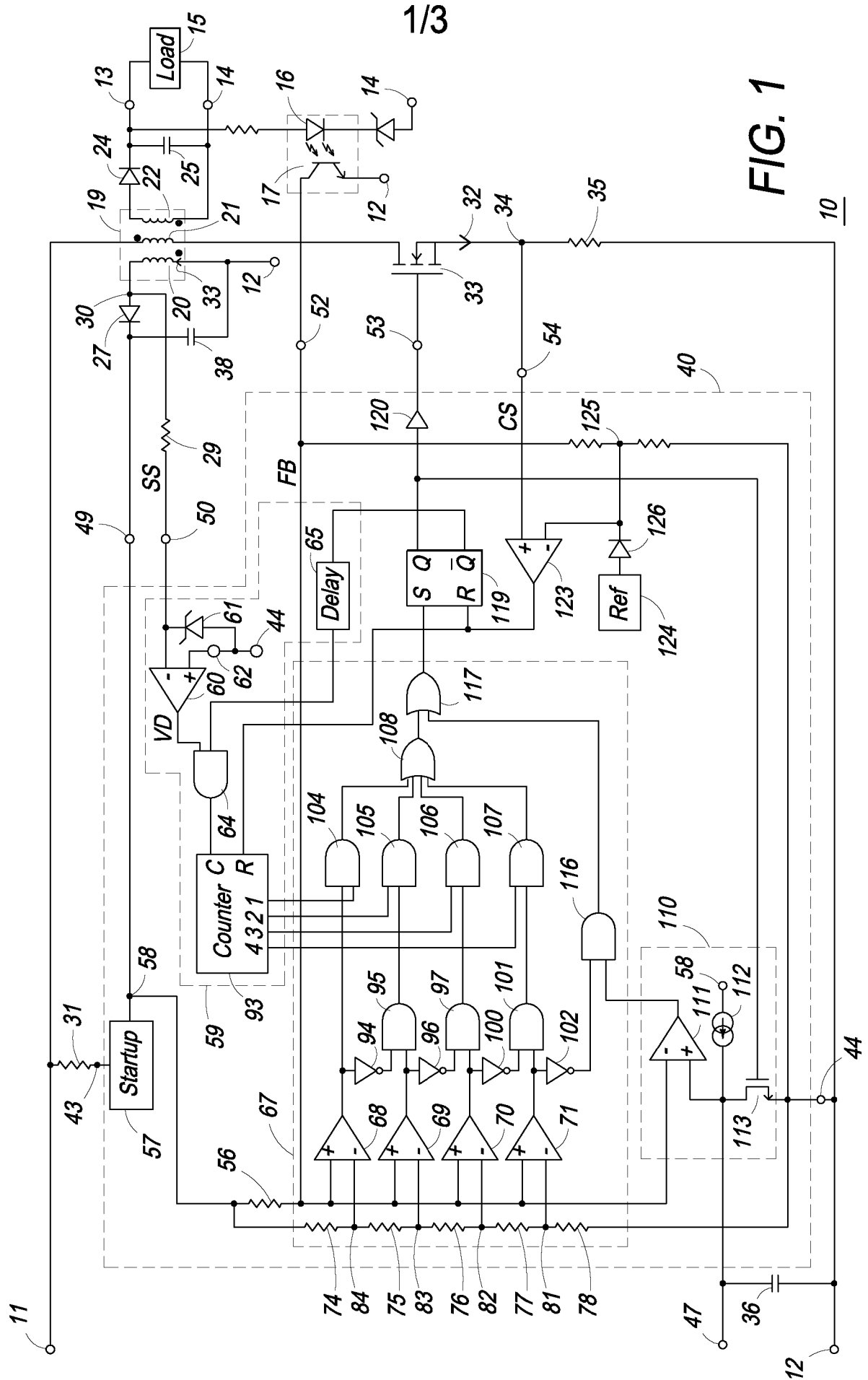
 17. The method of claim 16 wherein configuring the power supply controller to use the sense signal that is representative of the output voltage includes configuring
25 the power supply controller to form a plurality of value ranges around a plurality of values of the sense signal wherein a different value range of the plurality of value ranges is formed around different values of the plurality of values of the sense signal.

30

 18. The method of claim 17 wherein configuring the power supply controller to enable the switch during one valley value of the plurality of valley values
 responsively to the value of the sense signal includes
35 configuring the power supply controller to select the one valley value responsively to one value range of the plurality of value ranges.

19. The method of claim 16 wherein configuring the power supply controller to enable the switch during one valley value of the plurality of valley values includes
5 configuring the power supply controller to form a plurality of valley detection signals wherein a different valley detection signal is asserted for different valley values of the plurality of valley values and configuring the power supply controller to use a first valley
10 detection signal of the plurality of valley detection signals to select the one valley value.

20. The method of claim 19 wherein configuring the power supply controller to use the first valley detection
15 signal of the plurality of valley detection signals to select the one valley value includes configuring the power supply controller to use the value of the sense signal to select the first valley detection signal.



2/3

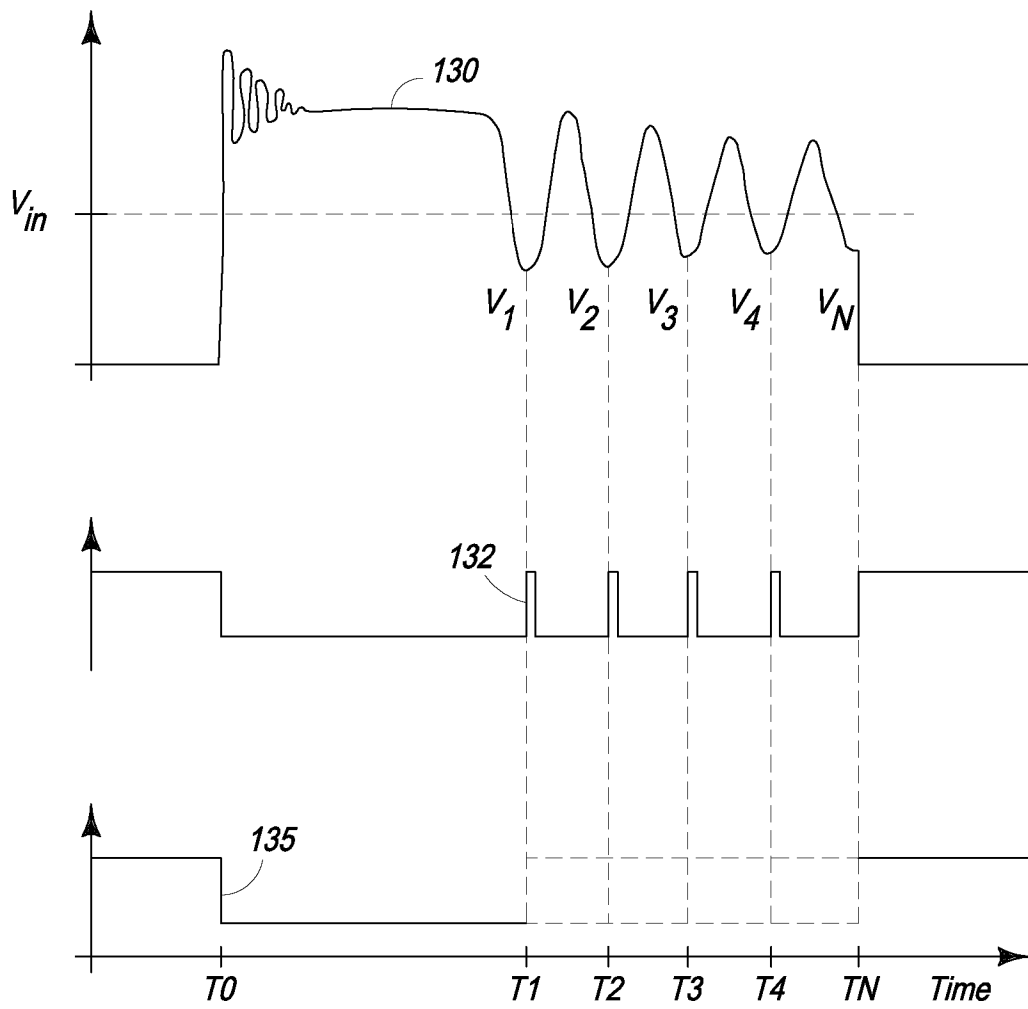


FIG. 2

3/3

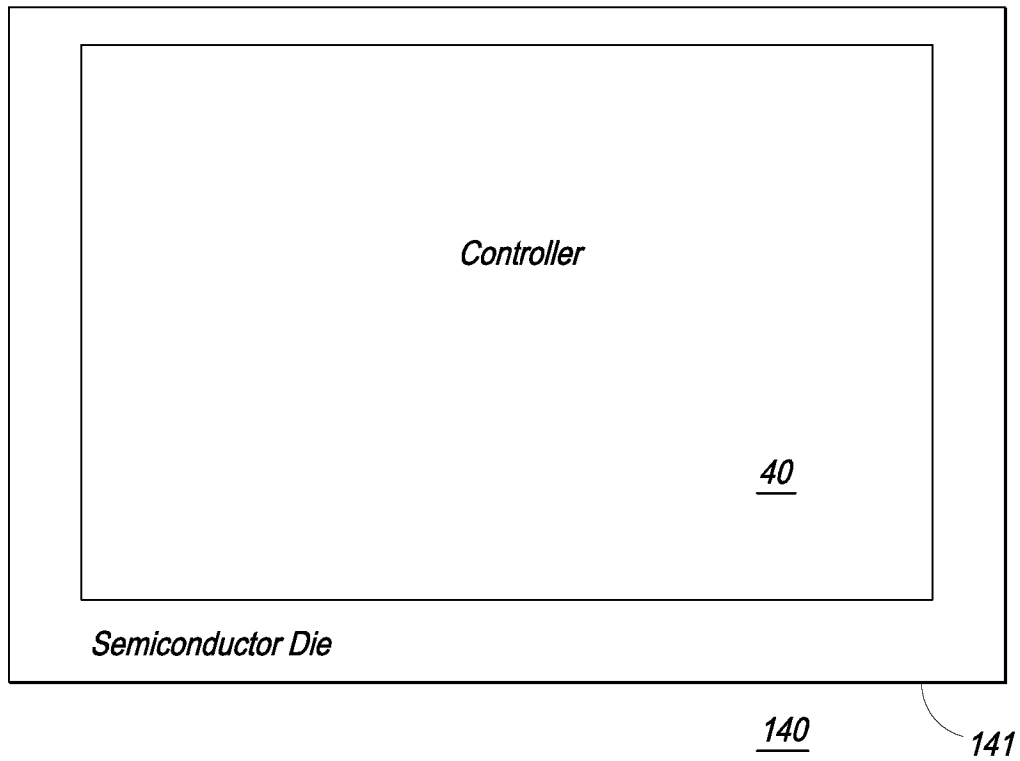


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/083588

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/121258 A1 (YOSHIKI HACHIYA) 31 May 2007 (2007-05-31) abstract figure 4 paragraphs [0004], [0014], [0015], [0018], [0028], [0030] -----	1-20
X	US 7 248 487 B1 (MAHESH DEVARAHANDI INDIKE DE SILVA ET AL.) 24 July 2007 (2007-07-24) abstract figure 3 column 2, line 30 - line 33 column 5, line 18 - line 33 column 6, line 36 - line 44 column 7, line 9 - line 20 column 7, line 35 - column 8, line 9 ----- -/--	1-20

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"Z" document member of the same patent family

Date of the actual completion of the international search

9 February 2009

Date of mailing of the international search report

18/02/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Lund, Michael

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/083588

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/74221 A (KONINKLIJKE PHILIPS ELECTRONICS) 7 December 2000 (2000-12-07) abstract page 2, line 21 - line 25 page 6, line 7 - line 12 page 6, line 22 - line 25; figure 5 -----	1-20
A	US 2002/085394 A1 (DEMETRI GIANNOPOULOS ET AL.) 4 July 2002 (2002-07-04) figures 1,4 paragraphs [0004] - [0006] -----	1-20
A	GB 2 421 594 A (CAMBRIDGE SEMICONDUCTOR LIMITED) 28 June 2006 (2006-06-28) abstract figures 5,20,28 page 27, line 31 - page 28, line 5 -----	1-20
A	US 2006/215424 A1 (SHINJI ASO ET AL.) 28 September 2006 (2006-09-28) paragraphs [0008], [0013], [0018]; figure 3 -----	1-20
A	US 2005/218942 A1 (TETSUJI YAMASHITA) 6 October 2005 (2005-10-06) figure 6 paragraph [0104] -----	1-20

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: -

The physical features of claim 1 relates to a power supply controller circuit, typically used for a flyback type converter, of the kind that is often referred to in the prior art as using quasi-resonant operation. Though reference signs are missing, these physical features appear in general to be clear.

Further, claim 1 includes some functional features that are concerned with how "valleys" are detected and used in the control of the power switch. The mere detection of valleys is understandable from claim 1, but is also known from the prior art. Claim 1 further elaborates on how more values detected during different "valleys" are combined. This part of claim 1 appear not to be clear. In particular the part of claim 1 reading: "....

configured to selectively enable the switch during the first valley value responsively to a second value of the sense signal and the first valley detection signal during a second switching cycle of the switching drive signal which is different from the first switching cycle, the second value of the sense signal being within a first range around the first value of the sense signal...." seems to have no unambiguous interpretation. As this may be the part of claim that is novel compared with the prior art, it is paramount that it is clear. Further, it is not clear if "...the first valley detection signal.." is a signal relating to the first valley observed after that the power switch is turned OFF or it is a detection signal that relates to a "valley" that is defined as "the first". This ambiguity leaves both options possible.

An incomplete search has been carried out based on the tangible, physical features of claim 1. A detailed search can only be carried out when features that are tangible and clearly different from the prior art cited are included in claim 1.

Eventual lacking unity of invention can only judged upon when independent claim 1 is clear.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2), should the problems which led to the Article 17(2)PCT declaration be overcome.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/083588

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/083588

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007121258 A1	31-05-2007	CN 1996732 A	11-07-2007
US 7248487 B1	24-07-2007	NONE	
WO 0074221 A	07-12-2000	JP 2003524359 T	12-08-2003
		US 6256210 B1	03-07-2001
US 2002085394 A1	04-07-2002	AT 313872 T	15-01-2006
		CN 1528043 A	08-09-2004
		EP 1428308 A2	16-06-2004
		WO 02054570 A2	11-07-2002
		JP 2004517595 T	10-06-2004
GB 2421594 A	28-06-2006	NONE	
US 2006215424 A1	28-09-2006	JP 2006262566 A	28-09-2006
		KR 20060100256 A	20-09-2006
US 2005218942 A1	06-10-2005	CN 1677825 A	05-10-2005
		JP 4127399 B2	30-07-2008
		JP 2005287260 A	13-10-2005
		KR 20060044988 A	16-05-2006