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(54) System and method for analog-to-digital conversion

(57) A system for ccnverting an analog signal to a digital signal may include a plurality of converter stages. One of the converter stages may include a multiplying digital-to-analog converter (MDAC) and an analog-to-digital subconverter (ADSC). The MDAC may be configured to (i) receive from a previous stage a first residue analog signal and a first idealized digital signal representing a first portion of the digital signal and corresponding to the first residue analog signal; (ii) convert the first idealized digital signal to an idealized analog signal; and (iii) output a second residue analog signal based on the difference between the first residue analog signal and the idealized analog signal. The ADSC may be configured to convert the second residue analog signal into a second idealized digital signal representing a second portion of the digital signal and corresponding to the second residue analog signal, the ADSC comprising a sloping analog-to-digital converter.

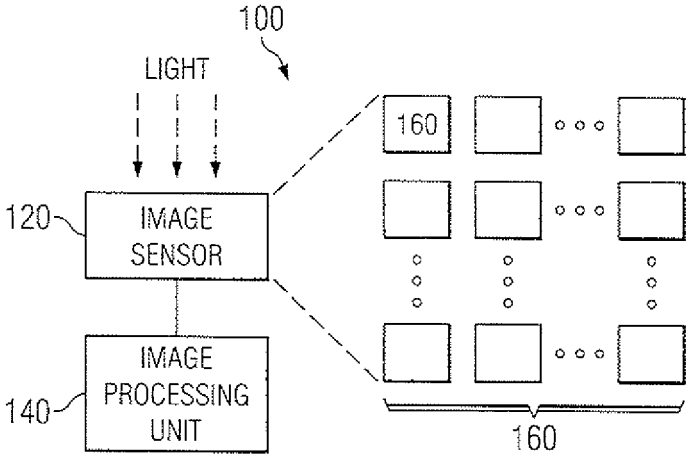

FIG. 1

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Description

TECHNICAL FIELD

[0001] This disclosure relates in general to conversion of analog signals to digital signals and more particularly to an analog-to-digital conversion system and method utilizing a pipelined single-slope analog-to-digital converter.

BACKGROUND

[0002] Many devices, including image sensing circuits, often require many channels of image data to be converted from analog signals to digital signals via analog-to-digital conversion. Such analog-to-digital converters (ADCs) may be located on an integrated circuit (IC) external to image sensing circuit, or such ADCs may be integrated on the same integrated circuit as the image sensing circuitry. Integration of ADCs on the same integrated circuit as the image sensing circuitry is often utilized as the number of channels (e.g. pixels) increase due to interconnect noise and transmission line loss associated with communicating signals to external ADC circuits. However, approaches employing traditional ADCs integrated on the same integrated circuit as imaging sensing circuitry often consume large amounts of power and area for large resolutions.

SUMMARY OF THE DISCLOSURE

[0003] According to one embodiment, a system for converting an analog signal to a digital signal may include a plurality of converter stages. One or more of the converter stages may include a multiplying digital-to-analog converter and an analog-to-digital subconverter. The multiplying digital-to-analog converter may be configured to (i) receive from a previous stage a first residue analog signal and a first idealized digital signal representing a first portion of the digital signal and corresponding to the fist residue analog signal; (ii) convert the first idealized digital signal to an idealized analog signal; and (iii) output a second residue analog signal based on the difference between the first residue analog signal and the idealized analog signal. The analog-to-digital subconverter may be configured to convert the second residue analog signal into a second idealized digital signal representing a second portion of the digital signal and corresponding to the second residue analog signal, the analog-to-digital subconverter comprising a sloping analog-to-digital converter.

[0004] Technical advantages of certain embodiments may including providing an analog-to-digital converter with low power and low space requirements, while also maintaining adequate conversion speed.

[0005] Other technical advantages will be readily apparent to one skilled in the art from the following figures, descriptions, and claims. Moreover, while specific advantages have been enumerated above, various embodiments may include all, some, or none of the enumerated advantages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] For a more complete understanding of the present disclosure and its advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 depicts a block diagram illustrating an example image sensing device that may be used to capture images, in accordance with certain embodiments of the present disclosure;
FIGURE 2 depicts a block diagram illustrating an example pipelined analog-to-digital converter that may be used to convert analog signals into digital signals, in accordance with certain embodiments of the present disclosure; and
FIGURE 3 depicts a block diagram illustrating an example sloping analog-to-digital subconverter that may be used in connection with the analog-to-digital converter depicted in FIGURE 2, in accordance with certain embodiments of the present disclosure.

DETAILED DESCRIPTION OE THE DISCLOSURE

[0007] Embodiments of the present disclosure and its advantages are best understood by referring to FIGURES 1 through 3 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

[0008] FIGURE 1 is a block diagram illustrating an image capture device 100 that may be used to capture images. For example, device 100 may be a digital camera, video camera, or any other suitable photographic and/or image capturing device. Image capture device 100 may include image sensor 120 and image processing unit 140. Image sensor 120 may be an active pixel sensor (APS) or any other suitable light sensing device that can capture images. Image sensor 120 may include, for example, a diode, a charge-coupled device (CCD), or any other photovoltaic detector or transducer. Image processing unit 140 may be a combination of hardware, software, or firmware that is operable to receive signal information from image sensor 120 and convert the signal information into an electronic image. For example, image processing unit 140 may include an analog-to-digital converter (ADC) to convert analog signals received by image sensor 120 to corresponding digital signals that may be further processed by image processing unit 140 and/or another processing device.

[0009] Image sensor 120 may include an array of unit cells 160. Unit cells 160 may accumulate charge proportional to the light intensity at the location of a coupled detector and may correspond to a pixel in the captured electronic image. Unit cell 160 may temporarily store the

accumulated charge for use by processing unit 140 to create an image.

[0010] FIGURE 2 depicts a block diagram illustrating an example pipelined analog-to-digital converter (ADC) 200 that may be used to convert analog signals (e.g., current, voltage, or electric charge) into digital signals, in accordance with certain embodiments of the present disclosure. While ADC 200 may be used for any suitable application, in certain embodiments, ADC 200 may be used in an imaging system (e.g., image capture device 100) in order to convert analog signals representing an image into corresponding digital signals. In the same or alternative embodiments, ADC 200 may be an integral part of an image processing unit (e.g., image processing unit 140) or similar image processing device.

[0011] As shown in FIGURE 2, ADC 200 may include one or more analog-to-digital subconverters (ADSCs) 202, one or more multiplying digital-to-analog converters (MDACs) 204, and one or more sample-and-hold circuits 214. In certain embodiments, some or all of the components of ADC 200 may form a single integrated circuit including such components. Each ADSC 202 may include any system, device, or apparatus configured to convert an analog signal to a discrete digital number of a particular bit length. In certain embodiments, one or more of ADSCs 202 may be a single-slope ADC, such as that depicted in FIGURE 3, for example.

[0012] Each MDAC 204 may include any system, device, or apparatus configured to convert a digital signal into a first analog signal, subtract the first analog signal from a second analog signal, and amplify the resulting difference between the second analog signal and the first analog signal. As shown in FIGURE 2, each MDAC 204 may include a digital-to-analog converter (DAC) 208, a summer 210, a gain amplifier 212, and a sample-and-hold (S/H) circuit 214.

[0013] Each DAC 208 may be any suitable device, system, or apparatus configured to convert a digital number to an analog signal (e.g., current, voltage or electric charge).

[0014] Each summer 210 may be any suitable device, system, or apparatus configured to receive two or more analog signals (e.g., current, voltage, or electric charge) and output another analog signal representative of the sum and/or difference of the input signals. In certain embodiments, one or more of summers 210 may include a summing amplifier.

[0015] Each gain amplifier 212 may be any suitable device, system, or apparatus configured to receive an input signal (e.g., current or voltage) and amplify the input signal by a gain to produce an output signal that is a multiple of the input signal. In certain embodiments, one or more of gain amplifiers 212 may include a noninverting amplifier, an inverting amplifier, or any combination thereof.

[0016] Each S/H circuit 214 may be any suitable device, system, or apparatus configured to receive a continuous analog signal (e.g., a time-varying current or voltage) and hold the analog signal steady for a specified period of time to allow an ADC or other following system to perform an operation on the held analog signal. In certain embodiments, S/H circuit 214 may include a capacitor to store an analog voltage, and may also include an electronic switch or gate to alternately connect and disconnect the capacitor from the analog input to be sampled and held.

[0017] In certain embodiments, DAC 208, summer 210, gain amplifier 212, and S/H circuit 214 of each MDAC 204 may be implemented in a single circuit, such as a solid state switched-capacitor circuit or a complimentary metal-on-silicon (CMOS) DAC, for example.

[0018] In operation, ADC 200 may convert an analog input signal received at an input of S/H 214a into a digital output representative of the analog input signal over a number of pipeline stages. To illustrate, in Stage 1 of ADC 200, an analog input signal may be sampled and held by S/H 214a. The held analog signal may be output to MDAC 204b of Stage 2, to be used as described in greater detail below. The held analog signal may be output to ADSC 202a, in which the most significant bits of the digital signal corresponding to the analog input signal may be computed. For example, if ASDC 202a has a resolution of four bits, the four most significant bits of the digital signal corresponding to the analog input signal may be computed and output by ASDC 202a. The digital signal corresponding to the most significant bits may then be output to MDAC 204b of Stage 2.

[0019] At Stage 2, DAC 208b of MDAC 204b may convert the output of ADSC 202a (the most significant bits of the digital output signal of ADC 200) to an analog signal, producing an idealized signal that is an approximation of the analog input signal to Stage 1. Summer 210b may subtract this idealized signal from the actual sampled-and-held analog signal from Stage 1, producing a residue analog signal equal to the difference between the actual analog signal and the idealized signal, such that the residue analog signal is less than the analog signal representation of one quantization level of ADSC 202a of Stage 1. Gain amplifier 212b may amplify the residual analog signal, and the amplified residual analog signal may be output to each of Stage 3 and ADSC 202b of Stage 2.

[0020] ADSC 202b may convert the Stage 2 amplified residual analog signal to a digital signal representative of the second most significant bits of the digital signal corresponding to the original analog input signal. For example, if each ADSC has a resolution of four bits, the combined output of ADSC 202a and ADSC 202b may represent the eight most significant bits of the digital signal corresponding to the original analog input signal. The digital signal output by ADSC 202b may be output to Stage 3.

[0021] Much like Stage 2, each additional stage of ADC 200 may compute a residual analog signal equal to the residual analog signal of the previous stage minus an idealized analog signal based on the digital output of the

previous stage. Such residual analog signal may then be amplified, sampled and held, output to the next stage of ADC 200, and used such that the next most significant bits of the digital output signal of ADC 200 may be computed based on the amplified residual analog signal. Such process may be repeated for each of N stages, until finally Stage N produces the least significant bits of the digital output signal of ADC 200. Accordingly, the resolution (R) of ADC 200 is a function of the number of stages (N) and the resolution of each ADSC 202a (r) (e.g., R = N x r).

[0022] FIGURE 3 depicts a block diagram illustrating an example sloping ADSC 300, in accordance with certain embodiments of the present disclosure. In certain embodiments, one or more of ADSCs 202 may include ADSC 300. As shown in FIGURE 3, ADSC 300 may include an analog input 302, an analog ramp 304, a comparator 306, a digital counter 308, and a digital output 310. Analog input 302 may include any interface configured to receive an analog signal (e.g., voltage or current). Similarly, digital output 310 may include any interface configured to communicate a digital signal.

[0023] Analog ramp 304 may include any device, system or apparatus that provides an increasing or decreasing magnitude of analog signal during the sampling of each analog input. For example, analog ramp 304 may, during each sampling cycle of ADSC 300, linearly increase from approximately zero, up to a maximum magnitude.

[0024] Comparator 306 may include any device, system or apparatus that compares two analog signals (e.g., voltages or currents) at its inputs and switches its output between two values to indicate which is larger. For example, comparator may output a logic zero if the analog signal of analog input 302 is of a lower magnitude than the magnitude of the output of analog ramp 304, and may output a logic one otherwise. Accordingly, comparator 306 may be thought of as a one-bit ADC.

[0025] Digital counter 308 may include any device, system or apparatus that provides an increasing or decreasing magnitude of digital signal during the sampling of each analog input. For example, digital counter 308 may, during each sampling cycle of ADSC 300, count from approximately zero (e.g., 0000 in a four-bit counter), up to a maximum magnitude (e.g., 1111 in a four-bit counter). In some embodiments, digital counter 308 cease counting during a particular sampling cycle of ADSC 300 if it receives a particular value at its input (e.g., digital counter 308 may count if its input value is a logic zero, and may cease counting if its input value switches to a logic one).

[0026] In operation, when a new analog sample is placed on analog input 302, analog ramp 304 may begin to ramp (e.g., from zero) and digital counter 308 may begin to count (e.g., from zero). When the magnitude of the signal outputted by analog ramp 304 exceeds the magnitude of the signal on analog input 302, the output value of comparator 306 may flip (e.g., from logic zero to logic one, or vice versa) and digital counter 308 may cease counting. Accordingly, the value of digital counter when it ceases counting may be a digital representation of the magnitude of the signal on analog input 302.

[0027] As discussed above, sloping ADSCs identical or similar to the sloping ADSC 300 of FIGURE 3 may be used as ADSCs 202 in ADC 200. The benefits of using a sloping ADSC in the architecture of ADC 200 is that sloping ASDCs require only a relatively small comparator and a relatively small digital counter within each stage of ADC in order to perform conversion. Another advantage is that a ramp circuit (e.g., analog ramp 304) may be shared among all ADSCs 202 in ADC 200 (and even amongst multiple ADCs). By pipelining into numerous stages each using a sloping ADSC, a desirable tradeoff between the size advantages and the speed disadvantages of sloping ADCs may be realized. For example, a 12-bit pipeline ADC including four three-bit sloping stages would ideally require $2^3 = 8$ clock cycles as compared to a noun-pipelined 12-bit sloping ADC requiring $2^{12} = 4096$ clock cycles. In addition, a plurality of sloping stages may consume less space and less power than traditional approaches to analog-to-digital conversion, such as flash or successive approximation approaches.

[0028] Although the embodiments in the disclosure have been described in detail, numerous changes, substitutions, variations, alterations, and modifications may be ascertained by those skilled in the art. For example, image sensor 120 may include any type of sensor including an APS, a separate detector, a separate detector material, or an alternate transducer other than an optical detector. Additionally or alternatively, while the disclosure is described predominantly in reference to visible detectors, the embodiments disclosed herein may be utilized with many types of detectors including, but not limited to, visible, infrared, ultraviolet, x-ray, or other radiation detectors. It is intended that the present disclosure encompass all such changes, substitutions, variations, alterations and modifications as falling within the spirit and scope of the appended claims.

[0029] It will be appreciated that optional features of embodiments of the invention can be used together in any number and in any combination. This includes, but is not limited to, using the features of dependent claims in any number, and in any combination.

Claims

1. A converter stage for converting an analog signal to a digital signal, comprising:

   a multiplying digital-to-analog converter (204) configured to:

   receive a first residue analog signal and a first idealized digital signal representing a first portion of the digital signal and corre-

sponding to the first residue analog signal;
convert the first idealized digital 1 signal to an idealized analog signal; and
output a second residue analog signal based on the difference between the first residue analog signal and the idealized analog signal; and

an analog-to-digital subconverter (202) configured to convert the second residue analog signal into a second idealized digital signal representing a second portion of the digital signal and corresponding to the second residue analog signal, the analog-to-digital subconverter (202) comprising a sloping analog-to-digital converter (300).

2. A converter stage according to Claim 1, the multiplying digital-to-analog converter (204) further configured to:

amplify the difference between the first residue analog signal and the idealized analog signal;
sample and hold the amplified difference; and
output the sampled and held amplified difference as the second residue analog signal.

3. A converter stage according to Claim 1, the sloping analog-to-digital subconverter (300) comprising a single-slope analog-to-digital converter.

4. A converter stage according to any preceding claim, the sloping analog-to-digital subconverter (300) comprising:

an analog ramp (304) configured to output a varying analog signal during a sampling cycle of the sloping analog-to-digital subconverter (300);
a comparator (306) configured to compare the varying analog signal to the second residue analog signal; and
a digital counter (308) configured to output a varying digital signal during the sampling cycle and to cease varying the digital counter based on the comparison made by the comparator (306), wherein:

the value of the digital counter (308) at the time the digital counter (308) ceases varying is the second idealized signal.

5. A converter stage according to any preceding claim, wherein the first residue analog signal is a voltage, current, or electrical charge.

6. A converter stage according to any preceding claim, wherein the second residue analog signal is a voltage, current, or electrical charge.

7. A system (100) for image sensing comprising:

a detector (120) configured to generate an electric charge in proportion to a detected light intensity;
a unit cell (160) coupled to the detector and configured to receive the electric charge; and
an image processing unit (140) electrically coupled to the detector (120) and configured to read an electrical analog signal of the unit cell (160) corresponding to the detected light intensity and comprising an analog-to-digital converter (200) configured to convert the electrical analog signal to a digital signal corresponding to the detected light intensity, the analog-to-digital converter (200) including a plurality of converter stages, wherein at least one of the converter stages is a converter stage according to any of Claims 1-7.

8. A system according to Claim 7, wherein the electrical analog signal is a voltage, current, or electrical charge.

9. A method for converting an analog electrical signal to a digital signal comprising:

sampling the electrical analog signal;
converting with a first sloping analog-to-digital subconverter (300) the electrical analog signal to a first idealized digital signal of a first bit length, the first idealized digital signal corresponding to the most significant bits of the digital signal;
converting the first idealized digital signal to a first idealized analog signal;
sampling a first residue analog signal based on the difference between the electrical analog signal and the first idealized analog signal; and
converting with a second sloping analog-to-digital subconverter (300) the first residue analog signal to a second idealized digital signal of a second bit length, the second idealized digital signal corresponding to the most significant bits of the digital signal remaining after the most significant bits of the digital signal corresponding to the first bit length.

10. A method according to Claim 9, comprising:

converting the second idealized digital signal to a second idealized analog signal;
sampling a second residue analog signal based on the difference between the first residue analog signal and the second idealized analog signal; and
converting with a third sloping analog-to-digital subconverter (300) the second residue analog signal to a third idealized digital signal of a third

bit length, the third idealized digital signal corresponding to the most significant bits of the digital signal remaining after the most significant bits of the digital signal corresponding to the first bit length and the most significant bits of the digital signal corresponding to the second bit length.

11. A method according to Claim 10, wherein the first bit length, second bit length, and third bit length are equal.

12. A method according to Claim 9, wherein the first bit length and second bit length are equal.

13. A method according to Claim 9, wherein the first sloping analog-to-digital subconverter (300) is substantially identical to the second sloping analog-to-digital subconverter (300).

14. A method according to Claim 9, wherein the first residue analog signal is a voltage, current, or electrical charge.

15. A method according to Claim 9, wherein the second residue analog signal is a voltage, current, or electrical charge.

16. A method according to Claim 9, wherein the electrical analog signal is a voltage, current, or electrical charge.

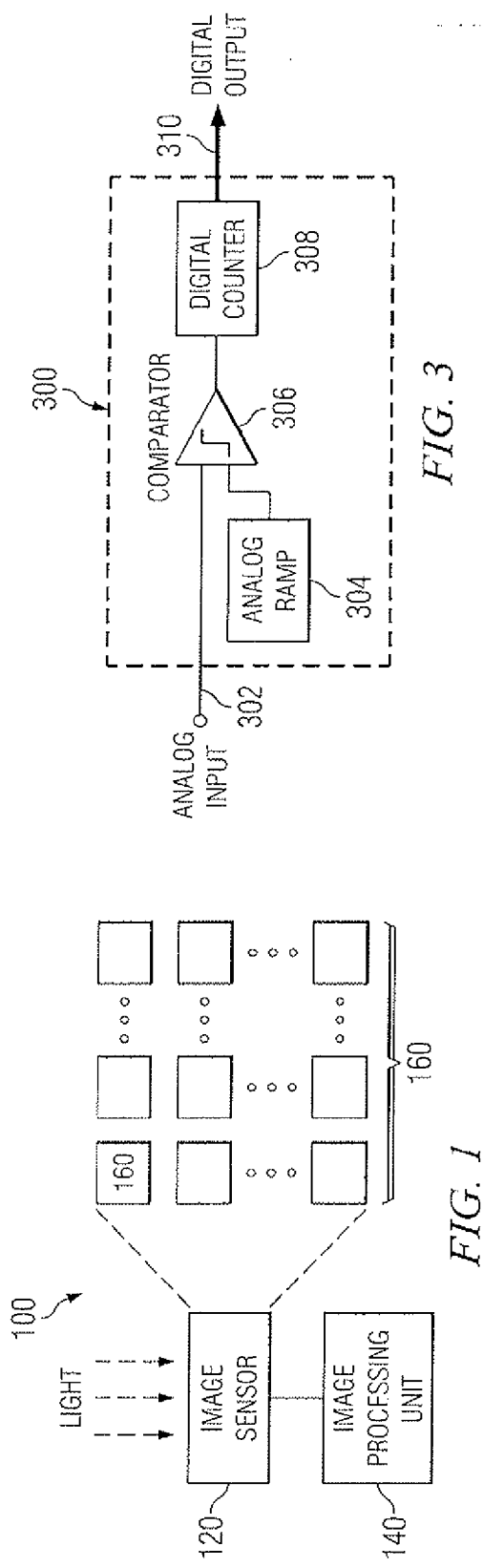

FIG. 1

FIG. 3

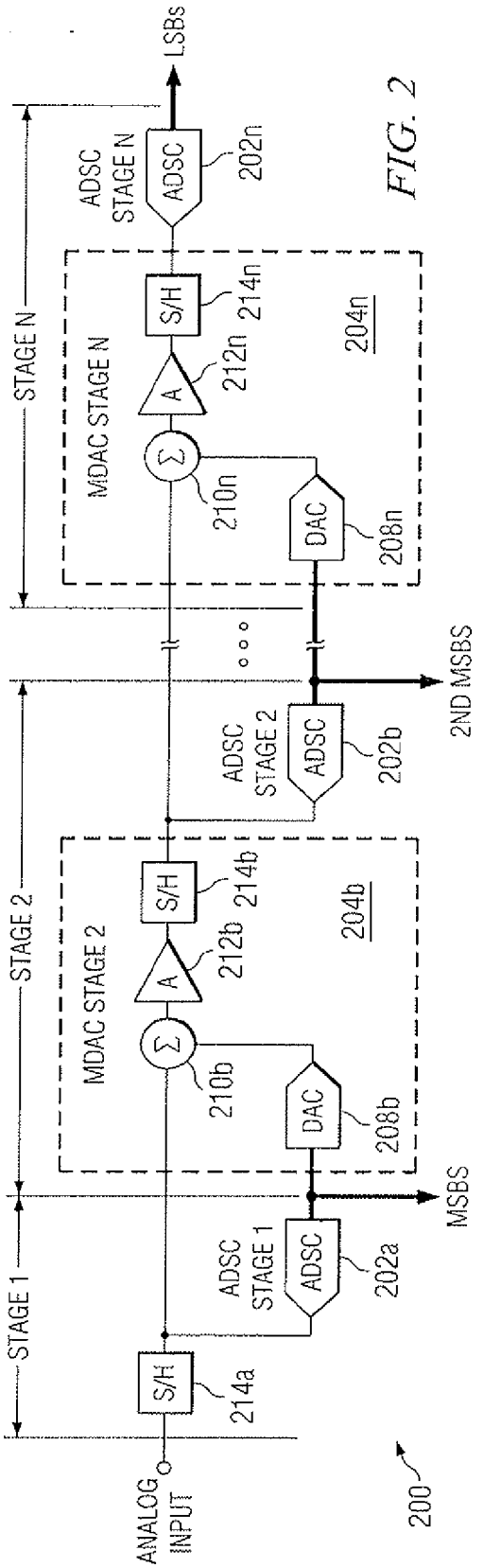

FIG. 2