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- (71) Applicant (for all designated States except US): INFINEON TECHNOLOGIES AG [DE/DE]; St.-Martin-Str. 53, 81669 München (DE).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): VERHOEVEN, Martin [NL/DE]; Am Jacobstein 30, 01445 Radebeul (DE).
- (74) Agent: EPPING HERMANN FISCHER PATENTANWALTSGESELLSCHAFT MBH; Ridlerstrasse 55, 80339 München (DE).
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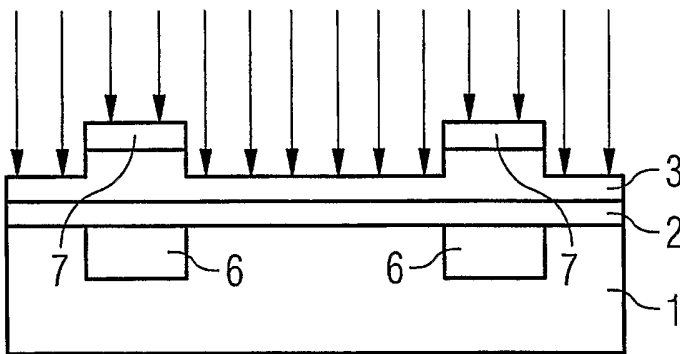
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(54) Title: METHOD FOR PRODUCTION OF CHARGE-TRAPPING MEMORY CELLS



(57) Abstract: An oxide layer (2), a nitride layer (3), and a layer of amorphous silicon (4) are applied to a surface of a semiconductor substrate (1). A resist mask (5) is applied and implantations are performed to form doped regions (6) of source and drain and doped regions within the amorphous silicon layer. The resist mask and undoped parts of the amorphous silicon are removed to form a silicon mask (7). The silicon mask is applied to etch back the nitride layer (3). After a removal of the silicon mask (7), the nitride (3) is oxidized to form an

oxide-nitride-oxide layer sequence which is laterally restricted to the area above the source/drain regions (6).

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<b>B. FIELDS SEARCHED</b>				
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB				
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>				
<b>Category*</b>	<b>Citation of document, with indication, where appropriate, of the relevant passages</b>	<b>Relevant to claim No.</b>		
A	US 2004/197995 A1 (LEE YONG-KYU ET AL) 7 October 2004 (2004-10-07) paragraphs [0073] - [0133]; figures 5-8 -----	1-3		
A	EP 1 231 646 A (FUJITSU LIMITED) 14 August 2002 (2002-08-14) paragraphs [0027], [0039] - [0122]; figures 2-10 -----	1-3		
A	US 2002/149066 A1 (CHANG KENT KUOHUA ET AL) 17 October 2002 (2002-10-17) paragraphs [0006] - [0018]; figures 1-6 -----	1-3		
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.				
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Information on patent family members

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