Title: AUDIO SIGNAL SWITCHING

Abstract: A switching arrangement for a circuit, the switching arrangement comprising: a signal input ($V_{in}$); a signal output ($V_{out}$); a switching stage (30) that has a control input, the switching stage being operative, in response to a control signal applied to the control input changing between a first voltage level and a second voltage level, to change between a first state in which it causes a signal on the signal input to pass to the signal output and a second state in which the signal output is muted; and a control stage (24) that operates: in a steady mode to apply a steady signal to the control input of the switching stage at one or other of the first or the second voltage level to cause the switching arrangement to be maintained in its first or its second state as required; and in a switching mode to apply a switching signal that transitions between the first voltage level and the second voltage level to the control input of the switching stage to cause the switching arrangement to transition between its first and its second state.
The present invention relates to switching signals and particularly but not exclusively to switching analogue audio signals (e.g. in an audio circuit).

The switching of audio signals within a complex audio system is a familiar problem in analogue electronic design, with the instantaneous transition between “on” and “off” states acting to generate an audible transient at the instant of the transition due to convolution of the spectra of the audio signal and of the switching waveform implementing the transition. So-called “soft switching” – that is, switching audio signals in such a manner as not to generate audible transients, which sometimes are referred to by the onomatopoeic phase “click and pop” – is a required feature of many audio devices.

A complex analogue audio circuit may require soft switching to be implemented in many places within multiple signal paths. Where such a circuit is implemented within a highly integrated architecture, such as a silicon chip or integrated circuit, limitations within the architecture, or limitations imposed through the connectivity which can be achieved through packaging of such highly-integrated assemblies, may make the provision of individual, replicated soft switches inefficient or impracticable.

The present applicant has identified the need for a way of more efficiently implementing soft switching in a complex circuit in a highly integrated architecture.
In accordance with a first aspect of the present invention, there is provided a switching arrangement for a circuit (e.g. audio circuit), the switching arrangement comprising: a signal input (e.g. analogue signal input); a signal output (e.g. analogue signal output); a switching stage that has a control input, the switching stage being operative, in response to a control signal applied to the control input changing between a first voltage level and a second voltage level, to change between a first state in which it causes a signal on the signal input to pass to the signal output and a second state in which the signal output is muted; a control stage that operates: in a steady mode to apply a steady signal to the control input of the switching stage at one or other of the first or the second voltage level to cause the switching arrangement to be maintained in its first or its second state as required; and in a switching mode to apply a switching signal that transitions between the first voltage level and the second voltage level (e.g. in a monotonic manner) to the control input of the switching stage to cause the switching arrangement to transition between its first and its second state.

In this way, a switching arrangement is provided in which the function of maintaining the output of the switching arrangement in its steady state is separated from the function of transitioning the switching arrangements between its states, the latter being controlled by switching signal.

In one embodiment, the switching signal is a soft-switching signal that transitions between the first and the second voltage levels in a period of time that causes the switching stage to change state at a rate that is sufficiently slow as to prevent audible transients appearing on the signal output. For example, the switching signal may transition between the first and the second voltage levels over a time in excess of 50 ms or in excess of 100 ms. In one embodiment the transition time is in the range of 100–1000 ms.

In one embodiment the voltage level of the switching signal changes smoothly between the first and the second voltage levels (e.g. with the switching signal passing in a continuous manner through a plurality of intermediate voltage levels as it changes between the first and second voltage levels). The switching signal may however be discontinuous outside of the range of the first and the second voltage levels.

In one embodiment the switching arrangement comprises a signal generator for generating the switching signal. Advantageously, the signal generator may include a square-wave generator and a waveform-shaping filter. This has the advantage that the same circuit
provides both a signal for use by the switching arrangement and a clock signal for use by the control stage.

In one embodiment, the signal generator further provides the complement of the universal switching signal (e.g. to allow switching on or off to be selected at any instant).

Typically, a respective pass gate is provided that can be operated, under the control of the control stage, to connect either the switching signal or the steady signal to the switching stage.

The control stage may be configured to cause the switching stage to change between its first and its second states in response to control logic (e.g. a control logic signal applied to the control stage so as to indicate that it should cause the switching arrangement to change between its first and its second states). However, this control logic does not directly effect the change, so can, for example, be a binary on/off signal that might otherwise give rise to transients in the output. The profile of the change in the output signal is determined entirely by the characteristics of the switching signal.

In one embodiment the switching signal is an oscillating signal (e.g. a signal that repeatedly transitions between the first and second voltage levels). In this way the switching signal may be continuously supplied to the control input of the switching stage with the control logic determining when the switching stage changes between its first and second states using the switching signal to effect the change.

In one embodiment, the switching stage functions as a voltage-controlled resistor (e.g. having a resistance that changes (e.g. monotonically) with voltage). In such a case, it may be configured to have a low-resistance when the switching stage is in the second state, thereby connecting the signal input to a ground or a reference voltage.

In accordance with a second aspect of the present invention, there is provided a circuit (e.g. audio circuit) comprising first and second switching arrangements as defined in the first aspect of the present invention and a signal generator configured to provide a universal switching signal to each of the first and second switching arrangements, wherein the control stage of each of the first and second switching arrangements is further configured to cause its respective switching stage to change between its first and its second states in response to control logic specific to each respective switching arrangement.

Advantageously, such an arrangement may include just one signal generator that supplies a signal to several or to all of the switching arrangements. In a complex analogue
system that includes multiple circuits that must be switched, this can result in a significant reduction in the number of components required to provide implement the switching circuits.

In one embodiment, the outputs of the first and second switching arrangements are connected together to form a multiple signal mixer or multiplexer. Such a circuit can operate to mute all signals, or to connect one or more signals from the input to the output – that is, as a channel mixer or a channel multiplexer.

In one embodiment, the signal generator further provides the complement of the universal switching signal.

In accordance with a third aspect of the present invention, there is provided a method of switching a signal in a circuit (e.g. audio circuit), the circuit including: a switching stage that has a signal input, a signal output and a control input, the switching stage operating to pass a signal from its input to its output at a level that varies from muted to a high level as a voltage appearing on the control input varies between a first and a second level; and a signal generator that generates a switching signal that transitions between the first and the second voltage levels; the method comprising: operating in a steady mode to retain the switching stage in one or other of the muted or the high level by applying to its control input a steady signal at the first or the second level; and, in a transition mode, applying the switching signal generated by the signal generator to the control input of the switching stage to cause the voltage appearing on the control input to transition between one and the other of the first and the second levels.

In one embodiment the switching signal is a soft-switching signal as previously defined in the first aspect of the invention. By suitable timing of the change in mode of operation, the occurrence of sudden changes in the voltage appearing on the control input can be minimised, thereby reducing the likelihood of audible transients appearing on the output.

Typically, in the transient mode, the transition of the voltage appearing on the control input of the switching stage occurs over a time being in the order of 100–1000 ms.

In one embodiment, the circuit includes a further switching stage as previously defined and the signal generator provides a universal switching signal to each of the first and further-defined switching stages, wherein the method further comprises varying operation of the first and further-defined switching stages between the muted and high levels by applying to the first and further-defined switching stages control logic specific to each respective
switching stage.

Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 shows a known arrangement of an operational amplifier configured to sum input signals,

Figure 2 shows a modification to the circuit of Figure 1 that can select from a plurality of inputs to be passed to an output;

Figure 3 shows a circuit embodying the invention for switching a single signal;

Figure 4 illustrates the conductive properties of a conventional pass gate and a voltage-controlled resistor, as used in embodiments of the invention;

Figure 5 shows control signal wave forms used in the control of embodiments of the invention; and

Figure 6 shows a circuit embodying the invention for switching or multiplexing two signals.

Figure 1 shows one known arrangement that may be considered a starting point for implementing signal switching in accordance with the invention. In this arrangement, an operational amplifier 10 is configured as a summing amplifier. In this example, three independent audio signals Vin,1, Vin,2, Vin,3 are summed together. The scheme of Figure 1 is readily extended to accept an arbitrarily large number of independent signals.

This circuit can be adapted, as shown in Figure 2, to function as a multiplexer that can select 0, 1 or more of n input signals to be passed to an output. In this circuit, each input signal Vin,1, Vin,2, Vin,3 is switched by a respective pass gate 12 each controlled by a respective switching signal A1, A2, A3 which, depending upon the particular implementation of the pass gate, may be a single logic signal or a pair of complementary signals. The speed at which the pass gates 12 operate (that is, the speed with which they change from a low-resistance to a high-resistance state) and the presence of any DC offset in the system will determine whether electronic transients, which may be heard as unwanted clicks and pops, will be generated.

A typical pass gate or “analogue switch” is designed such that there is, as near as possible an immediate transition between two distinct states (conducting or not-conducting) associated with the two allowed Boolean states of the input (asserted or not-asserted). This is likely to cause transients in the output of the circuit of Figure 2. Therefore, in moving
towards the present invention, the inventors have adapted the circuit of Figure 2 by using a modified circuit in place of the pass gate.

In implementing a soft switch for one signal, embodiments of the invention provide a circuit as shown in Figure 3.

The circuit of Figure 3 takes an input $V_{in,1}$ and provides an output $V_{out}$. The input $V_{in,1}$ is connected through a series resistance $R_{in,1}$ to an amplification stage 20 that uses a conventionally connected operational amplifier 22. The non-inverting input of the operational amplifier 22 is connected to a ground plane or other reference voltage, as the case may be. The circuit of Figure 3 additionally includes a control stage 24. The control stage 24 includes a voltage-controlled resistor (VCR) 30, a first pass gate 32 and a second pass gate. The VCR 30 has a conductive path connected between the series resistance $R_{in,1}$ and the ground plane or other reference voltage. (Note that the series resistance $R_{in,1}$ is, in typical embodiments, implemented as a length of conductive track on a substrate, with the VCR being connected part way along the track, so that the series resistance $R_{in,1}$ is shown diagrammatically as two series-connected resistors.) A control input of the VCR 30 is connected to outputs of each of the first and the second pass gate 32, 34. The first pass gate 32 receives complementary switching signals $A, \bar{A}$ and the second pass gate 34 receives complementary switching signals $B, \bar{B}$. An input of the first pass gate 32 is connected to a switching signal $V_{switch}$, and an input of the second pass gate 34 is connected to a steady signal $V_{steady}$.

The VCR 30 has a wide switching range. As shown in the lower graph of Figure 4, the input to output resistance $R$ changes from a high-resistance state to a low-resistance state as the voltage $V$ on its control input increases over a range of values, as compared with the sudden change of a typical pass gate, shown in the upper graph of Figure 4.

When this VCR 30 is in its high-resistance state, its presence does not influence the circuit; the input signal $V_{in,1}$ is passed to the amplification stage. When the VCR 30 is in its low-resistance state, it clamps the input to ground (or the voltage reference point), thereby effectively muting the signal.

Note that the resistance values in the circuit of Figure 3 are chosen to be commensurate with the range of resistances implemented by the VCR 30. In practice, these will provide “on” resistances in the low-resistance state of $\Omega(10\Omega)$, so the resistances are chosen to give acceptable attenuation in the muted state with this “on” resistance. The “off”
resistance in the high-resistance state of $O(10^6 \Omega)$, imposing little limitation on ordinary analogue design.

In the above arrangement, if the control signals applied to the voltage applied to the control input of the VCR 30 were changed overly quickly, it would still be capable of generating transients leading to audible clicks and pops on the output. Therefore, the control voltages applied to the control input of the VCR are managed to avoid such quick state changes.

The control voltages applied to the VCR 30 are managed in two parts. Each of these parts conveniently is associated with a respective one of the first and second pass gates, although the same functionality could be achieved using alternative embodiments of the invention. There is a functional split between the two aspects of controlling i) transition phases and ii) steady-state phases. These phases are associated with the first and second pass gates 32, 34.

The first pass gate 30 is used to manage the switching transitions of the VCR, which are made by the application of one half period of a globally available waveform $V_{\text{switch}}$. This waveform makes repeated transitions between control voltage magnitudes associated with the fully conducting, low-resistance state of the VCR 30 and the high-resistance, fully closed state. It is the responsibility of a controlling logic system to identify the sense of the required transition (open to closed or closed to open) and to identify which of the two half cycles of $V_{\text{switch}}$ should be applied to the control input to effect the required transition. It is further the responsibility of a controlling logic system to wait until the appropriate instant of time when that half cycle commences – at this instant, the VCR 30 can be taken through the intended transition.

The second pass gate 32 is used to hold the intended operating state of the VCR 30 for long-term, steady-state operation. This second pass gate is used to switch a Boolean control voltage, $V_{\text{steady}}$, to the VCR. The two defined states of this control voltage also are associated with the fully conducting state of the VCR and the fully "closed" state and, therefore, coincide intentionally with the extreme values of $V_{\text{switch}}$. It is the responsibility of a control logic system to ensure that the controlling inputs to the pass gates are mutually exclusive (that is, $A.B=0$) and to provide the appropriate steady-state control voltage for the VCR, $V_{\text{steady}}$.

The switching waveform, $V_{\text{switch}}$, in this embodiment, is generated by subjecting a
square wave signal to a low-pass filtering operation, as illustrated in Figure 5. This operation is conveniently achieved by a simple filter, which can be realized as a single resistor and capacitor network, in a manner that will be readily understood by those skilled in the technical field. The envelope of the switching waveform \( V_{\text{switch}} \), with its slow rates of change of voltage with respect to time, is responsible for the prevention of transients arising from the operation of the switches – accordingly, the period of the generating square wave and the time constant of the low-pass filter must be selected to give an appropriate signal. These can be easily determined by experiment, a switching time between the two extreme voltages of the order of hundreds of milliseconds \( O(10^{-1}) \) is typically appropriate.

Operation of the control logic system will now be described.

Assume the convention (as implied by Figure 4) that the pass gates 32, 34 and the VCR 30 require a positive control input to switch “on” (that is, go into a low-resistance state) and zero voltage to switch “off” (that is, go into a high-resistance state). The Boolean control variables for the first and second pass gates 32, 34 are, respectively, \( A \) and \( B \), as shown in Figure 3.

On receipt of a request to switch the VCR 30 of Figure 3 into a low-resistance state (thereby muting the audio input), the control logic must, with reference to Figure 5:

- wait until time \( T_1 \);
- turn on the first pass gate 30 (\( A=1 \)) and turn off the second pass gate 32 (\( B=0 \));
- assert the steady state control \( V_{\text{steady}} = 1 \) (note: the second pass gate 32 is off at this point and the switching waveform is applied via the first pass gate to the control input of the VCR);
- wait until time \( T_2 \); and
- turn off the first pass gate 32 (\( A=0 \)) and turn on the second pass gate 34 (\( B=1 \)).

The input is now muted and the logic simply maintains \( V_{\text{steady}} = 1 \) and \( B = 1 \) until the switch is to be changed again.

The description above has been simplified for clarity. In practice, the precise timing of the steps within 2 and 5 and the actions at 1 and 4 is important to ensure that no sudden changes to the voltage on the control input for the VCR 30 occur.

On receipt of a request to switch the VCR 30 of Figure 3 into its high-resistance state (thereby enabling the audio input), the control logic must:

- wait until time \( T_2 \);
turn on the first pass gate 30 ($A = 1$) and turn off the second pass gate 32 ($B = 0$); assert the steady state control ($V_{steady} = 0$) (note: the steady-state pass gate is off at this point and the switching waveform is again applied to the control input of the VCR); wait until $T_1$;

5 turn off the first pass gate ($A = 0$) and turn on the steady-state pass gate ($B = 1$) The input is now un-muted and the logic simply maintains $V_{steady} = 0$ and $B = 1$ until the switch is to be changed again.

The similarity between the procedures for the two transitions leads to efficiency in the design and implementation of the control logic.

10 The above embodiment shows how a single signal can be switched between a muted and an un-muted state. This can be extended straightforwardly to control multiple signals such that they can be muted, multiplexed or mixed, as required. For clarity, an embodiment that controls only two signals is illustrated in Figure 6 and will be described: the extension to a larger number of signals presents no difficulty.

15 Figure 6 shows a summing amplifier with two audio inputs. Each input is to a respective switching stage 241, 242 that is similar to the switching stage described above with reference to Figure 3. The circuit of Figure 6 has two signal inputs $V_{in,1}$ and $V_{in,2}$ that are connected to the respective switching stages 241, 242. The output of each of the switching stages 241, 242 is connected to the input of a common amplification stage 20, again, similar to that described with reference to Figure 3. This allows the individual inputs $V_{in,1}$ and $V_{in,2}$ to be enabled or muted independently.

In general, the circuit could have $n$ inputs being identified by an index $i$. Each input $V_{in,i}$ has associated Boolean control variables $A_i$, $B_i$ and $V_{steady,i}$ (and, if required, their complements). However, the analogue switching waveform $V_{switch}$ is a universal switching waveform formed by a single signal generator and shared between the inputs (and the inputs of any other switching stages forming part of the circuit). As shown in Figure 6, the system can mute or enable both switches simultaneously. If, however, the switches were required to make opposite transitions (one input muting, the other opening or vice versa), one transition would have to be made in one half cycle of $V_{switch}$ and the other in the subsequent half cycle. In such an embodiment, the maximum switching latency of the entire scheme would be $3T/2$, where $T$ is the period of the switching waveform $V_{switch}$.

In embodiments that require complementary control signals, it has already been
noted it may be desirable to distribute not only the waveform \( V_{\text{switch}} \) but also its complement. In such cases, it is possible to modify the controlling logic to exploit the fact that there is a positive-going and a negative-going transition of the switching waveform available every half cycle, such that the maximum switching latency of the entire scheme would be \( T \).

Advantageously, the provision of a universal switching waveform can result in a significant reduction in the number of components required to provide implement the switching circuits.

In the above embodiments a continuous switching waveform (e.g. oscillatory waveform) can be distributed to many switching circuits within a device. Alternatively, it is possible to use a centrally derived switching waveform covering only a single transition (potentially also distributed with its complement), which is sent to all switches and used by any making a transition. Similarly, it is possible to distribute this single transition waveform and its complement throughout the device, either to facilitate the control of the VCR or to minimise timing latency.
Claims:

1. A switching arrangement for a circuit, the switching arrangement comprising:
   a signal input;
   a signal output;
   a switching stage that has a control input, the switching stage being operative, in
   response to a control signal applied to the control input changing between a first voltage
   level and a second voltage level, to change between a first state in which it causes a signal on
   the signal input to pass to the signal output and a second state in which the signal output is
   muted;
   a control stage that operates: in a steady mode to apply a steady signal to the control
   input of the switching stage at one or other of the first or the second voltage level to cause
   the switching arrangement to be maintained in its first or its second state as required; and in
   a switching mode to apply a switching signal that transitions between the first voltage level
   and the second voltage level to the control input of the switching stage to cause the
   switching arrangement to transition between its first and its second state.

2. A switching arrangement according to claim 1, wherein the switching signal
   transitions between the first and the second voltage levels in a period of time that causes the
   switching stage to change state at a rate that is sufficiently slow as to prevent audible
   transients appearing on the signal output.

3. A switching arrangement according to claim 1 or claim 2, wherein the voltage level
   of the switching signal changes smoothly between the first and the second voltage levels.

4. A switching arrangement according to any of the preceding claims, wherein the
   control stage is configured to cause the switching stage to change between its first and its
   second states in response to control logic.

5. A switching arrangement according to any of the preceding claims, wherein the
   switching stage functions as a voltage-controlled resistor.
6. A switching arrangement according to claim 4, wherein the control stage is configured to connect the signal input to a ground or a reference voltage when the switching stage is in the second state.

7. A circuit comprising first and second switching arrangements as defined in any of the preceding claims and a signal generator configured to provide a universal switching signal to each of the first and second switching arrangements, wherein the control stage of each of the first and second switching arrangements is further configured to cause its respective switching stage to change between its first and its second states in response to control logic specific to each respective switching arrangement.

8. A circuit according to claim 7, wherein the signal generator further provides the complement of the universal switching signal.

9. A method of switching a signal in a circuit, the circuit including:
   
a switching stage that has a signal input, a signal output and a control input, the switching stage operating to pass a signal from its input to its output at a level that varies from muted to a high level as a voltage appearing on the control input varies between a first and a second level; and
   
a signal generator that generates a switching signal that transitions between the first and the second voltage levels;
   
   the method comprising: operating in a steady mode to retain the switching stage in one or other of the muted or the high level by applying to its control input a steady signal at the first or the second level; and, in a transition mode, applying the switching signal generated by the signal generator to the control input of the switching stage to cause the voltage appearing on the control input to transition between one and the other of the first and the second levels.

10. A method according to claim 9, wherein the circuit includes a further switching stage as previously defined and the signal generator provides a universal switching signal to each of the first and further-defined switching stages, wherein the method further comprises varying operation of the first and further-defined switching stages between the muted and
high levels by applying to the first and further-defined switching stages control logic specific to each respective switching stage.
Fig 1
(Prior Art)

Fig 2
Fig 3
Fig 4
Fig 6
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

**INV.** H03G3/34  H03K17/16

**ADD.**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H03K  H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
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<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
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<td>abstract; figures 1-5  column 1, line 26 - column 2, line 5  column 4, line 12 - column 5, line 23</td>
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<td>US 5 444 312 A (NOBLETT RONALD D [US] ET AL) 22 August 1995 (1995-08-22)</td>
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