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(54) Title: REMOTE WEARABLE INPUT SOURCES FOR ELECTRONIC DEVICES

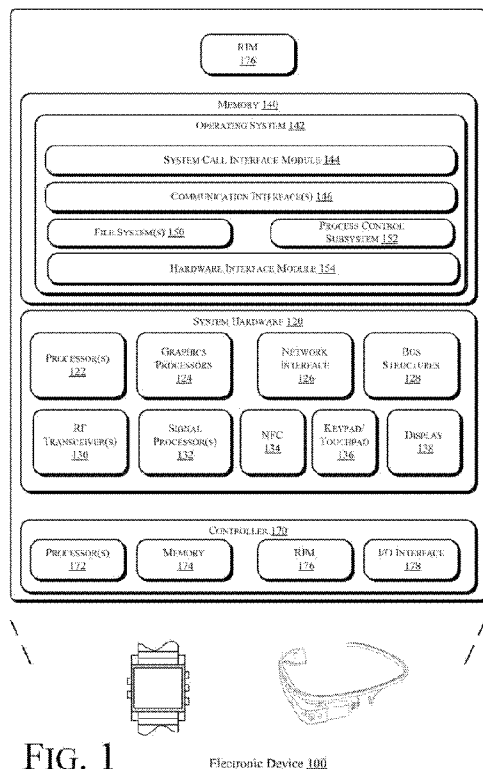


FIG. 1

Electronic Device 100

(57) Abstract: In one example an electronic device comprises at least one sensor to detect an input from a remote input source and a controller comprising logic, at least partly including hardware logic, to detect an input on the at least one sensor, generate a signal in response to the input; and forward the signal to an application. Other examples may be described.



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REMOTE WEARABLE INPUT SOURCES FOR ELECTRONIC DEVICES

BACKGROUND

The subject matter described herein relates generally to the field of electronic devices and more particularly to a remote input sources for electronic devices.

Some small form factor electronic devices including wearable electronic devices such as smart watches, smart glasses, smart bracelets, and the like, have limited space for input devices. Accordingly, remote input sources Techniques for electronic devices may find utility, particularly with small form factor and/or wearable devices.

BRIEF DESCRIPTION OF THE DRAWINGS

The detailed description is described with reference to the accompanying figures.

Fig. 1 is a schematic illustration of an electronic device which may be adapted to cooperate with a remote input source in accordance with some examples.

Fig. 2 is a high-level schematic illustration of an exemplary architecture to implement remote input sources with an electronic device in accordance with some examples.

Figs. 3A-3C are schematic illustrations of an electronic device adapted to implement remote input sources in accordance with some examples.

Figs. 4A-4C are schematic illustrations of an electronic device adapted to implement remote input sources in accordance with some examples.

Figs. 5A-5B are flowcharts illustrating operations in a method to implement remote input sources in accordance with some examples.

Figs. 6-10 are schematic illustrations of electronic devices which may be adapted to implement smart frame toggling in accordance with some examples.

DETAILED DESCRIPTION

Described herein are exemplary systems and methods to implement remote input sources in electronic devices. In the following description, numerous specific details are set forth to provide a thorough understanding of various examples. However, it will be understood by those skilled in the art that the various examples may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been illustrated or described in detail so as not to obscure the particular examples.

As described above, it may be useful to provide electronic device(s), and especially small form factor and/or wearable electronic devices, with remote input sources which may be used to

provide inputs to the electronic device(s). In some examples the subject matter described herein addresses these and other issues by providing a system comprising at least one conductive lead extending from at least one remote input source to a predetermined location and an electronic device, comprising at least one sensor to detect an input from the at least one conductive lead
5 extending from the at least one remote input source. The electronic device further comprises a controller comprising logic, at least partly including hardware logic, to detect an input on the at least one sensor, generate a signal in response to the input, and forward the signal to an application.

In some examples the electronic device may be embodied as a wearable device, e.g., a
10 bracelet or a smartwatch and the remote input source may be a region proximate the electronic device. The remote input source may be coupled to the electronic device by a conductive lead. In some examples the conductive lead and/or sensor may be embodied as a visible or invisible tattoo formed on the skin of a user. In other examples the system may include a sleeve, patch, or other wearable component which includes space for the input source(s) and conductive leads
15 extending from the input source(s) to a location that provides a contact with sensors on the electronic device.

Additional features and operating characteristics of the electronic device and associated system are described below with reference to Figs. 1-10.

Fig. 1 is a schematic illustration of an electronic device 100 which may be adapted to
20 include a remote input manager in accordance with some examples. In various examples, electronic device 100 may include or be coupled to one or more accompanying input/output devices including a display, one or more speakers, a keyboard, one or more other I/O device(s), a mouse, a camera, or the like. Other exemplary I/O device(s) may include a touch screen, a voice-activated input device, a track ball, a geolocation device, an accelerometer/gyroscope,
25 biometric feature input devices, and any other device that allows the electronic device 100 to receive input from a user.

The electronic device 100 includes system hardware 120 and memory 140, which may be implemented as random access memory and/or read-only memory. A file store may be communicatively coupled to electronic device 100. The file store may be internal to electronic
30 device 100 such as, e.g., eMMC, SSD, one or more hard drives, or other types of storage devices. Alternatively, the file store may also be external to electronic device 100 such as, e.g., one or more external hard drives, network attached storage, or a separate storage network.

System hardware 120 may include one or more processors 122, graphics processors 124, network interfaces 126, and bus structures 128. In one embodiment, processor 122 may be
35 embodied as an Intel® Atom™ processors, Intel® Atom™ based System-on-a-Chip (SOC) or

Intel ® i3/i5/i7 series processor available from Intel Corporation, Santa Clara, California, USA. As used herein, the term "processor" means any type of computational element, such as but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, or any other type of processor or processing circuit.

Graphics processor(s) 124 may function as adjunct processor that manages graphics and/or video operations. Graphics processor(s) 124 may be integrated onto the motherboard of electronic device 100 or may be coupled via an expansion slot on the motherboard or may be located on the same die or same package as the Processing Unit.

In one embodiment, network interface 126 could be a wired interface such as an Ethernet interface (see, e.g., Institute of Electrical and Electronics Engineers/IEEE 802.3-2002) or a wireless interface such as an IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a general packet radio service (GPRS) , 3G, 4G, LTE interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Bus structures 128 connect various components of system hardware 128. In one embodiment, bus structures 128 may be one or more of several types of bus structure(s) including a memory bus, a peripheral bus or external bus, and/or a local bus using any variety of available bus architectures including, but not limited to, 11-bit bus, Industrial Standard Architecture (ISA), Micro-Channel Architecture (MSA), Extended ISA (EISA), Intelligent Drive Electronics (IDE), VESA Local Bus (VLB), Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Advanced Graphics Port (AGP), Personal Computer Memory Card International Association bus (PCMCIA), and Small Computer Systems Interface (SCSI), a High Speed Synchronous Serial Interface (HSI), a Serial Low-power Inter-chip Media Bus (SLIMbus®), USB 3.0, Type-C or the like.

Electronic device 100 may include an RF transceiver 130 to transceive RF signals, a Near Field Communication (NFC) radio 134, and a signal processing module 132 to process signals received by RF transceiver 130. RF transceiver may implement a local wireless connection via a protocol such as, e.g., Bluetooth or 802.11X. IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band,

802.11G-2003). Another example of a wireless interface would be a WCDMA, LTE, general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Electronic device 100 may further include one or more input/output interfaces such as, e.g.,
5 a keypad 136 and a display 138. In some examples electronic device 100 may not have a keypad and use the touch panel for input.

Memory 140 may include an operating system 142 for managing operations of electronic device 100. In one embodiment, operating system 142 includes a hardware interface module 154 that provides an interface to system hardware 120. In addition, operating system 140 may
10 include a file system 150 that manages files used in the operation of electronic device 100 and a process control subsystem 152 that manages processes executing on electronic device 100.

Operating system 142 may include (or manage) one or more communication interfaces 146 that may operate in conjunction with system hardware 120 to transceive data packets and/or data streams from a remote source. Operating system 142 may further include a system call interface
15 module 144 that provides an interface between the operating system 142 and one or more application modules resident in memory 130. Operating system 142 may be embodied as a UNIX operating system or any derivative thereof (e.g., Linux, Android, *etc.*) or as a Windows® brand operating system, or other operating systems.

In some examples an electronic device may include a controller 170, which may comprise
20 one or more controllers that are separate from the primary execution environment. The separation may be physical in the sense that the controller may be implemented in controllers which are physically separate from the main processors. Alternatively, the trusted execution environment may be logical in the sense that the controller may be hosted on same chip or chipset that hosts the main processors.

By way of example, in some examples the controller 170 may be implemented as an
25 independent integrated circuit located on the motherboard of the electronic device 100, e.g., as a dedicated processor block on the same SOC die. In other examples the trusted execution engine may be implemented on a portion of the processor(s) 122 that is segregated from the rest of the processor(s) using hardware enforced mechanisms

In the embodiment depicted in Fig. 1 the controller 170 comprises a processor 172, a
30 memory module 174, a remote input manager (RIM) 176, and an I/O interface 178. In some examples the memory module 174 may comprise a persistent flash memory module and the various functional modules may be implemented as logic instructions encoded in the persistent memory module, e.g., firmware or software. The I/O module 178 may comprise a serial I/O
35 module or a parallel I/O module. Because the controller 170 is separate from the main

processor(s) 122 and operating system 142, the controller 170 may be made secure, i.e., inaccessible to hackers who typically mount software attacks from the host processor 122. In some examples portions of the remote input manager 176 may reside in the memory 140 of electronic device 100 and may be executable on one or more of the processors 122.

5 In some examples the remote input manager 176 interacts with one or more other components of the electronic device 100 to define one or more remote input sources for electronic device 100 and to accept inputs from the remote input sources. Fig. 2 is a high-level schematic illustration of an exemplary architecture to implement a remote input manager 176 in electronic devices. Referring to Fig. 2, a controller 220 may be embodied as general purpose processor 122 or as a low-power controller such as controllers 170. Controller 220 may comprise
10 an input/output (I/O) interface 240, a projector unit 250, a mapping unit 250, and a local memory 230. As described above, in some examples the mapping unit 260 may be implemented as logic instructions executable on controller 220, e.g., as software or firmware, or may be reduced to hardwired logic circuits. Local memory 230 may be implemented using volatile and/or non-
15 volatile memory.

Controller 220 may be communicatively coupled to one or more remote input sources 270A, 270B, 270C, which may be referred to collectively herein by reference numeral 270, by conductive leads 272A, 272B, 272C, which may be referred to collectively herein by reference numeral 272. In operation, conductive leads 272 convey signals input into remote input sources
20 270 to I/O interface 240.

As illustrated in Figs. 3A-3C, in some examples an electronic device 300 for pulse diagnosis may be implemented as a device capable of being worn about the wrist of a subject. Device 300 may comprise a band 320 and a display 316 mounted on the band 320. Sensors 310A, 310B, 310C, which may be referred to collectively herein by reference numeral 310, may
25 be mounted on a back panel of the display 318 and positioned to receive input signals from conductive leads 272 which extend remote input sources 270.

Figs. 4A-4C are schematic illustrations of an electronic device adapted to implement remote input sources in accordance with some examples. Referring to Figs. 4A-4C, in a first example the electronic device 300 is positioned about a wrist 410 of a user such that the
30 conductive leads 272 are in contact with the sensors 310 on electronic device 300. While in a second example the electronic device 300 may be coupled to a sleeve or wrap 420 that wraps about a portion of a user's wrist 410 such that the conductive leads 272 are in contact with the sensors 310 on electronic device 300.

As illustrated in Fig. 4B, in some examples the remote input source(s) 270 may be defined
35 by one or more tattoos on the skin of a user and the conductive leads 272 may be formed from

tattoos comprising electrically conductive ink. Alternatively, as illustrated in Fig. 4C the remote input source(s) may be projected onto a surface remote from the electronic device 300, or may be formed from ink that is visible only when illuminated by electromagnetic radiation of a specific frequency, e.g., ultraviolet or infrared light.

5 Referring to Figs. 4A and Fig. 5A in one example the remote input manager 176 includes logic which, at operation 510, detects an input on at least one of the sensors 310. In the example depicted in Fig. 4A the remote input manager 176 includes logic 450 which monitors a capacitance at the sensors 310. The conductive leads 272 are coupled to the sensors 310 via a dielectric material (e.g., skin or the sleeve 420) which results in a capacitance on capacitor 454.
10 When a user contacts the conductive link 272, e.g., by touching the remote input source 270 it causes the capacitance to change. The capacitance change causes a voltage change which drives a current through diode 456 into comparator 458. The voltage input to comparator 458 is compared against a threshold 460, and if the voltage level exceeds the threshold then switch 462 is triggered to generate an output on one of lines 464 or 466, which output may be detected by
15 remote input manager 176.

At operation 515 the remote input manager 176 generates a signal in response to the output detected at operation 510, and at operation 520 the signal is forwarded to an application executing on electronic device 100.

Fig. 5B is a flowchart which illustrates operations in an example of an electronic device
20 which incorporates a projector unit 250 as illustrated in Fig. 2 and Fig. 4C. Referring to Fig. 5B, at operation 550 input source requirements for one or more applications. For example, an application may require multiple remote input sources 270 to receive inputs from a user. At operation 555 the mapping unit 260 maps input source requirements onto a remote surface, and at operation 560 the projection unit 250 projects one or more images of a remote input source
25 onto the surface, as illustrated in Fig. 4C.

At operation 570 the remote input manager 176 detects an input on at least one of the sensors 310, as described above with reference to operation 510. At operation 575 the remote input manager 176 generates a signal in response to the output detected at operation 570, and at operation 580 the signal is forwarded to an application executing on electronic device 100.

30 As described above, in some examples the electronic device may be embodied as a computer system. Fig. 6 illustrates a block diagram of a computing system 600 in accordance with an example. The computing system 600 may include one or more central processing unit(s) 602 or processors that communicate via an interconnection network (or bus) 604. The processors 602 may include a general purpose processor, a network processor (that processes data communicated over a computer network 603), or other types of a processor (including a reduced
35

instruction set computer (RISC) processor or a complex instruction set computer (CISC)). Moreover, the processors 602 may have a single or multiple core design. The processors 602 with a multiple core design may integrate different types of processor cores on the same integrated circuit (IC) die. Also, the processors 602 with a multiple core design may be implemented as symmetrical or asymmetrical multiprocessors. In an example, one or more of the processors 602 may be the same or similar to the processors 102 of Fig. 1. For example, one or more of the processors 602 may include the control unit 120 discussed with reference to Figs. 1-3. Also, the operations discussed with reference to Figs. 3-5 may be performed by one or more components of the system 600.

A chipset 606 may also communicate with the interconnection network 604. The chipset 606 may include a memory control hub (MCH) 608. The MCH 608 may include a memory controller 610 that communicates with a memory 612 (which may be the same or similar to the memory 130 of Fig. 1). The memory 412 may store data, including sequences of instructions, that may be executed by the processor 602, or any other device included in the computing system 600. In one example, the memory 612 may include one or more volatile storage (or memory) devices such as random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), or other types of storage devices. Nonvolatile memory may also be utilized such as a hard disk. Additional devices may communicate via the interconnection network 604, such as multiple processor(s) and/or multiple system memories.

The MCH 608 may also include a graphics interface 614 that communicates with a display device 616. In one example, the graphics interface 614 may communicate with the display device 616 via an accelerated graphics port (AGP). In an example, the display 616 (such as a flat panel display) may communicate with the graphics interface 614 through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display 616. The display signals produced by the display device may pass through various control devices before being interpreted by and subsequently displayed on the display 616.

A hub interface 618 may allow the MCH 608 and an input/output control hub (ICH) 620 to communicate. The ICH 620 may provide an interface to I/O device(s) that communicate with the computing system 600. The ICH 620 may communicate with a bus 622 through a peripheral bridge (or controller) 624, such as a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) controller, or other types of peripheral bridges or controllers. The bridge 624 may provide a data path between the processor 602 and peripheral devices. Other types of topologies may be utilized. Also, multiple buses may communicate with the ICH 620, e.g., through multiple bridges or controllers. Moreover, other peripherals in communication with the

ICH 620 may include, in various examples, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), USB port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), or other devices.

5 The bus 622 may communicate with an audio device 626, one or more disk drive(s) 628, and a network interface device 630 (which is in communication with the computer network 603). Other devices may communicate via the bus 622. Also, various components (such as the network interface device 630) may communicate with the MCH 608 in some examples. In addition, the processor 602 and one or more other components discussed herein may be combined to form a
10 single chip (e.g., to provide a System on Chip (SOC)). Furthermore, the graphics accelerator 616 may be included within the MCH 608 in other examples.

 Furthermore, the computing system 600 may include volatile and/or nonvolatile memory (or storage). For example, nonvolatile memory may include one or more of the following: read-only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically
15 EPROM (EEPROM), a disk drive (e.g., 628), a floppy disk, a compact disk ROM (CD-ROM), a digital versatile disk (DVD), flash memory, a magneto-optical disk, or other types of nonvolatile machine-readable media that are capable of storing electronic data (e.g., including instructions).

 Fig. 7 illustrates a block diagram of a computing system 700, according to an example. The system 700 may include one or more processors 702-1 through 702-N (generally referred to
20 herein as “processors 702” or “processor 702”). The processors 702 may communicate via an interconnection network or bus 704. Each processor may include various components some of which are only discussed with reference to processor 702-1 for clarity. Accordingly, each of the remaining processors 702-2 through 702-N may include the same or similar components discussed with reference to the processor 702-1.

25 In an example, the processor 702-1 may include one or more processor cores 706-1 through 706-M (referred to herein as “cores 706” or more generally as “core 706”), a shared cache 708, a router 710, and/or a processor control logic or unit 720. The processor cores 706 may be implemented on a single integrated circuit (IC) chip. Moreover, the chip may include one or more shared and/or private caches (such as cache 708), buses or interconnections (such as a
30 bus or interconnection network 712), memory controllers, or other components.

 In one example, the router 710 may be used to communicate between various components of the processor 702-1 and/or system 700. Moreover, the processor 702-1 may include more than one router 710. Furthermore, the multitude of routers 710 may be in communication to enable data routing between various components inside or outside of the processor 702-1.

The shared cache 708 may store data (e.g., including instructions) that are utilized by one or more components of the processor 702-1, such as the cores 706. For example, the shared cache 708 may locally cache data stored in a memory 714 for faster access by components of the processor 702. In an example, the cache 708 may include a mid-level cache (such as a level 2 (L2), a level 3 (L3), a level 4 (L4), or other levels of cache), a last level cache (LLC), and/or combinations thereof. Moreover, various components of the processor 702-1 may communicate with the shared cache 708 directly, through a bus (e.g., the bus 712), and/or a memory controller or hub. As shown in Fig. 7, in some examples, one or more of the cores 706 may include a level 1 (L1) cache 716-1 (generally referred to herein as “L1 cache 716”). In one example, the control unit 720 may include logic to implement the operations described above with reference to the memory controller 122 in Fig. 2.

Fig. 8 illustrates a block diagram of portions of a processor core 706 and other components of a computing system, according to an example. In one example, the arrows shown in Fig. 8 illustrate the flow direction of instructions through the core 706. One or more processor cores (such as the processor core 706) may be implemented on a single integrated circuit chip (or die) such as discussed with reference to Fig. 7. Moreover, the chip may include one or more shared and/or private caches (e.g., cache 708 of Fig. 7), interconnections (e.g., interconnections 704 and/or 112 of Fig. 7), control units, memory controllers, or other components.

As illustrated in Fig. 8, the processor core 706 may include a fetch unit 802 to fetch instructions (including instructions with conditional branches) for execution by the core 706. The instructions may be fetched from any storage devices such as the memory 714. The core 706 may also include a decode unit 804 to decode the fetched instruction. For instance, the decode unit 804 may decode the fetched instruction into a plurality of uops (micro-operations).

Additionally, the core 706 may include a schedule unit 806. The schedule unit 806 may perform various operations associated with storing decoded instructions (e.g., received from the decode unit 804) until the instructions are ready for dispatch, e.g., until all source values of a decoded instruction become available. In one example, the schedule unit 806 may schedule and/or issue (or dispatch) decoded instructions to an execution unit 808 for execution. The execution unit 808 may execute the dispatched instructions after they are decoded (e.g., by the decode unit 804) and dispatched (e.g., by the schedule unit 806). In an example, the execution unit 808 may include more than one execution unit. The execution unit 808 may also perform various arithmetic operations such as addition, subtraction, multiplication, and/or division, and may include one or more an arithmetic logic units (ALUs). In an example, a co-processor (not shown) may perform various arithmetic operations in conjunction with the execution unit 808.

Further, the execution unit 808 may execute instructions out-of-order. Hence, the processor core 706 may be an out-of-order processor core in one example. The core 706 may also include a retirement unit 810. The retirement unit 810 may retire executed instructions after they are committed. In an example, retirement of the executed instructions may result in processor state being committed from the execution of the instructions, physical registers used by the instructions being de-allocated, etc.

The core 706 may also include a bus unit 714 to enable communication between components of the processor core 706 and other components (such as the components discussed with reference to Fig. 8) via one or more buses (e.g., buses 804 and/or 812). The core 706 may also include one or more registers 816 to store data accessed by various components of the core 706 (such as values related to power consumption state settings).

Furthermore, even though Fig. 7 illustrates the control unit 720 to be coupled to the core 706 via interconnect 812, in various examples the control unit 720 may be located elsewhere such as inside the core 706, coupled to the core via bus 704, etc.

In some examples, one or more of the components discussed herein can be embodied as a System On Chip (SOC) device. Fig. 9 illustrates a block diagram of an SOC package in accordance with an example. As illustrated in Fig. 9, SOC 902 includes one or more processor cores 920, one or more graphics processor cores 930, an Input/Output (I/O) interface 940, and a memory controller 942. Various components of the SOC package 902 may be coupled to an interconnect or bus such as discussed herein with reference to the other figures. Also, the SOC package 902 may include more or less components, such as those discussed herein with reference to the other figures. Further, each component of the SOC package 902 may include one or more other components, e.g., as discussed with reference to the other figures herein. In one example, SOC package 902 (and its components) is provided on one or more Integrated Circuit (IC) die, e.g., which are packaged into a single semiconductor device.

As illustrated in Fig. 9, SOC package 902 is coupled to a memory 960 (which may be similar to or the same as memory discussed herein with reference to the other figures) via the memory controller 942. In an example, the memory 960 (or a portion of it) can be integrated on the SOC package 902.

The I/O interface 940 may be coupled to one or more I/O devices 970, e.g., via an interconnect and/or bus such as discussed herein with reference to other figures. I/O device(s) 970 may include one or more of a keyboard, a mouse, a touchpad, a display, an image/video capture device (such as a camera or camcorder/video recorder), a touch surface, a speaker, or the like.

Fig. 10 illustrates a computing system 1000 that is arranged in a point-to-point (PtP) configuration, according to an example. In particular, Fig. 10 shows a system where processors, memory, and input/output devices are interconnected by a number of point-to-point interfaces. The operations discussed with reference to Fig. 2 may be performed by one or more components of the system 1000.

As illustrated in Fig. 10, the system 1000 may include several processors, of which only two, processors 1002 and 1004 are shown for clarity. The processors 1002 and 1004 may each include a local memory controller hub (MCH) 1006 and 1008 to enable communication with memories 1010 and 1012. MCH 1006 and 1008 may include the memory controller 120 and/or logic 125 of Fig. 1 in some examples.

In an example, the processors 1002 and 1004 may be one of the processors 702 discussed with reference to Fig. 7. The processors 1002 and 1004 may exchange data via a point-to-point (PtP) interface 1014 using PtP interface circuits 1016 and 1018, respectively. Also, the processors 1002 and 1004 may each exchange data with a chipset 1020 via individual PtP interfaces 1022 and 1024 using point-to-point interface circuits 1026, 1028, 1030, and 1032. The chipset 1020 may further exchange data with a high-performance graphics circuit 1034 via a high-performance graphics interface 1036, e.g., using a PtP interface circuit 1037.

As shown in Fig. 10, one or more of the cores 106 and/or cache 108 of Fig. 1 may be located within the processors 1004. Other examples, however, may exist in other circuits, logic units, or devices within the system 1000 of Fig. 10. Furthermore, other examples may be distributed throughout several circuits, logic units, or devices illustrated in Fig. 10.

The chipset 1020 may communicate with a bus 1040 using a PtP interface circuit 1041. The bus 1040 may have one or more devices that communicate with it, such as a bus bridge 1042 and I/O devices 1043. Via a bus 1044, the bus bridge 1043 may communicate with other devices such as a keyboard/mouse 1045, communication devices 1046 (such as modems, network interface devices, or other communication devices that may communicate with the computer network 1003), audio I/O device, and/or a data storage device 1048. The data storage device 1048 (which may be a hard disk drive or a NAND flash based solid state drive) may store code 1049 that may be executed by the processors 1004.

The following examples pertain to further examples.

Example 1 is an electronic device, comprising at least one sensor to detect an input from a remote input source and a controller comprising logic, at least partly including hardware logic, to detect an input on the at least one sensor, generate a signal in response to the input, and forward the signal to an application.

In Example 2, the subject matter of Example 1 can optionally include an arrangement in which the at least one sensor is positioned on a surface of the electronic device.

In Example 3, the subject matter of any one of Examples 1–2 can optionally include an arrangement in which the at least one sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.

In Example 4, the subject matter of any one of Examples 1–3 can optionally include logic, at least partially including hardware logic, configured to detect a change in capacitance proximate the sensor.

In Example 5, the subject matter of any one of Examples 1–4 can optionally include logic, at least partially including hardware logic, configured to detect a change in a voltage level proximate the sensor.

In example 6, the subject matter of any one of Examples 1–5 can optionally include a projection unit to project an image of at least one input source on a surface proximate the electronic device.

In Example 7, the subject matter of any one of Examples 1–6 can optionally include a mapping unit to associate the input source on the surface with the at least one sensor.

Example 8 is system comprising at least one conductive lead extending from at least one remote input source to a predetermined location and an electronic device, comprising at least one sensor to detect an input from the at least one conductive lead extending from the at least one remote input source and a controller comprising logic, at least partly including hardware logic, to detect an input on the at least one sensor, generate a signal in response to the input, and forward the signal to an application.

In Example 9, the subject matter of Example 8 can optionally include an arrangement in which the at least one conductive lead is defined by a conductive ink tattoo.

In Example 10, the subject matter of any one of Examples 8–9 can optionally include an arrangement in which the at least one sensor is positioned on a surface of the electronic device.

In Example 11, the subject matter of any one of Examples 8–10 can optionally include an arrangement in which the at least one sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.

In Example 12, the subject matter of any one of Examples 8–11 can optionally include logic, at least partially including hardware logic, configured to detect a change in capacitance proximate the sensor.

In Example 13 the subject matter of any one of Examples 8–12 can optionally include logic, at least partially including hardware logic, configured to detect a change in a voltage level proximate the sensor.

In example 14, the subject matter of any one of Examples 8-13 can optionally include a projection unit to project an image of at least one input source on a surface proximate the electronic device.

5 In Example 15, the subject matter of any one of Examples 8-14 can optionally include a mapping unit to associate the input source on the surface with the at least one sensor.

Example 16 is a remote input device manager for an electronic device, comprising a controller comprising logic, at least partly including hardware logic, to detect an input on the at least one sensor, generate a signal in response to the input, and forward the signal to an application.

10 In Example 17, the subject matter of Example 16 can optionally include an arrangement in which the at least one sensor is positioned on a surface of the electronic device.

In Example 18, the subject matter of any one of Examples 16-17 can optionally include an arrangement in which the at least one sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.

15 In Example 19, the subject matter of any one of Examples 16-18 can optionally include logic, at least partially including hardware logic, configured to detect a change in capacitance proximate the sensor.

In Example 20, the subject matter of any one of Examples 16-19 can optionally include logic, at least partially including hardware logic, configured to detect a change in a voltage level proximate the sensor.

20 In Example 21, the subject matter of any one of Examples 16-20 can optionally include a projection unit to project an image of at least one input source on a surface proximate the electronic device.

25 In Example 22, the subject matter of any one of Examples 16-21 can optionally include logic, at least partially including hardware logic, configured to detect a change in a voltage level proximate the sensor.

30 The terms "logic instructions" as referred to herein relates to expressions which may be understood by one or more machines for performing one or more logical operations. For example, logic instructions may comprise instructions which are interpretable by a processor compiler for executing one or more operations on one or more data objects. However, this is merely an example of machine-readable instructions and examples are not limited in this respect.

35 The terms "computer readable medium" as referred to herein relates to media capable of maintaining expressions which are perceivable by one or more machines. For example, a computer readable medium may comprise one or more storage devices for storing computer readable instructions or data. Such storage devices may comprise storage media such as, for

example, optical, magnetic or semiconductor storage media. However, this is merely an example of a computer readable medium and examples are not limited in this respect.

The term “logic” as referred to herein relates to structure for performing one or more logical operations. For example, logic may comprise circuitry which provides one or more output signals based upon one or more input signals. Such circuitry may comprise a finite state machine which receives a digital input and provides a digital output, or circuitry which provides one or more analog output signals in response to one or more analog input signals. Such circuitry may be provided in an application specific integrated circuit (ASIC) or field programmable gate array (FPGA). Also, logic may comprise machine-readable instructions stored in a memory in combination with processing circuitry to execute such machine-readable instructions. However, these are merely examples of structures which may provide logic and examples are not limited in this respect.

Some of the methods described herein may be embodied as logic instructions on a computer-readable medium. When executed on a processor, the logic instructions cause a processor to be programmed as a special-purpose machine that implements the described methods. The processor, when configured by the logic instructions to execute the methods described herein, constitutes structure for performing the described methods. Alternatively, the methods described herein may be reduced to logic on, e.g., a field programmable gate array (FPGA), an application specific integrated circuit (ASIC) or the like.

In the description and claims, the terms coupled and connected, along with their derivatives, may be used. In particular examples, connected may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Coupled may mean that two or more elements are in direct physical or electrical contact. However, coupled may also mean that two or more elements may not be in direct contact with each other, but yet may still cooperate or interact with each other.

Reference in the specification to “one example” or “some examples” means that a particular feature, structure, or characteristic described in connection with the example is included in at least an implementation. The appearances of the phrase “in one example” in various places in the specification may or may not be all referring to the same example.

Although examples have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. An electronic device, comprising:
at least one sensor to detect an input from a remote input source; and
a controller comprising logic, at least partly including hardware logic, to:
detect an input on the at least one sensor;
generate a signal in response to the input; and
forward the signal to an application.
2. The electronic device of claim 1, wherein the at least one sensor is positioned on a surface of the electronic device.
3. The electronic device of claim 2, wherein the at least on sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.
4. The electronic device of claim 2, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in capacitance proximate the sensor.
5. The electronic device of claim 2, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in a voltage level proximate the sensor.
6. The electronic device of claim 1, further comprising:
a projection unit to project an image of at least one input source on a surface proximate the electronic device.
7. The electronic device of claim 6, further comprising:
a mapping unit to associate the input source on the surface with the at least one sensor.

8. A system, comprising:
 - at least one conductive lead extending from at least one remote input source to a predetermined location; and
 - an electronic device, comprising:
 - at least one sensor to detect an input from the at least one conductive lead extending from the at least one remote input source; and
 - a controller comprising logic, at least partly including hardware logic, to:
 - detect an input on the at least one sensor;
 - generate a signal in response to the input; and
 - forward the signal to an application.
9. The system of claim 8, wherein the at least one conductive lead is defined by a conductive ink tattoo.
10. The system of claim 9, wherein:
 - the at least one sensor is positioned on a surface of the electronic device.
11. The system of claim 10, wherein the at least one sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.
12. The system of claim 11, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in capacitance proximate the sensor.
13. The system of claim 11, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in a voltage level proximate the sensor.
14. The system of claim 8, further comprising:
 - a projection unit to project an image of at least one input source on a surface proximate the electronic device.
15. The system of claim 14, further comprising:
 - a mapping unit to associate the input source on the surface with the at least one sensor.
16. A remote input device manager for an electronic device, comprising a controller comprising logic, at least partly including hardware logic, to:
 - detect an input on the at least one sensor;
 - generate a signal in response to the input; and
 - forward the signal to an application.

17. The remote input device manager of claim 16, wherein the at least one sensor is positioned on a surface of the electronic device.
18. The remote input device manager of claim 17, wherein the at least on sensor is positioned on a surface that is exposed to a body surface of a user of the electronic device.
19. The remote input device manager of claim 18, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in capacitance proximate the sensor.
20. The remote input device manager of claim 18, wherein the controller comprises logic, at least partly including hardware logic, to detect a change in a voltage level proximate the sensor.
21. The remote input device manager of claim 16, further comprising:
a projection unit to project an image of at least one input source on a surface proximate the electronic device.
22. The remote input device manager of claim 13, further comprising:
a mapping unit to associate the input source on the surface with the at least one sensor.

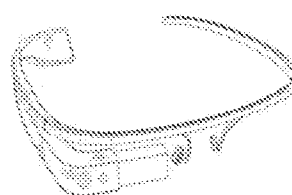
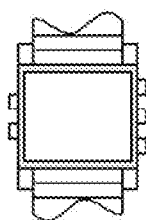
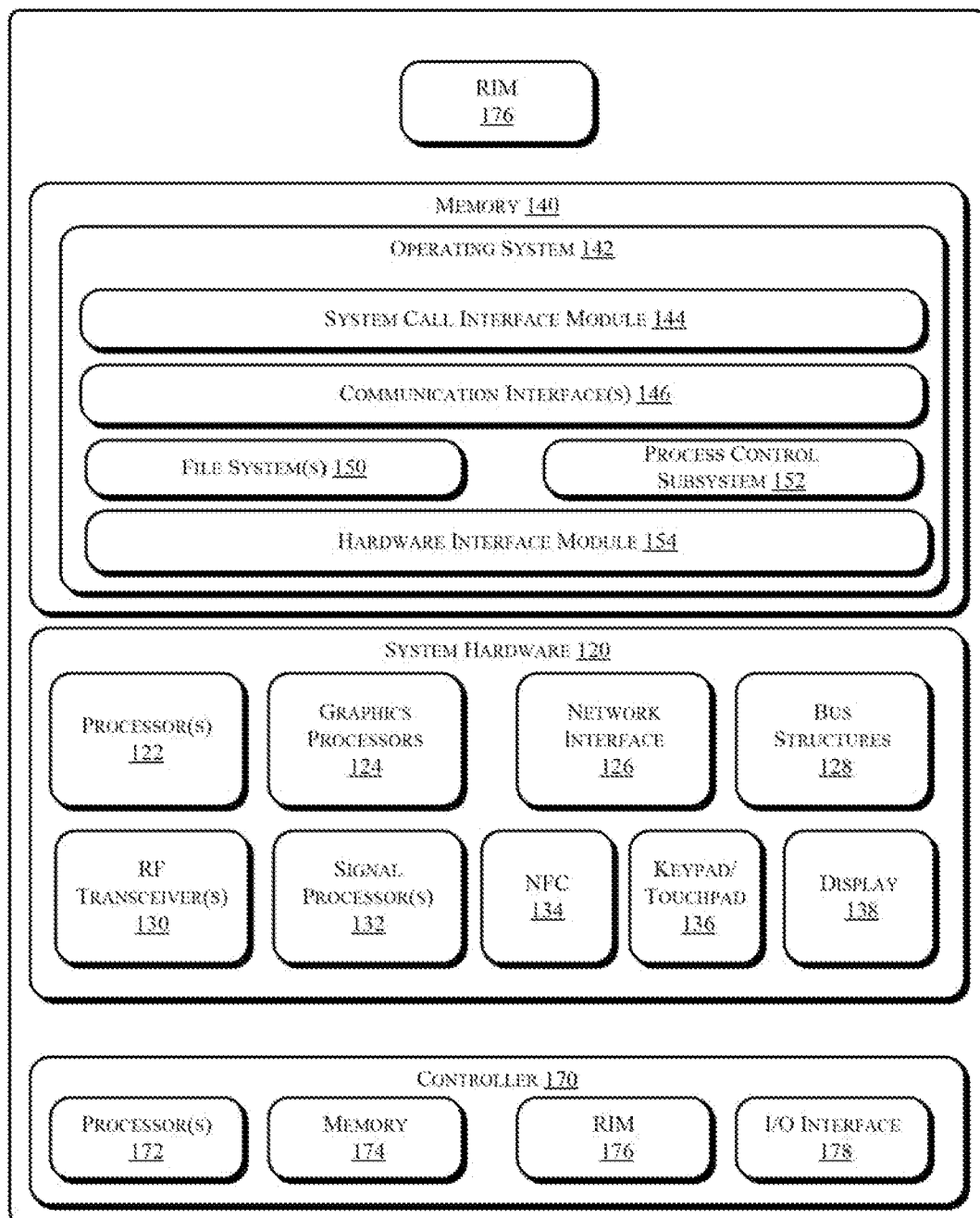


FIG. 1

Electronic Device 100

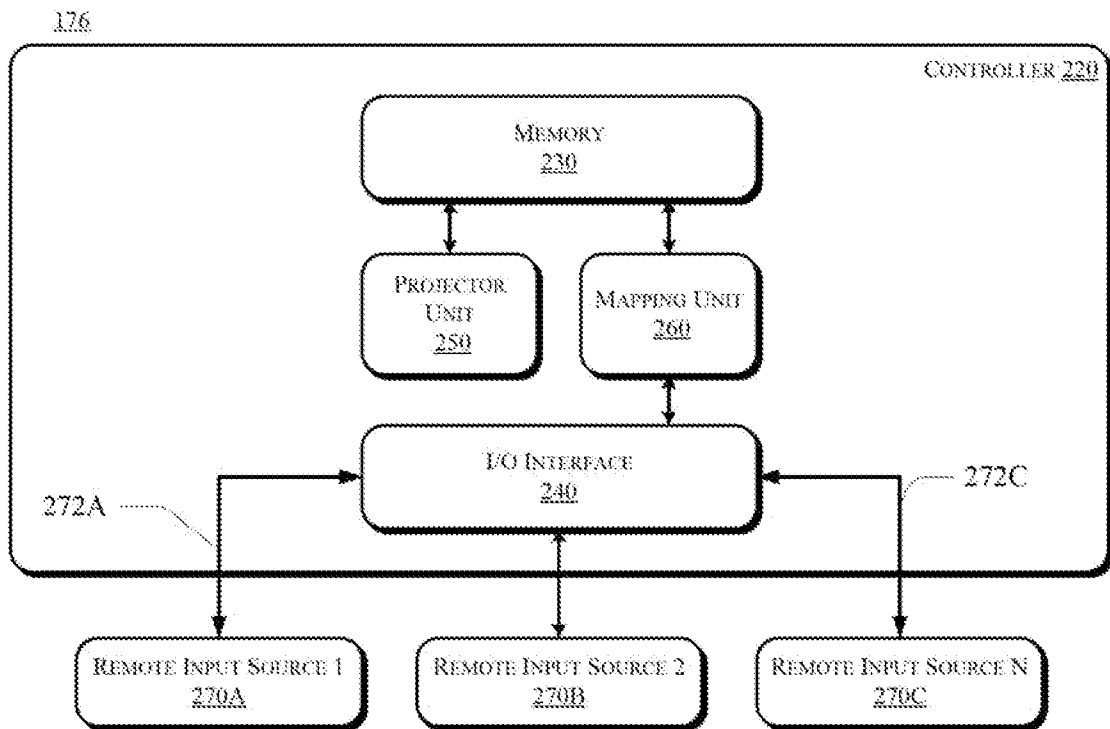


FIG. 2

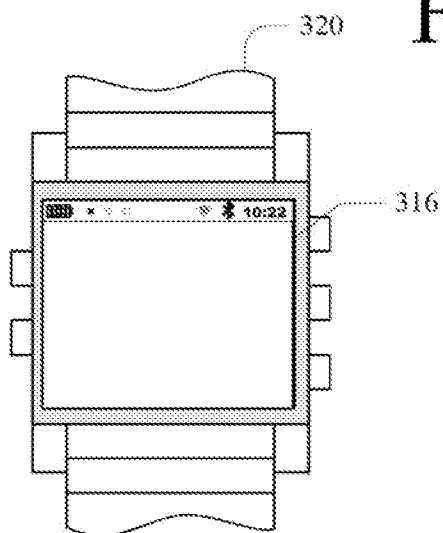


FIG. 3A

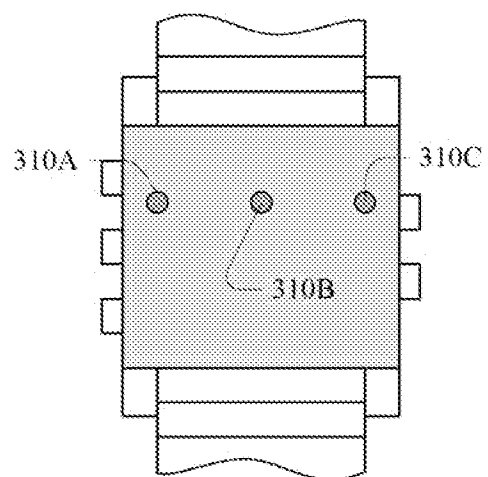


FIG. 3B

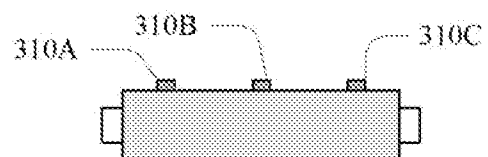


FIG. 3C

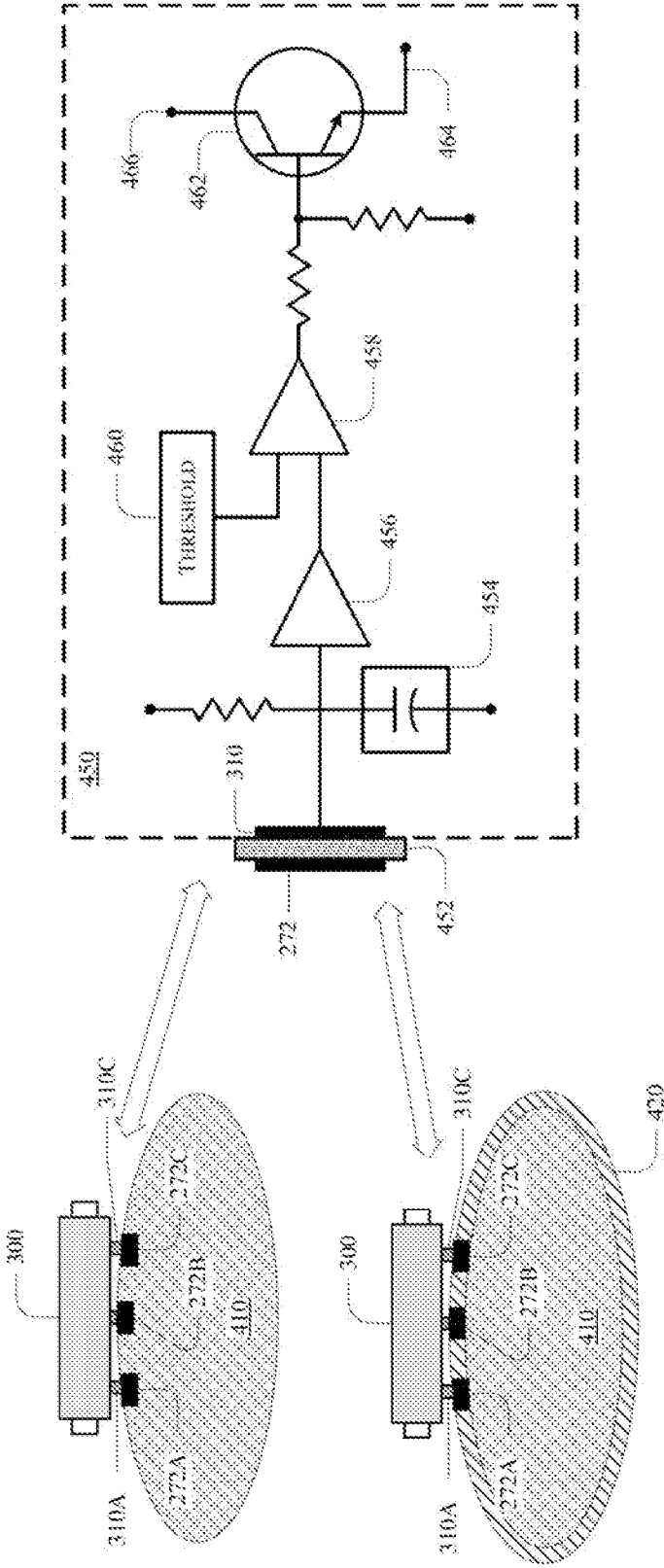


FIG. 4A

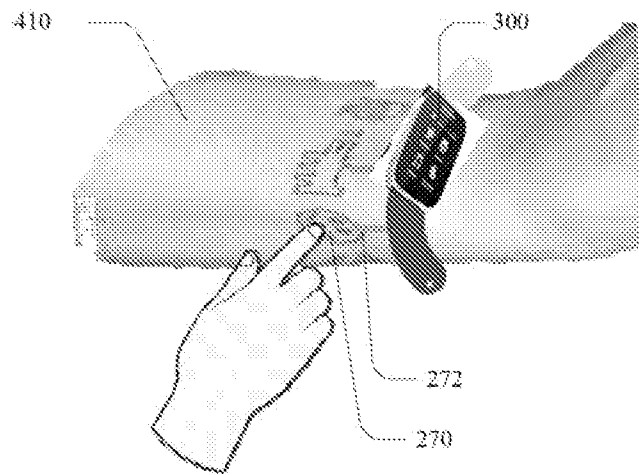


FIG. 4B

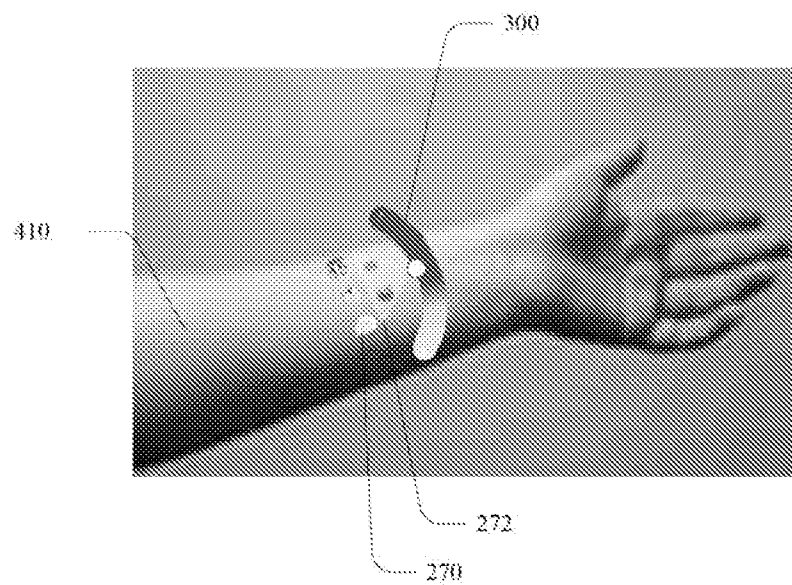


FIG. 4C

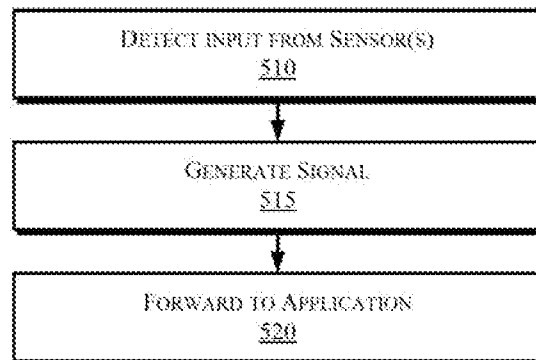


FIG. 5A

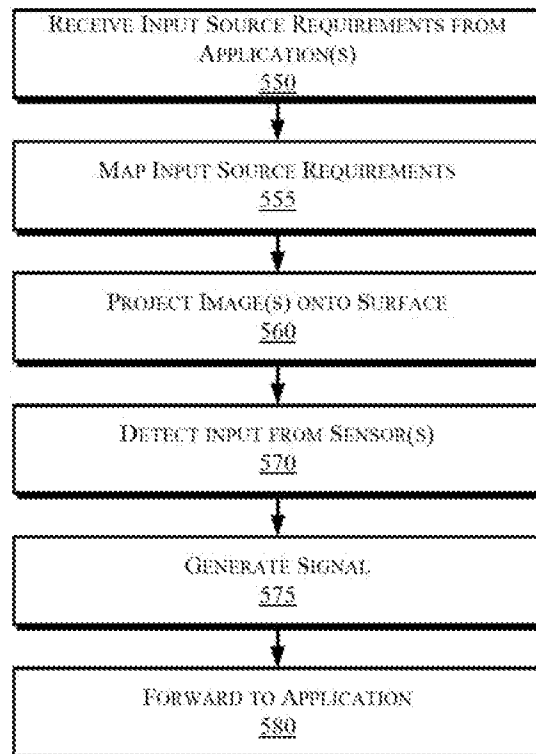


FIG. 5B

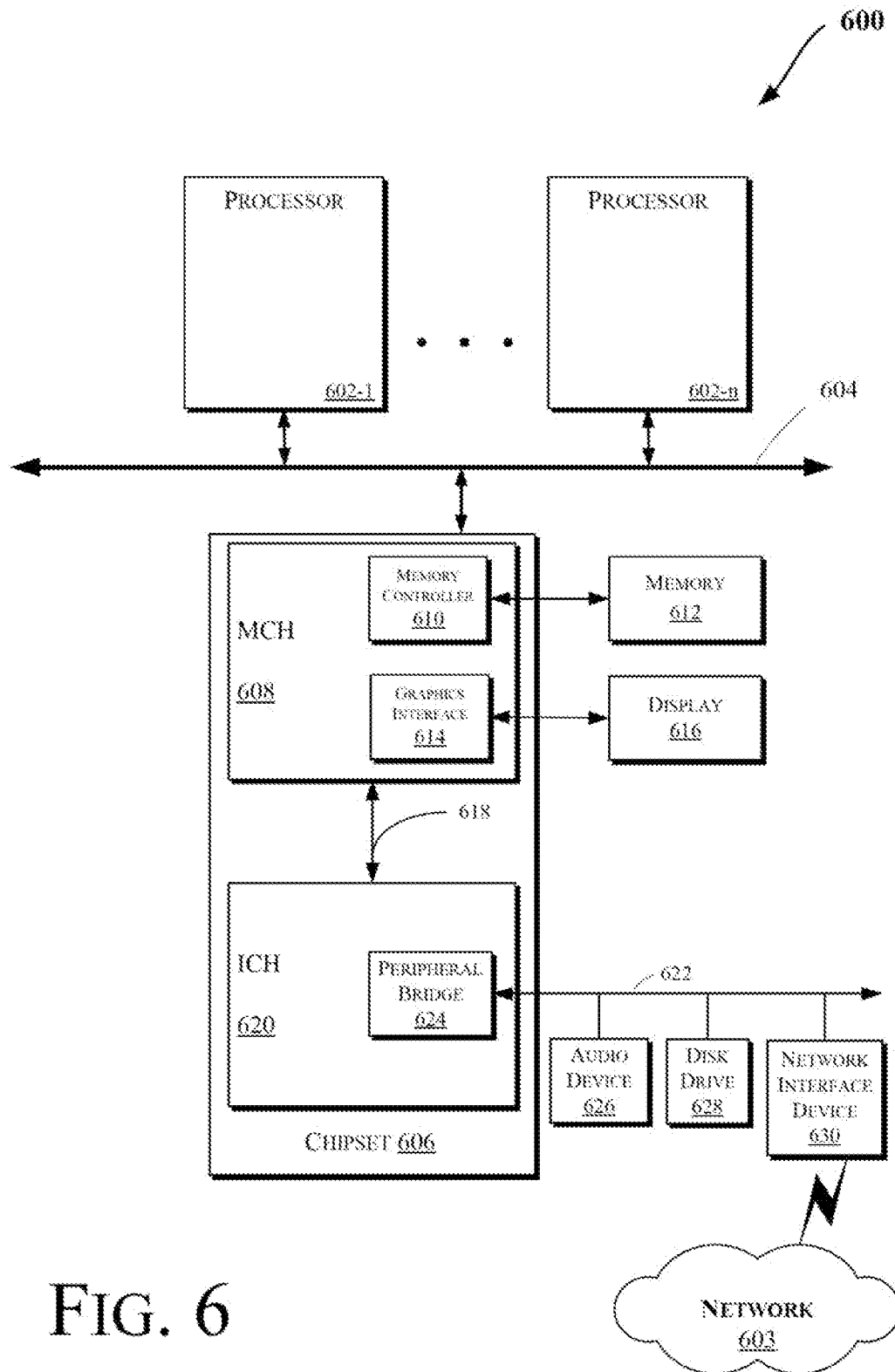


FIG. 6

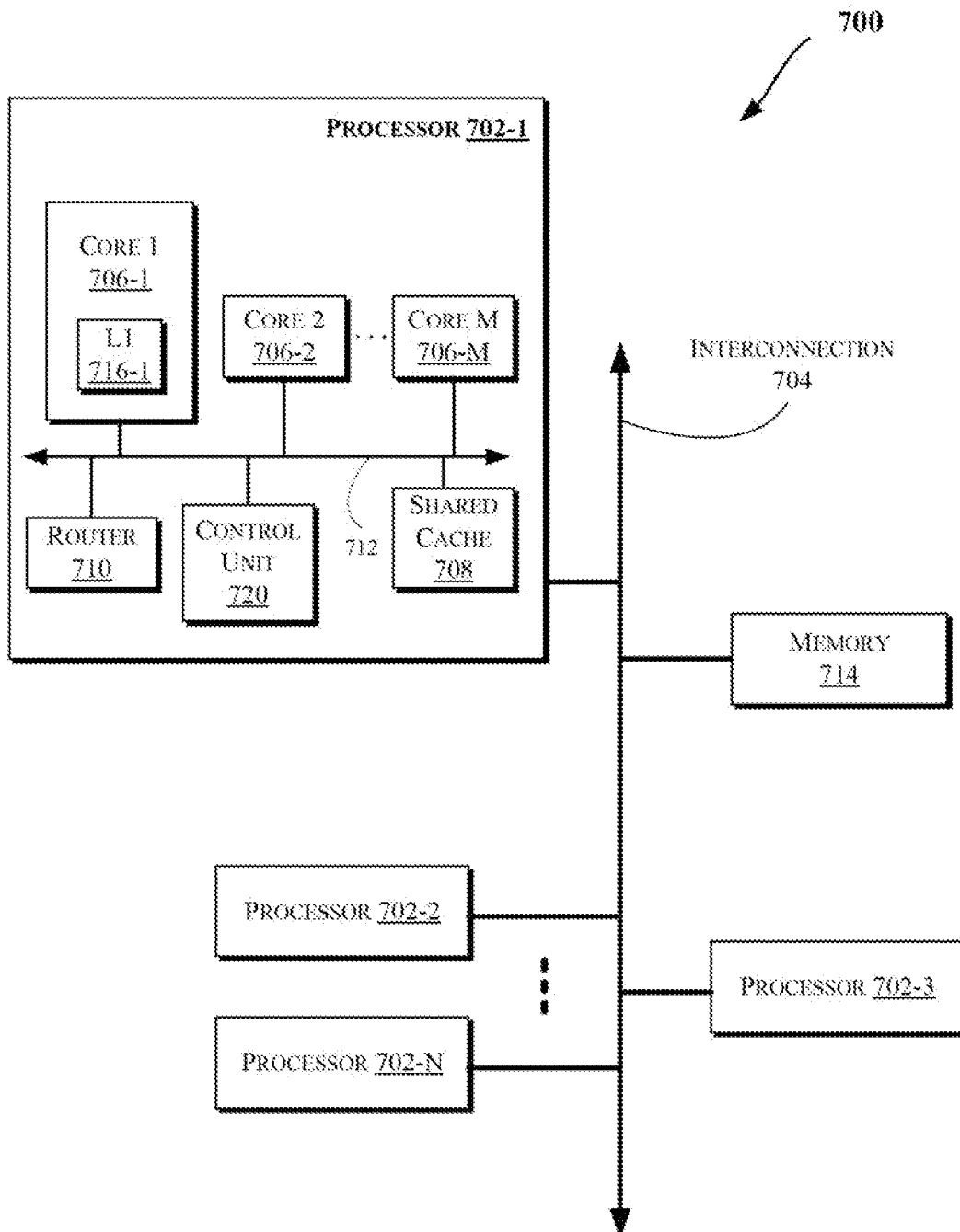


FIG. 7

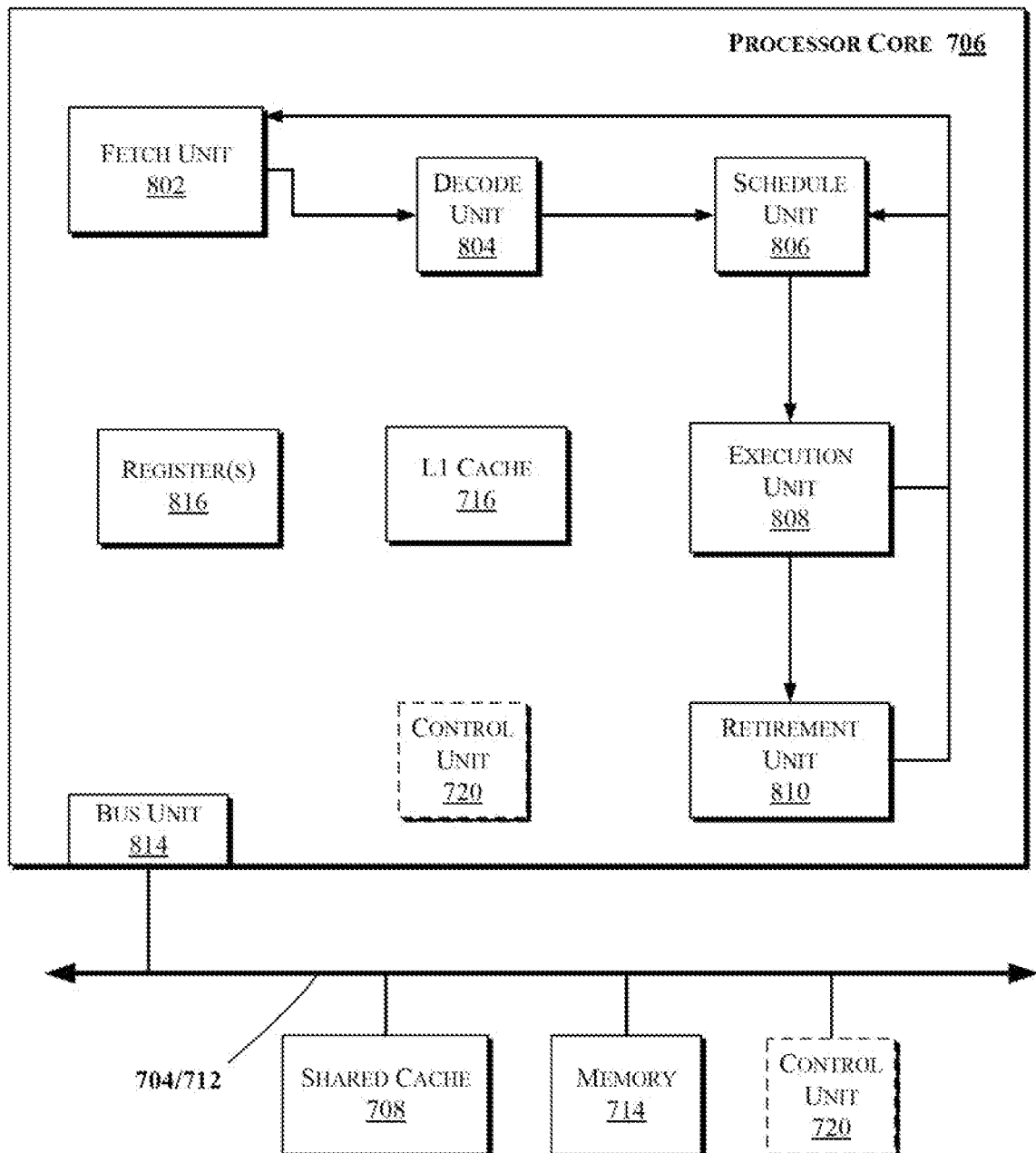


FIG. 8

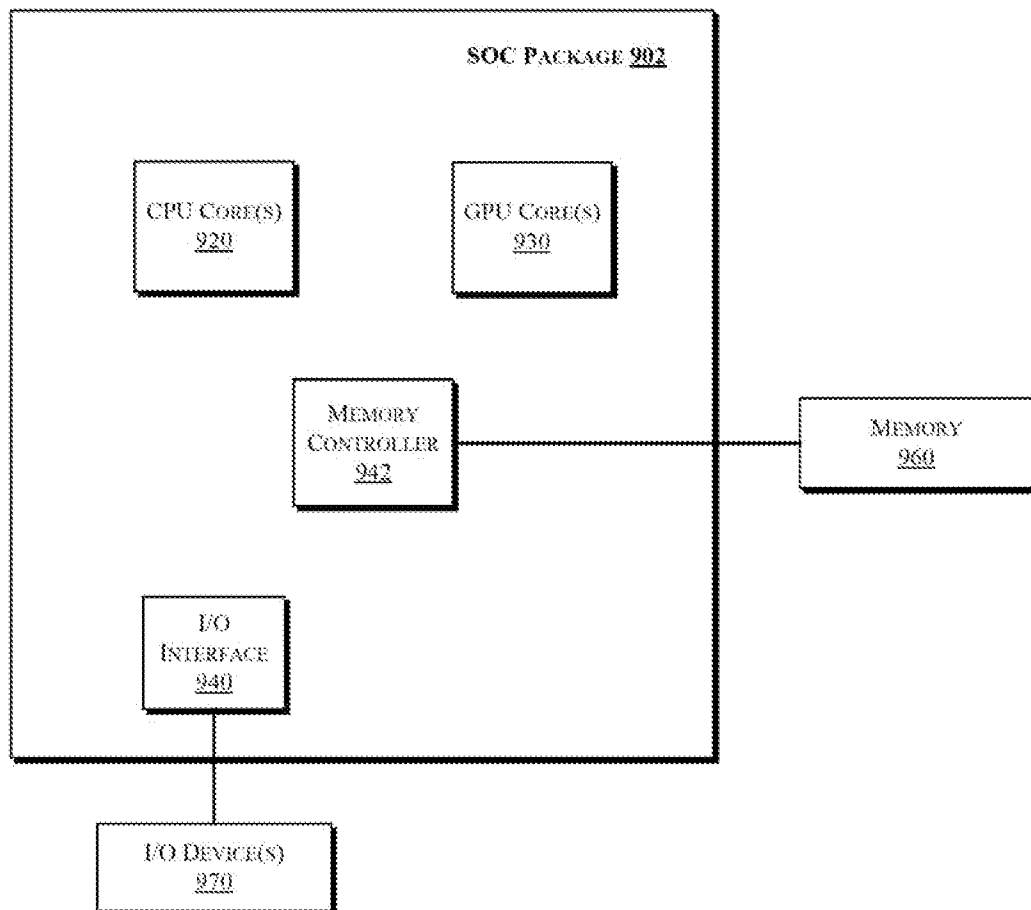


FIG. 9

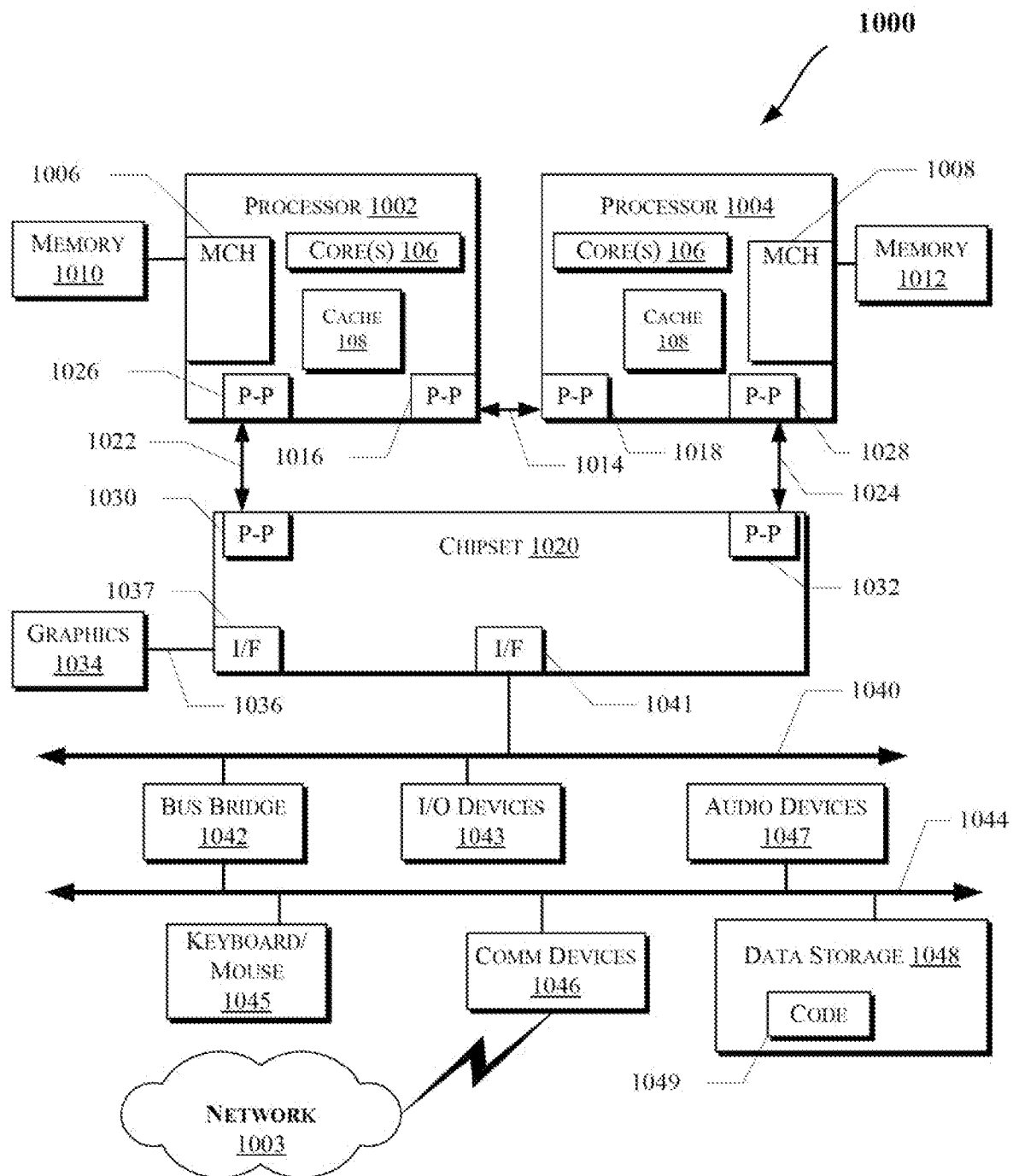


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/046897**A. CLASSIFICATION OF SUBJECT MATTER****G06F 3/01(2006.01)i, G06F 1/16(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 3/01; G09G 5/08; G06F 3/033; H04M 1/00; H05K 1/00; G06F 3/0488; G06F 3/0484; G09G 5/00; G06F 1/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:sensor, detect, input, remote input source, controller, logic, generate, signal, forward, application

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0124949 A1 (RANDOLPH C. DEMUYNCK et al.) 20 May 2010	1-3,6-7,16-18
Y	See paragraphs [0019]-[0020], [0047], [0049], [0067]; and figure 1.	,21-22 4-5,8-15,19-20
Y	US 6307751 B1 (LAWRENCE A. BODONY et al.) 23 October 2001	4-5,8-15,19-20
	See column 1, lines 54-55; column 3, lines 63-64; column 10, lines 34-39; and figure 8B.	
A	WO 2008-069577 A1 (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 12 June 2008	1-22
	See paragraphs [0031]-[0034]; and figure 1.	
A	US 2011-0080339 A1 (ALBERT C. SUN et al.) 07 April 2011	1-22
	See paragraphs [0017]-[0022]; and figure 1.	
A	US 2014-0240263 A1 (SAMSUNG ELECTRONICS CO., LTD.) 28 August 2014	1-22
	See paragraphs [0061]-[0066]; and figures 1-2.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 December 2015 (17.12.2015)

Date of mailing of the international search report

28 December 2015 (28.12.2015)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/046897

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