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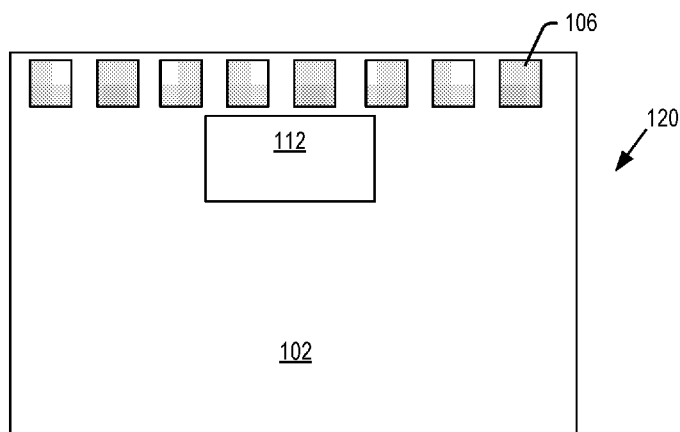
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## (54) Title: BIFURCATED MEMORY DIE MODULE SEMICONDUCTOR DEVICE

Fig. 5



(57) Abstract: A semiconductor device is disclosed including one or more integrated memory modules. Each integrated memory module may include a pair of semiconductor die, which together, operate as a single, integrated memory. In one example, the first die may include the memory cell array and the second die may include the logic circuit such as CMOS integrated circuits. In one example, the first die may be flip-chip bonded to the second die.



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## **BIFURCATED MEMORY DIE MODULE SEMICONDUCTOR DEVICE**

### **BACKGROUND**

**[0001]** The strong growth in demand for portable consumer electronics is driving the need for high-capacity storage devices. Non-volatile semiconductor memory devices, such as flash memory storage cards, are widely used to meet the ever-growing demands on digital information storage and exchange. Their portability, versatility and rugged design, along with their high reliability and large capacity, have made such memory devices ideal for use in a wide variety of electronic devices, including for example digital cameras, digital music players, video game consoles, PDAs and cellular telephones.

**[0002]** Recently, ultra high density memory devices have been proposed using a 3D stacked memory structure having strings of memory cells formed into layers. One such storage device is sometimes referred to as a Bit Cost Scalable (BiCS) architecture. In addition to the layered memory cells, 3D memory devices include a logic circuit for controlling read/write to the memory cells. The logic circuit, often fabricated using complementary metal–oxide–semiconductor (CMOS) technology, may typically be formed beneath stacked memory layers within a semiconductor wafer.

**[0003]** As the number of memory layers in 3D memory structures increases to meet ever growing memory demands, it is becoming harder to position the logic circuit beneath the 3D memory cell structure. Additionally, it is known to anneal the 3D memory cell structure with heat. While advantageous for the memory cell structure, the heat can adversely affect the operation of the logic circuit.

### **DESCRIPTION OF THE DRAWINGS**

**[0004]** FIGURE 1 is a flowchart for forming a semiconductor die device according to embodiments of the present technology.

**[0005]** FIGURE 2 is a top view of a first major surface of a first semiconductor wafer, and a first semiconductor die therefrom, according to embodiments of the present technology.

**[0006]** FIGURE 3 is a top view of a first major surface of a second semiconductor wafer, and a second semiconductor die therefrom, according to embodiments of the present technology.

**[0007]** FIGURE 4 is a top view showing assembly of the first and second semiconductor die into an integrated memory module according to embodiments of the present technology.

**[0008]** FIGURE 5 is a top view of a completed integrated memory module according to embodiments of the present technology.

**[0009]** FIGURES 6 and 7 are cross-sectional edge and top views showing an integrated memory module according to embodiments of the present technology.

**[0010]** FIGURE 8 is a functional block diagram of an integrated memory module coupled to a host device via a controller according to embodiments of the present technology.

**[0011]** FIGURE 9 is an edge view of a portion of a semiconductor device including a number of stacked integrated memory modules according to embodiments of the present technology.

**[0012]** FIGURE 10 is an edge view of a portion of a semiconductor device including a number of stacked and wire bonded integrated memory modules according to embodiments of the present technology.

**[0013]** FIGURE 11 is a perspective view of a portion of a semiconductor device including a number of stacked and wire bonded integrated memory modules according to embodiments of the present technology.

**[0014]** FIGURE 12 is an edge view of a completed semiconductor device including a number of stacked and wire bonded integrated memory modules according to embodiments of the present technology.

**[0015]** FIGURES 13-15 are perspective views of semiconductor devices according to alternative embodiments of the present technology.

**[0016]** FIGURES 16-19 are top and edge views of integrated memory modules according to alternative embodiments of the present technology.

**[0017]** FIGURES 20-21 are edge views of semiconductor devices according to further alternative embodiments of the present technology.

[0018] FIGURE 22 is a flowchart for forming a semiconductor device according to embodiments of the present technology.

[0019] FIGURE 23 is a top view of a first major surface of a first semiconductor wafer, and a first semiconductor die therefrom, according to embodiments of the present technology.

[0020] FIGURE 24 is a top view of a first major surface of a second semiconductor wafer, and a second semiconductor die therefrom, according to embodiments of the present technology.

[0021] FIGURES 25-27 are edge views of a second semiconductor die during fabrication according to embodiments of the present technology.

[0022] FIGURE 28 and 28A are edge views of a second semiconductor die including connective metal bumps according an alternative embodiment of the present technology.

[0023] FIGURE 29 is a top view showing assembly of the first and second semiconductor die into an integrated memory module according to embodiments of the present technology.

[0024] FIGURE 30 is a top view of a completed integrated memory module according to embodiments of the present technology.

[0025] FIGURES 31 and 32 are cross-sectional edge and edge views showing an integrated memory module according to embodiments of the present technology.

[0026] FIGURES 33-41 are perspective, top and edge views of a semiconductor device including a number of stacked integrated memory modules during fabrication according to embodiments of the present technology.

[0027] FIGURES 42-45 are perspective and edge views of a semiconductor device including a number of stacked integrated memory modules during fabrication according to alternative embodiments of the present technology.

[0028] FIGURE 46 is an edge view of a semiconductor device including a number of stacked integrated memory modules during fabrication according to a further alternative embodiment of the present technology.

[0029] FIGURE 47 is an edge view of a semiconductor device including a number of stacked integrated memory modules during fabrication according to another alternative embodiment of the present technology.

**[0030]** FIGURE 48 is an edge view of a semiconductor device including a number of stacked integrated memory modules during fabrication according to a further alternative embodiment of the present technology.

**[0031]** FIGURE 49 is a flowchart for forming a semiconductor device according to embodiments of the present technology.

**[0032]** FIGURE 50 is a flowchart showing additional detail step 2214 in Fig. 49.

**[0033]** FIGURE 51 is a top view of a first major surface of a first semiconductor wafer, and a first semiconductor die therefrom, according to embodiments of the present technology.

**[0034]** FIGURE 52 is a top view of a first major surface of a second semiconductor wafer, and a second semiconductor die therefrom, according to embodiments of the present technology.

**[0035]** FIGURES 53 and 53A are edge views of first and second semiconductor dies including connective metal bumps according to embodiments of the present technology.

**[0036]** FIGURES 54 and 55 are edge views of first and second semiconductor dies affixed to each other according to embodiments of the present technology.

**[0037]** FIGURE 56 is a perspective view of an integrated memory module including the first and second semiconductor dies according to embodiments of the present technology.

**[0038]** FIGURE 57 is a cross-sectional edge view showing an integrated memory module according to embodiments of the present technology.

**[0039]** FIGURES 58-74 are edge and perspective views of a semiconductor device including a number of stacked integrated memory modules during fabrication according to embodiments of the present technology.

**[0040]** FIGURE 75 is a flowchart for forming a semiconductor device according to embodiments of the present technology.

**[0041]** FIGURE 76 is a top view of a first major surface of a first semiconductor wafer, and a first semiconductor die therefrom, according to embodiments of the present technology.

**[0042]** FIGURE 77 is a top view of a first major surface of a second semiconductor wafer, and a second semiconductor die therefrom, according to embodiments of the present technology.

[0043] FIGURE 78 is a cross-sectional edge view of a first semiconductor die including through-silicon vias.

[0044] FIGURE 79 is a cross-sectional edge view of the first semiconductor die shown in Fig. 78, and further including bond pads on the through-silicon vias on upper and lower surfaces of the first semiconductor die.

[0045] FIGURE 80 is a cross-sectional edge view of a second semiconductor die including through-silicon vias.

[0046] FIGURE 81 is a cross-sectional edge view of the second semiconductor die shown in Fig. 80, and further including bond pads on the through-silicon vias on an upper surface of the second semiconductor die.

[0047] FIGURE 82 is an exploded edge view of an integrated memory module mounted on a carrier.

[0048] FIGURES 83-86 are edge views of a number of semiconductor devices on a carrier during fabrication according to embodiments of the present technology.

[0049] FIGURES 87-89 are edge views of a number of semiconductor devices including individual first semiconductor dies mounted on a wafer of second semiconductor dies during fabrication according to embodiments of the present technology.

[0050] FIGURES 90-92 are edge views of a number of semiconductor devices including one or more wafers of first semiconductor dies mounted on a wafer of second semiconductor dies during fabrication according to embodiments of the present technology.

[0051] FIGURES 93-95 are edge views of a number of semiconductor devices including individual first semiconductor dies mounted on a wafer of second semiconductor dies and a carrier during fabrication according to embodiments of the present technology.

#### DETAILED DESCRIPTION

[0052] The present technology will now be described with reference to the figures, which in embodiments, relate to a semiconductor device including one or more integrated memory modules. Each integrated memory module may include a pair of semiconductor die, which together, operate as a single, integrated memory. The division of the memory functionality between the pair of die in the module may vary in embodiments, but in one example, the first

die may include the memory cell array and the second die may include the logic circuit such as CMOS integrated circuits.

**[0053]** In embodiments, the second semiconductor die of the integrated memory module may be smaller than the first die, and may be flip-chip bonded to a surface of the first die, adjacent a row of die bond pads on the first die. With such a configuration, a number of such integrated memory modules may be stacked on top of each other in an offset stepped configuration in such a way that the second die of each integrated memory module does not factor into an overall height of the stack.

**[0054]** It is understood that the present invention may be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the invention to those skilled in the art. Indeed, the invention is intended to cover alternatives, modifications and equivalents of these embodiments, which are included within the scope and spirit of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be clear to those of ordinary skill in the art that the present invention may be practiced without such specific details.

**[0055]** The terms “top” and “bottom,” “upper” and “lower” and “vertical” and “horizontal,” and forms thereof, as may be used herein are by way of example and illustrative purposes only, and are not meant to limit the description of the technology inasmuch as the referenced item can be exchanged in position and orientation. Also, as used herein, the terms “substantially” and/or “about” mean that the specified dimension or parameter may be varied within an acceptable manufacturing tolerance for a given application. In one embodiment, the acceptable manufacturing tolerance is  $\pm 2.5\%$  of a given dimension.

**[0056]** An embodiment of the present technology will now be explained with reference to the flowchart of Fig. 1, and the views of Figs. 2-21. In step 200, a first semiconductor wafer 100 may be processed into a number of first semiconductor dies 102 as shown in Fig. 2. The first semiconductor wafer 100 may start as an ingot of wafer material which may be monocrystalline silicon grown according to either a Czochralski (CZ) or floating zone (FZ) process. However, first wafer 100 may be formed of other materials and by other processes in further embodiments.

**[0057]** The semiconductor wafer 100 may be cut from the ingot and polished on both the first major surface 104, and second major surface (not shown) opposite surface 104, to provide smooth surfaces. The first major surface 104 may undergo various processing steps to divide the wafer 100 into the respective first semiconductor dies 102, and to form integrated circuits of the respective first semiconductor dies 102 on and/or in the first major surface 104. These various processing steps may include metallization steps depositing metal contacts including die bond pads 106 and flip-chip bond pads 108 exposed on the first major surface 104. The metallization steps may further include depositing metal interconnect layers and vias within the wafer. These metal interconnect layers and vias may be provided for transferring signals to and from the integrated circuits, and to provide structural support to the integrated circuits as explained below with respect to Figs. 6-7.

**[0058]** The number of first semiconductor dies 102 shown on wafer 100 in Fig. 2 is for illustrative purposes, and wafer 100 may include more first semiconductor dies 102 than are shown in further embodiments. Similarly, the number of bond pads 106, 108 on the first semiconductor die 102 are shown for illustrative purposes, and each first die 102 may include more bond pads 106, 108 than are shown in further embodiments.

**[0059]** In one embodiment, the first semiconductor dies 102 may be processed to include integrated circuit memory cells, such as for example one or more 3D stacked memory cell arrays having strings of NAND memory. The first semiconductor dies 102 may include other and/or additional circuits in further embodiments as explained below.

**[0060]** Before, after or in parallel with the formation of the first semiconductor dies on wafer 100, a second semiconductor wafer 110 may be processed into a number of second semiconductor dies 112 in step 202 as shown in Fig. 3. The semiconductor wafer 110 may start as an ingot of monocrystalline silicon grown according to either a CZ, FZ or other process. The second semiconductor wafer 110 may be cut and polished on both the first major surface 114, and second major surface (not shown) opposite surface 114, to provide smooth surfaces. The first major surface 114 may undergo various processing steps to divide the second wafer 110 into the respective second semiconductor dies 112, and to form integrated circuits of the respective second semiconductor dies 112 on and/or in the first major surface 114. These various processing steps may include metallization steps depositing metal contacts including flip-chip bond pads 118 exposed on the first major surface 114. The metallization steps may further include depositing metal interconnect layers and vias within the wafer. These metal

interconnect layers and vias may be provided for transferring signals to and from the integrated circuits as explained below with respect to Figs. 6-7.

**[0061]** The number of second semiconductor dies 112 shown on wafer 110 in Fig. 3 is for illustrative purposes, and wafer 110 may include more second semiconductor dies 112 than are shown in further embodiments. Similarly, the number of flip-chip bond pads 118 on the second semiconductor die 112 is shown for illustrative purposes, and each second die 112 may include more bond pads 118 than are shown in further embodiments.

**[0062]** In one embodiment, the second semiconductor dies 112 may be processed to include integrated logic circuits, configured to control read/write operations for one or more integrated memory cell arrays. The logic circuits may be fabricated using CMOS technology, though the logic circuits may be fabricated using other technologies in further embodiments. The second semiconductor dies 112 may include other and/or additional circuits in further embodiments as explained below.

**[0063]** In step 204, first semiconductor dies 102 diced from wafer 100 and second semiconductor dies diced from wafer 110 may be physically and electrically coupled to each other as shown in Figs. 4 and 5. In one embodiment, the pattern of flip-chip bond pads 108 on first semiconductor die 102 may match the pattern of flip-chip bond pads 118 on second semiconductor die 112 as shown in Fig. 4. The particular patterns of bond pads 108, 118 shown in Fig. 4 is by way of example only and may vary in further embodiments. The second semiconductor die 112 may be flipped over, and respective bond pads 118 may be physically and electrically coupled to respective bond pads 108 using heat and pressure to reflow a solder bump 146 (Fig. 6) at each bond pad interface.

**[0064]** Once coupled together, the first and second semiconductor dies 102, 112 together form an integrated memory module 120 as shown in Fig. 5. In accordance with aspects of the present technology, the integrated memory module 120 functions as a single, complete memory, such as for example a BiCS flash memory. It is understood that the integrated memory module 120 may function as other types of flash memory, including 2D memories and other 3D memories, as well as other types of memories. Such other types of memories include, but are not limited to, Magnetic RAM, Resistive RAM, Phase-change RAM, etc.

**[0065]** Forming the integrated memory module 120 from two separate semiconductor dies has several advantages over conventional memory dies formed of a single die. For example, where the first die 102 includes a memory cell array, removal of the logic circuit from the first

die frees up valuable space for additional memory cells. For example, if memory cells and logic circuits are made on a wafer in “side-by-side” configuration, removal of the logic circuit allows additional area to be provided for the memory stack.

**[0066]** Moreover, separation of the memory cells and the logic circuits into two separate wafers allows the fabrication processes for both wafers to be customized and optimized for the particular integrated circuits formed on the respective wafers. For example, conventional processes for forming flash memory integrated circuits involved a heat step which could be detrimental to the CMOS logic circuits. By fabricating the logic circuits on their own wafer, this problem may be alleviated.

**[0067]** Referring again to Fig. 5, the second semiconductor die 112 of integrated memory module 120 may be significantly smaller than the first semiconductor die 102. As such, the overall footprint of the integrated memory module 120 may be determined exclusively by the footprint of the first semiconductor die 102. That is, the size of the second semiconductor die 112 does not increase or otherwise affect the footprint of the integrated memory module 120. As explained below, the relative sizes of the first and second semiconductor dies 102, 112 may vary from that shown in Fig. 5. In one further example, the second semiconductor die 112 may cover the entire surface of the first semiconductor die 102, with the exception that the die bond pads 106 of the first semiconductor die 102 be left exposed and uncovered by the second semiconductor die 112.

**[0068]** In the embodiments shown in Figs. 4-5, the first and second semiconductor dies 102, 112 include a pattern of bond pads for flip-chip bonding of the dies. It is understood that the first and second semiconductor dies 102, 112 may be electrically coupled to each other using other schemes in further embodiments. In one such further embodiment, the first and second semiconductor dies 102, 112 may be electrically coupled to each other using through-silicon vias (TSV). In another such embodiment, the first and second semiconductor dies 102, 112 may be wire bonded to each other. The flip-chip bond pads 108, 118 may be omitted in such alternative embodiments.

**[0069]** Additional details relating to the physical and electrical coupling of the first and second semiconductor dies 102, 112 will now be explained with reference to the cross-sectional edge view and top view of Figs. 6 and 7, respectively. First semiconductor die 102 may include memory cell array 122 formed in and/or on a substrate layer 124 within a chip region of the semiconductor die 102. As noted, the memory cell array 122 may be formed as a 3D stacked

memory structure having strings of memory cells formed into layers. After formation of the memory cell array 122, multiple layers of metal interconnects 126 and vias 128 may be formed sequentially in layers of a dielectric film 130. As is known in the art, the metal interconnects 126, vias 128 and dielectric film layers 130 may be formed a layer at a time using photolithographic and thin-film deposition processes. The photolithographic processes may include for example pattern definition, plasma, chemical or dry etching and polishing. The thin-film deposition processes may include for example sputtering and/or chemical vapor deposition. The metal interconnects 126 may be formed of a variety of electrically conductive metals including for example copper and copper alloys as is known in the art, and the vias 128 may be lined and/or filled with a variety of electrically conductive metals including for example tungsten, copper and copper alloys as is known in the art.

**[0070]** A passivation layer 132 may be formed on top of the upper dielectric film layer 130. The passivation layer 132 may be etched to form the bond pads 106, 108. Each bond pad 106, 108 may include a contact layer 134 formed over a liner 136. As is known in the art, the contact layer 134 may be formed for example of copper, aluminum and alloys thereof, and the liner 136 may be formed for example of a titanium/titanium nitride stack such as for example Ti/TiN/Ti, though these materials may vary in further embodiments. The bond pads 106, 108 (contact layer plus liner) may have a thickness of 720 nm, though this thickness may be larger or smaller in further embodiments.

**[0071]** The metal interconnects 126 and vias 128 may be used to form conductive nodes 140 as is known in the art within the chip region for transferring signals and voltages between the die bond pads 108 and integrated circuits 122. In accordance with aspects of the present technology, metal interconnects 126 may be used to electrically interconnect die on bond pads 106 with a first group of the flip-chip bond pads 108 (bond pads 108a in Fig. 6). Thus, as explained below, signals, for example from a memory controller, may be transferred to/from the second semiconductor die 112 via the die bond pads 106 and the first group of flip-chip bond pads 108a on first die 102. Signals may also be transferred between the first die 102 and second die 112 via a second group of flip-chip bond pads (bond pads 108b in Fig. 6). While Fig. 6 shows the die bond pads 106 electrically interconnected with single row of flip-chip bond pads 108a, it is conceivable that the die bond pads 106 be electrically interconnected with more than one row of flip-chip bond pads 108a, or less than an entire row of flip-chip bond pads 108a.

**[0072]** The metal interconnects 126 and vias 128 may also be used to form a seal ring 142 as is known in the art within a seal ring area. The seal ring 142 may surround the integrated circuits 122 and conductive nodes 140, and provide mechanical support to prevent damage to the integrated circuits 122 and conductive nodes 140 for example during dicing of the wafer 100.

**[0073]** Although shown without detail, the second semiconductor die 112 may be formed in a similar way to include integrated circuits (though, in examples, substituting the logic circuit for the memory cell array). As with first dies 102, the integrated circuits in second die 112 may be electrically interconnected with the flip-chip bond pads 118 of the second die 112 via a framework of metal interconnects and vias.

**[0074]** Fig. 7 shows a further top view of an integrated memory module 120 including the first and second dies 102, 112. In embodiments where the first die 102 includes integrated circuits 122 configured as memory cell arrays, the second semiconductor die 112 may overlie portions of the memory cell arrays in integrated memory module 120.

**[0075]** As noted, in embodiments the first semiconductor die 102 may include memory cell arrays and the second semiconductor die 112 may include control logic circuitry so that the integrated memory module 120 may function as a single, complete memory. In accordance with aspects of the present technology, the memory is bifurcated into two separate semiconductor die which are assembled together. Fig. 8 is a functional block diagram showing further detail of an embodiment where the first die includes memory cell arrays and the second die 112 includes a logic circuit.

**[0076]** The first die 102 of the integrated memory module 120 may include a memory structure 160 of memory cells, such as an array of memory cells, and read/write circuits 168. The second die 112 may include control logic circuitry 150. The memory structure 160 is addressable by word lines via a row decoder 164 and by bit lines via a column decoder 166. The read/write circuits 168 may include multiple sense blocks (sensing circuitry) that allow a page of memory cells to be read or programmed in parallel.

**[0077]** Multiple memory elements in memory structure 160 may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory systems in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND string is an example of a set of series-connected transistors comprising memory cells and select gate transistors.

**[0078]** A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a string is composed of multiple memory elements sharing a single bit line and accessed as a group. Alternatively, memory elements of memory structure 160 may be configured so that each element is individually accessible, e.g., a NOR memory array. NAND and NOR memory configurations are exemplary, and memory elements may be otherwise configured.

**[0079]** The memory structure 160 can be two-dimensional (2D) or three-dimensional (3D). The memory structure 160 may comprise one or more arrays of memory elements (also referred to as memory cells). A 3D memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three dimensions (i.e., in the x, y and z directions, where the z direction is substantially perpendicular and the x and y directions are substantially parallel to the major surface of the substrate 124, Fig. 6).

**[0080]** The memory structure 160 on the first die 102 may be controlled by control logic circuit 150 on the second die 112. The control logic circuit 150 may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. The control circuitry 150 cooperates with the read/write circuits 168 to perform memory operations on the memory structure 160. In embodiments, control circuitry 150 may include a state machine 152, an on-chip address decoder 154, and a power control module 156. The state machine 152 provides chip-level control of memory operations. A storage region 153 may be provided for operating the memory structure 160 such as programming parameters for different rows or other groups of memory cells. These programming parameters could include bit line voltages and verify voltages.

**[0081]** The on-chip address decoder 154 provides an address interface between that used by the host device or the memory controller (explained below) to the hardware address used by the decoders 164 and 166. The power control module 156 controls the power and voltages supplied to the word lines and bit lines during memory operations. It can include drivers for word line layers in a 3D configuration, source side select gates, drain side select gates and source lines. A source side select gate is a gate transistor at a source-end of a NAND string, and a drain side select gate is a transistor at a drain-end of a NAND string.

**[0082]** In accordance with aspects of the present technology, the above-described components of integrated memory module 170 are bifurcated into two separate semiconductor dies 102 and 112, one example of which dies 102, 112 are shown in Fig. 8. However, it is

understood that the division of the above-described components between the two different dies 102, 112 may vary from that shown in Fig. 8. Some or all of the components shown and described above as being part of die 102 may be provided on die 112, while some or all of the components shown and described above as being part of die 112 may be provided on die 102. Additional components may be added to either die 102 or die 112 in further embodiments. In embodiments, the control logic circuit 150 may include the components shown in Fig. 8 and described above. In further embodiments, all components other than the memory cells 160 can be thought of as one or more control logic circuits which are configured to perform the actions described herein. For example, one or more control logic circuits may include any one of, or a combination of, control circuitry 150, state machine 152, decoders 154/164/166, power control module 156, the sense blocks of read/write circuits and so forth.

**[0083]** Data and commands may be transferred to and from the integrated circuit module 120 by a memory controller 170. The memory controller 170 may for example comprise an ASIC, and may be processed on a semiconductor die that is separate from dies 102 and 112. In further embodiments, the memory controller 170 may be incorporated into one of the dies 102, 112, such as for example on die 112. The memory controller 170 may comprise a processor such as a microprocessor 170c, and storage devices (memory) such as read only memory (ROM) 170a and RAM 170b. RAM 170b may be, but is not limited to, SRAM and DRAM. The storage devices comprise code such as a set of instructions, and the processor is operable to execute the set of instructions to provide the functionality described herein. Alternatively or additionally, the processor can access code from a storage device region of the memory structure 160, such as a reserved area of memory cells in one or more word lines.

**[0084]** The code is used by the memory controller 170 to access the memory structure 160 such as for programming, read and erase operations. The code can include boot code and control code (e.g., a set of instructions). The boot code is software that initializes the memory controller 170 during a booting or startup process and enables the memory controller to access the memory structure 160. Upon being powered up, the processor 170c fetches the boot code from the ROM 170a or the storage device region of memory structure 160 for execution, and the boot code initializes the system components and loads the control code into the RAM 170b. Once the control code is loaded into the RAM 170b, it is executed by the processor 170c. The control code includes drivers to perform basic tasks such as controlling and allocating memory, prioritizing the processing of instructions, and controlling input and output ports.

**[0085]** The memory controller 170 controls communication between the integrated memory module 120 and a host device 174. The host device may for example be a printed circuit board to which the integrated memory module 120 and/or memory controller 162 are mounted. The host device may alternatively be a computing system. Commands and data are transferred between the host device 174 and memory controller 170 via an interface (e.g., data bus) 172 and between the memory controller and the integrated memory module 120 via line 158. The interface 172 between the host device 174 and the memory controller 170 may comprise a Peripheral Component Interconnect Express (PCIe) bus, but the interface 172 is not limited to a PCIe bus.

**[0086]** Referring again to Fig. 1, after the first and second dies 102, 112 are formed and coupled to each other to form integrated memory module 120, the memory module 120 may be tested in step 208 as is known, for example with read/write and burn in operations.

**[0087]** In step 212, two or more integrated memory modules may be stacked on a substrate 180 as shown in the edge view of Fig. 9. The substrate may be any of various chip-carrying media including conductive pads, electrical traces and vias for transferring data and commands between the stacked integrated memory modules 120 and a host device such as host device 174 described above. Such chip carrier media may include but are not limited to a printed circuit board (PCB), a leadframe or a tape automated bonded (TAB) tape. Passive components (not shown) may be mounted to the substrate either before or after the integrated memory modules 120. The passive components may include for example one or more capacitors, resistors and/or inductors, though other components are contemplated.

**[0088]** The integrated memory modules 120 may be mounted on each other in the z-direction so as to form a die stack 182 on the substrate 180 as shown in the edge view of Fig. 9. While 4 memory modules 120 are shown in the figures, there may be 1, 2, 4, 8, 16, 32, 64 or other numbers of memory modules 120 in different embodiments. Once electrically interconnected and encapsulated as explained below, the substrate 180 and die stack 182 may form a completed semiconductor device 190.

**[0089]** In accordance with aspects of the present technology, the integrated memory modules 120 may be stacked on each other in such a way that the second die 112 of each module 120 does not add to or otherwise affect the overall height required in the semiconductor device 190 for the die stack 182. In particular, the integrated memory modules 120 may be mounted on each other in stack 182 in an offset stepped configuration where the first

semiconductor die 102 of a memory module 120 is affixed directly to the first semiconductor die 102 of the memory module 120 immediately below it.

**[0090]** The memory modules 120 may be offset spaced from each other in the y-direction a distance so that the first die 102 of a stacked memory module sits next to the second die 112 of a memory module immediately below it. That is, where an upper memory module 120 is mounted on a lower memory module 120, both the upper memory module 120 and the second die 112 of the lower memory module 120 are mounted directly to the surface of the first die 102 of the lower memory module 120. The second die 112 may have a thickness that is less than or equal to the first die 102. Thus, the second die 112 of each module 120 does not add to the overall height required in the semiconductor device 190 for the die stack 182. The memory modules 120 may be stacked on each other using a die attach film (DAF) on a bottom surface of each of the first die 102.

**[0091]** The second die 112 of the lower memory module may sit between, and be slightly spaced in the y-direction from, the die bond pads 106 in the lower memory module and the upper memory module mounted thereon. In one embodiment, a second die 112 may be spaced 20 $\mu$ m to 50 $\mu$ m from the adjacent die bond pads 106, and 20 $\mu$ m to 50 $\mu$ m from the first die 102 of the next module 120 stacked thereon. These distances are by way of example and may vary in further embodiments.

**[0092]** Once the die stack 182 is formed, the die stack 182 may be electrically coupled to each other and the substrate 180 in a step 214. As shown in the edge view of Fig. 10 and the perspective view of Fig. 11, wire bonds 192 may be formed down the stepped edge of the die stack 182, between aligned die bond pads 106 on the first dies 102 of the integrated memory modules 120 in stack 182. Wire bonds 192 may also be used to electrically connect the die stack 182 to the contact pads 194 on substrate 180. Wire bonds may be used to electrically connect the aligned die bond pads 106 on respective memory modules 120 to each other and to substrate 180, thus allowing signal transfer between the substrate and the memory modules 120 in stack 182.

**[0093]** As seen in Figs. 10 and 11, it is a feature of the present technology that the wire bonds may extend between contact pads 106 at different levels over the second die 112 in each module 120 (except the top module). Thus, the second dies 112 may be provided in a space that is otherwise unused.

**[0094]** In one embodiment, the wire bonds 192 may be formed using ball bonds, though other types of bonds are contemplated. The wire bonds 192 may be formed of gold, gold alloy or other materials. The wire bonds 130 are shown generally in a straight vertical column from one layer of die to the next in the die stack 182, and to the substrate 180. However, one or more of the wire bonds may extend diagonally from one die to the next in alternative embodiments. Further, it may be that a wire bond skips one or more layers in the die stack 182. The number of wire bonds 192 shown in Fig. 11 is by way of example only, and there may be more wire bonds in further embodiments.

**[0095]** After the wire bonds 192 are formed, the semiconductor device 190 may be encapsulated in a mold compound 196 in step 216 and as shown in Fig. 12. Mold compound 196 may include for example solid epoxy resin, Phenol resin, fused silica, crystalline silica, carbon black and/or metal hydroxide. Such mold compounds are available for example from Sumitomo Corp. and Nitto-Denko Corp., both having headquarters in Japan. Other mold compounds from other manufacturers are contemplated. The mold compound may be applied by a FFT (Flow Free Thin) process or by other known processes, including by transfer molding or injection molding techniques.

**[0096]** In step 220, solder balls 198 (Fig. 12) may optionally be affixed to the contact pads 194 on a lower surface of substrate 180 of the semiconductor device 190. The solder balls 198 may be used to affix the semiconductor device 190 to a host device 174 (Fig. 8) such as a printed circuit board. Solder balls 198 may be omitted where the semiconductor device 190 is to be used as an LGA package.

**[0097]** In order to take advantage of economies of scale, multiple semiconductor devices 190 may be formed simultaneously on a panel of substrates 180. After formation and encapsulation of the devices 190 on the panel, the devices 190 may be singulated from each other in step 224 to form a finished semiconductor device 190 as shown in Fig. 12. The semiconductor devices 190 may be singulated by any of a variety of cutting methods including sawing, water jet cutting, laser cutting, water guided laser cutting, dry media cutting, and diamond coating wire cutting. While straight line cuts will define generally rectangular or square shaped semiconductor devices 190, it is understood that semiconductor device 190 may have shapes other than rectangular and square in further embodiments of the present technology.

**[0098]** In the embodiments described above, the die stack 182 may be stepped in a single direction. Fig. 13 shows an alternative embodiment, where the die stack 182 includes a first group of integrated memory modules 120 offset in a first stepped direction and a second group of integrated memory modules 120 offset in a second stepped direction opposite the first stepped direction. While the first and second groups are shown as including four memory modules 120 each, there may be fewer or greater than four memory modules 120 in the first and/or second groups. Both groups of integrated memory modules 120 may be coupled to each other and the substrate as shown using wire bonds 192. The memory modules 120 in the first and second groups are mounted so that the first die 102 of each memory module is stacked on the first die 102 of the memory module immediately below it.

**[0099]** In embodiments described above, the second die 112 and the first die 102 of the next higher memory module 120 are both affixed to the first die 102 of the lower memory module 120. However, other configurations of die in die stack 182 are contemplated. Fig. 14 shows one further embodiment where memory modules are stacked on top of each other such that the first die 102 is mounted on top of the second die 112 of the next lower memory module 120.

**[00100]** In the embodiment of Fig. 14, spacers 250 may be provided next to the second die 112 of all memory modules except the top memory module 120 in the stack 182. The spacers 250 may be formed of a gel or film, or may be a dielectric solid such as silicon dioxide. The memory modules 120 may be stacked in an offset stepped configuration. However, as there is no need to leave space for the second die 112, the offset in this embodiment may be smaller than in the embodiments described for example with respect to Figs. 10 and 11. The offset may be large enough to expose the die bond pads 106 on the first die 102 of each memory module 120.

**[00101]** In embodiments described above, multiple integrated circuit modules 120 were mounted on each other to form the die stack 182. In further embodiments, die other than integrated circuit modules 120 may be included in stack 182. For example, Fig. 15 shows an embodiment where stack 182 comprises an integrated circuit module 120, and then additional individual semiconductor dies, which in embodiments may be first dies 102 including memory cell arrays. In this embodiment, the single second die 112 shown may include a logic circuit which controls the transfer of data and commands to/from just its associated first die 102, or each of the first dies 102 shown in the die stack 182.

**[00102]** In the embodiment of Fig. 15, the die 102 mounted on the memory module 120 may be offset by an amount to leave space for the die bond pads 106 and second die 112 as described above. The remaining dies 102 may be offset on the bottom individual first die 102 by an amount to leave space for the die bond pads 106. The embodiment shown includes one integrated memory module 120 and three individual first dies 102. However, it is understood that there may be multiple integrated memory modules 120 mixed with one or more other individual semiconductor die. The integrated memory module(s) 120 need not be on the bottom of the stack 182 in further embodiments.

**[00103]** As noted above, the sizes of the first and second dies 102, 112 may vary with respect to each other. Fig. 5 shows an example where the length and width of the second die 112 are significantly smaller than the first die 102. Fig. 16 shows a further example where a length of the second die 112 is the only slightly smaller than the length of the first die 102. The second semiconductor 112 die may have the same length as the first semiconductor die 102 in further embodiments.

**[00104]** Fig. 17 shows a further embodiment where multiple smaller second die 112 are mounted on the surface of the first die 102. The example shows four such second dies 112, but there may be more or less than four second dies 112 in further embodiments. It is conceivable that the multiple second dies 112 shown in Fig. 17 be used to control transfer of data and commands to the multiple first die 102 shown in the embodiment of Fig. 15.

**[00105]** Figs. 18 and 19 show top and edge views of a further embodiment of the present technology where bond pads 106 on die 102 are omitted. In this embodiment, a pattern of die bond pads 258 are provided on a top surface of the second die 112. These bond pads 258 may be electrically connected to the pattern of die bond pads 118 on the opposite side of the second die 112 by TSVs 260. The bond pads 118 may be flip-chip bonded to bond pads 108 on the first die 102 as described above. The particular pattern of bond pads 258 are by way of example only, and may vary in further embodiments.

**[00106]** Fig. 20 shows an edge view of an example of a semiconductor device 190 including a number of stacked integrated memory modules 120 including second dies 112 with TSVs 260 as shown in Figs. 18 and 19. The memory modules 120 of Fig. 20 may be electrically interconnected to each other and the substrate 180 using the die bond pads 258 on the second dies 112 of each memory module 120. The die bond pads 258 provide access to both the first

and second dies 102, 112 in each memory module 120, as well as electrically interconnecting the memory modules 120 to each other and the substrate 180.

**[00107]** Fig. 21 shows an edge view of a semiconductor device 190 similar to that of Fig. 20, but the embodiment of Fig. 21 includes a single memory module 120 having a second die 112 with TSVs 260 as shown in Figs. 18 and 19. The remaining semiconductor die in the device 190 of Fig. 21 are individual semiconductor dies, which in embodiments may be first dies 102 including memory cell arrays. In this embodiment, the single second die 112 shown may include a logic circuit which controls the transfer of data and commands to/from just its associated first die 102, or each of the first dies 102 shown in the die stack 182.

**[00108]** In the embodiment of Fig. 21, the die 102 mounted on the memory module 120 may be offset by an amount sufficient to leave space for second die 112. The remaining dies 102 may be offset on the bottom individual first die 102 by an amount to leave space for the die bond pads 106. The embodiment shown includes one integrated memory module 120 and three individual first dies 102. However, it is understood that there may be multiple integrated memory modules 120 mixed with one or more other individual semiconductor die. The integrated memory module(s) 120 need not be on the bottom of the stack 182 in further embodiments.

**[00109]** In summary, an example of the present technology relates to an integrated memory module comprising: a first semiconductor die; a second semiconductor die flip-chip bonded to a surface of the first semiconductor die to electrically and physically couple the second semiconductor die to the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated memory.

**[00110]** The integrated memory module of above, wherein the first semiconductor die comprises a plurality of memory cells.

**[00111]** The integrated memory module of above, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.

**[00112]** The integrated memory module of above, wherein the control circuit comprises a complementary metal-oxide-semiconductor integrated circuit.

**[00113]** The integrated memory module of above, wherein the first and second dies together are configured as a nonvolatile memory device.

**[00114]** The integrated memory module of above, wherein the nonvolatile memory device comprises one of a NAND flash memory device, a Magnetic random access memory (RAM) device, a Phase Change RAM device and a resistive RAM device.

**[00115]** The integrated memory module of above, wherein the first semiconductor die comprises a plurality of bonding pads configured to wire bond the first semiconductor die.

**[00116]** The integrated memory module of above, wherein the integrated memory module has a footprint equal to a footprint of the first semiconductor die.

**[00117]** The integrated memory module of above, wherein the second semiconductor die is smaller than the first semiconductor die.

**[00118]** The integrated memory module of above, wherein the second semiconductor die includes a first group of bond pads, on a first surface of the second semiconductor die adjacent the first semiconductor die, for flip-chip bonding of the second semiconductor die to the first semiconductor die.

**[00119]** The integrated memory module of above, further comprising a second set of bond pads on a second surface of the first semiconductor die opposite the first surface.

**[00120]** In another example, the present technology relates to a semiconductor device, comprising: a substrate; a first integrated memory module affixed to the substrate, comprising: a first semiconductor die including a surface having a plurality of die bond pads; a second semiconductor die bonded to the surface of the first semiconductor die adjacent the plurality of die bond pads; wherein the first and second coupled semiconductor dies together are configured as an integrated memory.

**[00121]** The semiconductor device of above, further comprising a third semiconductor die, mounted on the surface of the first semiconductor die, adjacent the second semiconductor die.

**[00122]** The semiconductor device of above, wherein the third semiconductor die comprises a memory die.

**[00123]** The semiconductor device of above, wherein the third semiconductor die comprises a plurality of memory cells, the semiconductor device further comprising a fourth semiconductor die bonded to the surface of the third semiconductor, wherein the third and fourth coupled semiconductor dies together are configured as an integrated memory.

**[00124]** The semiconductor device of above, wherein the fourth semiconductor die is flip-chip bonded to the third semiconductor die.

**[00125]** The semiconductor device of above, wherein the fourth semiconductor die is electrically connected to the third semiconductor die using through silicon vias.

**[00126]** The semiconductor device of above, further comprising a wire bond extending between a contact pad on the substrate and a die bond pad on the first semiconductor die.

**[00127]** The semiconductor device of above, further comprising a wire bond extending between a contact pad on the substrate and a die bond pad on the second semiconductor die.

**[00128]** In another example, the present technology relates to a semiconductor device, comprising: a substrate; a first integrated memory module affixed to the substrate, comprising: a first semiconductor die including a surface having a first plurality of die bond pads; a second semiconductor die bonded to the surface of the first semiconductor die adjacent the plurality of die bond pads; wherein the first and second coupled semiconductor dies together are configured as an integrated memory; a third semiconductor die, mounted to the first integrated memory module, adjacent the second semiconductor die, the third semiconductor die comprising a second plurality of die bond pads; and wire bonds connected between the first and second pluralities of die bond pads, the wire bonds extending over the second semiconductor die.

**[00129]** The semiconductor device of above, wherein the third semiconductor die is mounted on the first surface of the first semiconductor die.

**[00130]** The semiconductor device of above, wherein the third semiconductor die is mounted on a surface of the second semiconductor die.

**[00131]** The semiconductor device of above, wherein the third semiconductor die comprises a memory die.

**[00132]** The semiconductor device of above, wherein the third semiconductor die comprises a plurality of memory cells, the semiconductor device further comprising a fourth semiconductor die bonded to the surface of the third semiconductor, wherein the third and fourth coupled semiconductor dies together are configured as an integrated memory.

**[00133]** The semiconductor device of above, wherein the fourth semiconductor die is flip-chip bonded to the third semiconductor die.

**[00134]** In another example, the present technology relates to an integrated memory module comprising: a first semiconductor die comprising memory means; a second semiconductor die comprising control means, the second semiconductor die flip-chip bonded to a surface of the first semiconductor die to electrically and physically couple the second semiconductor die to the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated memory.

**[00135]** A further embodiment of the present technology will now be described with reference to Figs. 22-48, which in embodiments, relate to a semiconductor device including stacked integrated memory modules. Each integrated memory module may include a pair of semiconductor die, which together, operate as a single, integrated flash memory. The division of the flash memory functionality between the pair of die in the module may vary in embodiments, but in one example, the first die may include the memory cell array and the second die may include the logic circuit such as CMOS integrated circuits.

**[00136]** In embodiments, the second semiconductor die of the integrated memory module may be smaller than the first semiconductor die, and may be flip-chip bonded to a surface of the first semiconductor die. In one embodiment, the second semiconductor die may be bonded to the first semiconductor die along an edge of the first die. In such embodiments, the integrated memory modules may be stacked in an offset, staggered configuration so that the first dies may be stacked directly on top of each other, leaving the second dies exposed on the edges of the first dies. In another embodiment, the second die may be bonded to a central portion of the first die. In such embodiments, the first dies may include an FOD (film on die) on a bottom surface of the first dies, so that a second die embeds within the film of the first die in the next higher integrated memory module.

**[00137]** An embodiment of the present technology will now be explained with reference to the flowchart of Fig. 22, and the views of Figs. 23-48. In step 1200, a first semiconductor wafer 1110 may be processed into a number of first semiconductor dies 1102 as shown in Fig. 23. The first semiconductor wafer 1110 may start as an ingot of wafer material which may be monocrystalline silicon grown according to either a Czochralski (CZ) or floating zone (FZ) process. However, first wafer 1110 may be formed of other materials and by other processes in further embodiments.

**[00138]** The semiconductor wafer 1110 may be cut from the ingot and polished on both the first major surface 1104, and second major surface (not shown) opposite surface 1104, to provide smooth surfaces. The first major surface 1104 may undergo various processing steps to divide the wafer 1110 into the respective first semiconductor dies 1102, and to form integrated circuits of the respective first semiconductor dies 1102 on and/or in the first major surface 1104. These various processing steps may include metallization steps depositing metal contacts including die bond pads 1106 and flip-chip bond pads 1108 exposed on the first major surface 1104. The metallization steps may further include depositing metal interconnect layers

and vias within the wafer. These metal interconnect layers and vias may be provided for transferring signals to and from the integrated circuits, and to provide structural support to the integrated circuits as explained below with respect to Fig. 31.

**[00139]** The number of first semiconductor dies 1102 shown on wafer 1110 in Fig. 23 is for illustrative purposes, and wafer 1110 may include more first semiconductor dies 1102 than are shown in further embodiments. Similarly, the number of bond pads 1106, 1108 on the first semiconductor die 1102 are shown for illustrative purposes, and each first die 1102 may include more bond pads 1106, 1108 than are shown in further embodiments.

**[00140]** In one embodiment, the first semiconductor dies 1102 may be processed to include integrated circuit memory cells, such as for example one or more 3D stacked memory cell arrays having strings of NAND memory. The first semiconductor dies 1102 may include other and/or additional circuits in further embodiments as explained below.

**[00141]** Before, after or in parallel with the formation of the first semiconductor dies on wafer 1110, a second semiconductor wafer 1110 may be processed into a number of second semiconductor dies 1112 in steps 1202 and 204 as shown in Fig. 24. The semiconductor wafer 1110 may start as an ingot of monocrystalline silicon grown according to either a CZ, FZ or other process. The second semiconductor wafer 1110 may be cut and polished on both the first major surface 1114, and second major surface (not shown) opposite surface 1114, to provide smooth surfaces. The first major surface 1114 may undergo various processing steps to divide the second wafer 1110 into the respective second semiconductor dies 1112, and to form integrated circuits of the respective second semiconductor dies 1112 on and/or in the first major surface 1114. The number of second semiconductor dies 1112 shown on wafer 1110 in Fig. 24 is for illustrative purposes, and wafer 1110 may include more second semiconductor dies 1112 than are shown in further embodiments.

**[00142]** In one embodiment, the second semiconductor dies 1112 may be processed to include integrated logic circuits 1115 (Fig. 25), configured to control read/write operations for one or more integrated memory cell arrays. The logic circuits may be fabricated using CMOS technology, though the logic circuits may be fabricated using other technologies in further embodiments. The second semiconductor dies 1112 may include other and/or additional circuits in further embodiments as explained below. Each logic circuit 1115 may be electrically coupled to a metal pad 1116 on an upper surface of the dies 1112 by metal interconnect layers and/or vias.

**[00143]** As described below, the metal pads 1116 of the logic circuits 1115 get electrically coupled to the bond pads 1108 on the first dies 1102. In embodiments, this is accomplished using a redistribution layer in step 1204 to reposition, or redistribute, the positions of the metal pads 1116 on the second dies 1112 into a pattern matching the pattern of bond pads 1108 on the first dies 1102. Such a redistribution layer (RDL) 1117 is shown in Fig. 26. The pattern of the RDL 1117 shown in Fig. 26 is by way of example only and may vary in further embodiments. It is conceivable that the metal pads 1116 on the second semiconductor die 1116 be arranged in a pattern needed to mate with the contact pads 1108 on the first semiconductor die 1102. In this case, the RDL 1117 may be omitted.

**[00144]** A pattern of bumps 1118 may be formed on the pads on an upper surface of the RDL 1117 as shown in Fig. 27. The bumps 1118 may be formed by a wide variety of techniques, including for example by stud bumping on the second wafer 1110 or using micro-bumps. The bumps 1118 may be formed of various materials, including for example Cu, Cu-Sn, Pb-Sn, Au, alloys thereof, or other solder materials and metals of relatively high melting points. The bumps 1118 are provided in a pattern matching that of the bond pads 1108 on the first dies 1102. In embodiments, the spacing between bumps 1118 may vary between 5microns ( $\mu\text{m}$ ) and 50  $\mu\text{m}$ , though the spacing may be smaller or larger than this in further embodiments.

**[00145]** In embodiments, the bumps 1118 may be cylindrical pillars or spherical balls. However, in further embodiments, the bumps 1118 may be cone-shaped as shown in Fig. 28 and the enlarged view of Fig. 28A. The cone-shaped bumps 1118 may have straight sidewalls to form a true cone, or have sidewalls with a concave portion at the base transitioning into a convex portion at the tip as shown in the figures. Cone-shaped bumps 1118 may be deposited on the RDL pads by first depositing a Ti/Cu seed layer on the pads on the upper surface of the RDL 1117. Next, undercut holes may be formed using a resist pattern over the seed layer by photolithography. The undercut holes in the resist film may then be filled with bump material, for example in an electroplating process. The photoresist and seed layer may then be removed using one or more solvents to leave the cone-shaped bumps 1118.

**[00146]** In embodiments, the cone-shaped bumps 1118 may have a base diameter,  $d_1$ , of 8-10  $\mu\text{m}$ , a tip diameter,  $d_2$ , of 2-3  $\mu\text{m}$ , and a height,  $h$ , of 8-9  $\mu\text{m}$ . However, each of these dimensions may vary in further embodiments, both proportionately and disproportionately to each other. The spacing between the cone-shaped bumps may be about 20  $\mu\text{m}$ , but this spacing may vary in further embodiments. As explained below, the cone-shaped bumps 1118 have

certain advantages with respect to shear strength when the cone-shaped bumps of dies 1112 are ultrasonically bonded to the pads 1108 of dies 1102. However, as noted, the bumps 1118 may be pillars, spherical or other shapes in further embodiments. The number of bumps 1118 on the second semiconductor die 1112 shown in Figs. 24, 27 and 28 is for illustrative purposes, and each second die 1112 may include more bumps 1118 than are shown in further embodiments.

**[00147]** In step 1206, first semiconductor dies 1102 diced from wafer 1110 and second semiconductor dies diced from wafer 1110 may be physically and electrically coupled to each other as shown in Figs. 29 and 30. In embodiments, a second semiconductor die 1112 may be mounted to a major planar surface of a first semiconductor die 1102, at an edge of the major planar surface. As noted, in one embodiment, the pattern of flip-chip bond pads 1108 on first semiconductor die 1102 may match the pattern of bumps 1118 on second semiconductor die 1112 as shown in Fig. 29. The particular patterns of bond pads 1108 and bumps 1118 shown in Fig. 29 is by way of example only and may vary in further embodiments.

**[00148]** In order to affix the first and second dies 1102 and 1112 together, the second semiconductor die 1112 may be flipped over, and respective bumps 1118 may be physically and electrically coupled to respective bond pads 1108 using heat and pressure to reflow the bumps 1118 at each pad interface. In particular, in embodiments, the bumps 1118 may be electrically and physically coupled to the bond pads 1108 using a thermo-compression technique where the bumps 1118 are pressed against the bond pads 1108 at elevated temperature for a period of time to reflow the bumps which diffuse with or otherwise adhere to the bond pads 1108. In further embodiments, ultrasonic vibrations may be applied to the bumps 1118 in addition to or instead of elevating the temperature to facilitate bonding of the bumps 1118 to the pads 1108. In embodiments, the cone-shaped bumps 1118 may adhere better than other types of bumps 1118 (*i.e.*, greater resistance to shear forces between bumps 1118 and pads 1108), as the ultrasonic welding and/or pressure are concentrated over a small diameter tip ( $d_2$  in Fig. 28A). However, as noted, bumps 1118 may have a variety of shapes in different embodiments.

**[00149]** As noted, the first and second semiconductor dies 1102 and 1112 may be coupled together after they are diced from their respective wafers 1100 and 1110. However, in further embodiments, the second semiconductor dies 1112 may be affixed to the first semiconductor

dies 1102 before the first semiconductor dies 1102 are diced from wafer 1110. After the first and second dies 1102 and 1112 are coupled, the first dies 1102 may be diced from wafer 1110.

**[00150]** Once coupled to each other, the first and second semiconductor dies 1102, 1112 together form an integrated memory module 1120 as shown in Fig. 30. In accordance with aspects of the present technology, the integrated memory module 1120 is a single, complete integrated flash memory, such as for example a BiCS flash memory. Forming the integrated memory module 1120 from two separate semiconductor dies has several advantages over conventional memory dies formed on a single die. For example, where the first die 1102 includes a memory cell array, removal of the logic circuit from the first die frees up valuable space for additional memory cells. For example, where the memory cells are configured as a layered 3D memory stack, removal of the logic circuit allows additional layers to be provided in the memory stack.

**[00151]** Moreover, separation of the memory cells and the logic circuits into two separate wafers allows the fabrication processes for both wafers to be customized and optimized for the particular integrated circuits formed on the respective wafers. For example, conventional processes for forming flash memory integrated circuits involve a heat step which could be detrimental to the CMOS logic circuits. By fabricating the logic circuits on their own wafer, this problem may be alleviated.

**[00152]** Referring again to Fig. 30, the second semiconductor die 1112 of integrated memory module 1120 may be significantly smaller than the first semiconductor die 1102. As such, the overall footprint of the integrated memory module 1120 may be determined exclusively by the footprint of the first semiconductor die 1102. That is, the size of the second semiconductor die 1112 does not increase or otherwise affect the footprint of the integrated memory module 1120.

**[00153]** In the embodiments shown in Figs. 29-30, the first and second semiconductor dies 1102, 1112 include a pattern of bond pads for flip-chip bonding of the dies. It is understood that the first and second semiconductor dies 1102, 1112 may be electrically coupled to each other using other schemes in further embodiments. In one such further embodiment, the first and second semiconductor dies 1102, 1112 may be electrically coupled to each other using through-silicon vias (TSV). In another such embodiment, the first and second semiconductor dies 1102, 1112 may be wire bonded to each other. The flip-chip bond pads 1108 and bumps 1118 may be omitted in such alternative embodiments.

**[00154]** Additional details relating to the physical and electrical coupling of the first and second semiconductor dies 1102, 1112 will now be explained with reference to the cross-sectional edge view of Fig. 31 and the edge view of Fig. 32. First semiconductor die 1102 may include integrated circuit memory cell array 1122 formed in and/or on a substrate layer 1124 within a chip region of the first semiconductor die 1102. As noted, the memory cell array 1122 may be formed as a 3D stacked memory structure having strings of memory cells formed into layers. After formation of the memory cell array 1122, multiple layers of metal interconnects 1126 and vias 1128 may be formed sequentially in layers of a dielectric film 1130. As is known in the art, the metal interconnects 1126, vias 1128 and dielectric film layers 1130 may be formed a layer at a time using photolithographic and thin-film deposition processes. The photolithographic processes may include for example pattern definition, plasma, chemical or dry etching and polishing. The thin-film deposition processes may include for example sputtering and/or chemical vapor deposition. The metal interconnects 1126 may be formed of a variety of electrically conductive metals including for example copper and copper alloys as is known in the art, and the vias 1128 may be lined and/or filled with a variety of electrically conductive metals including for example tungsten, copper and copper alloys as is known in the art.

**[00155]** A passivation layer 1132 may be formed on top of the upper dielectric film layer 1130. The passivation layer 1132 may be etched to form the bond pads 1106, 1108. Each bond pad 1106, 1108 may include a contact layer 1134 formed over a liner 1136. As is known in the art, the contact layer 1134 may be formed for example of copper, aluminum and alloys thereof, and the liner 1136 may be formed for example of a titanium/titanium nitride stack such as for example Ti/TiN/Ti, though these materials may vary in further embodiments. The bond pads 1106, 1108 (contact layer plus liner) may have a thickness of 720 nm, though this thickness may be larger or smaller in further embodiments.

**[00156]** The metal interconnects 1126 and vias 1128 may be used to form conductive nodes 1140 as is known in the art within the chip region for transferring signals and voltages between the die bond pads 1108 and integrated circuits 1122. Metal interconnects 1126 may also be used to transfer signals between the contact pads 1106 and the integrated circuits 1122 and/or the second die 1112. Thus, as explained below, signals, for example from a memory controller, may be transferred to/from the second semiconductor die 1112 via the die bond pads 1106, the metal interconnects 1126 and bond pads 1108 on first die 1102. Signals may also be transferred

between the first die 1102 and second die 1112 via the metal interconnects 1126 and bond pads 1108 on first die 1102.

**[00157]** The metal interconnects 1126 and vias 1128 may also be used to form a seal ring 1142 as is known in the art within a seal ring area. The seal ring 1142 may surround the integrated circuits 1122 and conductive nodes 1140, and provide mechanical support to prevent damage to the integrated circuits 1122 and conductive nodes 1140 for example during dicing of the wafer 1110.

**[00158]** As noted above, the second semiconductor die 1112 may be formed in a similar way to include integrated circuits such as for example CMOS logic circuits 1115. As with first dies 1102, the integrated circuits in second die 1112 may be electrically interconnected with the bumps 1118 of the second die 1112 via a framework of metal interconnects and vias, as well as with RDL 1117 as described above. The embodiment shown in Fig. 31 includes cone-shaped bumps 1118, but other types of bumps may be used including pillar and spherical bumps.

**[00159]** Fig. 32 shows a more general edge view of an integrated memory module 1120 including a second die 1112 affixed to first die 1102 by bumps 1118. The number of bumps 1118 shown in Figs. 31 and 32 is for illustrative purposes and will vary in further embodiments. Once the second die 1112 is affixed to the first die 1102, a space between the first and second dies may be under filled with an epoxy or other resin or polymer 1144. The under-fill material 1144 may be applied as a liquid which then hardens into a solid layer. This under-fill step protects the electrical connections between the first and second dies 1102, 1112, and further secures the second die 1112 onto the first die 1102. Various materials may be used as under-fill material 1144, but in embodiments, it may be Hysol epoxy resin from Henkel Corp., having offices in California, USA.

**[00160]** Referring again to Fig. 22, after the first and second dies 1102, 1112 are formed and coupled to each other to form integrated memory module 1120, the memory module 1120 may be tested in step 1208 as is known, for example with read/write and burn in operations.

**[00161]** In step 1212, two or more integrated memory modules 1120 may be stacked on a substrate 1180 as shown in the perspective views of Figs. 33 and 34. The substrate may be any of various chip-carrying media including conductive pads 1182, 1184, electrical traces and vias for transferring data and commands between the stacked integrated memory modules 1120 and a host device such as host device 1174 described above. Such chip carrier media may include

but are not limited to a printed circuit board (PCB), a leadframe or a tape automated bonded (TAB) tape. Passive components (not shown) may be mounted to the substrate either before or after the integrated memory modules 1120. The passive components may include for example one or more capacitors, resistors and/or inductors, though other components are contemplated.

**[00162]** As noted with respect to Fig. 31 above, a memory controller die 1170, such as an ASIC, may also be mounted to the substrate 1180 to control the exchange of information between the integrated memory modules 1120 and the host device. In embodiments, the controller die 1170 may be wire bonded to the substrate 1180, though it may be connected by other methods in further embodiments.

**[00163]** A first integrated memory module 1120 may be mounted on the substrate 1180 in step 1212, as by a die attach film (DAF) on a lower surface of the first die 1102. Electrical connections in the form of wire bonds 1185 may then be formed between the contact pads 1106 on the first die 1102 and a first set of pads 1182 on the substrate 1180 in step 1214. Wire bonds 1185 may be formed in a conventional manner, such as for example using ball bonds, though other types of bonds are contemplated. The wire bonds 1185 may be formed of gold, gold alloy or other materials. The substrate 1180 and the one or more wire bonded integrated memory modules 1120 together may form a semiconductor device 1190. As shown in Fig. 33 and described above, the second semiconductor die 1112 may be mounted along an edge of the first semiconductor die 1102 in semiconductor device 1190.

**[00164]** Steps 1212 and 214 may be repeated (as indicated by the dashed line in Fig. 22) to add additional integrated circuit memory modules 1120 to the semiconductor device 1190. As shown in Figs. 34 and 35, a second integrated memory module 1120 may be mounted on top of the first integrated memory module 1120, again using a DAF layer on a lower surface of die 1102 of the second integrated memory module 1120. In accordance with aspects of the present technology the second integrated memory module 1120 be mounted in a staggered, offset configuration.

**[00165]** In particular, the second integrated memory module 1120 may be offset relative to the first integrated memory module 1120 a distance,  $y'$  (Fig. 35), along the y-axis to leave room for the wire bonds 1185 on the bond pads 1106. In embodiments, the distance  $y'$  may range between 50 and 1100  $\mu\text{m}$ , though this distance may be lesser or greater than that in further embodiments. The second integrated memory module 1120 may also be offset relative to the

first integrated memory module 1120 a distance,  $x'$ , along the x-axis to leave room on the first semiconductor die 1102 for the second semiconductor die 1112 of the first integrated memory module 1120. Thus, the first die 1102 of the second integrated memory module 1120 may be mounted directly on a surface of the first die 1102 of the first integrated memory module 1120, next to the second die 1112 of the first integrated memory module 1120. In embodiments, the distance  $x'$  may range between 1100 and 500  $\mu\text{m}$ , though this distance may be lesser or greater than that in further embodiments.

**[00166]** The second integrated memory module 1120 may be rotated  $1180^\circ$  relative to the first integrated memory module 1120, so that the die bond pads 1106 of the second integrated memory module are located adjacent a second set of pads 1184 at a second edge of the substrate 1180. The die bond pads 1106 may be wire bonded to the second set of pads 1184 using a second set of wire bonds 1185. As seen in Fig. 35 for example, the second semiconductor die 1112 of the second integrated memory module 1120 is also located on an opposed edge of the semiconductor device 1190 from the second semiconductor die 1112 of the first integrated memory module 1120.

**[00167]** As shown in Figs. 36 and 37, a third integrated memory module 1120 may then be added to the semiconductor device 1190. The third integrated memory module 1120 may be mounted on top of the second integrated memory module 1120, again using a DAF layer on a lower surface of die 1102 of the third integrated memory module 1120. The third integrated memory module 1120 may be offset relative to the second integrated memory module 1120 a distance,  $y''$  (Fig. 37), along the y-axis to leave room for the wire bonds 1185 on the bond pads 1106 of the second integrated memory module 1120. The third integrated memory module 1120 may also be offset relative to the second integrated memory module 1120 a distance,  $x''$ , along the x-axis to leave room for the second semiconductor die 1112 at the edge of the second integrated memory module 1120.

**[00168]** In embodiments, the third integrated memory module 1120 may align directly over the first integrated memory module 1120. That is, in embodiments, the distance  $y''$  may be the same as  $y'$ , but in the opposite direction, and the distance  $x''$  may be the same as  $x'$ , but in the opposite direction. It is understood that the distances  $y'$  and  $y''$  need not be the same as each other in further embodiments, and that the distances  $x'$  and  $x''$  need not be the same as each other in further embodiments.

**[00169]** The first and third integrated memory modules 1120 may be spaced from each other by the thickness of the first semiconductor die and DAF layer of the second memory module 1120. This spacing is sufficiently large to leave room for the second semiconductor die 1112 beneath the third integrated memory module 1120. The third integrated memory module 1120 may be wire bonded to the substrate 1180 using wire bonds 1185 between bond pads 1106 on the third integrated memory module and the first set of pads 1182 on substrate 1180.

**[00170]** As shown in Figs. 38 and 39, a fourth integrated memory module 1120 may then be added to the semiconductor device 1190. The fourth integrated memory module 1120 may be mounted on top of the third integrated memory module 1120, again using a DAF layer on a lower surface of die 1102 of the fourth integrated memory module 1120. The fourth integrated memory module 1120 may be offset staggered relative to the third integrated memory module 1120 so as to lie directly over the second integrated memory module, leaving room for the second semiconductor die 1112 at the edge of the third integrated memory module 1120. The fourth integrated memory module 1120 may be wire bonded to the substrate 1180 using wire bonds 1185 between bond pads 1106 on the fourth integrated memory module and the second set of pads 1184 on substrate 1180.

**[00171]** The integrated memory modules 1120 may be mounted on each other in the z-direction in an alternating staggered offset configuration as described above so as to form a die stack 1186 on the substrate 1180 as shown in the edge view of Fig. 40. While 4 memory modules 1120 are shown in the figures, there may be 1, 2, 4, 8, 16, 32, 64 or other numbers of memory modules 1120 in stack 1186 in different embodiments.

**[00172]** In accordance with aspects of the present technology, the integrated memory modules 1120 may be stacked on each other in such a way that the second die 1112 of each module 1120 does not add to or otherwise affect the overall height required in the semiconductor device 1190 for the die stack 1186. In particular, the integrated memory modules 1120 may be mounted on each other in stack 1186 in a staggered, offset configuration so that the first semiconductor die 1102 of a memory module 1120 may be affixed directly to the first semiconductor die 1102 of the memory module 1120 immediately below it.

**[00173]** The second die 1112 may have a thickness that is less than or equal to a thickness of the first die 1102. Thus, the second die 1112 of each module 1120 does not add to the overall height required in the semiconductor device 1190 for the die stack 1186.

**[00174]** In order to prevent excess stresses on the overhanging portions of each of the first die 1102 (other than the die 1102 directly on the substrate 1180), spacers or solder pillars 1192 may be provided beneath the overhang portions as shown in Fig. 4 to provide support for the overhanging portions. A single solder pillar 1192 may be provided on each level. Alternatively, number of such solder pillars 1192 may be provided on each level (into the page of the figures) or one long spacer may be provided. The solder pillars 1192 may be omitted in further embodiments.

**[00175]** After all integrated memory modules are added to the stack 1186 and wire bonded, the semiconductor device 1190 may be encapsulated in a mold compound 1196 in step 1216 and as shown in Fig. 41. Mold compound 1196 may include for example solid epoxy resin, Phenol resin, fused silica, crystalline silica, carbon black and/or metal hydroxide. Such mold compounds are available for example from Sumitomo Corp. and Nitto-Denko Corp., both having headquarters in Japan. Other mold compounds from other manufacturers are contemplated. The mold compound may be applied by a FFT (Flow Free Thin) process or by other known processes, including by transfer molding or injection molding techniques.

**[00176]** In step 1220, solder balls 1198 (Fig. 41) may optionally be affixed to the contact pads 1194 on a lower surface of substrate 1180 of the semiconductor device 1190. The solder balls 1198 may be used to electrically and mechanically couple the semiconductor device 1190 to a host device 1174 (Fig. 42) such as a printed circuit board. Solder balls 1198 may be omitted where the semiconductor device 1190 is to be used as an LGA package.

**[00177]** In order to take advantage of economies of scale, multiple semiconductor devices 1190 may be formed simultaneously on a panel of substrates 1180. After formation and encapsulation of the devices 1190 on the panel, the devices 1190 may be singulated from each other in step 1224 to form a finished semiconductor device 1190 as shown in Fig. 41. The semiconductor devices 1190 may be singulated by any of a variety of cutting methods including sawing, water jet cutting, laser cutting, water guided laser cutting, dry media cutting, and diamond coating wire cutting. While straight line cuts will define generally rectangular or square shaped semiconductor devices 1190, it is understood that semiconductor device 1190 may have shapes other than rectangular and square in further embodiments of the present technology.

**[00178]** In the embodiments described above, the second semiconductor die 1112 is mounted at an edge of the first semiconductor die 1102, so that integrated memory modules 1120 may be stacked on top of each other without interference from the second semiconductor die 1112. In a further embodiment, the second semiconductor die 1112 may be centrally mounted on top of the first semiconductor die 1102. Such an embodiment will now be described with reference to Figs. 42-45.

**[00179]** Fig. 42 is a perspective view of a semiconductor device 290 including an integrated memory module 1120 mounted on a substrate 280. The integrated memory module 1120 may comprise a first die 1102 and a second die 1112 which may be fabricated and affixed to each other in accordance with any of the above-described embodiments. However, in the embodiment of Fig. 42, the second semiconductor die 1112 may be mounted on a central portion, away from the edges, of the upper surface of the first semiconductor die 1102. In embodiments, a central portion of the die may be any position that is spaced from the edges of the first semiconductor die 1102 by at least a width of the second semiconductor die 1112, and spaced from the die bond pads 1106 by at least a width of the second semiconductor die 1112. In further embodiments, the central portion may be the central 20% to 50% of the area of the first semiconductor die 1102.

**[00180]** The substrate 280 in the embodiment of Fig. 42 may be similar to the substrate 1180 described above, but may include a single row of contact pads 1182 (the contact pads 1184 of substrate 1180 may be omitted). Substrate 280 may include the first and second rows of contact pads 1182, 1184 in further embodiments. The integrated memory module 1120 may be electrically interconnected to the substrate 280 as described above, for example via wire bonds 1185 between pads 1106 on the first die 1102 and pads 1182 on the substrate 280.

**[00181]** In accordance with this embodiment, a second integrated memory module 1120 may be mounted directly on top of the first integrated memory module 1120, as shown in Fig. 43. In order to accommodate the second semiconductor die 1112 and wire bonds 1185 on the first integrated memory module 1120, an FOD (film on die) layer 250 may be provided on a lower surface of the first semiconductor die 1102 of the second integrated memory module 1120.

**[00182]** The FOD layer 250 may be an A-stage or B-stage thermosetting resin, or at some viscosity therebetween, tacked onto the lower surface of the first semiconductor die 1102 of

the second integrated memory module 1120. When the second integrated memory module 1120 is placed on top of the first integrated memory module 1120, the second semiconductor die 1112 and wire bonds 1185 of the first integrated memory module 1120 displace portions of the FOD layer 250. Thus, the second semiconductor die 1112 and wire bonds 25 of the first integrated memory module 1120 embed within the FOD layer 250 of the second integrated memory module 1120, and the second integrated memory module 1120 may lie flat on top of the first integrated memory module 1120 as shown in Fig. 43.

**[00183]** In embodiments, the FOD layer 250 may be the DAF layer formed on a lower surface of the first dies 1102 during wafer fabrication. In further embodiments, the FOD layer 250 may be applied to the lower surface of first dies 1102 in addition to or instead of the DAF layer. Although not shown, the lower surface of the first semiconductor die 1102 of the bottommost integrated memory module 1120 shown in Fig. 42 may also include the FOD layer 250.

**[00184]** The FOD layer 250 may have a thickness slightly greater than the thickness of the second semiconductor die 1112 and/or the height of wire bonds 1185 above the upper surface of the first die 1102. In embodiments, the thickness of the FOD layer 250 may range between 30 and 1100  $\mu\text{m}$ , though it may be thinner or thicker than that in further embodiments.

**[00185]** Once the second integrated memory module 1120 is mounted on top of the first integrated memory module 1120, the second integrated memory module 1120 may be electrically interconnected to the substrate 280, for example via wire bonds 1185 between pads 1106 on the first die 1102 and pads 1182 on the substrate 280 as shown in Fig. 43.

**[00186]** Additional integrated memory modules 1120 (having an FOD layer 250 on a lower surface of the first semiconductor die 1102) may be added to the semiconductor device 290, and wire bonded as described above. Fig. 44 is a side view of a semiconductor device 290 including four integrated memory modules 1120 stacked on top of each other. As shown, the second semiconductor dies 1112 and wire bonds 1185 are embedded within the FOD layer 250 of the above-mounted integrated memory module 1120. While four layers are shown, it is understood that semiconductor device 290 may include various numbers of stacked integrated memory modules 1120, including for example 11, 2, 4, 8, 116, 32 and 64 integrated memory modules 1120. Other numbers of integrated memory modules 1120 may be provided in further embodiments.

**[00187]** After all integrated memory modules are stacked on top of each other and wire bonded, the semiconductor device 290 may be encapsulated in a mold compound 1196 as described above and as shown in Fig. 45. As noted, mold compound 1196 may include for example solid epoxy resin, Phenol resin, fused silica, crystalline silica, carbon black and/or metal hydroxide. Additionally, solder balls 1198 may optionally be affixed to the contact pads 1194 on a lower surface of substrate 280 of the semiconductor device 290.

**[00188]** Fig. 46 illustrates a further embodiment of the present technology. The semiconductor device 290 of Fig. 46 is identical to that shown in Fig. 44, except that the integrated circuit modules are offset in a stepped configuration to each other so that the pads 1106 remain uncovered by an above-mounted integrated memory module 1120. As in Fig. 44, the second semiconductor die 1112 are embedded within the FOD layer 250 of the above-mounted integrated memory module 1120. In this embodiment, all integrated memory modules 1120 may be stacked on the substrate 280, and thereafter wire bonded down the stack using wire bonds 1185.

**[00189]** Fig. 47 illustrates a further embodiment of the present technology, including a first group of stacked integrated memory modules 1120 offset stepped in a first direction, and a second group of stacked integrated memory modules 1120 mounted on the first group and offset stepped in a second direction opposite to the first direction. An FOD layer 250 may be provided on the bottom of each integrated memory module 1120 in the first and second groups of stacked offset integrated memory modules 1120. In order to electrically connect the second (top) group of stacked integrated memory modules 1120 with the substrate 280, an interposer layer 260 may be provided between the first and second groups of integrated memory modules 1120. In this embodiment, the integrated memory modules 1120 in the first group and the interposer layer 260 may be stacked on the substrate 280, and thereafter wire bonded down the stack using wire bonds 1185. The second group of integrated memory modules 1120 may then be stacked on the interposer layer 260, and thereafter wire bonded down the stack using wire bonds 1185. As shown, the wire bond 1185 between the interposer layer 260 and the top-most integrated memory module 1120 in the first group may embed within the FOD layer 250 of the bottommost integrated memory module 1120 of the second group. Alternatively, a section of the FOD layer 250 on the interposer layer 260 (in dashed lines) may be omitted from beneath the interposer layer 250.

**[00190]** Fig. 47 shows four integrated memory modules 1120 in each of the first and second groups. It is understood that the number of integrated memory modules 1120 in the first and/or second groups may vary in further embodiments.

**[00191]** Fig. 48 is an edge view of a further embodiment of the present technology including one or more spacers 270 around one or more edges of the second semiconductor die 1112 of at least some of the integrated memory modules 1120 in the semiconductor device 290. In particular, sheer or other stresses may develop on a second semiconductor die 1112 when embedded within the FOD layer 250 upon mounting of the next higher integrated memory module 1120. The spacers 270 may be provided to reduce and/or alleviate these stresses. As noted, spacers 270 may be provided around a single edge, two edges, three edges or all four edges of the second semiconductor dies 1112. The spacers 270 may have a thickness which is slightly less than, equal to or greater than a thickness of the second semiconductor dies 1112. The spacers 270 may be formed of an inert material, such as for example silicon dioxide, though other materials are possible.

**[00192]** Although not shown, the devices 290 shown in the embodiments of Figs. 46-48 may be encapsulated in mold compound 1196 as described above. Additionally, solder balls 1198 may optionally be affixed to the contact pads 1194 on a lower surface of substrate 280 of the semiconductor devices 290 of Figs. 46-48.

**[00193]** In summary, an example of the present technology relates to an integrated memory module comprising: a first semiconductor die; a second semiconductor die flip-chip bonded to a major planar surface of the first semiconductor die, at an edge of the major planar surface of the first semiconductor die, to electrically and physically couple the second semiconductor die to the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory.

**[00194]** The above example of the integrated memory module, wherein the first semiconductor die comprises a plurality of memory cells.

**[00195]** The above example of the integrated memory module, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.

**[00196]** The above example of the integrated memory module, wherein the control circuit comprises a complementary metal–oxide–semiconductor integrated circuit.

**[00197]** The above example of the integrated memory module, wherein the first semiconductor die comprises a plurality of bonding pads configured to wire bond the first semiconductor die.

**[00198]** The above example of the integrated memory module, wherein the first semiconductor die comprises a plurality of bonding pads configured to bond the first semiconductor die to the second semiconductor die.

**[00199]** The above example of the integrated memory module, wherein the second semiconductor die comprises a plurality of bumps configured to mate with the plurality of bond pads on the first semiconductor die.

**[00200]** The above example of the integrated memory module, wherein the plurality of bumps are cone-shaped.

**[00201]** The above example of the integrated memory module, wherein the second semiconductor die is smaller than the first semiconductor die.

**[00202]** In another example, the present technology relates to A semiconductor device, comprising: a substrate; a first integrated memory module affixed to the substrate, comprising: a first semiconductor die including a surface having a plurality of die bond pads; a second semiconductor die bonded to the surface of the first semiconductor die adjacent the plurality of die bond pads; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory; and a third semiconductor die, mounted on the surface of the first semiconductor die, adjacent the second semiconductor die.

**[00203]** The above example of the semiconductor device, wherein the third semiconductor die is offset along a first axis with respect to the first semiconductor die, and the wherein the third semiconductor die is offset along a second axis with respect to the first semiconductor die, the second axis being orthogonal to the first axis.

**[00204]** The above example of the semiconductor device, wherein the third semiconductor die comprises a plurality of memory cells, the semiconductor device further comprising a fourth

semiconductor die bonded to the surface of the third semiconductor, wherein the third and fourth coupled semiconductor dies together comprise a second integrated flash memory.

**[00205]** The above example of the semiconductor device, wherein the fourth semiconductor die is flip-chip bonded to the third semiconductor die.

**[00206]** The above example of the semiconductor device, wherein the fourth semiconductor die is electrically connected to the third semiconductor die using through silicon vias.

**[00207]** The above example of the semiconductor device, further comprising a wire bond extending between a contact pad on the substrate and a die bond pad on the first semiconductor die.

**[00208]** The above example of the semiconductor device, wherein the plurality of bond pads on the first semiconductor die comprise a first plurality of bond pads, and wherein the third semiconductor die comprises a second plurality of bond pads.

**[00209]** The above example of the semiconductor device wherein, the first plurality of bond pads are wire bonded to a first set of contact pads on a first edge of the substrate, and wherein the second plurality of bond pads are wire bonded to a second set of contact pads on a second edge of the substrate opposite the first edge of the substrate.

**[00210]** The above example of the semiconductor device, wherein the third semiconductor die comprises: a surface having a plurality of die bond pads adjacent a first edge of the first semiconductor die, and a second edge adjacent the first edge, and a plurality of memory cells within an interior of the third semiconductor die; the semiconductor device further comprising a fourth semiconductor die bonded to the surface of the third semiconductor die, at the second edge of the third semiconductor die, the third and fourth coupled semiconductor dies together comprising a second integrated memory module; the semiconductor device further comprising a fifth semiconductor die, mounted on the surface of the third semiconductor die, adjacent the fourth semiconductor die.

**[00211]** The above example of the semiconductor device, wherein the fifth semiconductor die is offset along a first axis with respect to the third semiconductor die, and wherein the fifth semiconductor die is offset along a second axis with respect to the third semiconductor die, the second axis being orthogonal to the first axis.

**[00212]** The above example of the semiconductor device, wherein the fifth semiconductor die is aligned directly over the first semiconductor die.

**[00213]** In a further example, the present technology relates to a semiconductor device, comprising: a substrate; a first integrated memory module affixed to the substrate, comprising:

a first semiconductor die including a surface having a plurality of bond pads adjacent a first edge of the first semiconductor die, and a second edge adjacent the first edge; a second semiconductor die bonded to the surface of the first semiconductor die at the second edge; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory; and a third semiconductor die, mounted on the surface of the first semiconductor die, adjacent the second semiconductor die.

**[00214]** The above example of the semiconductor device, wherein the third semiconductor die comprises a plurality of memory cells, the semiconductor device further comprising a fourth semiconductor die bonded to the surface of the third semiconductor, wherein the third and fourth coupled semiconductor dies together comprise a second flash memory.

**[00215]** The above example of the semiconductor device, wherein the fourth semiconductor die is flip-chip bonded to the third semiconductor die.

**[00216]**

**[00217]** The above example of the semiconductor device, wherein the fourth semiconductor die is electrically connected to the third semiconductor die using through silicon vias.

**[00218]** The above example of the semiconductor device, further comprising a wire bond extending between a contact pad on the substrate and a die bond pad on the first semiconductor die.

**[00219]** The above example of the semiconductor device, wherein the third semiconductor die comprises: a surface having a plurality of die bond pads adjacent a first edge of the first semiconductor die, and a plurality of memory cells within an interior of the third semiconductor die; the semiconductor device further comprising a fourth semiconductor die bonded to the surface of the third semiconductor die, at a central portion of the surface of the third semiconductor die, the third and fourth coupled semiconductor dies together comprising a second integrated memory module; the semiconductor device further comprising a fifth semiconductor die comprising a film layer on a surface of the fifth semiconductor die, the fifth semiconductor die mounted to the surface of the third semiconductor die with the fourth semiconductor die embedded within the film layer.

**[00220]** The above example of the semiconductor device, wherein the fourth semiconductor die is aligned directly over the second semiconductor die.

**[00221]** The above example of the semiconductor device, wherein the third semiconductor die comprises a plurality of memory cells, the semiconductor device further comprising a fourth semiconductor die bonded to a central portion of the surface of the third semiconductor,

wherein the third and fourth coupled semiconductor dies together are configured as an integrated flash memory.

**[00222]** The above example of the semiconductor device wherein the fourth semiconductor die is flip-chip bonded to the third semiconductor die.

**[00223]** In another example, the present technology relates to an integrated memory module, comprising: a substrate; a first integrated memory module affixed to the substrate, comprising: a first semiconductor die including a surface having a plurality of bond pads adjacent a first edge of the first semiconductor die; a second semiconductor die bonded to the surface of the first semiconductor die, at a central portion of the surface of the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory; and a third semiconductor die comprising a film layer on a surface of the third semiconductor die, the third semiconductor die mounted to the surface of the first semiconductor die with the second semiconductor die embedded within the film layer.

**[00224]** In a further example, the present technology relates to an integrated memory module, comprising: a first semiconductor die comprising memory means; a second semiconductor die comprising control means, the second semiconductor die flip-chip bonded to a major planar surface of the first semiconductor die, at an edge of the major planar surface of the first semiconductor die, to electrically and physically couple the second semiconductor die to the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory.

**[00225]**

**[00226]** A further embodiment of the present technology will now be described with reference to Figs. 49-74, which in embodiments, relate to a semiconductor device including stacked integrated memory modules and plated column electrical connectors. Each integrated memory module may include a pair of semiconductor die, which together, operate as a single, integrated flash memory. The division of the flash memory functionality between the pair of die in the module may vary in embodiments, but in one example, the first die may include the memory cell array and the second die may include the logic circuit such as CMOS integrated circuits.

**[00227]** In embodiments, the second semiconductor die of the integrated memory module may be flip-chip bonded to a surface of the first semiconductor die to form an integrated

memory modules. A number of integrated memory modules may be stacked atop each other in an offset, stepped configuration and encapsulated to form a semiconductor device. In embodiments, columns of plated electrical conductors may be formed on each integrated memory module to electrically connect each integrated memory module with a surface of the semiconductor device.

**[00228]** An embodiment of the present technology will now be explained with reference to the flowchart of Figs. 49 and 50, and the views of Figs. 51-74. In step 2200, a first semiconductor wafer 2100 may be processed into a number of first semiconductor dies 2102 as shown in Fig. 51. The first semiconductor wafer 2100 may start as an ingot of wafer material which may be monocrystalline silicon grown according to either a Czochralski (CZ) or floating zone (FZ) process. However, first wafer 2100 may be formed of other materials and by other processes in further embodiments.

**[00229]** The semiconductor wafer 2100 may be cut from the ingot and polished on both the first major surface 2104, and second major surface (not shown) opposite surface 2104, to provide smooth surfaces. The first major surface 2104 may undergo various processing steps to divide the wafer 2100 into the respective first semiconductor dies 2102, and to form integrated circuits of the respective first semiconductor dies 2102 on and/or in the first major surface 2104. These various processing steps may include metallization steps depositing metal contacts including a row of bond pads 2106 and flip-chip bond pads 2108 exposed on the first major surface 2104. The metallization steps may further include depositing metal interconnect layers and vias within the wafer. These metal interconnect layers and vias may be provided for transferring signals to and from the integrated circuits as explained below with respect to Fig. 57.

**[00230]** The number of first semiconductor dies 2102 shown on wafer 2100 in Fig. 51 is for illustrative purposes, and wafer 2100 may include more first semiconductor dies 2102 than are shown in further embodiments. Similarly, the pattern of bond pads 2106, 2108, as well as the number of bond pads 2106, 2108, on the first semiconductor die 2102 are shown for illustrative purposes. Each first die 2102 may include more bond pads 2106, 2108 than are shown in further embodiments, and may include various patterns of bond pads 2106 and/or 2108. In one embodiment, the bond pads 2106 are formed in a row along an edge of each first die 2102.

**[00231]** In embodiments, the first semiconductor dies 2102 may be processed to include integrated circuit memory cells, such as for example one or more 3D stacked memory cell

arrays having strings of NAND memory. The first semiconductor dies 2102 may include other and/or additional circuits in further embodiments as explained below.

**[00232]** Before, after or in parallel with the formation of the first semiconductor dies on wafer 2100, a second semiconductor wafer 2110 may be processed into a number of second semiconductor dies 2112 in step 2202 as shown in Fig. 52. The semiconductor wafer 2110 may start as an ingot of monocrystalline silicon grown according to either a CZ, FZ or other process. The second semiconductor wafer 2110 may be cut and polished on both the first major surface 2114, and second major surface (not shown) opposite surface 2114, to provide smooth surfaces. The first major surface 2114 may undergo various processing steps to divide the second wafer 2110 into the respective second semiconductor dies 2112, and to form integrated circuits of the respective second semiconductor dies 2112 on and/or in the first major surface 2114. The number of second semiconductor dies 2112 shown on wafer 2110 in Fig. 52 is for illustrative purposes, and wafer 2110 may include more second semiconductor dies 2112 than are shown in further embodiments.

**[00233]** In one embodiment, the second semiconductor dies 2112 may be processed to include integrated logic circuits 2115 (Fig. 57), configured to control read/write operations for one or more integrated memory cell arrays. The logic circuits may be fabricated using CMOS technology, though the logic circuits may be fabricated using other technologies in further embodiments. The second semiconductor dies 2112 may include other and/or additional circuits in further embodiments as explained below. Each logic circuit 2115 may be electrically coupled to a metal bond pad 2116 (Fig. 53) on an upper surface of the dies 2112 by metal interconnect layers and/or vias.

**[00234]** A pattern of bumps 2118 may be formed on the bond pads 2116 on a surface of dies 2112 as shown for example in Figs. 52 and 53. The bumps 2118 may be formed by a wide variety of techniques, including for example by stud bumping on the second wafer 2110 or using micro-bumps. The bumps 2118 may be formed of various materials, including for example Cu, Cu-Sn, Pb-Sn, Au, alloys thereof, or other solder materials and metals of relatively high melting points. The pads 2116 and bumps 2118 are provided in a pattern matching that of the bond pads 2108 on the first dies 2102. In embodiments, the spacing between bumps 2118 may vary between 5 microns ( $\mu\text{m}$ ) and 50  $\mu\text{m}$ , though the spacing may be smaller or larger than this in further embodiments.

**[00235]** In embodiments, the bumps 2118 may be cylindrical pillars or spherical balls. However, in further embodiments, the bumps 2118 may be cone-shaped as shown in Fig. 53 and the enlarged view of Fig. 53A. The cone-shaped bumps 2118 may have straight sidewalls to form a true cone, or have sidewalls with a concave portion at the base transitioning into a convex portion at the tip as shown in the figures. Cone-shaped bumps 2118 may be deposited on the pads 2106 by first depositing a Ti/Cu seed layer on the pads. Next, undercut holes may be formed using a resist pattern over the seed layer by photolithography. The undercut holes in the resist film may then be filled with bump material, for example in an electroplating process. The photoresist and seed layer may then be removed using one or more solvents to leave the cone-shaped bumps 2118.

**[00236]** In embodiments, the cone-shaped bumps 2118 may have a base diameter,  $d_1$ , of 8-10  $\mu\text{m}$ , a tip diameter,  $d_2$ , of 2-3  $\mu\text{m}$ , and a height,  $h$ , of 8-9  $\mu\text{m}$ . However, each of these dimensions may vary in further embodiments, both proportionately and disproportionately to each other. The spacing between the cone-shaped bumps may be about 20  $\mu\text{m}$ , but this spacing may vary in further embodiments. As explained below, the cone-shaped bumps 2118 have certain advantages with respect to shear strength when the cone-shaped bumps of dies 2112 are ultrasonically bonded to the pads 2108 of dies 2102. However, as noted, the bumps 2118 may be pillars, spherical or other shapes in further embodiments. The number of bumps 2118 on the second semiconductor die 2112 shown in Figs. 52-55 is for illustrative purposes, and each second die 2112 may include more bumps 2118 than are shown in further embodiments.

**[00237]** In step 2206, first semiconductor dies 2102 from wafer 2100 and second semiconductor dies from wafer 2110 may be physically and electrically coupled to each other as shown in Figs. 54 and 55. As noted, in one embodiment, the pattern of flip-chip bond pads 2108 on first semiconductor die 2102 may match the pattern of bumps 2118 on second semiconductor die 2112 as shown in Fig. 54. The bumps 2118 may be bonded to each of the pads 2108. As explained below, conductive columns are formed on bond pads 2106 of dies 2102 to electrically interconnect the dies 2102 and/or 2112 with a host device such as a printed circuit board. Accordingly, the pads 2106 may be left open when the dies 2102 and 2112 are bonded together. That is, bumps 2118 bond with pads 2108 on dies 2102, and not with pads 2106 on dies 2102.

**[00238]** In order to affix the first and second dies 2102 and 2112 together, the second semiconductor die 2112 may be flipped over, and respective bumps 2118 may be physically

and electrically coupled to respective bond pads 2108 using heat and pressure to reflow the bumps 2118 at each pad interface. In particular, in embodiments, the bumps 2118 may be electrically and physically coupled to the bond pads 2108 using a thermo-compression technique where the bumps 2118 are pressed against the bond pads 2108 at elevated temperature for a period of time to reflow the bumps which diffuse with or otherwise adhere to the bond pads 2108. In further embodiments, ultrasonic vibrations may be applied to the bumps 2118 in addition to or instead of elevating the temperature to facilitate bonding of the bumps 2118 to the pads 2108. In embodiments, the cone-shaped bumps 2118 may adhere better than other types of bumps 2118 (*i.e.*, greater resistance to shear forces between bumps 2118 and pads 2108), as the ultrasonic welding and/or pressure are concentrated over a small diameter tip ( $d_2$  in Fig. 53A). However, as noted, bumps 2118 may have a variety of shapes in different embodiments.

**[00239]** In the embodiments described above, bumps 2118 are affixed to the second dies 2112, for coupling with the bond pads 2108 on the first dies 2102. In further embodiments, it is conceivable that the bumps 2118 may be affixed to the first dies 2102, and configured to couple with bond pads on the second dies 2112.

**[00240]** Once the second die 2112 is affixed to the first die 2102, a space between the first and second dies may be under filled with an epoxy or other resin or polymer 2117 (Fig. 55). The under-fill material 2117 may be applied as a liquid which then hardens into a solid layer. This under-fill step protects the electrical connections between the first and second dies 2102, 2112, and further secures the second die 2112 onto the first die 2102. Various materials may be used as under-fill material 2117, but in embodiments, it may be Hysol epoxy resin from Henkel Corp., having offices in California, USA.

**[00241]** The first and second semiconductor dies 2102 and 2112 may be coupled together after they are diced from their respective wafers 2100 and 2110. However, in further embodiments, the second semiconductor dies 2112 may be affixed to the first semiconductor dies 2102 before the first semiconductor dies 2102 are diced from wafer 2100. After the first and second dies 2102 and 2112 are coupled, the first dies 2102 may be diced from wafer 2100.

**[00242]** Once coupled to each other, the first and second semiconductor dies 2102, 2112 together form an integrated memory module 2120 as shown in Fig. 56. As shown, the second die 2112 may cover a substantial portion of the first die 2102, but the bond pads 2106 are left uncovered and accessible. In the embodiment shown, the bond pads 2106 are along a single

edge. However, in further embodiments, the bond pads 2106 may be along multiple (two or three) or around all four edges of die 2102. In such embodiments, the second die 2112 would be sized and shaped so as to leave all such bond pads 2106 uncovered and accessible. It is also conceivable that bond pads 2106 may be formed in center portion of the first die 2102. In such embodiments, the second die 2112 may be formed with a central opening so that the bond pads 2106 in the center of the first die 2102 are left uncovered and accessible.

**[00243]** In accordance with aspects of the present technology, the integrated memory module 2120 is a single, complete integrated flash memory, such as for example a BiCS flash memory. Forming the integrated memory module 2120 from two separate semiconductor dies has several advantages over conventional flash memory dies formed on a single die. For example, where the first die 2102 includes a memory cell array, removal of the logic circuit from the first die frees up valuable space for additional memory cells. For example, where the memory cells are configured as a layered 3D memory stack, removal of the logic circuit allows additional layers to be provided in the memory stack.

**[00244]** Moreover, separation of the memory cells and the logic circuits into two separate wafers allows the fabrication processes for both wafers to be customized and optimized for the particular integrated circuits formed on the respective wafers. For example, conventional processes for forming flash memory integrated circuits involve a heat step which could be detrimental to the CMOS logic circuits. By fabricating the logic circuits on their own wafer, this problem may be alleviated.

**[00245]** In the embodiments shown and described with respect to Figs. 53-56, the first and second semiconductor dies 2102, 2112 include a pattern of bond pads for flip-chip bonding of the dies. It is understood that the first and second semiconductor dies 2102, 2112 may be electrically coupled to each other using other schemes in further embodiments. In one such further embodiment, the first and second semiconductor dies 2102, 2112 may be electrically coupled to each other using through-silicon vias (TSV). In another such embodiment, the first and second semiconductor dies 2102, 2112 may be wire bonded to each other. The flip-chip bond pads 2108 and bumps 2118 may be omitted in such alternative embodiments.

**[00246]** Additional details relating to the physical and electrical coupling of the first and second semiconductor dies 2102, 2112 will now be explained with reference to the cross-sectional edge view of Fig. 57. First semiconductor die 2102 may include integrated circuit memory cell array 2122 formed in and/or on a substrate layer 2124 within a chip region of the

first semiconductor die 2102. As noted, the memory cell array 2122 may be formed as a 3D stacked memory structure having strings of memory cells formed into layers. After formation of the memory cell array 2122, multiple layers of metal interconnects 2126 and vias 2128 may be formed sequentially in layers of a dielectric film 2130. As is known in the art, the metal interconnects 2126, vias 2128 and dielectric film layers 2130 may be formed a layer at a time using photolithographic and thin-film deposition processes. The photolithographic processes may include for example pattern definition, plasma, chemical or dry etching and polishing. The thin-film deposition processes may include for example sputtering and/or chemical vapor deposition. The metal interconnects 2126 may be formed of a variety of electrically conductive metals including for example copper and copper alloys as is known in the art, and the vias 2128 may be lined and/or filled with a variety of electrically conductive metals including for example tungsten, copper and copper alloys as is known in the art.

**[00247]** A passivation layer 2132 may be formed on top of the upper dielectric film layer 2130. The passivation layer 2132 may be etched to form the bond pads 2106, 2108. Each bond pad 2106, 2108 may include a contact layer 2134 formed over a liner 2136. As is known in the art, the contact layer 2134 may be formed for example of copper, aluminum and alloys thereof, and the liner 2136 may be formed for example of a titanium/titanium nitride stack such as for example Ti/TiN/Ti, though these materials may vary in further embodiments. The bond pads 2106, 2108 (contact layer plus liner) may have a thickness of 720 nm, though this thickness may be larger or smaller in further embodiments.

**[00248]** The metal interconnects 2126 and vias 2128 may be used to form conductive nodes 2140 as is known in the art within the chip region for transferring signals and voltages between the integrated circuits 2122 and die bond pads 2108, and in turn between the bond pads 2108 and the second die 2112. Metal interconnects 2126 and vias 2128 may also be used to transfer signals between the integrated circuits 2122 and the contact pads 2106, and in turn between the bond pads 2106 and a host device as explained below. Signals may also be transferred between the first die 2102 and second die 2112 via the metal interconnects 2126 extending directly between bond pads 2106 and 2108. The metal interconnects 2126 may be used to couple pads 2106 with select ones of pads 2108.

**[00249]** As noted above, the second semiconductor die 2112 may be formed in a similar way to include integrated circuits such as for example CMOS logic circuits 2115. As with first dies 2102, the integrated circuits in second die 2112 may be electrically interconnected with

the bumps 2118 of the second die 2112 via a framework of metal interconnects and vias. The embodiment shown in Fig. 57 includes cone-shaped bumps 2118, but other types of bumps may be used including pillar and spherical bumps.

**[00250]** Referring again to Fig. 49, after the first and second dies 2102, 2112 are formed and coupled to each other to form integrated memory module 2120, the memory module 2120 may be tested in step 2208 as is known, for example with read/write and burn in operations.

**[00251]** In step 2212, two or more integrated memory modules 2120 may be stacked vertically in the z-direction on a carrier 2180 to form a die stack 2186 as shown in the edge view of Fig. 58. The integrated memory modules may be attached to each other and the carrier 2180 for example by a die attach film (DAF) on a bottom surface of each of the dies 2102. The carrier 2180 may be formed of an insulative material, such as for example silicon dioxide or glass, though other materials are possible for carrier 2180. The integrated memory modules 2120 may be stacked in an offset, stepped configuration, so that the bond pads 2106 of each integrated memory module remains accessible from above. While Fig. 58 shows four stacked integrated memory modules 2120, there may be 1, 2, 4, 8, 16, 32, 64 or other numbers of integrated memory modules on the carrier 2180 in further embodiments.

**[00252]** Once mounted in die stack 2186 as shown in Fig. 58, the electrical connections may then be formed on the contact pads 2106 in step 2214. Further details of forming the electrical connections in step 2214 will now be described with respect to the flowchart of Fig. 50 and the views of Figs. 58-63. In step 2228, the stack 2186 is encased within photoresist 2188 as shown in Fig. 59. A pattern mask 2190 is then applied over the photoresist (Fig. 60), and the photoresist 2188 is then exposed and developed in step 2230 to remove the photoresist in those areas of the stack not covered by the mask 2190. As shown in Fig. 61, the removal of the photoresist in step 2230 forms holes 2192 extending down from the top surface of the photoresist to the surfaces of bond pads 2106 on each integrated memory module 2120 in the stack 2186.

**[00253]** In step 2232, the mask 2190 may be removed (Fig. 61), and the holes 2192 may be filled with an electrical conductor in step 2234 to form conductive columns 2194 (Fig. 61). In embodiments, the conductive columns 2194 may be formed by electroplating process to plate the electrical conductor within the holes 2192. In embodiments, electrical conductor forming the conductive columns 2194 may be Cu or alloys thereof, but other electrical conductors are

contemplated. In step 2238, photoresist 2188 is removed leaving the conductive columns 2194 extending from contact pads 2106 as shown in Fig. 62.

**[00254]** Referring again to the flowchart of Fig. 49, after the conductive columns 2194 are formed, the stack 2186 and conductive columns 2194 may be encased in a housing such as mold compound 2196 in step 2216 to form a semiconductor device 2300 as shown in the edge and perspective views of Figs. 64 and 65. The upper surface of mold compound 2196 may be ground and/or polished so that the upper ends of conductive columns 2194 are flush with the upper surface of mold compound 2196. In embodiments, the semiconductor device 2300 shown in Figs. 64 and 65 may be complete with respect to the number of integrated memory modules 2120 included within the device 2300. However, as explained below, additional integrated memory modules 2120 may be added to the semiconductor device 2300.

**[00255]** The semiconductor device 2300 may be encapsulated in a mold compound 2196, which may include for example solid epoxy resin, Phenol resin, fused silica, crystalline silica, carbon black and/or metal hydroxide. Such mold compounds are available for example from Sumitomo Corp. and Nitto-Denko Corp., both having headquarters in Japan. Other mold compounds from other manufacturers are contemplated. The mold compound may be applied by a FFT (Flow Free Thin) process or by other known processes, including by transfer molding or injection molding techniques. The housing may be formed of other materials, and formed around the semiconductor device 2300 in other ways, in further embodiments.

**[00256]** As noted, the semiconductor device 2300 shown in Figs. 64 and 65 may be substantially complete. However, in further embodiments, additional integrated memory modules 2120 may be added (as indicated by the dashed arrow in the flowchart of Fig. 49). For example, as shown in Fig. 66, a second set of integrated memory modules 2120 may be stacked on top of the mold compound 2196 in a stepped, offset configuration so that the bond pads on each level of integrated memory module 2120 remain uncovered and accessible from above. The second set of integrated memory modules 2120 may be stacked on top of each other using a DAF layer on a bottom surfaces of the first dies 2102 of each integrated memory module 2120.

**[00257]** The second set of integrated memory modules 2120 may then be electrically interconnected in step 2214 and encapsulated in step 2216 as described above. In particular, the second set of integrated memory modules may be encased within photoresist 2288 as shown

in Fig. 67. A pattern mask 2290 is then applied over the photoresist (Fig. 68), and the photoresist 2288 is then exposed and developed in step 2230 to remove the photoresist in those areas of the stack not covered by the mask 2290. The mask pattern has a first group of openings that align directly over the conductive columns 2194. As shown in Fig. 68, the removal of the photoresist in step 2230 forms holes 2292 extending down from the top surface of the photoresist to the surfaces of bond pads 2106 on each integrated memory module 2120 in the second group. The removal of the photoresist in step 2230 also forms holes 2292 extending down from the top surface of the photoresist to connect with the tops of the conductive columns 2194 exposed at the surface of the mold compound 2196.

**[00258]** In step 2232, the mask 2290 may be removed (Fig. 69), and the holes 2292 may be filled with an electrical conductor in step 2234 to form a second group of conductive columns 2294. As shown in Fig. 69, the conductive columns 2294 extend from the bond pads 2106 of the second group of integrated memory modules 2120. The conductive columns also connect with and extend from the conductive columns 2194. In embodiments, a conductive column 2294 connected to a conductive column 2194 may be considered a single conductive column.

**[00259]** In embodiments, the conductive columns 2294 may be formed by electroplating process to plate the electrical conductor within the holes 2292. In embodiments, electrical conductor forming the conductive columns 2294 may be the same as the conductor used for columns 2194. In step 2238, photoresist 2288 may be removed leaving the conductive columns 2294 as shown in Fig. 70 extending above the surface of mold compound 2196 and extending from contact pads 2106 of the second group of integrated memory modules.

**[00260]** After the conductive columns 2294 are formed, the second group of integrated memory modules and conductive columns 2294 may be encased in a housing such as mold compound 2296 in step 2216 to form the semiconductor device 2300 as shown in the edge and perspective views of Figs. 71 and 72. The mold compound 2296 may be same as mold compound 2196, and applied in the same manner as mold compound 2196. The upper surface of mold compound 2296 may be ground and/or polished so that the upper ends of conductive columns 2294 are flush with the upper surface of mold compound 2296. The housing around the second group of integrated memory modules 2120 may be formed of other materials, and formed around the second group of memory modules in other ways, in further embodiments.

**[00261]** The conductive columns 2294 may be used to electrically connect the bond pads 2106 of the semiconductor device 2300 to a host device which may for example be a printed

circuit board. As shown in Figs. 73 and 74, the pattern of conductive columns may be distributed across a larger portion of the surface of the semiconductor device 2300 using a redistribution layer (RDL) 2295 in step 2220. The pattern of the RDL 2295 shown in Figs. 73 and 74 is by way of example only and may vary in further embodiments.

**[00262]** In step 2222, solder balls 2298 (Figs. 73 and 74) may optionally be affixed to the pads on the surface of RDL 2295. The solder balls 2298 may be used to electrically and mechanically couple the semiconductor device 2300 to a host device. Solder balls 2298 may be omitted where the semiconductor device 2300 is to be used as an LGA package.

**[00263]** In order to take advantage of economies of scale, multiple semiconductor devices 2300 may be formed simultaneously on a large carrier 2180. After formation and encapsulation of the devices 2300 on the carrier 2180, the carrier may be removed (step 2224) and the devices 2300 may be singulated from each other (step 2226) to form a finished semiconductor device 2300 as shown in Fig. 74. The devices 2300 may be singulated prior to removing the carrier in further embodiments.

**[00264]** The semiconductor devices 2300 may be singulated by any of a variety of cutting methods including sawing, water jet cutting, laser cutting, water guided laser cutting, dry media cutting, and diamond coating wire cutting. While straight line cuts will define generally rectangular or square shaped semiconductor devices 2300, it is understood that semiconductor device 2300 may have shapes other than rectangular and square in further embodiments of the present technology.

**[00265]** In the embodiments described above, each group of four integrated memory modules 2120 are stacked, electrical connections are formed, and then it is encapsulated. The semiconductor device 2300 may have more than two groups of integrated memory modules in further embodiments. Moreover, each group may have more or less than four integrated memory modules 2120. Each group may have the same number of memory modules, but they need not have the same number of memory modules in further embodiments.

**[00266]** In embodiments described above, the first semiconductor die 2102 is slightly larger than the second semiconductor die 2112, and includes an extra row of pads 2106 for receiving the conductive columns as described above. In further embodiments, the second semiconductor die 2112 may be slightly larger than the first semiconductor die 2102. In this

embodiment, the second semiconductor die 2112 may include an extra row of pads 2106 for receiving the conductive columns as described above.

**[00267]** In summary, an example of the present technology relates to an integrated memory module comprising: a first semiconductor die; a second semiconductor die flip-chip bonded to a major planar surface of the first semiconductor die, at an edge of the major planar surface of the first semiconductor die, to electrically and physically couple the second semiconductor die to the first semiconductor die; wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory.

**[00268]** The integrated memory module of above, wherein the first semiconductor die comprises a plurality of memory cells.

**[00269]** The integrated memory module of above, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.

**[00270]** The integrated memory module of above, wherein the control circuit comprises a complementary metal-oxide-semiconductor integrated circuit.

**[00271]** The integrated memory module of above, wherein the second semiconductor die comprises a plurality of bumps configured to mate with the second group of bond pads on the first semiconductor die.

**[00272]** The integrated memory module of above, wherein the plurality of bumps are cone-shaped.

**[00273]** The integrated memory module of above, wherein the second semiconductor die is smaller than the first semiconductor die.

**[00274]** In another example, the present technology relates to a semiconductor device, comprising: one or more integrated memory modules, each integrated memory module comprising: a first semiconductor die including a surface having a first plurality of bond pads and a second plurality of bond pads; a second semiconductor die bonded to the second plurality of bond pads; wherein the first and second bonded semiconductor dies together are configured as an integrated flash memory; a housing encasing the one or more integrated memory modules; and a plurality of conductive columns, in contact with the first plurality of bond pads on each first semiconductor die and extending from the first plurality of bond pads, through the housing, to a surface of the housing, the plurality of conductive columns configured to electrically connect the one or more integrated memory modules to a host device.

[00275] The semiconductor device of above, wherein the plurality of conductive columns are electroplated conductive columns.

[00276] The semiconductor device of above, wherein the one or more integrated memory modules comprise a plurality of memory modules stacked in an offset, stepped configuration which leaves the plurality of first bond pads uncovered and accessible from above the plurality of first bond pads.

[00277] The semiconductor device of above, wherein the first and second semiconductor dies are flip-chip bonded to each other.

[00278] The semiconductor device of above, further comprising a plurality of bumps on one of the first and second dies configured to couple the first and second dies together during the flip-chip bonding of the first and second semiconductor dies.

[00279] The semiconductor device of above, wherein the plurality of bumps are cone-shaped.

[00280] The semiconductor device of above, wherein the first and second semiconductor dies are bonded to each other by through silicon vias.

[00281] The semiconductor device of above, wherein the first and second plurality of bond pads on the first semiconductor die are electrically coupled together.

[00282] The semiconductor device of above, wherein the first semiconductor die comprises a plurality of memory cells.

[00283] The semiconductor device of above, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.

[00284] The semiconductor device of above, wherein the control circuit comprises a complementary metal–oxide–semiconductor integrated circuit.

[00285] A semiconductor device, comprising: a plurality of integrated memory modules stacked on each other, each integrated memory module comprising: a first semiconductor die including a surface having a first plurality of bond pads and a second plurality of bond pads; a second semiconductor die bonded to the second plurality of bond pads; wherein the first and second bonded semiconductor dies together are configured as an integrated flash memory; and wherein the plurality of memory modules are stacked on each other in an offset, stepped configuration which leaves the plurality of first bond pads on each first semiconductor die uncovered and accessible from above the plurality of first bond pads; a housing encasing the plurality of integrated memory modules; and a plurality of conductive columns, in contact with

the first plurality of bond pads on each first semiconductor die and extending from the first plurality of bond pads, through the housing, to a surface of the housing.

**[00286]** The semiconductor device of above, wherein: the plurality of integrated memory modules comprise a first plurality of memory modules, the housing comprises a first housing, and plurality of conductive columns comprise a first plurality of conductive column, the semiconductor device further comprising: a second plurality of integrated memory modules stacked on each other, each integrated memory module in the second plurality comprising: a third semiconductor die including a surface having a third plurality of bond pads and a fourth plurality of bond pads; a fourth semiconductor die bonded to the fourth plurality of bond pads; wherein the third and fourth bonded semiconductor dies together are configured as an integrated flash memory; and wherein the second plurality of memory modules are stacked on each other in an offset, stepped configuration which leaves the plurality of third bond pads uncovered and accessible from above the plurality of third bond pads; a second housing encasing the second plurality of integrated memory modules; and a second plurality of conductive columns, in contact with the first plurality of conductive columns and the third plurality of bond pads on each third semiconductor die and extending from the first plurality of conductive columns and third plurality of bond pads, through the second housing, to a surface of the second housing.

**[00287]** The semiconductor device of above, wherein the plurality of conductive columns are electroplated conductive columns.

**[00288]** The semiconductor device of above, wherein the first semiconductor die comprises a plurality of memory cells.

**[00289]** The semiconductor device of above, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.

**[00290]** The semiconductor device of above, wherein the control circuit comprises a complementary metal–oxide–semiconductor integrated circuit.

**[00291]** A semiconductor device, comprising: a plurality of stacked integrated memory modules, each integrated memory module comprising: a first semiconductor die comprising a first plurality of bond pads and memory means; a second semiconductor die bonded to the first semiconductor die and comprising control means for the memory means;

**[00292]** wherein the first and second bonded semiconductor dies together are configured as integrated flash memory means; housing means encasing the plurality of integrated memory modules; and electrical connector means, in contact with the first plurality of bond pads on

each first semiconductor die and extending from the first plurality of bond pads, through the housing means, to a surface of the housing means, the electrical connector means for electrically connecting the plurality of integrated memory modules to a host device.

**[00293]**

**[00294]** A further embodiment of the present technology will now be described with reference to Figs. 75-95, which in embodiments, relate to a semiconductor device including an integrated memory module. An integrated memory module may include multiple memory array semiconductor dies stacked on a CMOS logic circuit semiconductor die, which together, operate as a single, integrated flash memory. Each of the semiconductor die in an integrated memory module may be formed with a pattern of through-silicon vias (TSVs) capped with electrical connectors on opposed surfaces of the semiconductor die. In embodiments, a TSV is a hole etched or otherwise formed through a semiconductor die. The hole may be plated or filled with an electrical conductor. Before the hole is plated or filled, the hole may be lined with a barrier and/or seed layer to prevent diffusion of the plated or filled conductor.

**[00295]** Once the integrated memory module semiconductor dies are stacked on a CMOS logic circuit semiconductor die, the TSVs of the respective stacked semiconductor dies may be aligned and affixed to each other to electrically and mechanically connect each of the semiconductor dies in the integrated memory module. Further details of the integrated memory module and TSVs according to the present technology are provided below.

**[00296]** An embodiment of the present technology will now be explained with reference to the flowchart of Figs. 75 and 76, and the views of Figs. 77-95. In step 3200, a first semiconductor wafer 3100 may be processed into a number of first semiconductor dies 3102 as shown in Fig. 77. The first semiconductor wafer 3100 may start as an ingot of wafer material which may be monocrystalline silicon grown according to either a Czochralski (CZ) or floating zone (FZ) process. However, first wafer 3100 may be formed of other materials and by other processes in further embodiments.

**[00297]** The semiconductor wafer 3100 may be cut from the ingot and polished on both the first major planar surface 3104, and second major planar surface 3107 (Fig. 78) opposite surface 3104, to provide smooth surfaces. The first major surface 3104 may undergo various processing steps to divide the wafer 3100 into the respective first semiconductor dies 3102, and to form integrated circuits of the respective first semiconductor dies 3102 on and/or in the first major surface 3104.

**[00298]** In particular, in step 3200, the first semiconductor die 3102 may be processed in embodiments to include integrated circuit memory cell array 3122 formed in a dielectric substrate including layers 3124 and 3126 as shown in Fig. 78. In embodiments, the memory cell array 3122 may be formed as a 3D stacked memory structure having strings of memory cells formed into layers. However, it is understood that the first semiconductor die 3102 may be processed to include integrated circuits other than a 3D stacked memory structure. A passivation layer 3128 may be formed on top of the upper dielectric film layer 3126.

**[00299]** Multiple layers of metal interconnects and vias may be formed in and through the layers of the semiconductor die 3102. Notably, before, during or after formation of the memory cell array 3122, a pattern of through-silicon vias (TSVs) 3105 may be formed in step 3204 extending between the top and bottom major planar surfaces of the first wafer 3100. The TSVs 3105 may be formed by etching holes through the first semiconductor dies 3102 in the pattern of the finished TSVs 3105. The holes may then be lined with a barrier against diffusion of a later-applied metal, as explained below.

**[00300]** In an embodiment, the barrier layer may be formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, or the like. The barrier layer may be formed through physical vapor deposition (PVD), chemical vapor deposition (CVD) or atomic layer deposition (ALD), although other techniques could alternatively be used. The barrier layer may in turn be lined with a seed layer. The seed layer may be deposited by PVD or CVD, though it may be deposited by other techniques in further embodiments. The seed layer may be formed of copper, aluminum, tin, nickel, gold, alloys thereof or other materials.

**[00301]** A conductive material may then be plated onto the seed layer. The conductive material may comprise copper, although other suitable materials such as aluminum, tin, nickel, gold, doped polysilicon, and alloys or combinations thereof may be used. The conductive material may be formed by electroplating copper or other conductive material onto the seed layer. In embodiments, TSVs 3105 may be \*1 $\mu$ m to 50 $\mu$ m in diameter, but they may be smaller or larger than that in further embodiments. Once the TSVs have been filled with the conductive material, excess material extending beyond the first and/or major planar surfaces of semiconductor dies 3102 may be removed through a planarization process such as chemical mechanical polishing (CMP) or other processes.

**[00302]** In step 3208, bond pads 3108 may be formed on the opposite ends of each of the TSVs 3105 to physically and electrically couple the bond pads 3108 and TSVs 3105 as shown

in Fig. 79. The passivation layer 3128 may be etched over the TSVs 3105, and metal conductive layers applied, to form the bond pads 3108 on the first major surface of the semiconductor dies 3102. A like pattern of bond pads 3108 may be formed on the TSVs 3105 on the opposite major planar surface of semiconductor dies 3102 in a like manner.

**[00303]** Each bond pad 3108 may be formed over a liner 3106. As is known in the art, the bond pads 3108 may be formed for example of copper, aluminum and alloys thereof, and the liner 3106 may be formed for example of a titanium/titanium nitride stack such as for example Ti/TiN/Ti, though these materials may vary in further embodiments. The bond pads 3108 and liners 3106 together may have a thickness of 720 nm, though this thickness may be larger or smaller in further embodiments. The TSVs 3105 may be used for transferring signals and voltages between the integrated circuits 3122 and bond pads 3108.

**[00304]** Fig. 76 shows semiconductor dies 3102 on wafer 3100, and a pattern of bond pads 3108 on one of the semiconductor dies 3102, around a periphery of the semiconductor die 3102. The number of first semiconductor dies 3102 shown on wafer 3100 in Fig. 76 is for illustrative purposes, and wafer 3100 may include more first semiconductor dies 3102 than are shown in further embodiments. Similarly, the pattern of bond pads 3108, as well as the number of bond pads 3108, on the first semiconductor die 3102 are shown for illustrative purposes. Each first die 3102 may include more bond pads 3108 than are shown in further embodiments, and may include various other patterns of bond pads 3108.

**[00305]** Before, after or in parallel with the formation of the first semiconductor dies on wafer 3100, a second semiconductor wafer 3110 may be processed into a number of second semiconductor dies 3112 in step 3210 as shown in Fig. 77. The semiconductor wafer 3110 may start as an ingot of monocrystalline silicon grown according to either a CZ, FZ or other process. The second semiconductor wafer 3110 may be cut and polished on both the first major surface 3114, and second major surface 3117 (Fig. 80) opposite surface 3114, to provide smooth surfaces. The first major surface 3114 may undergo various processing steps to divide the second wafer 3110 into the respective second semiconductor dies 3112, and to form integrated circuits of the respective second semiconductor dies 3112 on and/or in the first major surface 3114.

**[00306]** In one embodiment, the second semiconductor dies 3112 may be processed to include integrated circuits 3132 (Fig. 80) formed in a dielectric substrate including layers 3134 and 3136. Integrated circuits 3132 may be configured as logic circuits to control read/write

operations for one or more integrated memory cell arrays. The logic circuits may be fabricated using CMOS technology, though the logic circuits may be fabricated using other technologies in further embodiments. The second semiconductor dies 3112 may include other and/or additional integrated circuits in further embodiments as explained below. A passivation layer 3138 may be formed on top of the upper dielectric film layer 3136.

**[00307]** Multiple layers of metal interconnects and vias may be formed in and through the layers of the second semiconductor die 3112. For example, before, during or after formation of integrated circuits 3132, a pattern of through-silicon vias (TSVs) 3115 may be formed in step 3214 extending between the top and bottom major planar surfaces of the second wafer 3110. The TSVs 3115 on the second semiconductor dies 3112 may be formed in the same pattern, and in the same manner, as TSVs 3105 on the first semiconductor dies 3102 described above.

**[00308]** In step 3218, bond pads 3118 may be formed on the active surface of each of the TSVs 3115 to physically and electrically couple the bond pads 3118 and TSVs 3115 as shown in Fig. 81. The passivation layer 3138 may be etched over the TSVs 3115, and metal conductive layers applied, to form the bond pads 3118 on the first major surface of the second semiconductor dies 3112. Each bond pad 3118 may be formed over a liner 3116 as described above. The bond pads 3118 and liners 3116 in the second semiconductor dies 3112 may be formed of the same materials, and in the same manner, as bond pads 3108 and liners 3106 on the first semiconductor dies 3102.

**[00309]** Fig. 77 shows the second semiconductor dies 3112 on wafer 3110, and a pattern of bond pads 3118 on one of the second semiconductor dies 3112, around a periphery of the second semiconductor die 3102. The number of second semiconductor dies 3112 shown on wafer 3110 in Fig. 77 is for illustrative purposes, and wafer 3110 may include more second semiconductor dies 3112 than are shown in further embodiments. Similarly, the pattern of bond pads 3118, as well as the number of bond pads 3118, on the second semiconductor die 3112 are shown for illustrative purposes. Each second die 3112 may include more bond pads 3118 than are shown in further embodiments, and may include various other patterns of bond pads 3118, matching the pattern of bond pads 3108 on first dies 3102. In embodiments, the size and shape of the second semiconductor dies 3112 match the size and shape of the first semiconductor dies 3102. The pattern of bond pads 3118 on the second semiconductor dies 3112 may also match the pattern of bond pads 3108 on the first semiconductor dies 3102.

**[00310]** In step 3220, a redistribution layer (RDL) 3140 may be formed on the second major planar surface 3117 of the second semiconductor dies 3112 opposite to the first major planar surface 3114 including bond pads 3118 as shown in Fig. 81. The RDL 3140 may electrically connect the bond pads 3118 and TSVs 3115 to a pattern of contact pads 3142 distributed across the second major planar surface 3117 of the second semiconductor dies 3112.

**[00311]** Referring now to Fig. 82, in one embodiment, a second semiconductor die 3112 may be mounted on a carrier 3144 in step in step 3224, and a number of first semiconductor dies 3102 may be stacked on top of each other, and on the second semiconductor die 3112 in step 3226 to form an integrated memory module 3120. The example of Fig. 82 shows three first die 3102 stacked on a second die 3112. However, there may be more or less than three first die 3102 on a second die 3112 in further embodiments. The stack comprising a carrier 3144, a second die 3112 and one or more first die 3102 may be assembled in any order. As one further example, a number of first die 3102 may be stacked on each other, that stack may be mounted on the second die 3112, and that combined stack may then be mounted on the carrier 3144.

**[00312]** The carrier 3144 may be formed of an insulative material, such as for example silicon dioxide, though other materials are possible for carrier 3144. An adhesive release layer 3146 may be provided on a surface of the carrier 3144 for releasably mounting the integrated memory module 3120.

**[00313]** The semiconductor dies 3102, 3112 in the integrated memory module 3120 may be bonded to each other by aligning the bond pads 3108/3118 on one die 3102, 3112 with the bond pads 3108/3118 of the next adjacent die 3102, 3112 in the stack. Thereafter, the bond pads 3108/3118 of adjacent die 3102, 3112 may be bonded together by any of a variety of bonding techniques, depending in part on bond pad size and bond pad spacing (*i.e.*, bond pad pitch).

**[00314]** In one embodiment, one or both sets of bond pads 3108/3118 on adjacent dies 3102, 3112 may include bumps which adhere the adjacent dies together using thermo-compression and/or ultrasonic bonding techniques. The bumps may be formed of Cu, Cu-Sn, Pb-Sn, Au, alloys thereof, or other metals and materials of relatively high melting points. In such embodiments, the bond pads may be about 70 $\mu$ m square and spaced from each other with a pitch of 50 $\mu$ m to \*100 $\mu$ m.

**[00315]** In a further embodiment, a small, controlled amount of solder, copper or other metal may be applied to one bond pad 3108/3118 at an interface between a pair of bond pads in a so-

called micro-bump bonding process. The respective bonds may be coupled to each other in the micro-bump bonding process using thermo-compression. In such embodiments, the bond pads 3108/3118 may be about 50 $\mu$ m square and spaced from each other with a pitch of 30 $\mu$ m to 50 $\mu$ m. The applied micro-bumps may be spherical or cylindrical. In a further embodiment, the applied micro-bumps may have a cone shape which has a wide base affixed to one of the bond pads, and tapers to a narrow tip which may get bonded to the opposed bond pad using thermo-compression and/or ultrasonic bonding techniques.

**[00316]** As explained below, in embodiments, the first semiconductor dies 3102 may include only memory array circuits, and all supporting control circuitry may be off-loaded to the second dies 3112. Such embodiments may have advantages, but require a large number of electrical connections (TSVs 3105/3115 and bond pads 3108/3118) between the first and second dies 3102 and 3112. In order to support such a large number of electrical connections, the bond pads 3108/3118 should be provided with a small area and pitch.

**[00317]** It is known to bond the bond pads 3108/3118 directly to each other, without solder or other added material, in a so-called Cu-to-Cu bonding process. In a Cu-to-Cu bonding process, the bond pads 3108/3118 are controlled to be highly planar and formed in a highly controlled environment largely devoid of ambient particulates that might otherwise settle on a bond pad 3108/3118. Under such conditions, the bond pads 3108/3118 of adjacent dies in the stack are aligned and pressed against each other to form a bond based on surface tension. Such bonds may be formed at room temperature, though heat may also be applied. In embodiments using Cu-to-Cu bonding, the bond pads 3108/3118 may be about 5 $\mu$ m square and spaced from each other with a pitch of 3 $\mu$ m to 5 $\mu$ m. While this process is referred to as Cu-to-Cu bonding, this term may also apply even where the bond pads 3108/3118 are formed of materials other than Cu.

**[00318]** When the area and pitch of bond pads 3108/3118 are small, it gets difficult to bond a pair of dies 3102, 3112 together. The pitch between bond pads 3108/3118 may be further reduced by providing a film layer on the surfaces of the first dies 3102 including the bond pads 3108, and a film layer on the surface of the second dies 3112 including the bond pads 3118. The film layer is provided around the bond pads 3108/3118. When two dies 3102, 3112 are brought together, the bond pads may bond to each other and the film layers may bond to each other. Such a bonding technique may be referred to as hybrid bonding. In embodiments using

hybrid bonding, the bond pads 3108/3118 may be about 3 $\mu$ m square and spaced from each other with a pitch of 31 $\mu$ m to 5 $\mu$ m.

**[00319]** As noted, once coupled to each other, the group of one or more first semiconductor dies 3102, and the second semiconductor die 3112 together form an integrated memory module 3120. In accordance with aspects of the present technology, the integrated memory module 3120 is a single, complete integrated flash memory, such as for example a BiCS flash memory, which is bifurcated into a group of one or more first dies 3102 and a second die 3112. Forming the integrated memory module 3120 from separate semiconductor dies has several advantages over conventional flash memory dies formed on a single die. For example, where the first dies 3102 includes memory cell arrays, removal of the logic circuit from the first dies frees up valuable space in each first die for additional memory cells. For example, where the memory cells are configured as a layered 3D memory stack, removal of the logic circuit allows additional layers to be provided in the memory stack.

**[00320]** Moreover, separation of the memory cells and the logic circuits into separate wafers allows the fabrication processes for the wafers to be customized and optimized for the particular integrated circuits formed on the respective wafers. For example, conventional processes for forming flash memory integrated circuits involve a heat step which could be detrimental to the CMOS logic circuits. By fabricating the logic circuits on their own wafer, this problem may be alleviated.

**[00321]** Figs. 83-86 show formation of semiconductor devices 3180 from the integrated memory modules 3120 according to a first embodiment. As noted, a second semiconductor die 3112 may be mounted on a carrier 3144 in step 3224, and a group of one or more first semiconductor dies 3102 (four in Figs. 83-86) may be mounted on the second semiconductor die 3112 in step 3226. Fig. 83 shows a number of integrated memory modules 3120 stacked on a carrier 3144 to take advantage of economies of scale in the fabrication of the semiconductor devices 3180. The top-most first semiconductor die 3102 in the stack of first semiconductor dies 3102 includes bond pads 3108 on an upper surface which do not get bonded to other bond pads. These bond pads 3108 on the upper surface of the top-most die 3102 may be omitted in further embodiments.

**[00322]** After the integrated memory modules 3120 are mounted on the carrier 3144, the respective integrated memory modules 3120 may be tested in step 3228 as is known, for example with read/write and burn in operations.

**[00323]** Once the first and second semiconductor dies 3102, 3112 are mounted on the carrier 3144, a space between the first and second dies may be under filled with an epoxy or other resin or polymer 3165 (Fig. 83) in step 3230. The under-fill material 3165 may be applied as a liquid which then hardens into a solid layer. This under-fill step protects the electrical connections between the first and second dies 3102, 3112, and further secures the second dies 3112 to each other and onto the first die 3102. Various materials may be used as under-fill material 3117, but in embodiments, it may be Hysol epoxy resin from Henkel Corp., having offices in California, USA.

**[00324]** Next, in step 3232, all of the integrated memory modules 3120 on carrier 3144 may be encased together in a housing such as mold compound 3164 as shown in Fig. 84. The mold compound 3164 may include for example solid epoxy resin, Phenol resin, fused silica, crystalline silica, carbon black and/or metal hydroxide. Such mold compounds are available for example from Sumitomo Corp. and Nitto-Denko Corp., both having headquarters in Japan. Other mold compounds from other manufacturers are contemplated. The mold compound may be applied by a FFT (Flow Free Thin) process or by other known processes, including by transfer molding or injection molding techniques. The housing may be formed of other materials, and formed around the integrated memory modules 3120 on carrier 3144 in other ways, in further embodiments.

**[00325]** In embodiments, the mold compound 3164 may fill in the gaps in between the first and second semiconductor dies 3102, 3112. In such embodiments, the under-fill material 3165 may be omitted. Additionally, in some embodiments, for example those using hybrid bonding, a film may be applied to one or both surfaces of the first and second semiconductor dies 3102, 3112 before they are stacked onto carrier 3144. In such embodiments, the under-fill step 3230 may also be omitted.

**[00326]** In step 3234, the carrier 3144 may be removed as shown in Fig. 85 by dissolving release layer 3146. Release layer 3146 may be dissolved using heat, chemicals, a laser and/or by other methods.

**[00327]** After removal of the carrier 3144, the block of mold compound 3164 may be singulated in step 3236 to form a finished semiconductor devices 3180 as shown in Fig. 86. The semiconductor devices 3180 may be singulated by any of a variety of cutting methods including sawing, water jet cutting, laser cutting, water guided laser cutting, dry media cutting,

and diamond coating wire cutting. While straight line cuts will define generally rectangular or square shaped semiconductor devices 3180, it is understood that semiconductor devices 3180 may have shapes other than rectangular and square in further embodiments of the present technology. The devices 3180 may be singulated prior to removing the carrier 3144 in further embodiments.

**[00328]** In step 3238, solder balls 3182 (Fig. 86) may optionally be affixed to the pads 3142 on the lower surface of RDL 3140 of one or more semiconductor devices 3180. Fig. 86 shows a single device 3180 including solder balls 3182, but more or less than one of the devices 3180 may have solder balls 3182 in further embodiments. The solder balls 3182 may be used to electrically and mechanically couple the semiconductor device 3180 to a host device. Solder balls 3182 may be omitted where the semiconductor device 3180 is to be used as an LGA package. The step 3238 of adding the solder balls 3182 may alternatively be performed prior to singulation of the devices 3180 in step 3236.

**[00329]** In the embodiment of Figs. 83-86, the first and second dies 3102, 3112 may both be diced from the first and second wafers 3100, 3110 before the dies 3102, 3112 are stacked on the carrier 3144. In further embodiments, individual first semiconductor dies 3102 may be diced from wafer 3100 and mounted on a second wafer 3110. Such an embodiment is shown in Fig. 87. Thereafter, the second wafer 3110 may be diced to form individual integrated memory modules 3120, which may be then mounted on a carrier 3144 as shown in Fig. 83. The individual integrated memory modules 3120 may then be encapsulated (Fig. 84), the carrier 3144 may be removed (Fig. 85), and the semiconductor devices 3180 may be singulated (Fig. 86) as described above.

**[00330]** However, instead of dicing the second wafer 3110 after receiving the first semiconductor dies 3102, the second wafer 3110 as a whole, including the individual first semiconductor dies 3102, may be encapsulated in mold compound 3164. Such an embodiment is shown in Fig. 88. In this embodiment, the carrier 3144 may be omitted. From Fig. 88, the mold compound 3164 and wafer 3110 may be singulated as shown in Fig. 89 to form the finished semiconductor devices 3180.

**[00331]** In a further embodiment, one or more first wafers 3100 may be stacked on top of a second wafer 3110. Such an embodiment is shown in Fig. 90. Thereafter, the first and second wafers 3100, 3110 may be diced to form individual integrated memory modules 3120, which

may be then mounted on a carrier 3144 as shown in Fig. 83. The individual integrated memory modules may then be encapsulated (Fig. 84), the carrier 3144 may be removed (Fig. 85), and the semiconductor devices 3180 may be singulated (Fig. 86) as explained above.

**[00332]** However, instead of dicing the first and second wafers 3100, 3110 after being mounted on each other, the whole wafers 3100 and 3110 may be encapsulated in mold compound 3164. Such an embodiment is shown in Fig. 91. In this embodiment, the carrier 3144 may be omitted. From Fig. 91, the mold compound 3164, first wafer(s) 3100 and second wafer 3110 may be singulated as shown in Fig. 92 to form the finished semiconductor devices 3180.

**[00333]** In the embodiments described above with respect to Figs. 83-86, the integrated memory modules 3120 are mounted on a carrier 3144 to provide stability and a fixed reference frame during fabrication of the finished semiconductor devices 3180. In the embodiments of Figs. 87-92, the carrier 3144 may be omitted. Alternatively, the carrier 3144 may be used in the embodiments of Figs. 87-92. Figs. 93-95 show an embodiment as in Figs. 87-89, but including a carrier 3144.

**[00334]** Instead of the carrier 3144, the embodiments of Figs. 87-92 may use a second wafer 3110 which is left relatively thick, such for example greater than 200 $\mu$ m, to provide structural support to the respective semiconductor devices 3180 during fabrication. In such embodiments, the TSVs 3115 may be formed through the thick second wafer 3110. The second wafer 3110 may be thinned after it is encapsulated as shown for example in Fig. 88. Thereafter, the RDL 3140 including pads 3142 may be formed on the thinned wafer 3110. Solder balls 3182 may then optionally be affixed to the pads 3142 as shown in Fig. 89.

**[00335]** In summary, an example of the present technology relates to an integrated memory module comprising: An integrated memory module, comprising: a plurality of first semiconductor dies comprising first and second opposed surfaces, each first semiconductor die of the plurality of first semiconductor dies comprising: first integrated circuits, a first group of bond pads on the first surface, a second group of bond pads on the second surface, and a first set of through-silicon vias electrically coupling the first and second groups of bond pads; a second semiconductor die comprising: third and fourth opposed surfaces, second integrated circuits, a third group of bond pads on the third surface, and a second set of through-silicon vias electrically coupled to the third group of bond pads; wherein the plurality of first

semiconductor dies and the second semiconductor die are coupled together by the first, second and third groups of bond pads; and wherein the plurality of first semiconductor dies and the second semiconductor die together are configured as an integrated flash memory.

**[00336]** The integrated memory module of above, wherein the first integrated circuits in each of the plurality of first semiconductor dies comprise a plurality of memory cells.

**[00337]** The integrated memory module of above, wherein the second integrated circuit comprises a control circuit for controlling access to the plurality of memory cells.

**[00338]** The integrated memory module of above, wherein the control circuit comprises a complementary metal–oxide–semiconductor integrated circuit.

**[00339]** The integrated memory module of above, wherein the plurality of first semiconductor die have the same length and width as each other and have the same patterns of first and second bond pads.

**[00340]** The integrated memory module of above, wherein the second semiconductor die have the same length and width as the plurality of first semiconductor die, and have the same pattern of third and fourth bond pads as the pattern of first and second bond pads.

**[00341]** A semiconductor device, comprising: a plurality of first semiconductor dies stacked on each other, the plurality of first semiconductor dies comprising first and second opposed surfaces, each first semiconductor die of the plurality of first semiconductor dies comprising: first integrated circuits, a first group of bond pads on the first surface, a second group of bond pads on the second surface, the first group of bond pads of a semiconductor die of the plurality of first semiconductor dies bonded to the second group of bond pads of a next adjacent die of the plurality of first semiconductor dies in the stack, and a first set of through-silicon vias electrically coupling the first and second groups of bond pads; a second semiconductor die, the plurality of first semiconductor die stacked on the second semiconductor die, the second semiconductor die comprising: third and fourth opposed surfaces, second integrated circuits, a third group of bond pads on the third surface, the third group of bond pads bonded to the second group of bond pads of a bottommost die of the plurality of first semiconductor dies in the stack, and a second set of through-silicon vias electrically coupled to the third group of bond pads; wherein the plurality of first semiconductor dies and the second semiconductor die together are configured as an integrated flash memory.

**[00342]** The semiconductor device of above, further comprising a fourth set of bond pads on the fourth surface of the second semiconductor die.

**[00343]** The semiconductor device of above, further comprising a redistribution patterns for electrically coupling the second set of through-silicon vias to the fourth set of bond pads on the fourth surface of the second semiconductor die.

**[00344]** The semiconductor device of above, further comprising solder balls affixed to the fourth set of bond pads.

**[00345]** The semiconductor device of above, wherein the first integrated circuits in each of the plurality of first semiconductor dies comprise a plurality of memory cells.

**[00346]** The semiconductor device of above, wherein the second integrated circuit comprises a control circuit for controlling access to the plurality of memory cells.

**[00347]** The semiconductor device of above, wherein the control circuit comprises a complementary metal–oxide–semiconductor integrated circuit.

**[00348]** A method of fabricating a semiconductor device, comprising: mounting bond pads of a plurality of first semiconductor dies to each other; mounting a set of bond pads of the plurality of first semiconductor dies to bond pads of a second semiconductor die, the first semiconductor dies and the second semiconductor die together being configured as an integrated flash memory; and encasing the plurality of first semiconductor dies and the second semiconductor die in a housing.

**[00349]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises mounting the plurality of first semiconductor dies to each other and the second semiconductor die after the plurality of first semiconductor dies and the second semiconductor die have been severed from wafers.

**[00350]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises mounting the plurality of first semiconductor dies to each other and the second semiconductor die after the plurality of first semiconductor dies have been severed from a wafer and before the second semiconductor die has been severed from a wafer.

**[00351]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises mounting the plurality of first semiconductor dies to each other and the second semiconductor die before the plurality of first semiconductor have been severed from a wafer and before the second semiconductor die has been severed from a wafer.

**[00352]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises applying solder to a pair of bond pads to be connected to each other and melting the solder using thermo-compression.

**[00353]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises applying solder to a pair of bond pads to be connected to each other and melting the solder using ultrasonic bonding.

**[00354]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises applying a micro-bump to one bond pad of a pair of bond pads to be connected to each other, and melting the micro-bump using thermo-compression.

**[00355]** The method of above, wherein mounting bond pads together in said steps (a) and (b) comprises a Cu-to-Cu bonding bringing the pair of bond pads together under pressure.

**[00356]** A semiconductor device, comprising: a plurality of first semiconductor dies stacked on each other, the plurality of first semiconductor dies comprising first and second opposed surfaces, each first semiconductor die of the plurality of first semiconductor dies comprising: first integrated circuit means, a first group of surface electrical connector means on the first surface for electrically connecting each of the plurality of first semiconductor dies, a second group of surface electrical connector means on the second surface for electrically connecting each of the plurality of first semiconductor dies, the first group of surface electrical connector means of a semiconductor die of the plurality of first semiconductor dies bonded to the second group of surface electrical connector means of a next adjacent die of the plurality of first semiconductor dies in the stack, and first through-silicon electrical connector means for electrically coupling the first and second groups of surface electrical connector means; a second semiconductor die, the plurality of first semiconductor die stacked on the second semiconductor die, the second semiconductor die comprising: third and fourth opposed surfaces, second integrated circuit means, a third group of surface electrical connector means on the third surface, the third group of surface electrical connector means bonded to the second group of surface electrical connector means of a bottommost die of the plurality of first semiconductor dies in the stack, and a second set of through-silicon electrical connector means electrically coupled to the third group of surface electrical connector means; wherein the plurality of first semiconductor dies and the second semiconductor die together are configured as an integrated flash memory.

**[00357]** The foregoing detailed description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best

utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

## CLAIMS

We claim:

1. An integrated memory module comprising:
  - a first semiconductor die;
  - a second semiconductor die flip-chip bonded to a surface of the first semiconductor die to electrically and physically couple the second semiconductor die to the first semiconductor die;
  - wherein the first and second coupled semiconductor dies together are configured as an integrated memory.
2. The integrated memory module of claim 1, wherein the first semiconductor die comprises a plurality of memory cells.
3. The integrated memory module of claim 2, wherein the second semiconductor die comprises a control circuit for controlling access of the plurality of memory cells.
4. The integrated memory module of claim 1, wherein the first and second dies together are configured as a nonvolatile memory device.
5. An integrated memory module comprising:
  - a first semiconductor die;
  - a second semiconductor die flip-chip bonded to a major planar surface of the first semiconductor die, at an edge of the major planar surface of the first semiconductor die, to electrically and physically couple the second semiconductor die to the first semiconductor die;
  - wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory.

6. The integrated memory module of claim 5, wherein the second semiconductor die comprises a plurality of bumps configured to mate with the plurality of bond pads on the first semiconductor die, wherein the plurality of bumps are cone-shaped.

7. A semiconductor device, comprising:

- a substrate;

- a first integrated memory module affixed to the substrate, comprising:

- a first semiconductor die including a surface having a plurality of die bond pads;

- a second semiconductor die bonded to the surface of the first semiconductor die adjacent the plurality of die bond pads;

- wherein the first and second coupled semiconductor dies together are configured as an integrated flash memory; and

- a third semiconductor die, mounted on the surface of the first semiconductor die, adjacent the second semiconductor die.

8. The semiconductor device of claim 7, wherein the third semiconductor die is offset along a first axis with respect to the first semiconductor die, and the wherein the third semiconductor die is offset along a second axis with respect to the first semiconductor die, the second axis being orthogonal to the first axis.

9. A semiconductor device, comprising:

- one or more integrated memory modules, each integrated memory module comprising:

- a first semiconductor die including a surface having a first plurality of bond pads and a second plurality of bond pads;

- a second semiconductor die bonded to the second plurality of bond pads;

- wherein the first and second bonded semiconductor dies together are configured as an integrated flash memory;

- a housing encasing the one or more integrated memory modules; and

a plurality of conductive columns, in contact with the first plurality of bond pads on each first semiconductor die and extending from the first plurality of bond pads, through the housing, to a surface of the housing, the plurality of conductive columns configured to electrically connect the one or more integrated memory modules to a host device.

10. The semiconductor device of claim 9, wherein the plurality of conductive columns are electroplated conductive columns.

11. The semiconductor device of claim 9, wherein the one or more integrated memory modules comprise a plurality of memory modules stacked in an offset, stepped configuration which leaves the plurality of first bond pads uncovered and accessible from above the plurality of first bond pads.

12. A semiconductor device, comprising:

a plurality of integrated memory modules stacked on each other, each integrated memory module comprising:

a first semiconductor die including a surface having a first plurality of bond pads and a second plurality of bond pads;

a second semiconductor die bonded to the second plurality of bond pads;

wherein the first and second bonded semiconductor dies together are configured as an integrated flash memory; and

wherein the plurality of memory modules are stacked on each other in an offset, stepped configuration which leaves the plurality of first bond pads on each first semiconductor die uncovered and accessible from above the plurality of first bond pads;

a housing encasing the plurality of integrated memory modules; and

a plurality of conductive columns, in contact with the first plurality of bond pads on each first semiconductor die and extending from the first plurality of bond pads, through the housing, to a surface of the housing.

13. A semiconductor device, comprising:

a plurality of first semiconductor dies stacked on each other, the plurality of first semiconductor dies comprising first and second opposed surfaces, each first semiconductor die of the plurality of first semiconductor dies comprising:

first integrated circuits,

a first group of bond pads on the first surface,

a second group of bond pads on the second surface, the first group of bond pads of a semiconductor die of the plurality of first semiconductor dies bonded to the second group of bond pads of a next adjacent die of the plurality of first semiconductor dies in the stack, and

a first set of through-silicon vias electrically coupling the first and second groups of bond pads;

a second semiconductor die, the plurality of first semiconductor die stacked on the second semiconductor die, the second semiconductor die comprising:

third and fourth opposed surfaces,

second integrated circuits,

a third group of bond pads on the third surface, the third group of bond pads bonded to the second group of bond pads of a bottommost die of the plurality of first semiconductor dies in the stack, and

a second set of through-silicon vias electrically coupled to the third group of bond pads;

wherein the plurality of first semiconductor dies and the second semiconductor die together are configured as an integrated flash memory.

14. The semiconductor device of claim 13, further comprising a fourth set of bond pads on the fourth surface of the second semiconductor die.

15. The semiconductor device of claim 14, further comprising a redistribution patterns for electrically coupling the second set of through-silicon vias to the fourth set of bond pads on the fourth surface of the second semiconductor die.

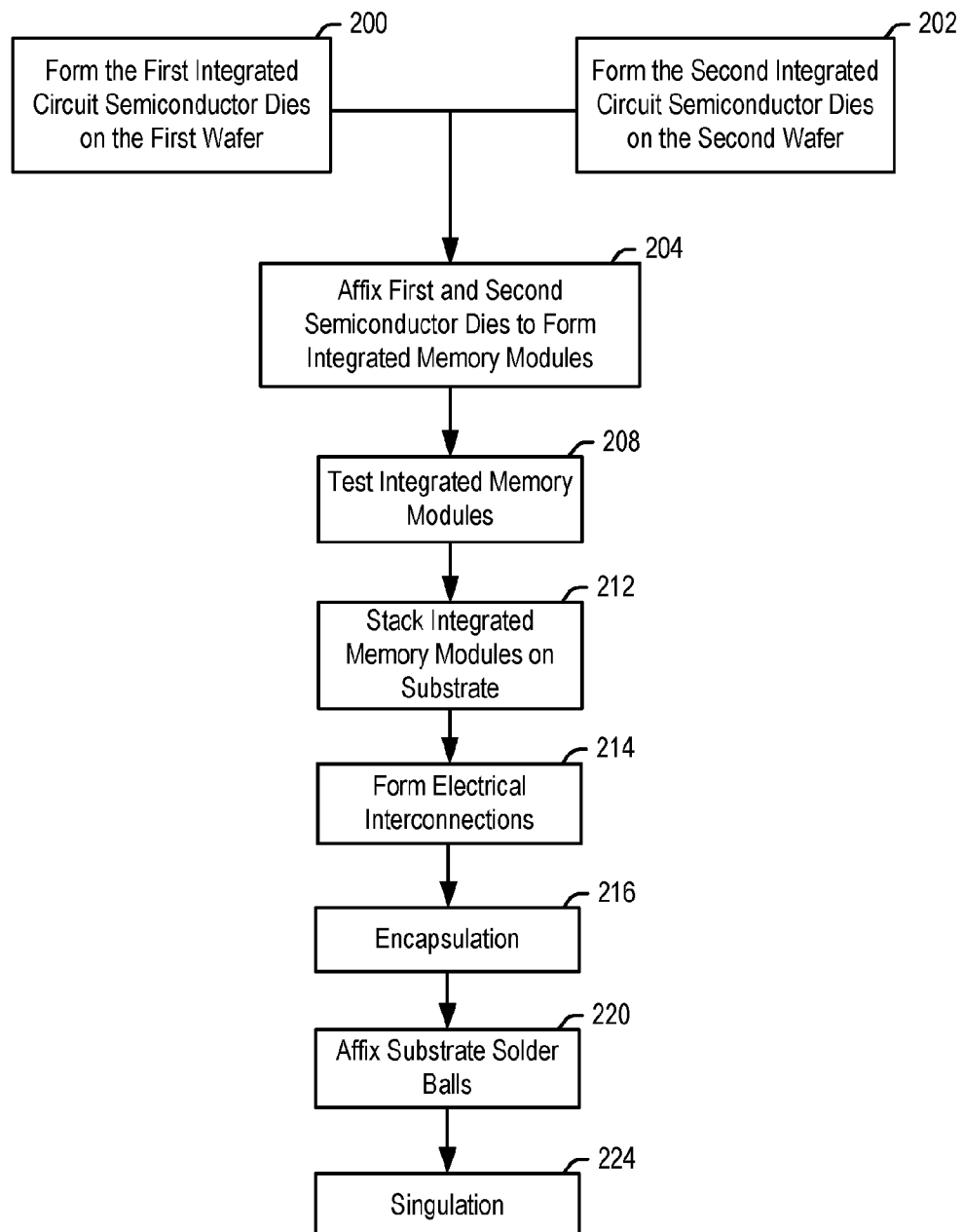
*Fig. 1*

Fig. 2

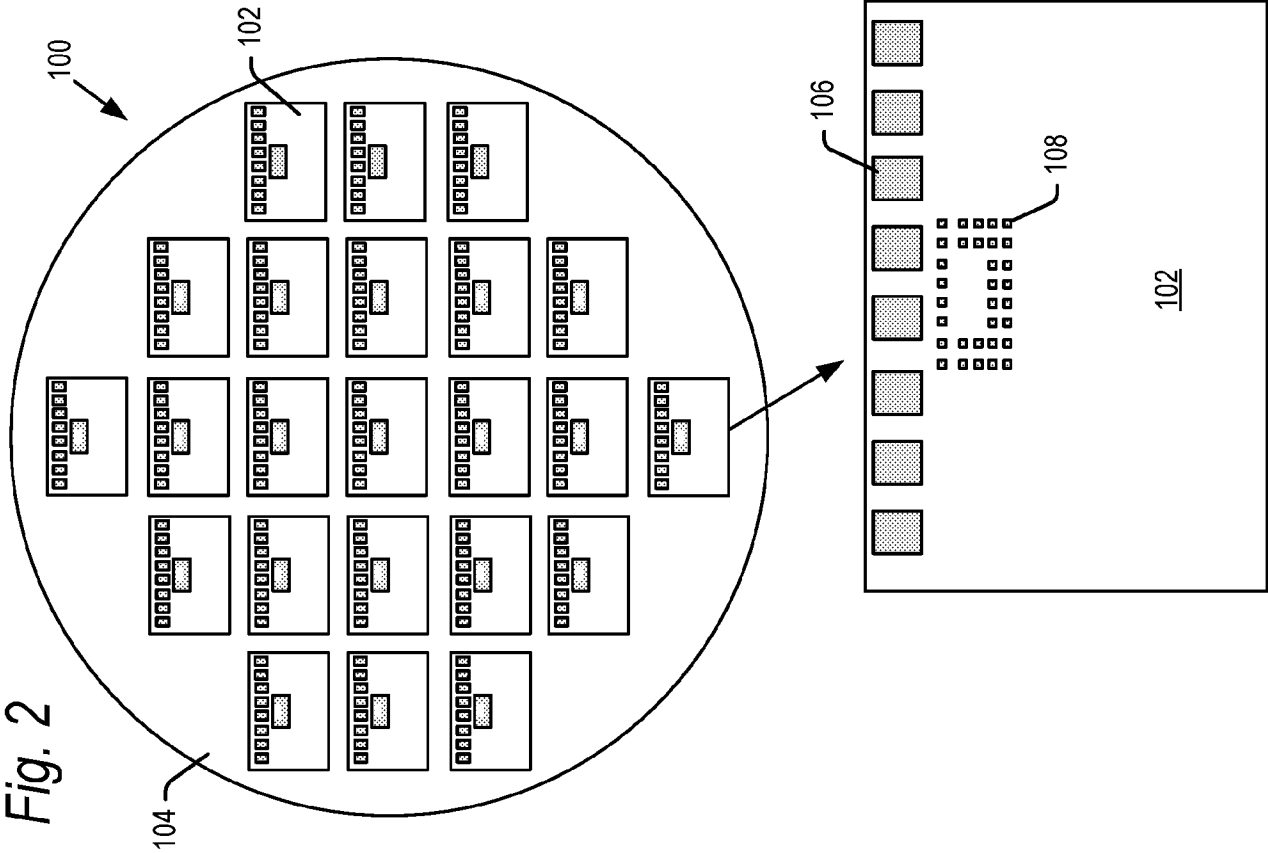
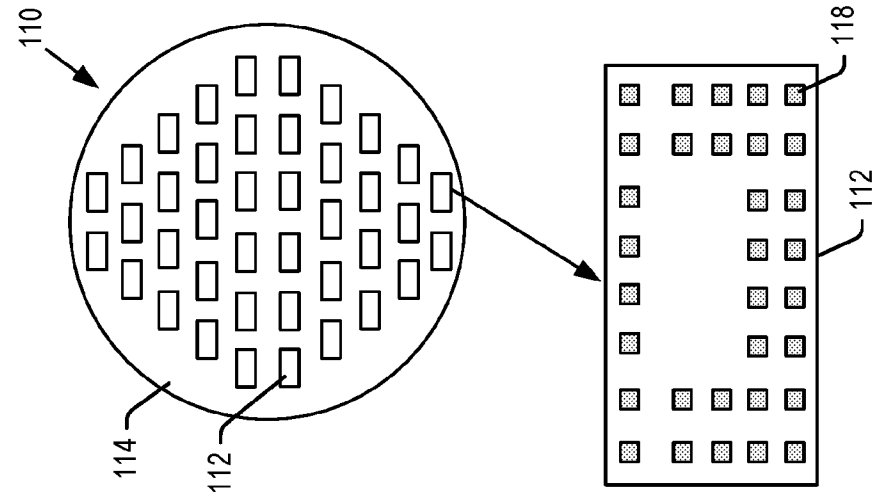


Fig. 3



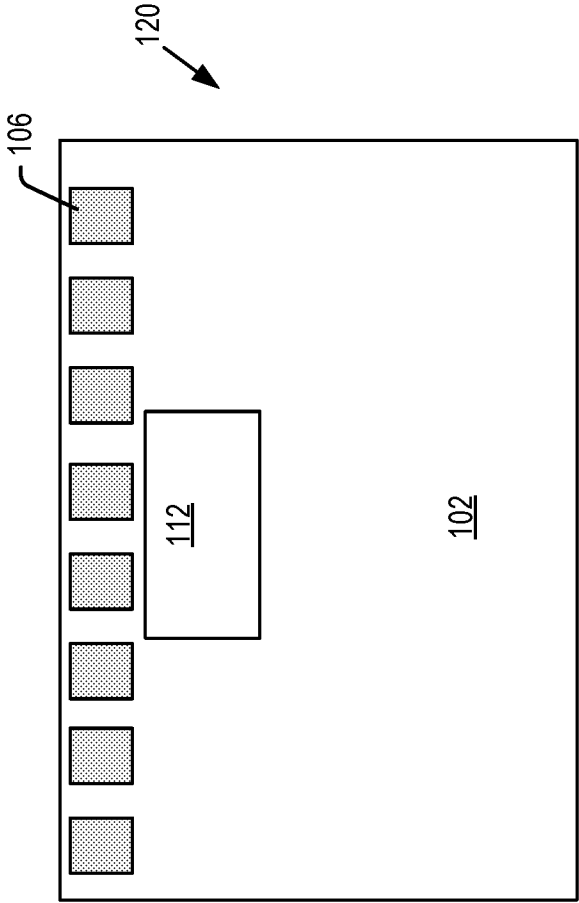
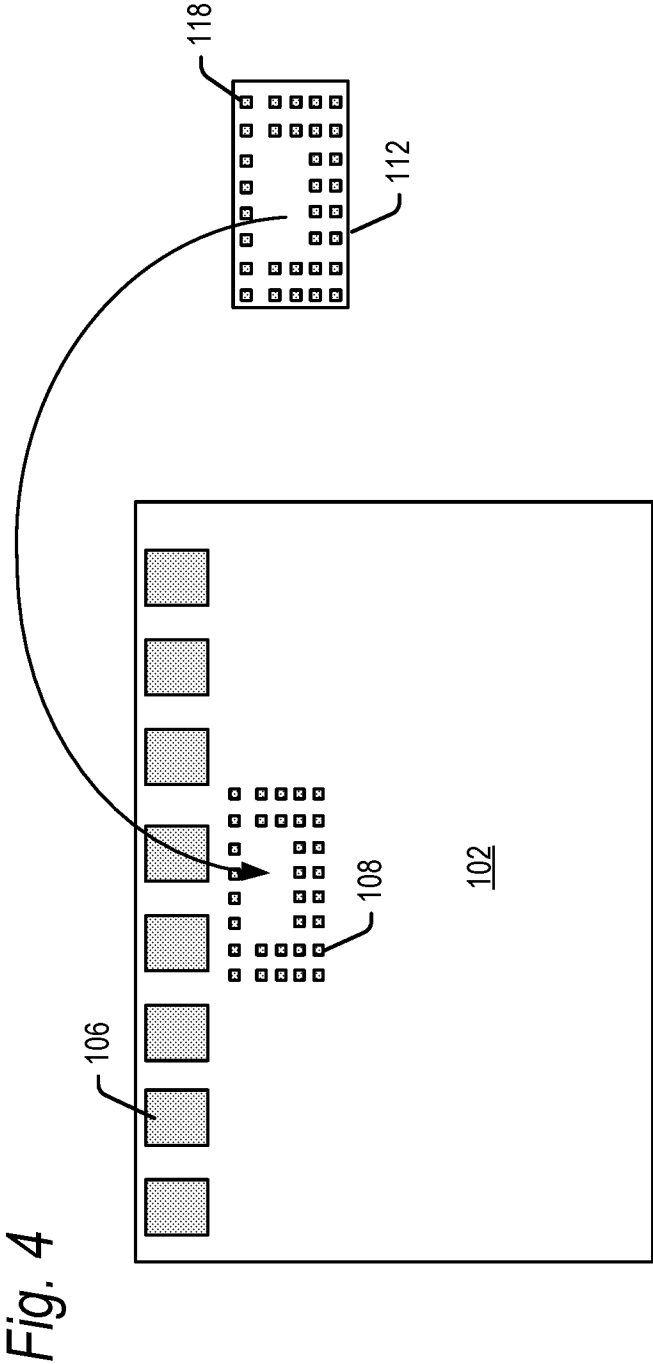


*Fig. 6*

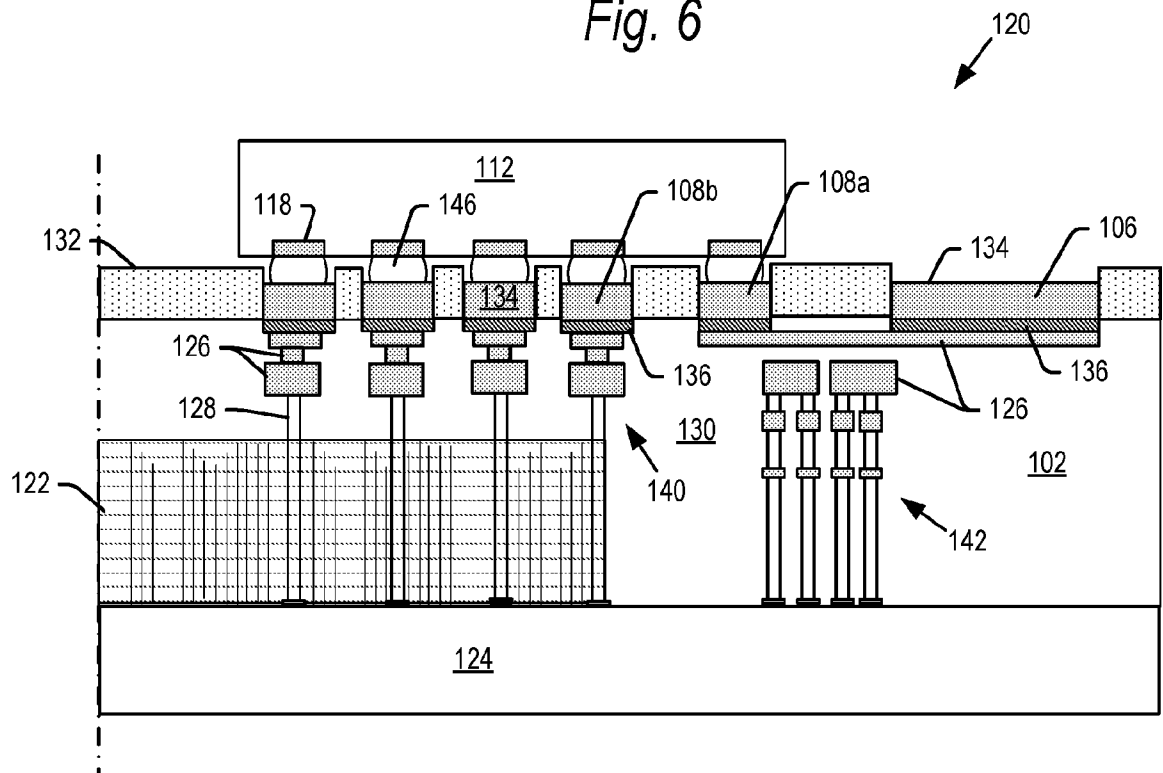


*Fig. 7*

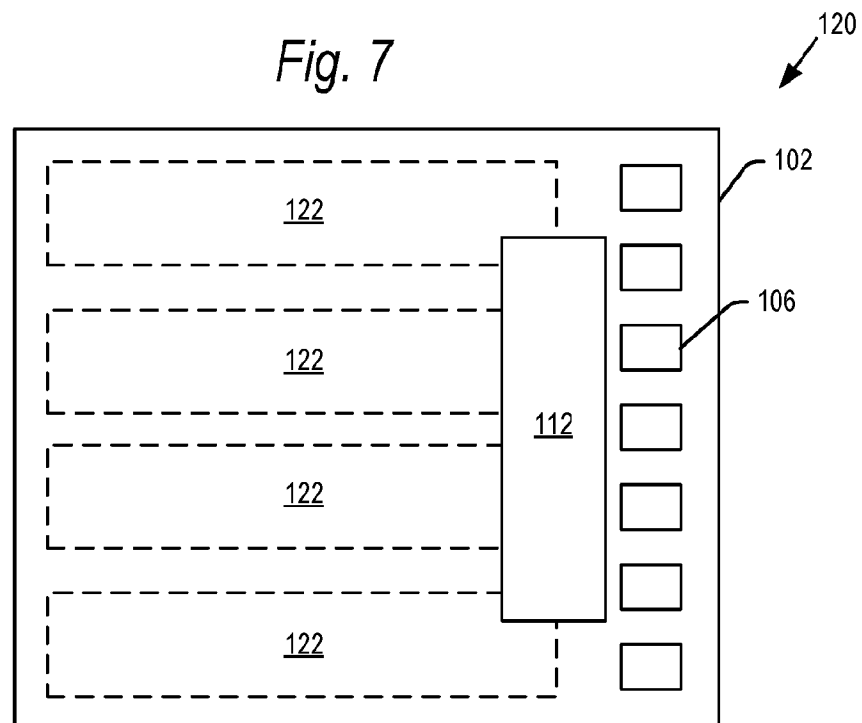


Fig. 8

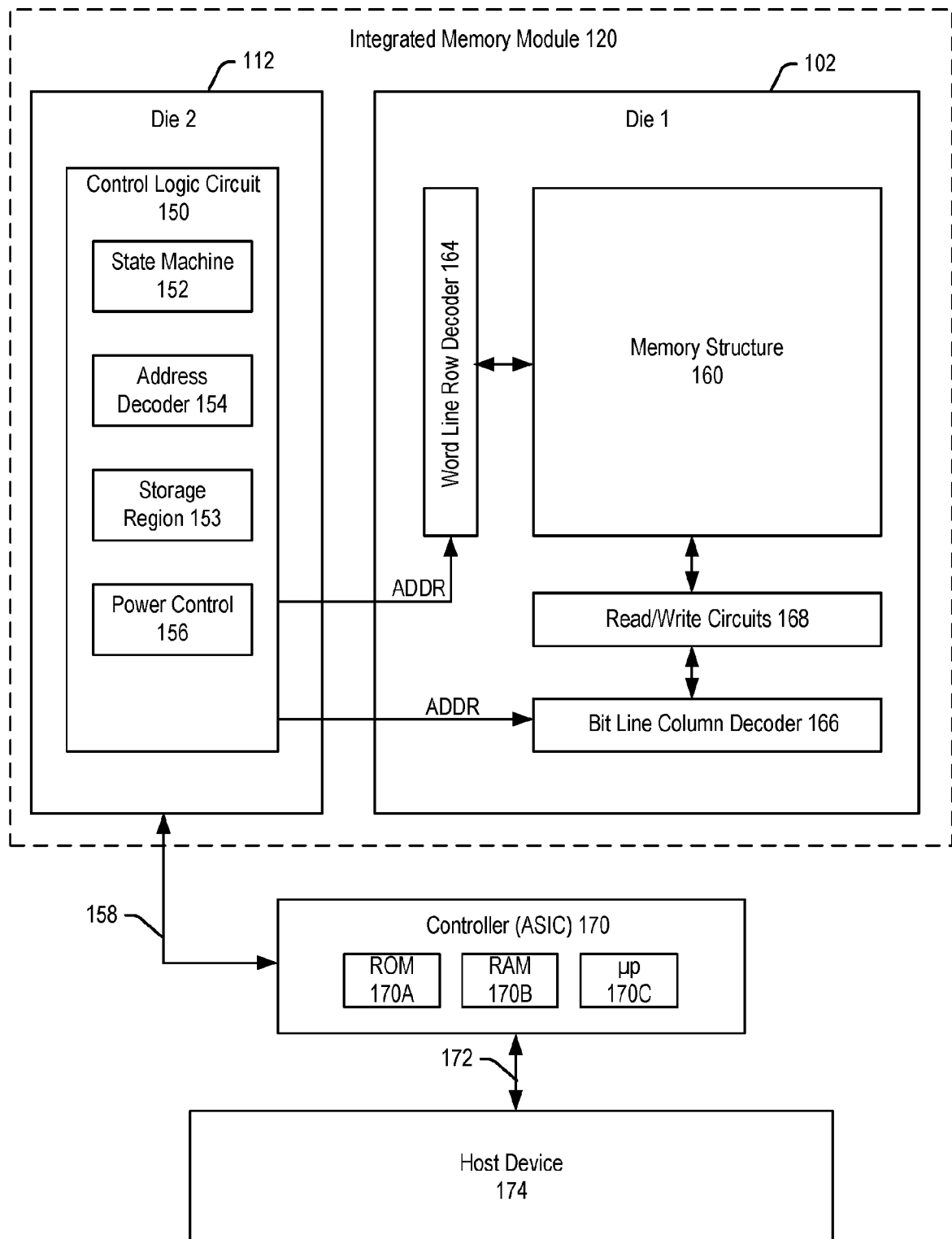


Fig. 9

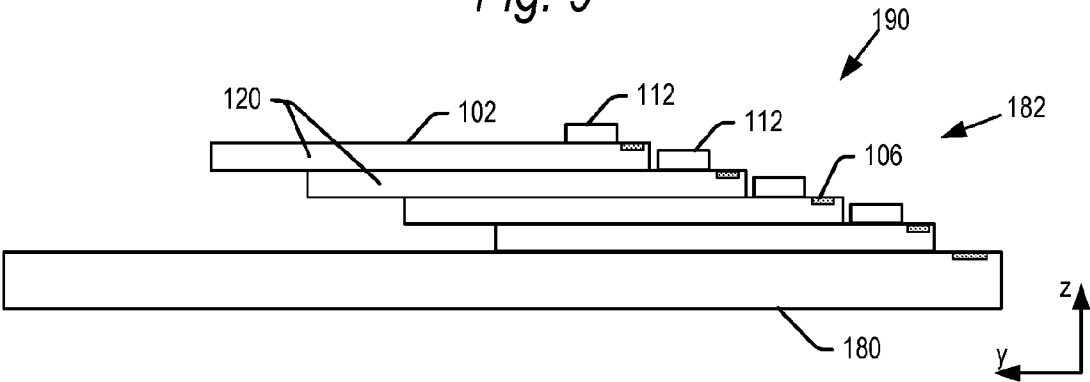
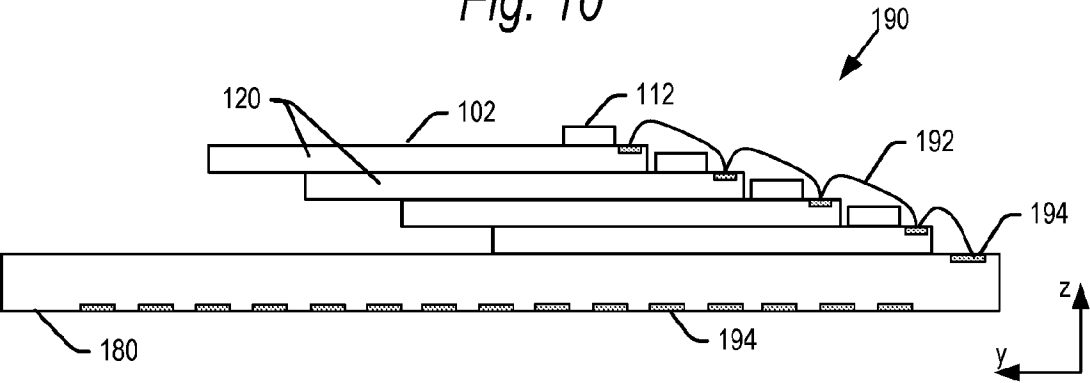


Fig. 10



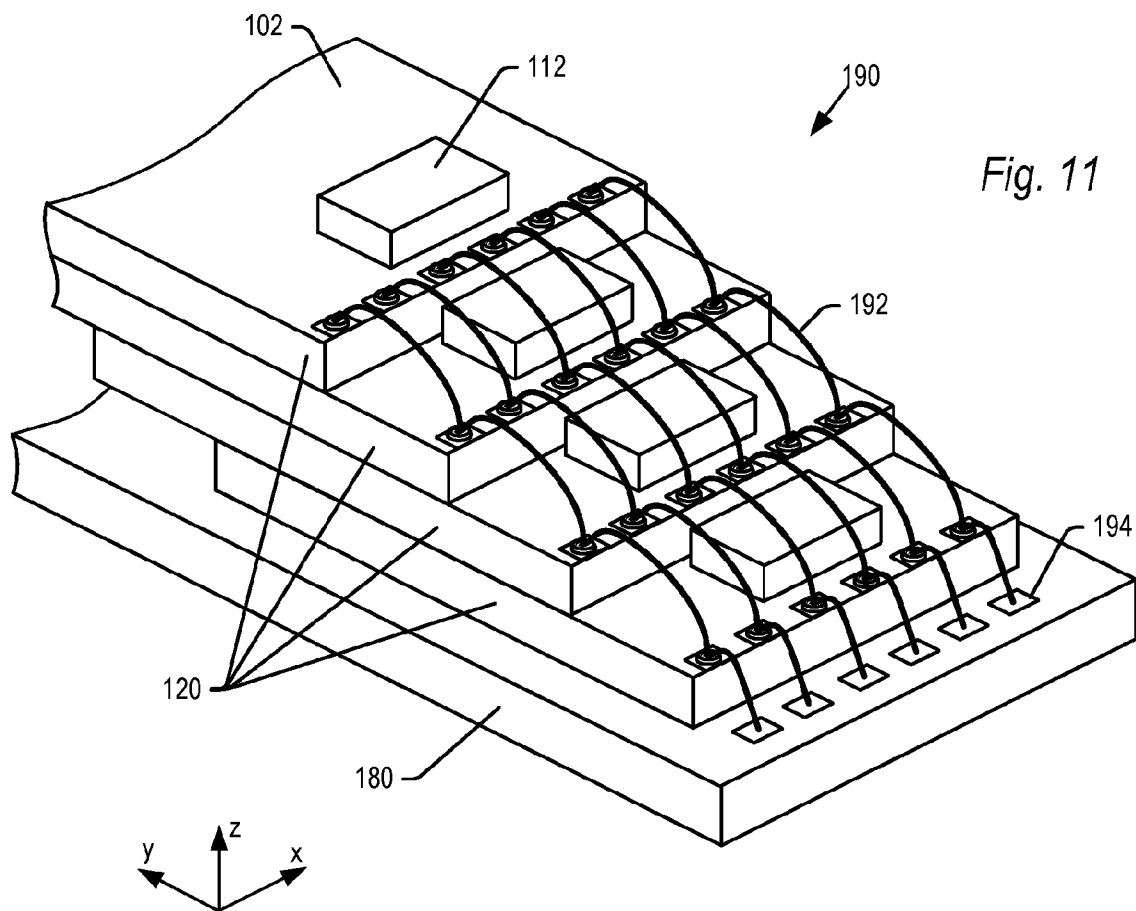


Fig. 12

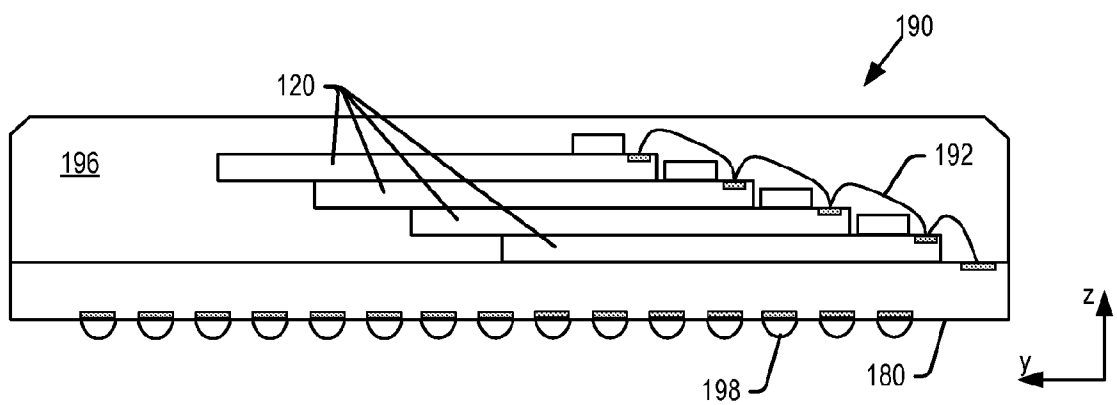


Fig. 13

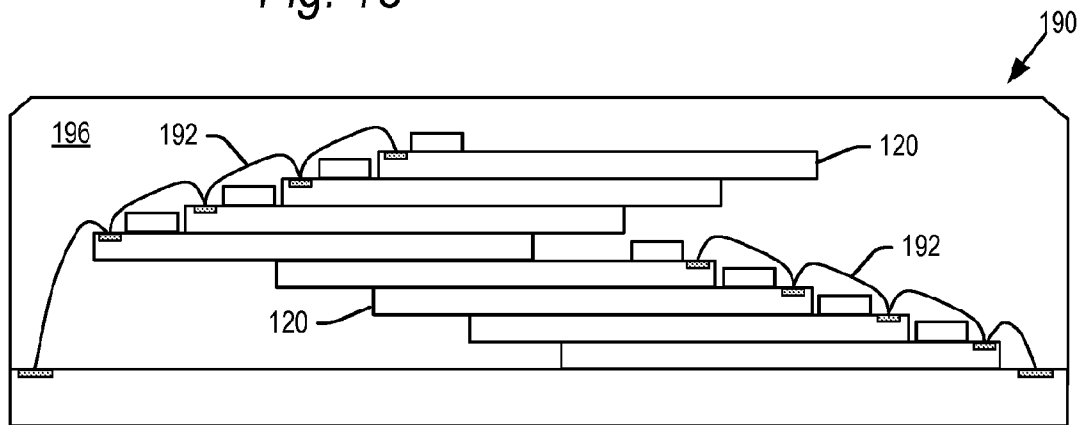


Fig. 14

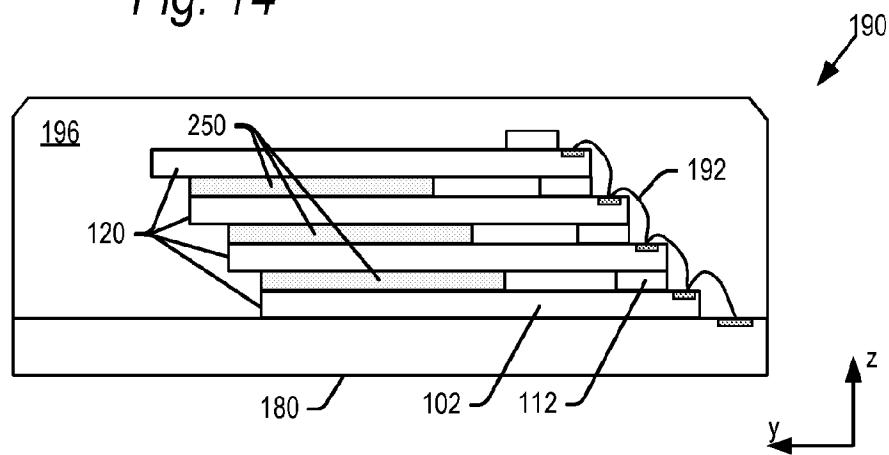


Fig. 15

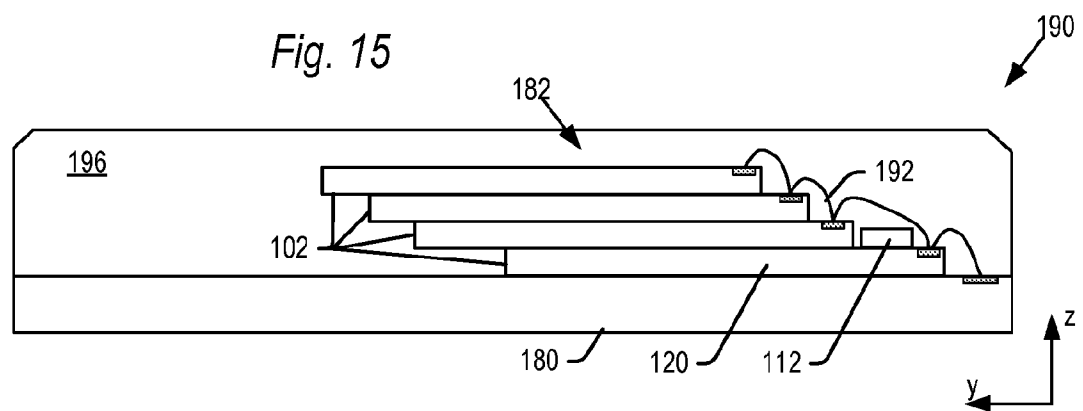


Fig. 16

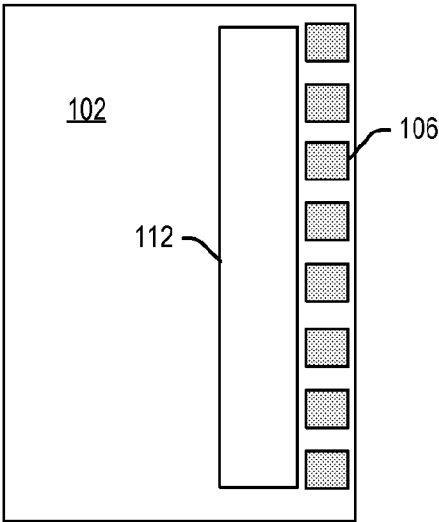


Fig. 17

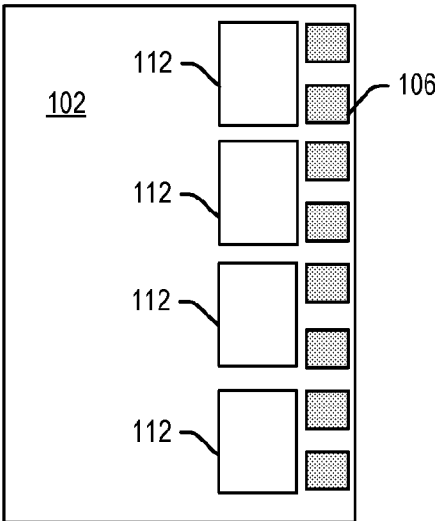


Fig. 18

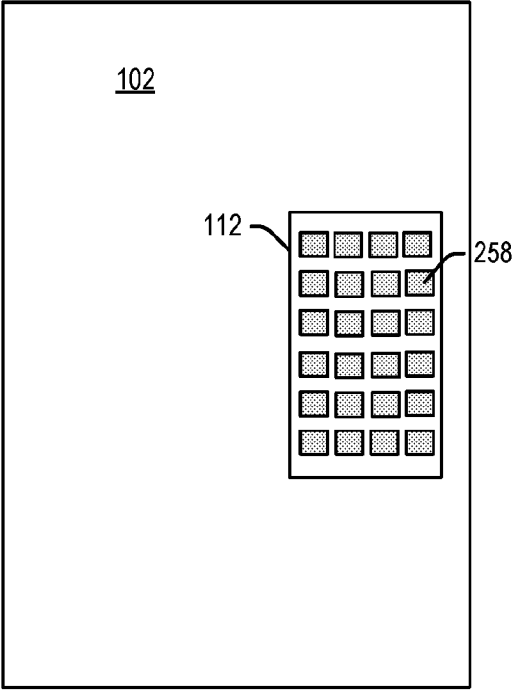


Fig. 19

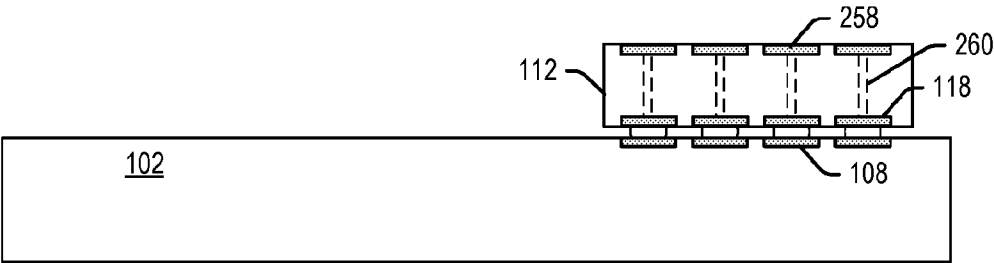


Fig. 20

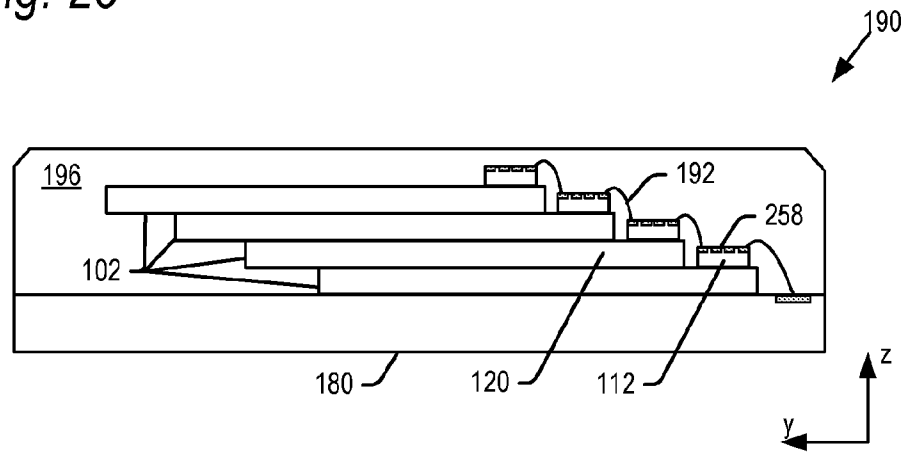
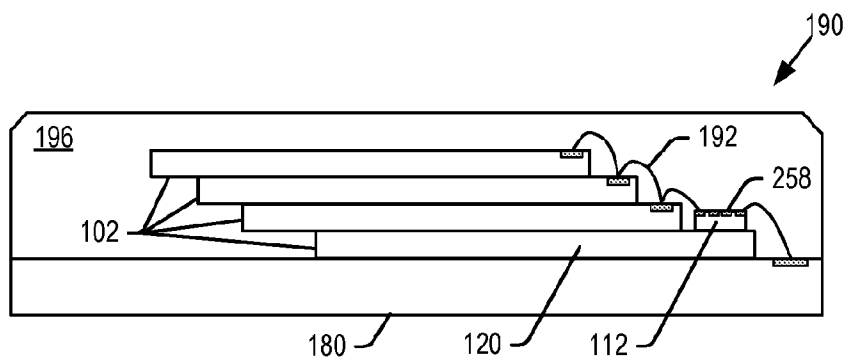


Fig. 21



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Fig. 22

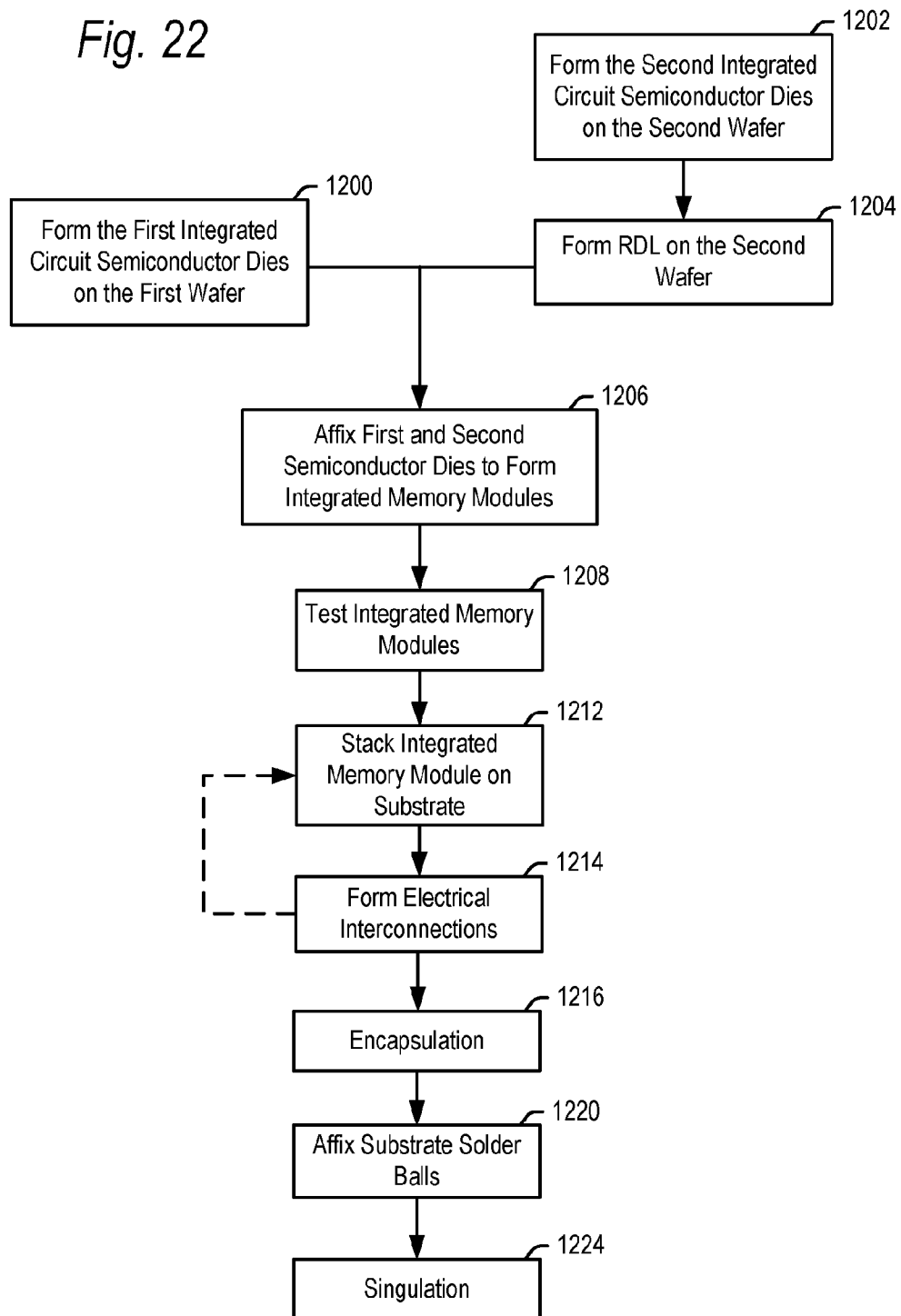


Fig. 23

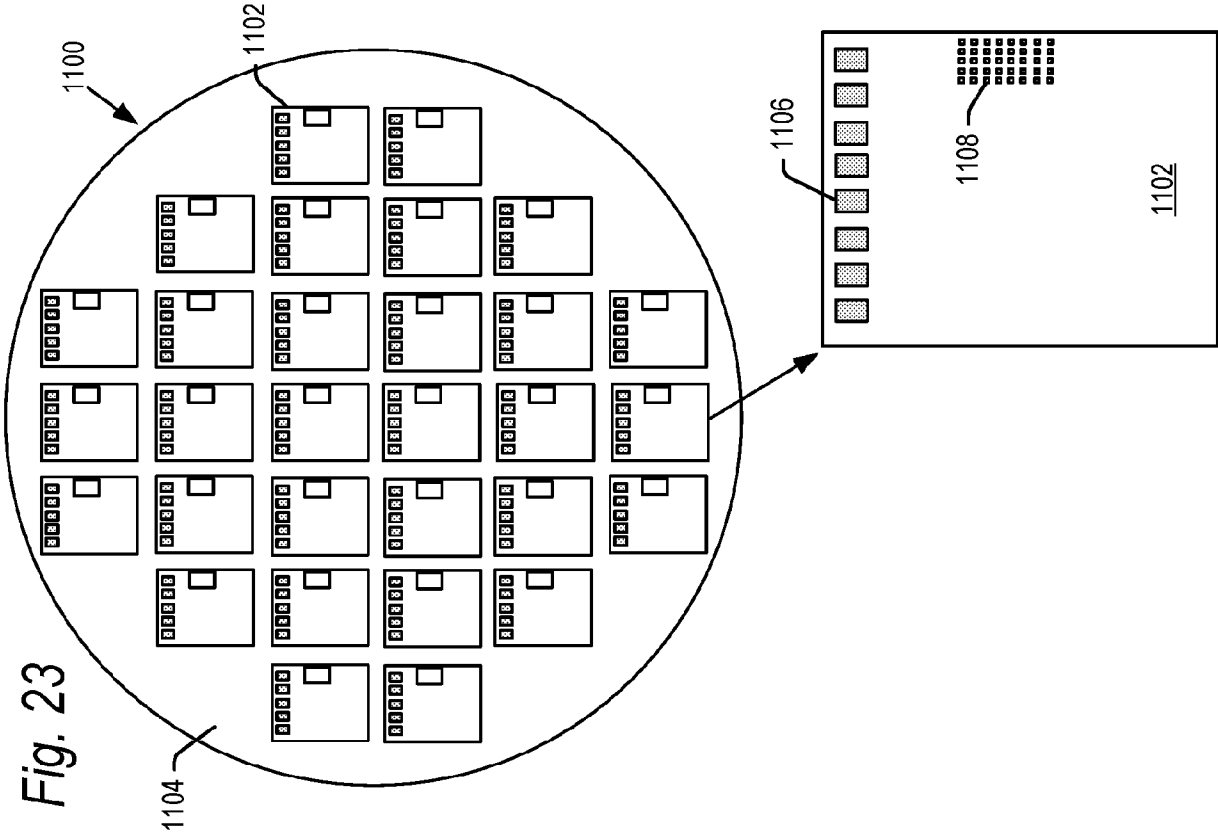


Fig. 24

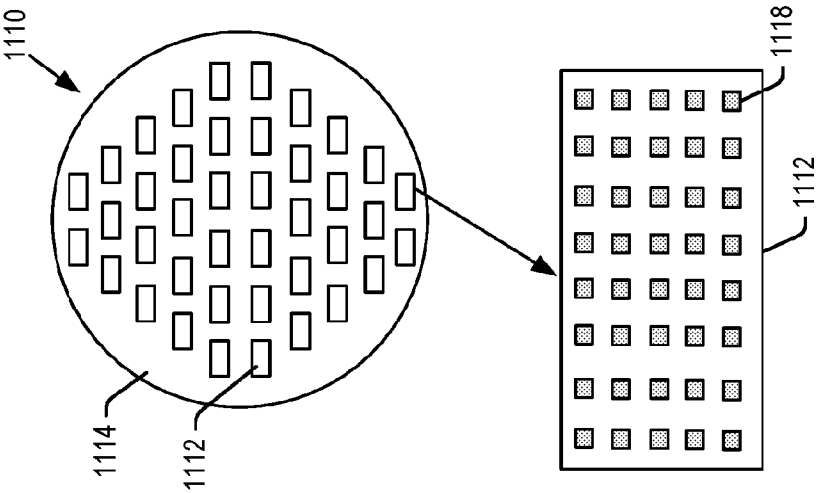


Fig. 25

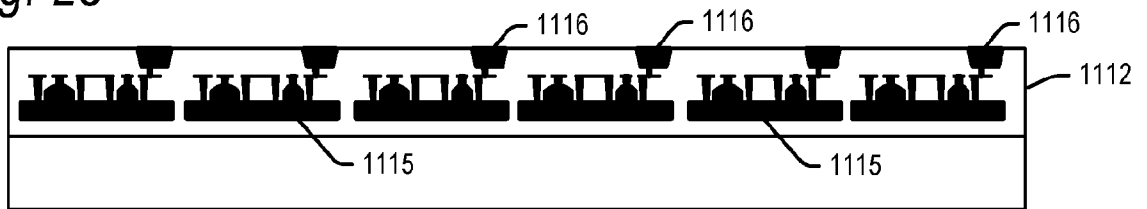


Fig. 26

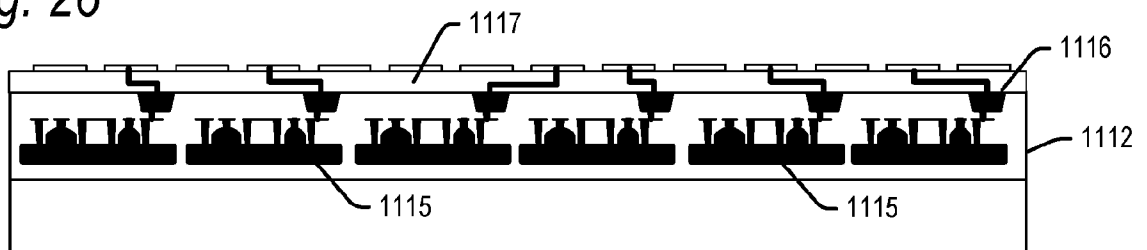


Fig. 27

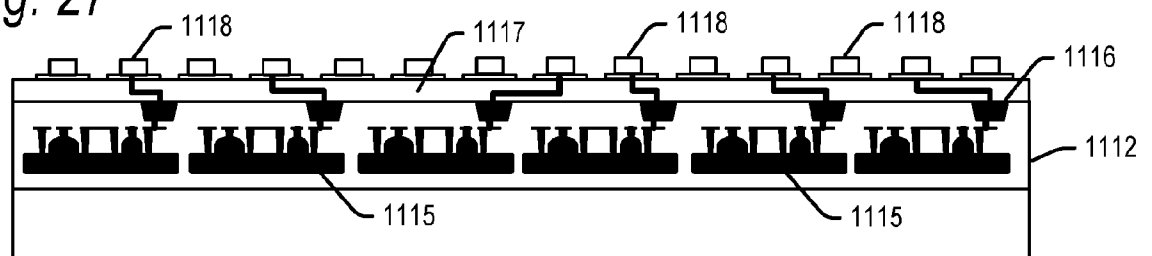


Fig. 28

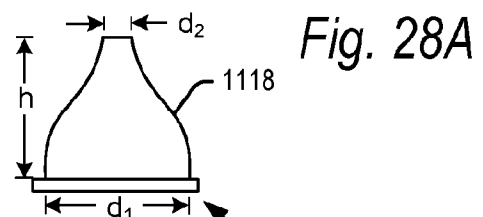
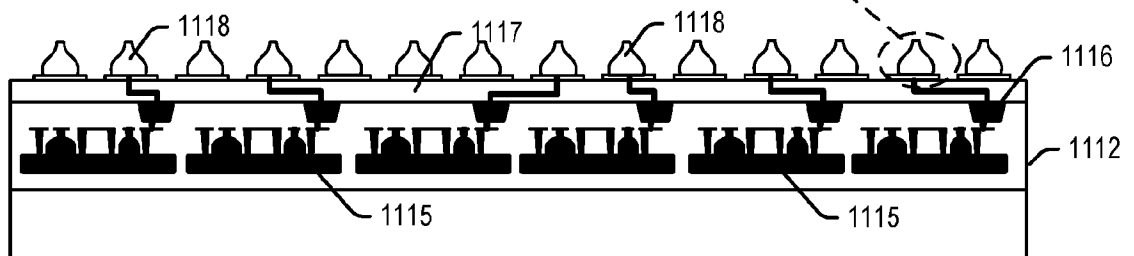


Fig. 28A

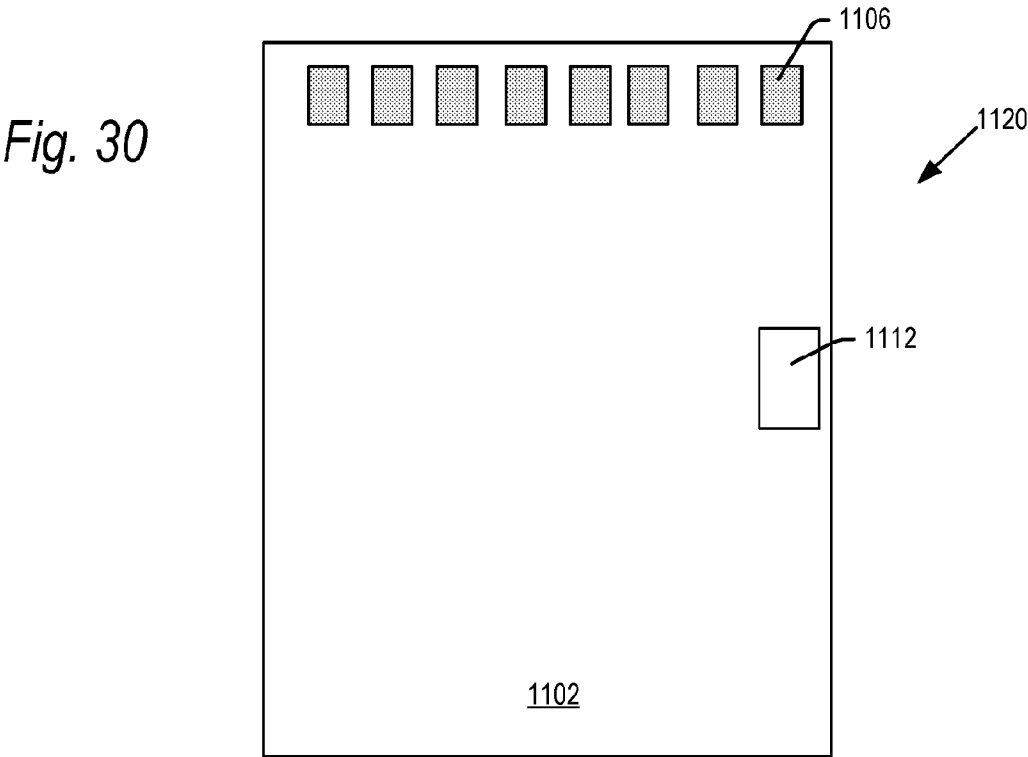
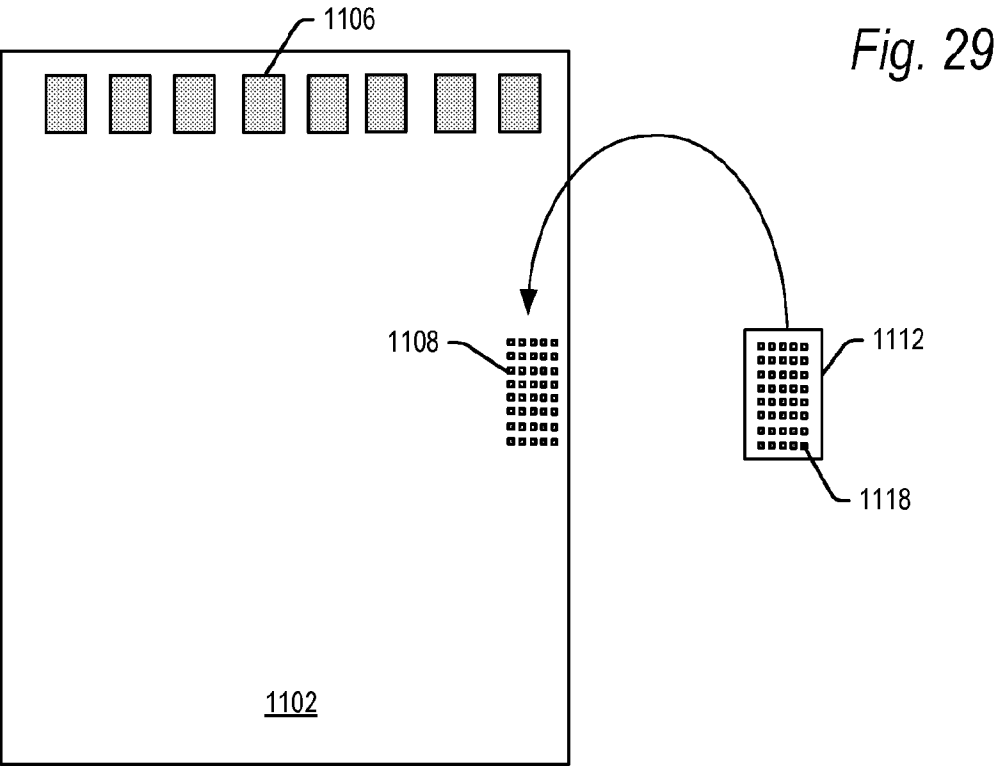


Fig. 31

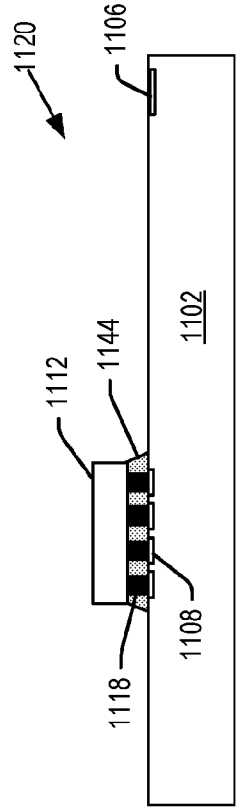
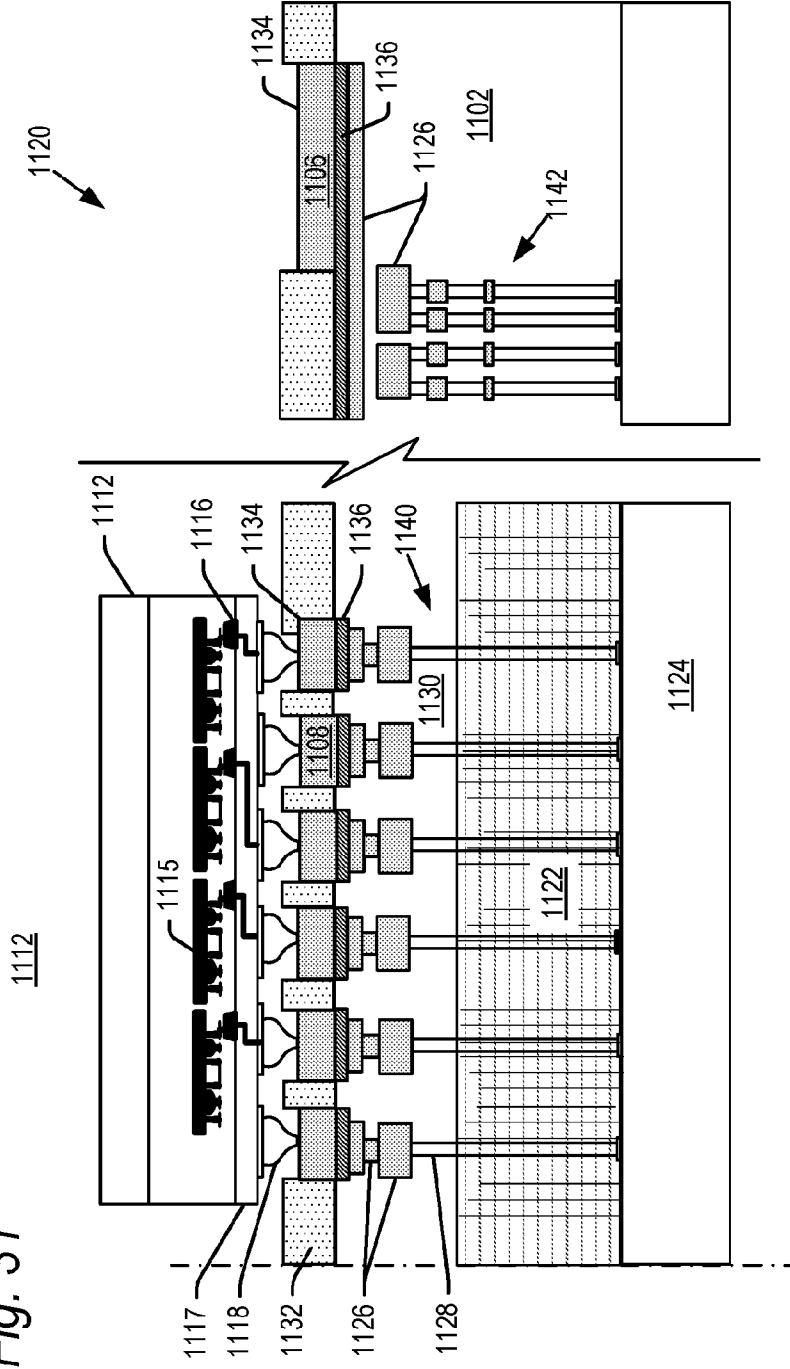


Fig. 32

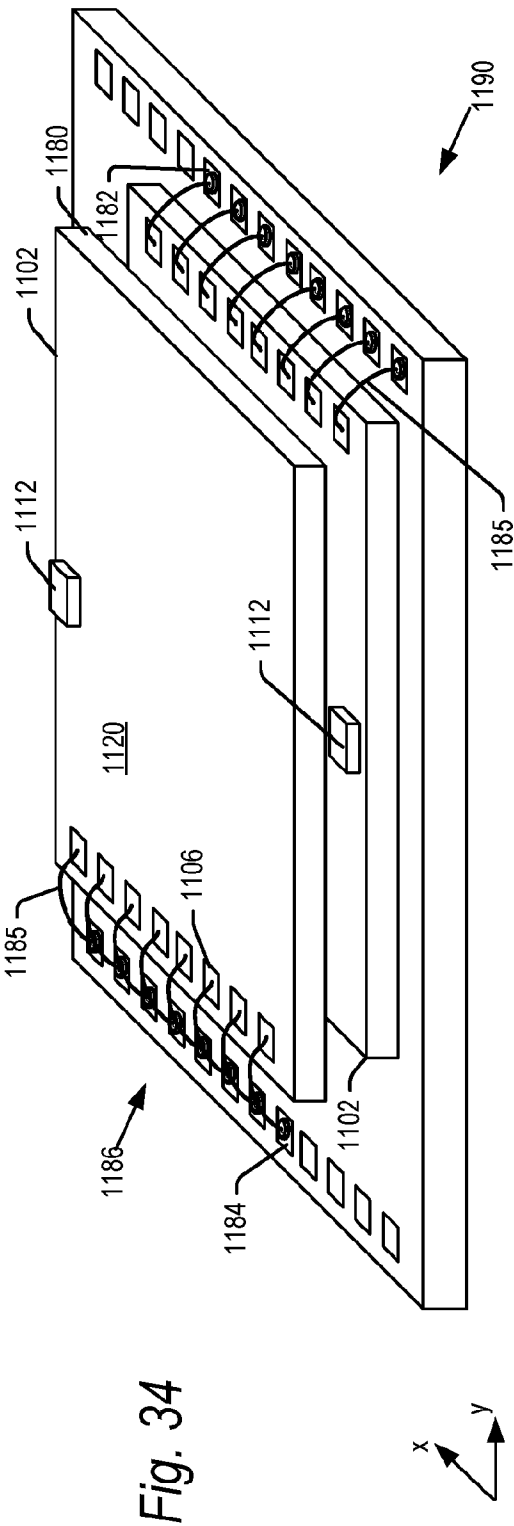
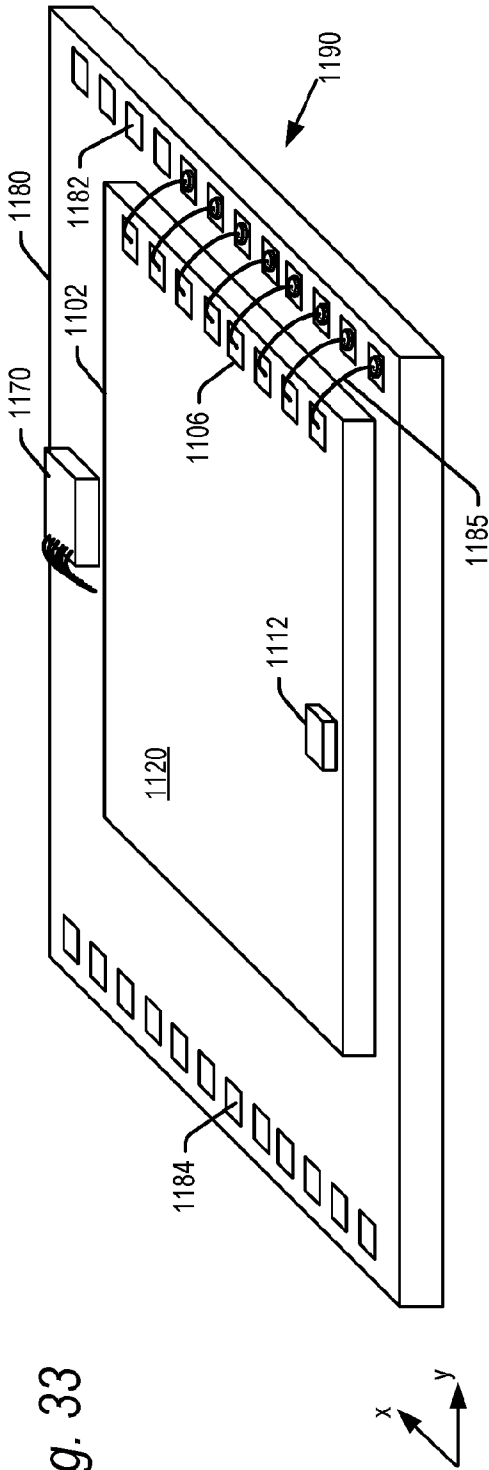
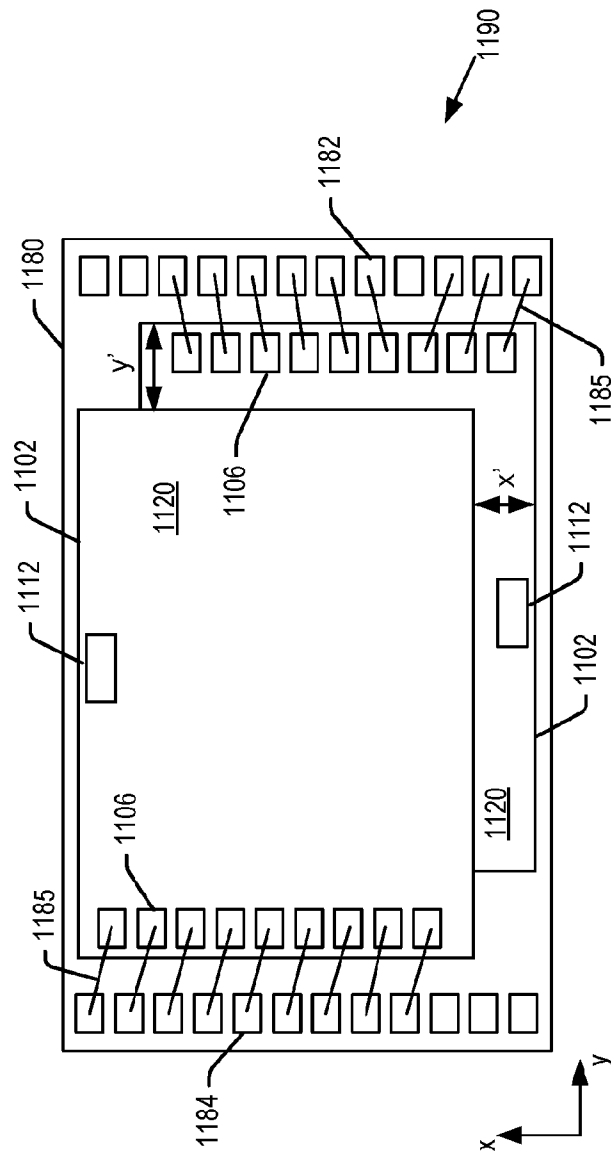
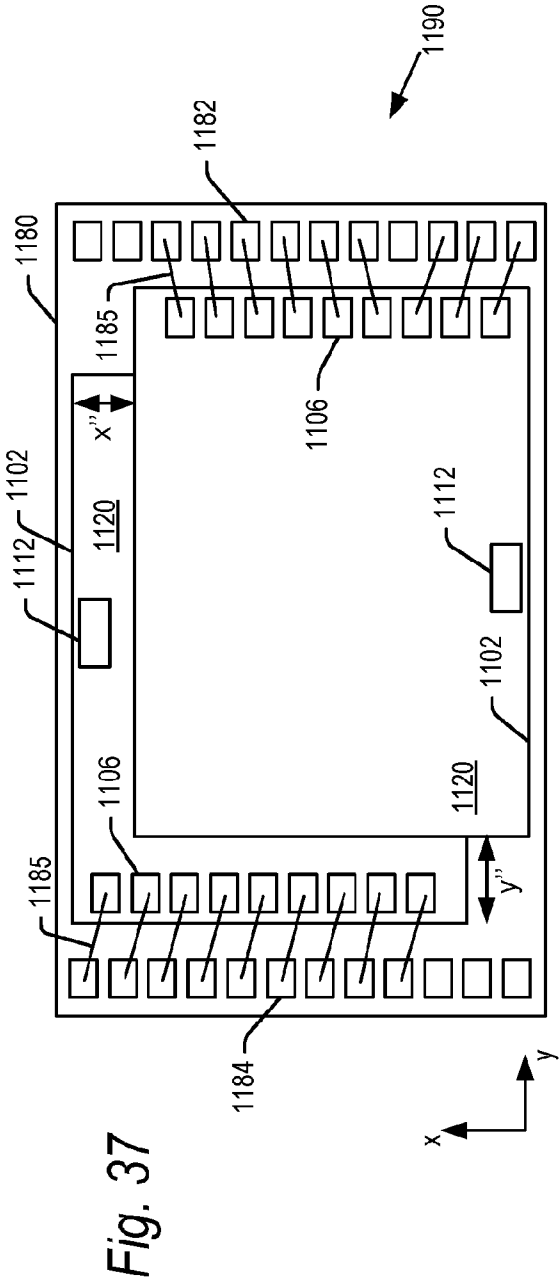
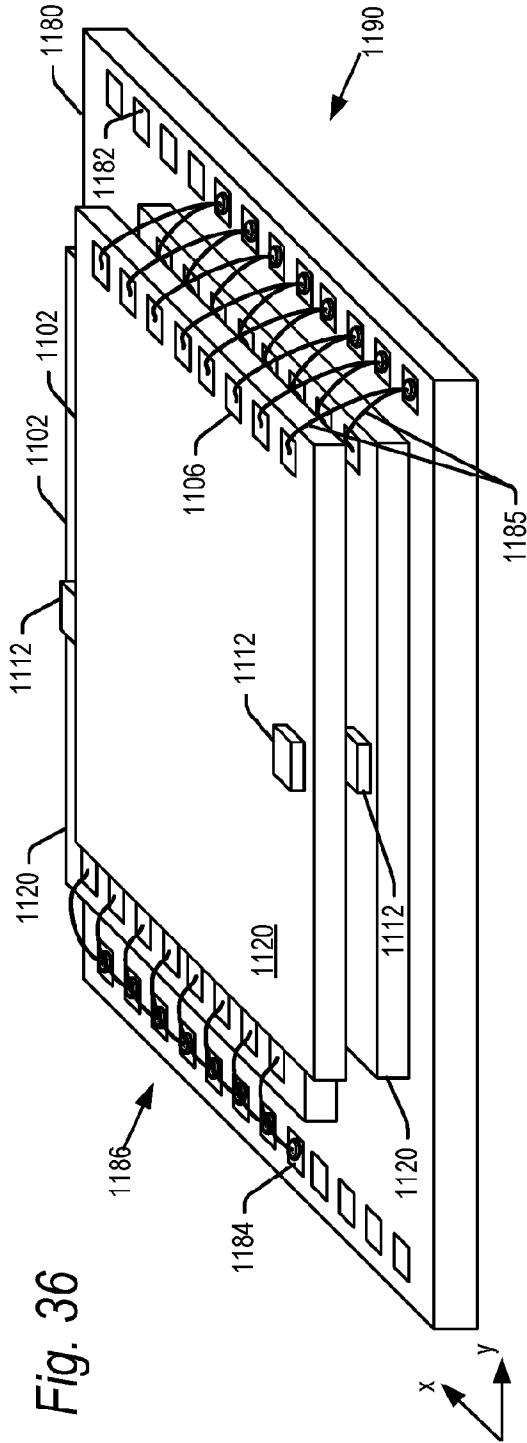


Fig. 35





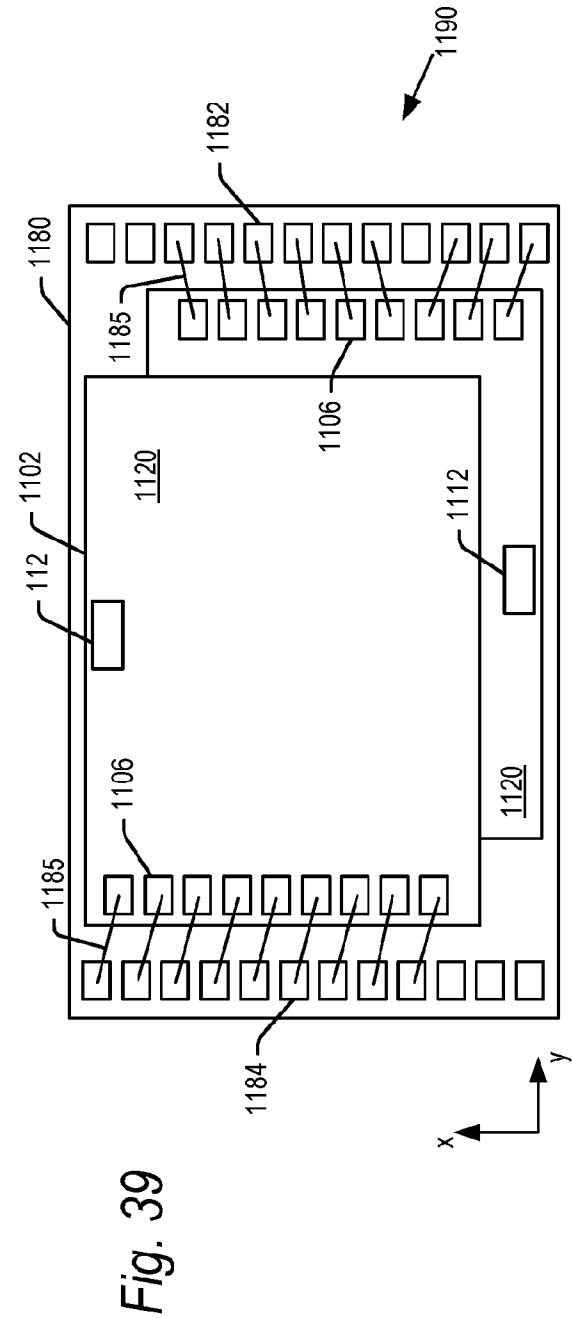
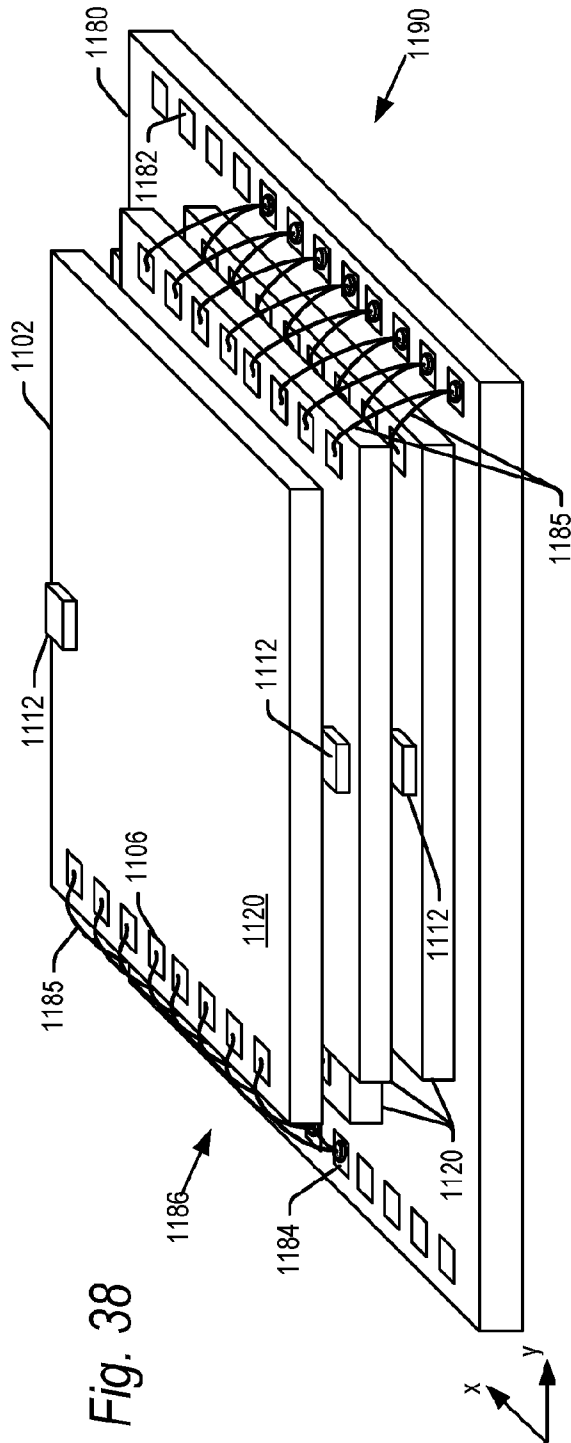


Fig. 40

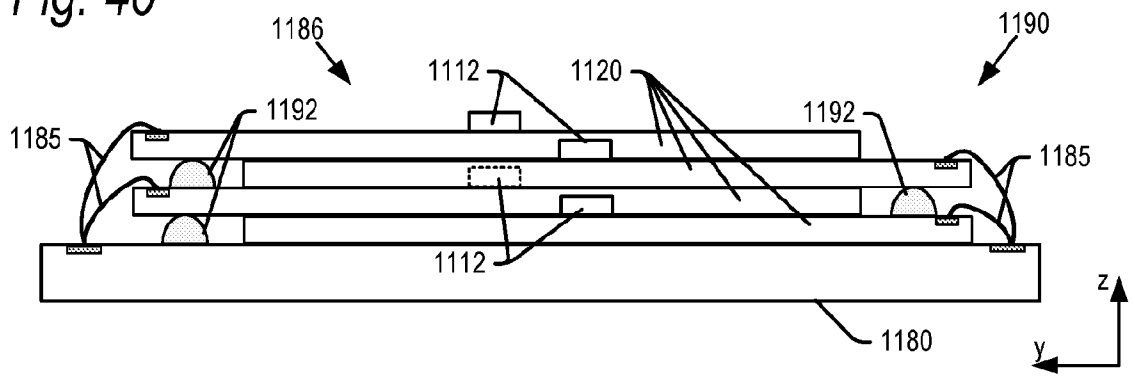
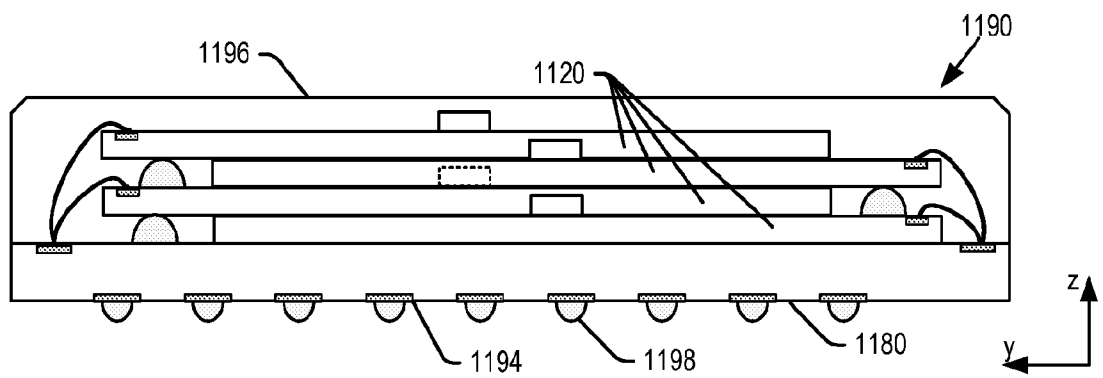


Fig. 41



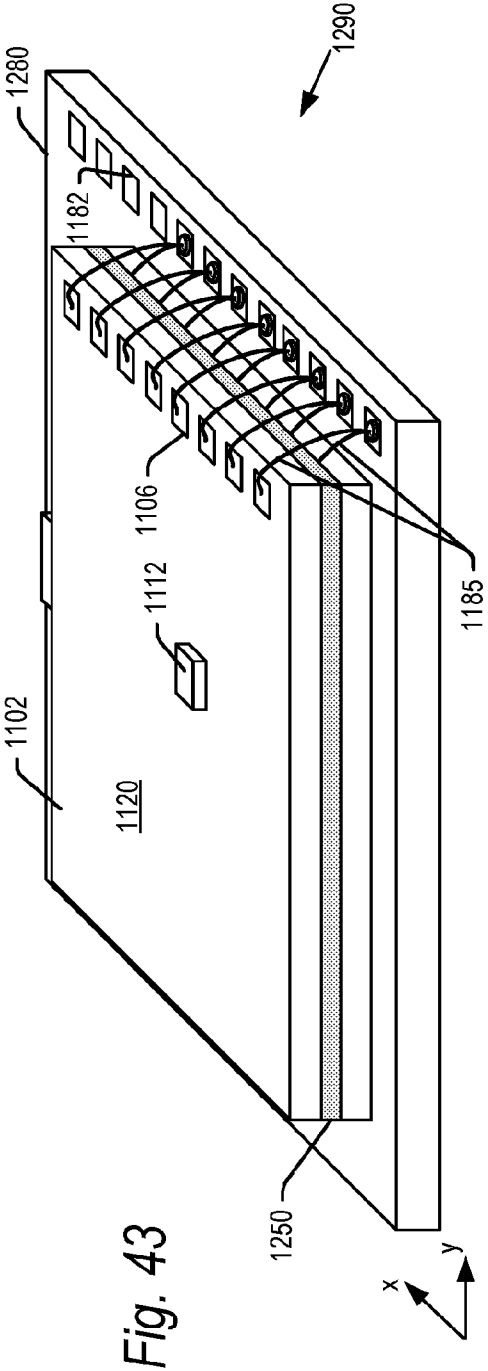
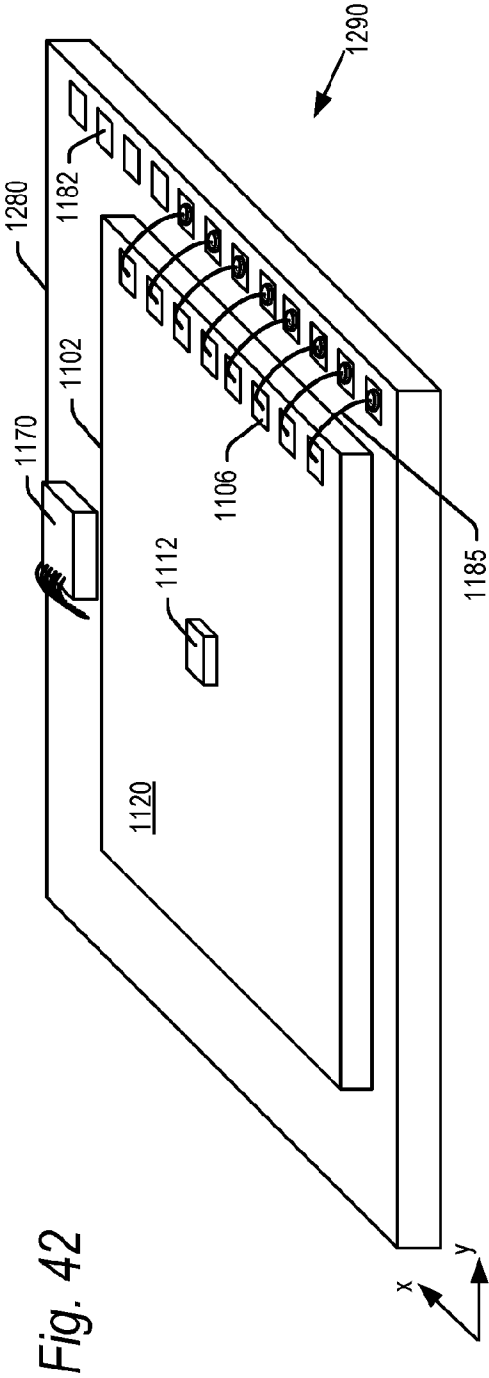


Fig. 44

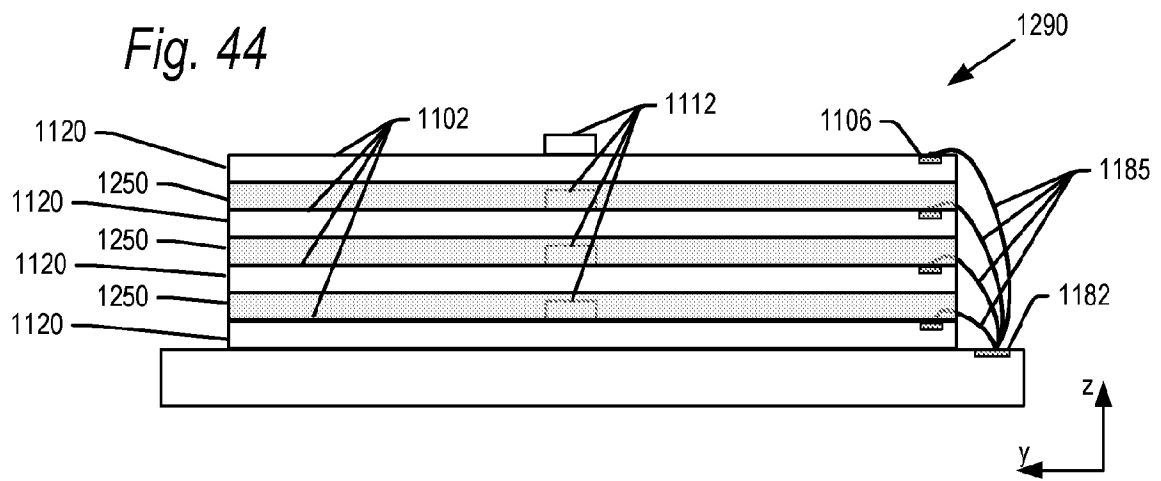


Fig. 45

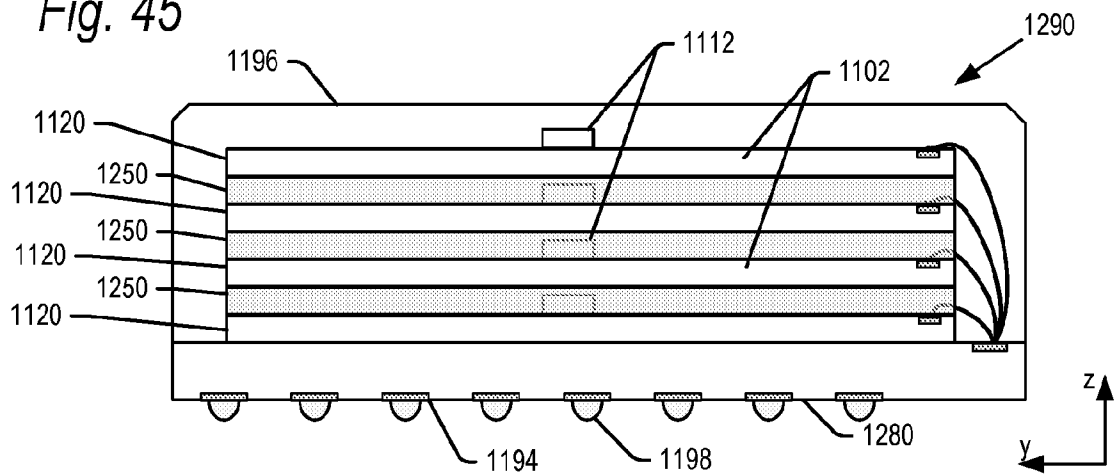


Fig. 46

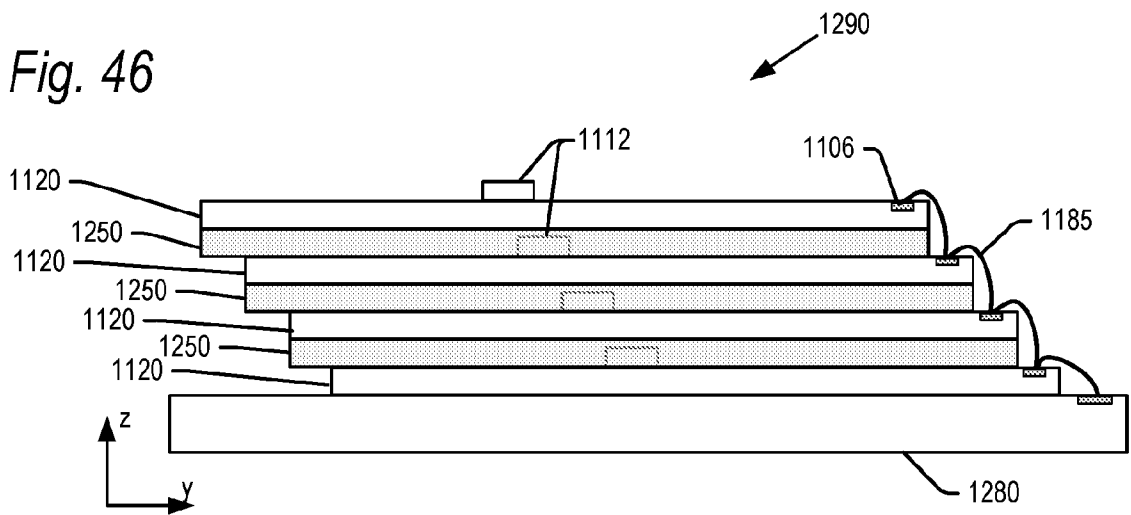


Fig. 47

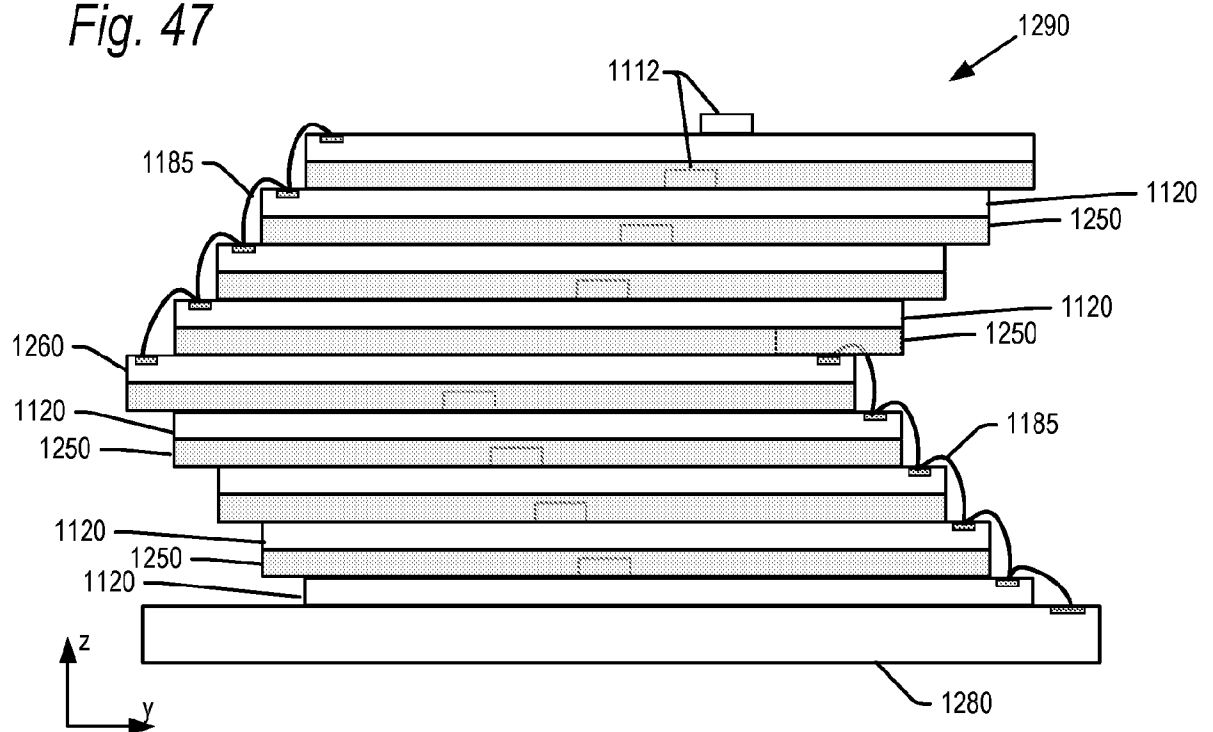


Fig. 48

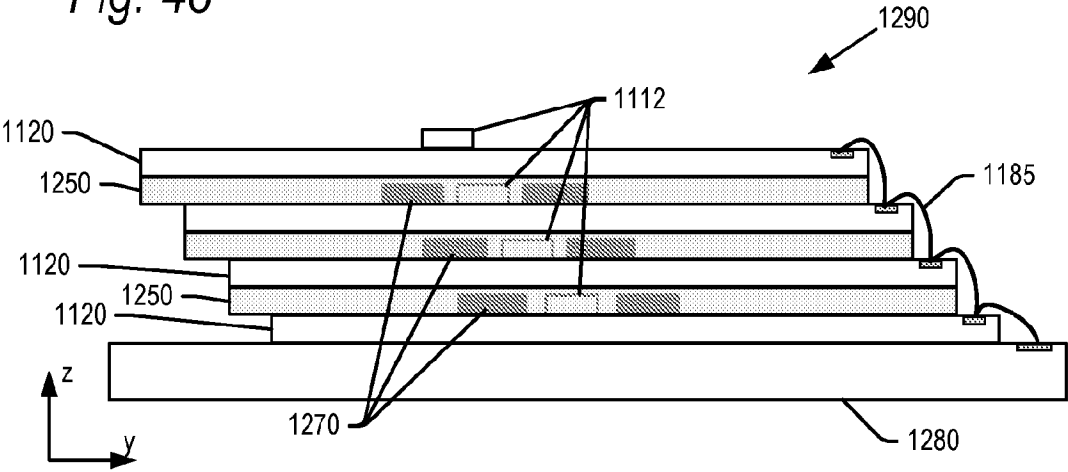


Fig. 49

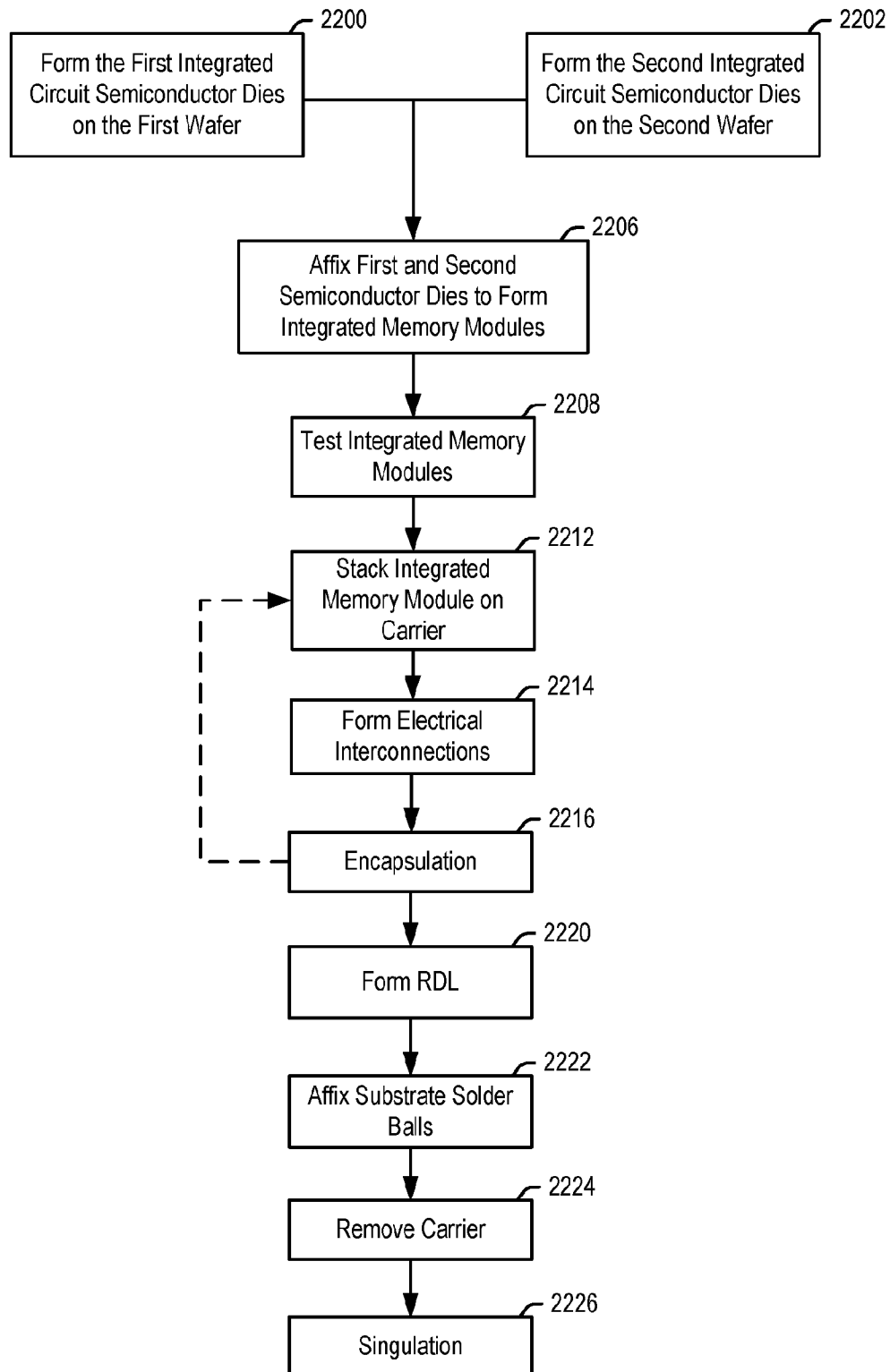


*Fig. 50*  
*(Step 214)*

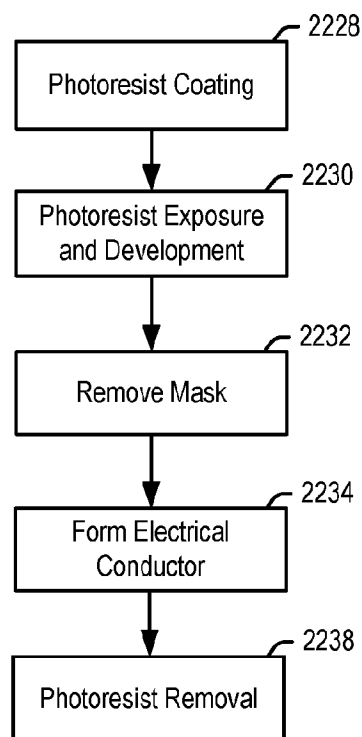


Fig. 52

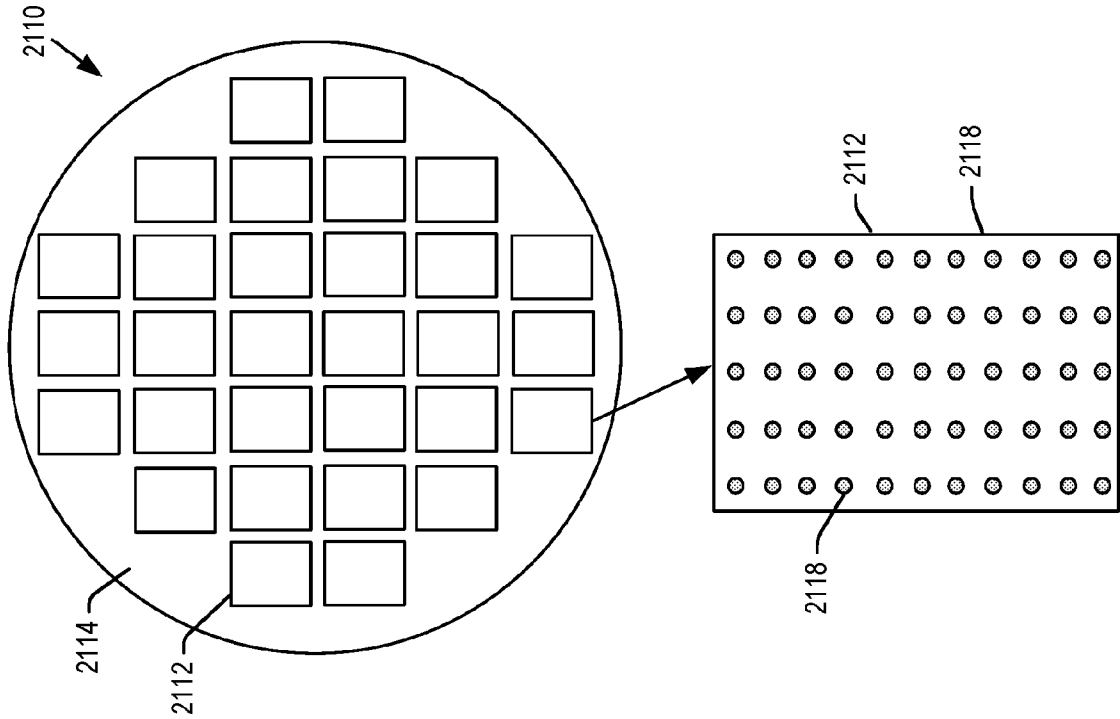
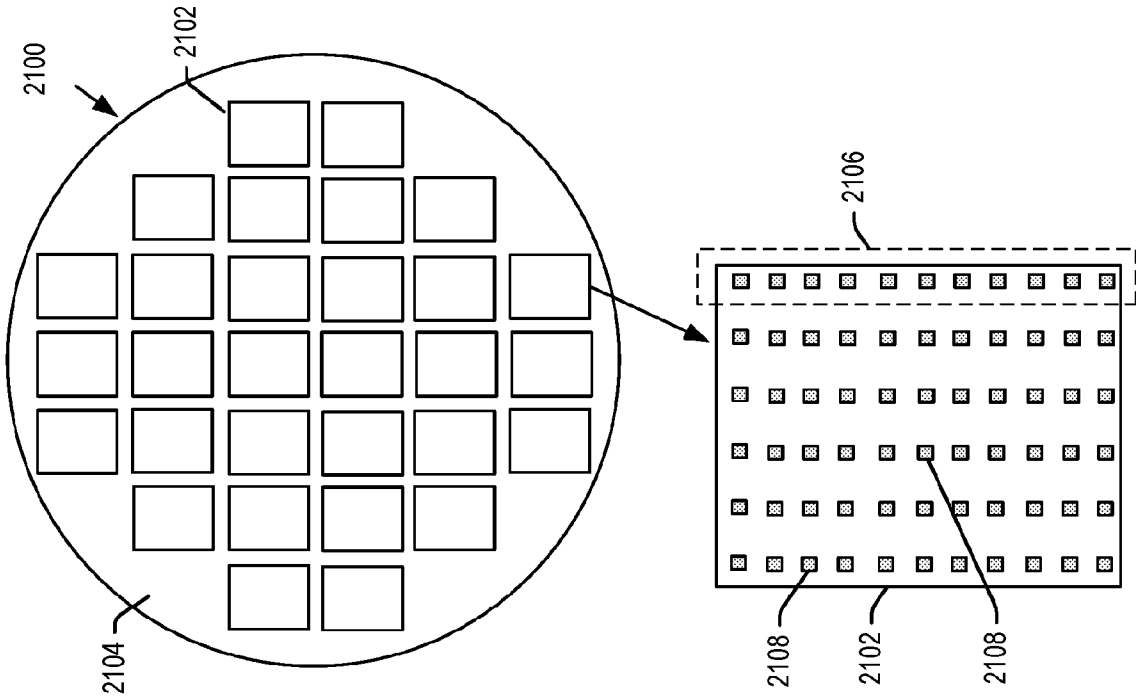


Fig. 51



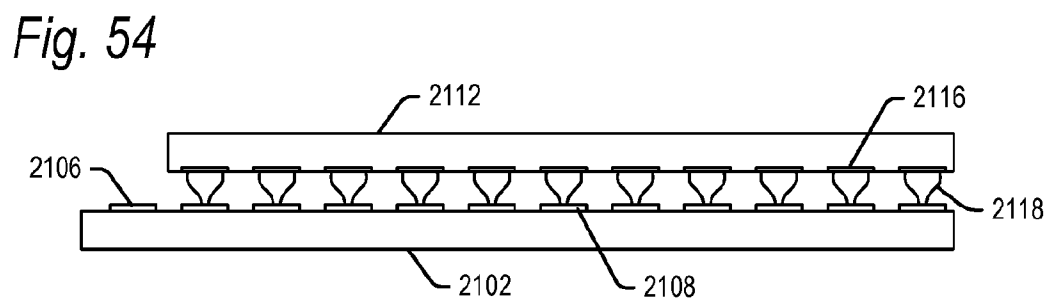
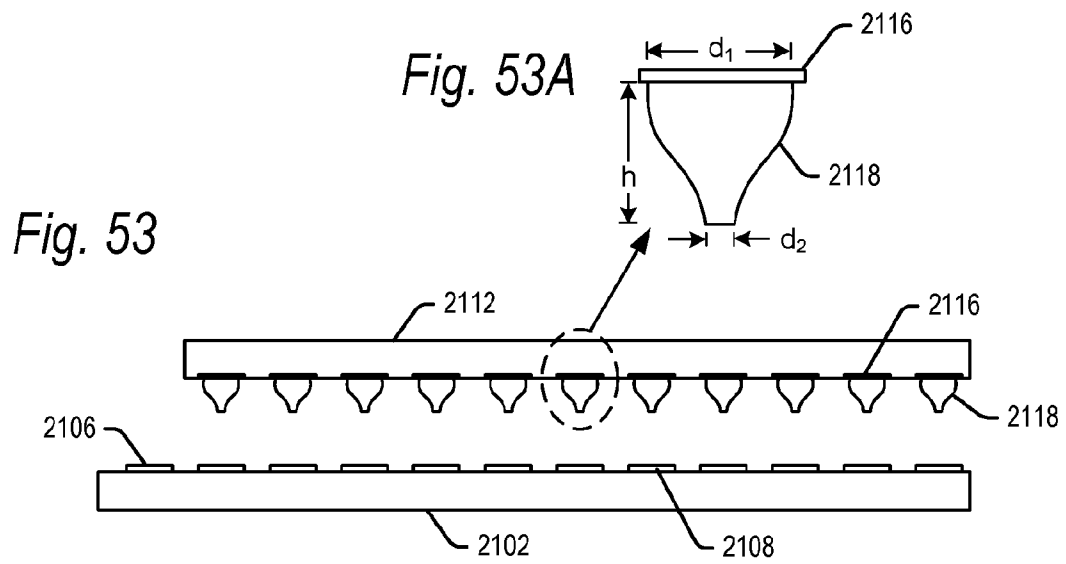


Fig. 55

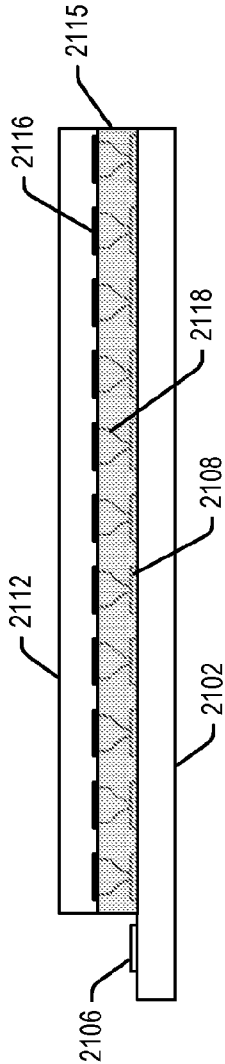


Fig. 56

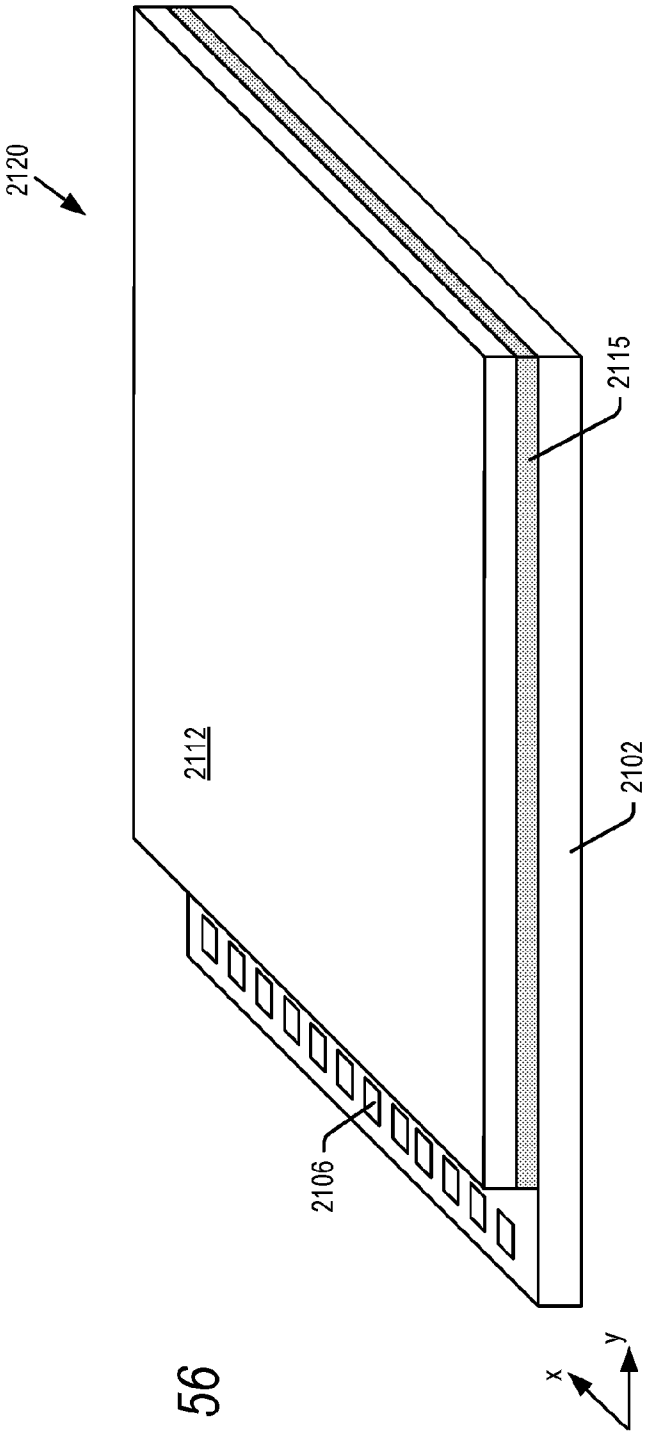


Fig. 57

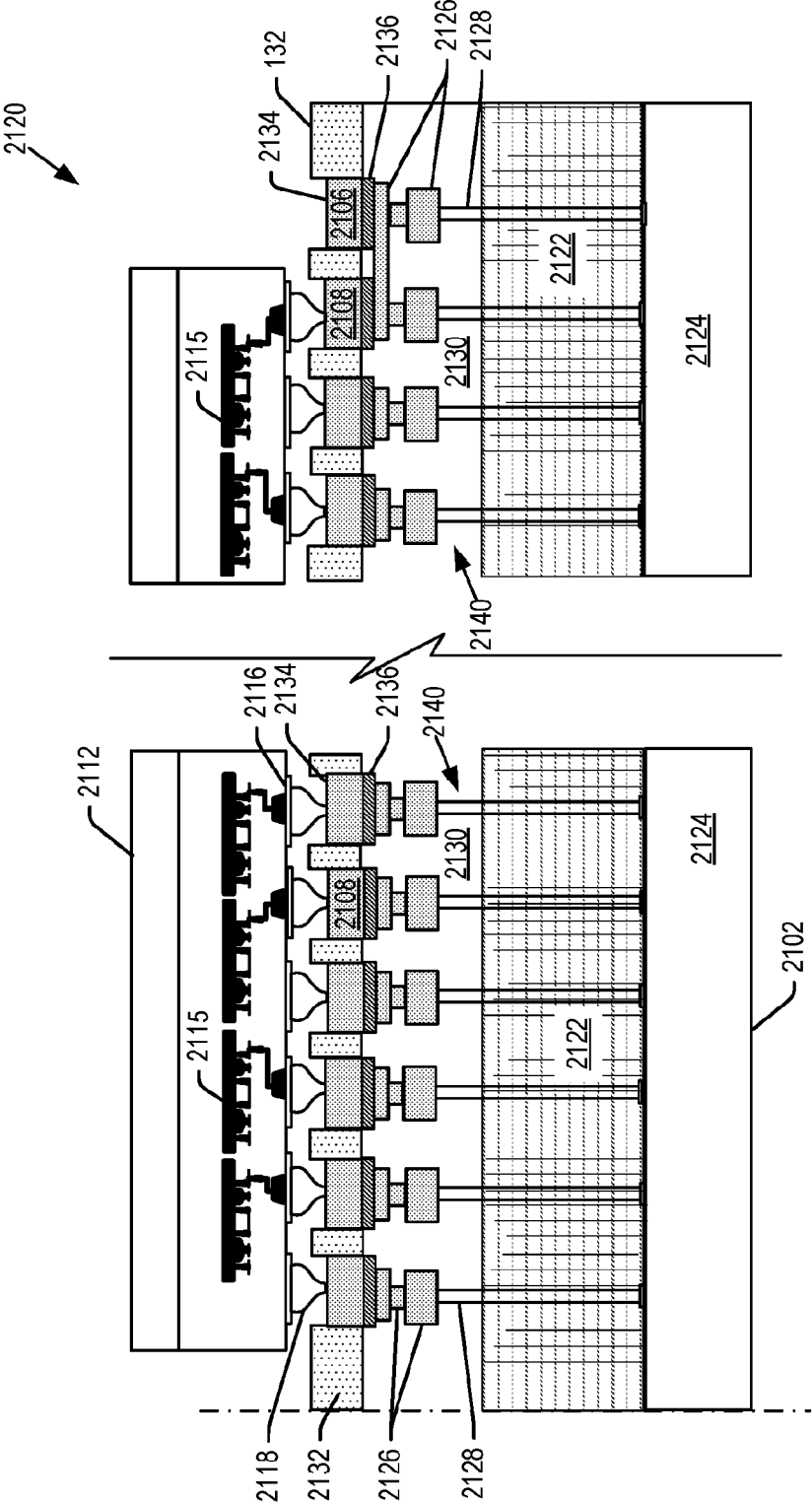


Fig. 58

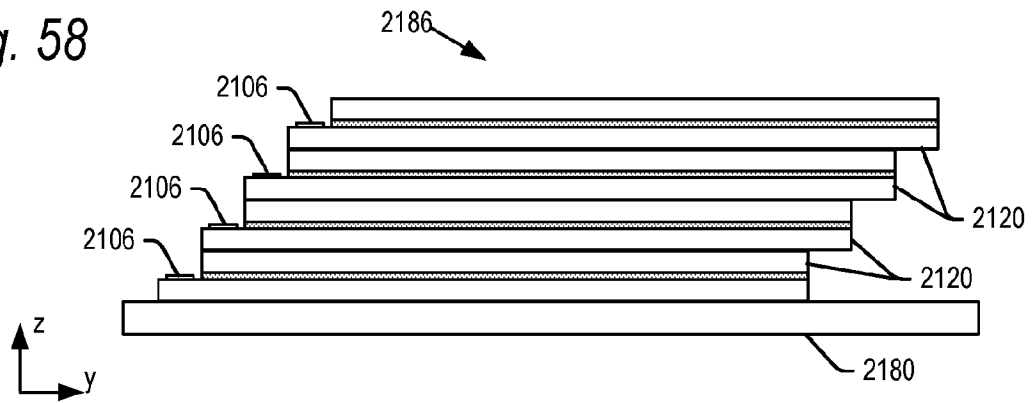


Fig. 59

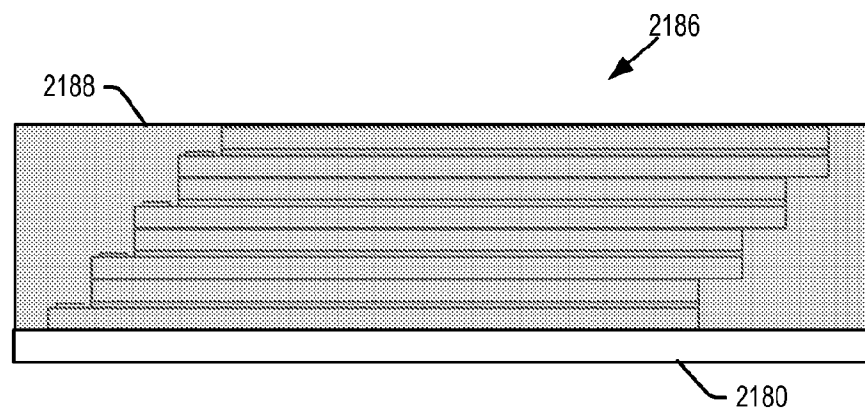


Fig. 60

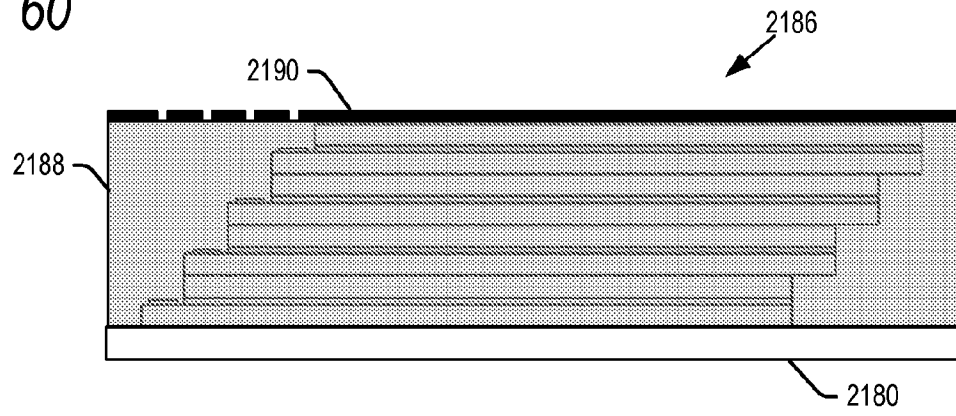


Fig. 61

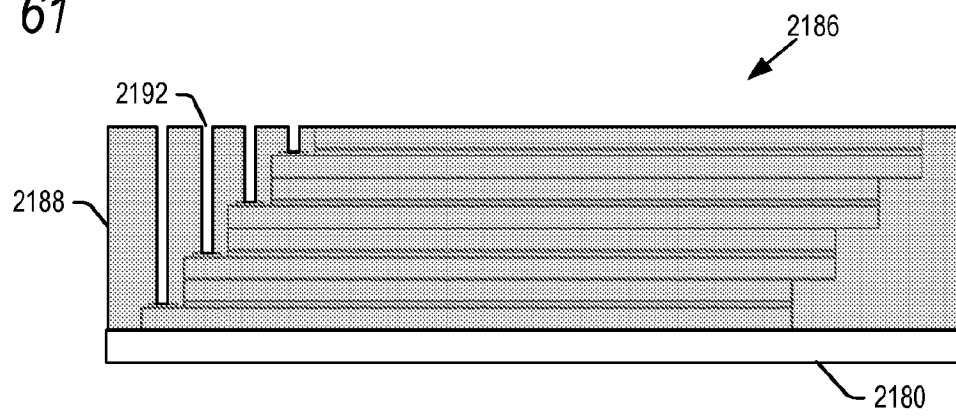


Fig. 62

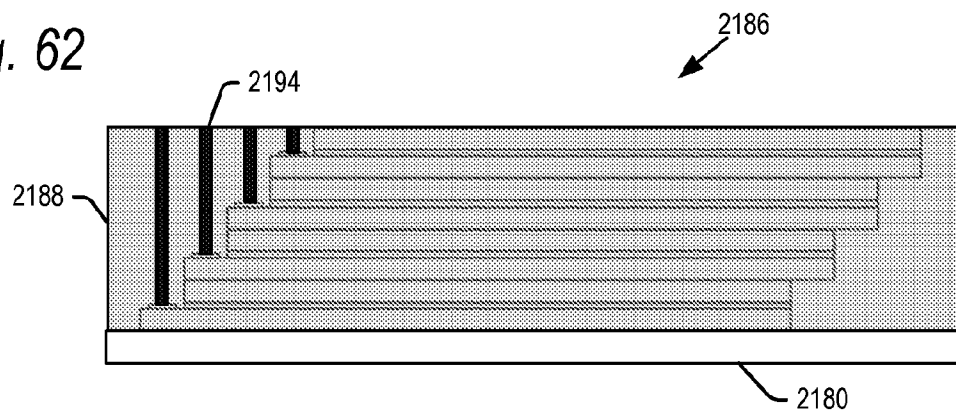


Fig. 63

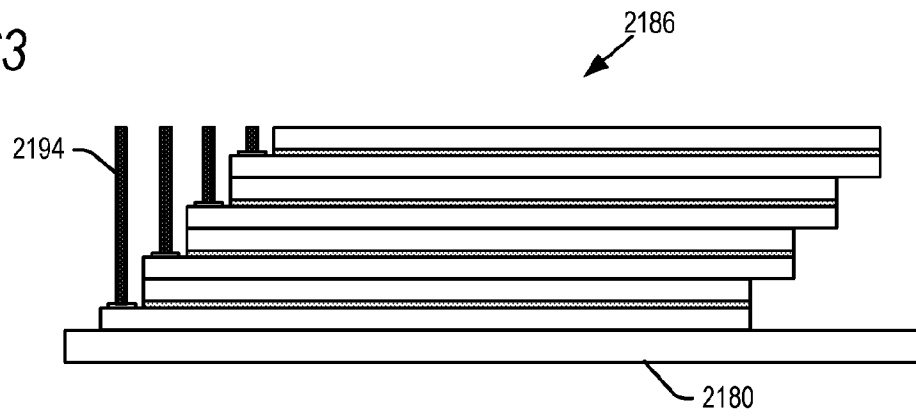


Fig. 64

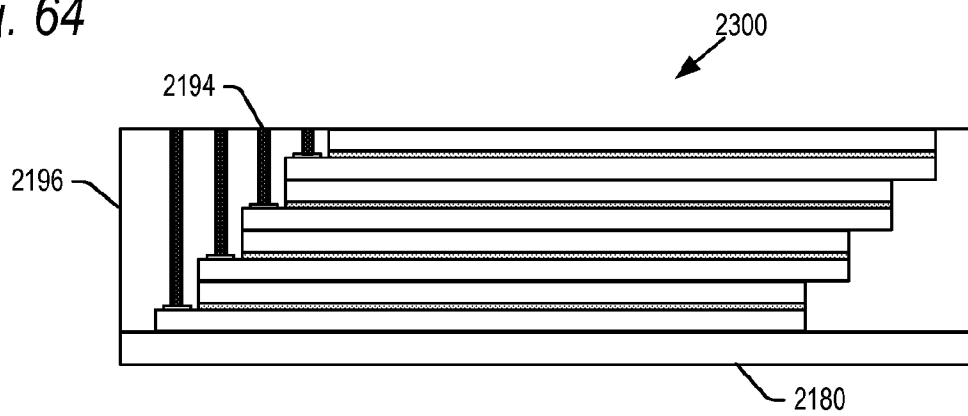


Fig. 65

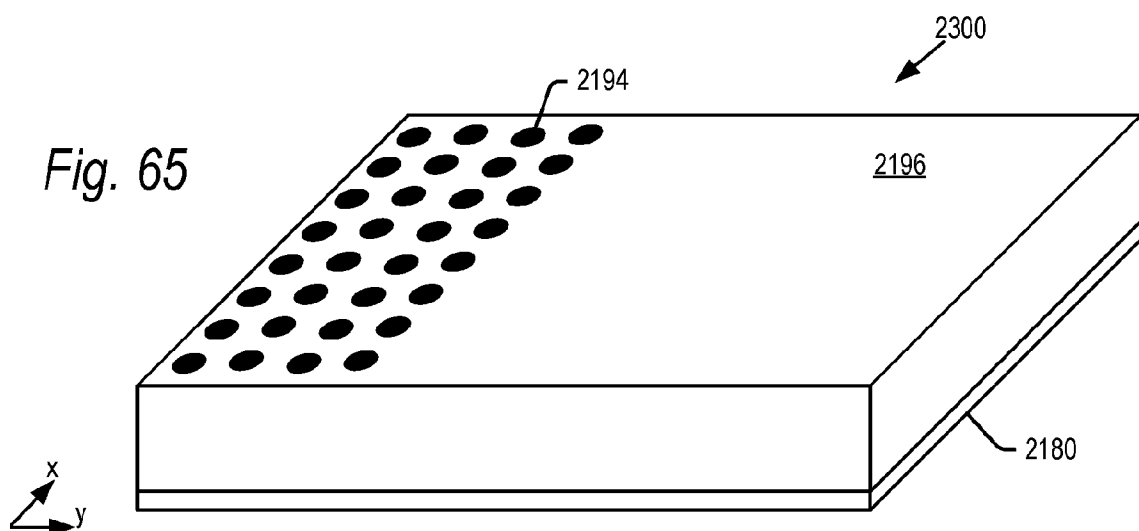


*Fig. 66*

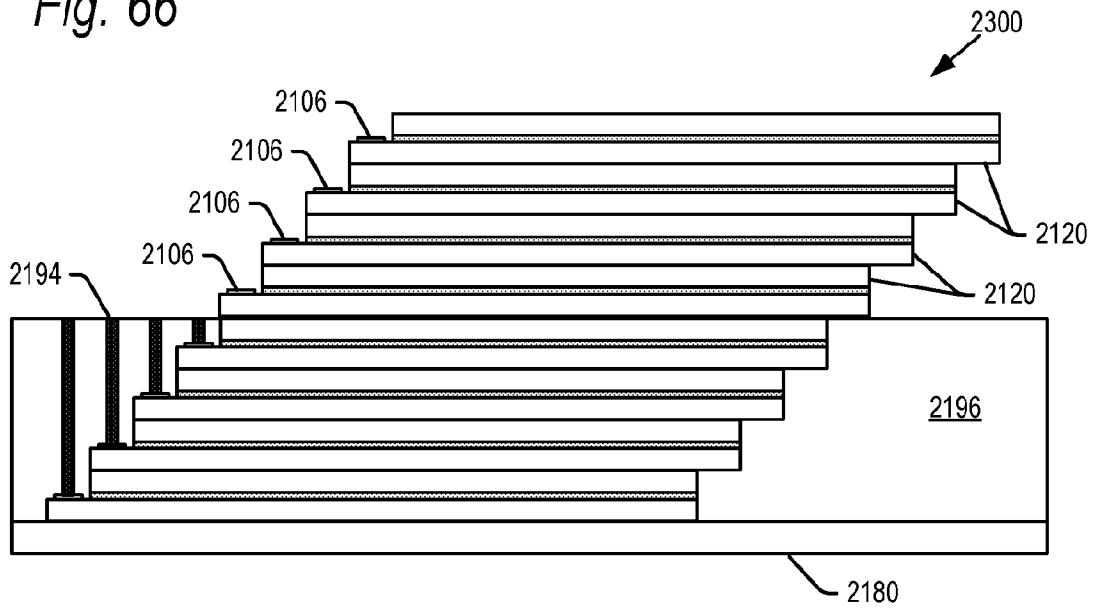


*Fig. 67*

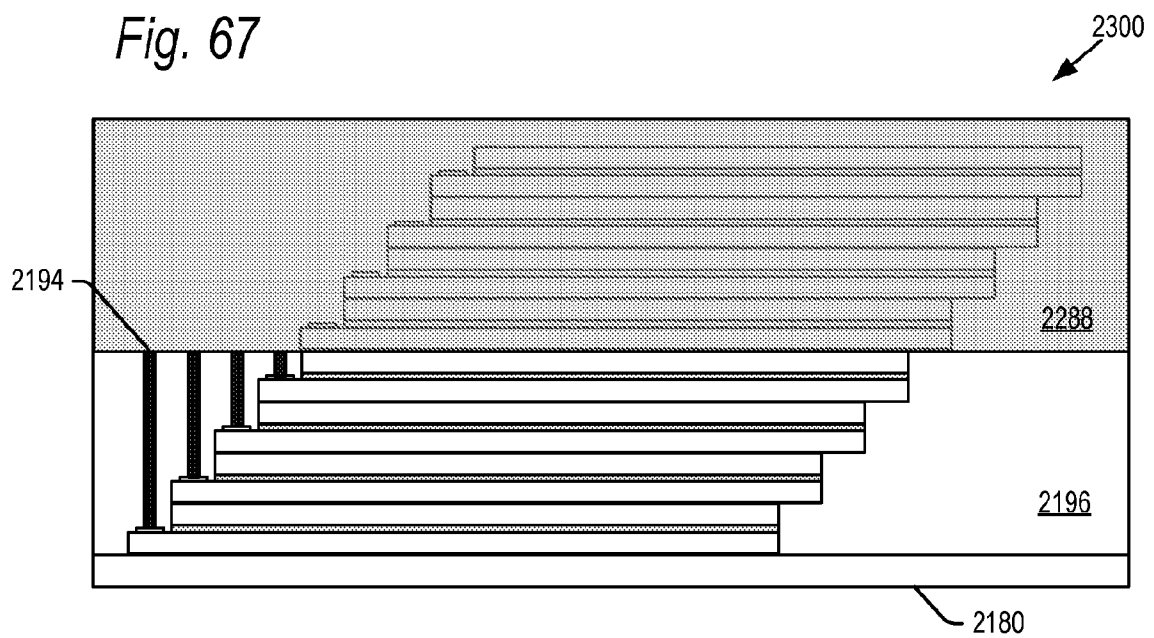


Fig. 68

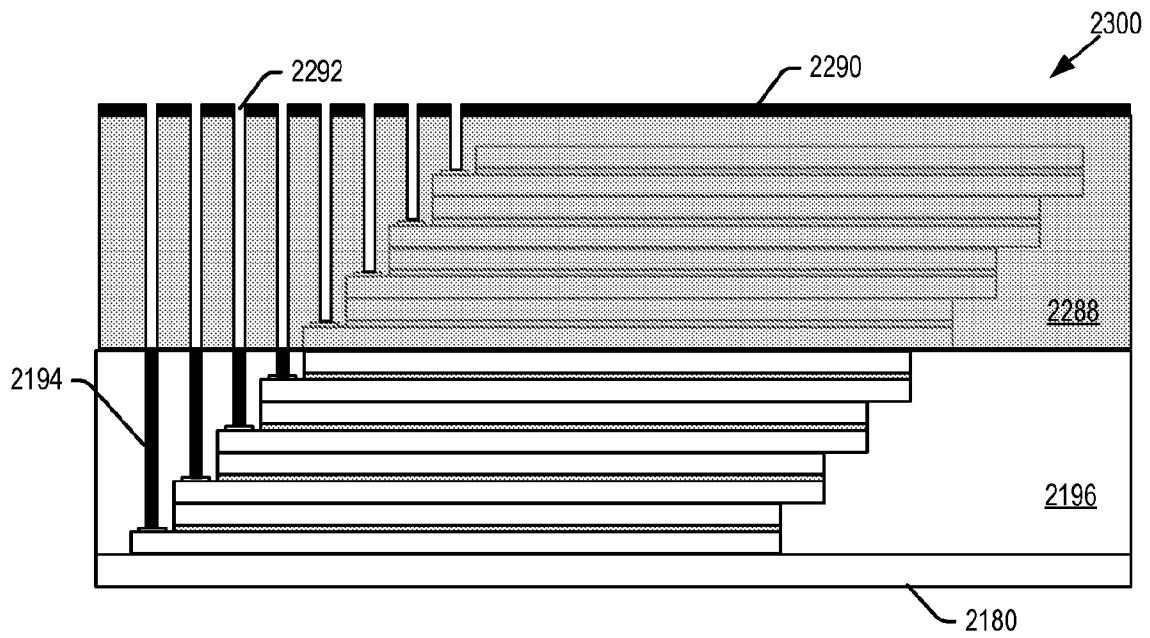


Fig. 69

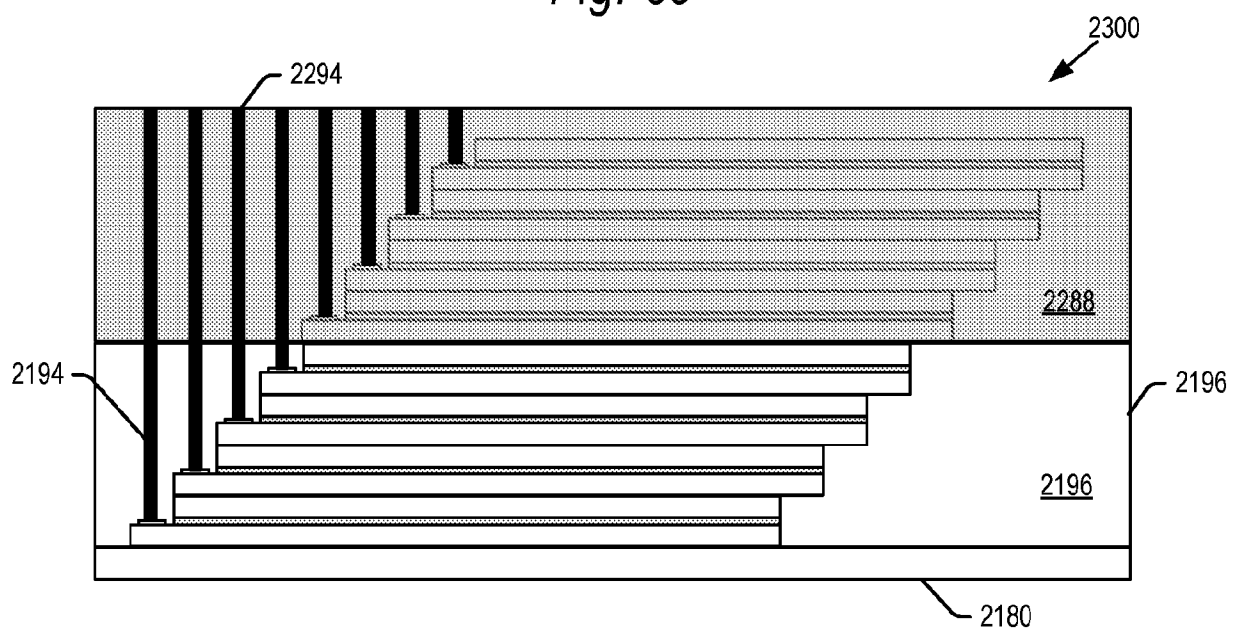


Fig. 70

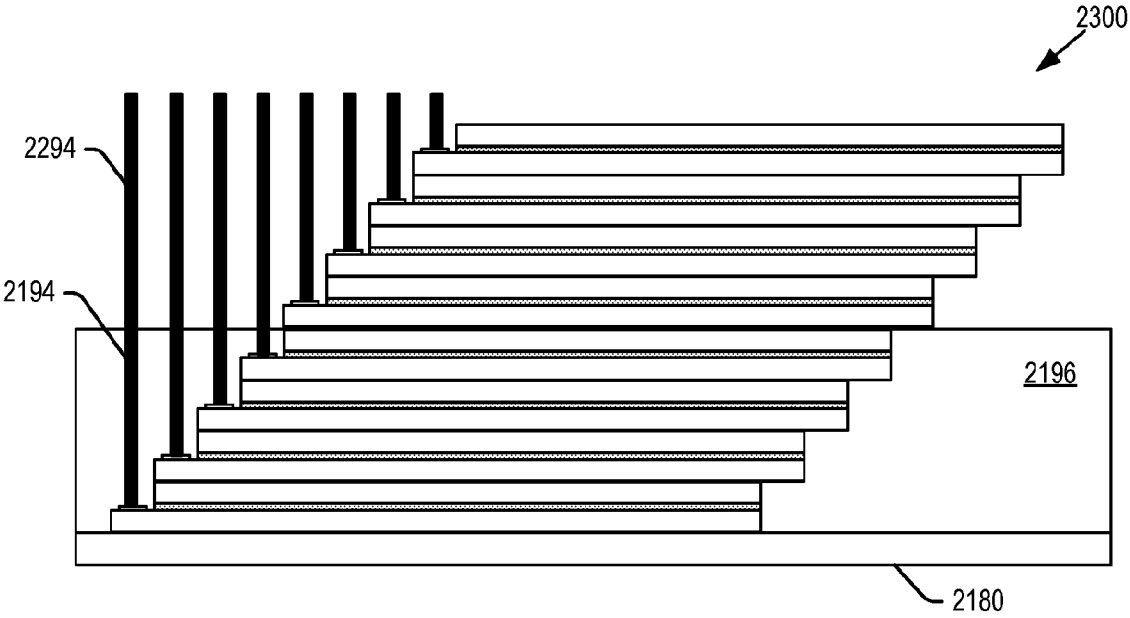


Fig. 71

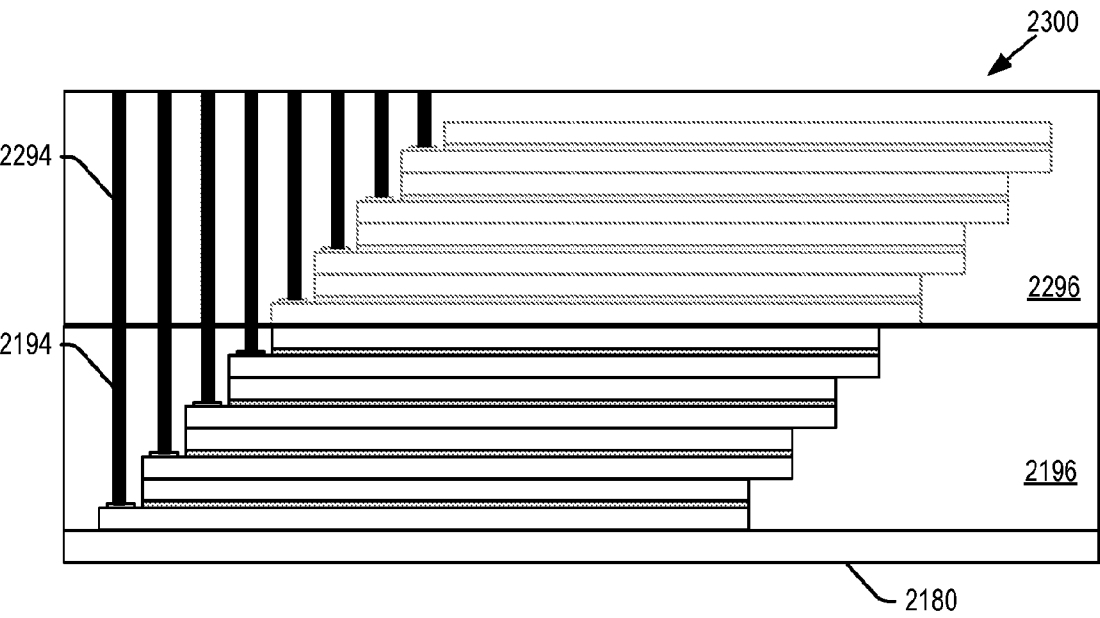


Fig. 72

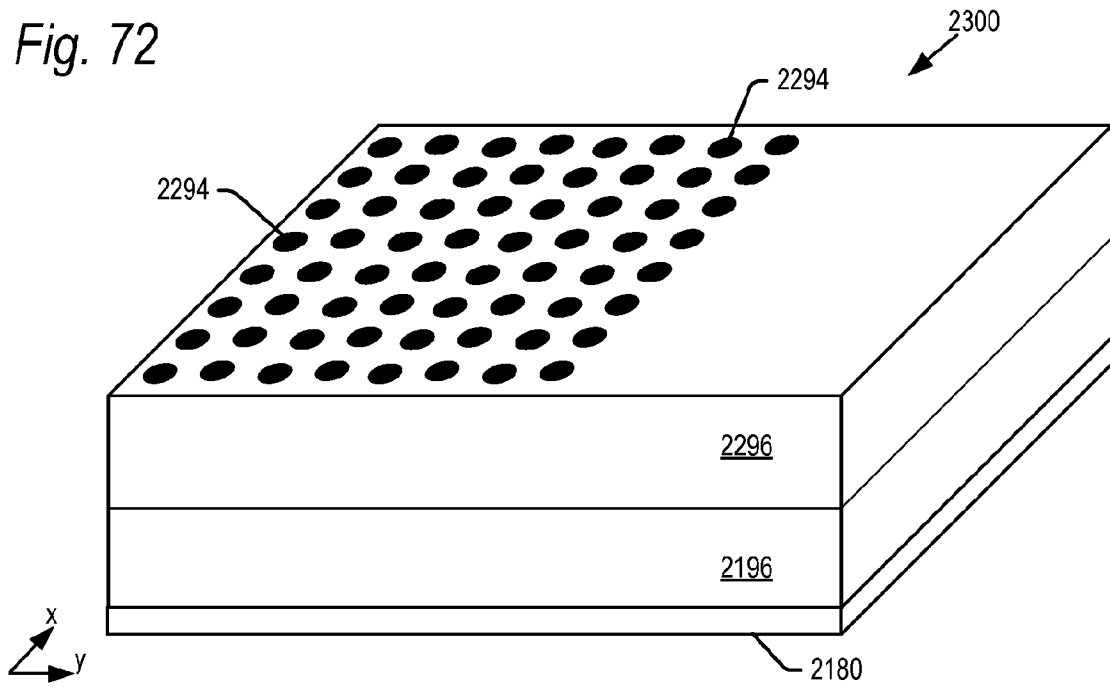


Fig. 73

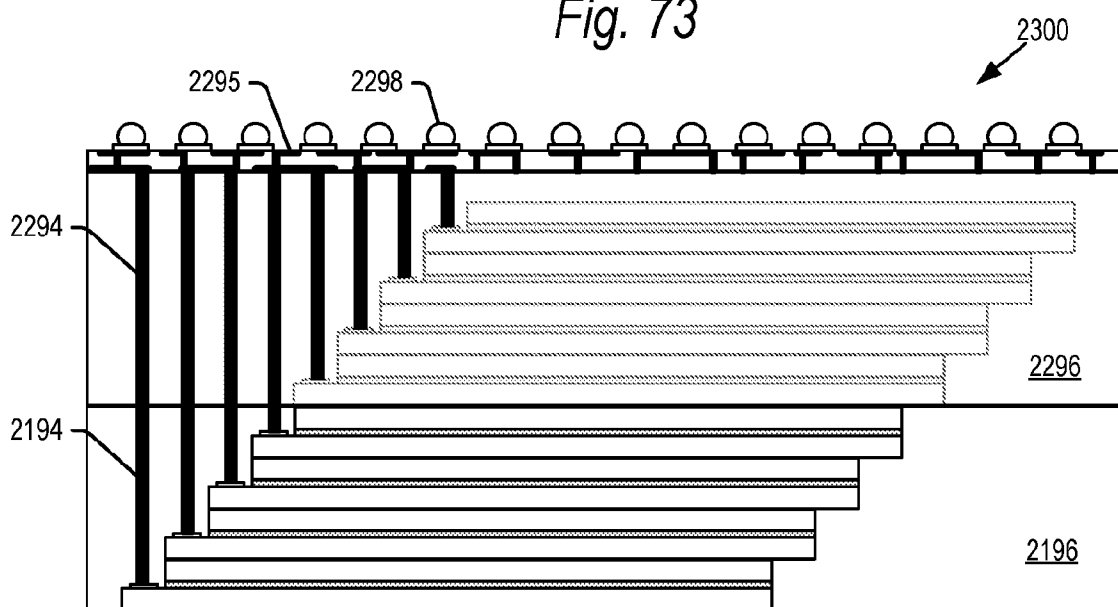
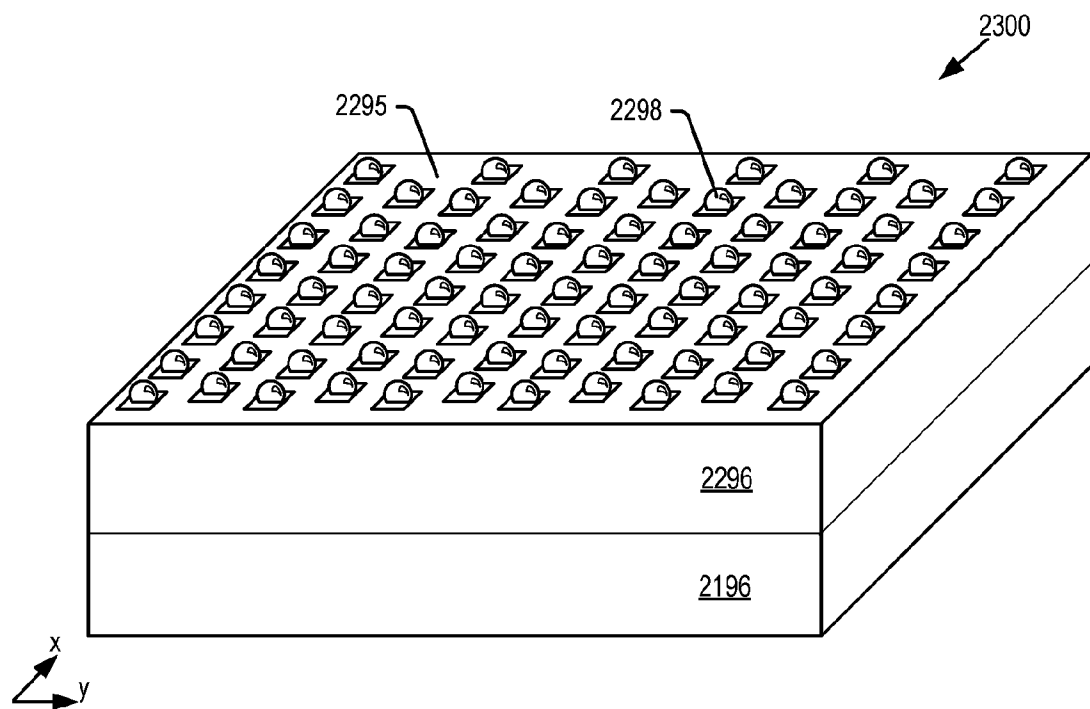


Fig. 74



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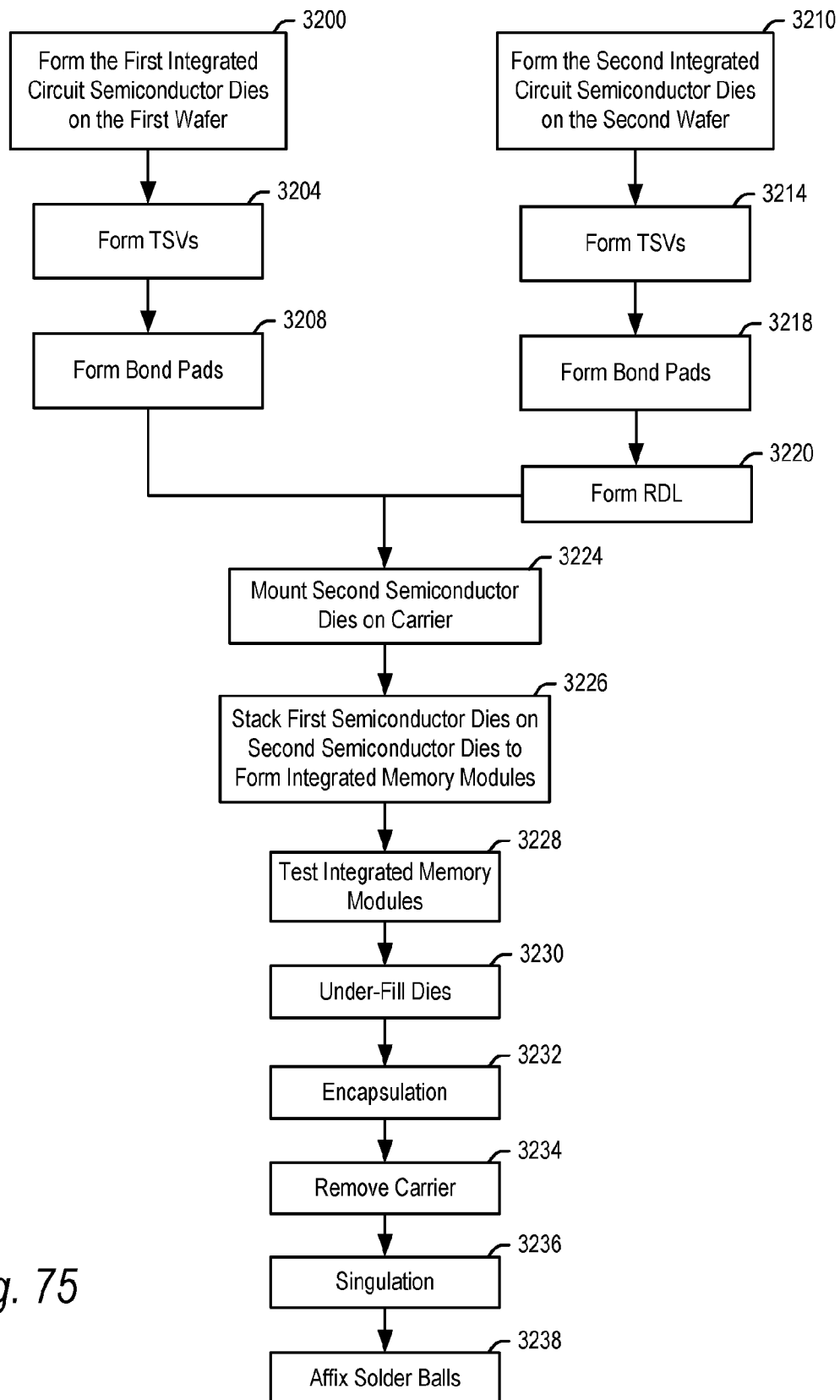
*Fig. 75*

Fig. 76

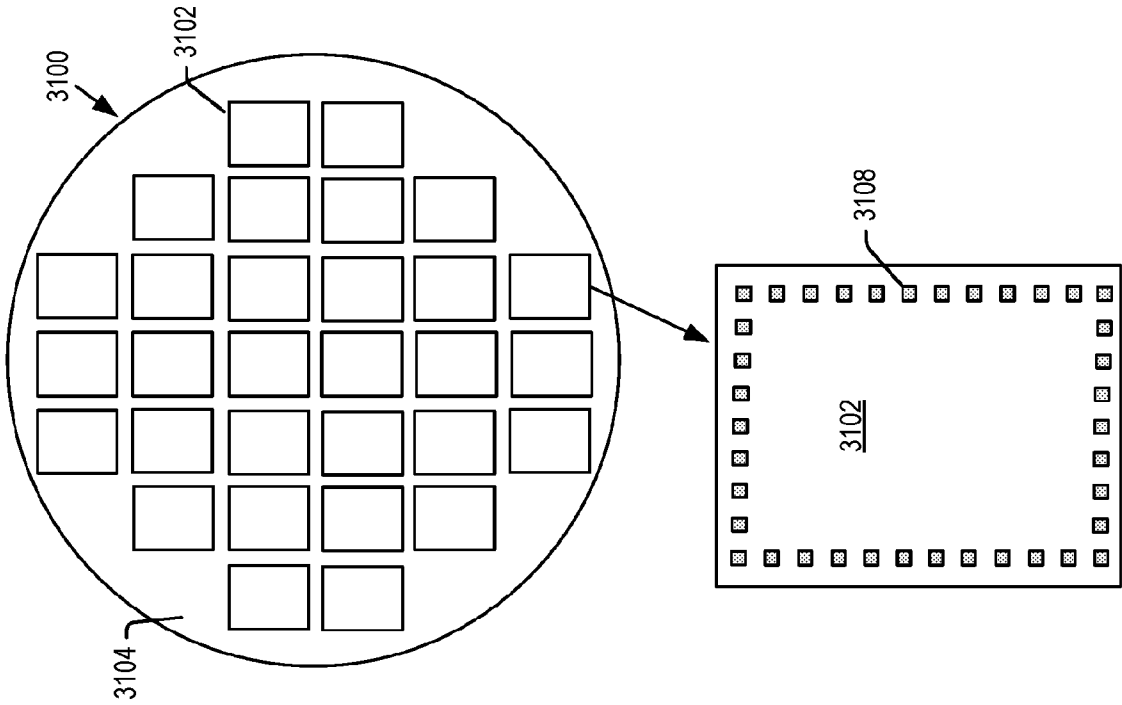


Fig. 77

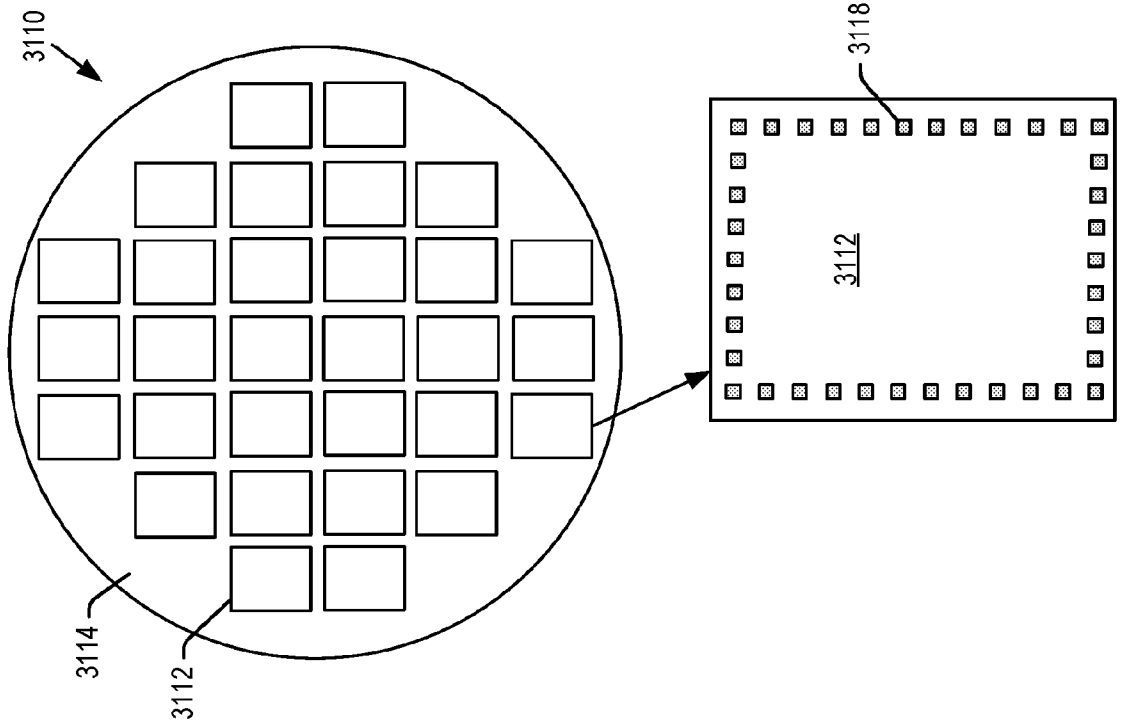


Fig. 78

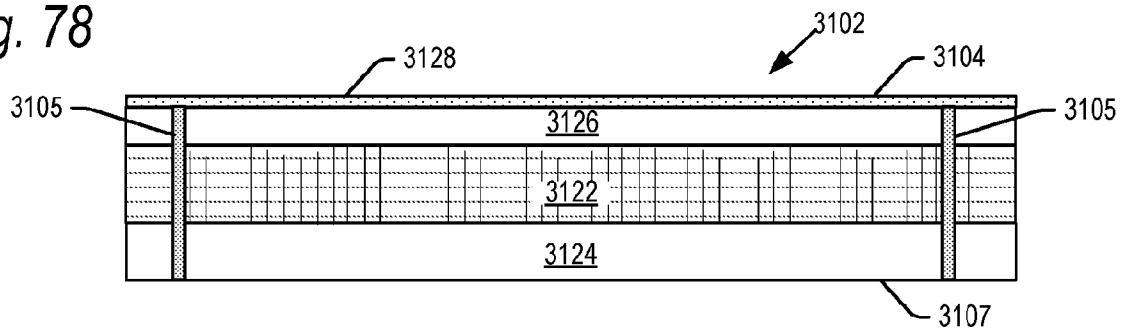


Fig. 79

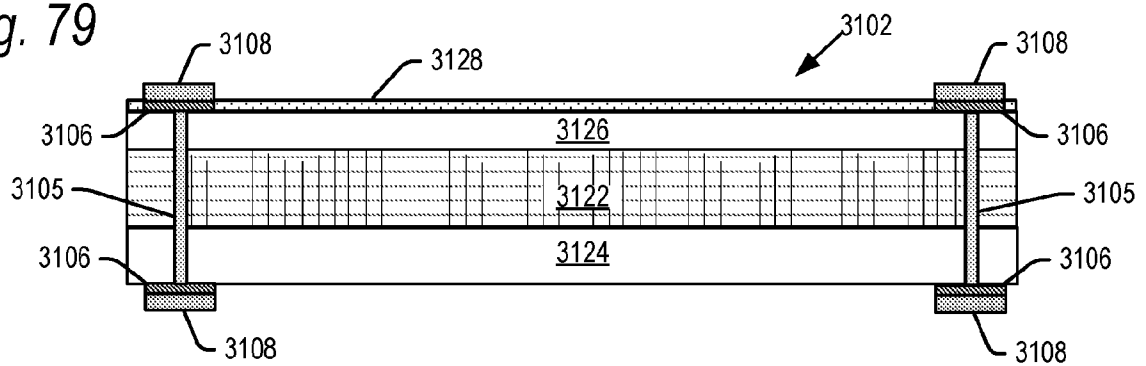


Fig. 80

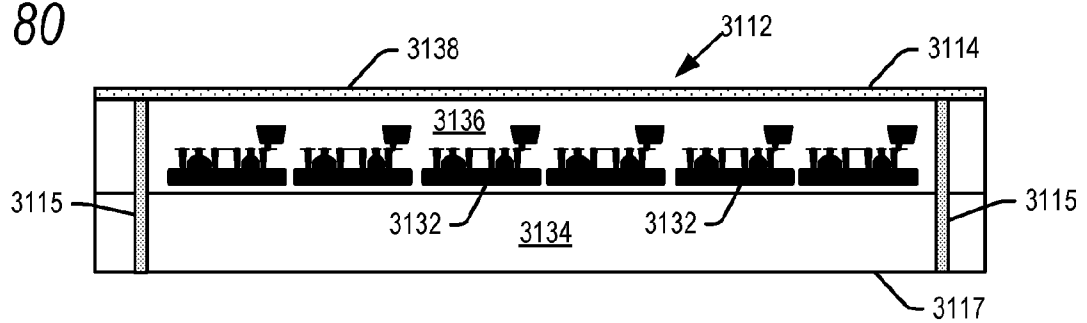


Fig. 81

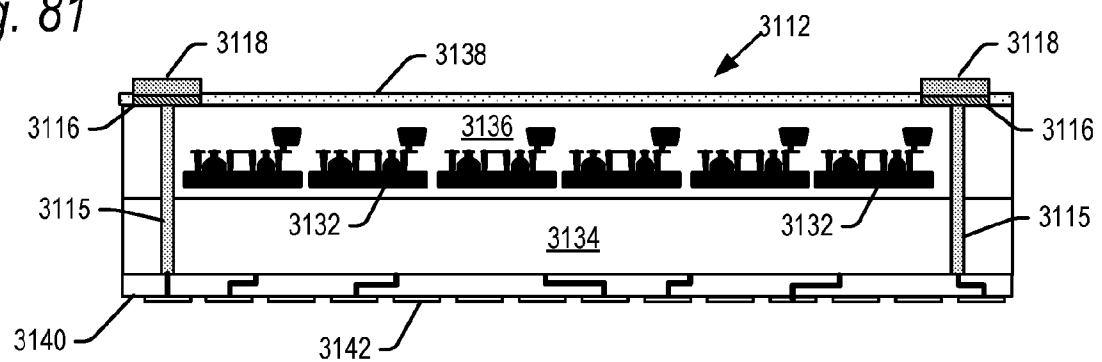


Fig. 82

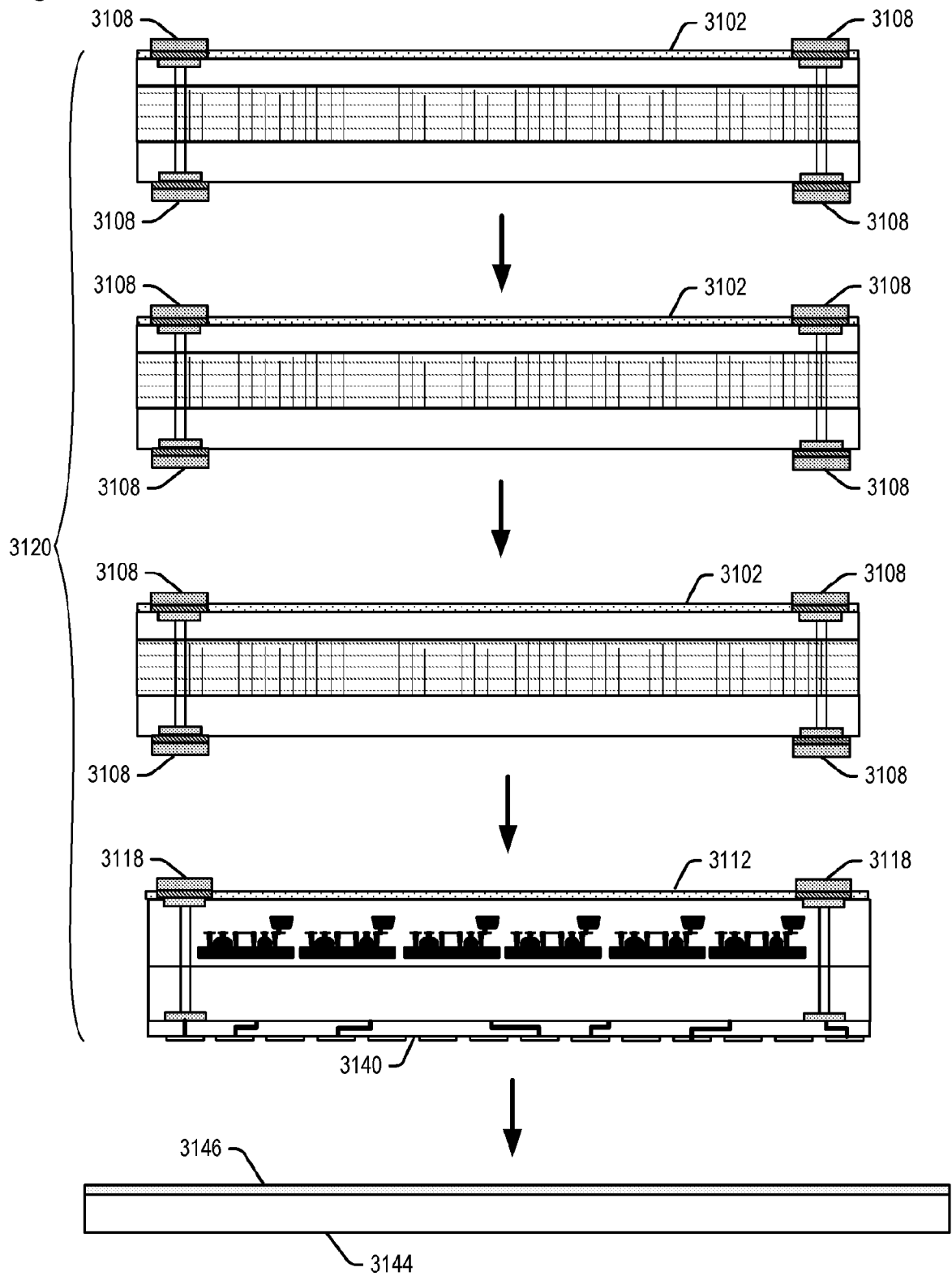


Fig. 83

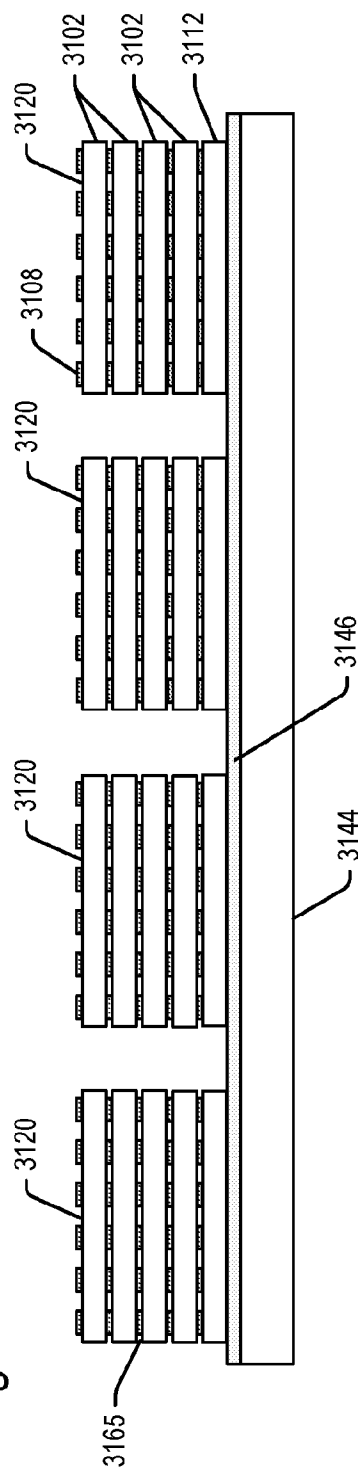


Fig. 84

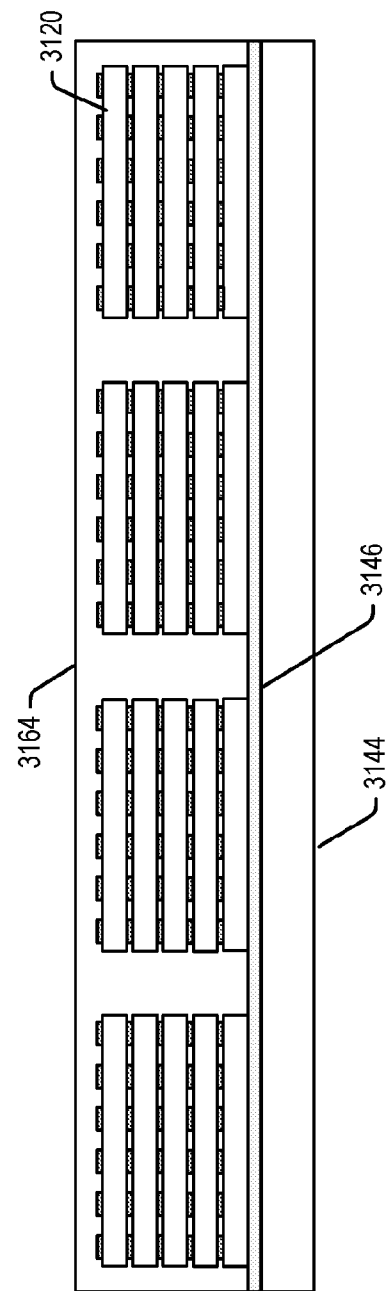


Fig. 85

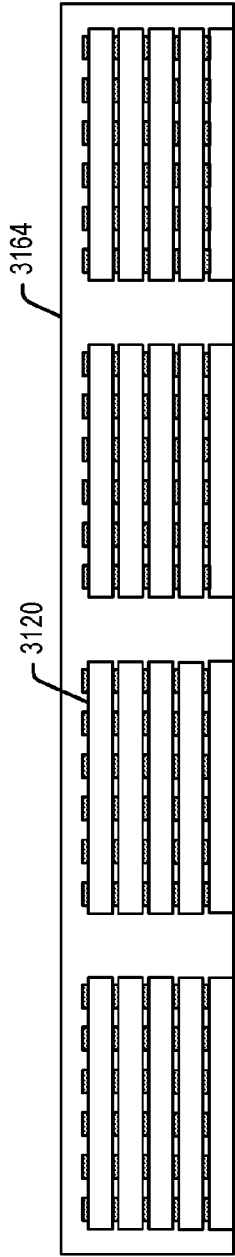
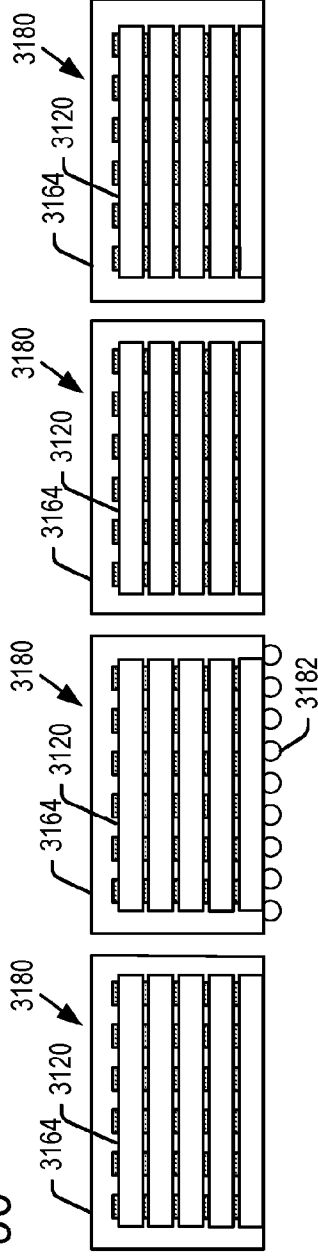


Fig. 86



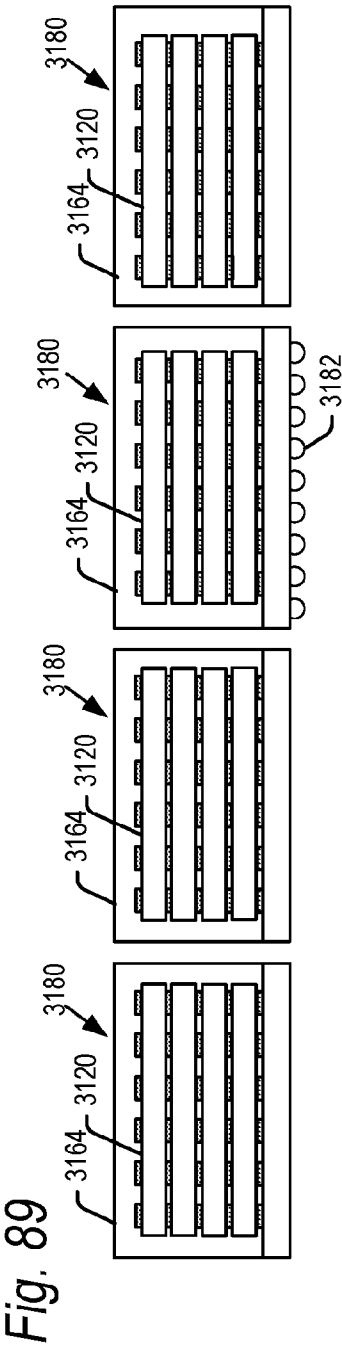
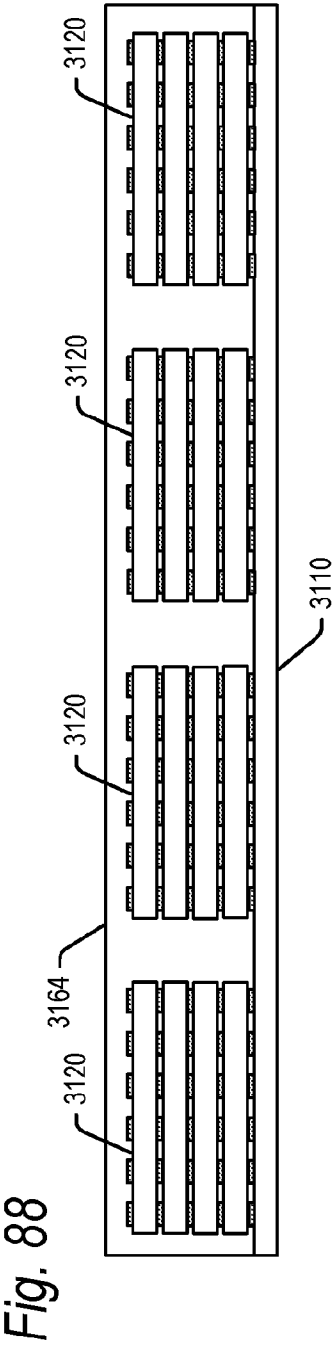
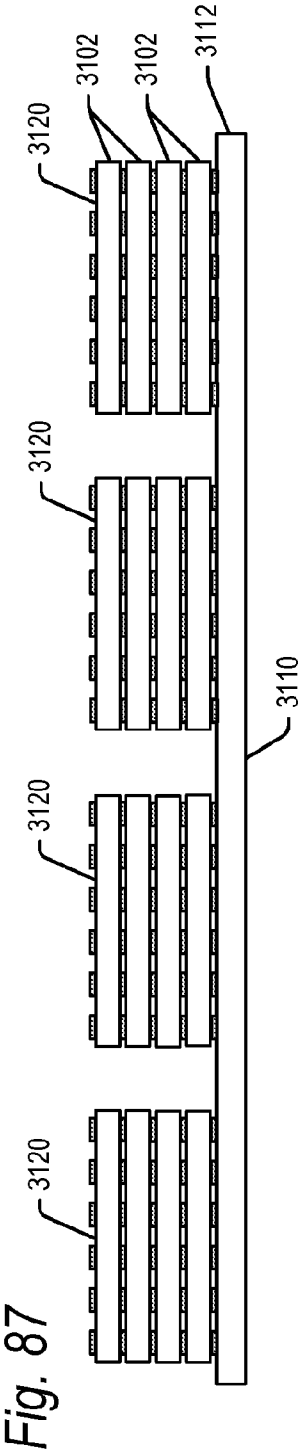


Fig. 90

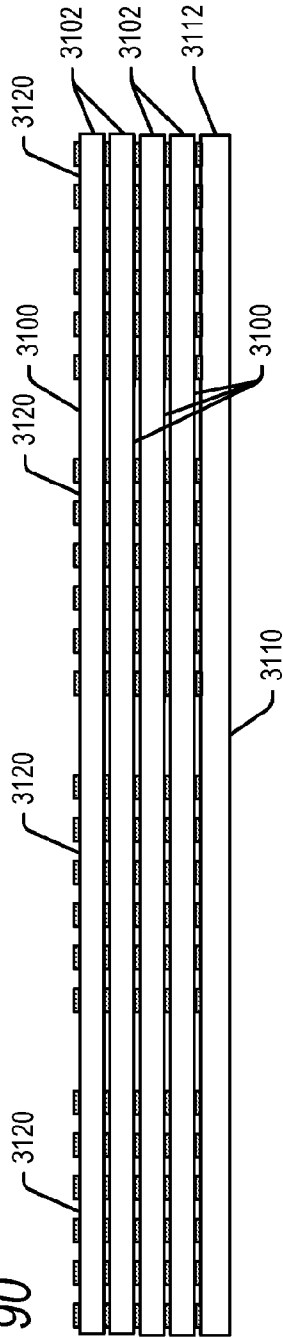


Fig. 91

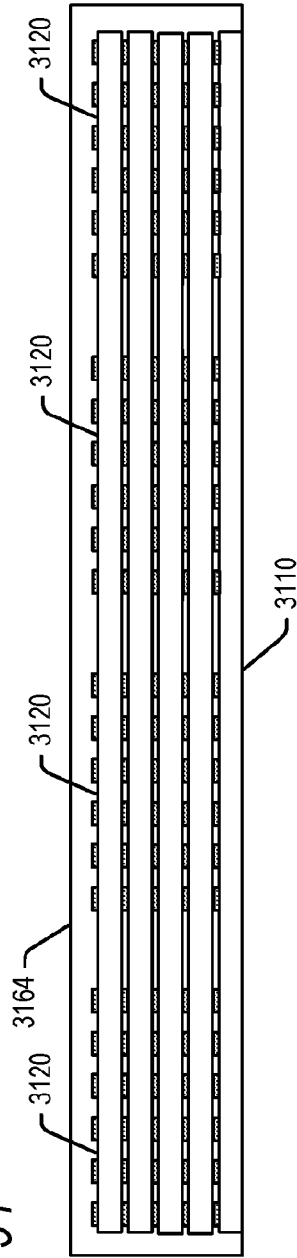


Fig. 92

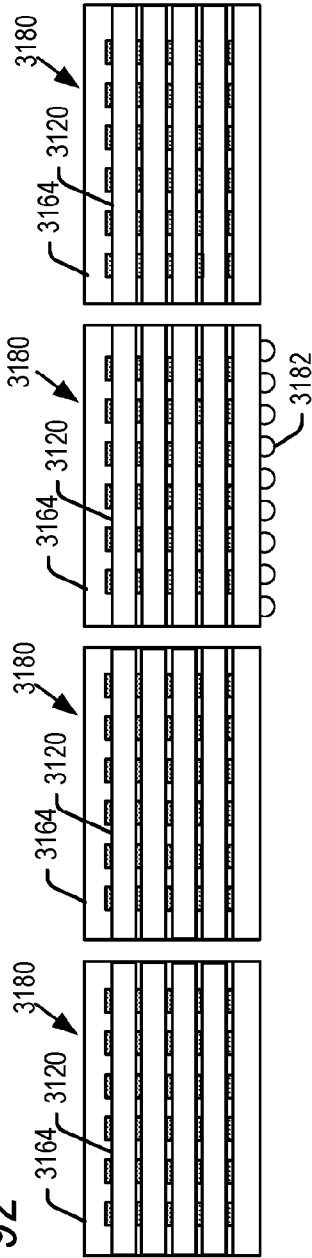


Fig. 93

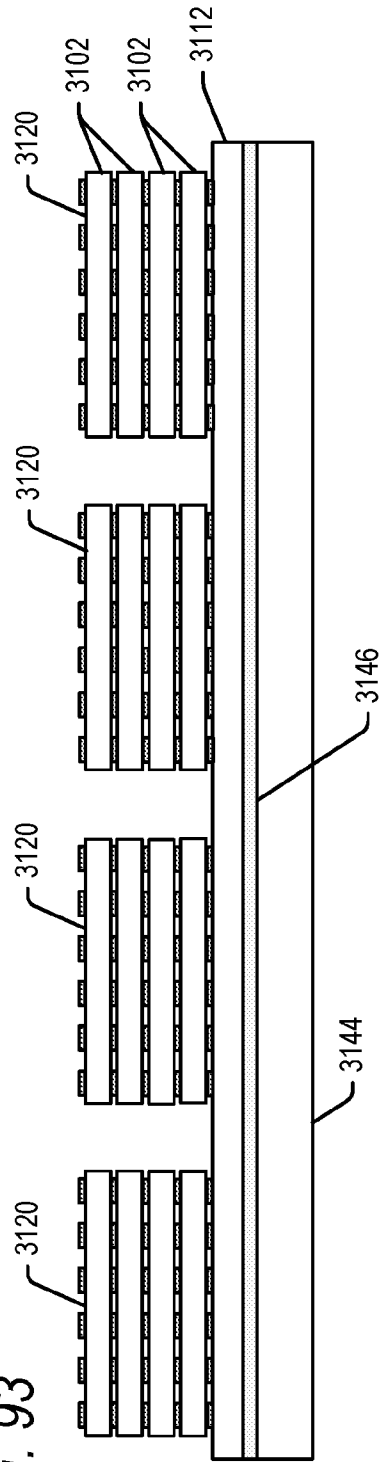


Fig. 94

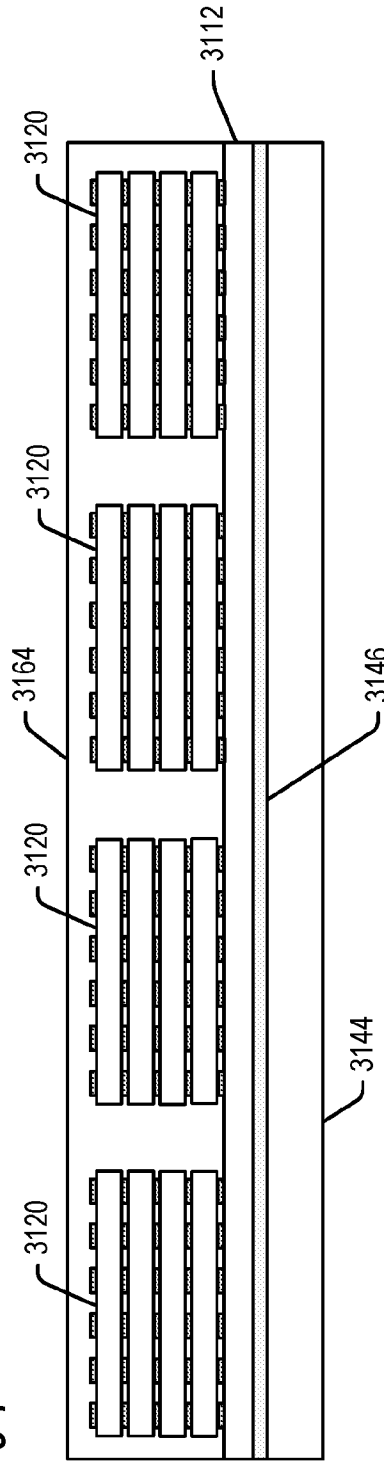
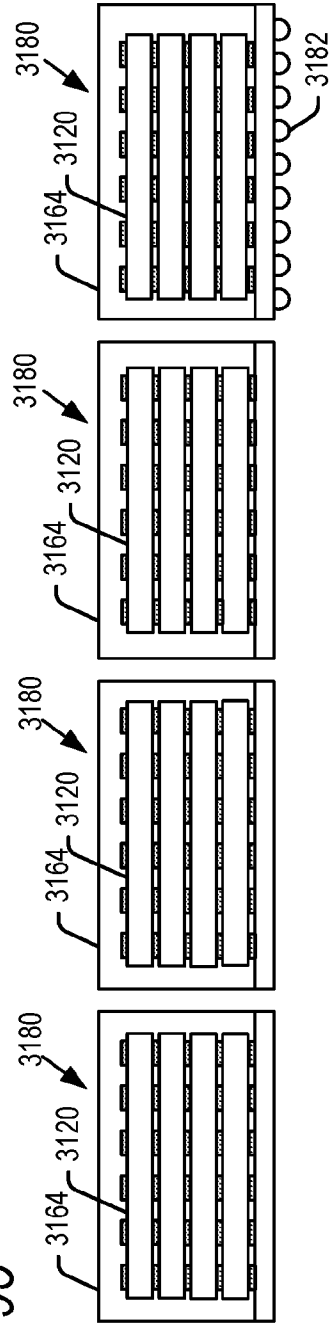


Fig. 95



**A. CLASSIFICATION OF SUBJECT MATTER****H01L 25/065(2006.01)i, H01L 27/11556(2017.01)i, H01L 21/56(2006.01)i, H01L 23/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; G06F 12/00; G06T 11/20; G11C 16/04; H01L 21/304; H01L 23/12; H01L 23/498; H01L 23/544; H01L 27/115; H01L 27/11556; H01L 21/56; H01L 23/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; keywords: memory module, stack, offset, column, step

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                        | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2011-0161583 A1 (SUN-PIL YOUN) 30 June 2011<br>See paragraphs [0032]-[0048] and figures 3A-3D.                         | 13-15                 |
| Y         |                                                                                                                           | 1-6                   |
| A         |                                                                                                                           | 7-12                  |
| Y         | US 2015-0294958 A1 (DEBENDRA MALLIK et al.) 15 October 2015<br>See paragraphs [0028]-[0043] and figures 1-5B.             | 1-6                   |
| A         | US 2013-0277831 A1 (SAMSUNG ELECTRONICS CO., LTD.) 24 October 2013<br>See paragraphs [0056]-[0068] and figure 1A.         | 1-15                  |
| A         | US 2017-0256501 A1 (MICRON TECHNOLOGY, INC.) 07 September 2017<br>See paragraphs [0023]-[0028] and figure 1D.             | 1-15                  |
| A         | US 8947931 B1 (SANDISK TECHNOLOGIES INC.) 03 February 2015<br>See column 2, line 31 - column 11, line 20 and figures 1-3. | 1-15                  |
| A         | KR 10-2015-0085687 A (SAMSUNG ELECTRONICS CO., LTD.) 24 July 2015<br>See paragraphs [0034]-[0107] and figures 1a-7.       | 1-15                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

10 June 2019 (10.06.2019)

Date of mailing of the international search report

**10 June 2019 (10.06.2019)**

Name and mailing address of the ISA/KR

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2019/019136**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                                                                                                  | Publication<br>date                                                                                                                      |
|-------------------------------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| US 2011-0161583 A1                        | 30/06/2011          | CN 102136292 A<br>KR 10-2011-0078189 A                                                                                                                                                      | 27/07/2011<br>07/07/2011                                                                                                                 |
| US 2015-0294958 A1                        | 15/10/2015          | CN 103988300 A<br>DE 112011105992 T5<br>TW 201342549 A<br>TW I508242 B<br>US 10090277 B2<br>US 2014-0217585 A1<br>US 2017-0103970 A1<br>US 9099444 B2<br>US 9530758 B2<br>WO 2013-095546 A1 | 13/08/2014<br>18/09/2014<br>16/10/2013<br>11/11/2015<br>02/10/2018<br>07/08/2014<br>13/04/2017<br>04/08/2015<br>27/12/2016<br>27/06/2013 |
| US 2013-0277831 A1                        | 24/10/2013          | KR 10-2013-0118175 A                                                                                                                                                                        | 29/10/2013                                                                                                                               |
| US 2017-0256501 A1                        | 07/09/2017          | US 9754895 B1                                                                                                                                                                               | 05/09/2017                                                                                                                               |
| US 8947931 B1                             | 03/02/2015          | CN 106463499 A<br>JP 2017-523587 A<br>JP 6346303 B2<br>KR 10-1908206 B1<br>KR 10-2017-0018301 A<br>TW 201602900 A<br>WO 2015-191243 A1                                                      | 22/02/2017<br>17/08/2017<br>20/06/2018<br>15/10/2018<br>17/02/2017<br>16/01/2016<br>17/12/2015                                           |
| KR 10-2015-0085687 A                      | 24/07/2015          | CN 104795386 A<br>US 10157883 B2<br>US 2015-0200187 A1<br>US 2017-0125378 A1<br>US 9589930 B2                                                                                               | 22/07/2015<br>18/12/2018<br>16/07/2015<br>04/05/2017<br>07/03/2017                                                                       |