(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 July 2013 (11.07.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/102879 Al

(51) International Patent Classification:
H02M 3/158 (2006.01)

(21) International Application Number:
PCT/IB20 13/050087

(22) International Filing Date:
4 January 2013 (04.01 .2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/583,645 6 January 2012 (06.01 .2012) US

(71) Applicant: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; High Tech Campus 5, NL-5656 AE Eindhoven (NL).

(72) Inventors: **CHEN, Zhiquan;** c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL). **XU, JianLin;** c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL). **WANG, Hongbo;** c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL). **ZHOU, Zhenhua;** c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL).

(74) Agents: **VAN EEUWIJK, Alexander, H., W.** et al; High Tech Campus 44, NL-5600 AE Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available):* AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available):* ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17 :

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.1 7(H))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.1 7(in))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: POWER CONVERTER WITH SEPARATE BUCK AND BOOST CONVERSION CIRCUITS

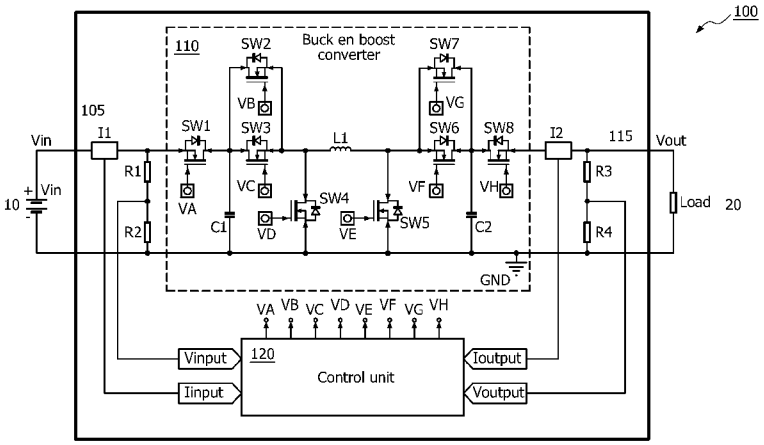

FIG. 1

(57) Abstract: An apparatus (100) includes a buck and boost conversion circuit (110), and a control unit (120, 200) for controlling operations of the buck and boost converter. The buck and boost converter includes a buck conversion circuit having a first set of switches (SW3, SW4), and a boost conversion circuit having a second set of switches (SW5, SW6). The buck conversion circuit and the boost conversion circuit may be controlled independently from each other. The control unit is configured to control delivery of power from the power converter to a load (20) via the buck conversion circuit in a buck conversion mode by controlling switching operations of the first set of switches, and to control the delivery of the power from the power converter to the load via the boost conversion circuit in a boost conversion mode by controlling switching operations of the second set of switches.

WO 2013/102879 A1

POwERooNVB?TERwrTH SEPARATEBUCKANDBOOST CONVERSON CIRCUITS

Technical Held

[0001] The present invention isdirected generally to a power converter. More particularly, various inventive methods and apparatus disclosed herein relate to a buck and boost converter with separate buck and boost conversion circuits.

Backcround

[0002] In general, power converters typically fall into one of three categories: buck converters; boost converters, and buck-boost converters.

[0003] A buck converter isastep-down DCto DCconverter, i.e., it converts a higher DC input voltage to a lower DCoutput voltage, and in general it is a switching mode power supply. In general, a buck converter may be highly efficient, but it operates over a narrow range of input voltage, when the input voltage received from a voltage source is greater than the output voltage to be supplied to a load.

[0004] Aboost converter isastep-up DCto DCconverter, i.e., it converts a lower DCinput voltage to a higher DCoutput voltage, and in general it is also a switching mode power supply. , In general a boost converter may have a simple circuit structure, and may provide a small ripple current at its input. However, like the buck converter it operates over a narrow range of input voltage, when the input voltage received from a voltage source is greater than the output voltage to be supplied to a load.

[0005] A buck-boost converter is atype of DCto- DC converter that has an output voltage magnitude that can be either greater than, or less than, the input voltage magnitude. In other words, a buck-boost converter includes both buck converter functionality and boost converter functionality.

[0006] In aconventional buck-boost converter, the buck functionality and boost functionality are not separate or independent from each other, but they share some important components such as the switching devices (e.g., MOSFETs, diodes, etc.), and therefore cannot

be separately controlled or optimized. The conventional buck-boost converter exhibits some limitations in terms of its efficiency, a limited range of input and output voltages, and the number of applications to which it can be applied.

[0007] Thus, it would be desirable to provide a power converter which is capable in operating in a buck conversion mode and a boost conversion mode. It would also be desirable to provide such a power converter which is capable of operating with greater efficiency over a wide range of input and output voltages in many different applications.

Summary

[0008] The present disclosure is directed to inventive methods and apparatus for a power converter. For example, in some embodiments a power converter is provided with a buck converter circuit and boost converter circuit which can be separately and independently controlled.

[0009] Generally, in one aspect, the invention relatesto an apparatus including: apower converter configured to convert an input voltage to an output voltage and to supply the output voltage to a load, and acontrol unit configured to control an operation of the power converter. The power converter includes: a buck conversion circuit including a first set of switches, and a boost conversion circuit including a second set of switches, wherein the second set of switches are separate from and capable of being controlled independently from the first set of switches. The control unit is configured to control delivery of power from the power converter to the load via the buck conversion circuit in a buck conversion mode by controlling switching operations of the first set of switches, and to control the delivery of the power from the power converter to the load viathe boost conversion circuit in a boost conversion mode by controlling switching operations of the second set of switches

[0010] In one or more embodiments, the control unit is configured to receive a sample of the input voltage, a sample of the output voltage, a sample of an input current supplied to the power converter, and asample of an output current supplied by the power converter, and is configured to control the delivery of the power to the load based on the sample of the input voltage, the sample of the output voltage, the sample of the input current and the sample of

the output current.

[0011] Accordingto one optional feature of these embodiments, the control unit includesa plurality of analog-to-digital converter (ADCs) configured to convert the sample of the input voltage, the sample of the output voltage, the sample of the input current and the sample of the output current to digital values. Accordingto another optional feature of these embodiments, the control unit includes circuitry configured to compare the input voltage and the output voltage to each other, wherein the control unit selects the power converter operating mode based on a result of the comparison. According to yet another optional feature of these embodiments, the control unit is configured to control the delivery of power from the power converter to the load viathe buck conversion circuit by switching at least one of the switches of the first set of switches at a switching frequency and aduty cycle, and by adjusting at least one of the switching frequency and the duty cycle in response to adifference between the sample of the input voltage and the sample of the output voltage. According to afurther optional feature of these embodiments, the control unit is configured to control the delivery of power from the power converter to the load viathe boost conversion circuit by switching at least one of the switches of the second set of switches at a switching frequency and aduty cycle, and by adjusting at least one of the switching frequency and the duty cycle in response to adifference between the sample of the input voltage and the sample of the output voltage.

[0012] In one or more embodiments, the control unit is configured: to control delivery of power from the power converter to the load when the input voltage is greater than a sum of the output voltage and a first fixed voltage, wherein the first fixed voltage is greater than or equal to zero volts, by controlling the switching operations of the first set of switches; and to control the delivery of the power from the power converter to the load when the input voltage is less than the output voltage by controlling the switching operations of the second set of switches.

[0013] Accordingto one optional feature of these embodiments, the first fixed voltage is lessthan 1 volt. Accordingto another optional feature of these embodiments, the control unit isfurther configured to control the power converter to operate in adirect conversion mode when the output voltage is greater than adifference between the input voltage and the first

fixed voltage, and less than a sum of the input voltage and the second fixed voltage.

[0014] Generally, in another aspect, the invention relates to a method including: sampling an input voltage, an output voltage, an input current, and an output current of a power converter that includes a buck conversion circuit including a first set of switches, and aboost conversion circuit including a second set of switches, wherein the second set of switches are separate from and capable of being controlled independently from the first set of switches; when the input voltage is greater than a sum of the output voltage and a first fixed voltage that is greater than or equal to zero volts, controlling delivery of power from the power converter to a load by controlling switching operations of the first set of switches; and when the input voltage is less than the output voltage, controlling the delivery of the power from the power converter to the load by controlling switching operations of the second set of switches.

[0015] In one or more embodiments, controlling delivery of power from the power converter to a load by controlling the switching operations of the first set of switches of the buck conversion circuit comprises supplying one or more control signals to one or more switches of the first set of switches and pulse width modulating the one or more control signals

[0016] According to one optional feature of this embodiment, pulse width modulating the one or more control signals comprises adjusting one of afrequency and aduty cycle of each pulse width modulated control signal in response to adifference between the input voltage and the output voltage.

[0017] In one or more other embodiments, controlling delivery of power from the power converter to a load by controlling the switching operations of the second set of switches of the boost conversion circuit comprises supplying one or more control signals to one or more switches of the second set of switches and pulse width modulating the one or more control signals. According to one optional feature of this embodiment, pulse width modulating the one or more control signals comprises adjusting one of afrequency and aduty cycle of each pulse width modulated control signal in response to adifference between the input voltage and the output voltage.

[0018] In one or more embodiments, the first fixed voltage is less than 1 volt.

[0019] Generally, in yet another aspect, the invention relatesto an apparatus including a buck and boost power converter capable of operating in a buck conversion mode and in a boost conversion mode, and acontrol unit. The buck and boost power converter comprises: an input node; an output node; afirst switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the first switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal is connected to the input node; afirst capacitor connected between the second terminal of the first switch and ground; a second switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the second switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminal of the first switch and to the first capacitor; athird switch having afirst terminal, asecond terminal, and a control terminal for selectively opening and closing the third switch to control acurrent path between the first terminal and the second terminal, wherein the third switch isconnected in parallel with the second switch; afourth switch having afirst terminal, asecond terminal, and a control terminal for selectively opening and closing the fourth switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminals of the second and third switches, and the second terminal is connected to ground; an inductor having afirst terminal and asecond terminal, wherein the first terminal is connected to the second terminals of the second, third and fourth switches; afifth switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the fifth switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminal of the inductor, and the second terminal isconnected to ground; asixth switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the sixth switch to control a current path between the first terminal and the second terminal, wherein the first terminal is connected to the second terminal of the inductor and the first terminal of the fifth switch; a seventh switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the seventh switch to control acurrent path between the first terminal and

the second terminal, wherein the sixth switch is connected in parallel with the fifth switch; a second capacitor connected between the second terminals of the sixth and seventh switches and ground; and an eighth switch having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the sixth switch to control a current path between the first terminal and the second terminal, wherein the first terminal is connected to the second capacitor and the second terminals of the sixth and seventh switches, and wherein the second terminal is connected to the output node. The control unit is configured to provide first through eighth control signalsto corresponding ones of the control terminals of the first through eighth switching devices so as to control switching of the first through eighth switching devices to cause the buck and boost power converter to operate selectively in one of a boost conversion mode and a buck conversion mode.

[0020] In one or more embodiments, when the control unit controls the buck and boost power converter to operate in the buck conversion mode, the control unit provides: the first control signal to turn on the first switch; the second control signal to turn off the second switch; the third control signal as afirst pulse width modulated signal having afirst frequency and a first duty cycle to alternately turn on and turn off the third switch; the fourth control signal as a second pulse width modulated signal having the first frequency and asecond duty cycle to alternately turn on and turn off the fourth switch; the fifth control signal to turn off the fifth switch; the sixth control signal to turn off the sixth switch; the seventh control signal to turn on the seventh switch; and the eighth control signal to turn on the eighth switch.

[0021] In one or more embodiments, when the control unit controls the buck and boost power converter to operate in the boost conversion mode, the control unit provides: the first control signal to turn on the first switch; the second control signal to turn on the second switch; the third control signal to turn off the third switch; the fourth control signal to turn off the fourth switch; the fifth control signal afirst pulse width modulated signal having afirst frequency and afirst duty cycle to alternately turn on and turn off the fifth switch; the sixth control signal asasecond pulse width modulated signal having the first frequency and asecond duty cycle to alternately turn on and turn off the sixth switch; the seventh control signal to turn off the seventh switch; and the eighth control signal to turn on the eighth switch.

[0022] In one or more embodiments, the control unit includes a plurality of analog-to-digital converter (ADCs) configured to provide digital values representing: an input voltage at the input node, an input current through the input node, an output voltage at the output node, an output current through the output node, and the control unit generates the first through eighth control signals to corresponding ones of the control terminals of the first through eighth switching devices so as to control switching of the first through eighth switching devices to cause the buck and boost power converter to operate selectively in one of a boost conversion mode and a buck conversion mode in response to the digital values.

[0023] According to one optional feature of this embodiment, the control unit is configured: to cause the buck and boost power converter to operate in the buck conversion mode when the input voltage is greater than asum of the output voltage and afirst fixed voltage, wherein the first fixed voltage is greater than or equal to zero volts; to cause the buck and boost power converter to operate in the boost conversion mode when the input voltage islessthan the output voltage; and to cause the buck and boost power converter to operate in a direct conversion mode when the output voltage is greater than adifference between the input voltage and the first fixed voltage, and less than output voltage.

[0024] As used herein for purposes of the present disclosure, the term "LED" should be understood to include any electroluminescent diode or other type of carrier injection/junction-based system that is capable of generating radiation in response to an electric signal. Thus, the term LED includes, but is not limited to, various semiconductor-based structures that emit light in response to current, light emitting polymers, organic light emitting diodes (OLEDs), electroluminescent strips, and the like. In particular, the term LED refersto light emitting diodes of all types (including semi-conductor and organic light emitting diodes) that may be configured to generate radiation in one or more of the infrared spectrum, ultraviolet spectrum, and various portions of the visible spectrum (generally including radiation wavelengths from approximately 380 nanometers to approximately 780 nanometers). Sbme examples of LEDs include, but are not limited to, various types of infrared LEDs, ultraviolet LEDs, red LEDs, blue LEDs, green LEDs, yellow LEDs, amber LEDs, orange LEDs, and white LEDs (discussed further below). For example, one implementation of an LED configured to generate essentially white

light (e.g., a white LED) may include a number of dies which respectively emit different spectra of electroluminescence that, in combination, mixto form essentially white light. In another implementation, a white light LED may be associated with a phosphor material that converts electroluminescence having afirst spectrum to adifferent second spectrum. In one example of this implementation, electroluminescence having a relatively short wavelength and narrow bandwidth spectrum "pumps" the phosphor material, which in turn radiates longer wavelength radiation having a somewhat broader spectrum.

[0025] It should also be understood that the term LED does not limit the physical and/or electrical package type of an LED. For example, as discussed above, an LED may refer to a single light emitting device having multiple dies that are configured to respectively emit different spectra of radiation (e.g., that may or may not be individually controllable). Also, an LED may be associated with a phosphor that is considered as an integral part of the LED (e.g., some types of white LEDs). In general, the term LED may refer to packaged LEDs, non-packaged LEDs, surface mount LEDs, chip-on-board LEDs, LEDs including some type of encasement and/ or optical element (e.g., adiffusing lens), etc.

[0026] The term "light source" should be understood to refer to any one or more of a variety of radiation sources, including, but not limited to, LED-based sources (including one or more LEDs as defined above), incandescent sources (e.g., filament lamps, halogen lamps), fluorescent sources, phosphorescent sources, high-intensity discharge sources (e.g., sodium vapor, mercury vapor, and metal halide lamps), lasers, other types of electroluminescent sources, pyro-luminescent sources (e.g., flames), candle-luminescent sources (e.g., gas mantles, carbon arc radiation sources), photo-luminescent sources (e.g., gaseous discharge sources), cathode luminescent sources using electronic satiation, galvano-luminescent sources, crystallo-luminescent sources, radioluminescent sources, and luminescent polymers.

[0027] A "lighting driver" isused herein to refer to an apparatus that supplies electrical power to one or more light sources in aformat to cause the light sourcesto emit light. In particular, a lighting driver may receive electrical power in afirst format (e.g., AC Mains power; afixed DCvoltage; etc.) and supplies power in a second format that is tailored to the requirements of the light source(s) (e.g., LED light source(s)) that it drives.

[0028] The terms "lighting unit" is used herein to refer to an apparatus including one or more light sources of same or different types. A given lighting unit may have any one of a variety of mounting arrangements for the light source(s), enclosure/housing arrangements and shapes, and/ or electrical and mechanical connection configurations. Additionally, agiven lighting unit optionally may be associated with (e.g., include, be coupled to and/or packaged together with) various other components (e.g., control circuitry; alighting driver) relating to the operation of the light source(s). An "LED-based lighting unit" refers to alighting unit that includes one or more LED-based light sources as discussed above, alone or in combination with other non LED-based light sources.

[0029] The term "controller" is used herein generally to describe various apparatus relating to the operation of apower converter. Acontroller can be implemented in numerous ways (e.g., such as with dedicated hardware) to perform various functions discussed herein. A "processor" isone example of acontroller which employs one or more microprocessors that may be programmed using software (e.g., microcode) to perform various functions discussed herein. Acontroller may be implemented with or without employing a processor, and also may be implemented as a combination of dedicated hardware to perform some functions and a processor (e.g., one or more programmed miaoprocessorsand associated circuitry) to perform other functions. Examples of controller components that may be employed in various embodiments of the present disclosure include, but are not limited to, conventional microprocessors, application specific integrated circuits (ASCs), and field-programmable gate arrays (FPGAs).

[0030] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0031] It should be appreciated that all combinations of the foregoing concepts and additional concepts discussed in greater detail below (provided such concepts are not mutually inconsistent) are contemplated as being part of the inventive subject matter disclosed herein.

In particular, all combinations of claimed subject matter appearing at the end of thisdisdosure are contemplated as being part of the inventive subject matter disclosed herein. It should also be appreciated that terminology explicitly employed herein that also may appear in any disclosure incorporated by reference should be accorded a meaning most consistent with the particular concepts disclosed herein.

Brief Description of the Drawings

[0032] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the prindplesof the invention.

[0033] FIG 1 illustrates an example embodiment of an apparatus induding a buck and boost converter.

[0034] FIG 2 illustrates one example embodiment of a control unit for a buck and boost converter.

[0035] FIG 3 is a timing diagram illustrating the timing of control signalsfor afirst operating mode (e.g., a buck conversion mode) of one embodiment of a buck and boost converter.

[0036] FIG 4 is a timing diagram illustrating the timing of control signalsfor asecond operating mode (e.g., a boost conversion mode) of one embodiment of a buck and boost converter.

[0037] FIG 5 is a timing diagram illustrating the timing of control signalsfor athird operating mode (e.g., adirect conversion mode) of one embodiment of a buck and boost converter.

[0038] FIG. 6 shows a state diagram illustrating transitions between various operating modes for one embodiment of a buck and boost converter.

Detailed Description

[0039] As discussed above, conventional buck-boost power converters exhibit some limitations in terms of efficiency, a limited range of input and output voltages, and the number of applications to which they can be applied. Therefore, Applicant herein has recognized and appreciated that it would be beneficial to provide a buck and boost converter which is capable in operating in a buck conversion mode and a boost conversion mode with greater efficiency over awide range of input and output voltages in many different applications.

[0040] In view of the foregoing, various embodiments and implementations of the present invention are directed to a buck and boost converter wherein one or more switches employed for a buck conversion operation are separate from and may be independently controlled with respect to one or more switches employed for a boost conversion operation.

[0041] FIG 1 illustrates an example embodiment of an apparatus 100 including a buck and boost converter. Apparatus 100 includes a power converter 110 and a control unit 120.

[0042] Fbwer converter 110 includes an input node 105 and an output node 115. Input node 105 isconnected to, and receives an input voltage VIN from, avoltage supply 10. Output node 115 isconnected to, and supplies an output voltage VOUT to, a load 20. Fbwer converter 110 also includes a first switch 3/V1, second switch 3/V2, third switch 3/V3, fourth switch 3/V4, fifth switch 3/V5, sixth switch S/V6, seventh switch 3/V7, eighth switch 3/V8, first capacitor CI, second capacitor C2, and an inductor L1. Fbwer converter 110 also includes first and second current sensing units 11 and I2, and voltage sampling resistors R1, F2, FB and F!4. In some embodiments, first through eighth switches S/V1~S/V8 are transistors, and in a particular embodiment are metal oxide semiconductor field effect transistors (MOSFETs). In some embodiments, one or more of the elementssuch asfirst capacitor CI, second capacitor C2, inductor L1, and voltage sampling resistors R1, F2, FB and F!4 may be realized with a combination of a plurality of series and or parallel arrangements of similar elements (e.g., CI could be realized by 2, 3 or 4 capacitors in parallel; L1 could be two inductors in series; etc.).

[0043] Control unit 120 receives samples of: the input voltage VIN sampled by the voltage

sampling resistors R1 and R2; the input current provided to input node 105 by voltage supply 10 and sampled by first current sensing unit 11; the output voltage VOUT sampled by the voltage sampling resistors R3 and R4; and the output current supplied to load 20 by power converter 110 and sampled by second current sensing unit I2. In response to these samples, control unit 120 generates eight switch control signals VA, VB, VC, VD, *VE,* VF, VGand VH for controlling the switched states of the eight switches S/V1~S/V8 to cause power converter 110 to convert the input voltage VIN at input node 105 to an output voltage VOUT at output node 115. In particular, control unit 120 supplies: VAto first switch 3/V1; VBto second switch 3/V2; VCto third switch 3/V3; VDto fourth switch S/V4; VEto fifth switch 3/V5; VFto sixth switch S/V6; VG to seventh switch 3/V7; VH to eighth switch 3/V8. Further details of a particular embodiment of control unit 120 will be provided with respect to FIG. 2 below.

[0044] Fbwer converter 110 is a buck-boost converter, and which may also be referred to as a buck and boost converter, and is capable of operating in a buck conversion mode and a boost conversion mode as explained in greater detail below. Fbwer converter 110 includes a buck conversion circuit and a boost conversion circuit which are capable or being controlled independently of each other. Fbwer converter 110 also includes a direct conversion mode which transfersthe input voltage VIN at input node 105 to output node 115 asthe output voltage VOUT. .

[0045] The buck conversion circuit includes a first set of switches including third and fourth switches3/V3 and 3/V4 which are switched in response to pulse width modulation (FWM) signals for power converter 110 to operate in a buck conversion mode. The third and fourth switches 3/V3 and 3/V4 operate together with CI, C2, L1 and 3/V7 to realize a buck conversion mode. In the buck conversion mode, first, seventh and eighth switches S/V1, 3/V7 and 3/V8 remain turned ON while the second, fifth and sixth switches 3/V2, 3/V5 and 3/V6 remain turned OFF. In some embodiments, in the buck conversion mode the switches are controlled according to the following sequence: (1) turn ON first switch 3/V1; (2) turn OFFfifth and sixth switches 3/V5 and 3/V6; (3) turn OFF second switch 3/V2; (4) turn ON seventh switch S/V7; (5) turn ON eighth switch 3/V8; and (6) drive third and fourth switches 3/V3 and S/V4 with a FWM signal whose duty cycle and/or frequency can be adjusted or varied to convert the input voltage

VIN to the output voltage VOUT. Thus while it seen that all eight of the switches S/V1 ~S/V8 must have proper settingsfor implementing the buck conversion mode, it isthe particular switching operations of third and fourth switches 3/V3 and S/V4 in response to FWM control signals from control unit 120 that realize the voltage buck effect to convert the input voltage VIN to the output voltage VOUT.

[0046] The boost conversion circuit includes a second set of switches including fifth and sixth switches S/V5 and 3/V6. The fifth and sixth switches S/V5 and 3/V6 operate together with CI , C2, L1 and 3/V2 to realize a boost conversion mode. In the boost conversion mode, first and eighth switches S/V1 and S/V8 remain turned ON while the third and fourth switches S/V3 and 3/V4 remain turned OFF In some embodiments, in the buck conversion mode the switches are controlled according to the following sequence: (1) turn ON first switch 3/V1 ; (2) turn OFFthird and fourth switches S/V3 and 3/V4; (3) turn OFF seventh switch 3/V7; (4) turn ON second switch 3/V2; (5) turn ON eighth switch 3/V8; and (6) drive fifth and sixth switches 3/V5 and S/V6 with a FWM signal whose duty cycle and/ or frequency can be adjusted or varied to convert the input voltage VIN to the output voltage VOUT. Thus while it seen that all eight of the switches 3/V1 -S/V8 must have proper settingsfor implementing the boost conversion mode, it isthe particular switching operations of fifth and sixth switches S/V5 and 3/V6 in response to FWM control signalsfrom control unit 120 that realizesthe voltage boost effect to convert the input voltage VIN to the output voltage VOUT.

[0047] The direct conversion circuit includes a third set of switches including second and seventh S/V2 and S/V7, which are turned ON for power converter 110 to operate in adirect conversion mode. The second and seventh switches 3/V2 and S/V7 operate together with CI , C2, and L1 to realize the direct conversion mode. In the direct conversion mode, first, second, seventh and eighth switches 3/V1 , S/V2, 3/V7 and S/V8 remain turned ON while third, fourth, fifth and sixth switches S/V3, 3/V4, 3/V5 and 3/V6 remain turned OFF.

[0048] First switch 3/V1 provides input reverse protection for power converter 110, and eighth switch 3/V8 provides output reverse protection for power converter 110, and may also be used to switch power converter 110 ON or OFF under various conditions

[0049] In operation, the output voltage VOUTof power converter 110 can be lessthan, equal to, or greater than the input voltage VIN. For example, input voltage VIN may be provided from voltage supply 10 (e.g., asolar panel) whose voltage may not be constant, but instead which may vary significantly depending on environmental conditions, and output voltage VOUTmay be determined by the nature of load 20, for example load 20 may comprise a battery having a substantially fixed voltage. In that case, control 120 needs to control power converter 110 to operate in different modes depending on whether the input voltage VIN is greater than, equal to, or lessthan the output voltage VOUT.

[0050] Theoretically, control unit 120 should control the first through eighth switches S/V1~S/V8 to cause apparatus 100: to operate in the boost conversion mode when the input voltage VIN at input node 105 is less than the output voltage VOUT at output node 115; to operate in the direct conversion mode when the input voltage VIN is equal to the output voltage VOUT; and to operate in the buck conversion mode when the input voltage VIN is greater than the output voltage VOUT.

[0051] However, due to small voltage drops across the switches in power converter 110, and perhaps a desire to provide hysteresis, in practice control unit 120 causesapparatus 100 to operate in the direct conversion mode over a small range of input voltages VIN about the output voltage VOUT.

[0052] Accordingly, in practice control unit 120 controls power converter 110 to operate: in a buck conversion mode when the input voltage VIN is greater than a buck threshold voltage; in a boost conversion mode when the input voltage VIN is less than a boost threshold voltage; and in adirect conversion mode when the input voltage VIN is between the boost threshold voltage and the buck threshold voltage. In some embodiments, the buck threshold voltage is equal to the sum of the output voltage VOUT and afirst fixed voltage. In general, the first fixed voltage is relatively small, for example less than 1 volt, and in particular 0.5 volts. In some embodiments, the first threshold voltage may be zero. The boost threshold voltage is equal to the difference between the output voltage VOUT and asecond fixed voltage. In some embodiments, the second fixed voltage may be zero, if which case the boost threshold voltage equalsthe output voltage VOUT.

[0053] FIG 2 illustrates one example embodiment of a control unit 200 for a buck and boost converter. Control unit 200 may be one embodiment of control unit 120 of FIG. 1. Control unit 200 includes: a plurality of analog-to-digital converters (ADCs) 212, 214, 216 and 218; a comparator 220; acont roller 230; a clock generator 240; ageneral purpose input/output (GPIO) interface 250; and a pulse width modulation (FWM) generator 260.

[0054] Controller 230, which may comprise a processor such as a general purpose processor, an application specific integrated circuit (A9Q, etc., includes a clock/ timer circuit 232. In an embodiment when controller 230 comprises a programmable processor, it may further comprise a memory device including code or instruct ions for causing the processor to execute an algorithm for controlling operations of a power converter, such as power converter 110, as described in greater detail below.

[0055] GPIOinterface 250 outputsfirst, second, seventh and eighth control signals VA, VB, VGand VH. FWM generator 260 outputsthird, fourth, fifth and sixth control signals VQ VD, VE and VF, which are FWM signals with a variable duty cycle and/ or frequency for implementing a buck conversion mode or a boost conversion mode and as will be explained in greater detail below. FWM generator 260 may include several FWM circuitswhich may operate independently, for example one FWM circuit each for third, fourth, fifth and sixth FWM control signals VQ VD, VEand VF.

[0056] An operation of control unit 200 will now be provided in a specific embodiment where control unit 200 is used as control unit 120 of apparatus 100.

[0057] In operation, ADCs 212, 214, 216 and 218 receive samples of: an input voltage (e.g., the input voltage VIN sampled by the voltage sampling resistors R1 and R2 in FIG 1); an input current (e.g., the input current provided to input node 105 by voltage supply 10 and sampled by first current sensing unit 11 in FIG. 1); an output voltage (e.g., the output voltage VOUT sampled by the voltage sampling resistors R3 and R4 in FIG. 1); and an output current (e.g., the output current supplied to load 20 by power converter 110 and sampled by second current sensing unit I2). In response to the received sample voltages and sample currents, ADCs 212, 214, 216 and 218 produce digital values representing the analog input samples. Comparator 220

compares the digital values representing the sampled input voltage, and the digital values representing the sampled output voltage, and provides a comparison signal to controller 230 that allows controller 230 to determine whether to control power converter 110 to operate in a buck conversion mode, a boost conversion mode, or adirect conversion mode.

[0058] As explained above, in response to the comparison of the sampled input voltage and the sampled output voltage, controller 230 determines whet her to control power converter 110 to operate in a buck conversion mode, a boost conversion mode, or adirect conversion mode. In particular, when the input voltage VIN is greater than a buck threshold voltage (e.g., the output voltage VOUT pius a small first fixed voltage), then controller 230 determines that power converter 110 should operate in a buck conversion mode. When the input voltage VIN is less than a boost threshold voltage (e.g., the output voltage VOUT), then controller 230 determines that power converter 110 should operate in a boost conversion mode. And when the input voltage VIN is between the boost threshold voltage and the buck threshold voltage, controller 230 determines that power converter 110 should operate in adirect conversion mode.

[0059] Controller 230 causes GPIO interface 250 to output first, second, seventh and eighth control signals VA, VB, VGand VH, and FWM generator 260 to output third, fourth, fifth and sixth control signals VC, VD, VEand VF, according to the selected operating mode of power converter 100.

[0060] As explained above, unit 200 may be one embodiment of control unit 120 of FIG. 2. However, it should be understood that other embodimentsof control unit 120 of FIG 1 are possible. In some embodiments, comparator 220 may be omitted and controller 230 may itself compare the digital values for the sampled input voltage and the sampled output voltage. In other embodiments, ADCs212 and 214 and comparator 220 may be replaced by an analog comparator that compares the sampled input and output voltages, followed by asingle ADC which convertsthe comparison result to adigital value. Other arrangements are possible.

[0061] FIG 3 is a timing diagram illustrating the timing of control signalsfor afirst operating mode, in particular for a buck conversion mode. As illustrated in FIG. 3, when controller 230

determines that power converter 110 should operate in the buck conversion mode, controller 230 causes GPIO interface 250 to output first, seventh and eighth output signals VA, VGand VH at a high level so as to turn ON first, seventh and eighth switches 3/V1, 3/V7 and 3/V8, and to output second output signal VBat a low level so as to keep second switch 3/V2 OFF. Controller 230 also causes FWM generator 260 to generate FWM signals VCand VDto control switching operations of third and fourth switches S/V3 and S/V4 with an appropriate frequency and duty cycle for a buck conversion mode for converting the input voltage VIN at input node 105 to the output voltage VOUT at output node 115. At thistime, FWM generator 260 also outputsfifth and sixth control signals VEand VFat a low level so as to maintain fifth and sixth switches 3/V5 and S/V6 in an OFF state. dock generator 230 provides a clock signal for controlling the timing of operations in control unit 200, and particularly may be used to generate the frequency and or duty cycle of the FWM signals VCand VD. Controller 230 may vary or adjust at least one of the frequency and the duty cycle of the FWM signals VCand VD to regulate the output provided to output node 115.

[0062] FIG 4 is a timing diagram illustrating the timing of control signalsfor asecond operating mode, in particular for a boost conversion mode. As illustrated in FIG. 4, when controller 230 determines that power converter 110 should operate in the boost conversion mode, controller 230 causes GPIO interface 250 to output first, second and eighth output signals VA VBand VH at a high level so as to turn ON first, second and eighth switches 3/V1, 3/V2 and 3/V8, and to output seventh output signal VGat alow level so as to keep seventh switch 3/V7 OFF. Controller 230 also causes FWM generator 260 to generate FWM signals VE and VFto control switching operations of fifth and sixth switches 3/V5 and 3/V6 with an appropriate frequency and duty cycle for a boost conversion mode for converting the input voltage VIN at input node 105 to the output voltage VOUT at output node 115. A thistime, FWM generator 260 also outputsthird and fourth control signals VCand VDat alow level so as to maintain third and fourth switches 3/V3 and S/V4 in an OFF state. Qock generator 230 provides a clock signal for controlling the timing of operations in control unit 200, and particularly may be used to generate the frequency and or duty cycle of the FWM signals VE and VF. Controller 230 may vary or adjust at least one of the frequency and the duty cycle of

the FWM signals VEand VFto regulate the output provided to output node 115.

[0063] FIG 5 is a timing diagram illustrating the timing of control signalsfor athird operating mode, in particular adirect conversion mode. As illustrated in FIG. 5, when controller 230 determines that power converter 110 should operate in the direct conversion mode, controller 230 causes GPIO interface 250 to output first, second, seventh and eighth output signals VA, VB, VGand VH at ahigh level so asto turn ON first, second, seventh and eighth switches S/V1, 3/V2, 3/V7 and 3/V8. At this time controller 230 also causes FWM generator 260 to output third, fourth, fifth and sixth control signals VC, VD, VEand VFat alow level so asto maintain third, fourth, fifth and sixth switches 3/V3, S/V4, 3/V5 and 3/V6 in an OFF state.

[0064] FIG 6 shows a state diagram illustrating transitions between various operating modes for one embodiment of a buck and boost converter. As illustrated in FIG. 6, TH1 is the buck threshold which is the transition point of the input voltage VIN between the buck conversion mode and the direct conversion mode, and TH2 isthe boost threshold which isthe transition point of the input voltage VIN between the direct conversion mode and the boost conversion mode. When the input voltage VIN at input node 105 increases, power converter 110 changes operating mode according to a sequence: Boost conversion mode -> direct conversion mode -> buck conversion mode. When the input voltage VIN isdecreasing, power converter 110 changes operating mode accordingto the sequence: Buck conversion mode -> direct conversion mode -> boost conversion mode.

[0065] Apparatus 100 as described above may be employed in a variety of devices or applications, indudingfor example: solar power controllers and inverters; battery chargers with high effident charging functionality for different batteries (e.g., Li-ion battery, Lead-add battery, Ni-MH battery, and Lithium iron phosphate battery); lighting drivers, for instance, constant current LEDdriversfor LED-based lighting unitsor other lighting units employing other light sources; general purpose DC-DC converters which may be included in consumer electronic devices, healthcare devices, etc.

[0066] While several inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures

for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented byway of example only and that, within the scope of the appended claims and equivalentsthereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

[0067] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0068] The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

[0069] The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elementsthal are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified.

[0070] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified.

[0071] It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one step or act, the order of the steps or acts of the method is not necessarily limited to the order in which the steps or acts of the method are recited. Also, reference numerals appearing in the claims in parentheses, if any, are provided merely for convenience and should not be construed as limiting the claims in any way.

What is claimed is:

CLAIMS

1. An apparatus (100), comprising:

a power converter (110) configured to convert an input voltage (VIN) to an output voltage (VOUT) and to supply the output voltage to a load (20), the power converter including:

a buck conversion circuit including a first set of switches (3/V3 and 3/V4), and

a boost conversion circuit including a second set of switches (3/V5 and 3/V6), wherein the second set of switches are separate from and capable of being controlled independently from the first set of switches; and

acontrol unit (120, 200) configured to control an operation of the power converter,

wherein the control unit is configured to control delivery of power from the power converter to the load viathe buck conversion circuit in a buck conversion mode by controlling switching operations of the first set of switches, and

wherein the control unit is configured to control the delivery of the power from the power converter to the load viathe boost conversion circuit in a boost conversion mode by controlling switching operations of the second set of switches.

2. The apparatus of claim 1, wherein the control unit isconfigured to receive a sample of the input voltage (Vinput), asample of the output voltage (Voutput), asample of an input current (linput) supplied to the power converter, and a sample of an output current (loutput) supplied by the power converter, and isconfigured to control the delivery of the power to the load based on the sample of the input voltage, the sample of the output voltage, the sample of an input current and the sample of the output current.

3. The apparatus of claim 2, wherein the control unit includes a plurality of analog-to-digital converter (ADCs) (212/214/216/218) configured to convert the sample of the input voltage, the sample of the output voltage, the sample of the input current and the sample of the output current to digital values.

4. The apparatus of claim 2, wherein the control unit includes circuitry (220) configured to compare the input voltage and the output voltage to each other, wherein the control unit selects an operating mode of the power converter based on a result of the comparison.

5. The apparatus of claim 2, wherein the control unit is configured to control the delivery of power from the power converter to the load viathe buck conversion circuit by switching at least one of the switches (S/V3, 3/V4) of the first set of switches at a switching frequency and aduty cycle, and by adjusting at least one of the switching frequency and the duty cycle in response to adifference between the sample of the input voltage and the sample of the output voltage.

6. The apparatus of claim 2, wherein the control unit is configured to control the delivery of power from the power converter to the load viathe boost conversion circuit by switching at least one of the switches (3/V5, S/V6) of the second set of switches at a switching frequency and aduty cycle, and by adjusting at least one of the switching frequency and the duty cycle in response to adifference between the sample of the input voltage and the sample of the output voltage.

7. The apparatus of claim 1, wherein the control unit is configured to control delivery of power from the power converter to the load when the input voltage isgreater than asum (TH1) of the output voltage and afirst fixed voltage, wherein the first fixed voltage is greater than or equal to zero volts, by controlling the switching operations of the first set of switches; and wherein the control unit is configured to control the delivery of the power from the power converter to the load when the input voltage is less than the output voltage (TH2) by controlling the switching operations of the second set of switches.

8. The apparatus of claim 7, wherein the first fixed voltage is less than 1 volt.

9. The apparatus of claim 7, wherein the control unit isfurther configured to control the

power converter to operate in a direct conversion mode when the output voltage is greater than adifference between the input voltage and the first fixed voltage (TH2), and lessthan a sum of the input voltage and the second fixed voltage (TH1).

10. A method, comprising:

sampling an input voltage (Vinput), an output voltage (Voutput), an input current (linput), and an output current (loutput) of a power converter (110) that includes a buck conversion circuit including a first set of switches (3/V3 & S/V4), and a boost conversion circuit including a second set of switches (S/V5 and S/V6), wherein the second set of switches are separate from and capable of being controlled independently from the first set of switches;

when the input voltage is greater than a sum (TH1) of the output voltage and afirst fixed voltage that is greater than or equal to zero volts, controlling delivery of power from the power converter to a load (20) by controlling switching operations of the first set of switches; and

when the input voltage is lessthan the output voltage (TH2), controlling the delivery of the power from the power converter to the load by controlling switching operations of the second set of switches.

11. The method of claim 10, wherein controlling delivery of power from the power converter to a load by controlling operations of the first set of switches of the buck conversion circuit comprises supplying one or more control signals (VQ VD) to one or more switches of the first set of switches and pulse width modulating the one or more control signals.

12. The method of claim 11, wherein pulse width modulating the one or more control signals comprises adjusting one of afrequency and aduty cycle of each pulse width modulated control signal in response to adifference between the input voltage and the output voltage.

13. The method of claim 10, wherein controlling delivery of power from the power converter to a load by controlling the switching operations of the second set of switches of the

boost conversion circuit comprises supplying one or more control signals (VE, VF) to one or more switches of the second set of switches and pulse width modulating the one or more control signals.

14. The method of claim 13, wherein pulse width modulating the one or more control signals comprises adjusting one of afrequency and aduty cycle of each pulse width modulated control signal in response to a difference between the input voltage and the output voltage.

15. The method of claim 10, wherein the first fixed voltage is lessthan 1 volt.

16. An apparatus, comprising:

a buck and boost power converter (110) capable of operating in a buck conversion mode and in a boost conversion mode, the buck and boost power converter comprising:

an input node (105);

an output node (115);

afirst switch (S/V1) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the first switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the input node;

afirst capacitor (CI) connected between the second terminal of the first switch and ground;

asecond switch (S/V1) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the second switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminal of the first switch and to the first capacitor;

athird switch (3/V3) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the third switch to control acurrent path between the first terminal and the second terminal, wherein the third switch isconnected in parallel with the second switch;

afourth switch (3/V4) having afirst terminal, a second terminal, and acontrol terminal for selectively opening and closing the fourth switch to control a current path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminals of the second and third switches, and the second terminal is connected to ground;

an inductor (L1) having afirst terminal and asecond terminal, wherein the first terminal is connected to the second terminals of the second, third and fourth switches;

afifth switch (3/V5) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the fifth switch to control a current path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminal of the inductor, and the second terminal is connected to ground;

asixth switch (3/V6) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the sixth switch to control a current path between the first terminal and the second terminal, wherein the first terminal isconnected to the second terminal of the inductor and the first terminal of the fifth switch;

aseventh switch (3/V7) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the seventh switch to control acurrent path between the first terminal and the second terminal, wherein the sixth switch is connected in parallel with the fifth switch;

asecond capacitor (C2) connected between the second terminalsof the sixth and seventh switches and ground; and

an eighth switch (S/V8) having afirst terminal, asecond terminal, and acontrol terminal for selectively opening and closing the sixth switch to control acurrent path between the first terminal and the second terminal, wherein the first terminal isconnected to the second capacitor and the second terminalsof the sixth and seventh switches, and wherein the second terminal is connected to the output node; and

acontrol unit (120, 200) configured to provide first through eighth control signals (VA~VH) to corresponding ones of the control terminals of the first through eighth switching devices so asto control switching of the first through eighth switching devices to cause the

buck and boost power converter to operate selectively in one of a boost conversion mode and a buck conversion mode.

17. The apparatus of claim 16, wherein when the control unit controls the buck and boost power converter to operate in the buck conversion mode, the control unit provides:

the first control signal (VA) to turn on the first switch (3/V1);

the second control signal (VB) to turn off the second switch (3/V2);

the third control signal (VC) asafirst pulse width modulated signal having afirst frequency and afirst duty cycle to alternately turn on and turn off thethird switch (S/V3);

the fourth control signal (VD) as a second pulse width modulated signal having the first frequency and asecond duty cycle to alternately turn on and turn off the fourth switch (S/V4);

the fifth control signal(VE) to turn off the fifth switch (3/V5);

the sixth control signal (VF) to turn off the sixth switch (3/V6);

the seventh control signal (VG) to turn on the seventh switch (S/V7); and

the eighth control signal (VH) to turn on the eighth switch (S/V8).

18. The apparatus of claim 16, wherein when the control unit controlsthe buck and boost power converter to operate in the boost conversion mode, the control unit provides:

the first control signal (VA) to turn on the first switch (3/V1);

the second control signal (VB) turn on the second switch (3/V2);

the third control signal (VQ to turn off the third switch (S/V3);

the fourth control signal(VD) to turn off the fourth switch (3/V4);

the fifth control signal (VEE) asafirst pulse width modulated signal having afirst frequency and afirst duty cycle to alternately turn on and turn off the fifth switch (3/V5);

the sixth control signal (VF) as a second pulse width modulated signal having the first frequency and a second duty cycle to alternately turn on and turn off the sixth switch (3/V6);

the seventh control signal (VG) to turn off the seventh switch (S/V7); and

the eighth control signal (VH) to turn on the eighth switch (S/V8).

19. The apparatus of claim 16, wherein the control unit (200) includes a plurality of analog-to-digital converter (ADCs) (212/214/216/218) configured to provide digital values representing: an input voltage (Vinput) at the input node, an input current (linput) through the input node, an output voltage (Voutput) at the output node, an output current (loutput) through the output node,

wherein the control unit provides the first through eighth control signals (VA-VH) to corresponding ones of the control terminals of the first through eighth switching devices so as to control switching of the first through eighth switching devices to cause the buck and boost power converter to operate selectively in one of the boost conversion mode and the buck conversion mode in response to the digital values.

20. The apparatus of claim 19, wherein the control unit (120, 200) is configured to cause the buck and boost power converter to operate in the buck conversion mode when the input voltage is greater than a sum (TH1) of the output voltage and a first fixed voltage, wherein the first fixed voltage is greater than or equal to zero volts; wherein the control unit is configured to cause the buck and boost power converter to operate in the boost conversion mode when the input voltage is less than the output voltage (TH2); and to cause the buck and boost power converter to operate in a direct conversion mode when the output voltage is greater than adifference between the input voltage and the first fixed voltage, and lessthan the output voltage (TH2).

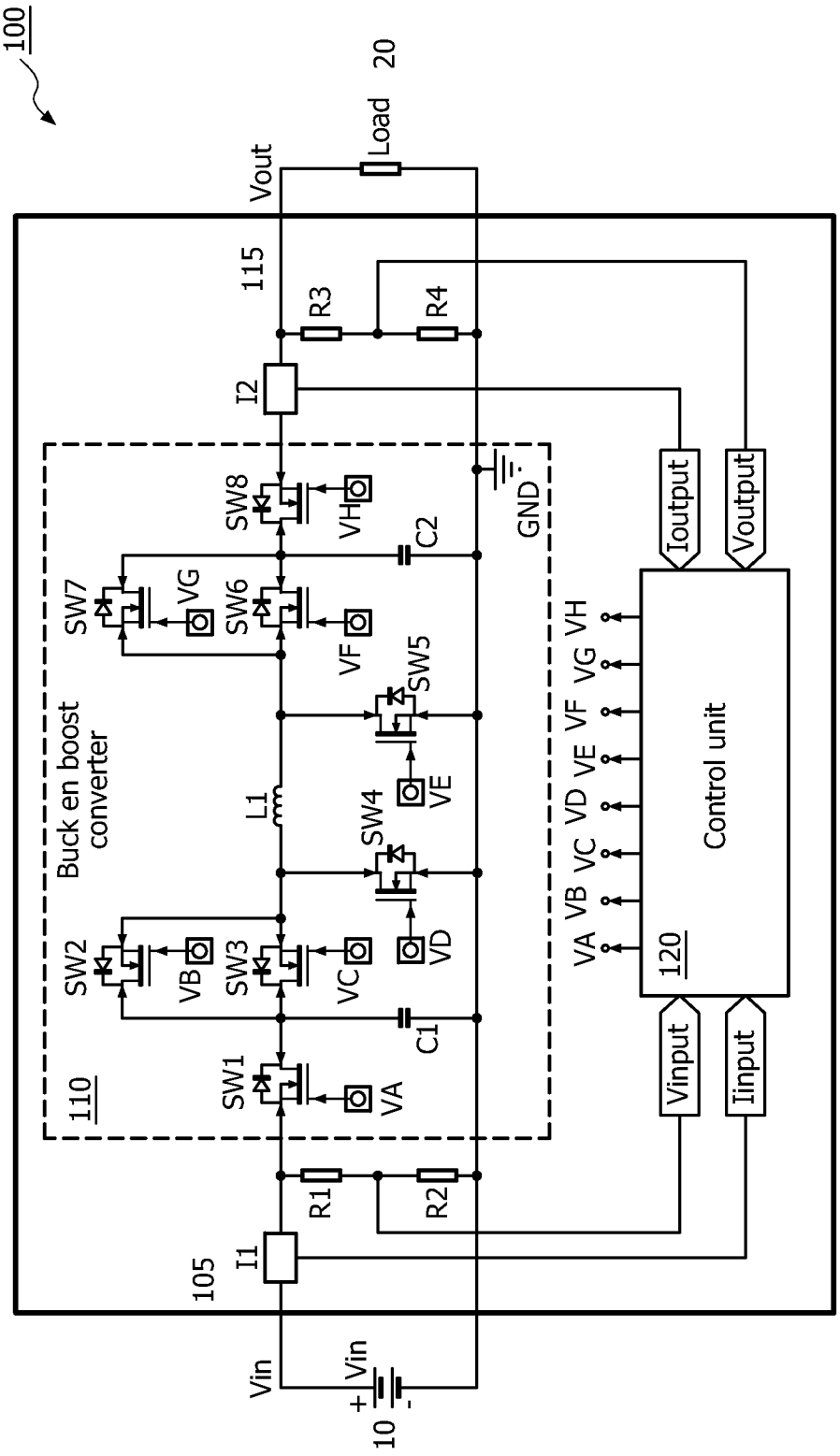
100
Load
20
Vout
115
R3
R4
I2
SW8
VH
C2
GND
SW7
VG
SW6
VF
SW5
VE
SW4
VD
SW2
VB
SW3
VC
SW1
VA
C1
L1
Buck en boost converter
110
R1
R2
I1
105
Vin
Vin
10
Ioutput
Voutput
Vinput
Iinput
VA VB VC VD VE VF VG VH
Control unit
120

FIG. 1

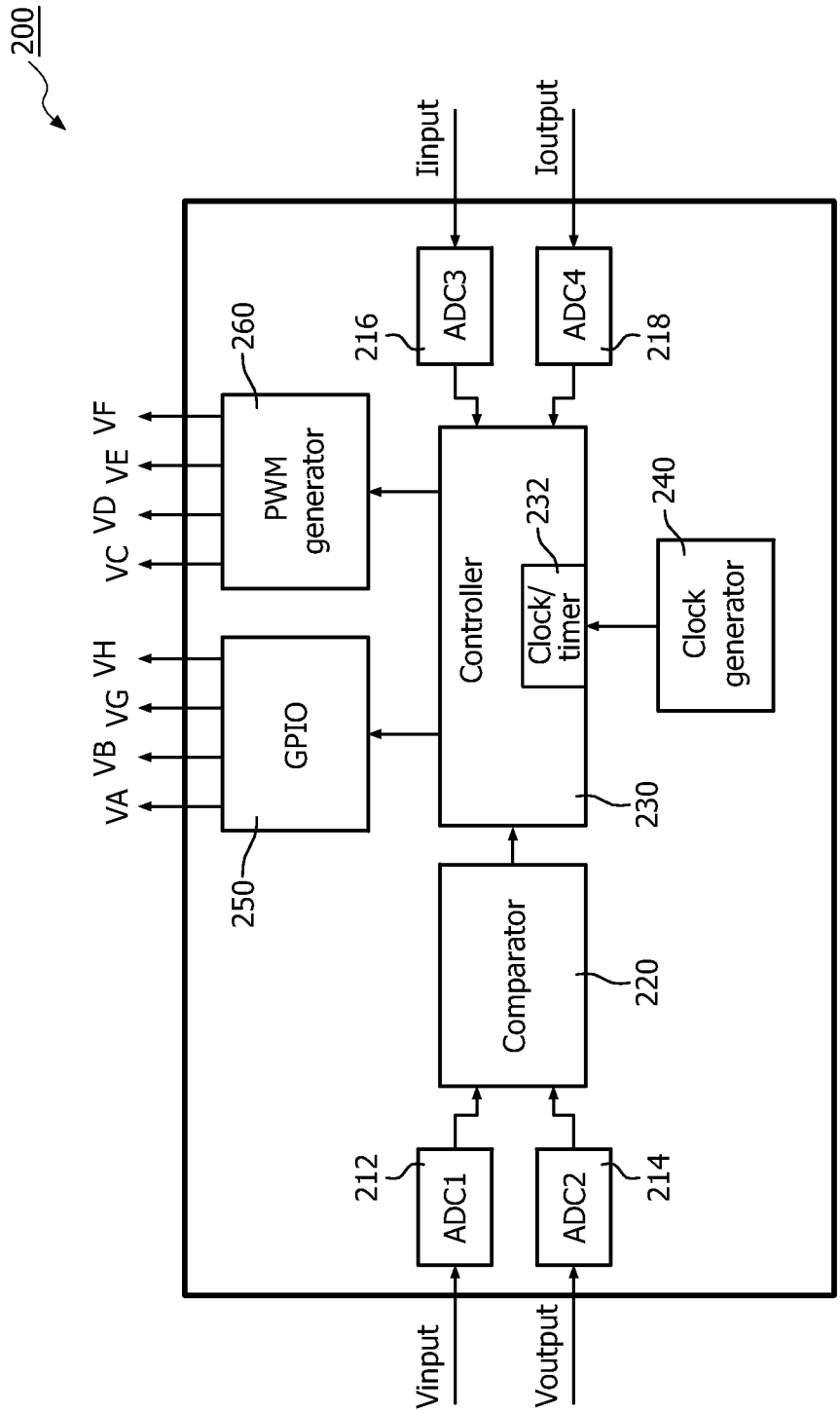
200
Iinput
Ioutput
ADC3
ADC4
216
218
260
PWM generator
VF
VE
VD
VC
Controller
232
Clock/ timer
240
Clock generator
VH
VG
VB
VA
GPIO
250
230
Comparator
220
212
ADC1
ADC2
214
Vinput
Voutput

FIG. 2

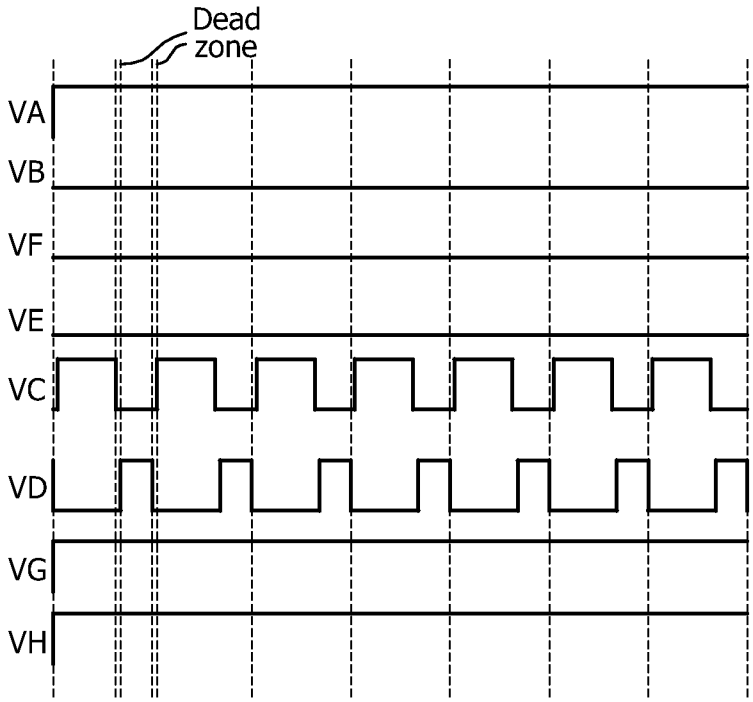

FIG. 3

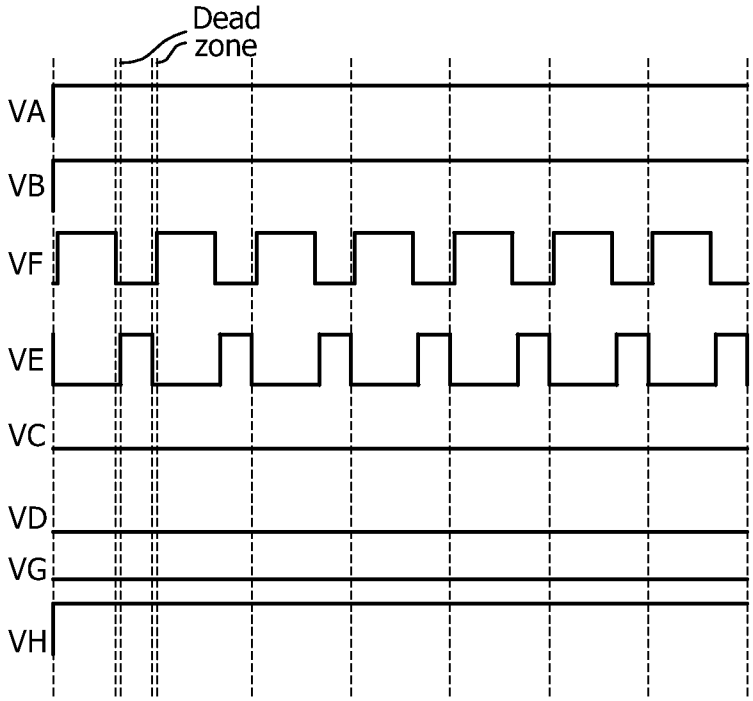

FIG. 4

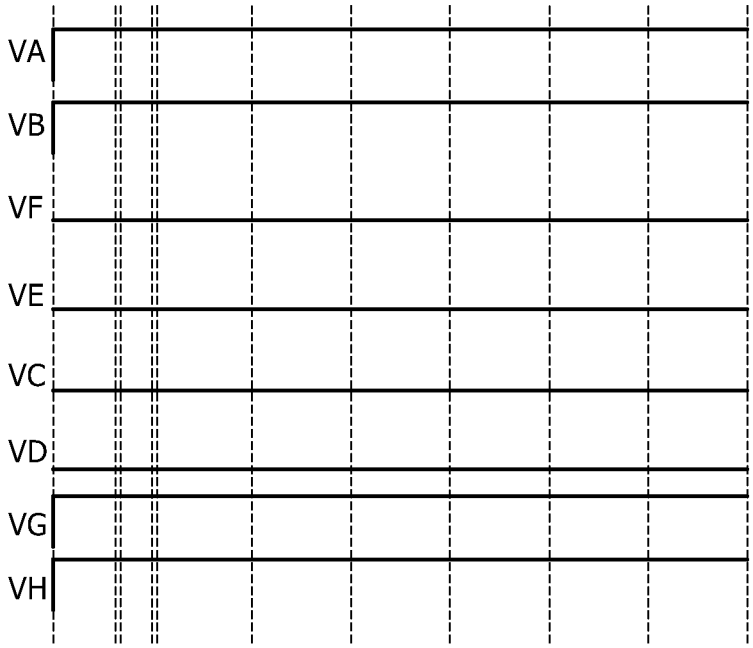
VA
VB
VF
VE
VC
VD
VG
VH

FIG. 5

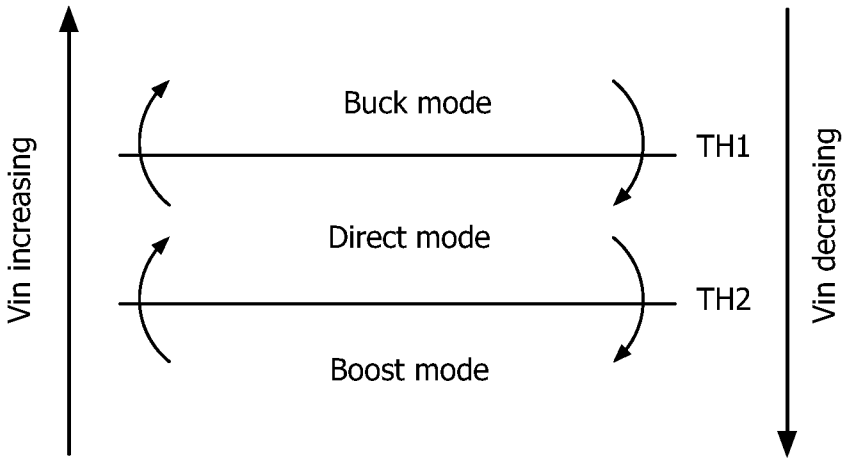
Vin increasing
Buck mode
TH1
Direct mode
TH2
Boost mode
Vin decreasing

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2013/050087

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/089915 Al (QIU WEI HONG [US] ET AL) 21 Apri l 2011 (2011-04-21)	1-20
Y	paragraphs [0016] - [0029] ; figures 1,2 paragraphs [0036] - [0038] ; figure 4	16

X	US 7 495 419 Bl (JU SHU-ING [US]) 24 February 2009 (2009-02-24) col umn 2, line 61 - col umn 5, line 34; figures 1,2 col umn 6, lines 58-61 ; figure 9A	1, 10, 16

Y	EP 1 548 921 Al (CIT ALCATEL [FR]) 29 June 2005 (2005-06-29) abstract	16

	-/- ·	

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" documentwhich may throw doubts on priority claim(s) orwhich is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 Apri l 2013	22/04/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	van Wesenbeeck, R

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DEUTY S: "Optimi zing transi stor performance in synchronous recti fier buck converters ", APPLI ED POWER ELECTRONICS CONFERENCE AND EXPOSITION , 2000. APEC 2000. FI FTEENTH ANNUAL I EEE, , vol . 2 , 6 February 2000 (2000-02-06) , pages 675-678, XP010371606, D0I : 10. 1109/APEC. 2000. 822577 ISBN : 978-0-7803-5864-5 page 675 , secti on 11; f i gure 1 -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2013/050087

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011089915 A1	21-04-2011	CN 102055332 A	11-05-2011
		US 2011089915 A1	21-04-2011
US 7495419 B1	24-02-2009	NONE	
EP 1548921 A1	29-06-2005	EP 1548921 A1	29-06-2005
		US 2005135124 A1	23-06-2005