



(51) International Patent Classification:
H10K 50/813 (2023.01)

(21) International Application Number:
PCT/CN2023/070336

(22) International Filing Date:
04 January 2023 (04.01.2023)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE,
KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU,
LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG,
NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS,
RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ,
TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA,
ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, CV,
GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST,
SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ,
RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ,
DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,
LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— with international search report (Art. 21(3))

(54) Title: DISPLAY SUBSTRATE, DISPLAY APPARATUS, AND METHOD OF REPAIRING DISPLAY SUBSTRATE

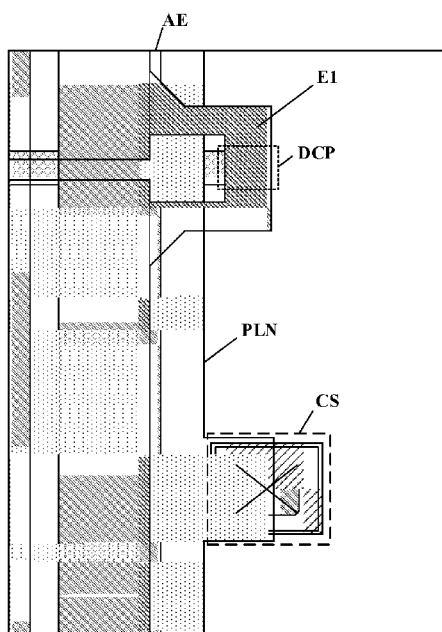


FIG. 14A

(57) Abstract: A display substrate is provided. The display substrate includes: a first conductive part; a second conductive part; and a repairing structure connecting the first conductive part with the second conductive part; wherein the first conductive part and the second conductive part are parts of a first electrode; the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line; and the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side.

DISPLAY SUBSTRATE, DISPLAY APPARATUS, AND METHOD OF REPAIRING DISPLAY SUBSTRATE

TECHNICAL FIELD

[0001] The present invention relates to display technology, more particularly, to a display substrate, a display apparatus, and a method of repairing a display substrate.

BACKGROUND

[0002] In recent years, more and more technology companies focus on development of transparent displays. For example, transparent displays have been used in store window display. A viewer can not only see the information displayed on the screen of a transparent display, but also the objects located behind the transparent display. Both the real product and on-screen product-related information can be presented simultaneously, enabling customers to understand the full range of the product information, and to obtain a better display experience. Transparent display panels have been used in vehicular display and various other commercial scenarios such as window display in a hotel or department store setting. The transparent display panels have the advantages of excellent display quality and highly realistic display effects.

SUMMARY

[0003] In one aspect, the present disclosure provides a display substrate, comprising: a first conductive part; a second conductive part; and a repairing structure connecting the first conductive part with the second conductive part; wherein the first conductive part and the second conductive part are parts of a first electrode; the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line; and the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side.

[0004] Optionally, the first conductive part and the second conductive part are parts of a first electrode in a same subpixel region.

[0005] Optionally, the first electrode comprises a plurality of sub-layers; and the first conductive part and the second conductive part are parts of one sub-layer of the plurality of sub-layers of the first electrode.

[0006] Optionally, the first electrode is an anode of a light emitting element.

[0007] Optionally, the repairing structure comprises a first portion, a second portion connecting the first portion with the first conductive part, and a third portion connecting the second portion with the second conductive part; and the first conductive part and the second conductive part are otherwise spaced apart from each other.

[0008] Optionally, the first electrode is electrically connected to a drain electrode of a transistor through the first portion.

[0009] Optionally, the display substrate further comprises a light shield in a light shield layer on a side of the first conductive part, the second conductive part, and the repairing structure closer to a base substrate; wherein the first portion is connected to the light shield; the light shield is electrically connected to a drain electrode of a transistor; the first portion is electrically connected to the drain electrode of the transistor through the light shield.

[0010] Optionally, the first portion is directly connected to a drain electrode of a transistor.

[0011] Optionally, the first portion extends along a first direction; the second portion extends along a second direction; and the third portion extends along a second direction.

[0012] Optionally, the display substrate further comprises a first gap spacing apart the first conductive part and the second conductive part; and a second gap surrounded by the first portion, the second portion, the third portion, a portion of the first conductive part, a portion of the second conductive part, and the first gap; wherein the first gap is connected with the second gap.

[0013] Optionally, a first portion of a light shield is in a region having the first gap; and a second portion of the light shield is in a region having the second gap.

[0014] Optionally, an orthographic projection of the light shield on a base substrate partially overlaps with an orthographic projection of the first portion on the base substrate.

[0015] Optionally, the second portion is spaced apart from the light shield by a first minimum distance; the third portion is spaced apart from the light shield by a second minimum distance; the second portion of the light shield have an average line width; the first minimum distance is at least 2 times of the average line width; and the second minimum distance is at least 2 times of the average line width.

[0016] Optionally, at least the first portion comprises a curved line portion.

[0017] Optionally, the first portion comprises a straight line portion, a first curved line portion, and a second curved line portion; the straight line portion connects the first curved line portion with the second curved line portion; the first curved line portion connects the straight line portion with the second portion; and the second curved line portion connects the straight line portion with the third portion.

[0018] Optionally, at least the first portion comprises multiple straight line portions connected together.

[0019] Optionally, the first portion comprises a first straight line portion, a second straight line portion, a third straight line portion, a fourth straight line portion, and a fifth straight line

portion; the second straight line portion connects the first straight line portion with the third straight line portion; the third straight line portion connects the second straight line portion with the second portion; the second portion connects the third straight line portion with the first conductive part; the first straight line portion connects the second straight line portion with the fourth straight line portion; the fourth straight line portion connects the first straight line portion with the fifth straight line portion; the fifth straight line portion connects the fourth straight line portion with the third portion; and the third portion connects the fifth straight line portion with the second conductive part.

[0020] Optionally, the first straight line portion, the third straight line portion, and the fifth straight line portion respectively extend along a first direction; and the second straight line portion and the fourth straight line portion respectively extend along a second direction.

[0021] In another aspect, the present disclosure provides a display apparatus, comprising the above display substrate, and one or more integrated circuits connected to the display substrate.

[0022] In another aspect, the present disclosure provides a method of repairing a display substrate: wherein the display substrate includes: a first conductive part; a second conductive part; and a repairing structure connecting the first conductive part with the second conductive part; wherein the first conductive part and the second conductive part are parts of a first electrode; the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line; the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side; and the repairing structure comprises a first portion, a second portion connecting the first portion with the first conductive part, and a third portion connecting the second portion with the second conductive part; wherein the method comprises: disconnecting the first conductive part from at least a portion of the first portion, or disconnecting the second conductive part from at least a portion of the first portion.

BRIEF DESCRIPTION OF THE FIGURES

[0023] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0024] FIG. 1 is a schematic diagram illustrating the structure of a display substrate in some embodiments according to the present disclosure.

[0025] FIG. 2 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure.

[0026] FIG. 3 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure.

[0027] FIG. 4 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure.

[0028] FIG. 5 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure.

[0029] FIG. 6 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure.

[0030] FIG. 7 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure.

[0031] FIG. 8 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure.

[0032] FIG. 9A is a cross-sectional view of a connecting structure in some embodiments according to the present disclosure.

[0033] FIG. 9B is a cross-sectional view of a connecting structure in some embodiments according to the present disclosure.

[0034] FIG. 10A illustrates the structure of a portion of a display substrate in some embodiments according to the present disclosure.

[0035] FIG. 10B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 10A.

[0036] FIG. 10C illustrates the structure of a semiconductor material layer in the portion of a display substrate depicted in FIG. 10A.

[0037] FIG. 10D illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 10A.

[0038] FIG. 10E illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 10A.

[0039] FIG. 10F illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 10A.

[0040] FIG. 10G illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 10A.

[0041] FIG. 10H illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 10A.

[0042] FIG. 10I illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 10A.

- [0043] FIG. 10J illustrates the structure of a pixel definition layer in the portion of a display substrate depicted in FIG. 10A.
- [0044] FIG. 10K illustrates the structure of a black matrix layer in the portion of a display substrate depicted in FIG. 10A.
- [0045] FIG. 11A illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate depicted in FIG. 10A.
- [0046] FIG. 11B illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure.
- [0047] FIG. 11C illustrates the structure of a gate layer and a signal line layer in the portion of a display substrate depicted in FIG. 10A.
- [0048] FIG. 11D illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure.
- [0049] FIG. 11E illustrates the structure of a pixel definition layer and an auxiliary electrode in some embodiments according to the present disclosure.
- [0050] FIG. 11F illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure.
- [0051] FIG. 11G illustrates the structure of an auxiliary electrode and a plurality of connecting structures in some embodiments according to the present disclosure.
- [0052] FIG. 11H illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure.
- [0053] FIG. 12A illustrates the structure of a planarization layer in the portion of a display substrate in some embodiments according to the present disclosure.
- [0054] FIG. 12B illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate in some embodiments according to the present disclosure.
- [0055] FIG. 12C illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure.
- [0056] FIG. 13A illustrates the structure of a planarization layer in the portion of a display substrate in some embodiments according to the present disclosure.
- [0057] FIG. 13B illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate in some embodiments according to the present disclosure.
- [0058] FIG. 13C illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure.

[0059] FIG. 14A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure.

[0060] FIG. 14B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 14A.

[0061] FIG. 14C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 14A.

[0062] FIG. 14D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 14A.

[0063] FIG. 14E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 14A.

[0064] FIG. 14F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 14A.

[0065] FIG. 14G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 14A.

[0066] FIG. 14H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 14A.

[0067] FIG. 15A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure.

[0068] FIG. 15B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 15A.

[0069] FIG. 15C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 15A.

[0070] FIG. 15D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 15A.

[0071] FIG. 15E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 15A.

[0072] FIG. 15F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 15A.

[0073] FIG. 15G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 15A.

[0074] FIG. 15H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 15A.

[0075] FIG. 16A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure.

[0076] FIG. 16B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 16A.

[0077] FIG. 16C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 16A.

[0078] FIG. 16D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 16A.

[0079] FIG. 16E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 16A.

[0080] FIG. 16F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 16A.

[0081] FIG. 16G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 16A.

[0082] FIG. 16H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 16A.

[0083] FIG. 17A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure.

[0084] FIG. 17B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 17A.

[0085] FIG. 17C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 17A.

[0086] FIG. 17D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 17A.

[0087] FIG. 17E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 17A.

[0088] FIG. 17F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 17A.

[0089] FIG. 17G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 17A.

[0090] FIG. 17H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 17A.

DETAILED DESCRIPTION

[0091] The disclosure will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0092] The present disclosure provides, *inter alia*, a display substrate, a display apparatus, and a method of repairing a display substrate that substantially obviate one or more of the problems due to limitations and disadvantages of the related art. In one aspect, the present disclosure provides a display substrate. In some embodiments, the display substrate includes a first conductive part; a second conductive part; and a repairing structure connects the first conductive part with the second conductive part. Optionally, the first conductive part and the second conductive part are parts of a first electrode. Optionally, the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line. Optionally, the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side.

[0093] FIG. 1 is a schematic diagram illustrating the structure of a display substrate in some embodiments according to the present disclosure. Referring to FIG. 1, the display substrate includes a subpixel region SR and an inter-subpixel region ISR. As used herein, a subpixel region refers to a light emission region of a subpixel, such as a region corresponding to a pixel electrode in a liquid crystal display substrate, a region corresponding to a light emissive layer in a light emitting diode display substrate. Optionally, a pixel may include a number of separate light emission regions corresponding to a number of subpixels in the pixel. Optionally, the subpixel region is a light emission region of a red color subpixel. Optionally, the subpixel region is a light emission region of a green color subpixel. Optionally, the subpixel region is a light emission region of a blue color subpixel. Optionally, the subpixel region is a light emission region of a white color subpixel.

[0094] As used herein, an inter-subpixel region refers to a region between adjacent subpixel regions, such as a region corresponding to a black matrix in a liquid crystal display, a region corresponding to a pixel definition layer or a black matrix in an organic light emitting diode display panel. Optionally, the inter-subpixel region is a region between adjacent subpixel regions in a same pixel. Optionally, the inter-subpixel region is a region between two adjacent subpixel regions from two adjacent pixels. Optionally, the inter-subpixel region is a region between a subpixel region of a red color subpixel and a subpixel region of an adjacent green color subpixel. Optionally, the inter-subpixel region is a region between a subpixel region of a red color subpixel and a subpixel region of an adjacent blue color subpixel. Optionally, the inter-subpixel region is a region between a subpixel region of a green color subpixel and a subpixel region of an adjacent blue color subpixel.

[0095] Referring to FIG. 1, the display substrate includes a light emitting element LE in the subpixel region SR, and a connecting structure CS in the inter-subpixel region ISR. The connecting structure CS may be disposed in any appropriate location in the inter-subpixel region ISR. In one example, the display substrate includes a plurality of pixels px. A respective pixel of the plurality of pixels px includes one or more subpixels, e.g., a red subpixel, a blue subpixel, and a green subpixel. In another example, the connecting structure CS is disposed in a location in the inter-subpixel region ISR between two subpixels respectively from two adjacent pixels of the plurality of pixels px, as depicted in FIG. 1. In another example, the connecting structure CS is disposed in a location in the inter-subpixel region ISR between two subpixels in a same pixel of the plurality of pixels px.

[0096] FIG. 2 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure. For example, FIG. 2 may be a cross-sectional view along an A-A' line of the display substrate depicted in FIG. 1. Referring to FIG. 2, the display substrate in some embodiments includes a planarization layer PLN; a light emitting element LE on the planarization layer PLN and in the subpixel region SR; and a connecting structure CS in the inter-subpixel region ISR.

[0097] In some embodiments, the light emitting element LE includes a first electrode E1 (e.g., an anode), an organic layer OL on the first electrode E1, and a second electrode E2 (e.g., a cathode) on a side of the organic layer OL away from the first electrode E1. The organic layer OL may include one or more organic material layers. In one example, the organic layer OL includes a light emitting layer. In another example, the organic layer OL further includes at least one of a hole injection layer, a hole transport layer, an emitting material layer, an electron transport layer, an electron injection layer, and a charge generating layer.

[0098] In some embodiments, the display substrate further includes an auxiliary electrode AE in a layer different from the second electrode E2, and the auxiliary electrode AE is electrically connected to the second electrode E2. Optionally, the connecting structure CS electrically connects the auxiliary electrode AE and the second electrode E2.

[0099] In some embodiments, the planarization layer PLN is an insulating material layer that is in direct contact with at least a portion of the first electrode E1. The planarization layer PLN facilitates formation of layers thereon by planarizing a surface of the substrate prior to forming the layers on the planarization layer PLN. The planarization layer PLN extends at least partially in the subpixel region SR. Optionally, the planarization layer PLN extends at least partially in the subpixel region SR, and extends at least partially in the inter-subpixel region ISR.

[0100] Various appropriate insulating materials and various appropriate fabricating methods may be used for making the planarization layer PLN. For example, an insulating material may

be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process or a sputtering process, e.g., a magnetron sputtering process. Examples of appropriate insulating materials include various appropriate resin materials, polyimide, silicon oxide (SiO_y), silicon nitride (SiNy, e.g., Si₃N₄), and silicon oxynitride (SiO_xN_y).

[0101] FIG. 3 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 3, the connecting structure in some embodiments includes a first connecting electrode CE1, a second connecting electrode CE2, and a third connecting electrode CE3 sequentially stacked. In one example, the first connecting electrode CE1 is in direct contact with the second connecting electrode CE2, and the second connecting electrode CE2 is in direct contact with the third connecting electrode CE3. The second connecting electrode CE2 connects the first connecting electrode CE1 and the third connecting electrode CE3.

[0102] Various appropriate conductive electrode materials and various appropriate fabricating methods may be used to make the connecting electrodes. For example, a conductive electrode material may be deposited on the substrate by, e.g., sputtering or vapor deposition, and patterned by, e.g., lithography such as a wet etching process to form the connecting electrodes. Examples of appropriate conductive electrode materials include, but are not limited to, metallic conductive electrode materials and non-metallic conductive electrode materials. Examples of appropriate metallic conductive electrode materials include, but are not limited to, aluminum, chromium, tungsten, titanium, tantalum, molybdenum, copper, and alloys or laminates containing the same. Examples of appropriate non-metallic conductive electrode materials include, but are not limited to, various transparent metal oxide electrode materials and transparent nano-carbon tubes. Examples of transparent metal oxide materials include, but are not limited to, indium tin oxide, indium zinc oxide, indium gallium oxide, and indium gallium zinc oxide.

[0103] In one example, the first connecting electrode CE1 and the third connecting electrode CE3 are made of indium tin oxide. In another example, the second connecting electrode CE2 is made of a reflective electrode material such as aluminum alloy.

[0104] Various appropriate conductive electrode materials and various appropriate fabricating methods may be used to make the first electrode E1. For example, a conductive electrode material may be deposited on the substrate by, e.g., sputtering or vapor deposition, and patterned by, e.g., lithography such as a wet etching process to form the connecting electrodes. Examples of appropriate conductive electrode materials include, but are not limited to, metallic conductive electrode materials and non-metallic conductive electrode materials. Examples of appropriate metallic conductive electrode materials include, but are not limited to, aluminum, chromium, tungsten, titanium, tantalum, molybdenum, copper, and alloys or laminates containing the same. Examples of appropriate non-metallic conductive electrode

materials include, but are not limited to, various transparent metal oxide electrode materials and transparent nano-carbon tubes. Examples of transparent metal oxide materials include, but are not limited to, indium tin oxide, indium zinc oxide, indium gallium oxide, and indium gallium zinc oxide.

[0105] In some embodiments, the first electrode E1 includes a plurality of sub-layers. Optionally, the first electrode E1 includes a first sub-layer SUB1, a second sub-layer SUB2, and a third sub-layer SUB3 sequentially stacked.

[0106] In one example, the first sub-layer SUB1 and the third sub-layer SUB3 are made of indium tin oxide. In another example, the second sub-layer SUB2 is made of a reflective electrode material such as aluminum alloy.

[0107] In some embodiments, the first sub-layer SUB1 and the first connecting electrode CE1 are in a same layer; the second sub-layer SUB2 and the second connecting electrode CE2 are in a same layer; and the third sub-layer SUB3 and the third connecting electrode CE3 are in a same layer. Optionally, the first sub-layer SUB1 and the first connecting electrode CE1 are spaced apart from each other, e.g., by a pixel definition layer PDL; the second sub-layer SUB2 and the second connecting electrode CE2 are spaced apart from each other, e.g., by the pixel definition layer PDL; and the third sub-layer SUB3 and the third connecting electrode CE3 are spaced apart from each other, e.g., by the pixel definition layer PDL.

[0108] Various appropriate conductive electrode materials and various appropriate fabricating methods may be used to make the second electrode E2. For example, a conductive electrode material may be deposited on the substrate by, e.g., sputtering or vapor deposition, and patterned by, e.g., lithography such as a wet etching process to form the connecting electrodes. Examples of appropriate conductive electrode materials for making the second electrode E2 include, but are not limited to, various transparent metal oxide electrode materials and transparent nano-carbon tubes. Examples of transparent metal oxide materials include, but are not limited to, indium tin oxide, indium zinc oxide, indium gallium oxide, and indium gallium zinc oxide. In one example, the second electrode E2 is made of indium zinc oxide.

[0109] In some embodiments, the second electrode E2 is in direct contact with at least one of the first connecting electrode CE1, the second connecting electrode CE2, or the third connecting electrode CE3. In one example, the second electrode E2 is in direct contact with the first connecting electrode CE1. In another example, the second electrode E2 is in direct contact with the second connecting electrode CE2. In another example, the second electrode E2 is in direct contact with the first connecting electrode CE1 and the second connecting electrode CE2. In another example, the second electrode E2 is in direct contact with the second connecting electrode CE2 and the third connecting electrode CE3. In another example,

the second electrode E2 is in direct contact with the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3.

[0110] In some embodiments, referring to FIG. 2 and FIG. 3, the auxiliary electrode AE is on a side of the first connecting electrode CE1 away from the second connecting electrode CE2. In one example, the auxiliary electrode AE is in a same layer as a source electrode S and a drain electrode D of a transistor in the display substrate.

[0111] In some embodiments, the display substrate includes a base substrate BS; a light shielding layer LSL on the base substrate, and comprising a light shield LS; a buffer layer BUF on a side of the light shielding layer LSL away from the base substrate BS; an active layer ACT on a side of the buffer layer BUF away from the base substrate BS, wherein an orthographic projection of the light shield LS on the base substrate BS at least partially overlaps with (e.g., completely covers) an orthographic projection of the active layer ACT on the base substrate BS; a gate insulating layer GI on a side of the active layer ACT away from the base substrate BS; a gate layer CT comprising a gate electrode G on a side of the gate insulating layer GI away from the base substrate BS; an inter-layer dielectric layer ILD on a side of the gate layer CT away from the base substrate BS; a signal line layer SL comprising a source electrode S, a drain electrode D, and an auxiliary electrode AE on a side of the inter-layer dielectric layer ILD away from the base substrate BS; a passivation layer PVX on a side of the signal line layer SL away from the base substrate BS; a planarization layer PLN on a side of the passivation layer PVX away from the base substrate BS; a pixel definition layer PDL, a light emitting element LE, and a connecting structure CS on a side of the planarization layer PLN away from the base substrate BS. The pixel definition layer PDL defines a subpixel aperture for receiving at least one sub-layer (e.g., a light emitting layer) of the organic layer OL.

[0112] Referring to FIG. 2 and FIG. 3, in some embodiments, the connecting structure CS further includes at least one of a residual organic layer ROL stacked on a side of the third connecting electrode CE3 away from the second connecting electrode CE2; and a residual second electrode RE2 stacked on a side of the residual organic layer ROL away from the third connecting electrode CE3. In one example as depicted in FIG. 2 and FIG. 3, the connecting structure CS includes a sequentially stacked structure comprising a first connecting electrode CE1, a second connecting electrode CE2 on the first connecting electrode CE1, a third connecting electrode CE3 on a side of the second connecting electrode CE2 away from the first connecting electrode CE1, a residual organic layer ROL on a side of the third connecting electrode CE3 away from the second connecting electrode CE2, and a residual second electrode RE2 on a side of the residual organic layer ROL away from the third connecting electrode CE3.

[0113] In some embodiments, the residual organic layer ROL is in a same layer as the organic layer OL, and at least partially (e.g., completely) segregated from the organic layer OL.

Optionally, at least one sub-layer of the residual organic layer ROL and at least one sub-layer of the organic layer OL are in a same layer. In one example, the residual organic layer ROL includes a residual hole transport layer in a same layer as a hole transport layer of the organic layer OL. In another example, the residual organic layer ROL includes a residual hole injection layer in a same layer as a hole injection layer of the organic layer OL. In one example, the residual organic layer ROL includes a residual electron transport layer in a same layer as an electron transport layer of the organic layer OL. In another example, the residual organic layer ROL includes a residual electron injection layer in a same layer as an electron injection layer of the organic layer OL.

[0114] In some embodiments, the residual second electrode RE2 is in a same layer as the second electrode E2, and at least partially (e.g., completely) segregated from the second electrode E2.

[0115] Referring to FIG. 2 and FIG. 3, in some embodiments, the first connecting electrode CE1 extends through a via to connect with the auxiliary electrode AE. In one example depicted in FIG. 2 and FIG. 3, the via extends through the planarization layer PLN and the passivation layer PVX. As shown in FIG. 2 and FIG. 3, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate BS completely covers an orthographic projection of the first connecting electrode CE1 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS completely covers an orthographic projection of the second connecting electrode CE2 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS completely covers an orthographic projection of the third connecting electrode CE3 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS completely covers an orthographic projection of the connecting structure CS on the base substrate BS.

[0116] In some embodiments, the connecting structure CS further includes at least one of a residual organic layer ROL or a residual second electrode RE2. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS completely covers an orthographic projection of the residual organic layer ROL on the base substrate BS, and completely covers an orthographic projection of the residual second electrode RE2 on the base substrate BS.

[0117] By having the orthographic projection of the planarization layer PLN on the base substrate BS completely covers the orthographic projection of the connecting structure CS on the base substrate BS, the connecting structure CS (e.g., layers of the connecting structure CS) are formed on a planarized surface. The connecting structure CS can be made to have a substantially flat morphology, obviating damages to the organic layer OL caused by protrusions of the connecting structure CS.

[0118] FIG. 4 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure. FIG. 5 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 4 and FIG. 5, in some embodiments, the first connecting electrode CE1 extends through a via to connect with the auxiliary electrode AE. In one example depicted in FIG. 4, the via extends through the passivation layer PVX but not the planarization layer PLN. As shown in FIG. 4 and FIG. 5, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate BS is non-overlapping with an orthographic projection of the first connecting electrode CE1 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS is non-overlapping with an orthographic projection of the second connecting electrode CE2 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS is non-overlapping with an orthographic projection of the third connecting electrode CE3 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS is non-overlapping with an orthographic projection of the connecting structure CS on the base substrate BS.

[0119] In some embodiments, the connecting structure CS further includes at least one of a residual organic layer ROL or a residual second electrode RE2. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS is non-overlapping with an orthographic projection of the residual organic layer ROL on the base substrate BS, and is non-overlapping with an orthographic projection of the residual second electrode RE2 on the base substrate BS.

[0120] By having the orthographic projection of the planarization layer PLN on the base substrate BS non-overlapping with an orthographic projection of the connecting structure CS on the base substrate BS, the connecting structure CS (e.g., layers of the connecting structure CS) are formed having a relatively smaller height with respect to the base substrate BS. When the substrate is subject to brush cleaning during the fabricating process, edges of the connecting structure CS is less prone to be damages. Intact edges of the connecting structure CS can ensure segregation of the residual organic layer ROL from the organic layer OL, and segregation of the residual second electrode RE2 from the second electrode E2.

[0121] FIG. 6 is a cross-sectional view of a display substrate in some embodiments according to the present disclosure. FIG. 7 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 6 and FIG. 7, the first connecting electrode CE1 extends through a via to connect with the auxiliary electrode AE. In one example depicted in FIG. 6 and FIG. 7, the via extends through the passivation layer PVX but not the planarization layer PLN. As shown in FIG. 6 and FIG. 7, in some embodiments, an orthographic projection of the planarization layer PLN on a base

substrate BS only partially overlaps with an orthographic projection of the first connecting electrode CE1 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS only partially overlaps with an orthographic projection of the second connecting electrode CE2 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS only partially overlaps with an orthographic projection of the third connecting electrode CE3 on the base substrate BS. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS only partially overlaps with an orthographic projection of the connecting structure CS on the base substrate BS.

[0122] In some embodiments, the connecting structure CS further includes at least one of a residual organic layer ROL or a residual second electrode RE2. Optionally, the orthographic projection of the planarization layer PLN on the base substrate BS only partially overlaps with an orthographic projection of the residual organic layer ROL on the base substrate BS, and only partially overlaps with an orthographic projection of the residual second electrode RE2 on the base substrate BS.

[0123] By having the orthographic projection of the planarization layer PLN on the base substrate BS only partially overlaps with an orthographic projection of the connecting structure CS on the base substrate BS, the edges of the connecting structure CS may be maintained substantially intact when the substrate is subject to brush cleaning during the fabricating process, ensuring segregation of the residual organic layer ROL from the organic layer OL, and segregation of the residual second electrode RE2 from the second electrode E2. At the same time, the connecting structure CS may be made without large protrusions that may damage the organic layer OL.

[0124] FIG. 8 is a schematic diagram illustrating the structure of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 8, FIG. 2, FIG. 4, and FIG. 6, in some embodiments, the second connecting electrode CE2 includes an upper surface in contact with the third connecting electrode CE3, a lower surface in contact with the first connecting electrode CE1 and opposite to the upper surface. In some embodiments, a cross-section along a plane intersecting the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3, and perpendicular to a main surface of the base substrate BS (e.g., a cross-section as shown in any of FIG. 2 to FIG. 7) includes a top side located within the upper surface and a bottom side located within the lower surface, an orthographic projection of the bottom side on the base substrate BS covers an orthographic projection of the top side on the base substrate BS.

[0125] Having the auxiliary electrode AE further reduces the voltage drop across the extension path of the second electrode E2 when the display substrate is in operation. Accordingly, the second electrode can be made relatively thinner, thereby increasing light

transmittance of the display substrate. In the present display substrate, the orthographic projection of the bottom side of the cross-section of the second connecting electrode CE2 on the base substrate BS covers the orthographic projection of the top side of the cross-section of the second connecting electrode CE2 on the base substrate BS. In some embodiments, the second connecting electrode CE2 has a slope structure located between its upper and lower surfaces, as described further below, and this slope structure facilitates the achievement of a larger contact area between the second electrode E2 and the connecting structure CS, reducing the contact resistance between the second electrode E2 and the connecting structure CS, further effectively reducing the voltage drop across the extension path of the second electrode E2 during operation of the display substrate. Accordingly, excessive voltage drop across the second electrode E2 can be obviated, light transmittance of the display substrate can be further improved by making the second electrode E2 thinner, further enhancing the brightness uniformity of the image displayed by the display substrate.

[0126] As discussed above, the orthographic projection of the auxiliary electrode AE on the base substrate BS is non-overlapping with the orthographic projection of the subpixel region SR on the base substrate BS, thereby minimizing the effect of the auxiliary electrode AE on light emission in the subpixel region SR. The auxiliary electrode AE and the connecting structure CS may have various appropriate relative positional relationship. In one example, the orthographic projection of the auxiliary electrode AE on the base substrate BS is non-overlapping with the orthographic projection of the connecting structure CS on the base substrate BS. In another example, the orthographic projection of the auxiliary electrode AE on the base substrate BS is at least partially overlapping with the orthographic projection of the connecting structure CS on the base substrate BS, to increase aperture ratio of the display substrate. The auxiliary electrode AE is in a layer (e.g., the signal line layer SL) on a side of the organic layer OL closer to the base substrate BS, to obviate adverse effects of the auxiliary electrode AE on the light emitting layer of the organic layer OL.

[0127] In some embodiments, an orthographic projection of the first connecting electrode CE1 on the base substrate BS completely covers an orthographic projection of the third connecting electrode CE3 on the base substrate BS; and an orthographic projection of the second connecting electrode CE2 on the base substrate BS does not exceed the orthographic projection of the third connecting electrode CE3 on the base substrate BS. In one example, in a cross-section along a plane intersecting the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3, and perpendicular to a main surface of the base substrate BS (e.g., a cross-section as shown in any of FIG. 2 to FIG. 8), the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3 have a Γ shape, which is conducive for forming a stable and effective connection between the second electrode E2 and the connecting structure CS.

[0128] In some embodiments, the second connecting electrode CE2 includes an upper surface in contact with the third connecting electrode CE3, a lower surface in contact with the first connecting electrode CE1 and opposite to the upper surface. In some embodiments, a cross-section along a plane intersecting the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3, and perpendicular to a main surface of the base substrate BS (e.g., a cross-section as shown in any of FIG. 2 to FIG. 7) includes a top side located within the upper surface, a bottom side located within the lower surface, and a lateral side connecting the top side and the bottom side. The lateral side and the lower surface intersect at an intersection point within the lower surface. An included angle between a line from any point on the lateral side to the intersection point and the lower surface is less than or equal to 90 degrees, wherein an opening of the included angle is facing the second connecting electrode CE2. A slope structure of the second connecting electrode CE2 having the included angle is conducive for allowing the material of the second electrode E2 to spread onto the lateral side of the second connecting electrode CE2 during the fabrication process of the display substrate, facilitating the achievement of a larger contact area between the second electrode E2 and the second connecting electrode CE2.

[0129] FIG. 9A is a cross-sectional view of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 9A, the second connecting electrode CE2 has a cross-section perpendicular to its upper and lower surfaces, a height of the cross-section along a vertical direction being H. The cross-section of the second connecting electrode CE2 includes a top side located in the upper surface, a bottom side located in the lower surface, and a lateral side connecting the top side to the bottom side. The lateral side and the bottom side intersect to form an acute angle α . The acute angle α shown in FIG. 9A is an example of the aforementioned included angle.

[0130] The lateral side of the second connecting electrode CE2 may have any appropriate morphology. In one example, the lateral side may be substantially flat. In another example, the lateral side may be uneven or irregular. FIG. 9B is a cross-sectional view of a connecting structure in some embodiments according to the present disclosure. Referring to FIG. 9B, the lateral side is uneven. The lateral side and the lower surface intersect to form an acute angle β .

[0131] The inventors of the present disclosure discover, through extensive experiments, that degrees of the included angle can affect the effective connection between the second electrode E2 and the second connecting electrode CE2. A relatively small included angle may lead to occurrence of bulge on the second connecting electrode CE2, preventing or reducing effective connection between the second electrode E2 and the second connecting electrode CE2. The inventors of the present disclosure discover, through extensive experiments, an included angle in a range between 45 degrees and 70 degrees is optimal for avoiding bulge on the second

connecting electrode CE2 and forming effective connection between the second electrode E2 and the second connecting electrode CE2.

[0132] The cross-section of the second connecting electrode CE2 may have various appropriate shapes. In one example depicted in FIG. 9A, the cross-section of the second connecting electrode CE2 has a trapezoidal shape.

[0133] Referring to FIG. 2, FIG. 4, and FIG. 6, the display substrate in some embodiments further includes a pixel definition layer PDL surrounding the subpixel region SR. Optionally, an orthographic projection of the planarization layer PLN on a base substrate BS at least partially overlaps with (e.g., at least 30%, at least 40%, at least 50%, at least 60%, at least 70%, at least 80%, at least 90%, at least 95%, or at least 99%) an orthographic projection of the pixel definition layer PDL on the base substrate BS. Optionally, an orthographic projection of the pixel definition layer PDL on the base substrate BS is non-overlapping with an orthographic projection of the second connecting electrode CE2 on the base substrate BS, and is non-overlapping with an orthographic projection of the third connecting electrode CE3 on the base substrate BS.

[0134] In some embodiments, the second electrode E2 extends from the subpixel region SR, over the pixel definition layer PDL, and into the inter-subpixel region ISR to be in direct contact with at least one of the first connecting electrode CE1, the second connecting electrode CE2, or the third connecting electrode CE3.

[0135] In some embodiments, at least one sub-layer of the organic layer OL extends from the subpixel region SR, over the pixel definition layer PDL, and into the inter-subpixel region ISR.

[0136] In some embodiments, the display substrate includes a stacked structure comprising the pixel definition layer PDL; a portion of at least one sub-layer of the organic layer OL on the pixel definition layer PDL and in direct contact with the pixel definition layer PDL; and a portion of the second electrode E2 on a side of the portion of at least one sub-layer of the organic layer OL away from the pixel definition layer PDL, and in direct contact with the portion of at least one sub-layer of the organic layer OL. Optionally, an orthographic projection of the second electrode E2 on the base substrate BS at least partially overlaps with (e.g., completely covers) an orthographic projection of the pixel definition layer PDL on the base substrate BS. Optionally, an orthographic projection of the at least one sub-layer of the organic layer OL on the base substrate BS at least partially overlaps with (e.g., completely covers) an orthographic projection of the pixel definition layer PDL on the base substrate BS.

[0137] In some embodiments, referring to FIG. 8, the connecting structure CS has an open groove GV formed between the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3. The second electrode E2 extends at least partially into the open groove GV to be in direct contact with at least one of the first

connecting electrode CE1, the second connecting electrode CE2, or the third connecting electrode CE3.

[0138] In some embodiments, an orthographic projection of the third connecting electrode CE3 on a base substrate BS covers an orthographic projection of the open groove GV on the base substrate BS, and at least partially overlaps with (e.g., completely covers) an orthographic projection of the second connecting electrode CE2 on the base substrate BS. Optionally, an orthographic projection of the first connecting electrode CE1 on the base substrate BS covers an orthographic projection of the open groove GV on the base substrate BS, and at least partially overlaps with (e.g., completely covers) an orthographic projection of the second connecting electrode CE2 on the base substrate BS. Optionally, the orthographic projection of the third connecting electrode CE3 on the base substrate BS partially overlaps with an orthographic projection of the second electrode E2 on the base substrate BS.

[0139] In some embodiments, referring to FIG. 2, FIG. 4, FIG. 6, and FIG. 8, the open groove GV has an open side open toward the pixel definition layer PDL. The second electrode E2 extends through the open side into the open groove GV to be in direct contact with at least one of the first connecting electrode CE1, the second connecting electrode CE2, and the third connecting electrode CE3.

[0140] In some embodiments, the open groove has an upper wall, a lower wall and a side wall. The upper wall of the open groove GV is formed by a portion of the third connecting electrode CE3 that extends towards the pixel definition layer PDL and not in direct contact with the second connecting electrode CE2. The lower wall is formed by a portion of the first connecting electrode CE1 that extends towards the pixel definition layer PDL and not in direct contact with the second connecting electrode CE2. The side wall is formed by a portion of the second connecting electrode CE2. The upper wall extends along a horizontal direction parallel to a main surface of the base substrate BS for a first length, the lower wall extends along the horizontal direction parallel to the main surface of the base substrate BS for a second length. Optionally, the second length is greater than the first length.

[0141] Referring to FIG. 9A and FIG. 9B, the first length is denoted as D1, and the second length is denoted as D2. The presence of the open groove GV in the connecting structure facilitates the extension of the material of the second electrode E2 into the open groove GV and to be in direct contact with the third connecting electrode CE3 during the fabrication of the display substrate, further reducing the voltage drop across the second electrode E2 during operation of the display substrate.

[0142] In some embodiments, the second length D2 is from 4 to 10 times of the first length D1. In one example, the second length D2 is approximately 5 μm , while the first length D1 is between 0.5 μm and 1.2 μm . The inventors of the present disclosure discover that these ranges

ensures that the second electrode E2 may extend inside the open groove GV to be in direct contact with at least one of the lower wall and the side wall of the open groove GV, increasing the contact area between the second electrode E2 and the first connecting electrode CE1, or between the second electrode E2 and the second connecting electrode CE2, further reducing the voltage drop across the extension path of the second electrode E2 during the operation of the display substrate.

[0143] In some embodiments, the third connecting electrode CE3 extends along a horizontal direction parallel to the surface direction of the base substrate BS for a third length D3. Optionally, the third length D3 is in a range between 12 μm and 14 μm .

[0144] In some embodiments, the first length D1 is 1 to 2 times of a height of the second connecting electrode CE2 in the second direction, the second direction being a vertical direction perpendicular to the horizontal direction. This may facilitate the process of making the display substrate by preventing too much material of the light-emitting layer EL from entering the open groove GV. The height of the second connecting electrode CE2 in the second direction is denoted as H in FIG. 9A and FIG. 9B. In some embodiments, the height H is between 0.5 μm and 0.6 μm , and a height d2 of the organic layer OL in the second direction is approximately 3200 Å. As shown in FIG. 9A and FIG. 9B, at least part of the organic layer OL in the sub-pixel area may extend beyond the pixel definition layer PDL to the auxiliary electrode connection area. Optionally, the height H of the second connecting electrode CE2 in the second direction is 1.5 to 2 times of the height d2 of the organic layer OL in the second direction.

[0145] FIG. 10A illustrates the structure of a portion of a display substrate in some embodiments according to the present disclosure. FIG. 10B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10C illustrates the structure of a semiconductor material layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10D illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10E illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10F illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10G illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10H illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10I illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10J illustrates the structure of a pixel definition layer in the portion of a display substrate depicted in FIG. 10A. FIG. 10K illustrates the structure of a black matrix layer in the portion of a display substrate depicted in FIG. 10A. Referring to FIG. 10A to FIG. 10K, the display substrate includes a subpixel region SR and an inter-subpixel region outside the subpixel region SR. Each individual subpixel

region corresponds to an individual subpixel. In the inter-subpixel region, the display substrate further includes a transparent region TR allowing a viewer to see through.

[0146] As shown in FIG. 10A to FIG. 10K, the auxiliary electrode AE in some embodiments extends at least partially in one or more subpixels. Optionally, the auxiliary electrode AE extends at least partially in a plurality of subpixels in a plurality of subpixel regions, as shown in FIG. 10A. FIG. 11A illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate depicted in FIG. 10A. Referring to FIG. 11A, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate at least partially overlaps with an orthographic projection of the auxiliary electrode AE on the base substrate. In the display substrate depicted in FIG. 10A to FIG. 10K, and FIG. 11A, the orthographic projection of the planarization layer PLN on a base substrate completely covers the orthographic projection of the auxiliary electrode AE on the base substrate.

[0147] FIG. 12A illustrates the structure of a planarization layer in the portion of a display substrate in some embodiments according to the present disclosure. FIG. 12B illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate in some embodiments according to the present disclosure. FIG. 13A illustrates the structure of a planarization layer in the portion of a display substrate in some embodiments according to the present disclosure. FIG. 13B illustrates the structure of a planarization layer and a signal line layer in the portion of a display substrate in some embodiments according to the present disclosure. Referring to FIG. 12A, FIG. 12B, FIG. 13A, and FIG. 13B, in some embodiments, the orthographic projection of the planarization layer PLN on a base substrate only partially overlaps with the orthographic projection of the auxiliary electrode AE on the base substrate.

[0148] FIG. 11B illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure. Referring to FIG. 11B, in some embodiments, the auxiliary electrode includes an auxiliary electrode line AEL extending along a first direction DR1 through a plurality of subpixels; and a branch line BL extending from the auxiliary electrode line AEL along a second direction DR2. The second direction DR2 is different from the first direction DR1.

[0149] Referring to FIG. 2, FIG. 4, FIG. 6, FIG. 10A to FIG. 10K, FIG. 11A, and FIG. 11B, in some embodiments, the first connecting electrode CE1 extends through a via to connect to the branch line BL. Optionally, an orthographic projection of the first connecting electrode CE1 on a base substrate BS partially overlaps with an orthographic projection of the branch line BL on the base substrate BS, and is non-overlapping with an orthographic projection of the auxiliary electrode line AEL on the base substrate BS.

[0150] In some embodiments, the auxiliary electrode further includes one or more auxiliary electrode blocks AEB in a layer different from the auxiliary electrode line AEL. In one

example, the one or more auxiliary electrode blocks AEB is in the gate layer, and the auxiliary electrode line AEL is in the signal line layer. FIG. 11C illustrates the structure of a gate layer and a signal line layer in the portion of a display substrate depicted in FIG. 10A. FIG. 11D illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure. Referring to FIG. 11C and FIG. 11D, the auxiliary electrode line AEL is connected to the one or more auxiliary electrode blocks AEB through one or more vias v1. Optionally, the one or more auxiliary electrode blocks AEB are arranged along the first direction DR1. Optionally, an orthographic projection of the auxiliary electrode line AEL on the base substrate at least partially overlaps with an orthographic projection of the one or more auxiliary electrode blocks AEB on the base substrate.

[0151] Referring to FIG. 2, FIG. 4, FIG. 6, and FIG. 11D, the display substrate in some embodiments includes an inter-layer dielectric layer ILD between the gate layer CT and the signal line layer SL. Optionally, the auxiliary electrode line AEL is on a side of the inter-layer dielectric layer ILD away from the one or more auxiliary electrode blocks AEB. Optionally, the auxiliary electrode line AEL is connected to the one or more auxiliary electrode blocks AEB through one or more vias v1 extending through the inter-layer dielectric layer ILD.

[0152] FIG. 11E illustrates the structure of a pixel definition layer and an auxiliary electrode in some embodiments according to the present disclosure. Referring to FIG. 11E, FIG. 2, FIG. 4, and FIG. 6, in some embodiments, an orthographic projection of the pixel definition layer PDL on a base substrate partially overlaps with an orthographic projection of the auxiliary electrode line AEL on the base substrate BS, and is non-overlapping with an orthographic projection of the first connecting electrode CE1 on the base substrate BS. Optionally, the orthographic projection of the pixel definition layer PDL on a base substrate partially overlaps with an orthographic projection of the one or more auxiliary electrode blocks AEB on the base substrate BS. Optionally, the orthographic projection of the pixel definition layer PDL on a base substrate is at least partially non-overlapping with an orthographic projection of the branch line on the base substrate BS.

[0153] FIG. 11F illustrates the structure of an auxiliary electrode in some embodiments according to the present disclosure. Referring to FIG. 11F, the auxiliary electrode includes an auxiliary electrode line AEL extending along a first direction DR1 through a plurality of subpixels; and a plurality of branch lines BLS extending from the auxiliary electrode line AEL along a second direction DR2, the second direction DR2 different from the first direction DR1. Optionally, the plurality of branch lines BLS includes a first branch line BL1 and multiple second branch lines BL2.

[0154] FIG. 11G illustrates the structure of an auxiliary electrode and a plurality of connecting structures in some embodiments according to the present disclosure. Referring to FIG. 11G, the display substrate in some embodiments includes a plurality of connecting

structures CSS, each of which electrically connecting the auxiliary electrode and the second electrode. Optionally, the plurality of connecting structures CSS includes a first connecting structure CS1 and multiple second connecting structures CS2. As shown in FIG. 11G, the first branch line BL1 connects the first connecting structure CS1 to the auxiliary electrode line AEL. The multiple second branch lines BL2 respectively connect the multiple second connecting structures CS2 to the auxiliary electrode line AEL. The first branch line BL1 extends along the second direction DR2 by a first length L1. The multiple second branch lines BL2 respectively extend along the second direction DR2 by multiple second lengths L2. The first length L1 is greater than each of the multiple second lengths L2.

[0155] FIG. 11H illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure. Referring to FIG. 11H, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate is completely non-overlapping with an orthographic projection of the first connecting structure CS1 on the base substrate. Optionally, the orthographic projection of the planarization layer PLN on the base substrate at least partially overlaps with orthographic projections of the multiple second connecting structures CS2 on the base substrate. In one example depicted in FIG. 11H, the orthographic projection of the planarization layer PLN on the base substrate covers the orthographic projections of the multiple second connecting structures CS2 on the base substrate.

[0156] FIG. 12C illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure. Referring to FIG. 12C, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate is completely non-overlapping with an orthographic projection of the first connecting structure CS1 on the base substrate, and is completely non-overlapping with orthographic projections of the multiple second connecting structures CS2 on the base substrate.

[0157] FIG. 13C illustrates the structure of a planarization layer, an auxiliary electrode, a plurality of connecting structures in some embodiments according to the present disclosure. Referring to FIG. 13C, in some embodiments, an orthographic projection of the planarization layer PLN on a base substrate is completely non-overlapping with an orthographic projection of the first connecting structure CS1 on the base substrate. Optionally, the orthographic projection of the planarization layer PLN on the base substrate only partially overlaps with orthographic projections of the multiple second connecting structures CS2 on the base substrate. In one example depicted in FIG. 13C, the orthographic projection of the planarization layer PLN on the base substrate only partially overlaps with each of the orthographic projections of the multiple second connecting structures CS2 on the base substrate.

[0158] Referring to FIG. 10G, the display substrate in some embodiments includes a repairing structure RPS. The repairing structure connects a first conductive part EC1 and a second conductive part EC2 together. In some embodiments, the first conductive part EC1 and the second conductive part EC2 are parts of a first electrode (e.g., the first electrode E1 depicted in FIG. 2). Optionally, the first conductive part EC1 and the second conductive part EC2 are parts of a first electrode in a same subpixel region (e.g., the subpixel region SR depicted in FIG. 1, FIG. 2, FIG. 4, and FIG. 10A). Optionally, the first electrode includes a plurality of sub-layers. For example, referring to FIG. 2 and FIG. 4, in some embodiments, the first electrode E1 includes a first sub-layer SUB1, a second sub-layer SUB2, and a third sub-layer SUB3 sequentially stacked. Optionally, the first conductive part EC1 and the second conductive part EC2 are parts of one sub-layer of the plurality of sub-layers of the first electrode. Referring to FIG. 10G, in some embodiments, the first conductive part EC1 and the second conductive part EC2 are parts of the first sub-layer SUB1 of the first electrode E1.

[0159] In some embodiments, the first conductive part EC1 and the second conductive part EC2 are at least partially (e.g., at least 50%, at least 60%, at least 70%, at least 80%, at least 90%, at least 95%, at least 99%, or 100%) on a first side S1 of a virtual straight line VL, and the repairing structure RPS is at least partially (e.g., at least 50%, at least 60%, at least 70%, at least 80%, at least 90%, at least 95%, at least 99%, or 100%) on a second side S2 of the virtual straight line VL. In one example, the first conductive part EC1 and the second conductive part EC2 are completely on the first side S1 of the virtual line VL, and the repairing structure RPS is completely on the second side S2 of the virtual straight line VL. Optionally, the virtual straight line VL is a border line separating the repairing structure RPS and the first conductive part EC1, and separating the repairing structure RPS and the second conductive part EC2.

[0160] FIG. 14A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure. FIG. 14B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 14A. FIG. 14H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 14A.

[0161] Referring to FIG. 14A to FIG. 14H, the repairing structure RPS in some embodiments includes a first portion P1, a second portion P2 connecting the first portion P1 with the first conductive part EC1, and a third portion P3 connecting the second portion P2 with the second

conductive part EC2. The first conductive part EC1 and the second conductive part EC2 are otherwise spaced apart from each other. As discussed above, in some embodiments, the first conductive part EC1 and the second conductive part EC2 are parts of a first electrode in a same subpixel region (e.g., the subpixel region SR depicted in FIG. 1, FIG. 2, FIG. 4, and FIG. 10A). When a defect occurs in the same subpixel region, it is necessary to repair to the display substrate. In one example, the defect is a bright spot defect, e.g., the same subpixel region in a black display mode is emitting light. In another example, the defect is a dark spot defect, e.g., the same subpixel region in a white display mode fails to emit light.

[0162] In one example, the first portion P1 extends along a first direction DR1. In another example, the second portion P2 extends along a second direction DR2. In another example, the third portion P3 extends along a second direction DR2.

[0163] In another aspect, the present disclosure provides a method of repairing a display substrate. The inventors of the present disclosure discover that the defect can be at least partially obviated by disconnecting the first conductive part EC1 from the first portion P1, or disconnecting the second conductive part EC2 from the first portion P1, or both.

[0164] In one example, the defect is a bright spot defect. By disconnecting the first conductive part EC1 from the first portion P1, or disconnecting the second conductive part EC2 from the first portion P1, only half of the same subpixel region is configured to function, at least partially obviating the bright spot issue. For example, if the bright spot defect is due to a short issue in a first sub-region of the same subpixel region having the first conductive part EC1, disconnecting the first conductive part EC1 from the first portion P1 electrically isolates the short in the first sub-region from a second sub-region of the same subpixel region having the second conductive part EC2. Subsequent to the repairing, the second sub-region of the same subpixel region having the second conductive part EC2 is configured to emit light normally. In another example, if the bright spot defect is due to a short issue in a second sub-region of the same subpixel region having the second conductive part EC2, disconnecting the second conductive part EC2 from the first portion P1 electrically isolates the short in the second sub-region from a first sub-region of the same subpixel region having the first conductive part EC1. Subsequent to the repairing, the first sub-region of the same subpixel region having the first conductive part EC1 is configured to emit light normally.

[0165] In another example, the defect is a dark spot defect. By disconnecting the first conductive part EC1 from the first portion P1, or disconnecting the second conductive part EC2 from the first portion P1, only half of the same subpixel region is configured to function, at least partially obviating the dark spot issue. For example, if the dark spot defect is due to an issue in a first sub-region of the same subpixel region having the first conductive part EC1, disconnecting the first conductive part EC1 from the first portion P1 electrically isolates the issue in the first sub-region from a second sub-region of the same subpixel region having the

second conductive part EC2. Subsequent to the repairing, the second sub-region of the same subpixel region having the second conductive part EC2 is configured to emit light normally. In another example, if the dark spot defect is due to an issue in a second sub-region of the same subpixel region having the second conductive part EC2, disconnecting the second conductive part EC2 from the first portion P1 electrically isolates the issue in the second sub-region from a first sub-region of the same subpixel region having the first conductive part EC1. Subsequent to the repairing, the first sub-region of the same subpixel region having the first conductive part EC1 is configured to emit light normally.

[0166] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the second portion P2. Optionally, disconnecting the first conductive part EC1 from the first portion P1 comprises cutting the second portion P2 using a laser.

[0167] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the third portion P3. Optionally, disconnecting the second conductive part EC2 from the first portion P1 comprises cutting the third portion P3 using a laser.

[0168] In some embodiments, the first electrode E1 is electrically connected to a drain electrode (e.g., D denoted in FIG. 2 or FIG. 4) of a transistor through the first portion P1. By cutting the second portion P2, the first conductive part EC1 is electrically disconnected from the drain electrode of the transistor, the second conductive part EC2 is still electrically connected to the drain electrode of the transistor. By cutting the third portion P3, the second conductive part EC2 is electrically disconnected from the drain electrode of the transistor, the first conductive part EC1 is still electrically connected to the drain electrode of the transistor.

[0169] In some embodiments, the first portion P1 includes a connecting portion DCP. In some embodiments, the first electrode E1 is electrically connected to a drain electrode (e.g., D denoted in FIG. 2 or FIG. 4) of a transistor through the connecting portion DCP.

[0170] In some embodiments, the first portion P1 is connected to the light shield LS. Optionally, the light shield LS is electrically connected to the drain electrode of the transistor (as shown in FIG. 2 or FIG. 4). Thus, the first portion P1 is electrically connected to the drain electrode of the transistor through the light shield LS.

[0171] In alternative embodiments, the first portion P1 is directly connected to the drain electrode of the transistor, as depicted in FIG. 2 or FIG. 4.

[0172] In some embodiments, the display substrate includes a first gap G1 spacing apart the first conductive part EC1 and the second conductive part EC2. In some embodiments, the display substrate includes a second gap G2 surrounded by the first portion P1, the second portion P2, the third portion P3, a portion of the first conductive part EC1, a portion of the

second conductive part EC2, and the first gap G1. Optionally, the first gap G1 is connected with the second gap G2.

[0173] In some embodiments, a first portion of the light shield LS is in a region having the first gap G1 spacing apart the first conductive part EC1 and the second conductive part EC2. In some embodiments, a second portion of the light shield LS is in a region having the second gap G2 surrounded by the first portion P1, the second portion P2, the third portion P3, a portion of the first conductive part EC1, a portion of the second conductive part EC2, and the first gap G1.

[0174] In some embodiments, an orthographic projection of the light shield LS on a base substrate partially overlaps with an orthographic projection of the first portion P1 on the base substrate. Optionally, an orthographic projection of the light shield LS on a base substrate partially overlaps with an orthographic projection of the first conductive part EC1 on the base substrate. Optionally, an orthographic projection of the light shield LS on a base substrate partially overlaps with an orthographic projection of the second conductive part EC2 on the base substrate.

[0175] In some embodiments, an orthographic projection of the light shield LS on a base substrate partially overlaps with an orthographic projection of the auxiliary electrode AE on the base substrate.

[0176] The inventors of the present disclosure discover that, in repairing the display substrate, the repairing structure RPS is typically at a position in close proximity to either a light shield LS or a planarization layer PLN (e.g., a resin layer), or both, making it difficult to determine a disconnecting point (e.g., a cutting point) that would not cause damage to the light shield LS or the planarization layer PLN. Similarly, additional care is necessary to determine a size of a laser beam for cutting the repairing structure RPS for the same consideration. Accordingly, the inventors of the present disclosure discover that various alternative implementations of the repairing structure RPS may be practiced to prevent these potential issues.

[0177] FIG. 15A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure. FIG. 15B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 15A. FIG. 15C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 15A. FIG. 15D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 15A. FIG. 15E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 15A. FIG. 15F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 15A. FIG. 15G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG.

15A. FIG. 15H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 15A.

[0178] Referring to FIG. 15A to FIG. 15H, the repairing structure RPS in some embodiments includes a first portion P1, a second portion P2 connecting the first portion P1 with the first conductive part EC1, and a third portion P3 connecting the second portion P2 with the second conductive part EC2. As compared to the repairing structure RPS depicted in FIG. 14A to FIG. 14H, the second portion P1 in the repairing structure RPS depicted in FIG. 15A to FIG. 15H is spaced apart further from the light shield LS, and the third portion P3 in the repairing structure RPS depicted in FIG. 15A to FIG. 15H is spaced apart further from the light shield LS.

[0179] In one example, the first portion P1 extends along a first direction DR1. In another example, the second portion P2 extends along a second direction DR2. In another example, the third portion P3 extends along a second direction DR2.

[0180] In some embodiments, the second portion P2 and the third portion P3 are spaced apart from each other by an average distance d . Optionally, the second portion P2 is spaced apart from the light shield LS by a first minimum distance $d1$, the third portion P3 is spaced apart from the light shield LS by a second minimum distance $d2$. Optionally, the second portion of the light shield LS in the region having the second gap G2 has an average line width lw . Optionally, the average distance d is substantially the same as a sum of the first minimum distance $d1$, the second minimum distance $d2$, and the average line width lw . As used herein, the term “substantially the same” refers to a difference between two values not exceeding 10% of a base value (e.g., one of the two values), e.g., not exceeding 8%, not exceeding 6%, not exceeding 4%, not exceeding 2%, not exceeding 1%, not exceeding 0.5%, not exceeding 0.1%, not exceeding 0.05%, and not exceeding 0.01%, of the base value.

[0181] In some embodiments, the first minimum distance $d1$ is at least 2 times (e.g., at least 2 times, at least 3 times, at least 4 times, at least 5 times, at least 6 times, at least 7 times, at least 8 times, at least 9 times, at least 10 times, at least 11 times, at least 12 times, at least 13 times, at least 14 times, at least 15 times, at least 16 times, at least 17 times, at least 18 times, at least 19 times, or at least 20 times) of the average line width lw .

[0182] In some embodiments, the second minimum distance $d2$ is at least 2 times (e.g., at least 2 times, at least 3 times, at least 4 times, at least 5 times, at least 6 times, at least 7 times, at least 8 times, at least 9 times, at least 10 times, at least 11 times, at least 12 times, at least 13 times, at least 14 times, at least 15 times, at least 16 times, at least 17 times, at least 18 times, at least 19 times, or at least 20 times) of the average line width lw .

[0183] In some embodiments, the average distance d is at least 4 times (e.g., at least 4 times, at least 6 times, at least 8 times, at least 10 times, at least 12 times, at least 14 times, at least 16 times, at least 18 times, at least 20 times, at least 22 times, at least 24 times, at least 26 times, at

least 28 times, at least 30 times, at least 32 times, at least 34 times, at least 36 times, at least 38 times, or at least 40 times) of the average line width lw .

[0184] The inventors of the present disclosure discover that, by spacing apart the first portion P1 from the light shield LS, and/or by spacing apart the second portion P2 from the light shield LS, potential issues of damaging the light shield LS during the process of repairing the display substrate can be prevented. For example, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 can be performed by cutting the first portion P1, e.g., at a position outside of the connecting portion DCP. Similarly, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 can be performed by cutting the first portion P1, e.g., at a position outside of the connecting portion DCP.

[0185] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the first portion P1, e.g., at a position outside of the connecting portion DCP. Optionally, disconnecting the first conductive part EC1 from the first portion P1 comprises cutting the first portion P1 using a laser.

[0186] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the first portion P1, e.g., at a position outside of the connecting portion DCP. Optionally, disconnecting the second conductive part EC2 from the first portion P1 comprises cutting the first portion P1 using a laser.

[0187] In some embodiments, the first electrode E1 is electrically connected to a drain electrode of a transistor through the first portion P1 (e.g., through the connecting portion DCP). By cutting the first portion P1, e.g., at a position A outside of the connecting portion DCP, the first conductive part EC1 is electrically disconnected from the drain electrode of the transistor, the second conductive part EC2 is still electrically connected to the drain electrode of the transistor. By cutting the first portion P1, e.g., at a position B outside of the connecting portion DCP, the second conductive part EC2 is electrically disconnected from the drain electrode of the transistor, the first conductive part EC1 is still electrically connected to the drain electrode of the transistor.

[0188] FIG. 16A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure. FIG. 16B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 16A. FIG. 16C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 16A. FIG. 16D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 16A. FIG. 16E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 16A. FIG. 16F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 16A. FIG. 16G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG.

16A. FIG. 16H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 16A.

[0189] Referring to FIG. 16A to FIG. 16H, the repairing structure RPS in some embodiments includes a first portion P1, a second portion P2 connecting the first portion P1 with the first conductive part EC1, and a third portion P3 connecting the second portion P2 with the second conductive part EC2.

[0190] Referring to FIG. 16A to FIG. 16H, in some embodiments, the repairing structure RPS includes a curved line portion. Optionally, at least the first portion P1 includes a curved line portion. Optionally, the first portion P1 includes two curved line portions. In one example, the first portion P1 includes a straight line portion in the middle and two curved line portions respectively connected to the straight line portion in the middle. As shown in FIG. 16A to FIG. 16H, the first portion P1 includes a straight line portion P1-1, a first curved line portion P1-2, and a second curved line portion P1-3. The straight line portion P1-1 connects the first curved line portion P1-2 with the second curved line portion P1-3. The first curved line portion P1-2 connects the straight line portion P1-1 with the second portion P2. The second curved line portion P1-3 connects the straight line portion P1-1 with the third portion P3. The first curved line portion P1-2 respectively curves away from the first conductive part EC1. The second curved line portion P1-3 curves away from the second conductive part EC2.

[0191] The inventors of the present disclosure discover that, by having the curved line portion in the repairing structure RPS, the repairing structure RPS can be further spaced apart from the planarization layer PLN (e.g., a resin layer). The potential issues of damaging the planarization layer PLN during the process of repairing the display substrate can be prevented.

[0192] For example, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 can be performed by cutting the first curved line portion P1-2. Similarly, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 can be performed by cutting the second curved line portion P1-3.

[0193] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the first portion P1, e.g., cutting the first curved line portion P1-2. Optionally, disconnecting the first conductive part EC1 from the first portion P1 comprises cutting the first curved line portion P1-2 using a laser.

[0194] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the first portion P1, e.g., cutting the second curved line portion P1-3. Optionally, disconnecting the second conductive part EC2 from the first portion P1 comprises cutting the second curved line portion P1-3 using a laser.

[0195] In some embodiments, the first electrode E1 is electrically connected to a drain electrode of a transistor through the first portion P1 (e.g., through the connecting portion DCP).

By cutting the first portion P1, e.g., at a position C outside of the connecting portion DCP, the first conductive part EC1 is electrically disconnected from the drain electrode of the transistor, the second conductive part EC2 is still electrically connected to the drain electrode of the transistor. By cutting the first portion P1, e.g., at a position D outside of the connecting portion DCP, the second conductive part EC2 is electrically disconnected from the drain electrode of the transistor, the first conductive part EC1 is still electrically connected to the drain electrode of the transistor.

[0196] FIG. 17A is a schematic diagram illustrating a portion of a display substrate in some embodiments according to the present disclosure. FIG. 17B illustrates the structure of a light shielding layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17C illustrates the structure of a gate layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17D illustrates the structure of a signal line layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17E illustrates the structure of a planarization layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17F illustrates the structure of a first conductive layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17G illustrates the structure of a second conductive layer in the portion of a display substrate depicted in FIG. 17A. FIG. 17H illustrates the structure of a third conductive layer in the portion of a display substrate depicted in FIG. 17A.

[0197] Referring to FIG. 17A to FIG. 17H, the repairing structure RPS in some embodiments includes a first portion P1, a second portion P2 connecting the first portion P1 with the first conductive part EC1, and a third portion P3 connecting the second portion P2 with the second conductive part EC2.

[0198] Referring to FIG. 17A to FIG. 17H, in some embodiments, the repairing structure RPS includes multiple straight line portions connected together. In some embodiments, the first portion P1 includes multiple straight line portions connected together. In one example, the first portion P1 includes a first straight line portion S1, a second straight line portion S2, a third straight line portion S3, a fourth straight line portion S4, and a fifth straight line portion S5. In another example, the first straight line portion S1, the third straight line portion S3, and the fifth straight line portion S5 respectively extend along a first direction DR1. In another example, the second straight line portion S2 and the fourth straight line portion S4 respectively extend along a second direction DR2. The second straight line portion S2 connects the first straight line portion S1 with the third straight line portion S3. The third straight line portion S3 connects the second straight line portion S2 with the second portion P2. The second portion P2 connects the third straight line portion S3 with the first conductive part EC1. The first straight line portion S1 connects the second straight line portion S2 with the fourth straight line portion S4. The fourth straight line portion S4 connects the first straight line portion S1 with the fifth straight line portion S5. The fifth straight line portion S5 connects the fourth straight line

portion S4 with the third portion P3. The third portion P3 connects the fifth straight line portion S5 with the second conductive part EC2.

[0199] The inventors of the present disclosure discover that, by having the multiple straight line portions in the repairing structure RPS, the repairing structure RPS can be further spaced apart from the planarization layer PLN (e.g., a resin layer). The potential issues of damaging the planarization layer PLN during the process of repairing the display substrate can be prevented. For example, the third straight line portion S3 is further spaced apart from the planarization layer PLN as compared to the first straight line portion S1, and the fifth straight line portion S5 is further spaced apart from the planarization layer PLN as compared to the first straight line portion S1. In the process of repairing the repairing structure RPS, a variety of suitable positions are available for cutting the repairing structure RPS. In one example, the repairing structure RPS may be cut at a position in the second portion P2 or the third portion P3 to avoid damaging the light shield LS. In another example, the repairing structure RPS may be cut at a position in the third straight line portion S3 or the fifth straight line portion S5 to avoid damaging the light shield LS and the planarization layer PLN.

[0200] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the second portion P2, e.g., using a laser.

[0201] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the third portion P3, e.g., using a laser.

[0202] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the second straight line portion S2, e.g., using a laser.

[0203] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the fourth straight line portion S4, e.g., using a laser.

[0204] In some embodiments, disconnecting the first conductive part EC1 from at least a portion of the first portion P1 comprises cutting the third straight line portion S3, e.g., using a laser.

[0205] In some embodiments, disconnecting the second conductive part EC2 from at least a portion of the first portion P1 comprises cutting the fifth straight line portion S5, e.g., using a laser.

[0206] In some embodiments, the first electrode E1 is electrically connected to a drain electrode of a transistor through the first portion P1 (e.g., through the connecting portion DCP). By cutting the first portion P1, e.g., at a position E outside of the connecting portion DCP, the first conductive part EC1 is electrically disconnected from the drain electrode of the transistor,

the second conductive part EC2 is still electrically connected to the drain electrode of the transistor. By cutting the first portion P1, e.g., at a position F outside of the connecting portion DCP, the second conductive part EC2 is electrically disconnected from the drain electrode of the transistor, the first conductive part EC1 is still electrically connected to the drain electrode of the transistor.

[0207] In another aspect, the present invention provides a display apparatus, including the display substrate described herein or fabricated by a method described herein, and one or more integrated circuits connected to the array substrate. Examples of appropriate display apparatuses include, but are not limited to, an electronic paper, a mobile phone, a tablet computer, a television, a monitor, a notebook computer, a digital album, a GPS, etc. Optionally, the display apparatus is an organic light emitting diode display apparatus. Optionally, the display apparatus is a liquid crystal display apparatus.

[0208] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. A display substrate, comprising:
a first conductive part;
a second conductive part; and
a repairing structure connecting the first conductive part with the second conductive part;
wherein the first conductive part and the second conductive part are parts of a first electrode;
the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line; and
the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side.
2. The display substrate of claim 1, wherein the first conductive part and the second conductive part are parts of a first electrode in a same subpixel region.
3. The display substrate of claim 1, wherein the first electrode comprises a plurality of sub-layers; and
the first conductive part and the second conductive part are parts of one sub-layer of the plurality of sub-layers of the first electrode.
4. The display substrate of any one of claims 1 to 3, wherein the first electrode is an anode of a light emitting element.
5. The display substrate of any one of claims 1 to 4, wherein the repairing structure comprises a first portion, a second portion connecting the first portion with the first conductive part, and a third portion connecting the second portion with the second conductive part; and
the first conductive part and the second conductive part are otherwise spaced apart from each other.
6. The display substrate of claim 5, wherein the first electrode is electrically connected to a drain electrode of a transistor through the first portion.
7. The display substrate of claim 5, further comprising a light shield in a light shield layer on a side of the first conductive part, the second conductive part, and the repairing structure closer to a base substrate;
wherein the first portion is connected to the light shield;
the light shield is electrically connected to a drain electrode of a transistor;

the first portion is electrically connected to the drain electrode of the transistor through the light shield.

8. The display substrate of claim 5, wherein the first portion is directly connected to a drain electrode of a transistor.

9. The display substrate of claim 5, wherein the first portion extends along a first direction;

the second portion extends along a second direction; and

the third portion extends along a second direction.

10. The display substrate of any one of claims 5 to 9, further comprising: a first gap spacing apart the first conductive part and the second conductive part; and

a second gap surrounded by the first portion, the second portion, the third portion, a portion of the first conductive part, a portion of the second conductive part, and the first gap;

wherein the first gap is connected with the second gap.

11. The display substrate of claim 10, wherein a first portion of a light shield is in a region having the first gap; and

a second portion of the light shield is in a region having the second gap.

12. The display substrate of claim 11, wherein an orthographic projection of the light shield on a base substrate partially overlaps with an orthographic projection of the first portion on the base substrate.

13. The display substrate of claim 11, wherein the second portion is spaced apart from the light shield by a first minimum distance;

the third portion is spaced apart from the light shield by a second minimum distance;

the second portion of the light shield have an average line width;

the first minimum distance is at least 2 times of the average line width; and

the second minimum distance is at least 2 times of the average line width.

14. The display substrate of any one of claims 5 to 8, wherein at least the first portion comprises a curved line portion.

15. The display substrate of claim 14, wherein the first portion comprises a straight line portion, a first curved line portion, and a second curved line portion;

the straight line portion connects the first curved line portion with the second curved line portion;

the first curved line portion connects the straight line portion with the second portion; and

the second curved line portion connects the straight line portion with the third portion.

16. The display substrate of any one of claims 5 to 8, wherein at least the first portion comprises multiple straight line portions connected together.

17. The display substrate of claim 16, wherein the first portion comprises a first straight line portion, a second straight line portion, a third straight line portion, a fourth straight line portion, and a fifth straight line portion;

the second straight line portion connects the first straight line portion with the third straight line portion;

the third straight line portion connects the second straight line portion with the second portion;

the second portion connects the third straight line portion with the first conductive part;

the first straight line portion connects the second straight line portion with the fourth straight line portion;

the fourth straight line portion connects the first straight line portion with the fifth straight line portion;

the fifth straight line portion connects the fourth straight line portion with the third portion; and

the third portion connects the fifth straight line portion with the second conductive part.

18. The display substrate of claim 17, wherein the first straight line portion, the third straight line portion, and the fifth straight line portion respectively extend along a first direction; and

the second straight line portion and the fourth straight line portion respectively extend along a second direction.

19. A display apparatus, comprising the display substrate of any one of claims 1 to 18, and one or more integrated circuits connected to the display substrate.

20. A method of repairing a display substrate:
wherein the display substrate includes:

a first conductive part;
a second conductive part; and
a repairing structure connecting the first conductive part with the second conductive part;
wherein the first conductive part and the second conductive part are parts of a first electrode;
the first conductive part and the second conductive part are at least partially on a first side of a virtual straight line;
the repairing structure is at least partially on a second side of the virtual straight line, the second side opposite to the first side; and
the repairing structure comprises a first portion, a second portion connecting the first portion with the first conductive part, and a third portion connecting the second portion with the second conductive part;
wherein the method comprises:
disconnecting the first conductive part from at least a portion of the first portion, or disconnecting the second conductive part from at least a portion of the first portion.

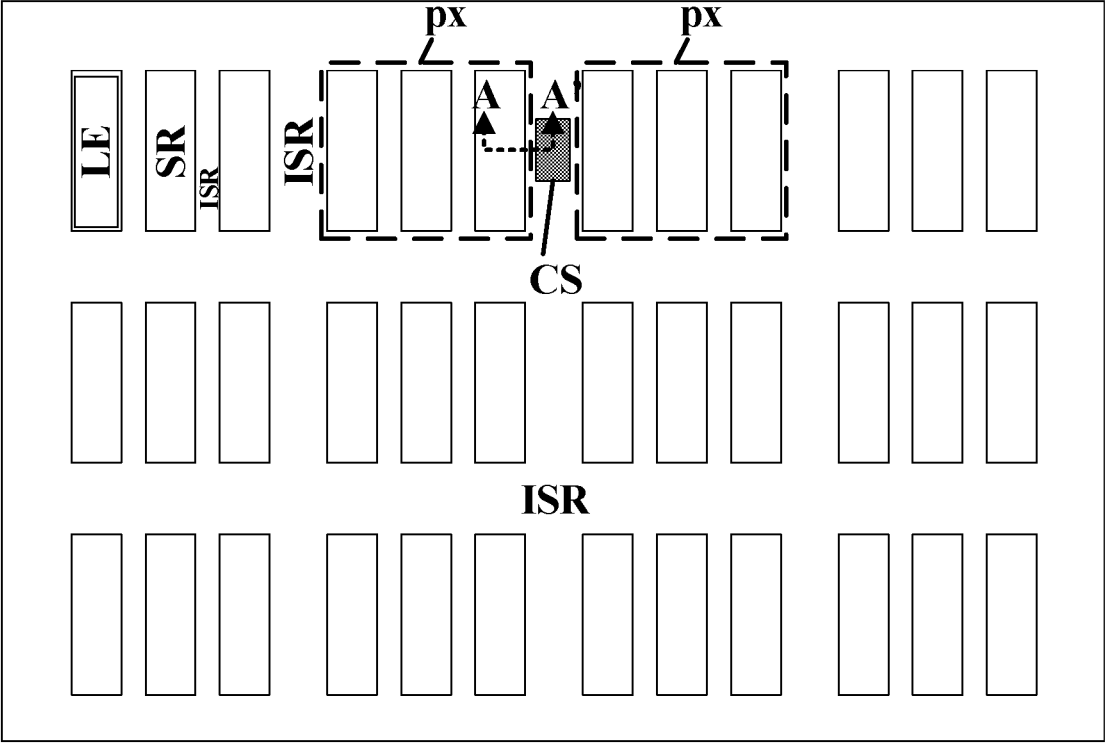


FIG. 1

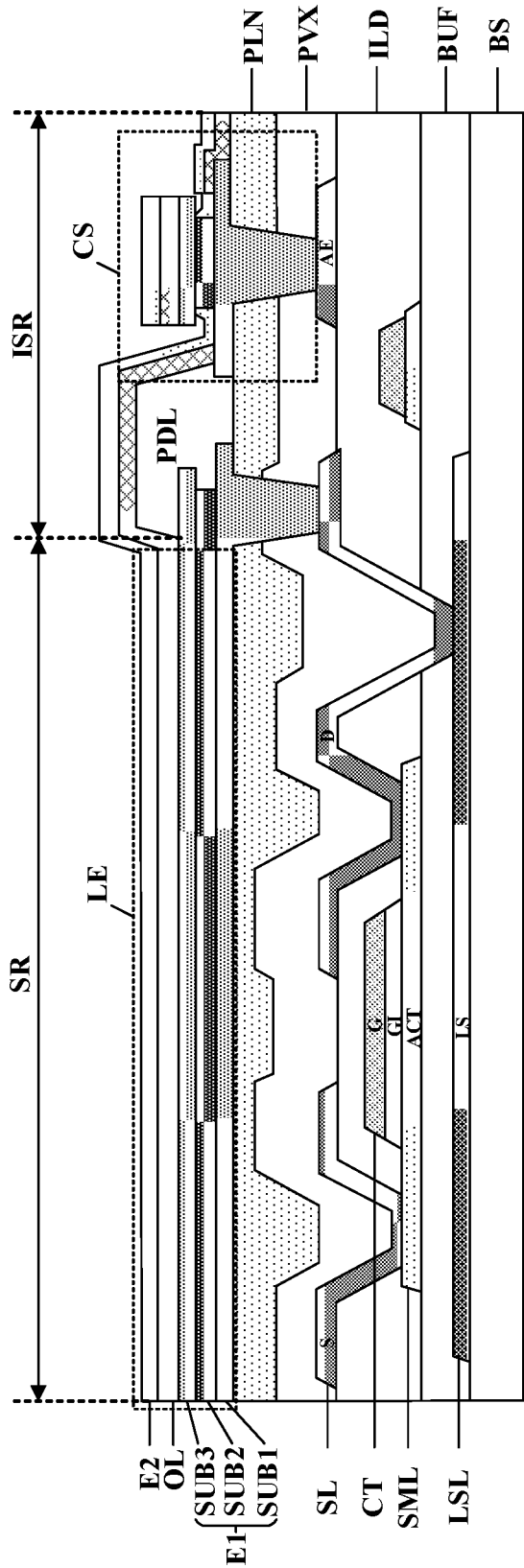


FIG. 2

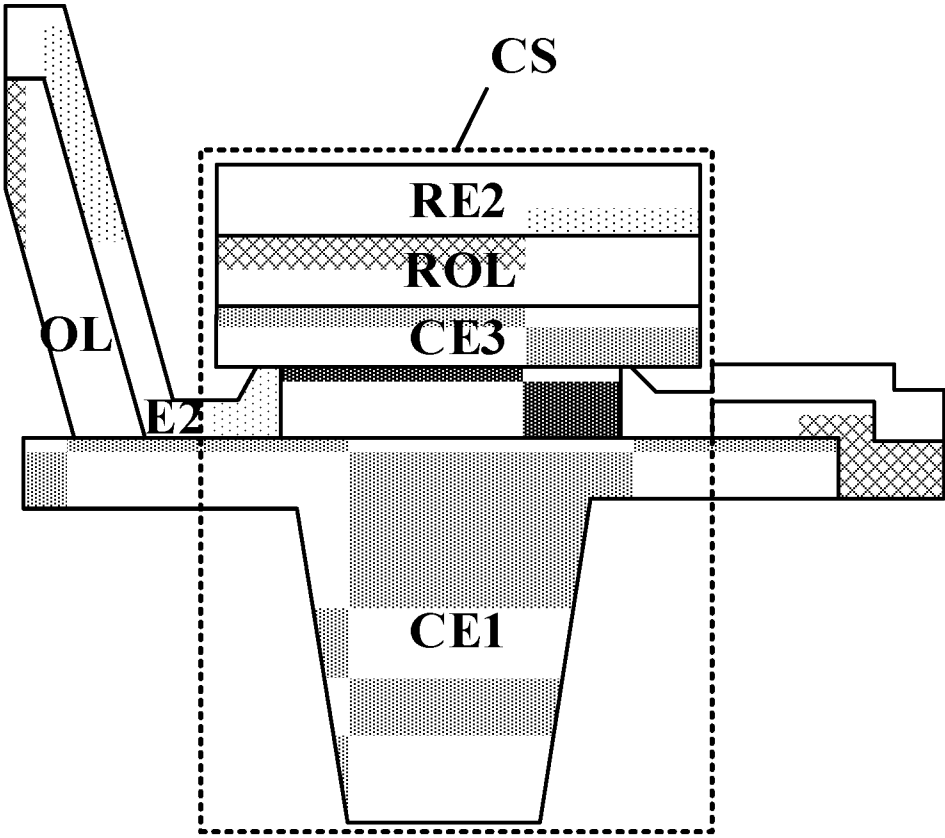


FIG. 3

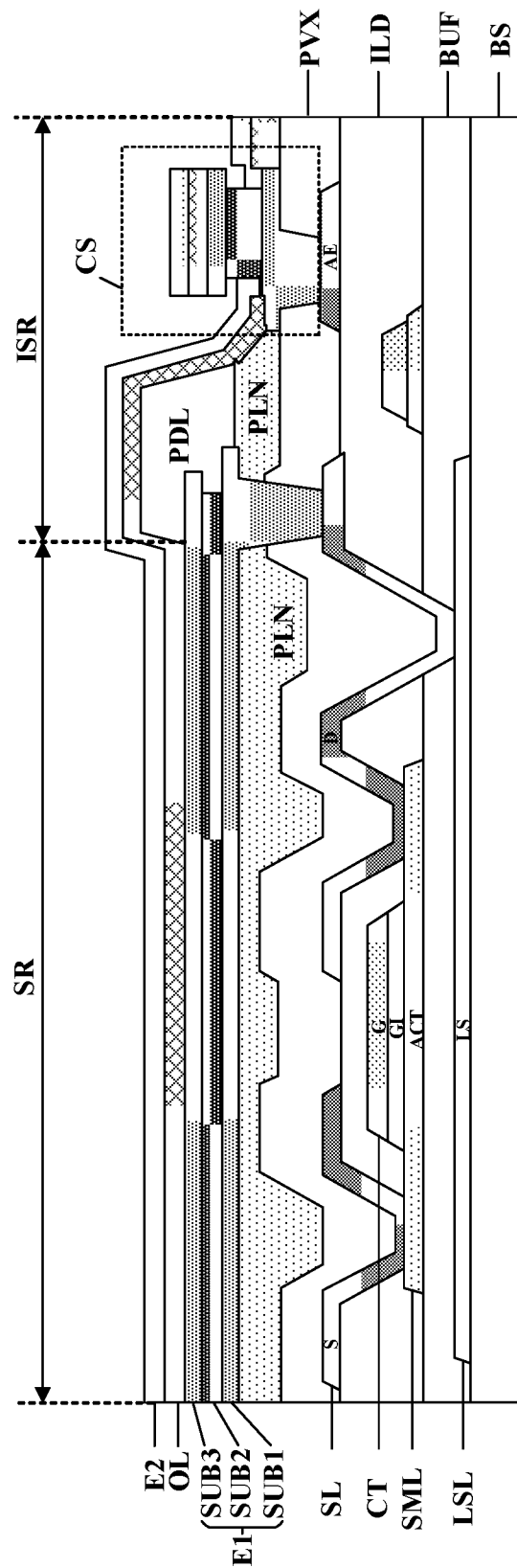


FIG. 4

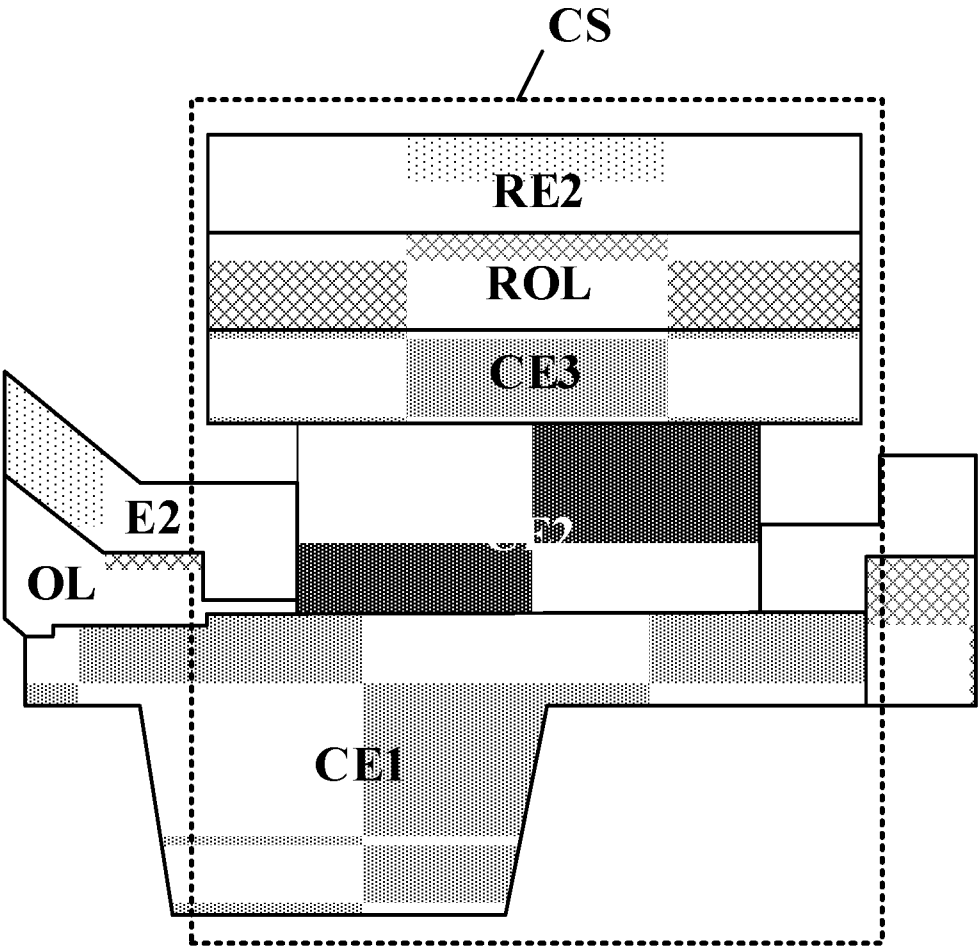


FIG. 5

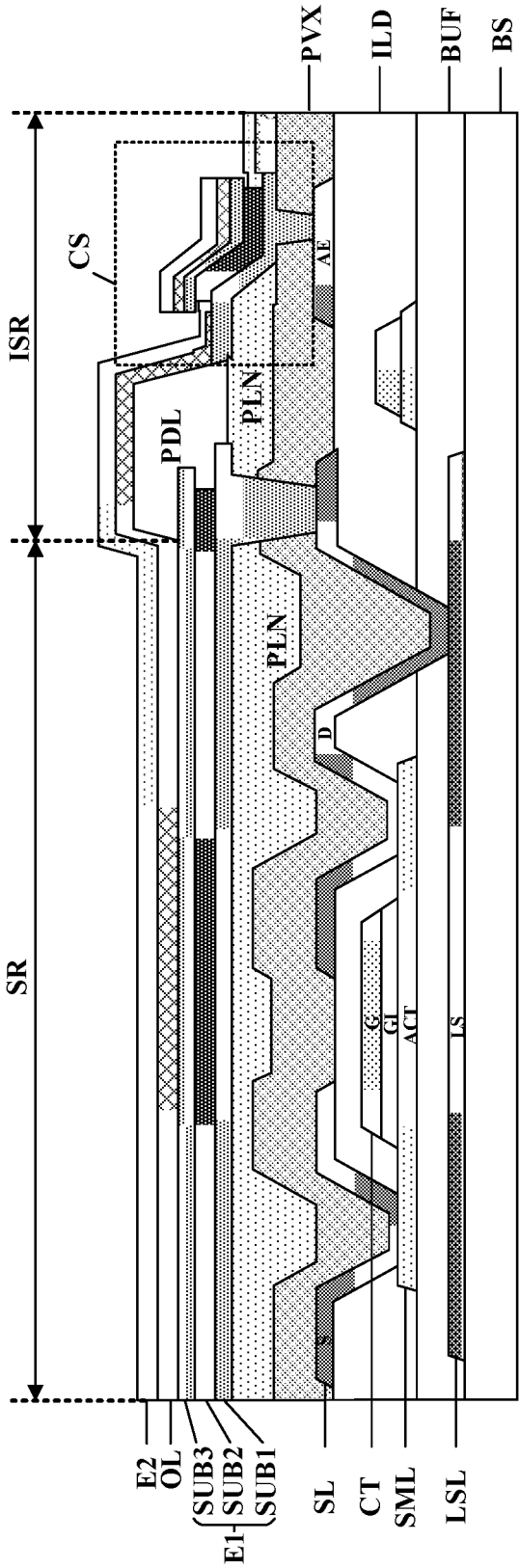


FIG. 6

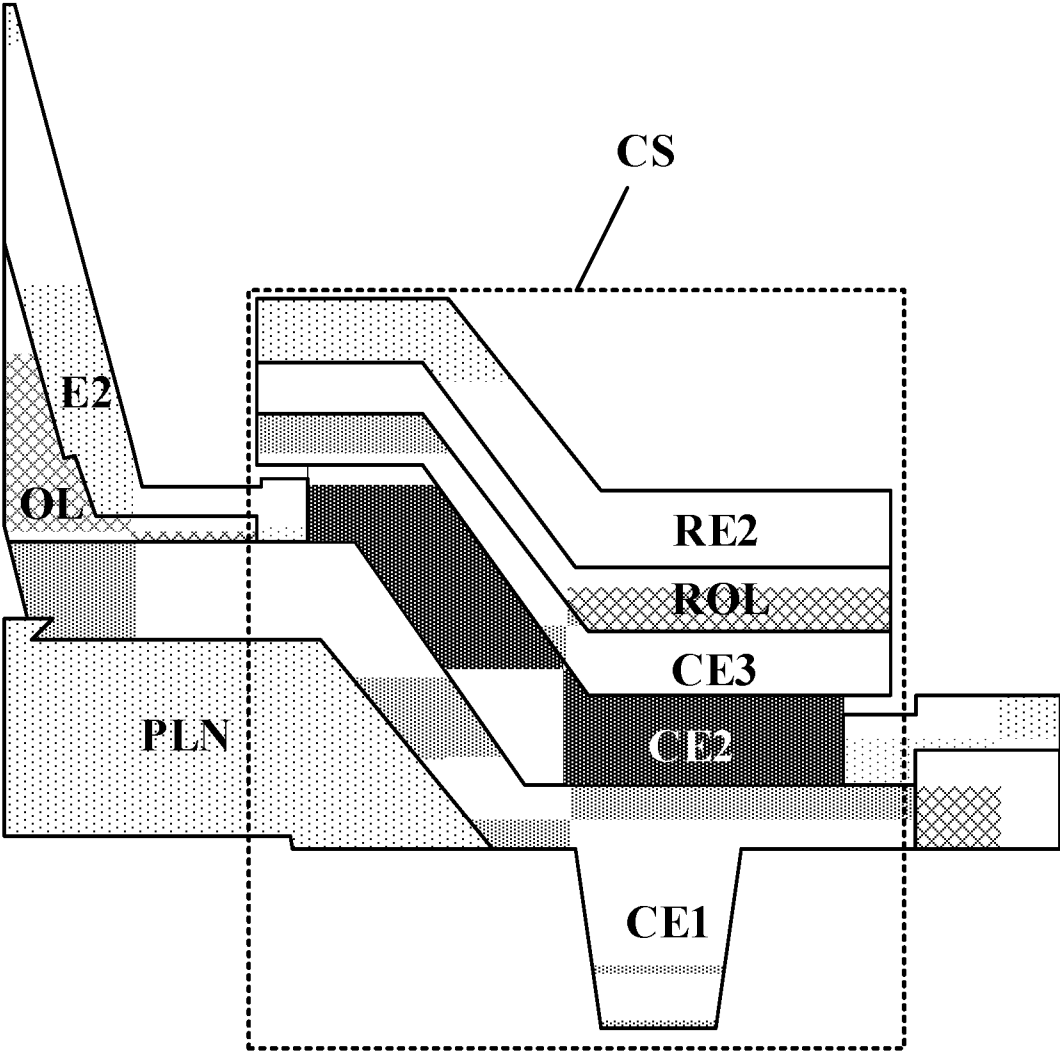


FIG. 7

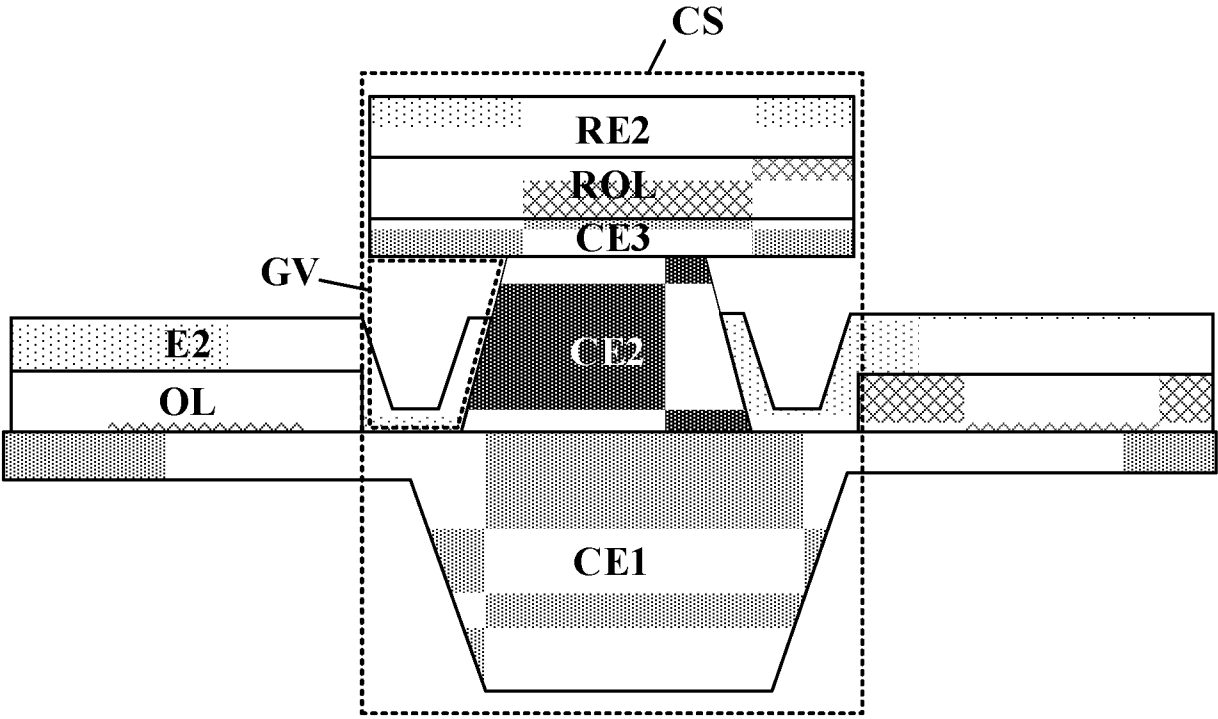


FIG. 8

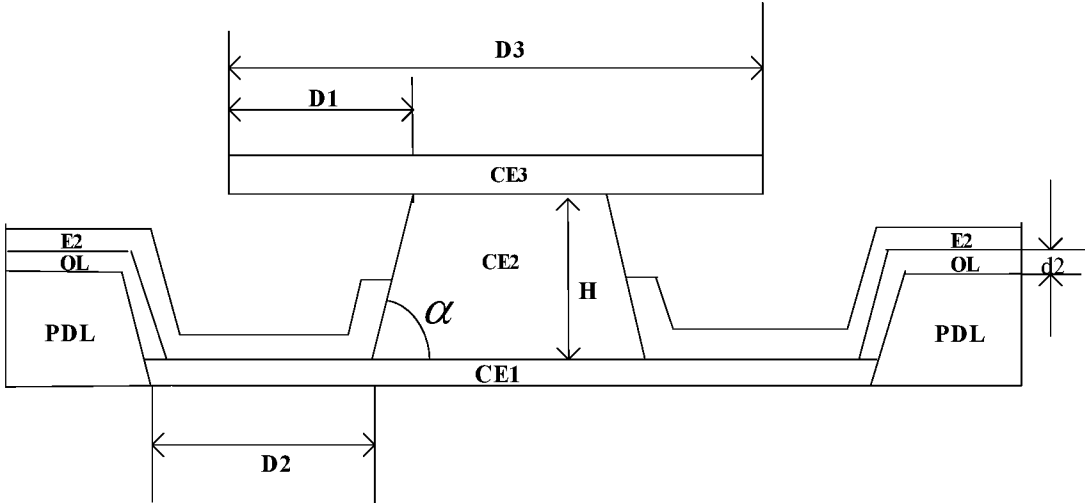


FIG. 9A

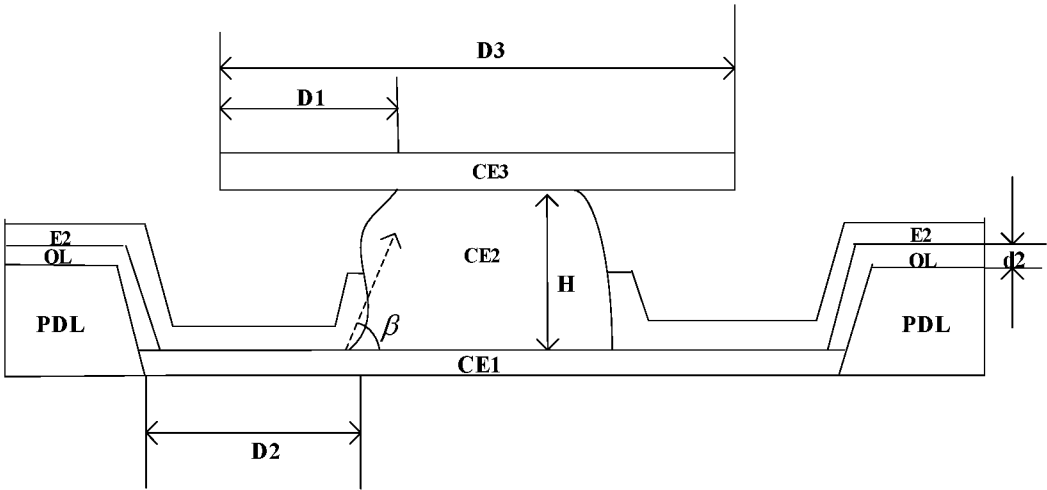


FIG. 9B

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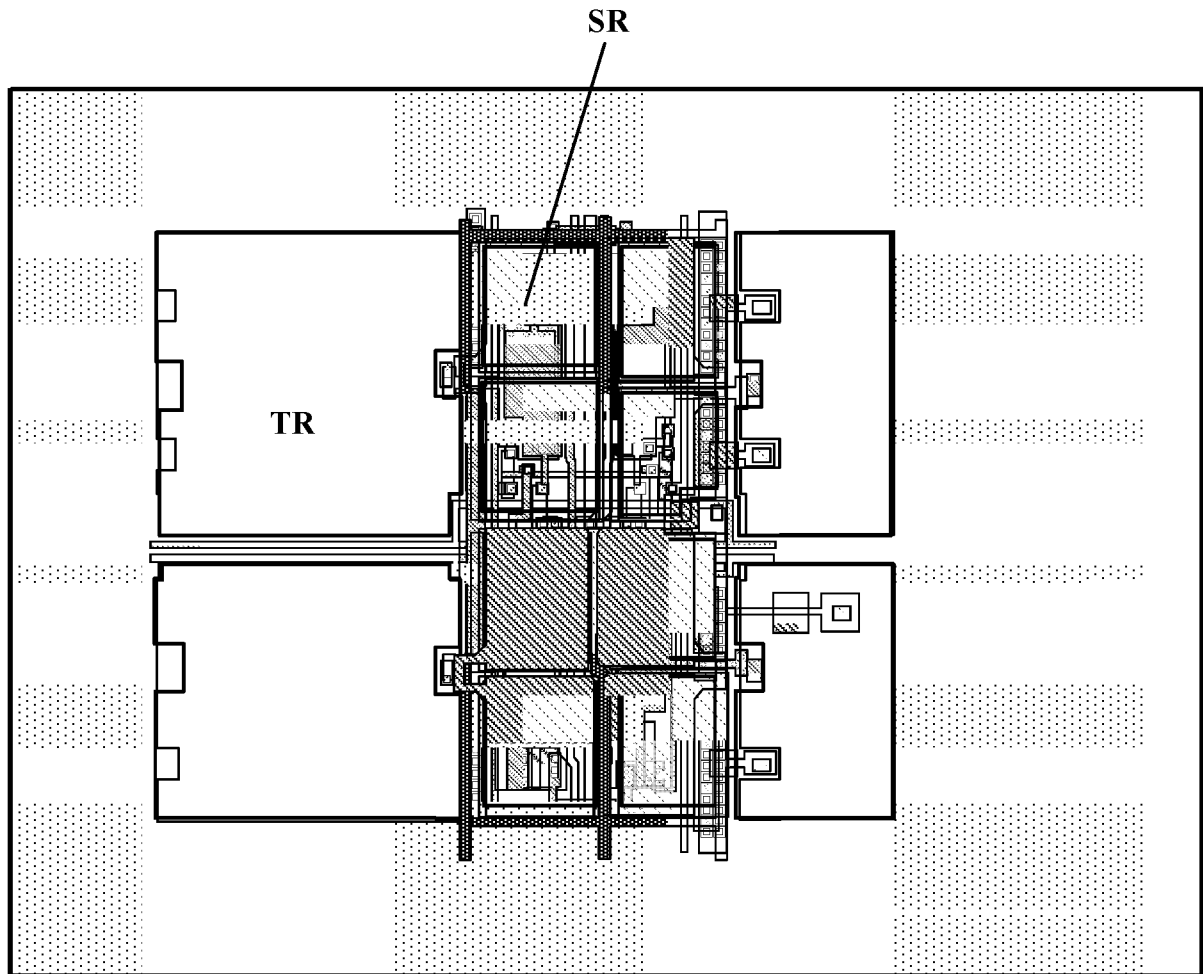


FIG. 10A

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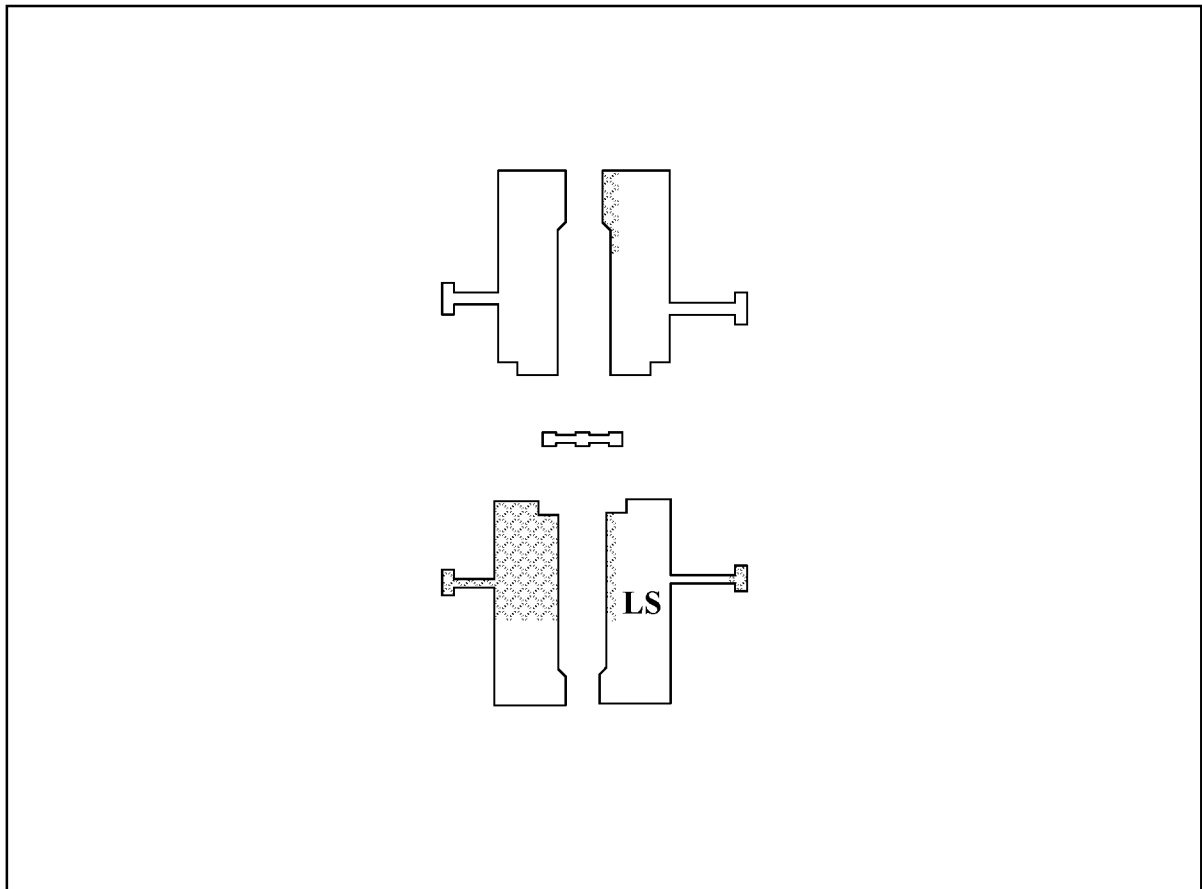


FIG. 10B

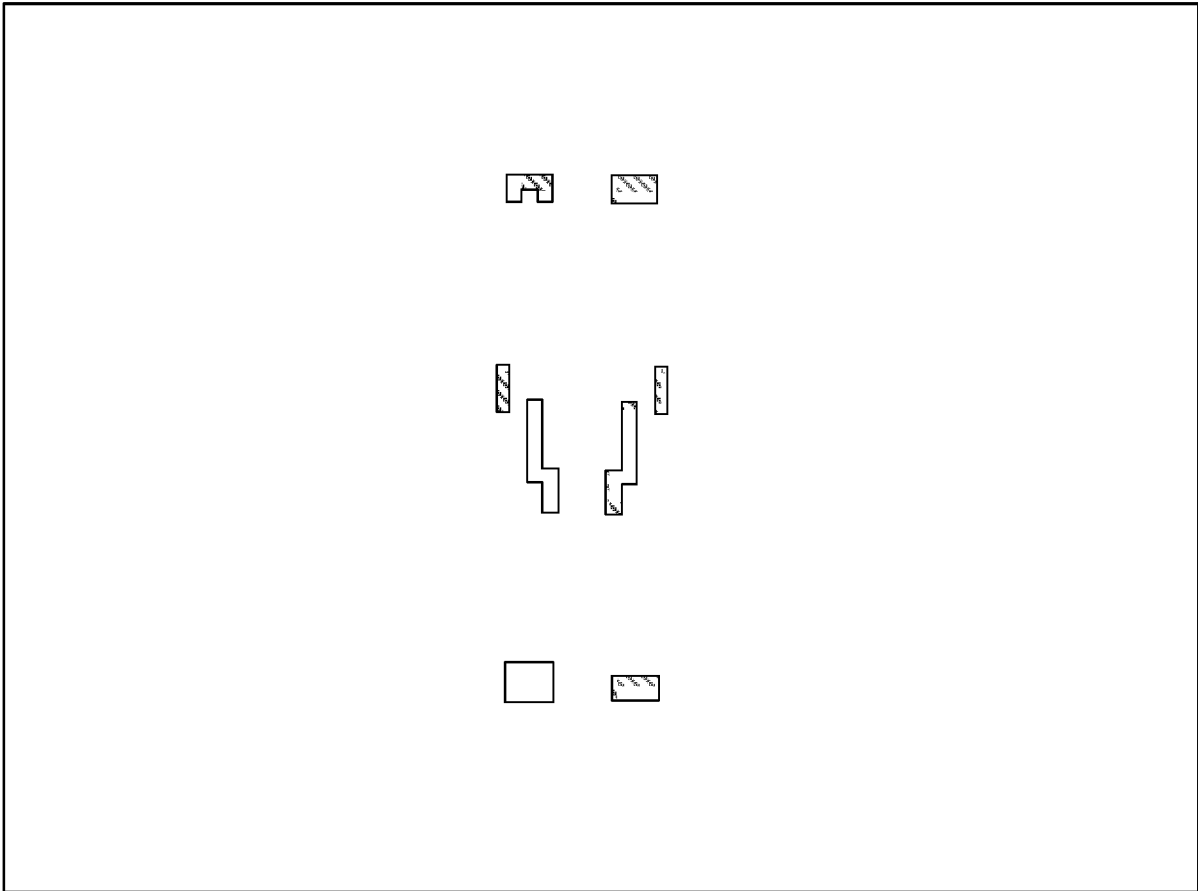


FIG. 10C

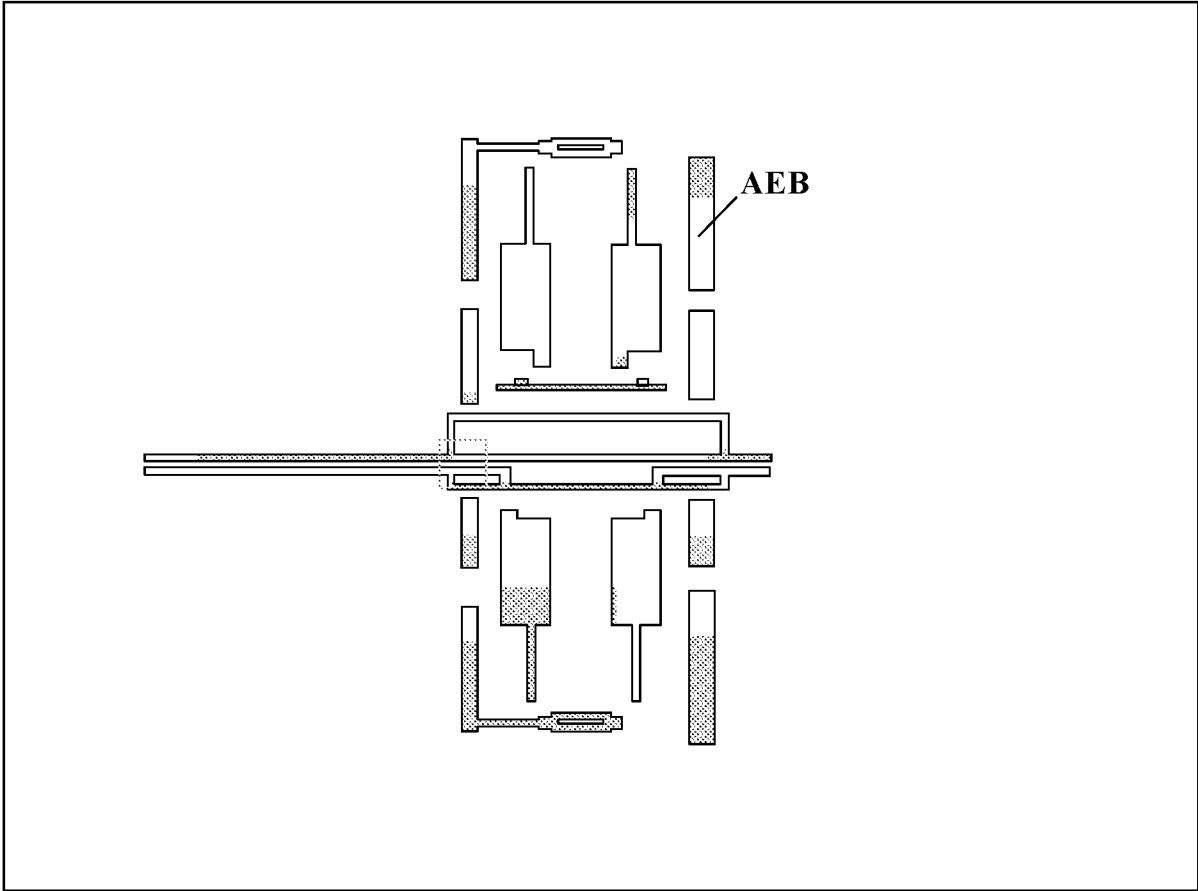


FIG. 10D

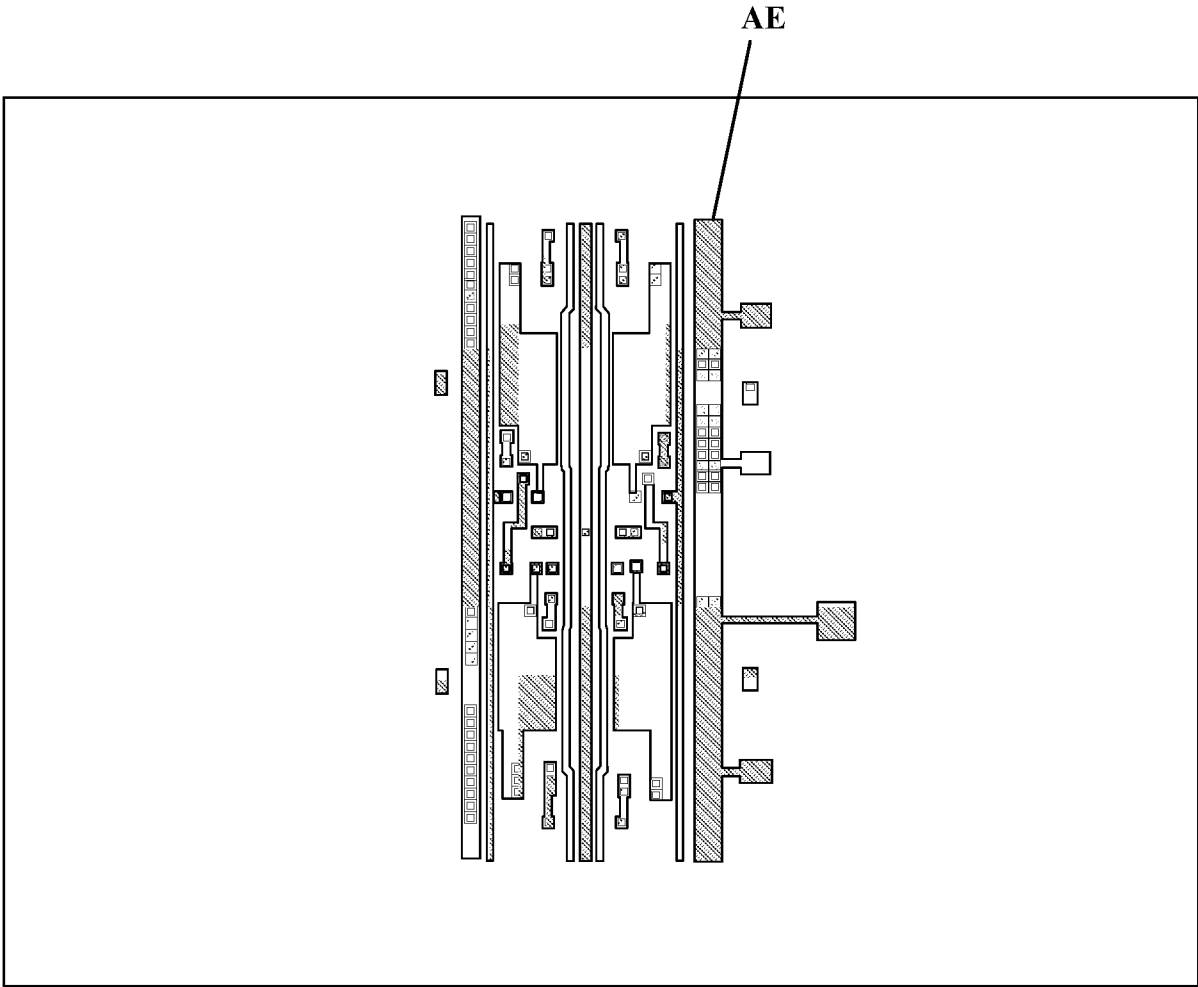


FIG. 10E

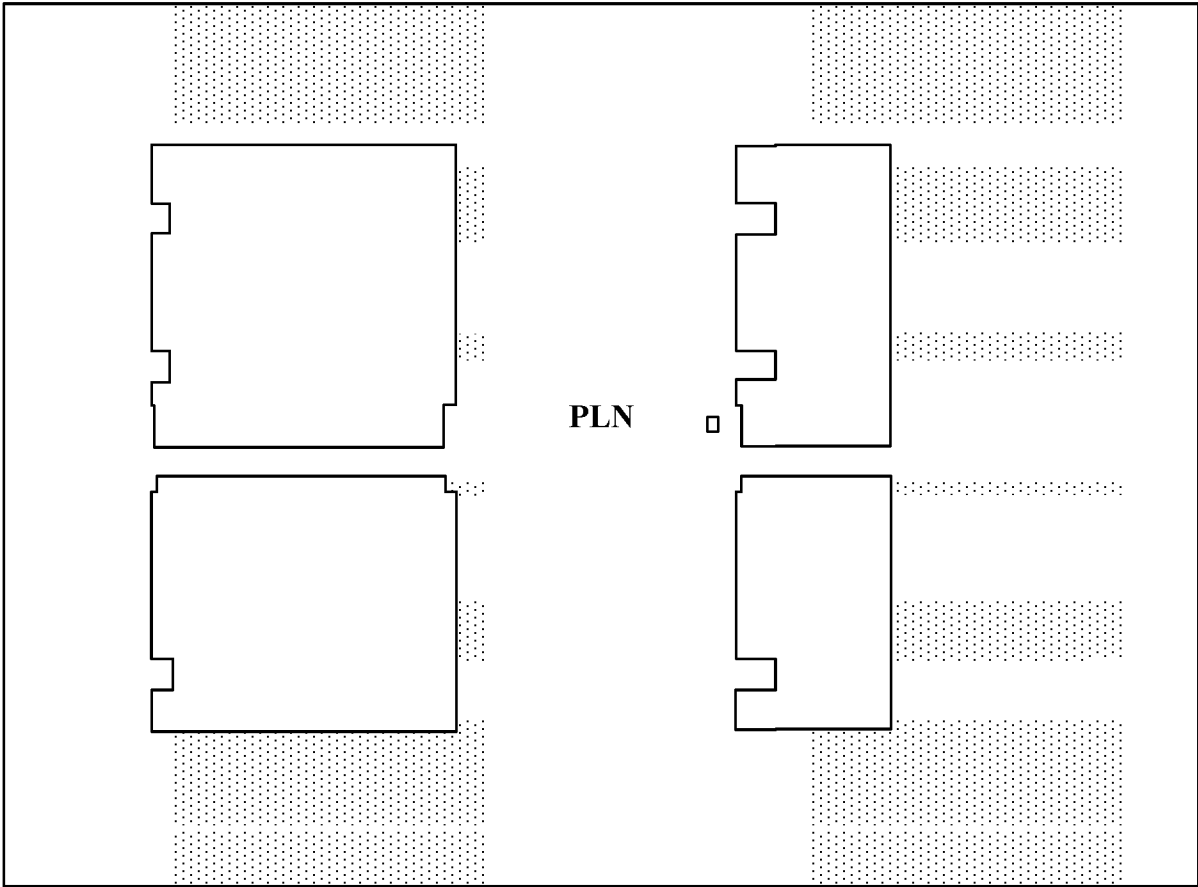


FIG. 10F

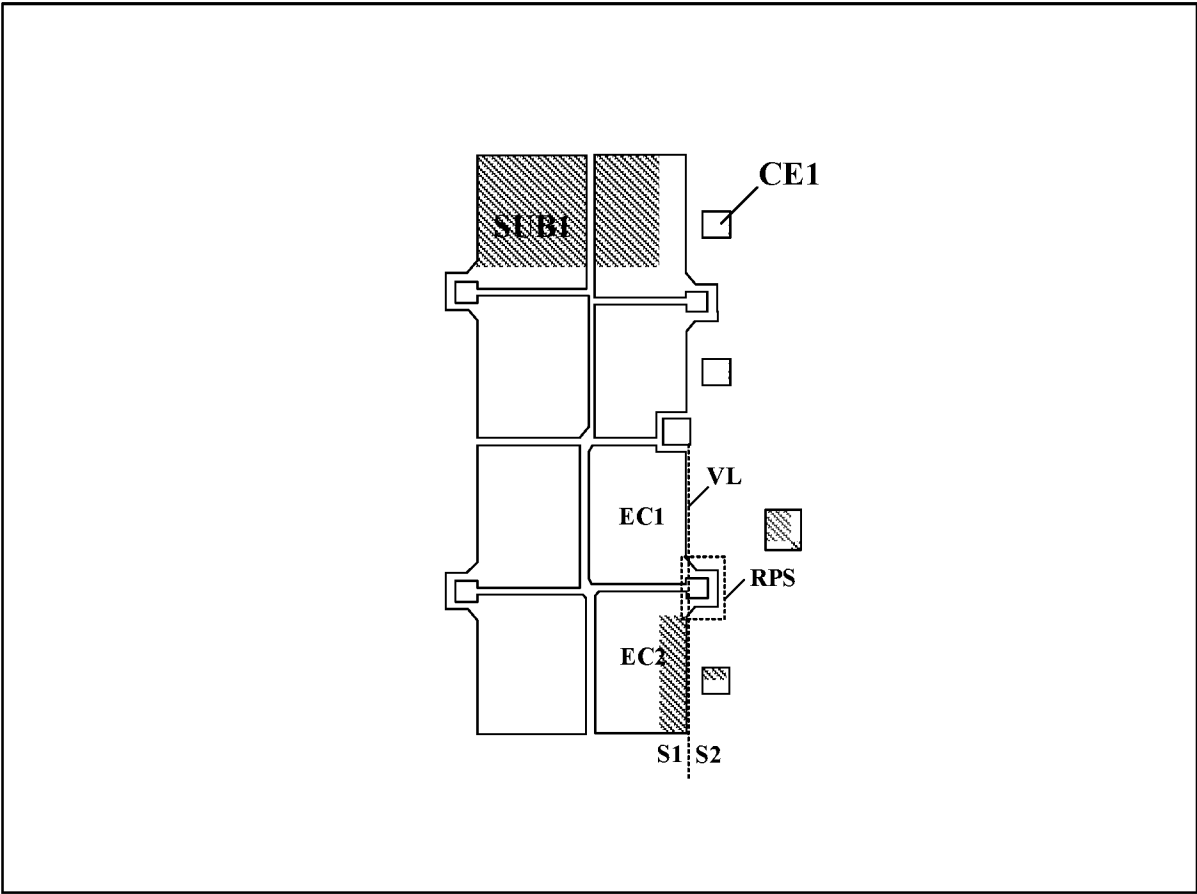


FIG. 10G

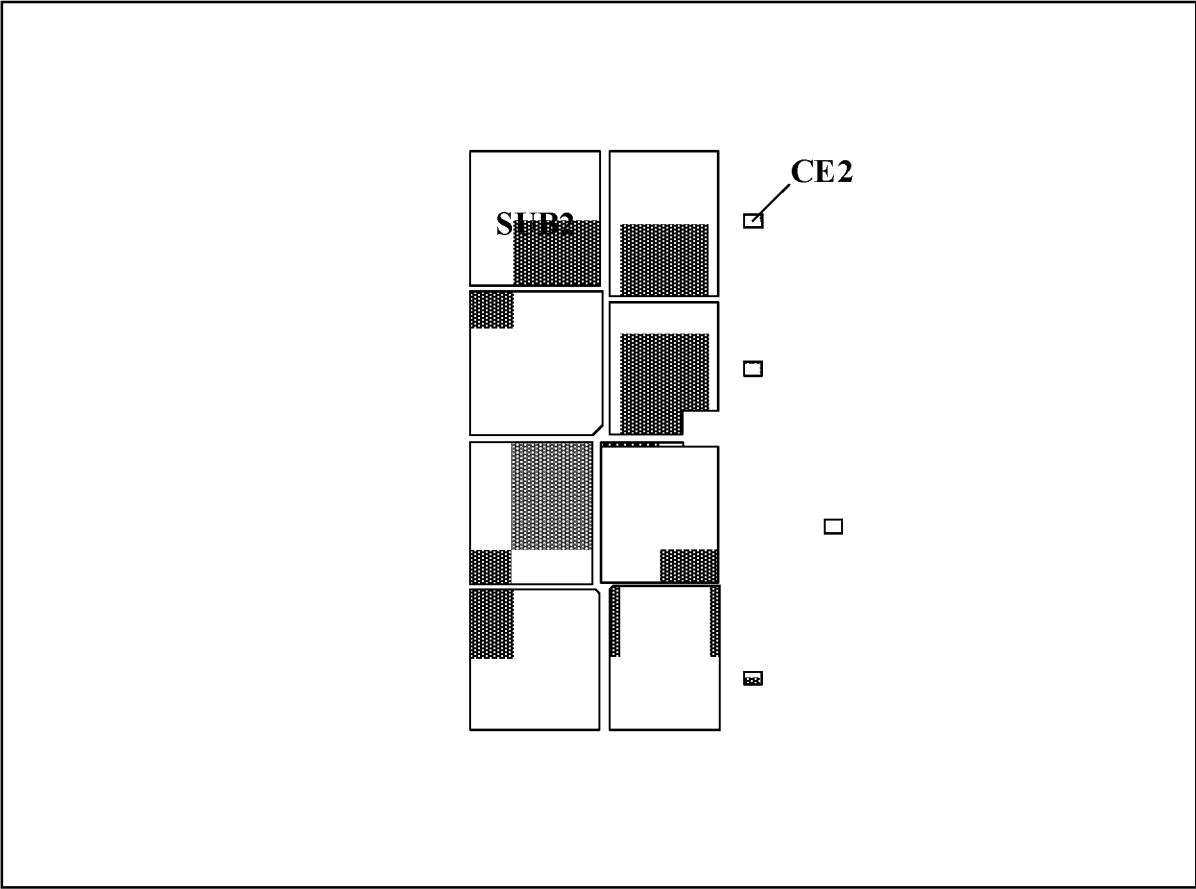


FIG. 10H

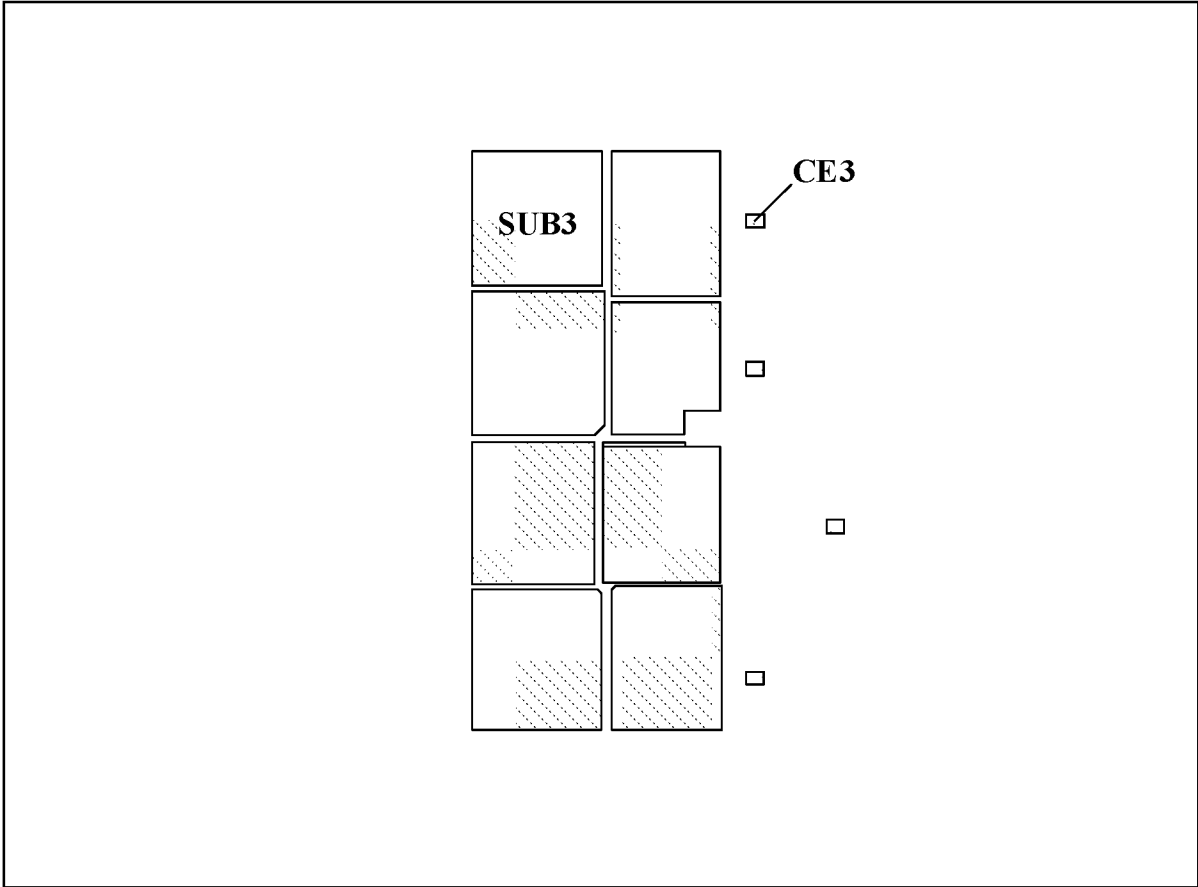
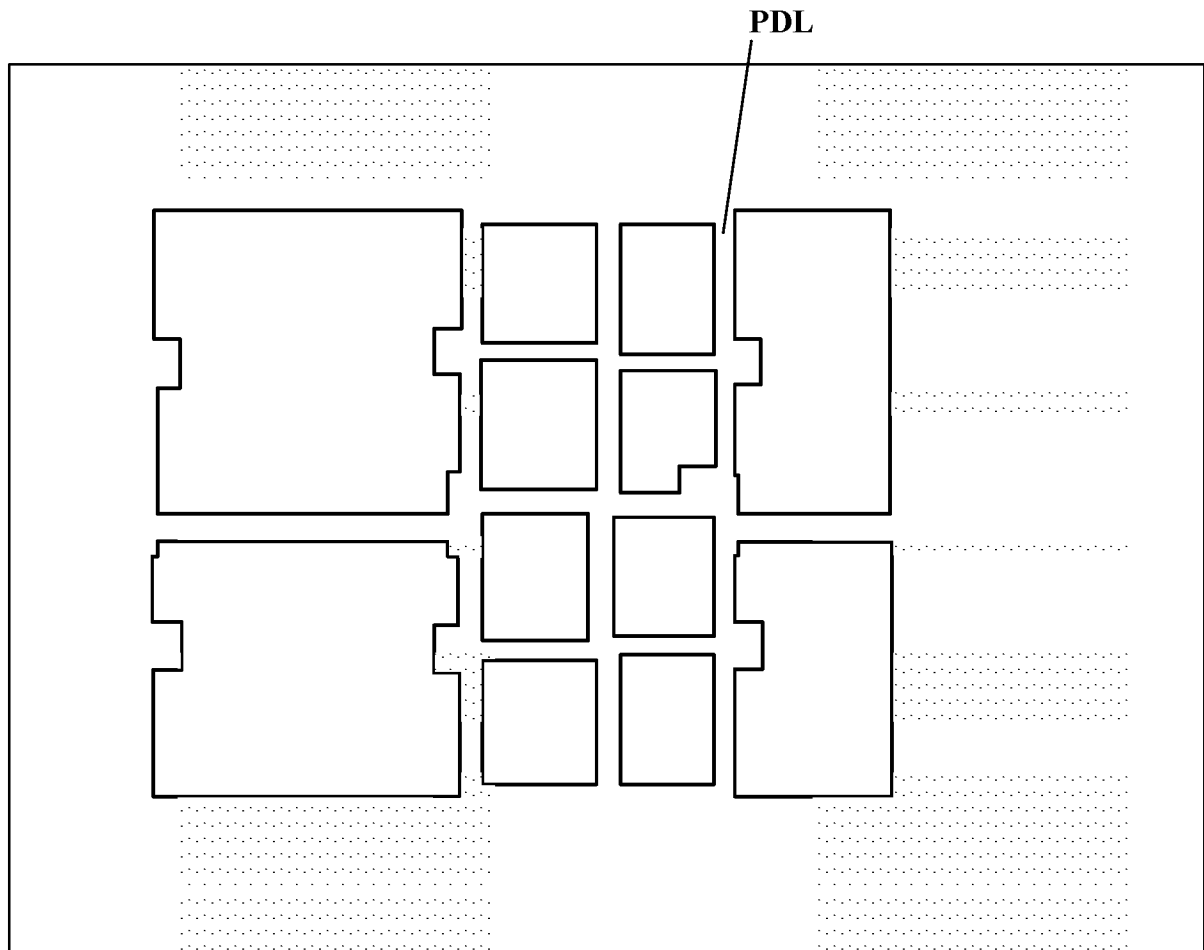


FIG. 10I

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**FIG. 10J**

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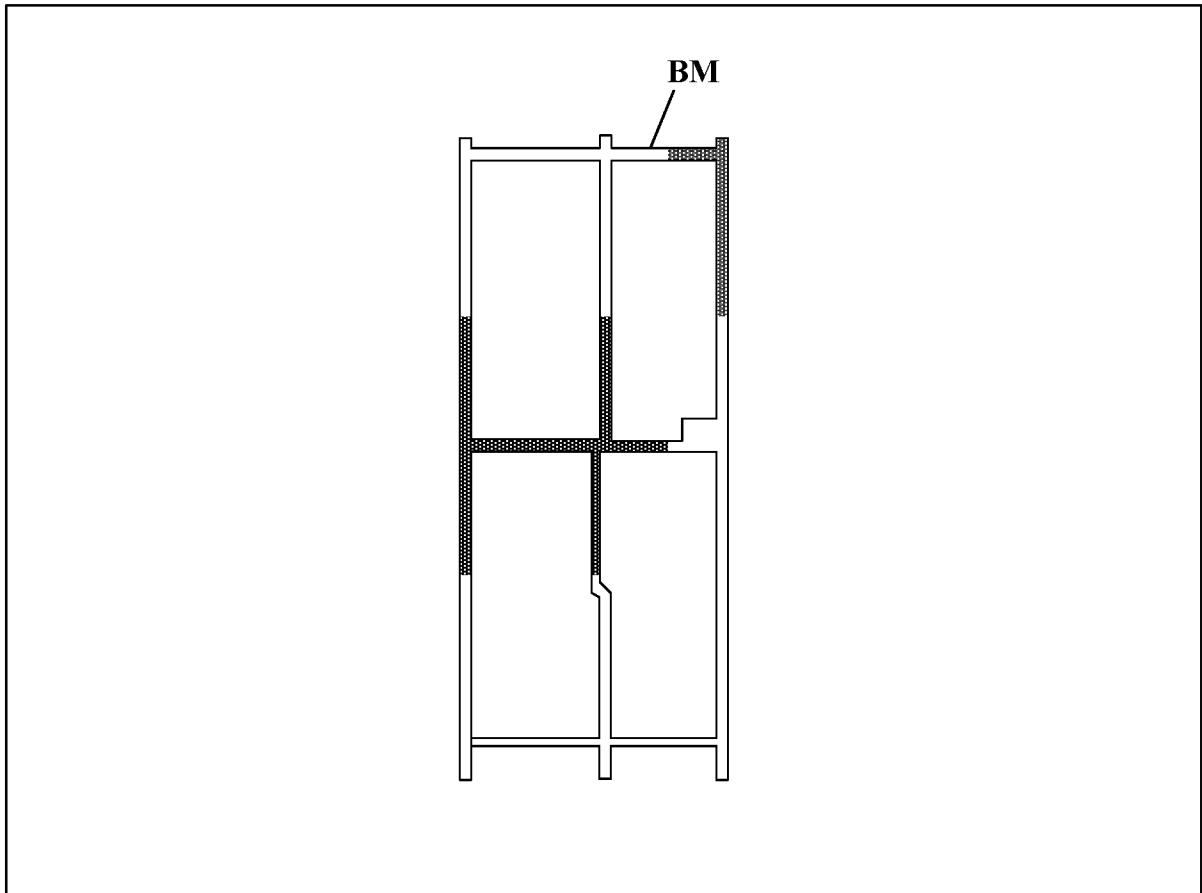


FIG. 10K

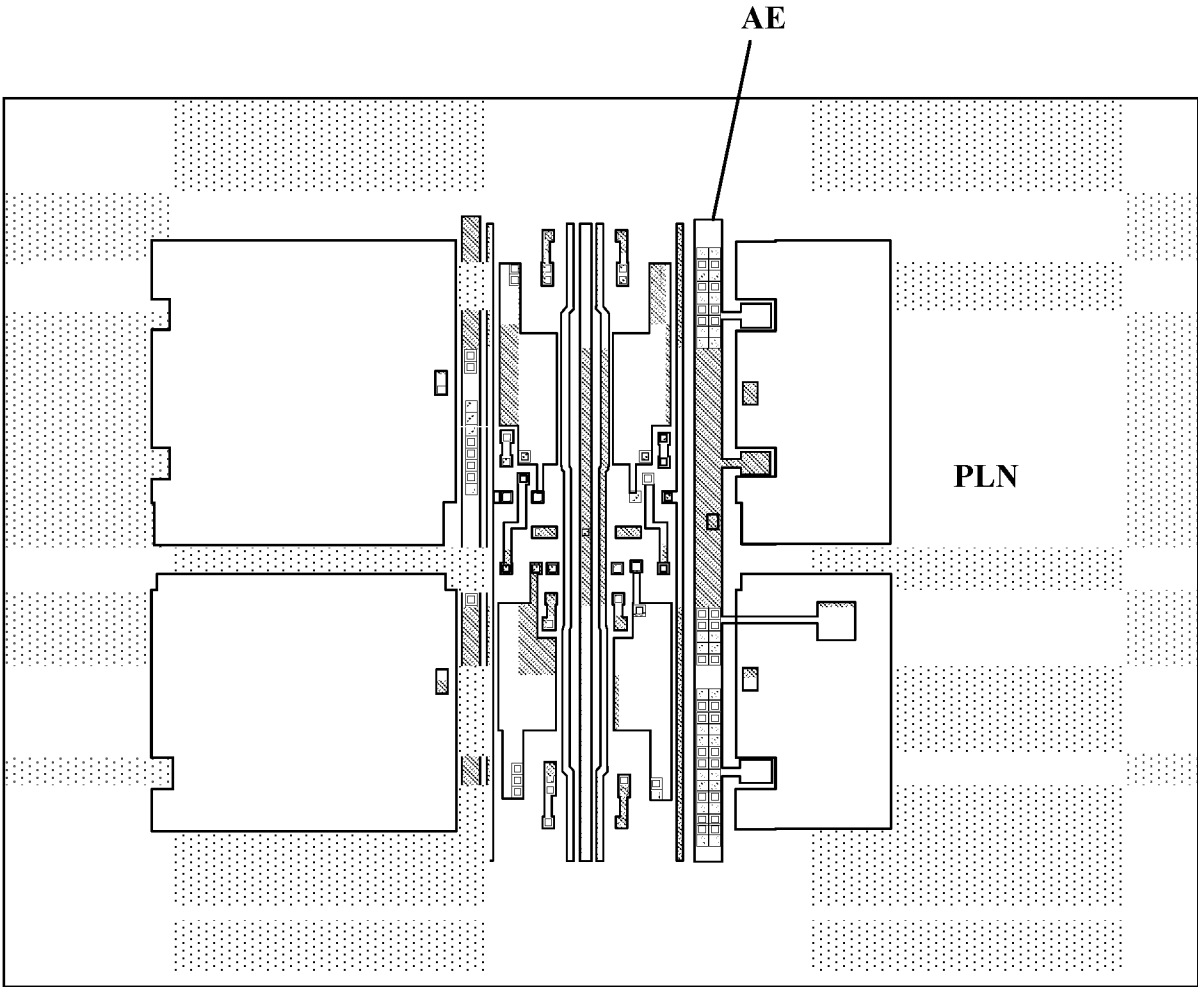


FIG. 11A

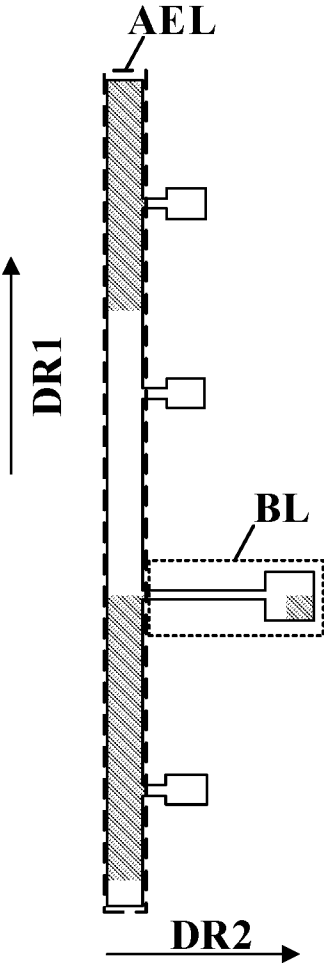


FIG. 11B

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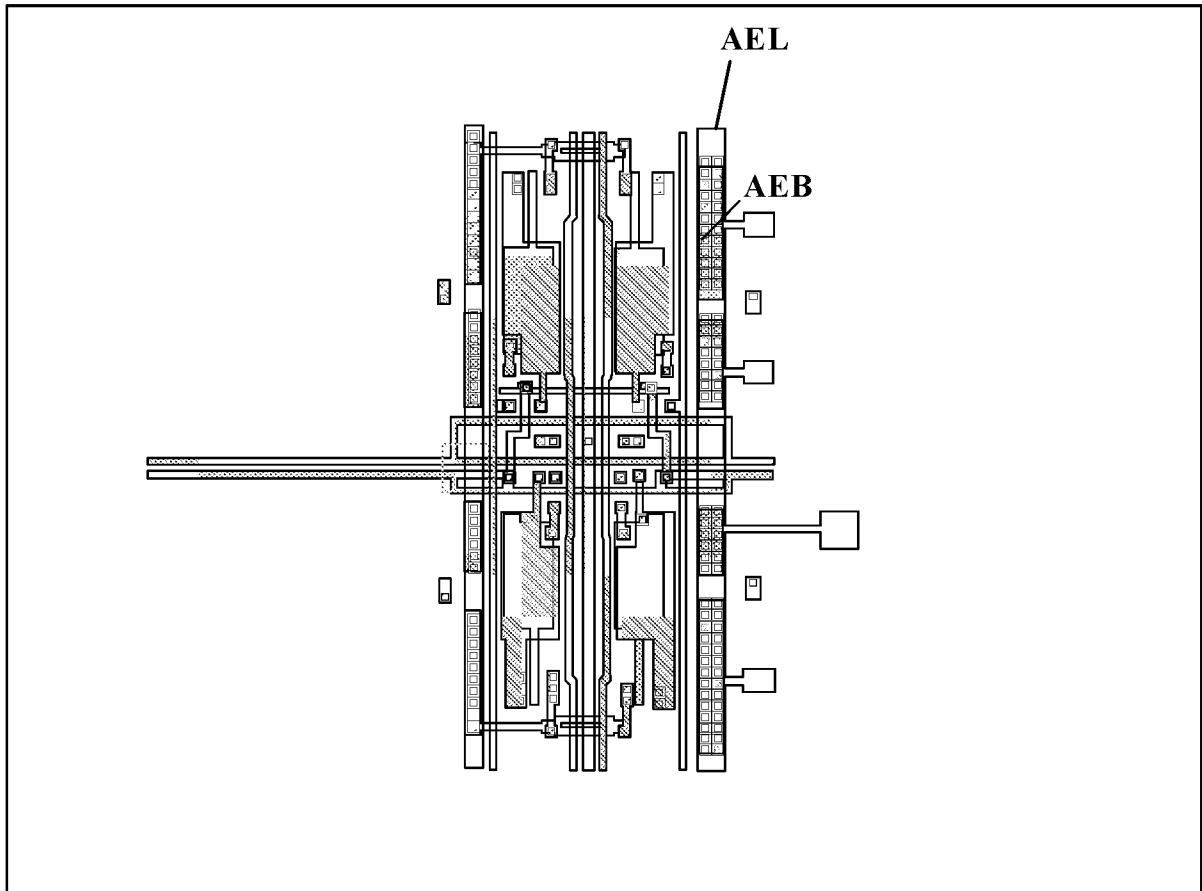


FIG. 11C

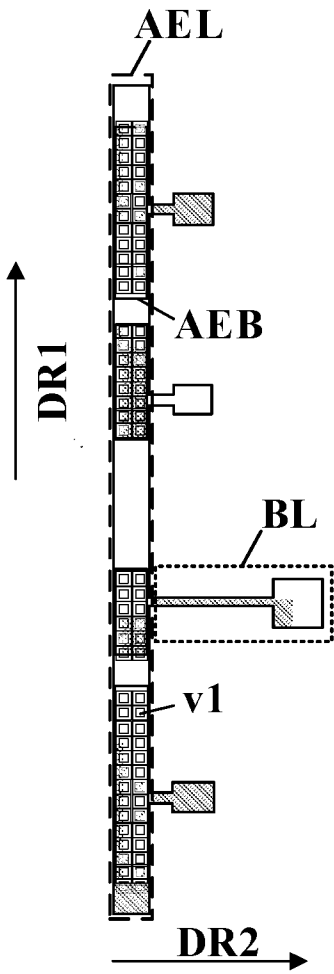


FIG. 11D

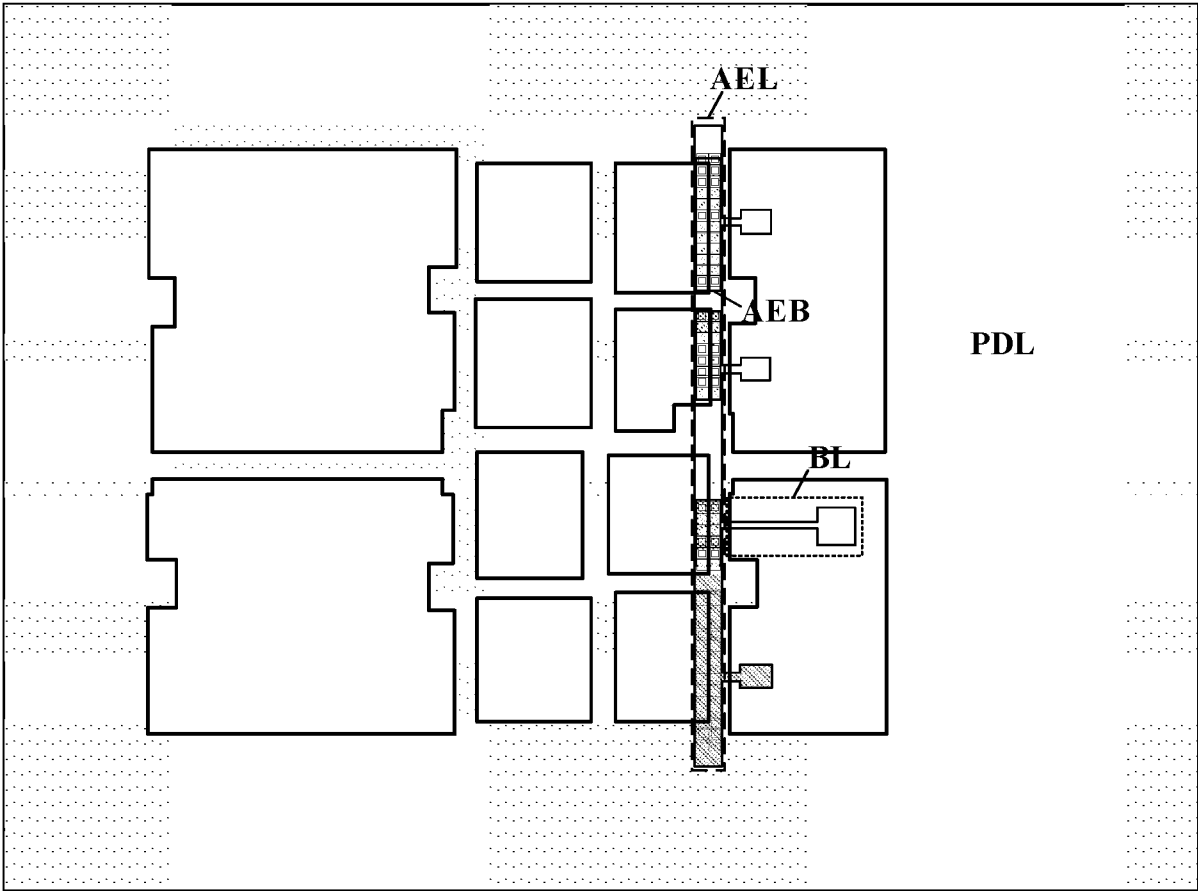


FIG. 11E

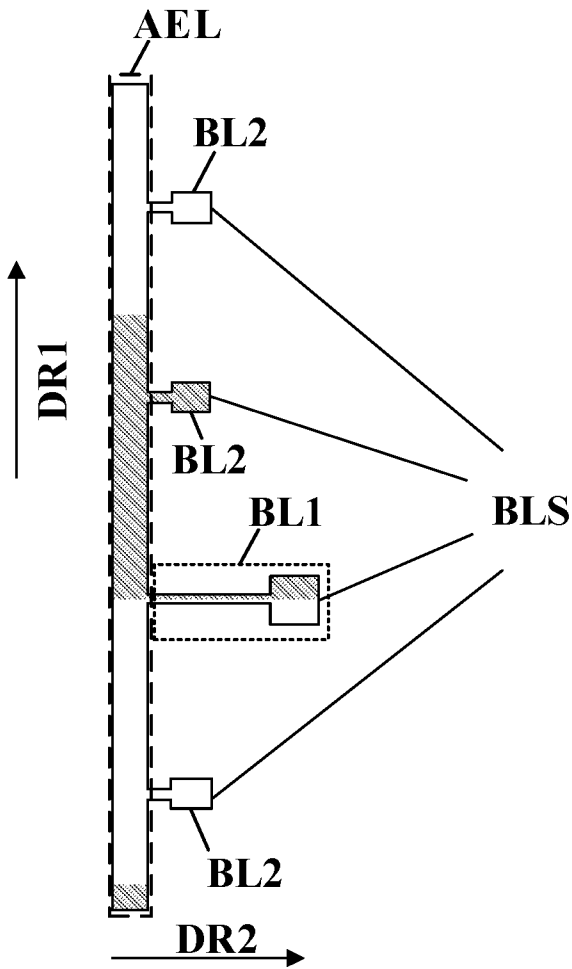


FIG. 11F

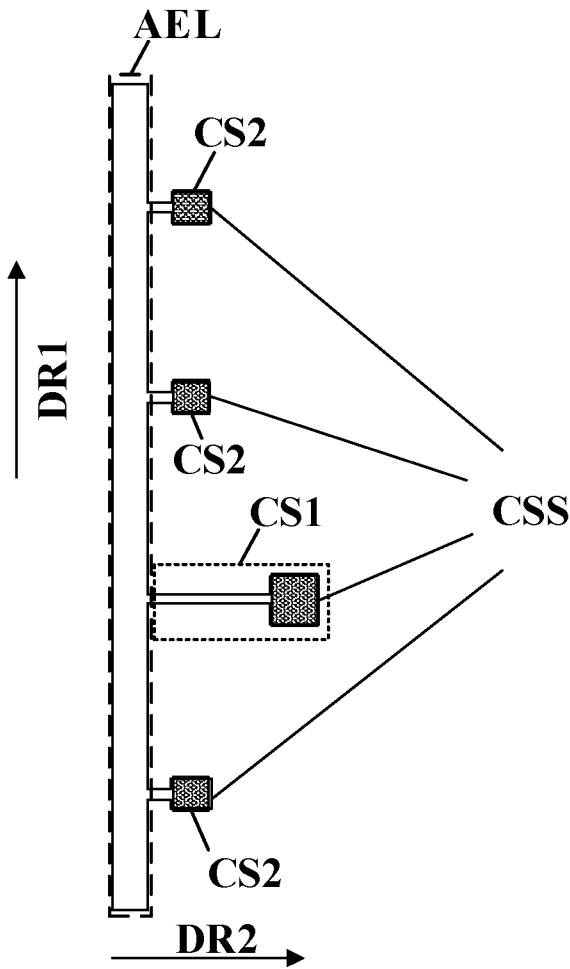


FIG. 11G

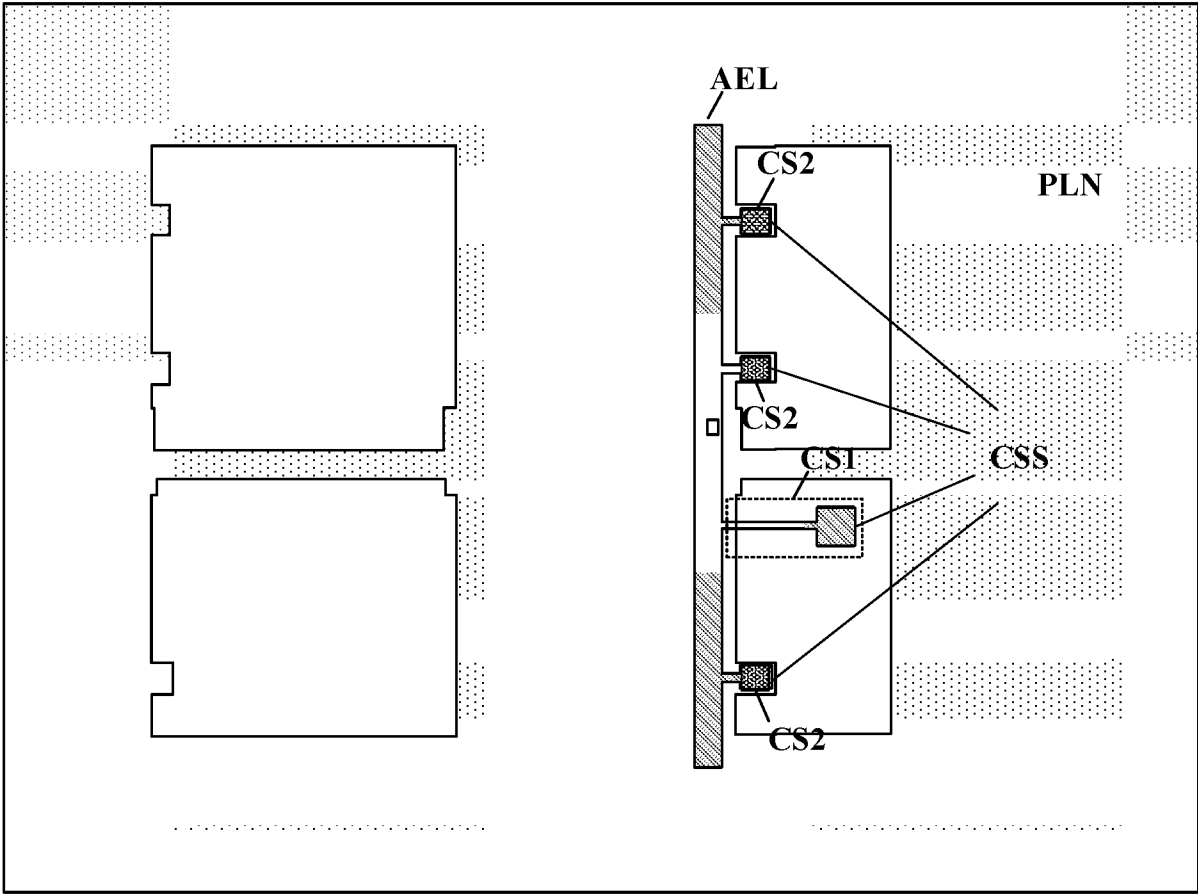


FIG. 11H

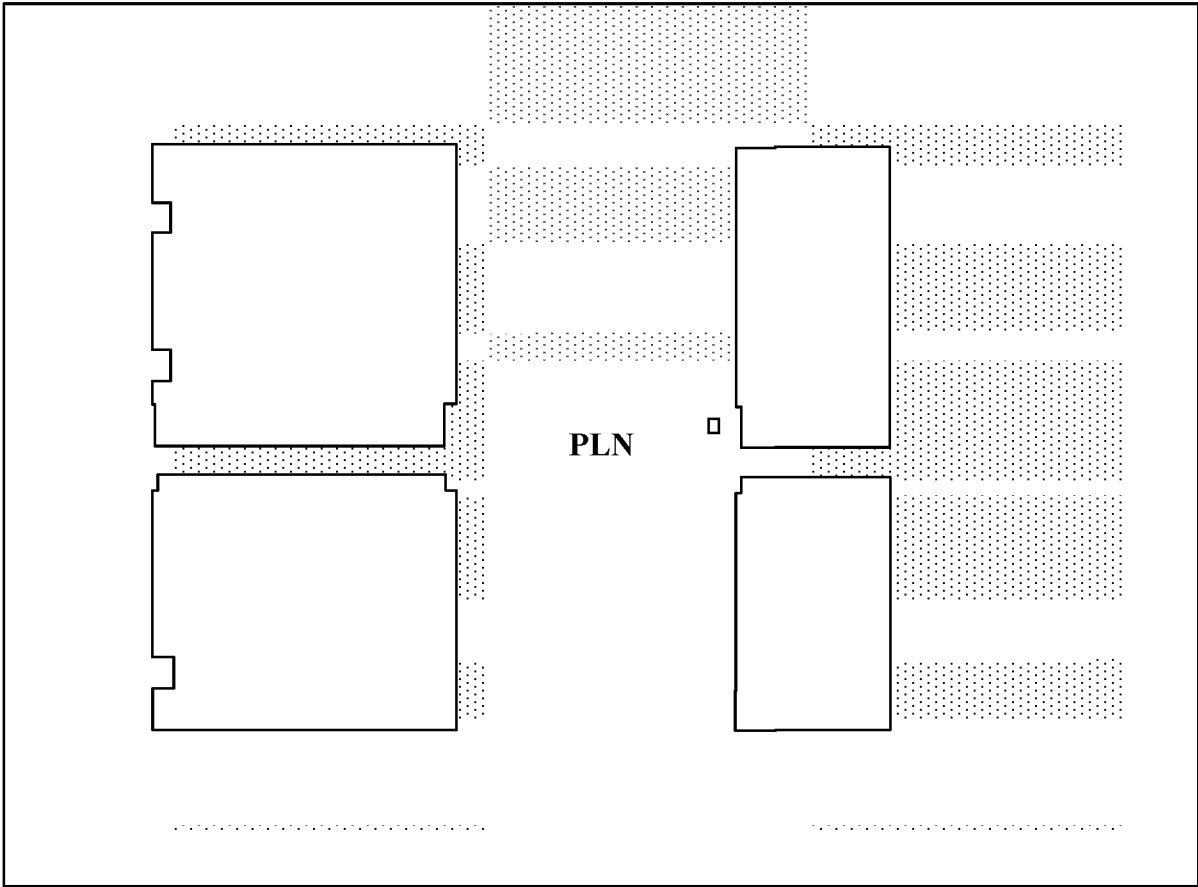


FIG. 12A

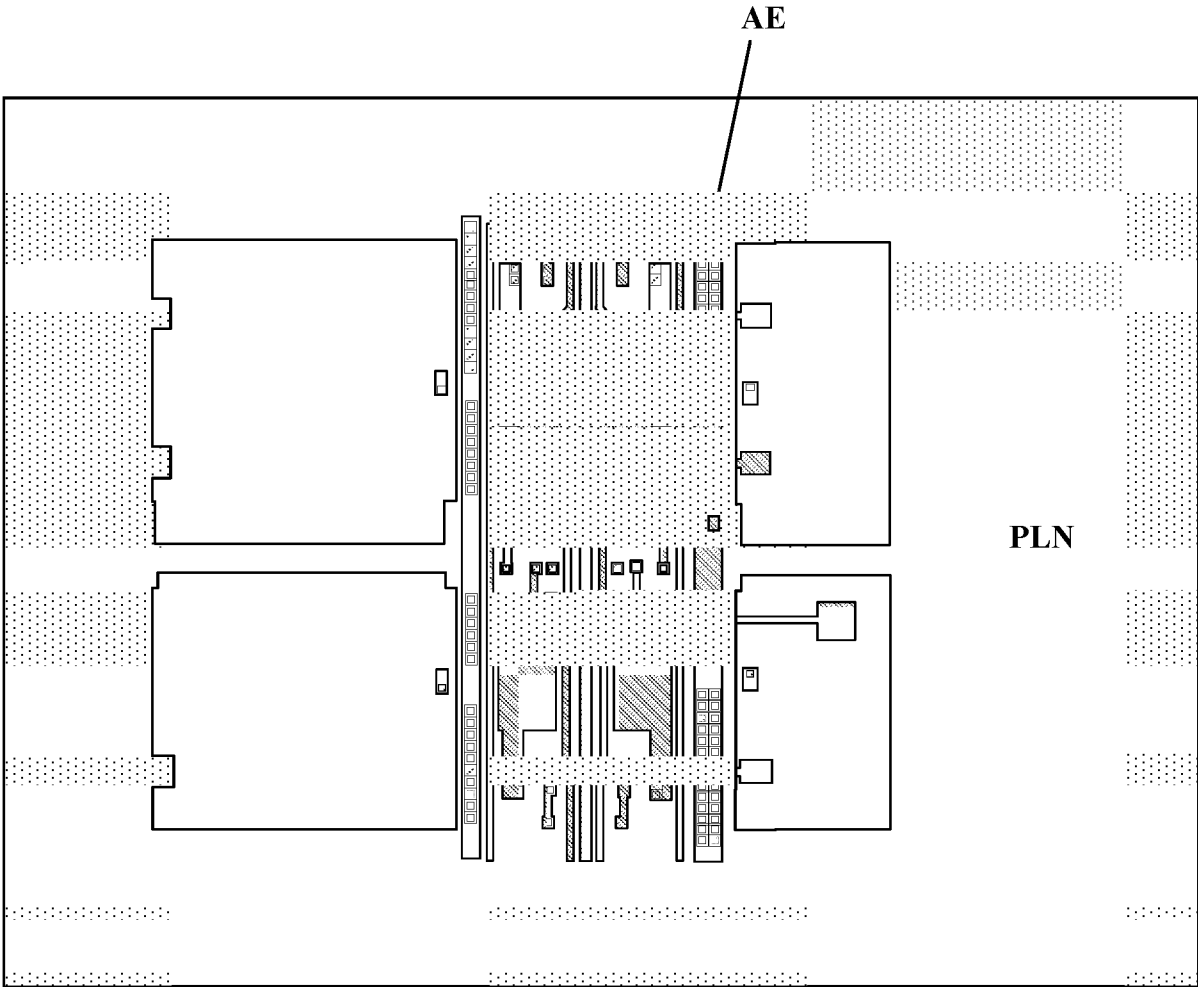


FIG. 12B

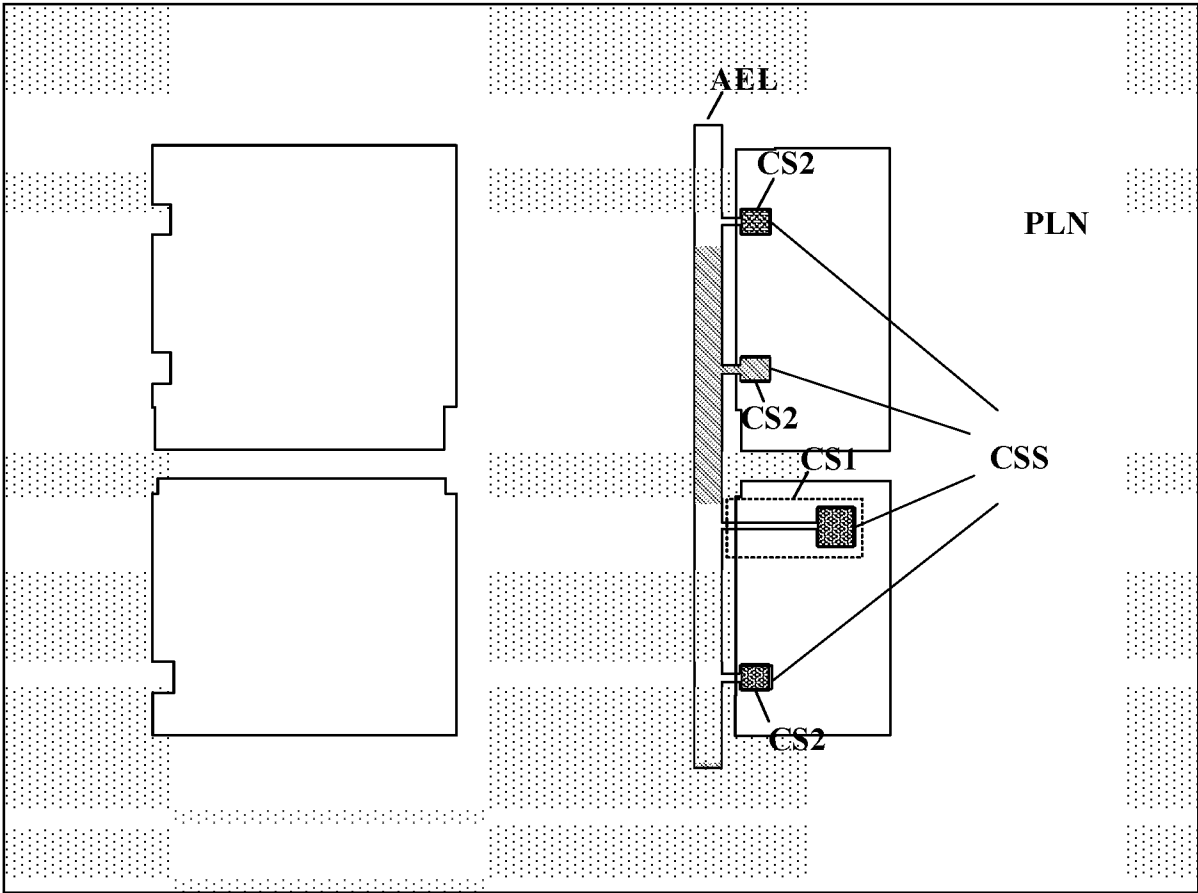


FIG. 12C

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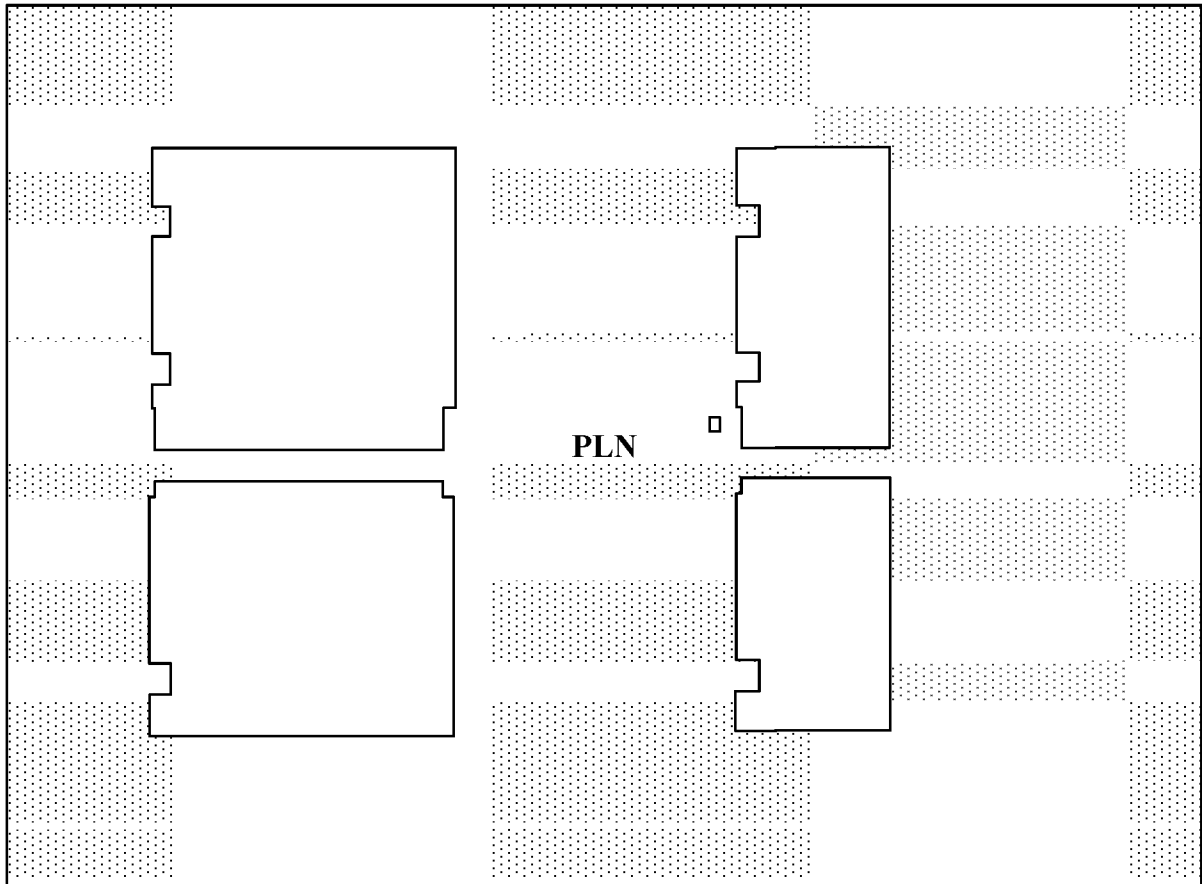


FIG. 13A

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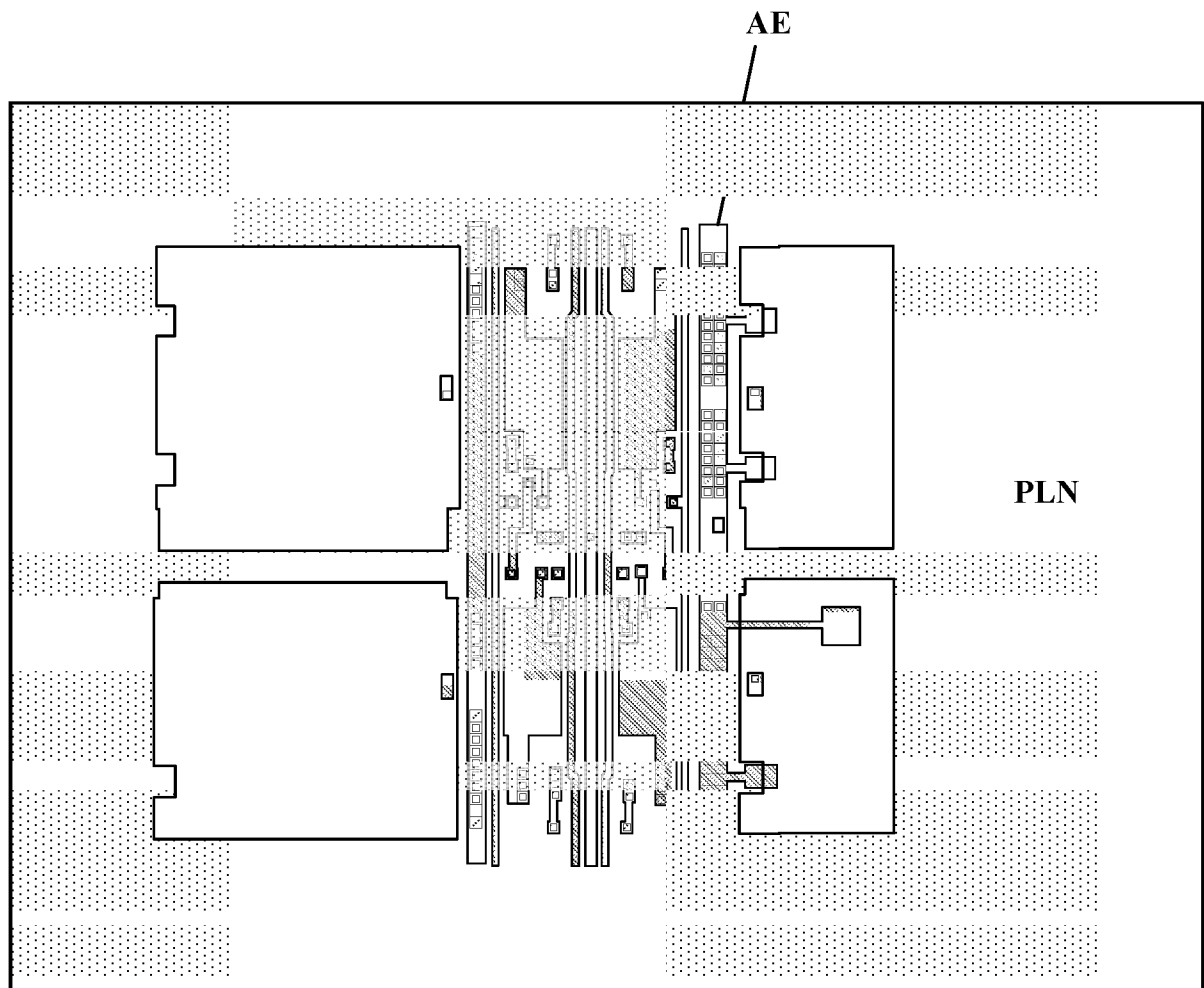


FIG. 13B

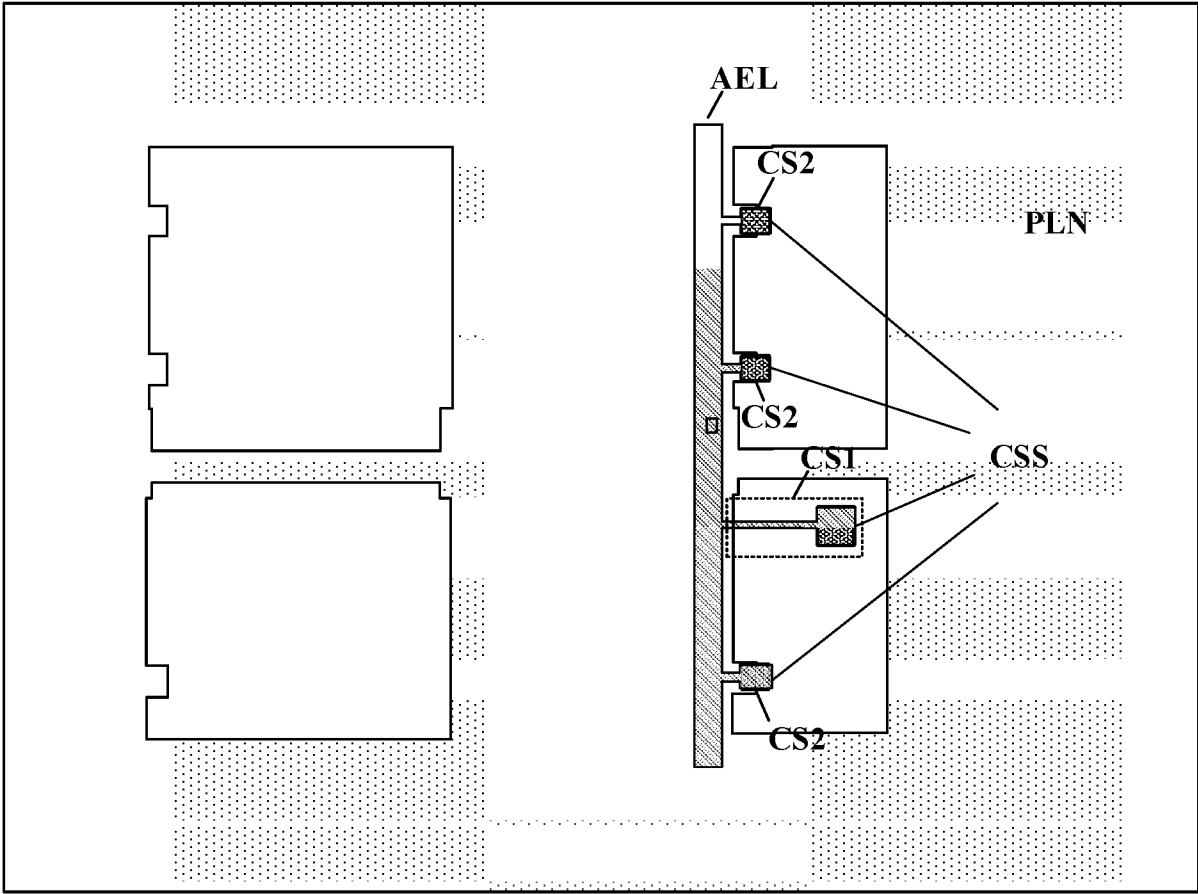


FIG. 13C

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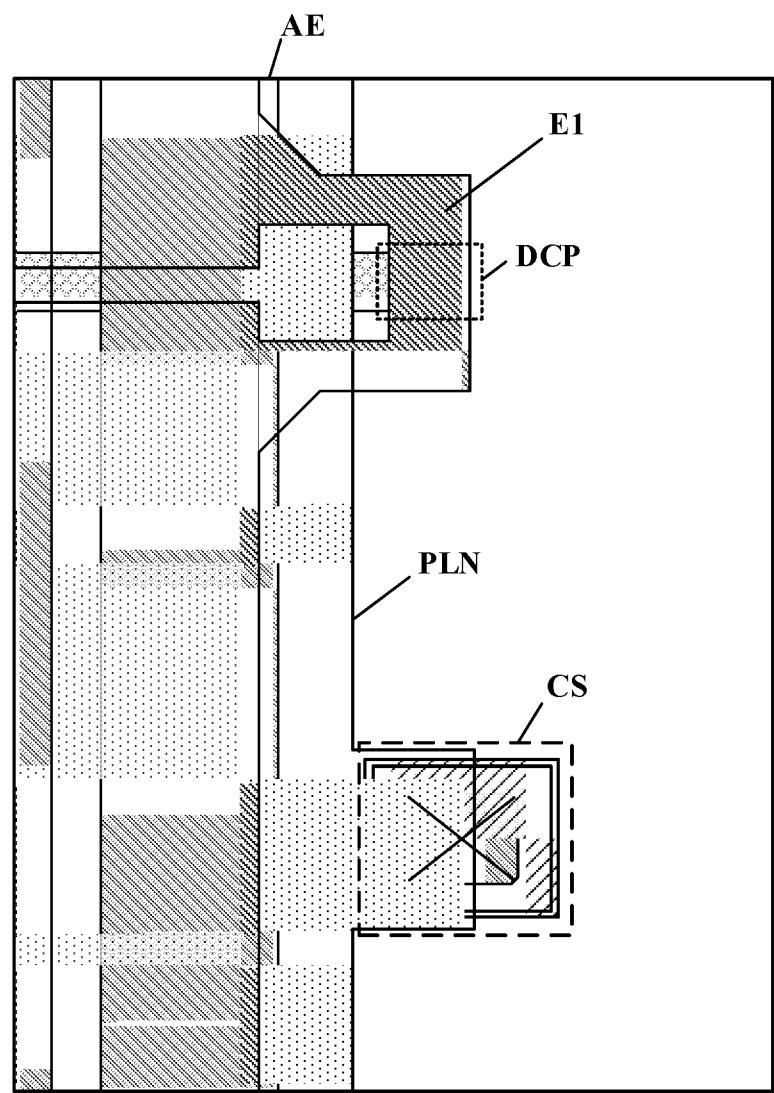


FIG. 14A

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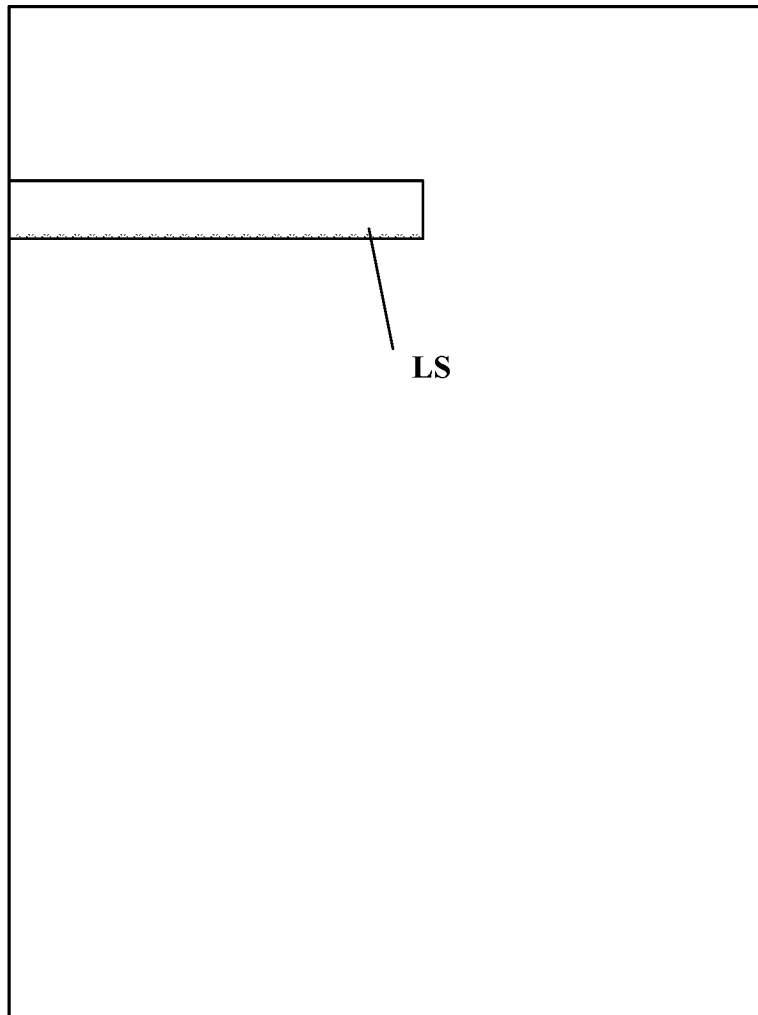


FIG. 14B

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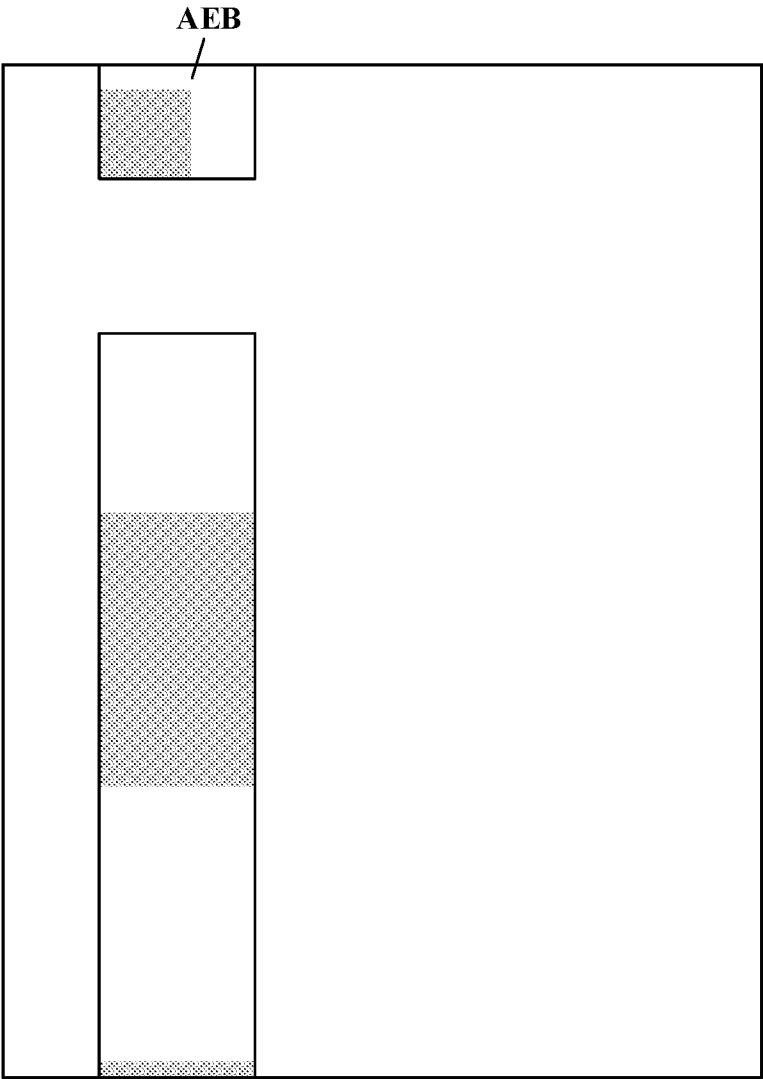


FIG. 14C

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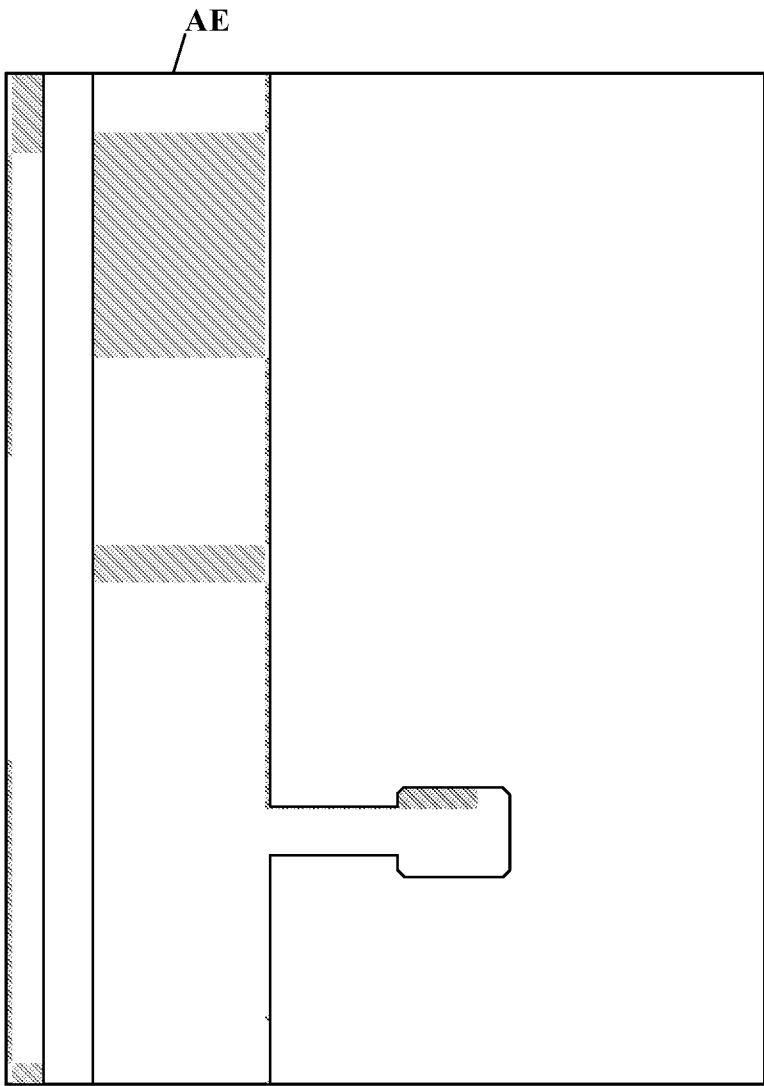


FIG. 14D

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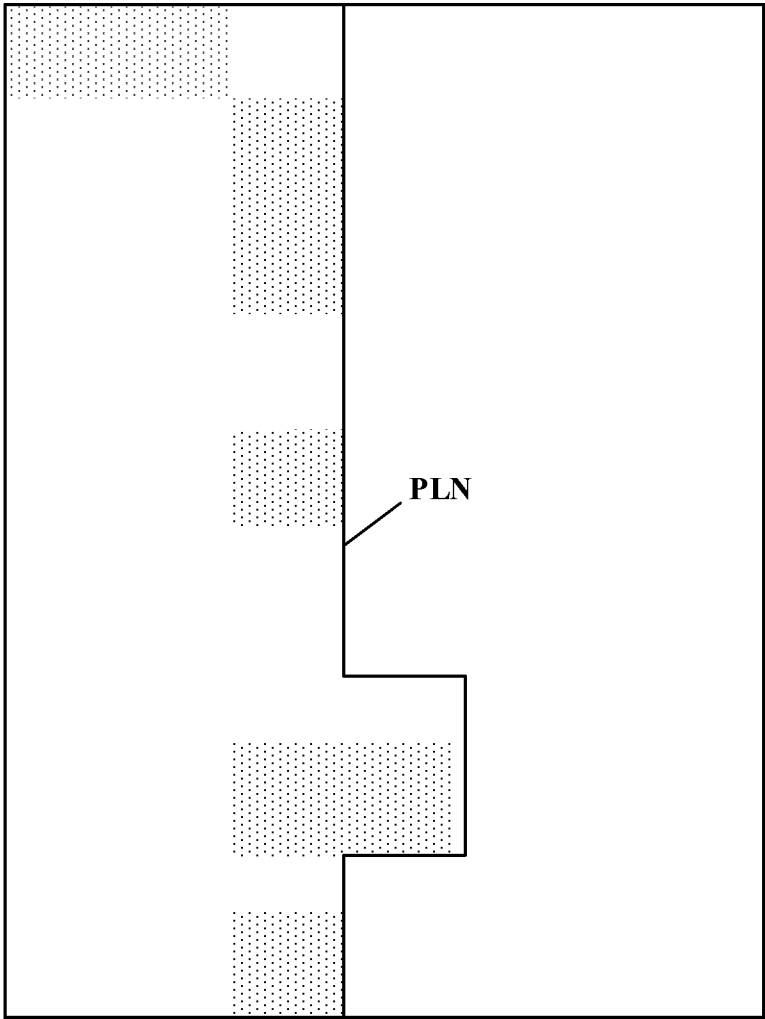


FIG. 14E

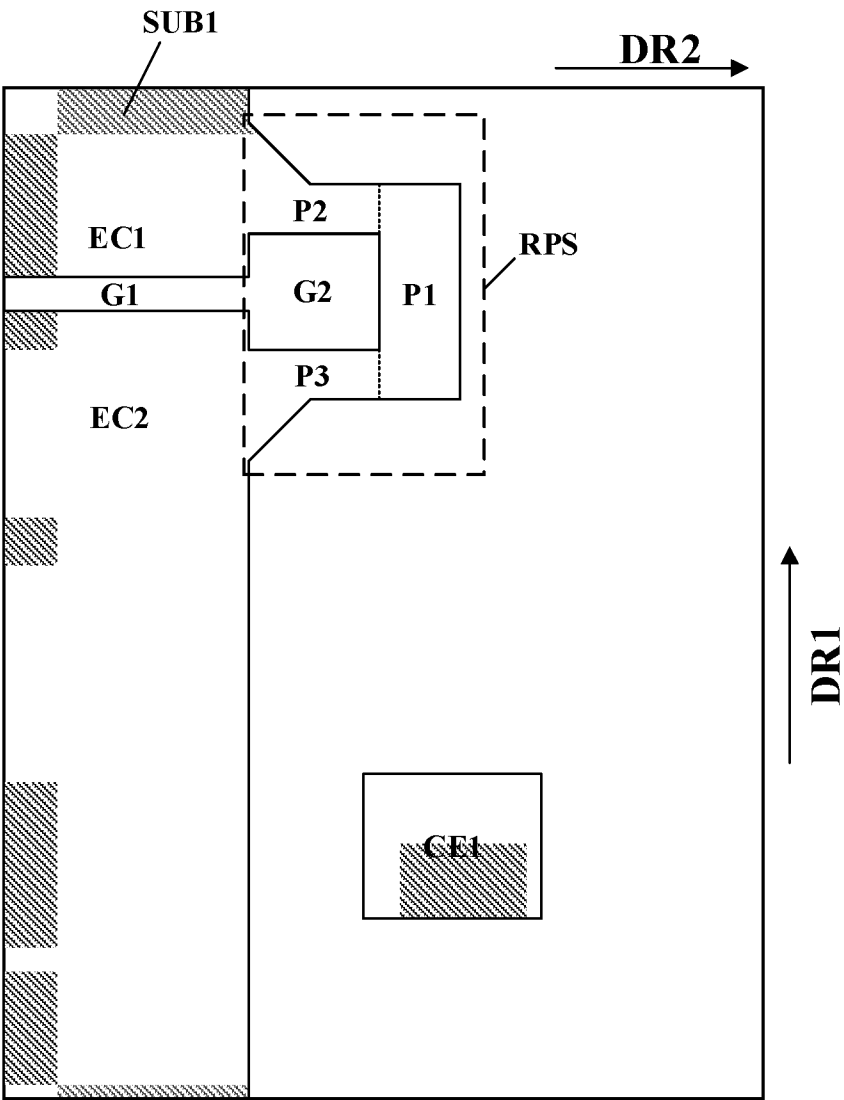


FIG. 14F

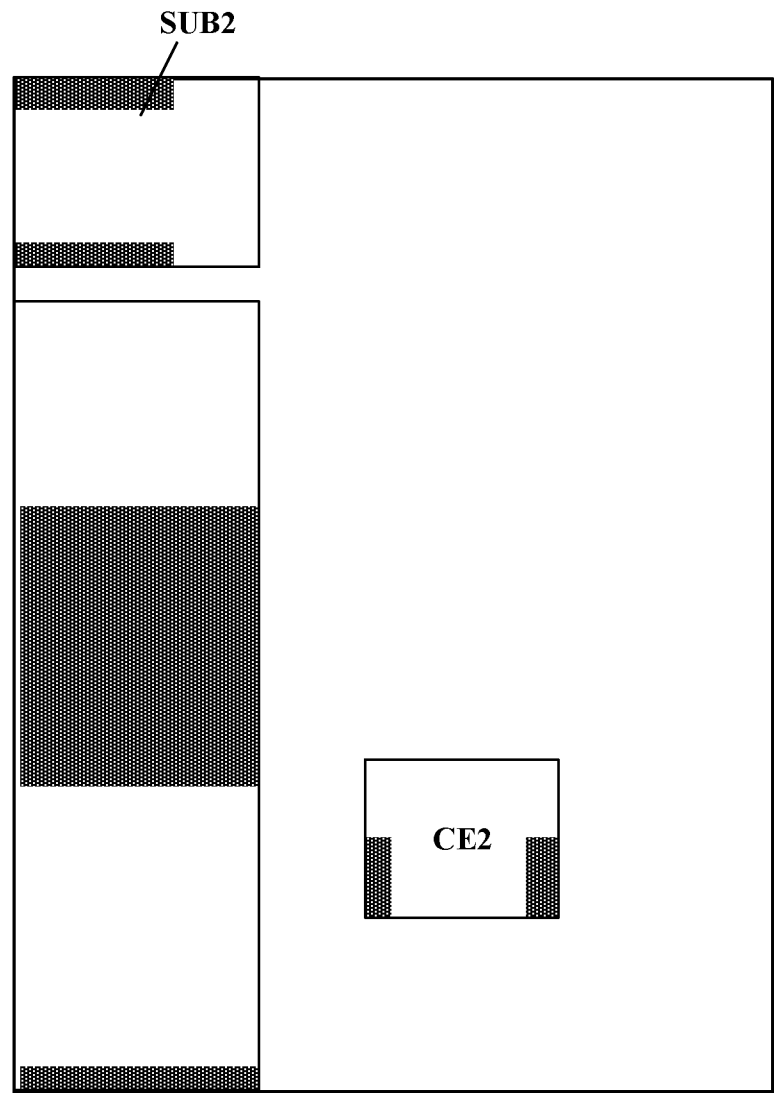


FIG. 14G

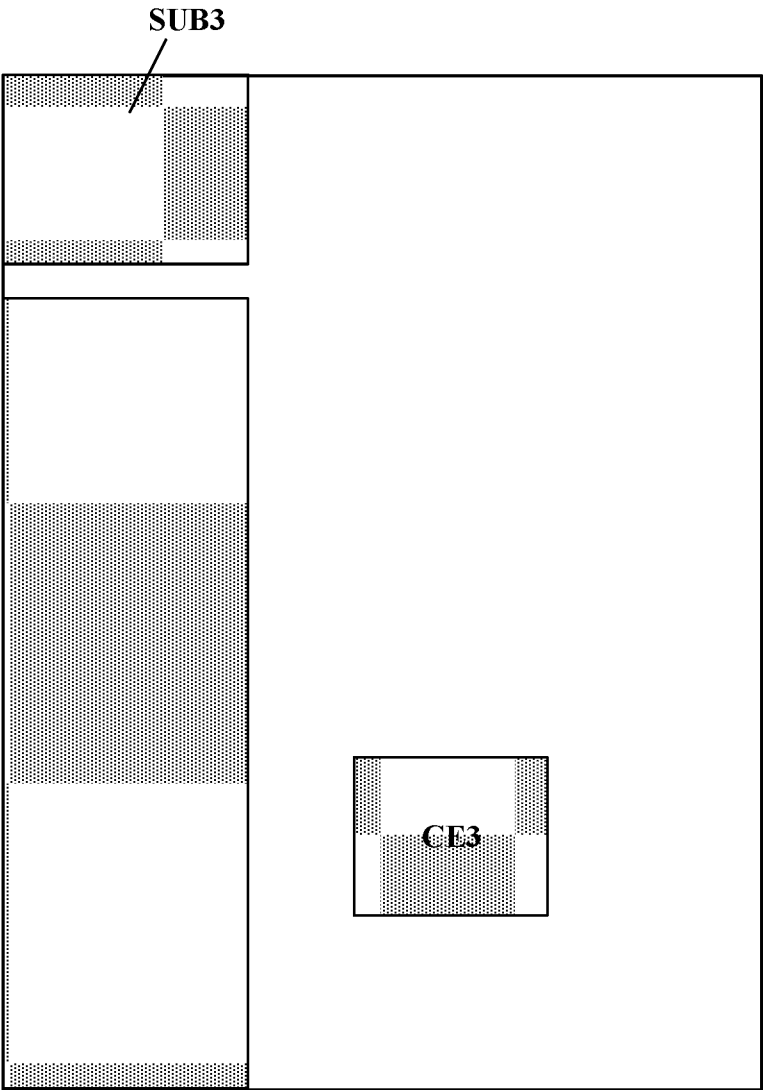


FIG. 14H

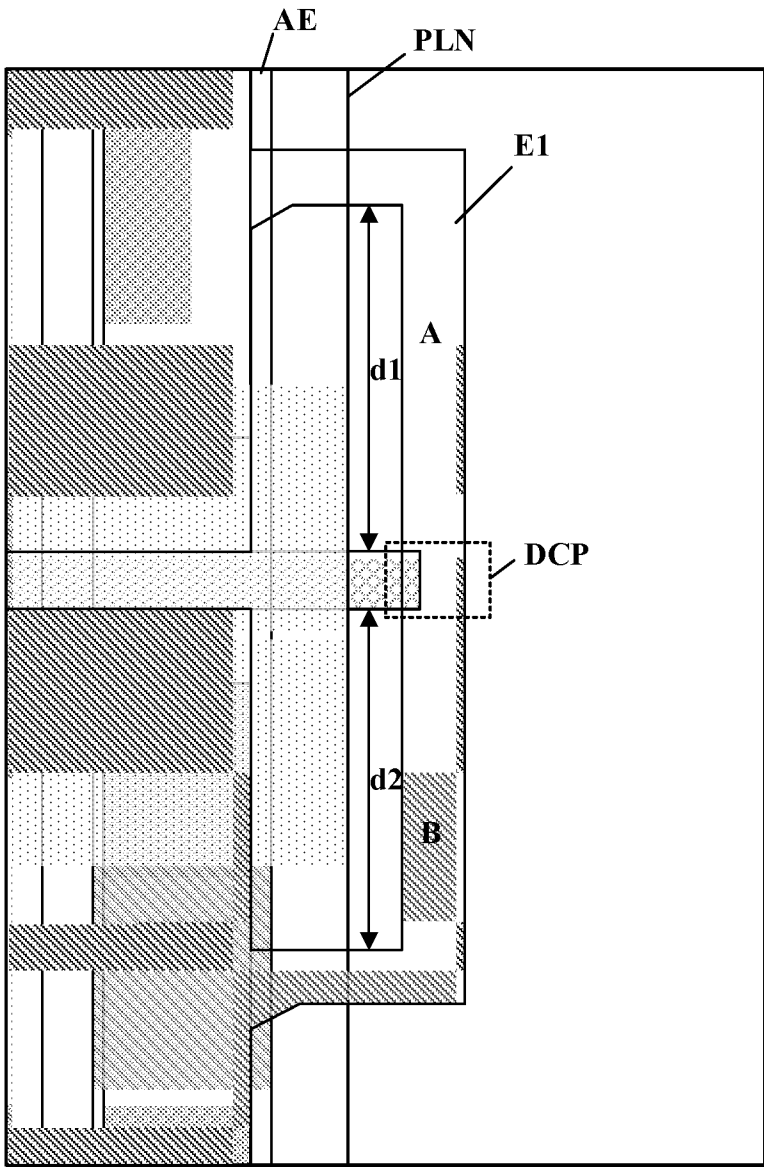


FIG. 15A

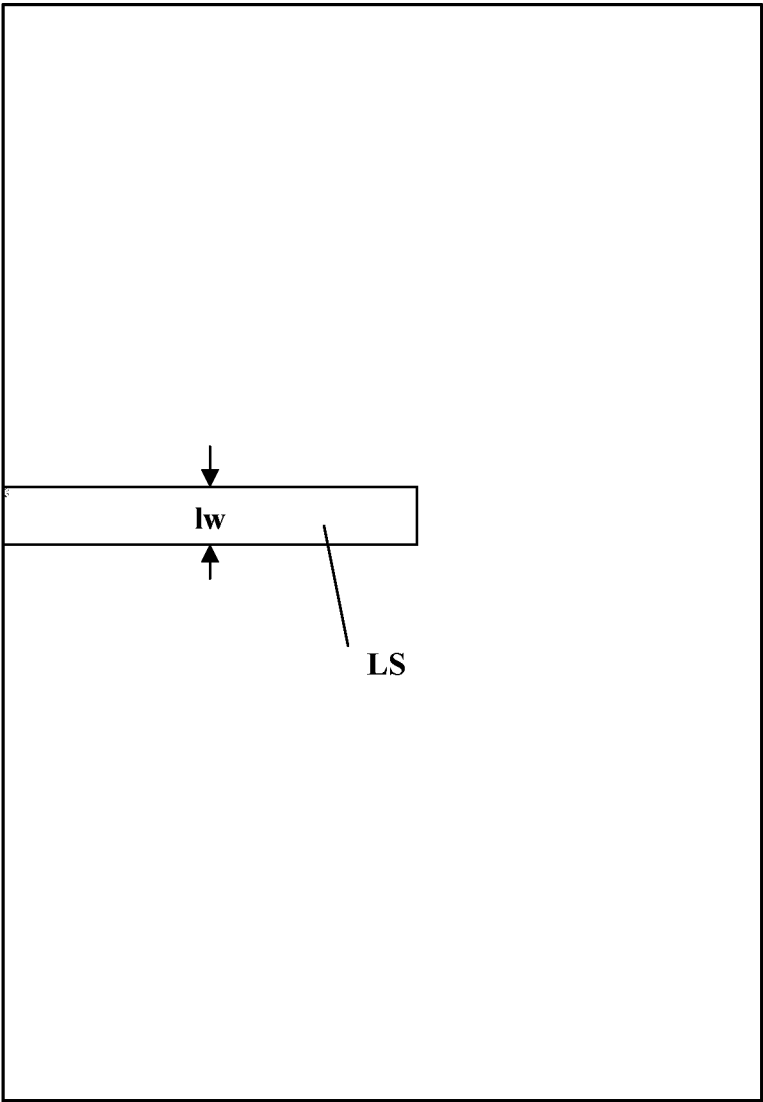


FIG. 15B

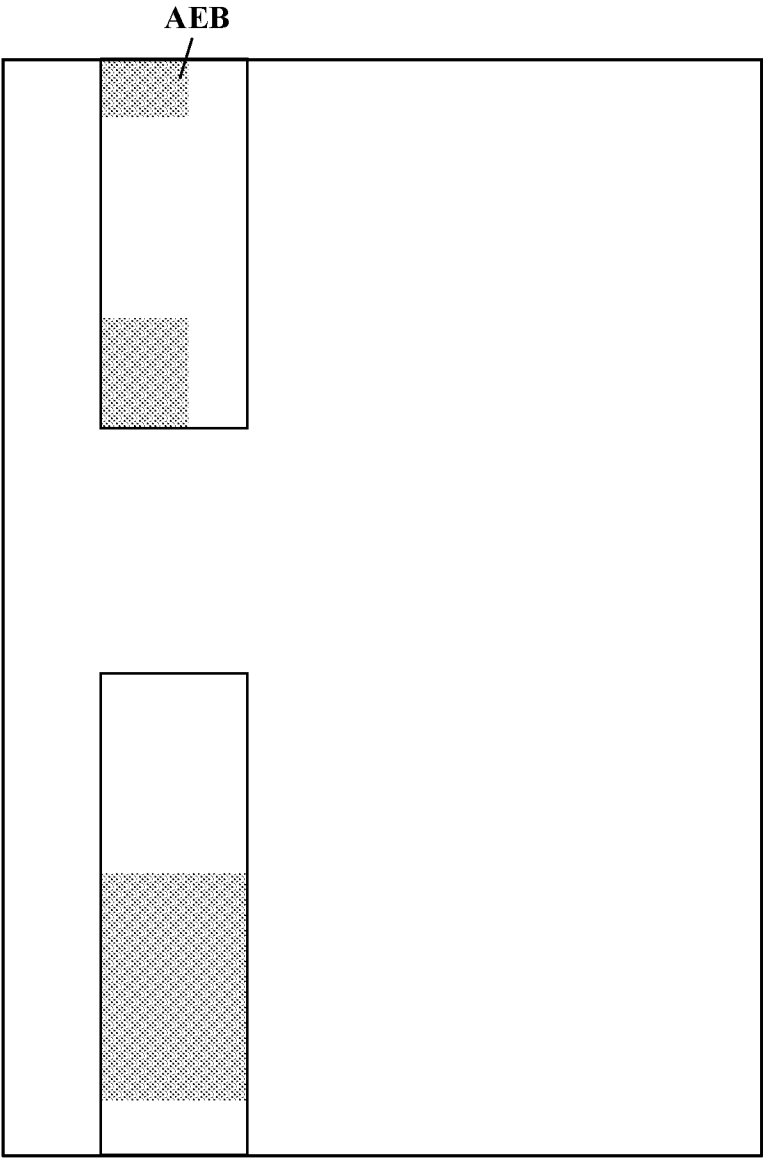


FIG. 15C

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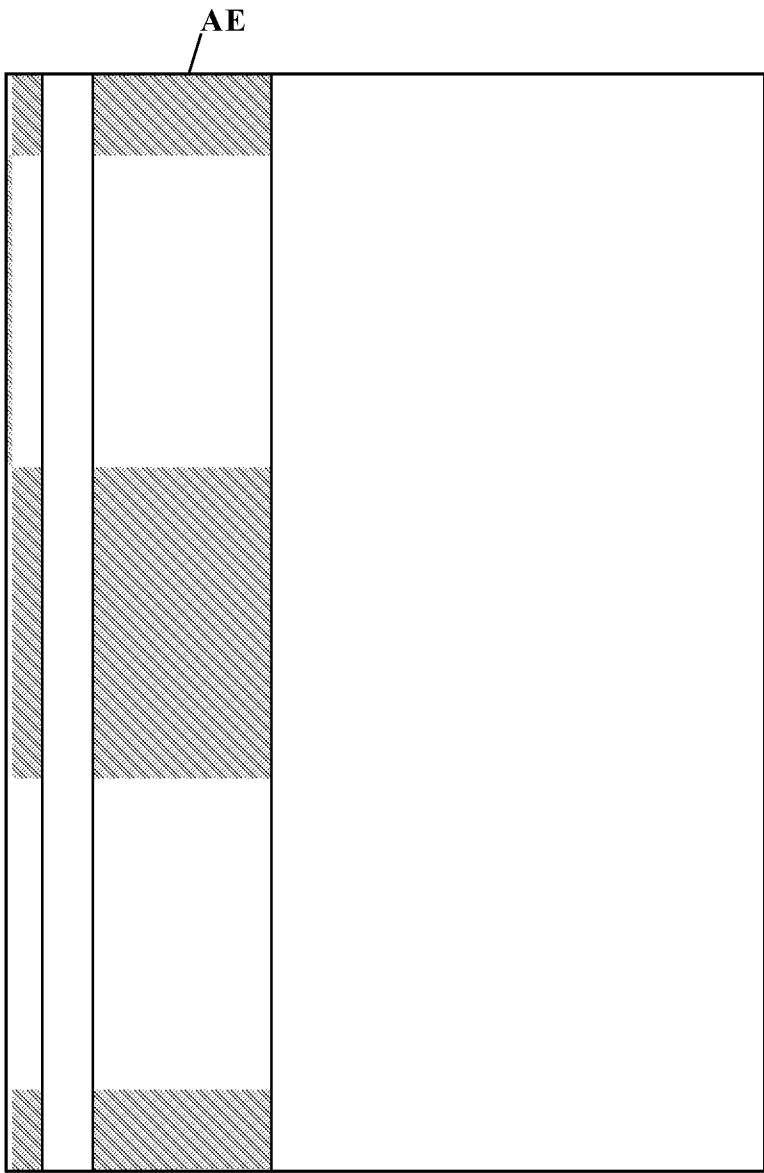


FIG. 15D

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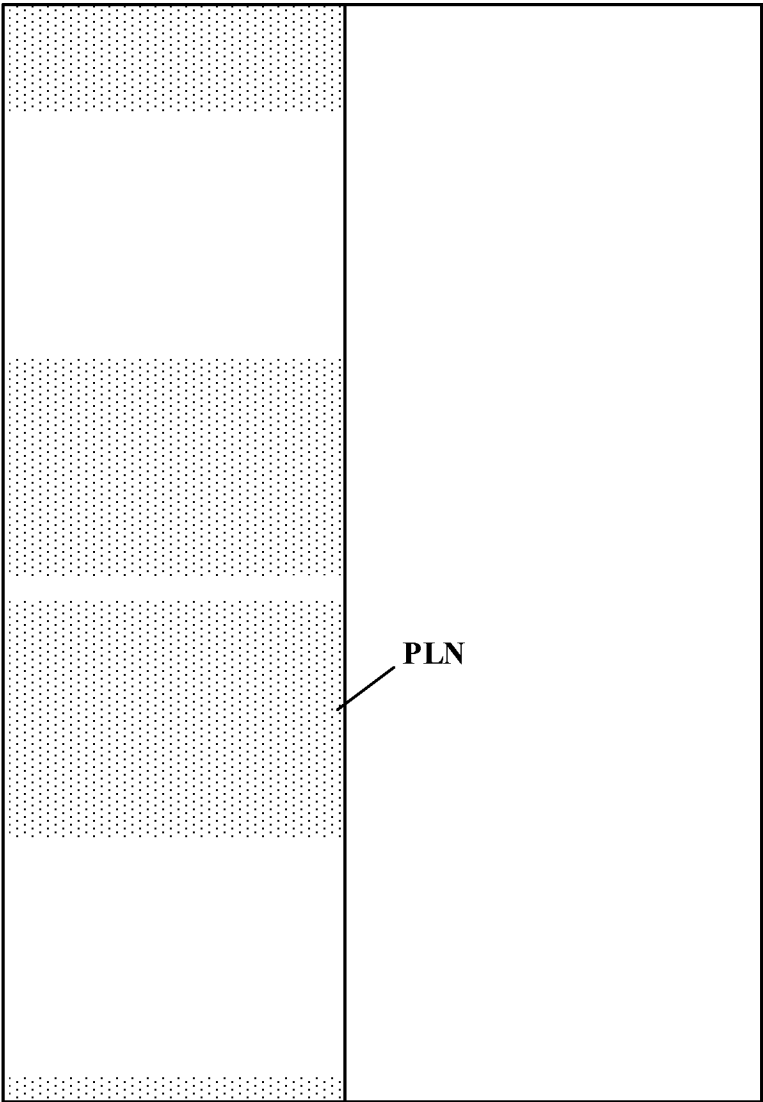


FIG. 15E

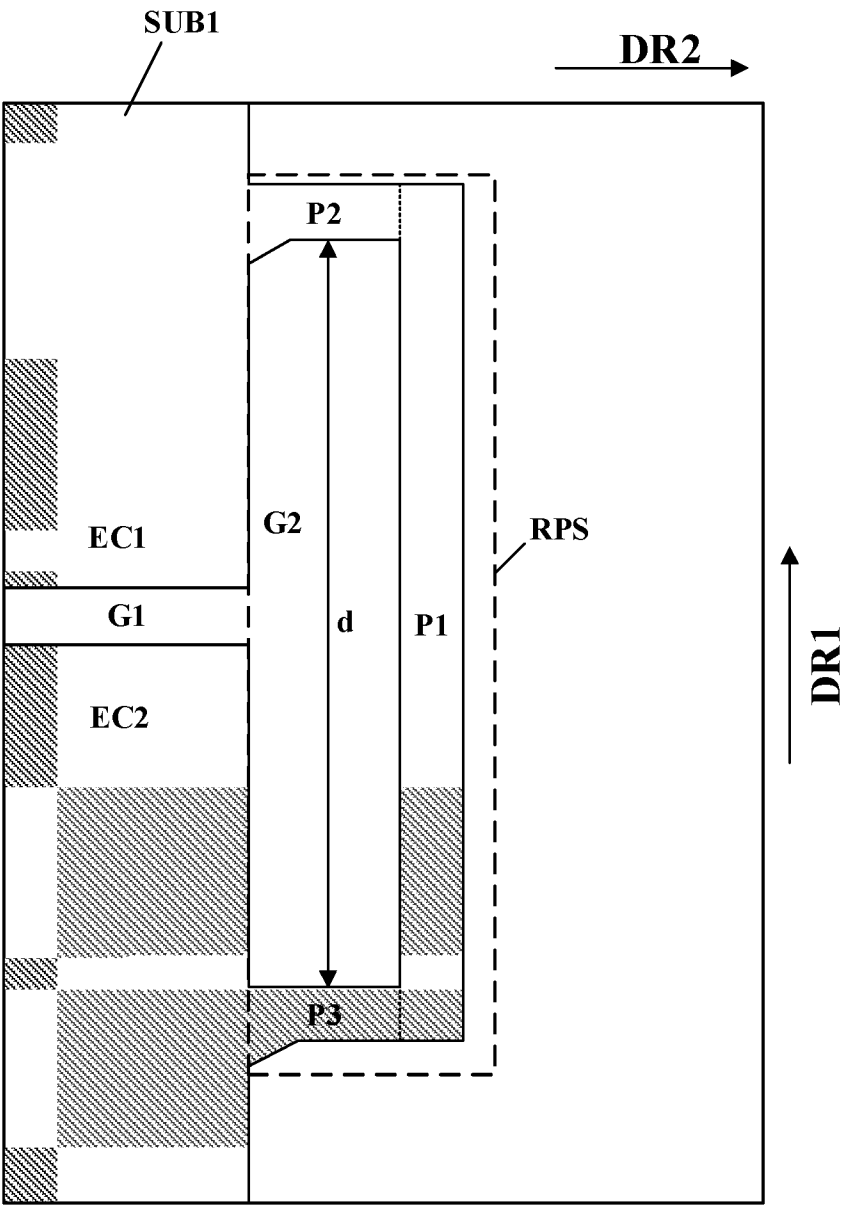


FIG. 15F

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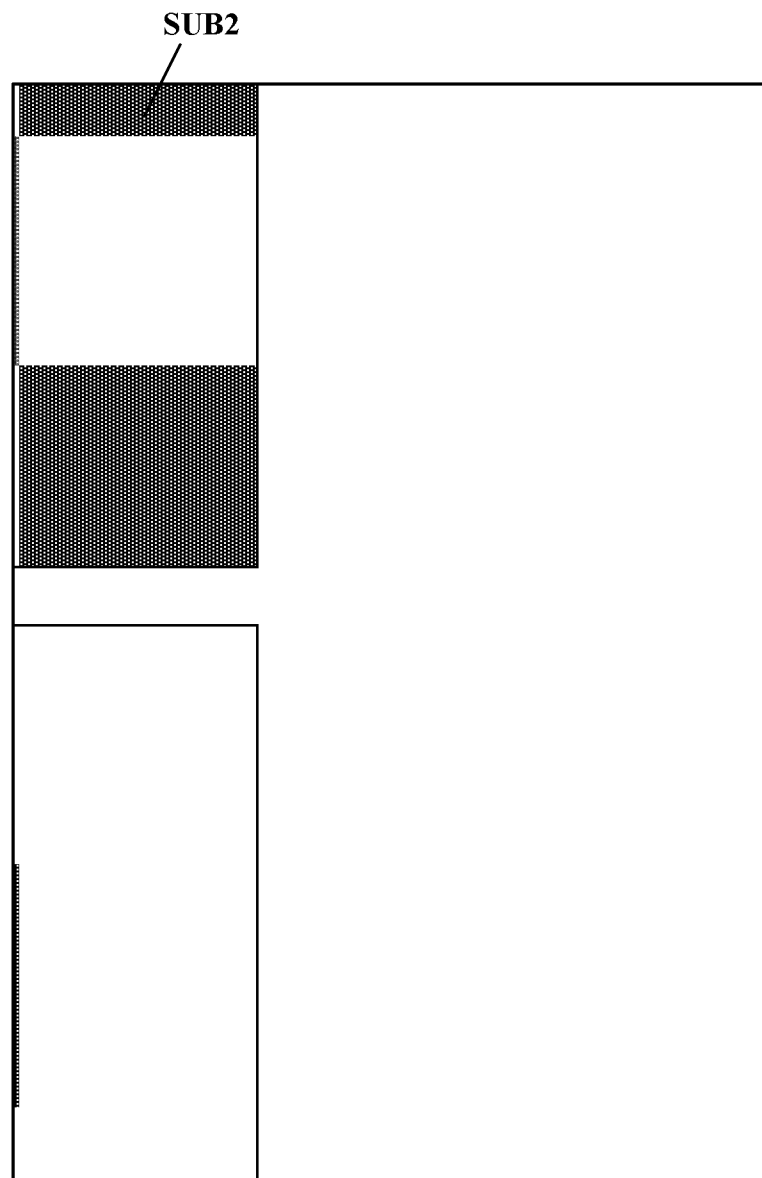


FIG. 15G

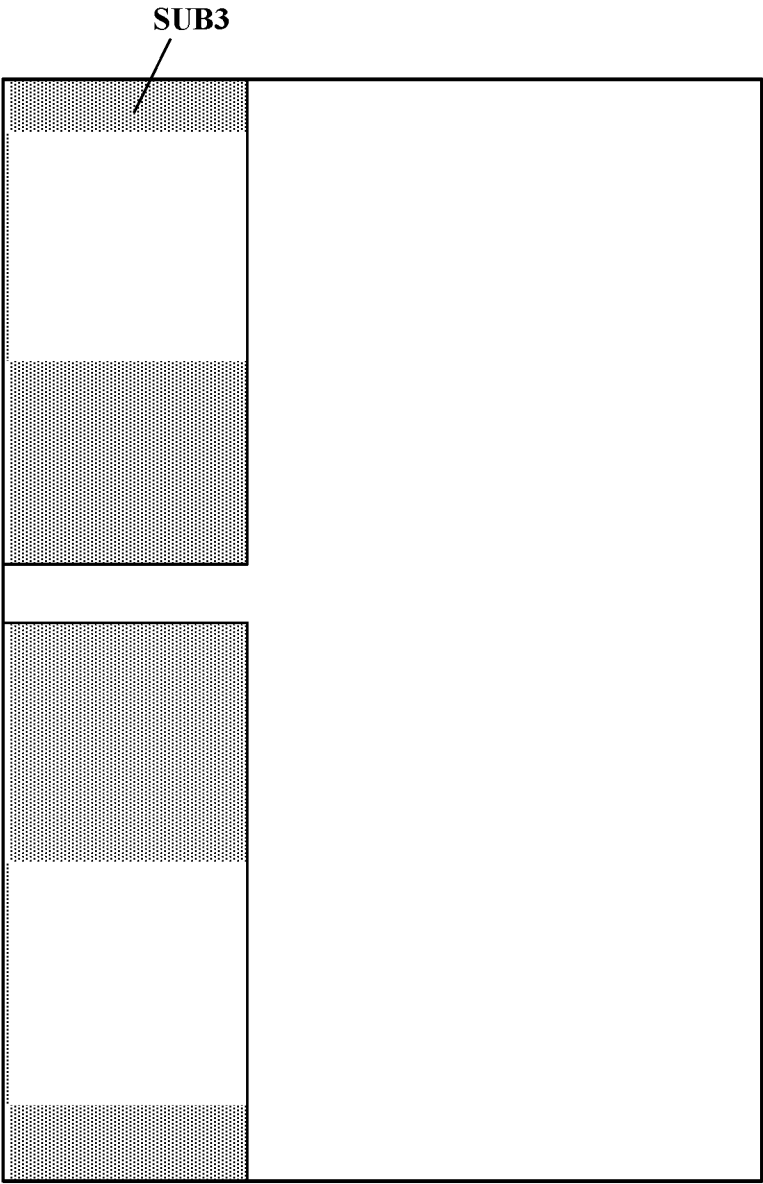


FIG. 15H

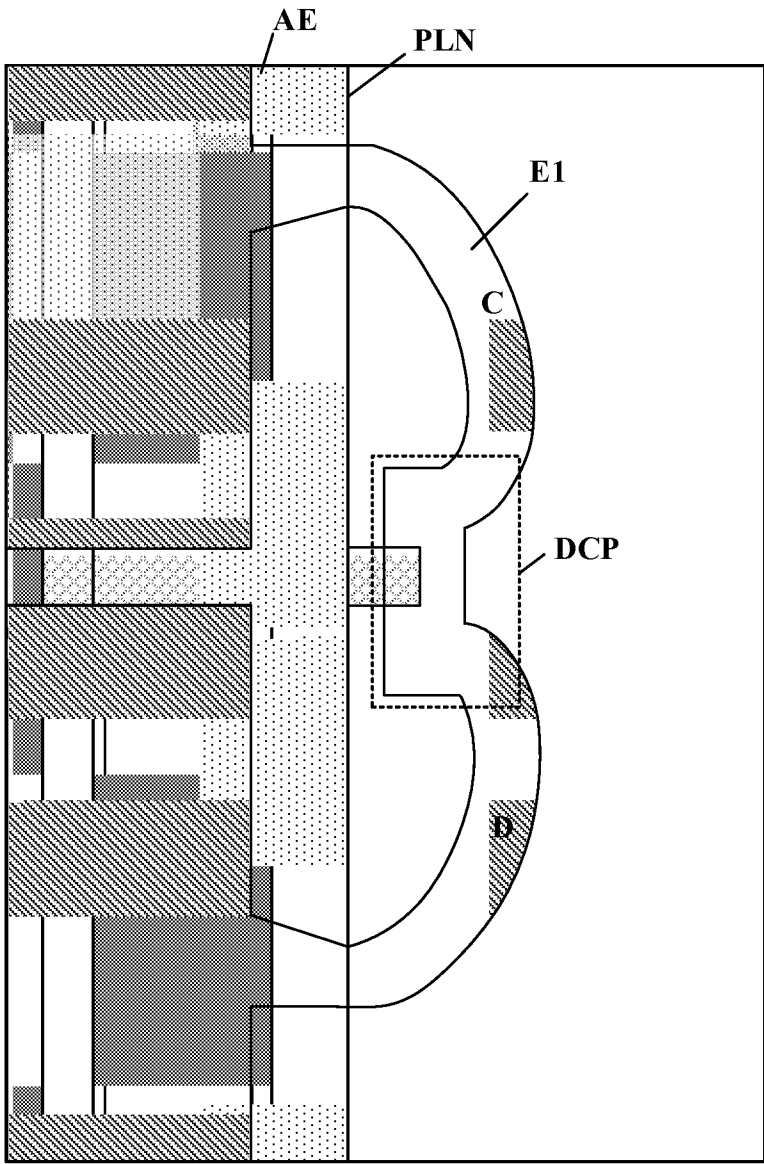


FIG. 16A

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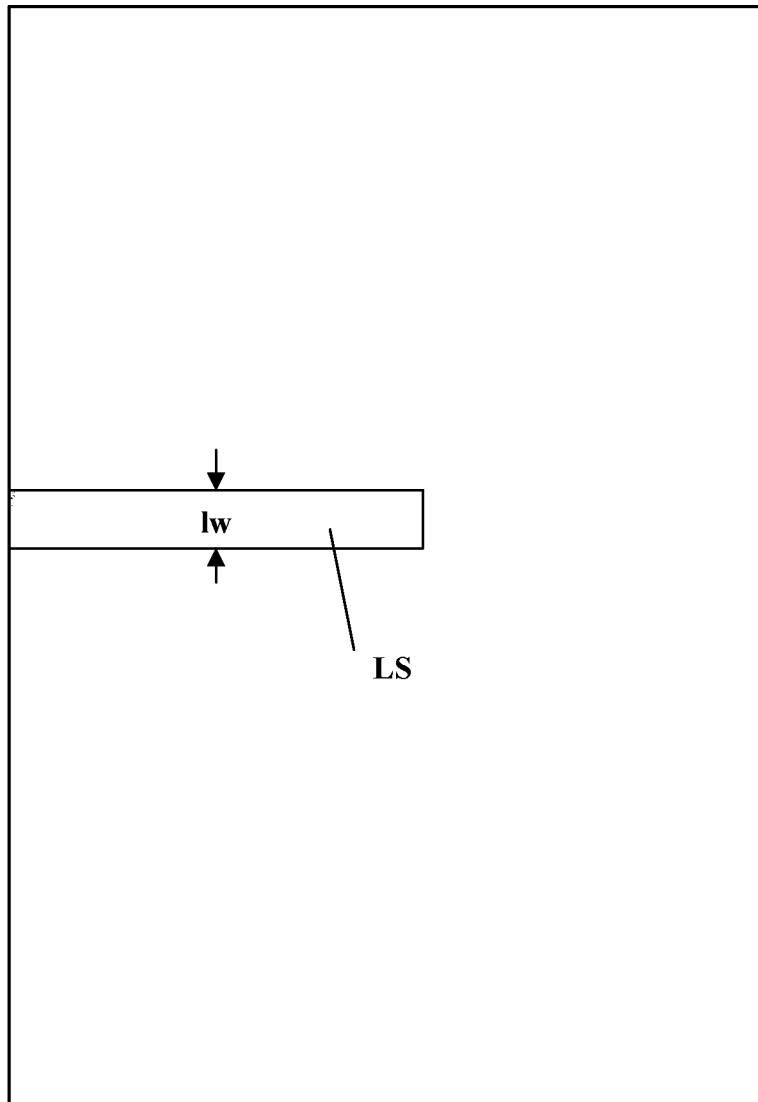


FIG. 16B

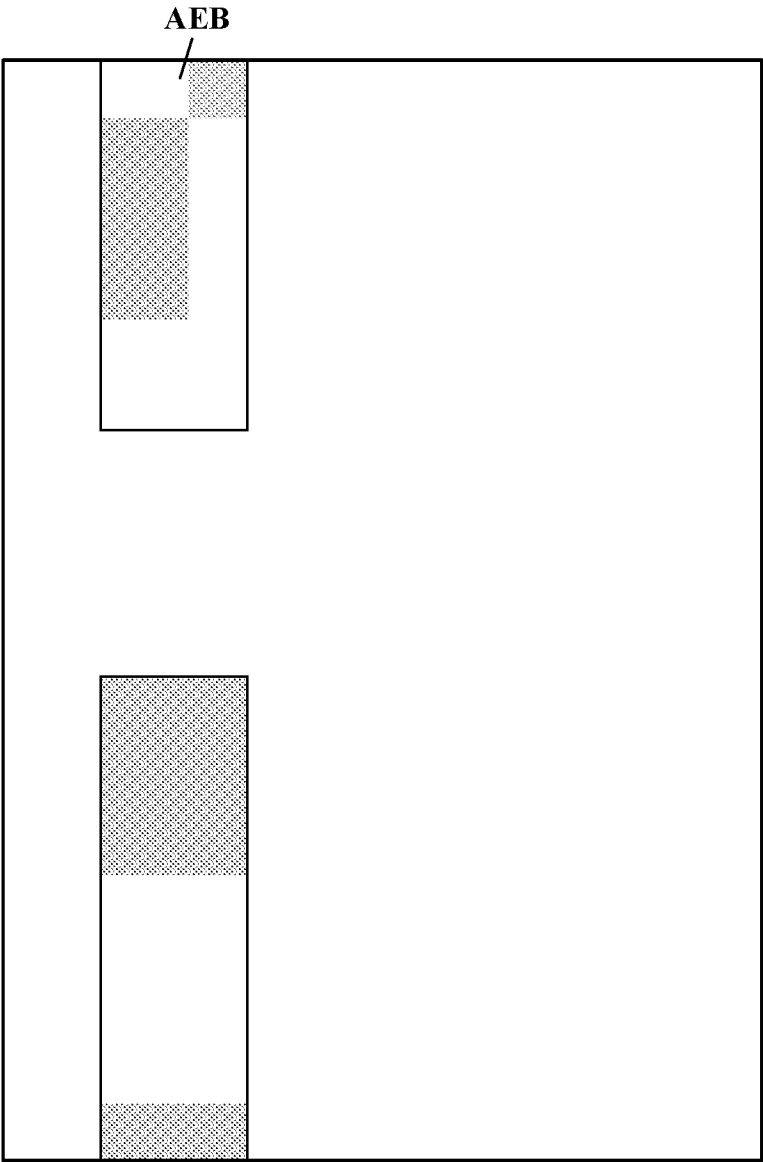


FIG. 16C

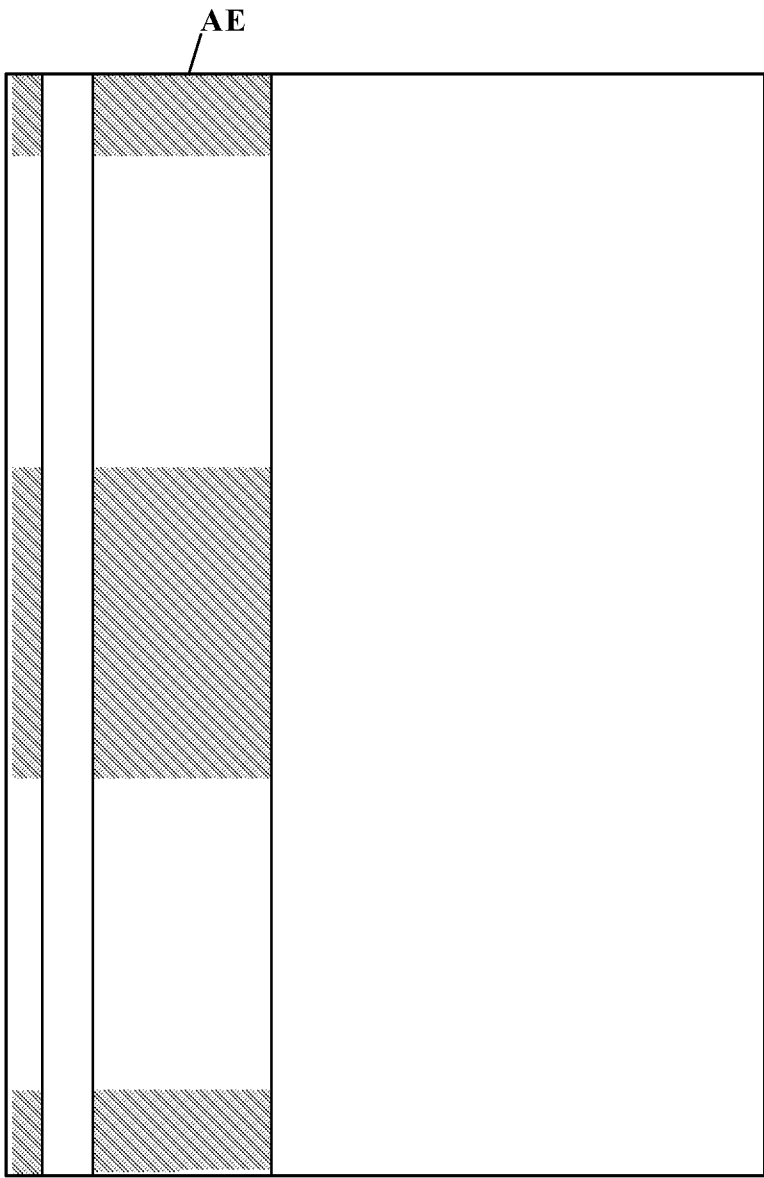


FIG. 16D

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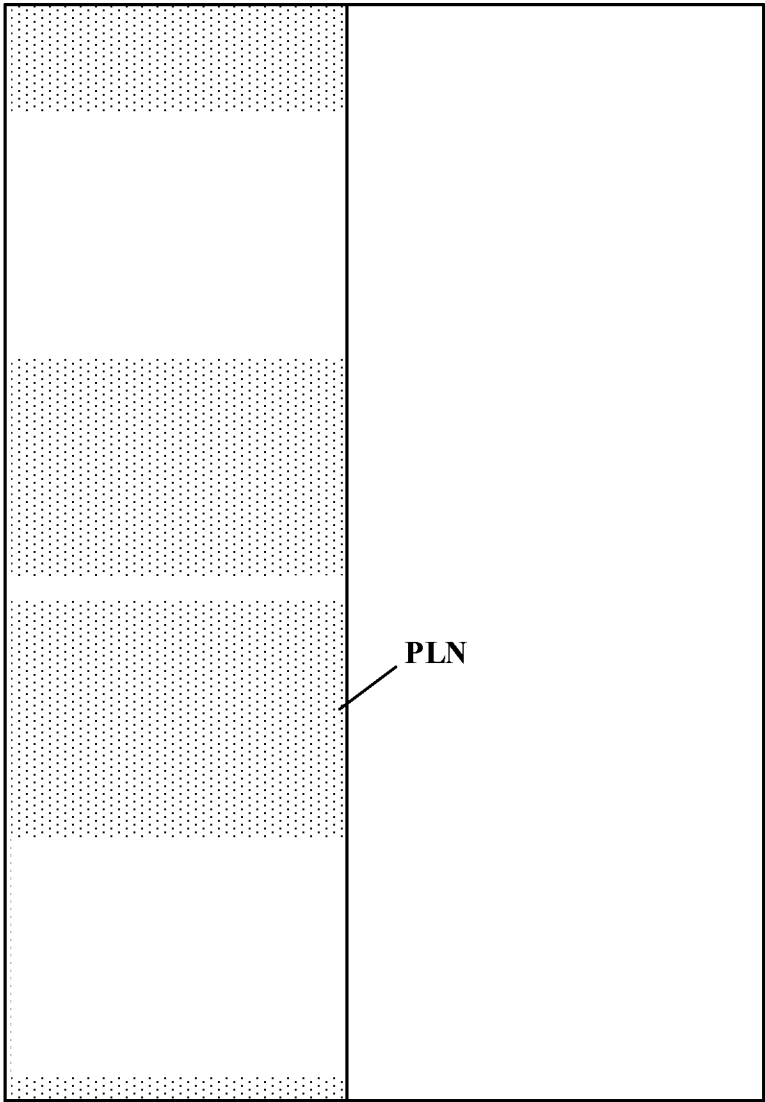


FIG. 16E

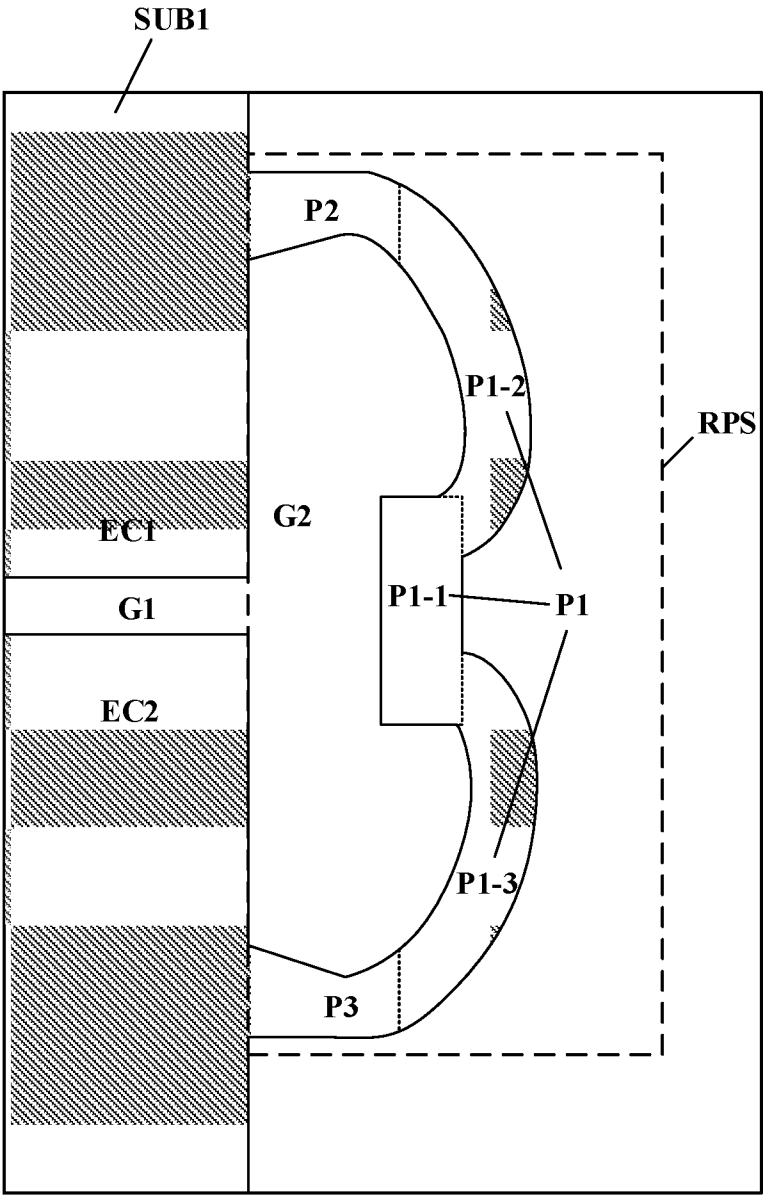


FIG. 16F

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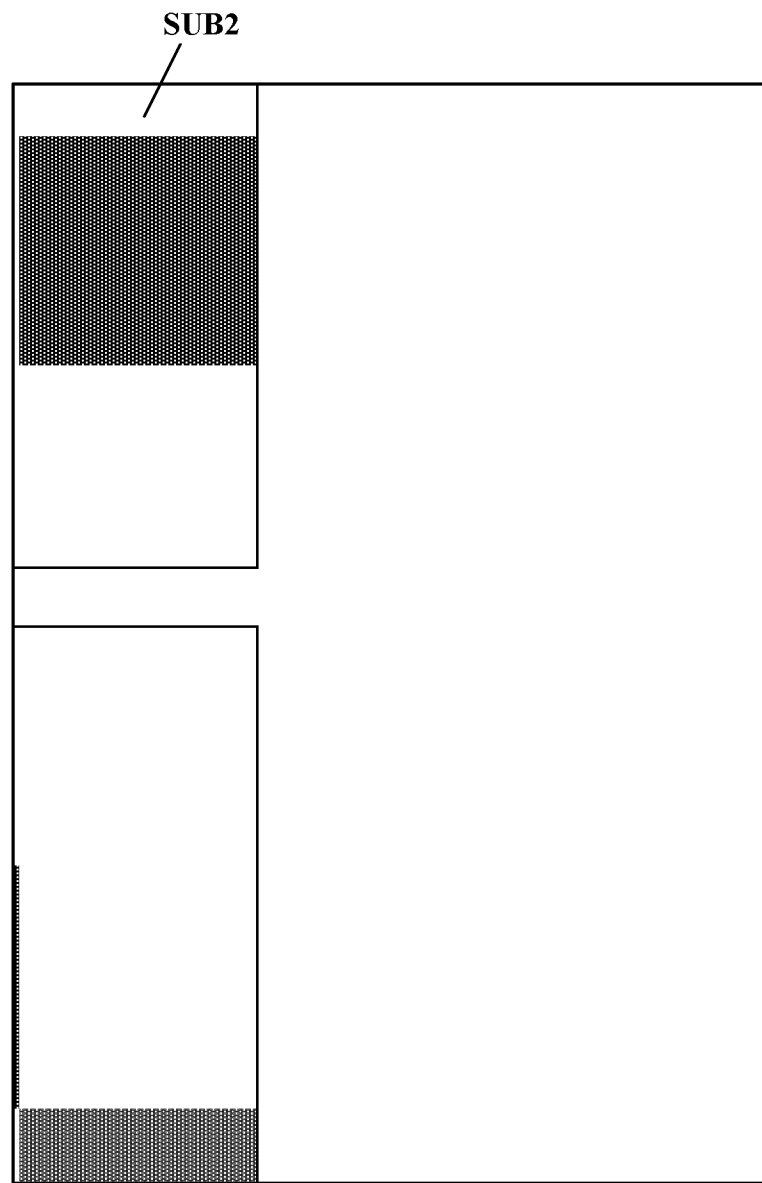


FIG. 16G

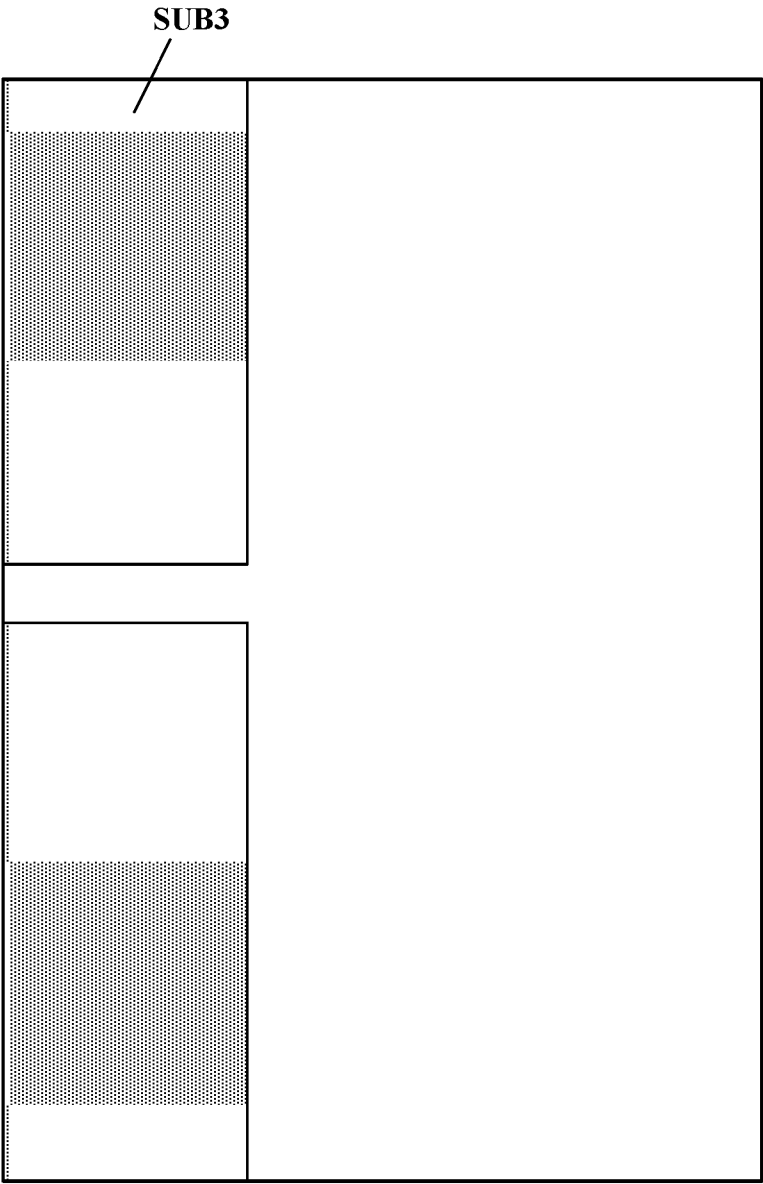


FIG. 16H

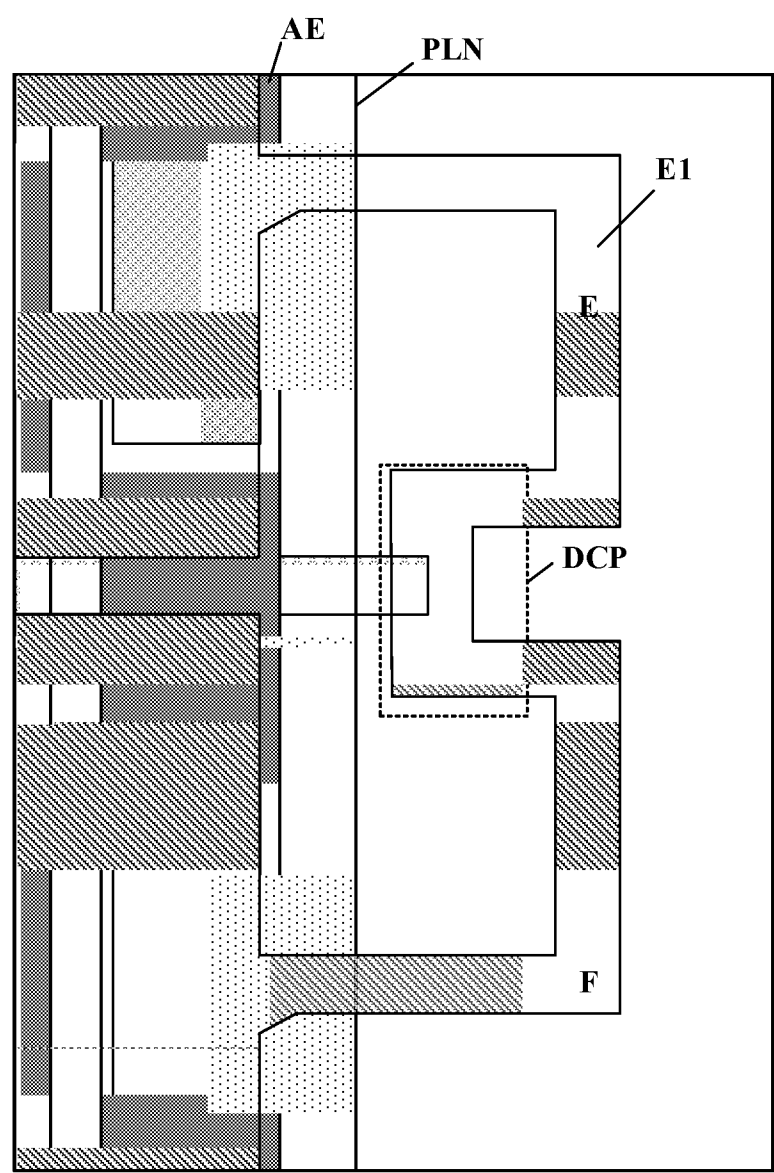


FIG. 17A

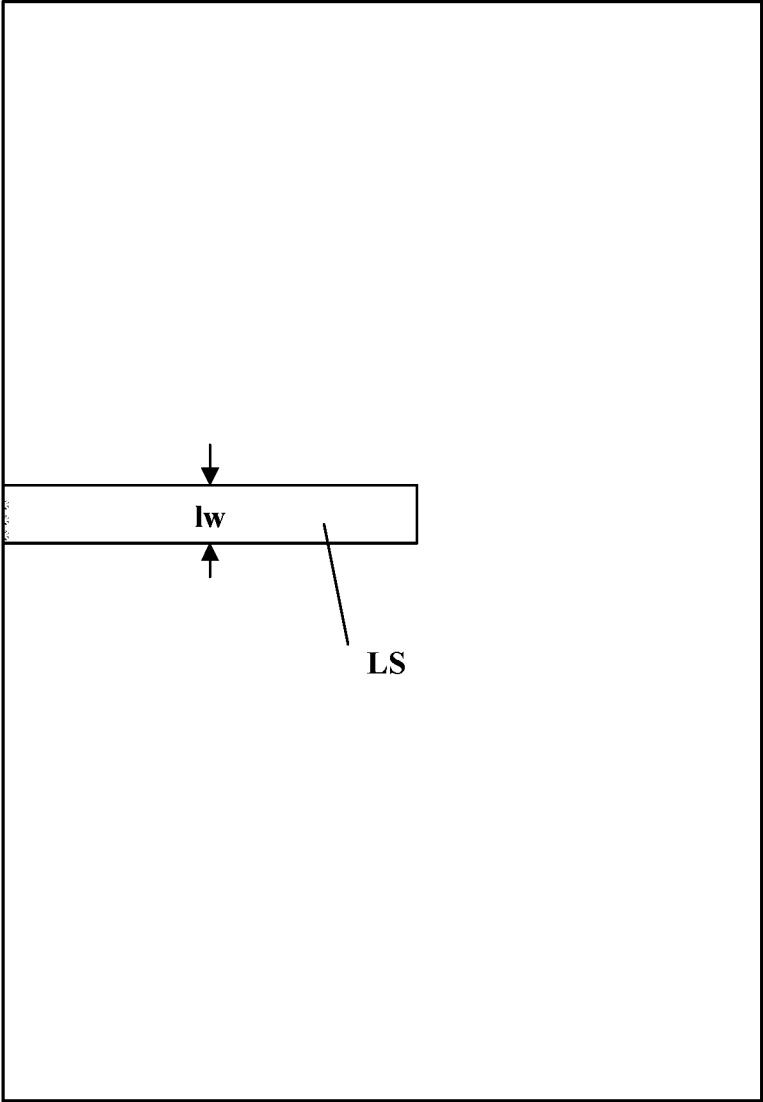


FIG. 17B

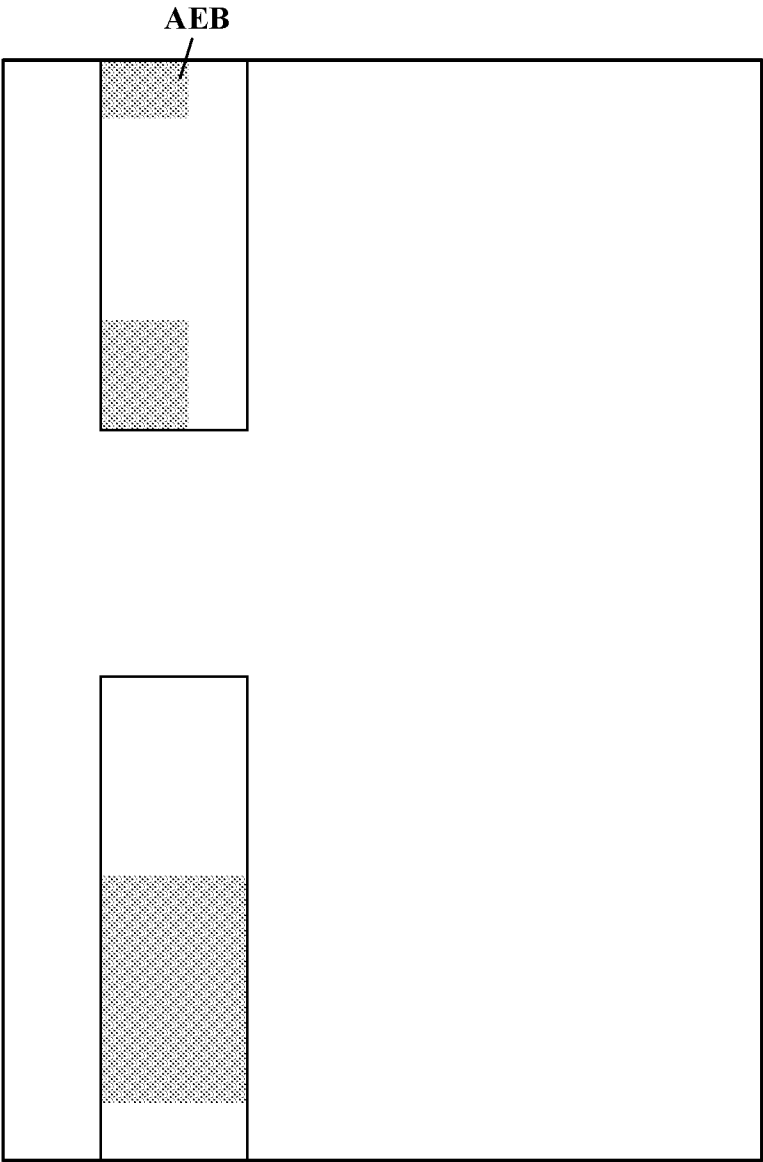


FIG. 17C

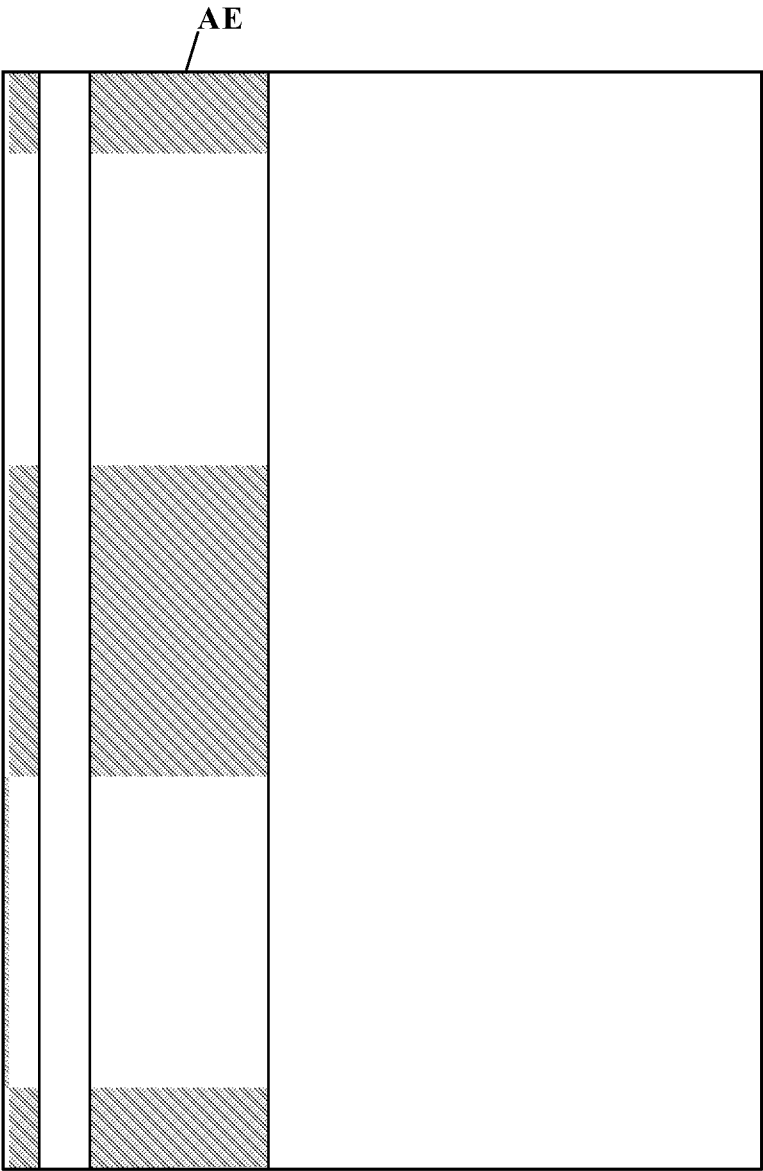


FIG. 17D

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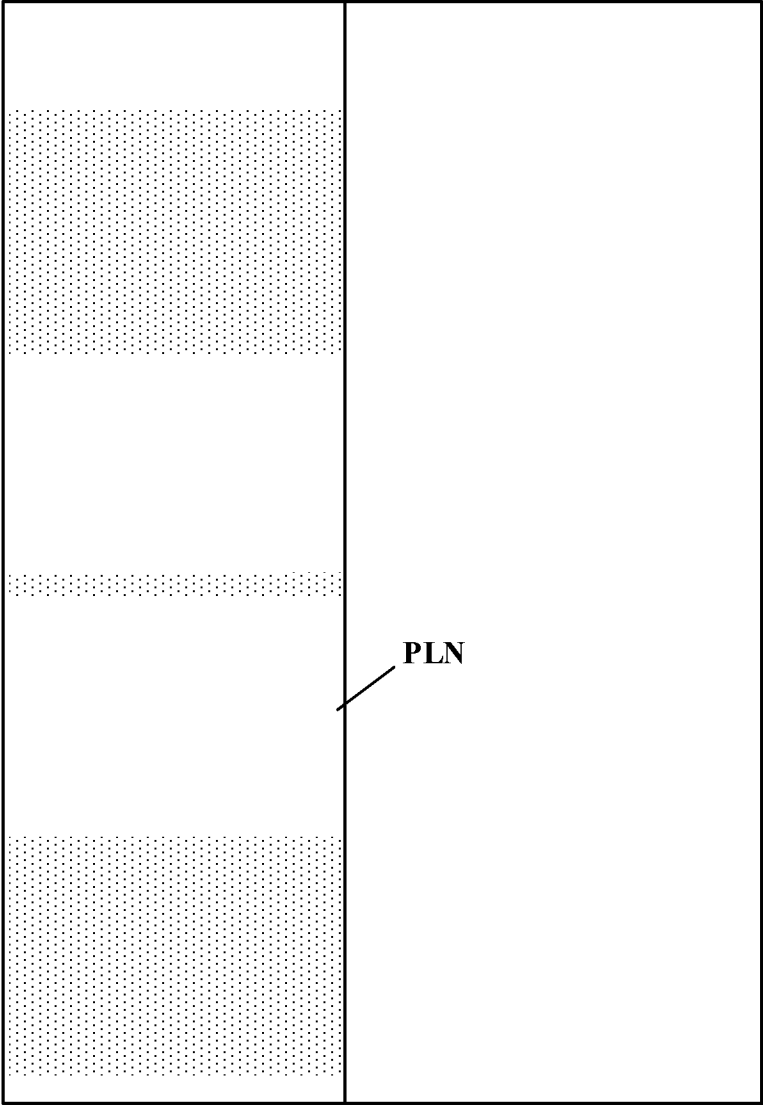


FIG. 17E

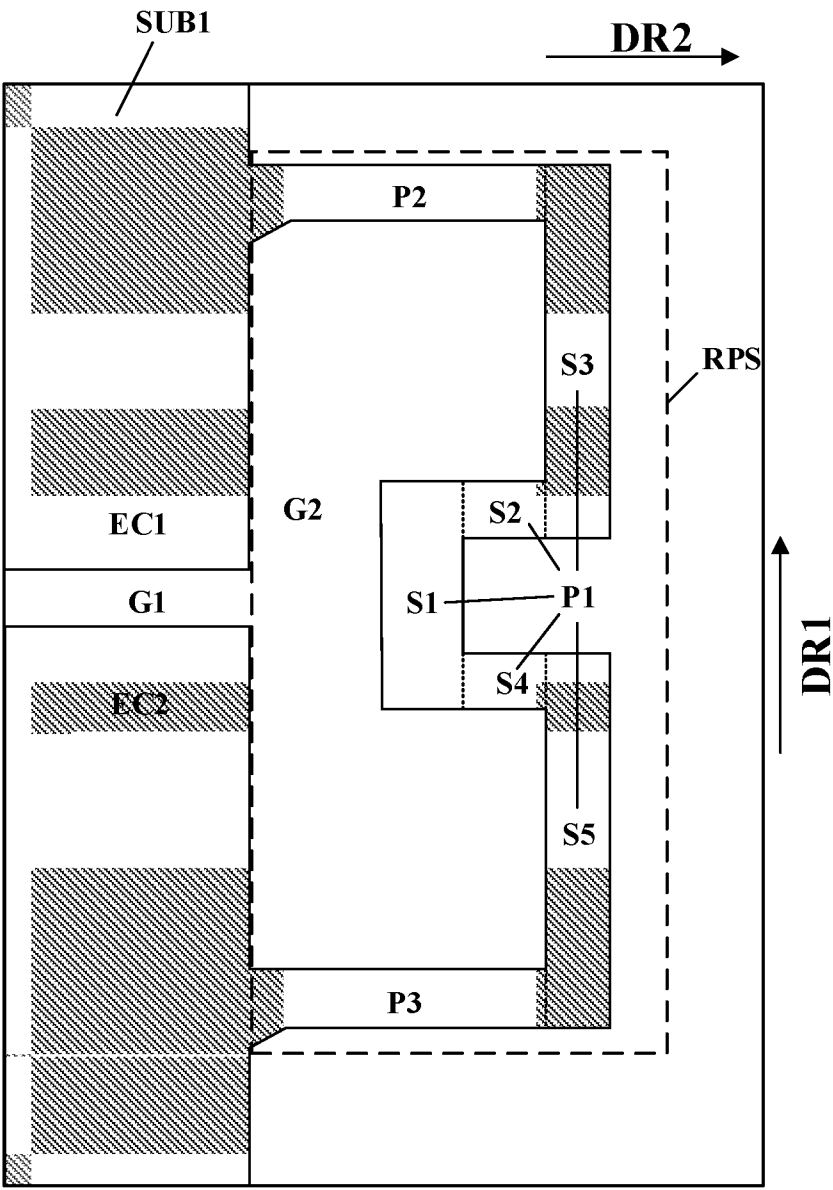


FIG. 17F

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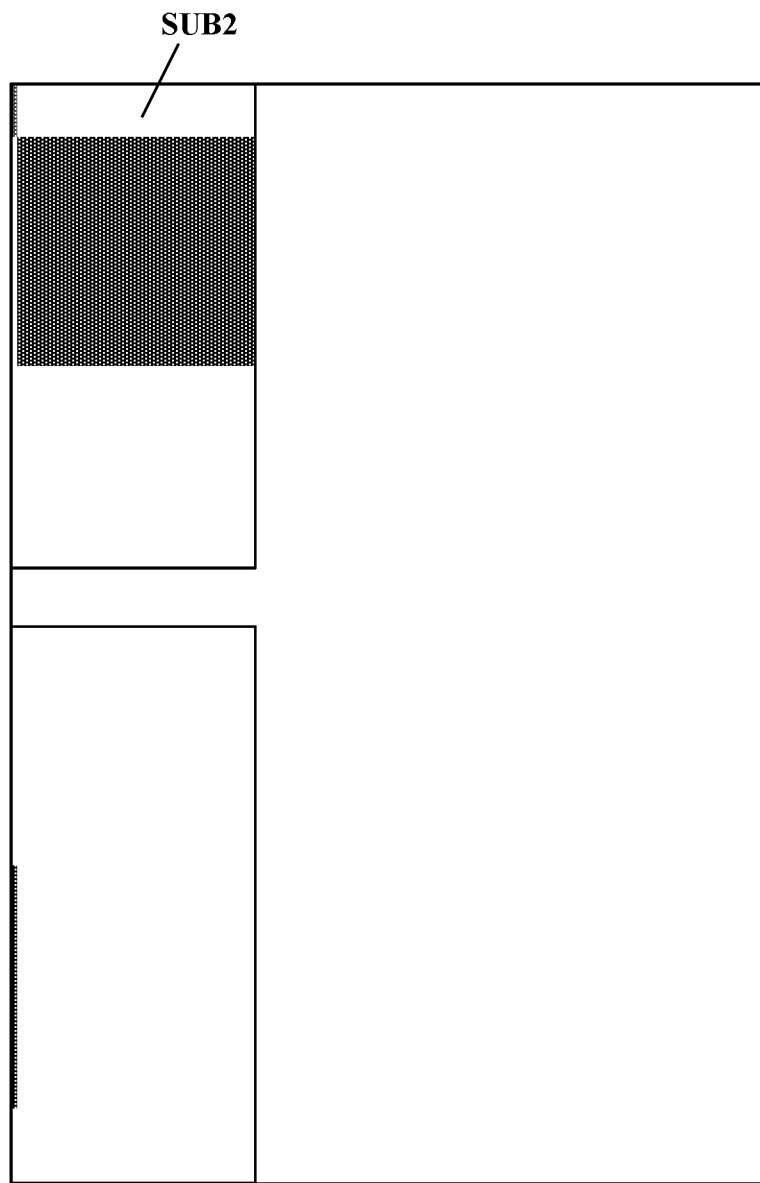


FIG. 17G

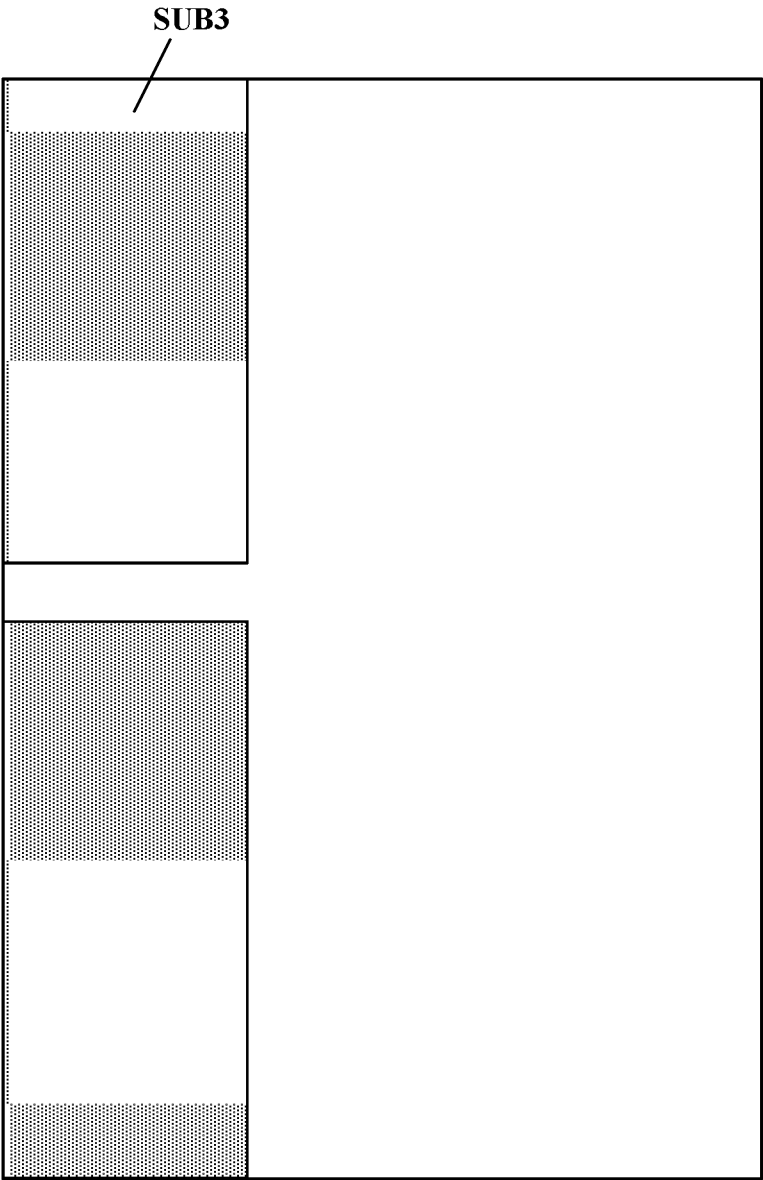


FIG. 17H

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2023/070336

A. CLASSIFICATION OF SUBJECT MATTER

H10K50/813(2023.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H10K,H01L,G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

VEN, CNABS, CNTXT, WOTXT, EPTXT, USTXT, CNKI, IEEE: display, panel, electrode, anode, repair, connect, laser, subpixel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 111384113 A (LG DISPLAY CO., LTD.) 07 July 2020 (2020-07-07) description, paragraphs [0043]-[0156], and figures 1-8E	1-20
X	CN 104183621 A (SAMSUNG DISPLAY CO., LTD.) 03 December 2014 (2014-12-03) description, paragraphs [0071]-[0233], and figures 1-43	1-20
A	US 2015294618 A1 (SAMSUNG DISPLAY CO., LTD.) 15 October 2015 (2015-10-15) the whole document	1-20
A	US 2016204181 A1 (SAMSUNG DISPLAY CO., LTD.) 14 July 2016 (2016-07-14) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“D” document cited by the applicant in the international application

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 March 2023

Date of mailing of the international search report

22 March 2023

Name and mailing address of the ISA/CN

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Telephone No. (+86) 010-53961457

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2023/070336

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	111384113	A	07 July 2020	US	2022123069	A1	21 April 2022
				US	2020212131	A1	02 July 2020
				US	11244987	B2	08 February 2022
				KR	20200080896	A	07 July 2020
CN	104183621	A	03 December 2014	US	2014346475	A1	27 November 2014
				US	9911799	B2	06 March 2018
				EP	2806458	A2	26 November 2014
				EP	2806458	A3	11 March 2015
				EP	2806458	B1	04 July 2018
				JP	2014228867	A	08 December 2014
				JP	6573753	B2	11 September 2019
				KR	20140137272	A	02 December 2014
				TW	201501289	A	01 January 2015
US	2015294618	A1	15 October 2015	KR	20150117358	A	20 October 2015
				KR	102152950	B1	08 September 2020
				US	9286832	B2	15 March 2016
US	2016204181	A1	14 July 2016	KR	20160087458	A	22 July 2016
				KR	102284142	B1	30 July 2021
				US	9520457	B2	13 December 2016