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(54) IMPROVEMENTS IN OR RELATING TO BINARY DATA STORE READ OUT CIRCUITS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The invention relates to binary data store read out circuits, especially for stores whose data evaluation is effected at a node point formed by the source electrodes of two switching transistors of a flip-flop stage, said flip flop stage comprising two arms each containing a load transistor and a switching transistor, all in the form of MOS-transistors, for the amplification of the read-out signals supplied by two portions of a bit line of the store, so that a separate evaluation flip flop stage is provided for each bit line of the store, and all the nodal points connected to a common function generator, which supplies a voltage to the nodal point at the beginning of a read-out cycle to charge the associated line portions and so bring the node point to a given level, and for subsequent evaluation of the read-out signals on the bit line the nodal point is then discharged in such manner that any selected flip-flops trigger into a state governed by the read-out signal on the bit lines.

In order to evaluate the read-out signals of dynamic MOS-stores, it is known to divide each bit line into two portions, and to arrange a read-out amplifier circuit designed as flip-flop stage between the two portions (see for example the publication in "IEEE Journal of Solid-State Circuits, Vol. SC7, No. 5, October, 1972, pages 336 to 340). A read-out amplifier circuit of this type is constructed in the manner of a keyed flip-flop stage. The fundamental properties of such known read-out amplifier circuits consist in the obtainable symmetry, the low degree of dependence upon parameter fluctuations, and the automatic regeneration of the stored signals. Read-out amplifier circuits of this type are particularly suitable for MOS-stores in which individual one-transistor storage cells are used.

Further development of MOS-store technology has been accompanied by a constant increase in the storage density available per storage module. This in turn leads to smaller read-out signals, and more heavily fluctuating component parameters. A more suitable evaluation circuit arrangement for read-out signals from MOS-stores of this type is an amplifier circuit such as described, for example, in "IEEE Journal of Solid-State Circuits Vol. SC8, No. 5, October, 1973, pages 310 to 318 and in "IEEE Journal of Solid-State Circuits, Vol. 9, No. 2, April 1974, pages 49 to 54. In this read-out amplifier circuit the load transistors of the flip-flop merely serve to pre-charge the portions of the bit lines at the connection points between the associated load transistor and switching transistor. During the evaluation process of a read-out signal, the load transistors remain blocked. If a signal voltage has set up on the portions of a bit line following the read-out of an item of information from a storage cell, then means must be provided to slowly reduce the voltage level then present at the connection point between the source electrodes of the switching transistors in order to ensure that only one of the switching transistors is rendered conductive, namely the transistor whose sink electrode is connected to the read-out signal. With this mode of operation the amplification of the flip-flop is very considerable, and fluctuations in the geometry of the transistors and the capacitances of the bit line have virtually no influence.

However a disadvantage of this read-out amplifier circuit consists in the relatively long period involved in each evaluation-time cycle. Therefore attempts have been made to reduce the voltage level required at the con-

nection point of the source electrodes of the switching transistors in accordance with an optimum curve calculated to be such that one of the switching transistors is exactly at the blocking limit, or alternatively operates in a weakly conductive state in which the current is constant. This measure serves to reduce the resultant evaluation time requirement to some extent, although it is still relatively long. This is particularly true in cases where, for reasons of space economy, a plurality of read-out amplifier circuits of a storage module are commonly connected to a common circuit arrangement which serves to set up the voltage at the connection point of the source electrodes of the switching transistors, i.e. to the node point. The relatively significant variations between threshold voltages of the switching transistors of non-adjacent flip-flops then necessitate a substantial increase in the evaluation time to ensure reliable operation.

One object of the present invention is to provide a read-out circuit arrangement having a function generator for the production of the voltage across the node point of such stores, to which a plurality of flip-flop stages may be connected for the evaluation of respective read-out signals, which function generator operates in such manner that the plurality of flip-flops connected to the node point do not influence the evaluation time of read-out signals.

The invention consists in a binary data store read-out circuit in which a common function generator is provided for the production of a predetermined voltage level at a node point which is formed by the source electrodes of MOS switching transistors each of a plurality of flip-flop stages having two arms which each comprise a load transistor and a switching transistor, each of which stages serves for the amplification of read-out signals supplied by respective bit line portions of the store, each arm of each flip-flop stage having the junction point of its load transistor and switching transistor connected to a respective portion of a respective bit line of the store, and the curve of the voltage waveform supplied to the node point is such that at the beginning of the cycle of the read-out process the node point is charged, the evaluation of the read-out signals on the bit line portions subsequently being effected by an evaluation discharge that is effected in such manner that each flip-flop stage triggers into a state govered by any read-out signal on its respective bit line portions, and in which a pre-discharge circuit is provided in said function generator to effect a preparatory discharge (pre-discharge) of the nodal point in a time zone between the charging and the subsequent evaluation discharging of the node point, so that as the potential changes at the node point the switching transistors of each flip-flop stage connected to said node are rendered conductive, and the associated portions of the bit lines are set at the voltage level which prevails at the node point, as modified in each case by the respective threshold voltage of the associated switching transistor.

Thus this pre-discharging of the node point ensures that the respective portions of the bit lines are set at a voltage level which already takes into consideration the threshold voltages of the respective switching transistors of the flip-flop stages. Any change in the voltage at the node point during the evaluation process then influences all the flip-flop stages in the same way, and the fact that differing threshold voltages are exhibited by switching transistors of the flip-flop stages no longer has any adverse influence.

Preferably the preliminary discharge circuit consists of two transistors connected in parallel and operated by respective timing signals, the two transistors being mutually different in their dimensions so that the timing signals can be timed to ensure that the discharge of the node point only takes place to such an extent that all the portions of the bit lines can be individually set to the change in the node point voltage which is governed by the threshold voltages, despite differing threshold voltages of the switching transistors.

The invention will now be described with reference to the drawings, in which;-

Figure 1 is a simplified schematic circuit diagram of one exemplary embodiment of the invention, showing the basic interconnection of a read-out amplifier circuit with three flip-flop stages and a function generator;

Figure 2 illustrates details of the function generator and its pre-discharge circuit as used in the embodiment shown in Figure 1;

Figure 3 illustrates details of the particular circuit arrangement for the production of the timing signals for the pre-discharge circuit in the exemplary embodiment shown in Figure 1;

Figure 4 is a set of explanatory waveforms indicating the mode of operation of the exemplary read-out amplifier circuit shown in Figure 1; and

Figure 5 is a graph plotting the voltage of the timing signals supplied to the pre-discharge circuit against time.

The exemplary embodiment of read-out amplifier circuit illustrated in Figure 1 consists of a number of individual flip-flop stages FF and a common function generator FG, which contains a pre-discharge circuit.

The details of one flip-flop FF are shown, in full, and it will be seen that each consists of two mutually parallel arms, each comprising a load transistor and a switching transistor.

Thus, one arm contains a load transistor TL1 and a switching transistor TS1, whilst the second arm contains a load transistor TL2 and a switching transistor TS2. The connection point between each of the switching transistors and its associated load transistor is connected to a portion of a bit line, the portion BL of the bit line being connected to a connection point $p1$ between load transistor TL1 and switching transistor TS1, whereas the portion BR of the bit line is connected to connection point $p2$ between load transistor TL2 and switching transistor TS2. The connection points $p1$ and $p2$ are connected via a transistor TO, which acts as a balancing transistor. The connection point between the source electrodes of the switching transistors TS1 and TS2 forms a node point K. The load transistors TL1 and TL2 are operated with the aid of a timing signal S2, whereas the balancing transistor TO is operated with the aid of a timing signal S3. A fixed supply voltage VDD is connected to the junction of the load transistors TL1 and TL2.

The node point K is connected to a plurality of flip-flops, which are all constructed in the same way. However, these flip-flops will inevitably differ in some extent in respect of the properties which the particular switching transistors possess, as it is not possible to construct all switching transistors of the flip-flops in such a way that they all possess precisely the same threshold voltage. Therefore the function generator FG, which is connected to the node point K, is constructed in such a way that the voltage which it feeds to the node point K influences each of the flip-flops FF in such manner that the differing threshold voltages of the switching transistors of the various flip-flops do not influence the evaluation process.

By reference to Figure 4 it will now be explained how it is possible to avoid any adverse influence of the differing threshold voltages of the switching transistors. It has been assumed that the transistors are n-channel transistors, and therefore the voltage waveforms given in Figure 4 have positive voltages relative to a reference potential such as earth.

Before it is possible to analyse a read-out signal connected to the bit line portions BL and BR, the read-out amplifier circuit must be pre-charged. For this purpose the balancing transistor TO is rendered conductive by a signal pulse S3. The load transistors TL1 and TL2 can also be brought into the conductive state by the connection of a timing signal pulse S2. The node point K is then at a voltage V3, which in this case is still low. Under these circumstances the bit line portions BL and BR are charged to a voltage level of YDD-VT, where VT is the particular threshold voltage of the load transistors TL1 and TL2 of one flip-flop. It is also possible to charge the bit line portions BL and BR via auxiliary transistors (not shown) for example by applying a signal pulse SO (Figure 4, first line) being connected to control these transistors. It is also possible to charge the bit line portions BR and BL to another voltage level, e.g. VDD-2.VT. Since the bit line portions BR and BL can be charged via separate auxiliary transistors and/or via the load transistors TL, the timing signal pulse S2 which occurs during the pre-charging of the bit line portions is drawn in broken line fashion in Figure 4. In this phase the switching transistors TS1 and TS2 are likewise in the conductive state. The node point K is also charged to a level of substantially V3 = VDD - VT - (VT + Δ VT max), where ΔVT max is the maximum difference between threshold voltages of all the switching transistors which are connected to the node point K. The duration of the pre-charging phase is from the time $t1$ to $t2$. During this time the node point K is charged.

At the end of the pre-charging phase, at the time $t2$, the pre-charging signal pulse SO or S2 is disconnected, so that the load transistors TL1 and TL2 assume the blocking state.

The pre-charging is followed by the read-out preparation period, which is composed of two time zones, one lasting from $t2$ to $t3$ and the second from $t3$ to $t4$.

During the time zone from $t2$ to $t3$ the timing signal pulse S3 is still connected to the balancing transistor TO to hold the latter conductive so that the bit line portions BL and BR for any flip flop remain connected to one another. Now the voltage at the node point K begins to reduce, in accordance with the lowest curve in Figure 4, under the influence of a pre-discharge circuit in the function generator FG. As the switching transistors TS1 and TS2 are in the conductive state, the voltage at the node point K passes via the switching transistors to the bit line portions BL and BR. These bit line portions BL and BR are now at a voltage equal to the node point voltage V3 plus VT min, where VT min is the lower threshold voltage of the switching transistors TS1 and TS2. Thus, voltages which are dependent upon the threshold voltage of the switching transistors are formed on the associated bit line portions BR and BL in each flip-flop. When a plurality of flip-flops comprising switching transistors of mutually different threshold voltages are connected to the node point, in accordance with the different threshold voltages of the switching transistors, different voltages will be set up on the respective bit line portions BR and BL of the various bit lines. The greater the threshold voltage of any particular switching transistor, the more positive is the voltage level at the corresponding bit line portions. This ensures that any chagne in the voltage at the node point K uniformly influ-

ences all the flip-flops. This means that the time of the triggering of the flip-flops is the same for all the flip-flops, and is no longer dependent upon the different threshold voltages of the individual switching transistors. The pre-discharge circuit modifies the voltage at the node point K by a quantity which is dependent upon the threshold voltages of the switching transistors, and which will expediently amount to approximately 1 volt.

During the time zone from $t3$ to $t4$ the timing signal pulse S3 is disconnected so that the balancing transistor TO is blocked. As a result the bit line portions BR and BL of each flip-flop are now isolated from one another. The reduction in the timing signal pulse S3 also results in the voltage of the bit line portions BR and BL being reduced by the parasitic capacitances of the balancing transistor T10. Consequently the switching transistors are safely blocked after the time $t4$.

After the time $t4$, the read-out process from a storage call commences. During the time zone from $t4$ to $t5$ an item of information is read out from a storage cell and accordingly a read-out signal Vsig is formed by the voltage difference between the two bit line portions. In Figure 4, this is indicated by two arrows in the time zone from $t4$ to $t5$ indicating the respective voltages VBL and VBR then standing at the respective bit line portions BL and BR. It will be seen that there is a voltage difference between the bit line portions BR and BL. The switching transistors TS1 and TS2 of the flip-flops continue to be blocked.

At the time $t5$ the evaluation process commences. For this purpose, a signal pulse S1 causes that part of the function generator FG effective to discharge the node point K to be connected, and discharging is carried out in accordance with the lowermost curve in Figure 4. Thus, initially the voltage level at the node point K is reduced very rapidly. The rapid reduction of the voltage level at the node point K renders conductive that particular switching transistor, in the selected flip-flop FF, whose drain electrode is connected to the line portion whose voltage changed on the read-out of the information. If it is assumed that a storage cell which is connected to the bit line portion BL of the flip-flop illustrated in full detail is read out, the switching transistor TS1 is rendered conductive. Thus a current can flow through this switching transistor (the currents J12 and J22 through the switching transistors TS1 and TS2 respectively are illustrated in Figure 4).

During the time $t6$ to $t7$, the voltage level at the node point K is reduced only very slowly, and remains virtually constant. This process speeds up gradually, and in the exemplary embodiment it takes place in such a way that the previously blocked switching transistor is also rendered conductive again. In the quoted example, this is the switching transistor TS2. This can be seen from the curve of the voltages VBL and VBR, and from the currents J12 and J22 in Figure 4. However, the curve of the reduction in the voltage level at the node point K is now such that in spite of differences in the geometry of the switching transistors and the capacitances of the bit line portions, thus even under the most unfavourable conditions, the flip-flop nevertheless reaches its trigger point again, and the switching transistor TS2 is blocked again, at a time $t8$. Accordingly the current through the switching transistor TS2 reduces again, whereas the voltage difference on the bit line portion increases rapidly.

At a time $t9$, the timing signal pulse S2 is connected to the load transistors TL1 and TL2, to render them conductive. The result is that the bit line portions BR and BL are set to the O-level and 1-level respectively, whilst the discharge of the node point K is further accelerated. The node point continues to be discharged until a time $t10$. On the bit line portion, e.g. BR, on which the voltage change occurred due to the information read-out, a level has set up which can be employed to regenerate the read-out storage cell.

At the time $t10$ the timing signal pulse S1 is disconnected, and thus the function generator FG is cut off from the flip-flop FF. At a time $t11$ the read-out and regenerating processes are terminated.

The function of the read-out amplifier circuit has been described on the basis of a discharge curve which is extremely advantageous. Naturally the evaluation discharge of the node point K can also take place differently, e.g. in the manner described in the above quoted publications. The evaluation discharge of the node point does not in fact affect the preliminary discharge of the node point K which is effected in the time zone between $t2$ and $t3$. Furthermore, the operation of the read-out amplifier circuit has been described in detail with reference to the specific flip-flop shown in full detail. It has already been stated that the node point K is connected to a plurality of flip-flops FF, all constructed in accordance with the flip-flop FF shown in detail in Figure 1, and all these flip-flops are operated in precisely the manner explained with reference to the flip-flop FF shown in detail in Figure 1.

Figure 2 illustrates a preferred embodiment of the function generator FG, with a pre-discharge circuit VR, which is active in the time zone from $t2$ to $t3$ and an evaluation discharge circuit ES, which is active in the time zone from $t5$ to $t10$. The discharge circuit ES in this embodiment is in the form of a circuit arrangement which has already been described in detail in our Patent United

Kingdom (Serial No. 1587129), Specification No. (Application No. 21585/77), so that it need only be discussed briefly here.

The pre-discharge circuit VR of the present invention is constructed from two transistors TR1 and TR2, connected in parallel with their controlled paths located between the node point K and a fixed supply potential VSS. The control input of the transistor TR1 is connected with a first timing signal pulse S10, and the control input of the transistor TS2 is connected with a second timing signal pulse S11, which occur in the time zone from $t2$ to $t3$. The transistor TR2 is very briefly rendered conductive by the timing signal pulse S11, in order to speed up the discharge process at the beginning of the preliminary discharge. The timing signal pulse S10, which is connected simultaneously to the timing signal pulse S11, has a longer duration, and brings about a further discharge of the node point K. However, as the transistors TR1 and TR2 are differently dimensioned, the influence exerted on the discharge of the node point K is different. The transistor TR1 is smaller than the transistor TR2 in this embodiment, the ratio W to L (with to length of the channel) being approximately 200 for the transistor TR2, but only 40 for the transistor TR1, for example. It will thus be clear that through the selection of the ratio W:L of the transistors TR1 and TR2, and by the time duration of the timing signal pulses S10 and S11 it is possible to influence the degree of the pre-discharge of the node point K in the desired manner. The timing signal pulse S11 can be connected for 20-30 ns, for example, and the timing signal pulse S10 applied for 40 to 50 ns.

The evaluation discharge circuit ES consists of a circuit arrangement with the aid of which the node point K is discharged very rapidly in the time zone from $t5$ to $t6$, and of a circuit arrangement which undertakes the remainder of the discharge of the node point K. The rapid discharge is carried out with the aid of the transistors TR6 and TR7, together with a capacitor C. The control input of the transistor TR6 is connected with a signal $\overline{CE}$, i.e. a signal is applied when the module is not selected, and thus the module is not fed with the module selector signal CE. For such time as the signal $\overline{CE}$ is applied, the transistor TR6 is conductive, and the connection point $p5$ can charge to the voltage of the node point K. At the beginning of the evaluation process, the timing signal pulse S1 renders the transistor TR7 conductive, whereas the transistor TR6 is blocked. As a result, the capacitor C can discharge very rapidly, and the voltage at the node point K changes correspondingly rapidly.

The further discharge of the node point K is carried out with the aid of transistors TR3, TR4 and TR5, together with delay circuits VZ1 and VZ2. The timing signal pulse S1 is directly fed to the transistor TR3, and brings the latter into the conductive state. As a result the node point K can discharge via the transistor TR3. At the end of a delay period, determined by the delay circuit VZ1, the transistor TR4 is also rendered conductive to bring about an acceleration of the discharge process of the node point K. At the end of a further delay period, produced by the delay circuit VZ2, the transistor TR5 is finally also rendered conductive.

All three transistors TR3, TR4 and TR5, are then conductive together, and the node point K is discharged relatively rapidly in the zone from $t9$ to $t10$. The shape of the discharge curve can be determined by the dimensioning of the transistors TR3, TR4 and TR5, and the delay times of the delay circuits VZ1 and VZ2.

Finally, Figure 3 illustrates a circuit arrangement with the aid of which the timing signal pulses S10 and S11 are produced. This circuit arrangement consists of a diode D1 and transistors TR10 to TR19. The timing signal pulses S11 and S10 are triggered by a module selector signal pulse CE. Here the circuit arrangement operates in such a way that the timing signal pulses S10 and S11 initially follow the module selector signal CE, whereupon, however, they assume a lower amplitude value than that of the module selector signal pulse CE. For such time as the module selector signal pulse CE is not applied, whereas $\overline{CE}$ is applied, the transistor TR13 is conductive, and the connection point $p10$ can charge. The outcome is that the transistors TR11 and TR15 are rendered conductive. On the other hand, the transistors TR18 and TR12 are blocked. Since, however, the module selector signal CE is not yet connected to the transistors TR19 and TR11, and thus the potential at these points is zero, the potential of the signal pulses S10 and S11 is also zero. If the module selector signal CE is now applied, initially the timing signal pulses S11 and S10 directly follow the module selector signal CE. However, as the transistor TR10 is simultaneously rendered conductive by the module selector signal, the connection point $p10$ discharges. The outcome is that after a certain length of time the transistor TR15 becomes blocked, whereas the transistor TR14 is rendered conductive, particularly when the transistor TR16 is brought into the conductive state. The transistor TR18 then becomes conductive, whereas the transistor TR19 is blocked. The timing signal pulse S11 therefore returns to its commencing value again. The transistor TR11 remains conductive, although it limits the amplitude of the timing signal pulse S10. Not until a signal pulse $\overline{S3}$ is connected to the transistor TR12, thus at the time $t3$, said latter transistor is opened and the signal

pulse S10 returns to its commencing state.

Figure 5 illustrates the relationships between the module selector signal CE and the timing signal pulses S10 and S11. Here it can be seen that the timing signal pulses S10 and S11 initially directly follow the module selector signal CE, but after a length of time governed by the dimensioning of the circuit arrangement, no longer maintain the rise of the module selector signal CE. It can also be seen that the timing signal pulse S11 disappears earlier than the timing signal pulse S10.

One advantage of a function generator constructed in accordance with the invention is that, employing the pre-discharge circuit, the node point K is pre-discharged, prior to the actual discharge process, during the time of the evaluation of a read-out signal, and in this way the influence of the various threshold voltages of the switching transistors of the flip-flops upon the evaluation is substantially eliminated.

WHAT WE CLAIM IS:-

1. A binary data store read-out circuit in which a common function generator is provided for the production of a predetermined voltage level at a node point which is formed by the source electrodes of MOS switching transistors of each of a plurality of flip-flop stages having two arms which each comprise a load transistor and a switching transistor, each of which stages serves for the amplification of read-out signals supplied by respective bit line portions of the store, each arm of each flip-flop stage having the junction point of its load transistor and switching transistor connected to a respective portion of a respective bit line of the store, and the curve of the voltage waveform supplied to the node point is such that at the beginning of the cycle of the read-out process the node point is charged, the evaluation of the read-out signals on the bit line portions subsequently being effected by an evaluation discharge that is effected in such manner that each flip-flop stage triggers into a state governed by any read-out signal on its respective bit line portions and in which a pre-discharge circuit is provided in said function generator to effect a preparatory discharge (pre-discharge) of the nodal point in a time zone between the charging and the subsequent evaluation discharging of the node point, so that as the potential changes at the node point the switching transistors of each flip-flop stage connected to said node are rendered conductive, and the associated portions of the bit lines are set at the voltage level which prevails at the node point, as modified in each case by the respective threshold voltage of the associated switching transistor.

2. A read-out circuit with a function generator, as claimed in Claim 1, in which said pre-discharge circuit consists of a first transistor driven by a first timing signal pulse and a second transistor driven by a second timing signal pulse, said first and second transistors being connected in parallel, and the pre-discharging of the node point being influenced by the use of different dimensions for the first transistor and the second transistor, and by the shape of the respective timing signal pulses.

3. A read-out circuit with a function generator, as claimed in Claim 2, in which the first and second timing signal pulses are derived from a module selector signal in such manner that they initially follow the front flank of the module selector signal, but are limited to an amplitude lower than the amplitude of the module selector signal.

4. A read-out circuit with a function generator, as claimed in Claim 3, in which said second transistor has greater dimensions than the first transistor, and the second timing signal pulse is of a shorter duration than the first timing signal pulse.

5. A read-out circuit with a function generator as claimed in Claim 4, in which said pre-discharge circuit comprises a trigger circuit having a first arm containing a switching transistor and a load transistor that is driven by a negated module selector signal, a second arm which is feed-back coupled to the first arm thereof, which second arm contains a switching transistor and a load transistor driven by the module selector signal, a first series arrangement connected to a first output of the trigger circuit, and consisting of a transistor driven by the module selector signal, together with a diode, a second series arrangement comprising a first transistor whose control input is connected to the first output of the trigger circuit, and which is supplied at an electrode of the controlled path with the module selector signal, a second transistor which is driven by the one timing signal pulse, a third series arrangement comprising a first transistor whose control input is connected to the first output of the trigger circuit and is supplied at an electrode of the controlled path with the module selector signal, said third series arrangement further comprising a second transistor whose control input is connected to a second output of the trigger circuit, the first timing signal pulse being withdrawn from the connection point of the transistors of the second series arrangement, and the second timing signal pulse being withdrawn from the connection point of the transistors of the third series arrangement.

6. A binary data store read-out circuit substantially as described with reference to Figures 1, 2 and 3.

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1587130 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

Fig.1

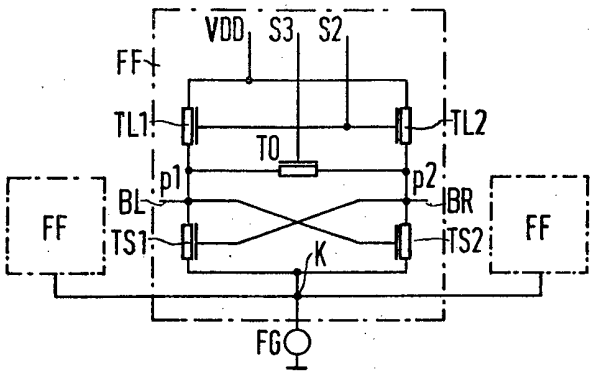


Fig.2

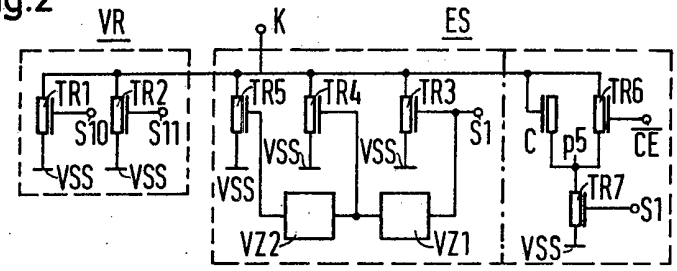
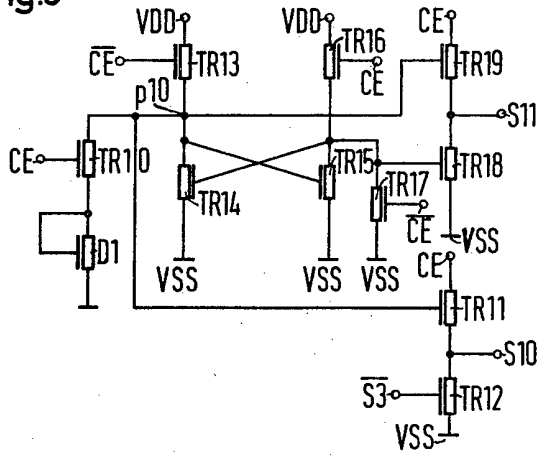
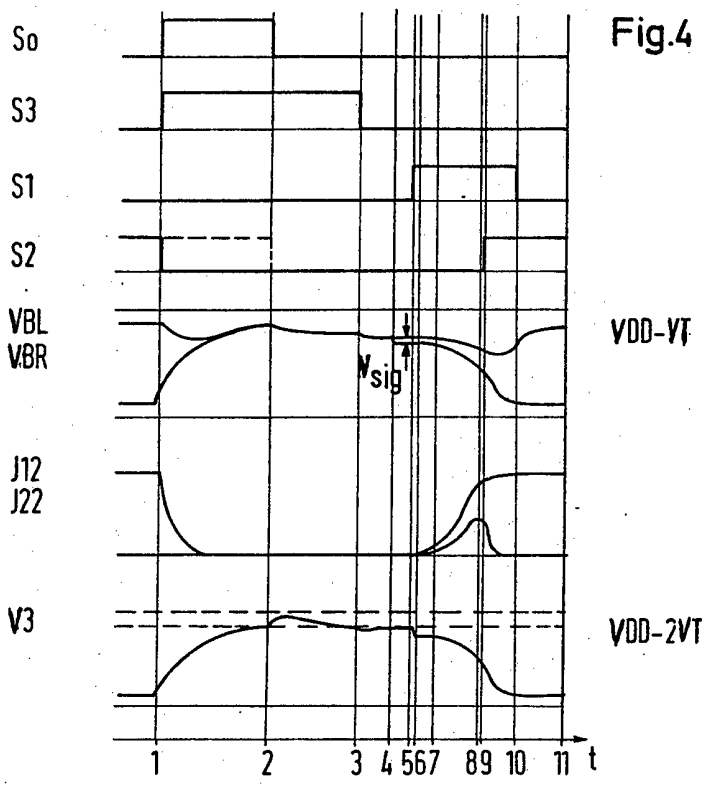


Fig.3

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S3
S1
S2
VBL
VBR
J12
J22
V3
VDD-VT
VDD-2VT
Vsig
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3
4
5
6
7
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9
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11
t

Fig.4

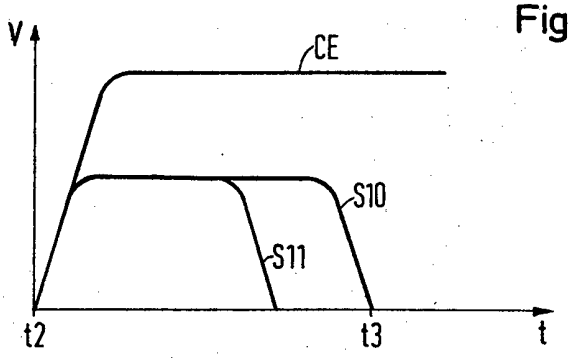
V
CE
S10
S11
t2
t3
t

Fig.5