(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 May 2012 (24.05.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/065485 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/CN2011/080671

(22) International Filing Date:
12 October 2011 (12.10.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201010552466.4 19 November 2010 (19.11.2010) CN

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: LDMOS DEVICE AND METHOD FOR FABRICATING THE SAME

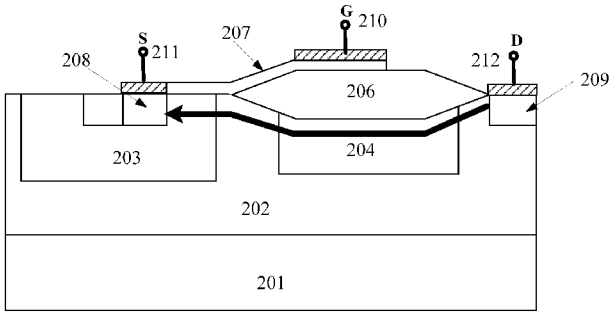


Figure 4

(57) **Abstract**: An LDMOS device and a method for fabricating the same are disclosed in embodiments of the present invention. The device includes: a substrate including an epitaxial layer and a well region located in a surface of the epitaxial layer; a source region located in the well region, and a drain region located in the epitaxial layer; a first region and a second region located in the surface of the epitaxial layer and having doping states different from a doping state of the epitaxial layer, where the first region and the second region are located in a drift region between the source region and the drain region, and have different doping states; a field oxide layer located above the first region and the second region; and a gate region located on the well region and the field oxide layer. In the present invention, by replacing the drift region with only one doping state in the prior art with the first region and the second region having different doping states, the doping states of the first region and the second region can be adjusted according to the requirements for the breakdown voltage and the on-resistance, so that the on-resistance is further decreased and the power consumption of the device is reduced while a high breakdown voltage is ensured.

WO 2012/065485 A1

LDMOS DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS REFERENCE TO RELATED ART

[0001] This application claims the benefit of priority to Chinese Patent Application No.201010552466.4, entitled "LDMOS DEVICE AND METHOD FOR FABRICATING THE SAME", filed on November 19, 2010 with State Intellectual Property Office of PRC, which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of semiconductor fabrication, and more particular to an LDMOS device and a method for fabricating the same.

BACKGROUND OF THE INVENTION

[0003] With increasing development of semiconductor technique, Lateral Double-diffuse MOS (LDMOS) device is used more and more widely. At the same time, higher requirement has been put forward for the performance of the LDMOS device, and more and more attention has been paid to the issue of reducing the power consumption of the device as much as possible while ensuring a high breakdown voltage.

[0004] An existing method for fabricating an LDMOS device is shown in Figures 1-3, and the method includes the following steps:

[0005] Step 1: referring to Figure 1, providing a substrate, where the substrate includes an epitaxial layer 101 and a field oxide (FOX) layer 102 located on the epitaxial layer 101,

the field oxide layer 102 is formed by local oxidation of silicon (LOCOS), and the method is described by taking a N-type epitaxy as an example;

[0006] Step 2: referring to Figure 2, forming a well region 103 (P well) in a surface of the epitaxial layer 101, depositing poly-silicon on the epitaxial layer 101 and the field oxide layer 102 and forming a gate region 104; and

[0007] Step 3: referring to Figure 3, forming a (N-type doped) source region 105 in a surface of the well region 103, and forming a (N-type doped) drain region 106 in the surface of the epitaxial layer 101.

[0008] A sectional view of the LDMOS device in the prior art is shown in Figure 3, in which a drift region exists between the drain region 106 and the source region 105, and the drift direction of the carriers is indicated by the arrow in Figure 3.

[0009] Owing to the structure of the LDMOS device, the LDMOS device has a good characteristic of short groove and operates generally in the saturation region, which means a substantially constant working current. Thus, the power consumption of the LDMOS device depends mainly on the on-resistance of the device, and decrease in the on-resistance of the device helps to reduce the power consumption. However, for a power MOS device, the increase in the breakdown voltage and the decrease in the on-resistance are conflicting: if the breakdown voltage is to be increased, the on-resistance will be increased, and if the on-resistance is to be decreased, the requirement for a high breakdown voltage can not be satisfied.

SUMMARY OF THE INVENTION

[0010] Embodiments of the present invention provide an LDMOS device and a method for fabricating the same, which ensure a high breakdown voltage while further decrease the on-resistance and reduce the power consumption of the device in comparison with prior art.

[0011] To achieve the above objects, the embodiments of the present invention provide

the following technical solutions.

[0012] An LDMOS device, including:

a substrate including an epitaxial layer and a well region located in a surface of the epitaxial layer;

a source region located in the well region, and a drain region located in the epitaxial layer;

a first region and a second region located in the surface of the epitaxial layer and having doping states different from a doping state of the epitaxial layer, where the first region and the second region are in a drift region between the source region and the drain region, and have doping states different from each other;

a field oxide layer located above the first region and the second region; and

a gate region located on the well region and the field oxide layer.

[0013] Preferably, the first region and the second region are arranged as being perpendicular to a drift direction in a plane of the substrate.

[0014] Preferably, the first region and the second region have opposite conducting types.

[0015] Preferably, the second region has a same conducting type as that of the epitaxial layer and has a doping concentration greater than that of the epitaxial layer.

[0016] Preferably, the first region and the second region have substantially a same doping concentration.

[0017] Preferably, the first region and the second region have a same depth.

[0018] Preferably, the first region is P-type doped, the second region is N-type doped, and the first region has a length less than that of the second region.

[0019] Preferably, the first region and the second region are sequentially formed by a selective epitaxial growth process.

[0020] Preferably, the first region and the second region are sequentially formed by ion implanting.

[0021] Embodiments of the present invention further discloses a method for fabricating an LDMOS, which includes:

providing a substrate, where the substrate includes an epitaxial layer and a well region located in a surface of the epitaxial layer;

forming a first region and a second region in the surface of the epitaxial layer, where the first region and the second region have different doping states;

forming a field oxide layer on the epitaxial layer above the first region and the second region; and

forming a gate region on the well region and the field oxide layer, forming a source region in the well region, and forming a drain region in the epitaxial layer, where the first region and the second region are located in a drift region between the source region and the drain region.

[0022] Compared with the prior art, the above technical solutions have the following advantages.

[0023] In the LDMOS device provided by the embodiments of the present invention, by changing the doping state of the drift region in the epitaxial layer, that is to say, by adding, in the drift region with the same doping state as that of the epitaxial layer in the prior art, a first region and a second region with doping states different from that of the epitaxial layer, the doping state of the drift region is changed, and the first region and the second region have different doping states. Because the doping states (including the doping concentration and the impurity type) of the first region and the second region can be adjusted according to the requirement for the breakdown voltage and the on-resistance of the device, on one hand the on-resistance is reduced by controlling the doping concentrations of the first region and the second region to be greater than that of the epitaxial layer; on the other hand the breakdown voltage of the device is increased by forming a PN junction between the first region and the second region, whereby the drain region is completely depleted without affecting the breakdown voltage BV of the drain region. Hence, the high breakdown voltage of the LDMOS device is ensured, while the on-resistance and the power

consumption of the device is reduced in comparison with the LDMOS device in prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other objects, features and advantages of the present invention will be clearer from the drawings. Throughout the figures, similar reference numerals indicate similar parts. The figures are not drawn to scale, and the purpose is to show the concept of the present invention.

[0025] Figures 1-3 show an LDMOS device in the prior art;

[0026] Figure 4 is a structural sectional view of an LDMOS device disclosed in an embodiment of the present invention;

[0027] Figure 5 is a top view of the LDMOS device disclosed by an embodiment of the present invention; and

[0028] Figures 6-15 are sectional views for explaining a method for fabricating an LDMOS device disclosed by an embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0029] For the purpose of better understanding the above objects, features and advantages, embodiments of the present invention will be described in detail hereinafter in conjunction with the drawings.

[0030] To facilitate the sufficient understanding of the invention, many details are set forth in the following description. However, the present invention can be implemented in other manners than those described herein, and similar extensions can be made by those skilled in the art without deviating from the spirit of the present invention. Therefore the present invention is not limited by the embodiments disclosed hereinafter.

[0031] Furthermore, the present invention is described in detail in conjunction with

schematic diagrams. In describing the embodiments of the present invention in detail, for convenient description, sectional views showing structures of the device are not drawn to scale, and these schematic diagrams are only examples and should not limit the scope of protection of the present invention. Moreover, three-dimensional size including length, width and depth should be given in practical implementation.

[0032] As mentioned in the background of the present invention, in the prior art the high breakdown voltage and the low on-resistance of the LDMOS device are conflicting. The research of the present inventor shows that the reason for this problem mainly lies in that high breakdown voltage demands for a thick lightly doped (i.e. with low concentration doped) epitaxial layer and a long drift region, and low on-resistance demands for a thin heavily doped (i.e. high concentration doped) epitaxial layer and a short drift region. In the LDMOS device of the prior art, since only one configuration of the doping state of the epitaxial layer and the length of the drift region may be selected, the determination of the doping state of the epitaxial layer and the length of the drift region is ultimately a tradeoff between the breakdown voltage and the on-resistance, i.e., to obtain a minimum on-resistance under a scope of the breakdown voltage, rather than to obtain a higher breakdown voltage as well as a lower on-resistance.

[0033] Embodiment 1

[0034] Accordingly, an LDMOS device is provided in this embodiment, the structure of which is shown in Figure 4 and Figure 5. Figure 4 is a sectional view of the LDMOS device of this embodiment, and Figure 5 is a top view showing the locations of the first region and the second region. The LDMOS device includes:

[0035] a substrate including a body layer 201, an epitaxial layer 202 located on the body layer 201, and a well region 203 in a surface of the epitaxial layer;

[0036] It should be noted that in this embodiment, the substrate can include a semi-conductive element, such as silicon or SiGe of monocrystalline structure, polycrystalline structure or non-crystalline structure, and can further include a mixed semiconductor structure, such as silicon carbide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, alloy semiconductor or

any other combination; and the substrate in this embodiment can also be Silicon On Insulator (SOI). Furthermore, the semiconductor substrate can further include other materials, such as in a multiple-layered structure of an epitaxial layer or a buried layer. Although several examples of the material applicable for the substrate are described herein, any other materials that can be used as a semiconductor substrate fall within the spirit and the scope of the present invention.

[0037] a source region 208 located in the well region 203, and a drain region 209 located in the epitaxial layer 202;

[0038] a first region 204 and a second region 205 (as shown in Figure 5) located in the surface of the epitaxial layer 202 and having doping states different from that of the epitaxial layer 202, where the first region 204 and the second region 205 are located in a drift region between the source region 208 and the drain region 209, and have doping states different from each other;

[0039] The doping state includes doping concentration and impurity type. In this embodiment, the impurity types of the first region 204 and the second region 205 are different, and the doping concentrations thereof are substantially the same, so that a PN junction is formed between the first region 204 and the second region 205, to ensure that the breakdown voltage BV of the drain region 209 is not affected and the drain region 209 is depleted completely, thereby increasing the breakdown voltage of the device. Furthermore, each of the first region 204 and the second region 205 has a doping concentration greater than that of the epitaxial layer 202. In order to form a PN junction between the first region 204 and the second region 205, one of the first region 204 and the second region 205 has the same conducting type as that of the epitaxial layer, and the other has an opposite conducting type.

[0040] a field oxide layer 206 located above the first region 204 and the second region 205; and

[0041] a gate region 207 located on the well region 203 and the field oxide layer 206.

[0042] Furthermore, the LDMOS device of this embodiment further includes a gate 210

located on an upper surface of the gate region 207, a source 211 located on an upper surface of the source region 208, and a drain 212 located on an upper surface of the drain region 209.

[0043] The gate region 207 in this embodiment includes at least a gate oxide layer and a gate poly-silicon layer, and generally further includes a silicide layer on the upper surface of the gate poly-silicon layer, which may be determined from the structure of the device and will not be described in detail in this embodiment.

[0044] In the LDMOS device of this embodiment, the breakdown voltage and the on-resistance of the device are changed mainly by changing the doping state of the drift region in the epitaxial layer. By adding a first region 204 and a second region 205 with doping states different from that of the epitaxial layer 202 in the drift region which has the same doping concentration as that of the epitaxial layer in the prior art, the doping state of the drift region is changed. And then by adjusting the doping states of the first region 204 and the second region 205, the breakdown voltage and the on-resistance of the device may be adjusted, so as to ensure the high breakdown voltage while further decrease the on-resistance.

[0045] The structure and the doping states of the LDMOS device in this embodiment will be described hereinafter by taking a P-type LDMOS device as an example.

[0046] Referring to Figure 4 and Figure 5, in the P-type LDMOS device, the body layer 201 is P-type doped, the epitaxial layer 202 is N-type doped, the well region 203 is P-type doped, and the source region 208 and the drain region 209 are N-type doped. In this embodiment, the conducting types of the doping materials of the first region 204 and the second region 205 are opposite, and specifically, the first region 204 is P-type doped and the second region 205 is N-type doped.

[0047] If the doping type is N-type, the doping ions can be phosphorus ions or other pentavalent ions; if the doping type is P-type, the doping ions can be boron ions or other trivalent ions. In this embodiment, the first region 204 and the second region 205 are doped with different impurity types but at a same doping concentration: the first region 204 is doped with boron ions in a doping dose of $5E16cm^{-3}$, and the second region 205 is doped

with phosphorus ions in a doping dose of $5E16cm^{-3}$. Due to the different impurity types and the same doping concentrations of the first region and the second region, a PN junction can be formed between the first region and the second region.

[0048] It should be noted that in this embodiment, the doping concentrations of the first region and the second region are both greater than the doping concentration of the epitaxial layer. That is to say, the lightly doped drift region in the prior art is replaced with a heavily doped drift region, which significantly reduces on-resistance in comparison with the prior art. At the meantime, a high breakdown voltage can be ensured because of the existing of the PN junction between the first region and the second region.

[0049] In this embodiment, the epitaxial layer 202 can be an N-type epitaxial layer once-grown on the body layer 201 by means of CVD process, and the thickness of the epitaxial layer can be determined according to the specific application of the device. In this embodiment, the body layer 201 can be a P-type doped silicon substrate.

[0050] In this embodiment, the drift direction of the carriers in the LDMOS device is indicated by the arrow in Figure 4. Referring to Figure 4 and Figure 5, it can be seen that the first region 204 and the second region 205 are arranged as being perpendicular to the drift direction in the plane of the substrate. That is to say, as can be seen form Figure 5, the first region 204 and the second region 205 are arranged in a from-top-to-bottom order in the Figure, and the drift direction of the carriers is from right to left (i.e., the direction from the drain region 209 to the source region 208 in Figure 4). Such an arrangement facilitates the forming of the PN junction between the first region 204 and the second region 205, without increasing the on-resistance of the device.

[0051] Furthermore, it can be seen from Figure 5 that the lengths of the first region 204 and the second region 205 are different, and more specifically, the length of the first region 204 is less than the length of the second region 205. As used herein, the term "length" refers to the dimension of the first region 204 or the second region 205 in the drift direction of the carriers in a plane parallel to the substrate.

[0052] The extra part of the second region 205 with respect to the first region 204 in the length direction is located in the epitaxial layer close to the drain region. The drain region

has a same impurity type, which is N-type, as that of the second region, thus the extra part of the second region 205 with respect to the first region 204 can function to induce the N-type impurities of the drain region, which facilitates the implanting of the impurity ions of the drain region.

[0053] It should be noted that the lengths of the first region 204 and the second region 205 must be set according to the above description, because if the lengths of the first region 204 and the second region 205 are the same, or the length of the first region 204 is greater than that of the second region 205, the N-type impurities of the drain region will also be implanted into the first region 204, resulting in a PN junction between the first region 204 and the drain region 209 and further affecting the breakdown voltage of the drain region.

[0054] Furthermore, to form a PN junction between the first region 204 and the second region 205, the depths of the first region 204 and the second region 205 are the same. As used herein, the term "depth" refers to the thicknesses of the first region or the second region extending from the surface of the epitaxial layer towards the inside of the epitaxial layer.

[0055] Moreover, it should be noted that in this embodiment, one or more than one PN junctions, which are similar to the PN junction between the first region and the second region, can be provided. Nevertheless, the more than one PN junctions must be arranged according to the above principle: the more than one PN junctions must be arranged on the surface of the substrate in a direction perpendicular to the drift direction; the two regions between which the PN junction is formed must have a same depth, a same doping concentration, and opposite conducting types, where the doping concentration is greater than that of the epitaxial layer; and for at least one of these PN junctions, one of the regions between which the at least one PN junction is formed, which has the same doping type as that of the drain region, must have a length configuration similar to that of the second region, while for any of other PN junctions the lengths of the two regions can be the same. The more than one PN junctions may be or may be not spaced, depending on the demand of the device.

[0056] The above is only the description of the specific structure, the doping type and the like of the present invention by taking the P-type LDMOS device as an example. However, in practice, the structure of the LDMOS device disclosed by the present invention can also be applied to the N-type LDMOS device.

[0057] Similarly, the doping types and the doping concentrations of the first region and the second region provided in this embodiment are only preferred parameters. In practice, the doping types and the doping concentrations of the first region and the second region should be determined by taking the thickness, the length, and other parameters of the first region and the second region into consideration, so as to decrease the on-resistance and meanwhile ensure a high breakdown voltage.

[0058] In this embodiment, the first region and the second region may be formed in many ways. For example, the first region and the second region may be formed sequentially by selective epitaxial growth process, or can be formed sequentially by ion implanting. The forming of the first region and the second region will be described in detail in the following embodiments.

[0059] The main concept of the present invention is to replace the drift region with only one doping state in the prior art with multiple regions having multiple types of doping states, and to adjust the breakdown voltage and the on-resistant of the device by adjusting the doping states of individual regions and the proportions of individual regions in the drift region, including the length, the thickness, the area of individual regions.

[0060] Generally, the breakdown voltage can be increased by decreasing the doping concentration of one or more regions in the drift region and by increasing the thickness or the length of the one or more regions properly; and the on-resistance can be decreased by increasing the doping concentration of one or more regions in the drift region and by decreasing the thickness or the length of the one or more regions. According to the above principle, by selecting proper parameters, the on-resistance may be further decreased and the power consumption of the device may be reduced in comparison to the LDMOS device of the prior art while a high breakdown voltage may be ensured.

[0061] The specific structure of the LDMOS device disclosed in the present invention is

described in reference to the above embodiment, and the method for fabricating the same will be described in detail in the following embodiment.

[0062] Embodiment 2

[0063] The respective steps of a method for fabricating the LDMOS device as disclosed in the present embodiment are shown by referring to the sectional views in Figures 6-15. By taking a P-type LDMOS device as an example, the method includes the following steps.

[0064] As shown in Figure 6 and Figure 7, a substrate is provided. The substrate includes a body layer 301, an epitaxial layer 302 located on the body layer 301, and a well region 303 located in the surface of the epitaxial layer 302. In this embodiment, the body layer 301 can be a P-type silicon substrate and can further include a buried layer (not shown) or other structures. The epitaxial layer 302 can be an N-type epitaxial layer once-grown on the body layer 301 by CVD process.

[0065] In this embodiment, the well region 303 (referring to Figure 7) can be P-type doped, and may be formed as follows. Firstly, a photoresist pattern of the well region 303 is formed on the surface of the epitaxial layer 302 by lithography. Then the well 303 is formed with ion implanting by taking this photoresist pattern (not shown) as a mask. Subsequently, the photoresist on the epitaxial layer 302 and the polymer formed during the plasma process are removed by a series of chemical wet cleaning processes. And then an annealing process is performed, and a new blocking oxide layer is formed on the exposed surface of the exposed epitaxial layer. The implanted impurities are diffused towards the silicon of the epitaxial layer under a high temperature, and the covalent bond between the impurity atom and the silicon atom is activated, so that the impurity atom becomes part of the lattice structure, and thus the electric activation is completed. Meanwhile, by the annealing process, the damage made to the atom structure of the silicon covalent bond during the ion implanting can be restored.

[0066] After the well region 303 is formed in the surface of the epitaxial layer 302, the first region and the second region with different doping states are formed in the surface of the epitaxial layer, the process of which is shown in Figures 8-13, the specific description

thereof will be given in the following.

[0067] Reference is made to Figure 8. Firstly, a blocking oxide layer 304 of the first region is formed on the surface of the epitaxial layer 302 by chemical vapor deposition, where the blocking oxide layer 304 can be a silicon oxide film prepared from tetraethyl orthosilicate (TEOS). Subsequently, a photoresist layer is spin coated on the blocking oxide layer 304, and an anti-reflecting layer (not shown) to reduce unnecessary reflection can be further formed between the photoresist layer and the blocking oxide layer 304, so as to ensure the exposure accuracy. Then an exposure process is performed on the photoresist layer by means of a mask with a pattern of the first region to form the pattern of the first region on the surface of the photoresist layer. The photoresist layer at the first region pattern is removed, an opening for the first region pattern is formed on the photoresist layer, and then the first region pattern 305 is formed by dry etching the material of the epitaxial layer underneath the opening for the first region pattern, by taking the photoresist layer having the opening for the first region pattern as a mask.

[0068] The first region pattern 305 can be formed in the surface of the epitaxial layer 302 by anisotropic etching process. The sectional view of the first region pattern 305 is shown in Figure 8, and the top view thereof is shown in Figure 9. In the top view, the width and the length of the first region pattern 305 only consist part of the width of the drift region in the device, rather than extend over the whole drift region.

[0069] Referring to Figure 10, after the first region pattern 305 is formed, a first region 306 is formed in the first region pattern 305 by selective epitaxial growth. The first region 306 is a P-type doped epitaxial region with boron or other trivalent ions as impurity ions in a doping concentration of $5E16cm^{-3}$.

[0070] After the first region 306 is formed, by taking the blocking oxide layer 304 or the silicon oxide film (not shown) formed on the surface of the epitaxial layer as an etching stopping layer, the P-type epitaxial material grown on the blocking oxide layer 304 or on the surface of the silicon oxide film of the first region can be removed with etching back or CMP process, so as to make the surface of the first region 306 flush with the surface of the epitaxial layer 302, and ensure the smooth of the surface of the substrate. The blocking

oxide layer 304 or the silicon oxide film is removed subsequently by wet chemical cleaning or other methods.

[0071] After the first region 306 is formed, a second region is formed in a similar method, as shown in Figures 11-13. Referring to Figure 11, the blocking oxide layer 304 of the first region is removed, and then an oxide layer is deposited by CVD process to serve as a blocking oxide layer 307 of the second region. The blocking oxide layer 307 of the second region may have material similar to that of the blocking oxide layer 304 of the first region, which is a silicon oxide film prepared from TEOS.

[0072] Then, as shown in Figure 12, which is a top view showing the forming of a second region pattern 308, a photoresist pattern of the second region (not shown) is formed on the surface of the blocking oxide layer 307 in the second region by lithography, and the second region pattern 308 is formed in the surface of the epitaxial layer 302 with etching process by taking the photoresist layer with the second region pattern as a mask. Then the photoresist layer is removed.

[0073] Referring to Figure 13, the second region 309 is formed in the second region pattern 308 (as shown in Figure 12) by selective epitaxial growth. The second region 309 is an N-type doped epitaxial region with phosphorus or other pentavalent ions as impurity ions in a doping concentration of $5E16cm^{-3}$. It can be seen from the drawing that the length of the second region 309 is greater than that of the first region 306, and the whole width consisted of the widths of the first region 306 and the second region 309 exactly equals to the width of the drift region of the device. The term "width" refers to the dimension in a direction perpendicular to the drift direction of the carriers on the surface of the substrate.

[0074] Similarly, after the second region 309 is formed, the N-type epitaxial material grown on the surface of the blocking oxide layer 307 of the second region can be removed by etching back or CMP process, to make the surface of the second region 309 flush with the surface of the epitaxial layer 302 and to ensure the smooth of the surface of the silicon sheet. This step is similar to the step performed after the first region 306 is formed, which will not be described in detail herein.

[0075] Those skilled in the art can understand that the order for forming the first region

and the second region can be inverted, and the locations of the first region and the second region can also be exchanged, as long as a high breakdown voltage and a low on-resistance can be ensured.

[0076] The above phrase "in the surface of the epitaxial layer" means in a region extending downward for a certain depth from the surface of the epitaxial layer 302, which region is a part of the epitaxial layer 302; and the above phrase "on the surface of the implanting oxide layer 303" means in a region extending upward from the surface of the implanting oxide layer 303, which region is not a part of the implanting oxide layer 303 itself. The meaning of other phrases can be deduced similarly.

[0077] Referring to Figure 14, after the first region 306 and the second region 309 are formed, a field oxide layer 310 is formed on the epitaxial layer above the first region 306 and the second region 309. The field oxide layer 310 includes at least silicon oxide. In this embodiment, the method for forming the field oxide layer 310 is the same as that in the prior art: an oxide layer may be formed on the epitaxial 302 by CVD process, and then the field oxide layer 310 is formed by lithography and etching process. The field oxide layer 310 can also be formed in other ways, which will not be described herein.

[0078] Referring to Figure 15, a gate region 311 is formed on the well region 303 and the field oxide layer 310, a source region 312 is formed in the well region 303, and a drain region 313 is formed in the epitaxial layer 302. In this embodiment, the source region 312 and the drain region 313 are both N-type doped, and the first region 306 and the second region 309 are located in a drift region between the source region 312 and the drain region 313.

[0079] The gate region 311 includes at least a gate poly-silicon layer. In other embodiments of the invention, the gate region can further include a laminated layer doped with poly-silicon or formed of poly-silicon and metal silicides on the poly-silicon. The process for forming the gate region 311 is as follows: a poly-silicon layer (not shown) is deposited on the field oxide layer 310, a photoresist layer with a gate region pattern is formed on the surface of the poly-silicon layer by lithography process, and then the gate region 311 is formed with dry etching by taking the photoresist layer with the gate region

pattern as a mask. The poly-silicon layer can be formed by chemical vapor deposition, physical vapor deposition or other manners, which is not limited in this embodiment.

[0080] In this embodiment, the source region 312 and the drain region 313 may be formed by ion implanting. Specifically, a photoresist layer with source region pattern or drain region pattern is formed on the epitaxial layer 302 by lithography, and then the source region 312 and the drain region 313 are formed with ion implanting by taking this photoresist layer as a mask.

[0081] The method in this embodiment further includes: subsequently forming a gate 314 on the gate region 311, forming a source 315 on the source region 312 and forming a drain 316 on the drain region 313.

[0082] In this embodiment, the gate 314, the source 315 and the drain 316 are similarly formed in the following process. Firstly, a dielectric layer, i.e., an inter-layer dielectric layer, is deposited on the surface of the epitaxial layer 302. Then a photoresist pattern with a gate through-hole, a source through-hole, and a drain thourgh-hole is formed on the surface of the inter-layer dielectric layer by lithography process. The above three through-holes are then formed in the inter-layer dielectric layer in corrosion process by taking this photoresist pattern (not shown) as a mask, and the gate region 311, the source region 312 and the drain region 313 is connected with metal via respective through-holes, so that the gate 314, the source 315 and the drain 316 are formed.

[0083] In the above embodiment, the first region and the second region are formed by selective epitaxial growth. In practice, the first region and the second region may also be formed by ion implanting, which is specifically described in the following embodiment.

[0084] Embodiment 3

[0085] The method for fabricating an LDMOS device as disclosed in this embodiment differentiates from that of the last embodiment in that the first region and the second region are formed by ion implanting in this embodiment. Specifically, a silicon oxide film prepared from TEOS is formed on the surface of the epitaxial layer by CVD, a photoresist pattern of the first region is formed on the silicon oxide film by lithography, and then the

first region is formed with ion implanting by taking the photoresist layer with the first region pattern as a mask. The silicon oxide film is then removed. The ions implanted into the first region are boron or other trivalent ions.

[0086] Similarly, the second region is formed in a way similar to that of the first region, which will not be described in detail herein.

[0087] The above embodiments are only preferred embodiments of the present invention, but not meant to restrict the present invention in any form.

[0088] Although the present invention is disclosed in preferred embodiments as mentioned above, the preferred embodiments are not meant to restrict the present invention. Numerous modifications, variations and equivalent alternatives can be made by those skilled in the art based on the above disclosed method and technical contents without departing from the scope of the technical solutions. Therefore, any content that dose not deviate form the technical solutions of the present invention, and any simple variations, equivalents and modifications made to the above embodiments based on the essence of the present invention fall in the scope of protection of the present invention.

CLAIMS:

1. An LDMOS device, comprising:

a substrate comprising an epitaxial layer and a well region located in a surface of the epitaxial layer;

a source region located in the well region, and a drain region located in the epitaxial layer;

a first region and a second region located in the surface of the epitaxial layer and having doping states different from a doping state of the epitaxial layer, wherein the first region and the second region are located in a drift region between the source region and the drain region, and have doping states different from each other;

a field oxide layer located above the first region and the second region; and

a gate region located on the well region and the field oxide layer.

2. The LDMOS device according to claim 1, wherein the first region and the second region are arranged as being perpendicular to a drift direction in a plane of the substrate.

3. The LDMOS device according to claim 2, wherein the first region and the second region have opposite conducting types.

4. The LDMOS device according to claim 3, wherein the second region has a same conducting type as the epitaxial layer and has a doping concentration greater than that of the epitaxial layer.

5. The LDMOS device according to claim 4, wherein the first region and the second region have substantially a same doping concentration.

6. The LDMOS device according to claim 5, wherein the first region and the second region are in same depth.

7. The LDMOS device according to claim 6, wherein the first region is P-type doped, the second region is N-type doped, and the first region has a length less than that of the second region.

8. The LDMOS device according to any one of claims 1-7, wherein the first region and the second region are sequentially formed by a selective epitaxial growth.

9. The LDMOS device according to any one of claims 1-7, wherein the first region and the second region are sequentially formed by ion implanting.

10. A method for fabricating an LDMOS device, comprising:

providing a substrate, wherein the substrate comprises an epitaxial layer and a well region located in a surface of the epitaxial layer;

forming a first region and a second region in the surface of the epitaxial layer, wherein the first region and the second region have different doping states;

forming a field oxide layer on the epitaxial layer above the first region and the second region; and

forming a gate region on the well region and the field oxide layer, forming a source region in the well region, and forming a drain region in the epitaxial layer, wherein the first region and the second region are located in a drift region between the source region and the drain region.

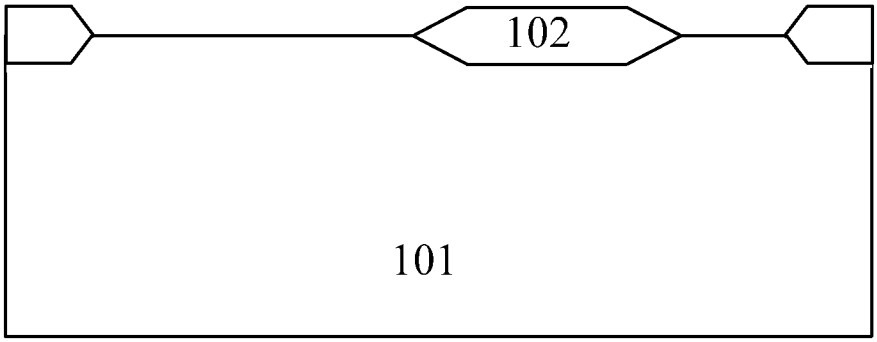


Figure 1

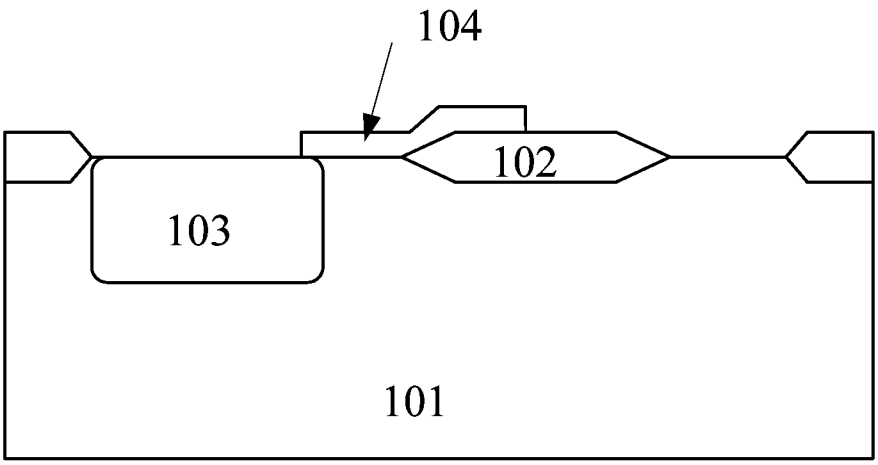
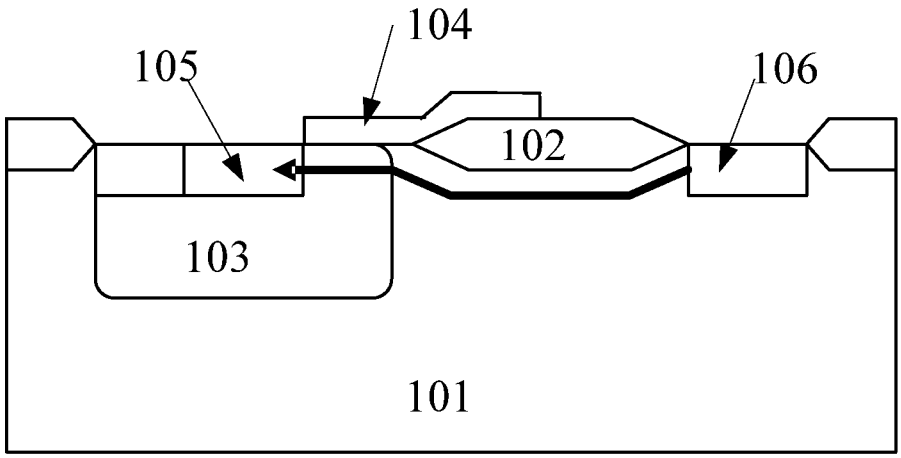


Figure 2



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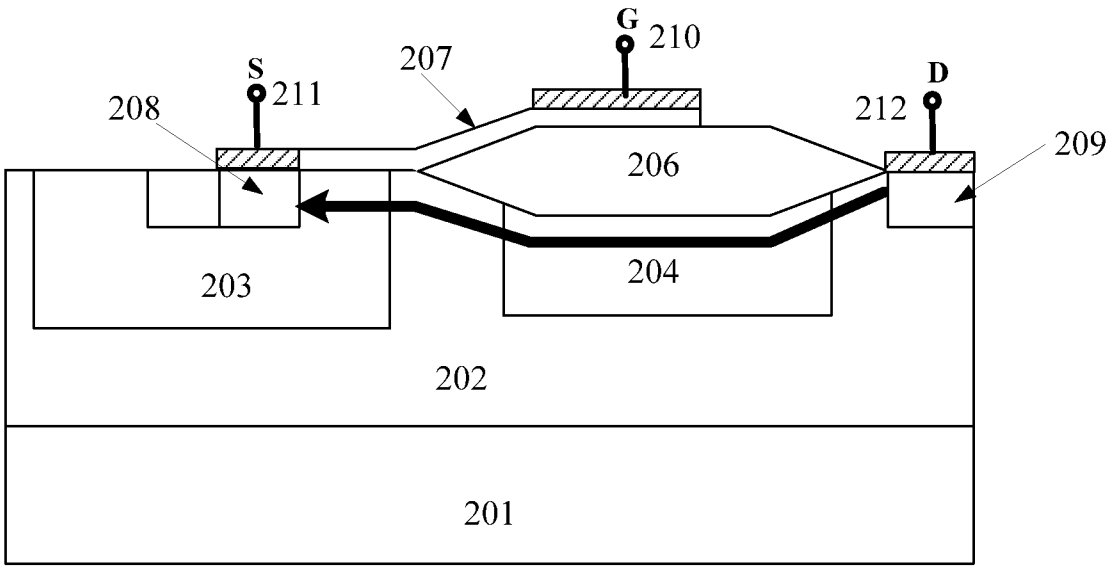

Figure 4

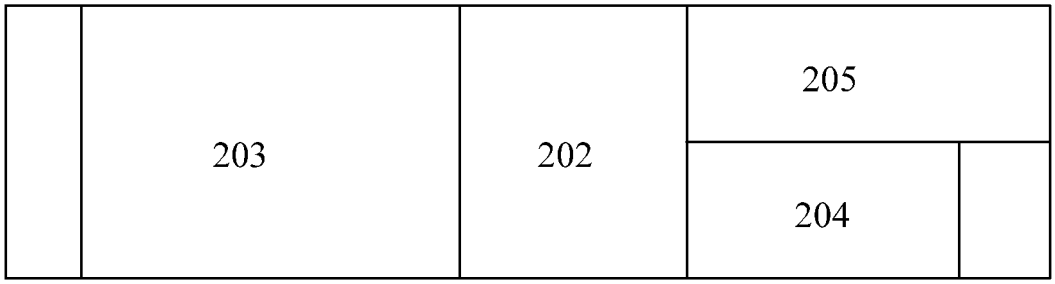

Figure 5

Figure 6

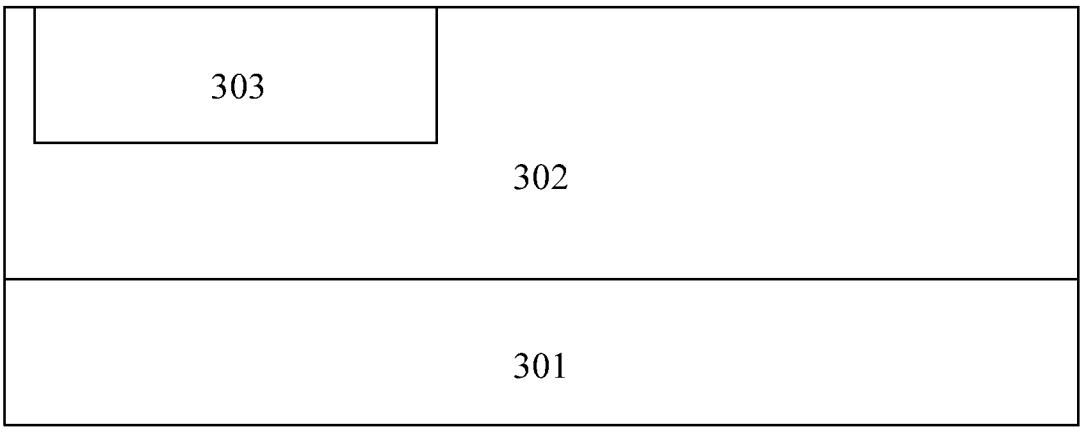

Figure 7

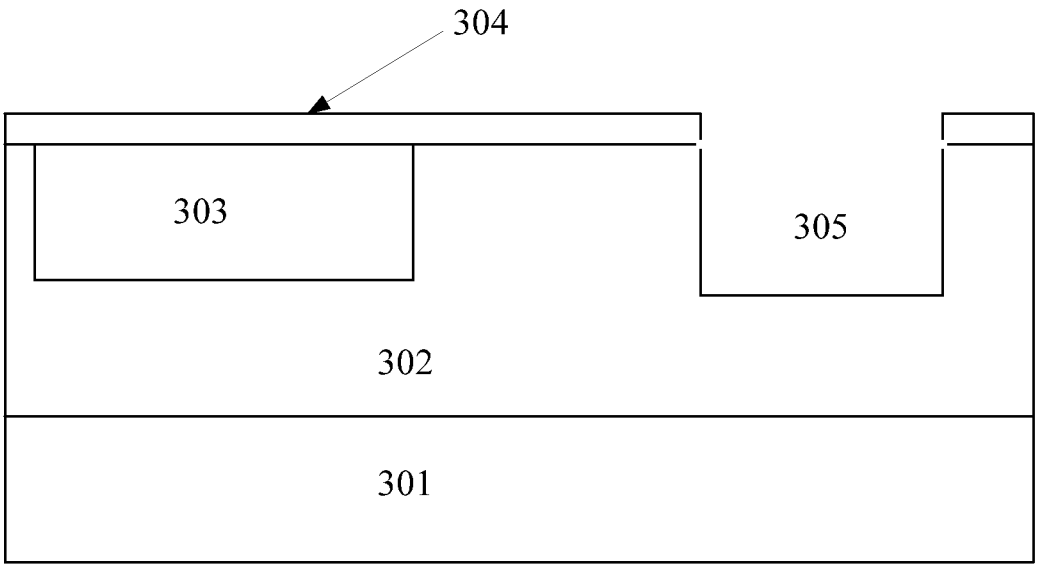

Figure 8

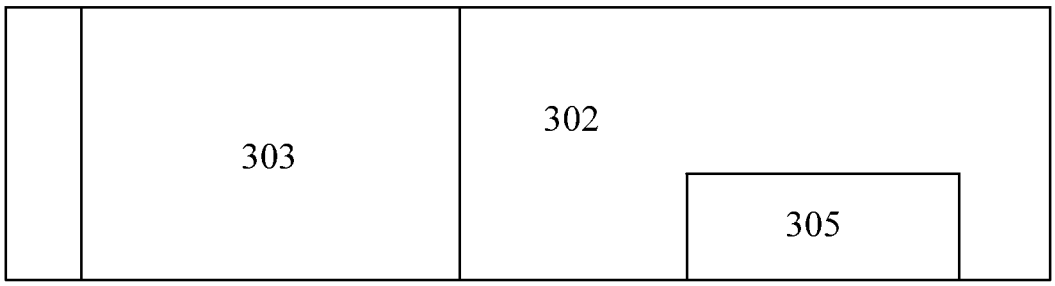

Figure 9

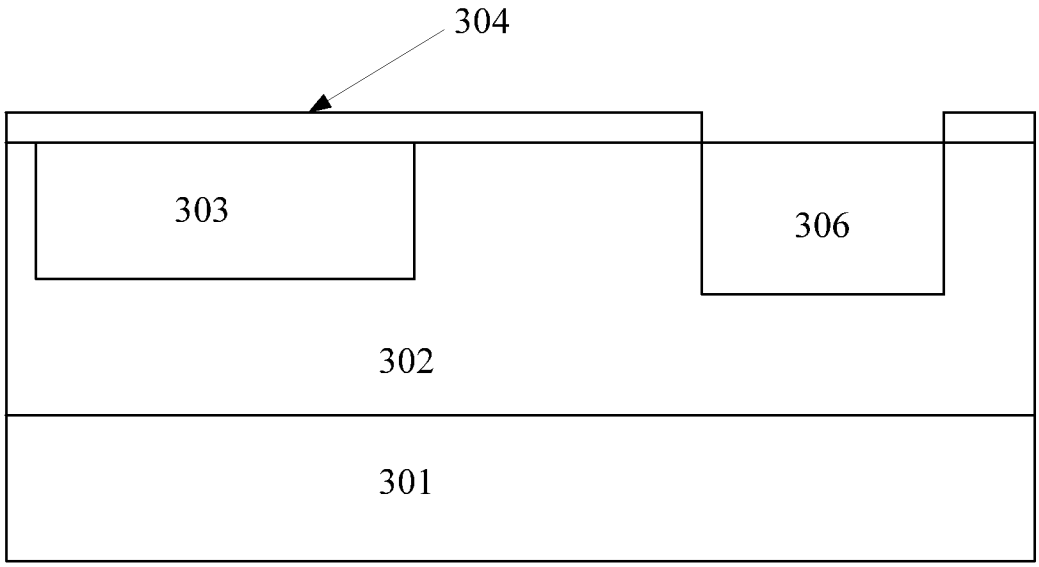

Figure 10

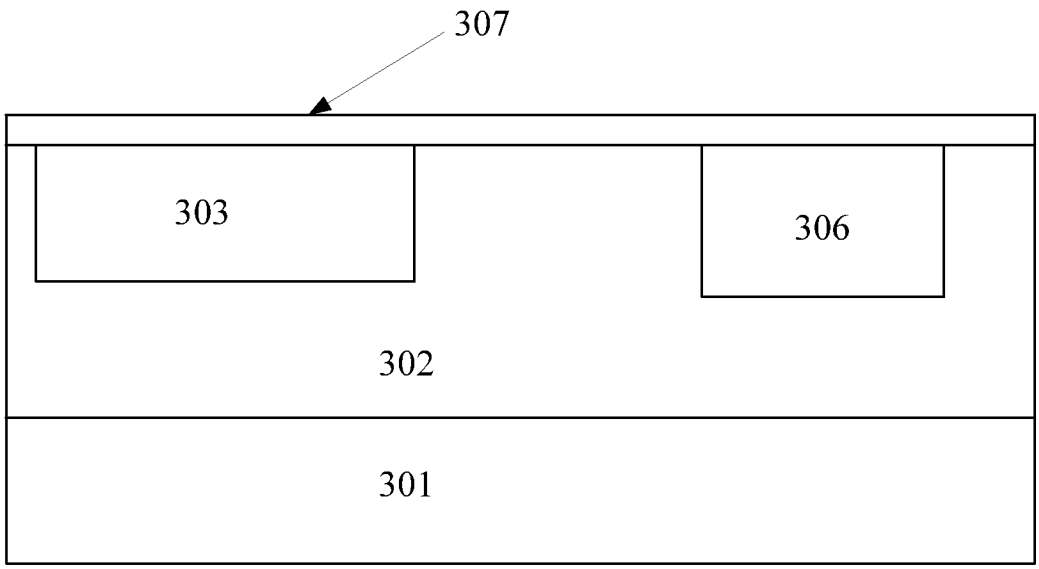

Figure 11

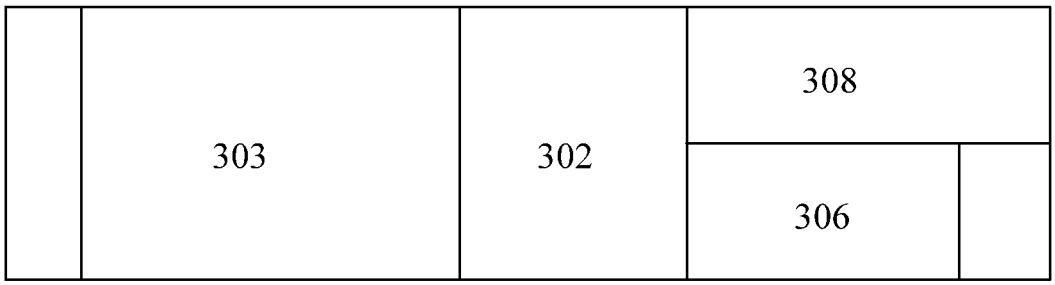

Figure 12

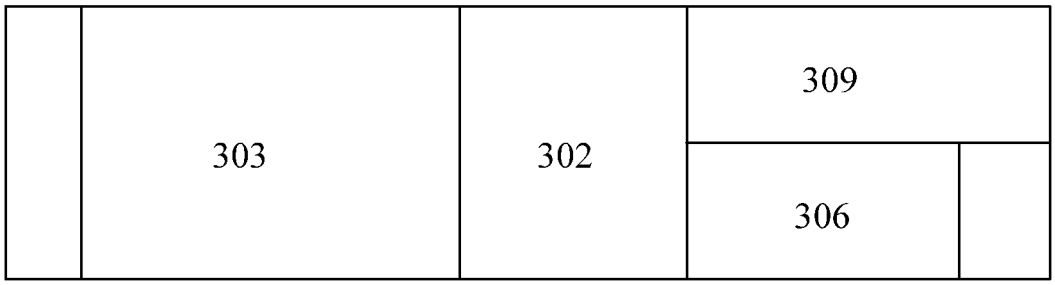

Figure 13

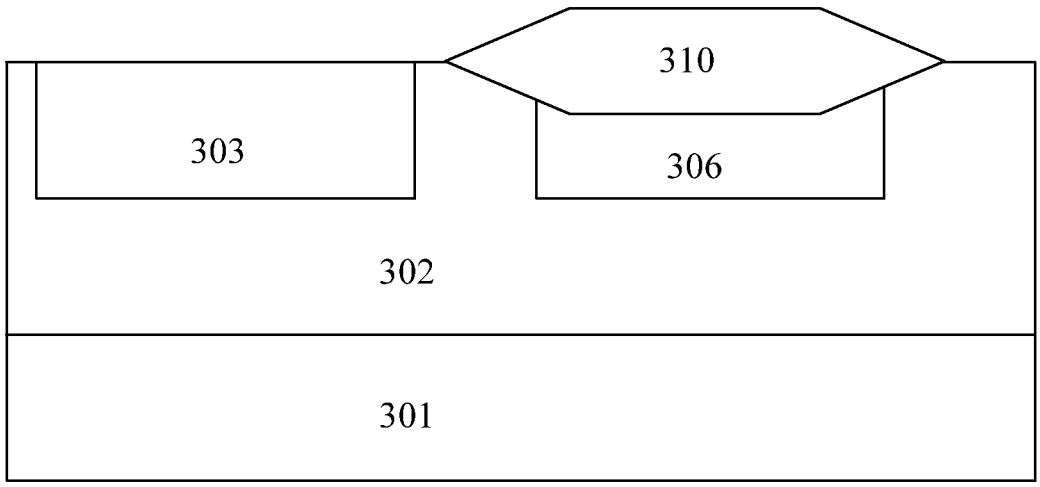

Figure 14

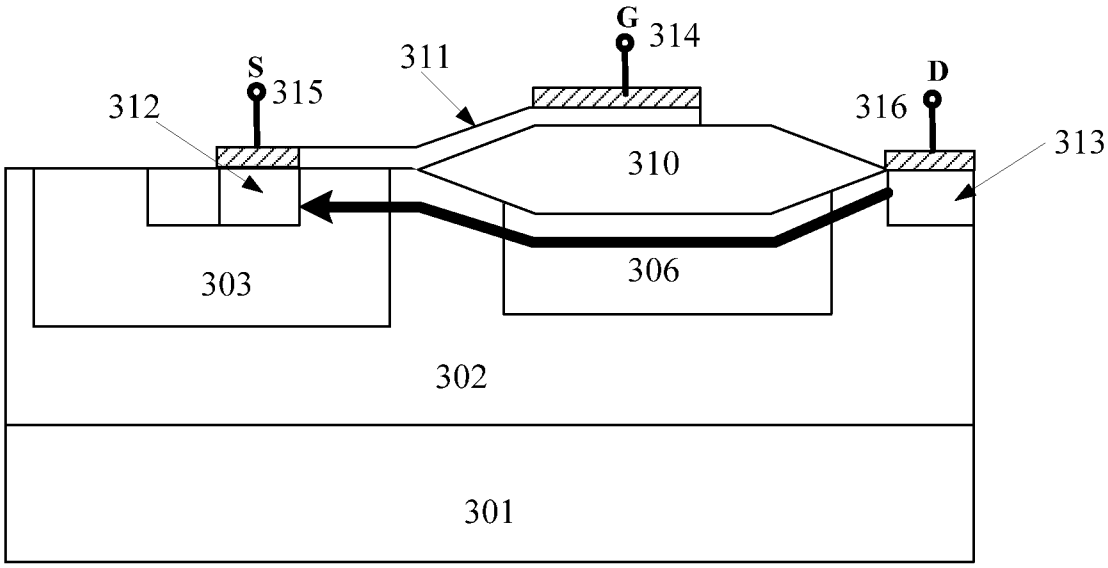

Figure 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/080671

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01L29/-; H01L21/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
CNPAT;CNKI;WPI;EPODOC:LDMOS,LATERAL,DOUBLE,DIFFUS+,DRIFT+,CHANNEL+,BREAKDOWN+,ON RESISTANCE,SOURCE+,DRAIN+,PN JUNCTION+,DOP+,LENGTH+,PARALLEL+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN1909200A (SEMICONDUCTOR COMPONENTS IND.) 07 Feb.2007 (07.02.2007) description page 5 line 5 – page 13 line 27, figs. 1-20	1-6,8-10
Y		7
Y	US2004212032A1(ONISHI, Yasuhiko et al.) 28 Oct.2004(28.10.2004) description paragraphs 49-57, fig. 2	7
A	CN101789435A(CHINESE ACADEMY OF SCIENCE SHANGHAI INSTITUTE OF MICROSYSTEM AND INFORMATION TECHNOLOGY et al.)28 Jul.2010(28.07.2010) the whole document	1-10
A	US6111289A(UDREA, Florin) 29 Aug.2000(29.08.2000) the whole document	1-10
A	US2004051141A1(UDREA, Florin) 18 Mar.2004(18.03.2004) the whole document	1-10

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 Dec. 2011(19.12.2011)	**19 Jan. 2012 (19.01.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer FANG,Yan Telephone No. (86-10)62413925

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/080671

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN1909200A	07.02.2007	US2007023855A1	01.02.2007
		KR20070015891A	06.02.2007
		US7381603B2	03.06.2008
		TW200709303A	01.03.2007
		CN1909200B	30.06.2010
		HK1103167A1	04.03.2011
US2004212032A1	28.10.2004	DE10120030A1	31.10.2001
		JP2001308324A	02.11.2001
		US2001050394A1	13.12.2001
		US6756636B2	29.06.2004
		US7002211B2	21.02.2006
		DE10120030B4	06.09.2007
		JP4534303B2	01.09.2010
CN101789435A	28.07.2010	None	
US6111289A	29.08.2000	EP1026750A1	09.08.2000
		JP2000228521A	15.08.2000
US2004051141A1	18.03.2004	WO2004004013A1	08.01.2004
		AU2003241057A1	19.01.2004
		US6858884B2	22.02.2005
		EP1516369A1	23.03.2005
		JP2005531153A	13.10.2005
		CN1663049A	31.08.2005

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/080671

CLASSIFICATION OF SUBJECT MATTER

H01L29/78 (2006.01) i

H01L21/336 (2006.01) i