(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 May 2003 (22.05.2003)

PCT

(10) International Publication Number
WO 03/043019 A1

(51) International Patent Classification[7]: G11C 11/16, 11/15

(21) International Application Number: PCT/US02/34954

(22) International Filing Date: 30 October 2002 (30.10.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/010,574 13 November 2001 (13.11.2001) US

(71) Applicant: MOTOROLA INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventor: RIZZO, Nicholas, D.; 1238 North Palmsprings Drive, Gilbert, AZ 85234 (US).

(74) Agents: KOCH, William, E. et al.; Corporate Law Department, 3102 North 56th Street, P.O. Box 10219, Phoenix, AZ 85018 (US).

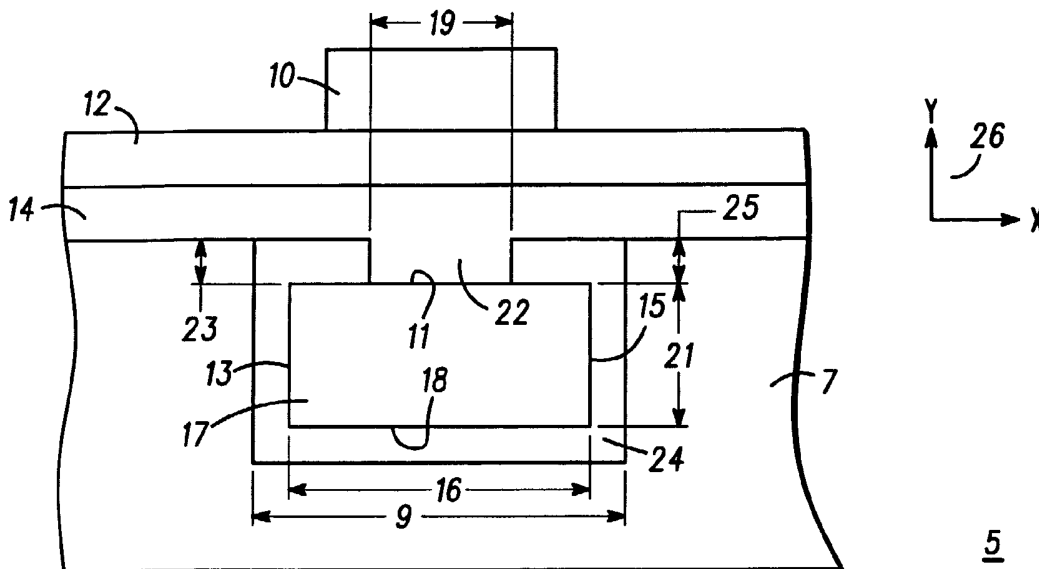
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** CLADDING FIELD ENHANCEMENT OF AN MRAM DEVICE



(57) **Abstract:** A conductive line for programming a magnetoresistive memory device which includes a metal interconnect region positioned proximate to a magnetoresistive random access memory device, wherein the metal interconnect region supplies a current which produces a magnetic field and wherein the metal interconnect region includes a metal layer with a length and a width and has a first side, a second side, a third side, and a fourth side wherein a ferromagnetic cladding region with a thickness is positioned on the first side, the second side, the third side, and the fourth side of the metal layer, and wherein the ferromagnetic cladding region positioned on the first side has a trench having a length less than the length of the metal layer and a width approximately equal to the thickness of the ferromagnetic of the magnetic cladding region. The length of the trench can be changed to adjust the magnitude of the magnetic field.

WO 03/043019 A1

Cladding Field Enhancement of an MRAM Device

FIELD OF THE INVENTION

5 This invention relates to semiconductor memory devices.

More particularly, the present invention relates to enhancing the magnetic field for programming semiconductor random access memory devices that utilize a magnetic field.

10

BACKGROUND OF THE INVENTION

A magnetoresistive random access memory (hereinafter referred to as "MRAM") device has a structure which includes ferromagnetic layers separated by
15 non-ferromagnetic layers. The ferromagnetic layers each have a free magnetic moment vector that can be oriented in one of several preferred directions relative to a pinned magnetic moment vector that is fixed in direction.

Unique resistance values are created by the orientation of the free magnetic
20 moment vector relative to the pinned magnetic moment vector. These unique resistance values are used to represent stored information. Accordingly, stored information is read by detecting resistance changes of the magnetic memory device. In typical magnetic memory devices, two resistance states are available. The stored

states can be read by passing a sense current through the cell in a sense line to detect the difference between the magnetic resistances of the states.

In MRAM devices, the memory cells are programmed by magnetic fields produced by a current carrying conductor such as a copper interconnect. Typically, two orthogonal interconnects are employed, with one positioned above (hereinafter referred to as the bit line) the MRAM device and the second positioned below (hereinafter referred to as the digit line) the MRAM device. The purpose of the bit and digit lines is to provide magnetic fields for programming the MRAM device.

A problem with programming a MRAM device is the large current required to produce a magnetic field of sufficient magnitude. This is especially a problem for low power applications, such as laptop computers, cell phones, pagers, and other portable electronic devices. In addition, as the magnetic memory cell is reduced in size to increase the areal density of the memory, the magnetic field required for programming of the ferromagnetic free layer must be increased to maintain the stability of the memory state against thermal fluctuations. Further, a MRAM device integrates magnetic memory elements and other circuits, for example, a control circuit for magnetic memory elements, comparators for detecting states in a magnetic memory element, input/output circuits, etc. These circuits are usually fabricated in the process of CMOS technology, which operates at low current and high efficiency, in order to lower the power consumption of the system.

In the prior art, the bit lines and digit lines are typically surrounded by a ferromagnetic cladding region to focus the magnetic field towards the MRAM device. For an uncladded conductive line, the magnetic field is given by the equation $H \approx I/2 \cdot w$, where I is the current flowing through the conductive line and w is the width of the conductive line. For simplicity of discussion, we are ignoring the magnetic field loss caused by the finite distance between the bit and the conductive line, as well as the field loss caused by the finite thickness of the conductive line. However, for a conductive line cladded on three sides, the magnetic field is given by the equation $H \approx I/w$, which is a factor of two larger than the uncladded bit line. Hence, the magnetic field of a conductive line can be increased for a given current by adding a ferromagnetic cladding region. Thus, by adding the ferromagnetic cladding region, it is possible to program MRAM devices with less current. However, further reductions in current are desired so that MRAM devices are more compatible with CMOS technology.

It would be highly advantageous, therefore, to remedy the foregoing and other deficiencies inherent in the prior art.

Accordingly, it is an object of the present invention to provide a new and improved magnetoresistive random access memory device.

It is an object of the present invention to provide a new and improved magnetoresistive random access memory device which reduces power consumption of the device.

It is a further object of the present invention to provide a new and improved magnetoresistive random access memory device which is more compatible with CMOS technology.

5

It is another object of the present invention to provide a new and improved magnetoresistive random access memory device which operates at currents typically produced by CMOS technology.

10

SUMMARY OF THE INVENTION

To achieve the objects and advantages specified above and others, a conductive line for programming a MRAM device is disclosed which includes a metal interconnect region, wherein the metal interconnect region is capable of
15 supplying a current which produces a magnetic field. The metal interconnect region includes a metal layer with a thickness and a width and has a first side, a second side, a third side, and a fourth side wherein a ferromagnetic cladding region with a thickness is positioned on the first side, the second side, the third side, and the fourth side of the metal layer. Further, the ferromagnetic cladding region positioned
20 on the first side has a trench having a width, g, which is less than the width, w, of the metal layer and a depth approximately equal to the thickness of the ferromagnetic cladding region. The trench within the ferromagnetic cladding region is positioned adjacent to a magnetoresistive random access memory device. The purpose of the trench is to concentrate the magnetic field proximate to the

magnetoresistive random access memory device, wherein the magnetic field is increased by a factor approximately equal to w/g, the width of the metal layer divided by the width of the trench.

5 BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in 10 conjunction with the following drawings:

FIG. 1 is a simplified sectional view illustrating a conductive line in accordance with the present invention;

15 FIG. 2 is a plot illustrating the magnitude of the magnetic field verses the width of the trench within the ferromagnetic cladding region at a distance from the conductive line; and

FIGS. 3, 4, 5, and 6 are simplified sectional views illustrating sequential 20 steps in a process of fabricating a metal interconnect region positioned above a memory bit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turn now to FIG. 1, which illustrates a simplified sectional view of a conductive line 5 for programming a MRAM device 10 in accordance with the present invention. Conductive line 5 includes a metal interconnect region 9 positioned proximate to MRAM device 10 and formed within a substrate 7, wherein
5 the metal interconnect region 9 is capable of supplying a current which produces a magnetic field for switching MRAM device 10. An *x-y* coordinate system 26 is used as a reference for the present discussion. In this embodiment, MRAM device 10 is supported on a dielectric interlayer 14 and a metal contact layer 12, which connects MRAM device 10 to a transistor (not shown). It will be understood that
10 metal interconnect region 9 can be positioned in other configurations relative to MRAM device 10 such that the magnetic field produced by the current in metal interconnect region 9 is sufficient to program MRAM device 10.

Metal interconnect region 9 includes a metal layer 17 which has a width 16
15 and a thickness 21 and also has a first side 11, a second side 13, a third side 15, and a fourth side 18. In the preferred embodiment, metal layer 17 includes copper, but it will be understood that metal layer 17 can include other metals, such as aluminum, silver, gold, platinum, or another suitable conductive material. Typically, metal layer 17 is deposited by physical vapor deposition (hereinafter referred to as PVD)
20 and plating or another suitable deposition technique.

A ferromagnetic cladding region 24 with a thickness 23 is positioned on first side 11, second side 13, third side 15, and fourth side 18 of metal layer 17. Ferromagnetic cladding region 24 positioned on first side 11 has a trench 22 having

a width 19 which is less than width 16 of metal layer 17. Further, trench 22 has a depth 25 approximately equal to thickness 23 of ferromagnetic cladding region 24. Ion milling can be used to create trench 22 and a spacer layer may also be needed.

5 In the preferred embodiment, ferromagnetic cladding region 24 includes ferromagnetic materials that have high magnetic permeability, such as NiFeCo alloys. With a high permeability, the cladding magnetization rotates in response to an applied magnetic field which enables the magnetic flux focusing and magnetic field enhancement of the ferromagnetic cladding region. While a rectangular metal 10 layer is illustrated and described it will be understood that other forms or shapes could be used and all such forms or shapes will incorporate the described sides, and will include a width and a depth. Further, the forming of the various layers included in metal interconnect region 9 can be formed using other semiconductor patterning and etching techniques well known to those skilled in the art.

15

In this specific embodiment, MRAM device 10 is a standard MRAM bit formed according to well-known practices in the art. While a standard MRAM bit is illustrated herein for convenience, it will be understood by those skilled in the art that many other types of devices could be provided. Also, while a single MRAM bit 20 is illustrated for convenience it should be understood that, for example, a complete array of devices or control/driver circuits around the periphery of an array of magnetic memory bits may be formed.

For ease of discussion, a digit line not in physical contact with the magnetic memory bit is discussed in reference to FIG. 1. However, it should be understood that while the drawings illustrate a digit line not in physical contact with the magnetic memory bit, that it is also anticipated by this disclosure to form a digit line that is in physical contact with the magnetic memory bit. Thus, it will be understood that in an alternative embodiment, physical contact is made between MRAM device 10 and a magnetically coupled digit line.

Ferromagnetic cladding region 24 can be formed by etching a trench in substrate 7 using standard semiconductor patterning and etching techniques. Also, ferromagnetic cladding region 24 is illustrated as a single layer, but it will be understood that ferromagnetic cladding region 24 can include a plurality of layers. For example, it is well known to those skilled in the art that a metal layer/ ferromagnetic layer/ metal layer can be used as an effective cladding layer, wherein the metal layers can include tantalum and the ferromagnetic layer can include nickel iron (NiFe). However, ferromagnetic cladding region 24 is illustrated as including one layer of a ferromagnetic material, such as NiFe, in this embodiment for simplicity.

Conductive line 5 in FIG. 1 illustrates a metal interconnect region 9 positioned below MRAM device 10. Metal interconnect region positioned thus is often referred to as a digit line. However, it will be understood that another metal interconnect region could be formed using standard semiconductor processes well know to those skilled in the art positioned above MRAM device 10 in a similar

manner and be referred to as a bit line. Further, a bit line can be formed using a self-aligned process as will be discussed presently. Also, it will be understood that this is a simplified view that only shows the areas of interest, and in particular metal interconnect region 9. Further, in this embodiment, the metal layers are illustrated as being stacked on MRAM device 10, but it will be understood that the metal layers can be positioned in other configurations relative to MRAM device 10 wherein the metal layers supply a large enough magnetic field to program MRAM device 10.

Turn now to FIG. 2 which illustrates a plot 27 of the magnitude of the magnetic field in the *x*-direction, as referenced to *x*-*y* coordinate system 26 (See FIG. 1) verses width 19. The data in Plot 27 was generated using a numerical magnetostatic solver assuming that width 16 is equal to 0.9 μm and thickness 21 is equal to 0.4 μm. In addition, the ferromagnetic cladding region 24 includes $Ni_{80}Fe_{20}$ and thickness 23 is assumed to be equal to 25 nm. Further, plot 27 illustrates the magnitude of the magnetic field at a point 0.15 μm above metal layer 17 and over the center of metal layer 17 with a current of 4 mA. Also, plot 27 is normalized to width 16 such that the magnitude of the magnetic field is assumed to be one when width 16 is equal to width 19. Hence, width 19 is adjusted to choose the magnitude of the magnetic field. The magnetic field is increased by a factor approximately equal to width 16 divided by width 19. Thus, Plot 27 illustrates that the magnitude of the magnetic field can be increased by decreasing width 19.

Thus, conductive line 5 reduces the current and power needed to program MRAM device 10 since the magnitude of the magnetic field is increased by decreasing width 19. Trench 22 in ferromagnetic cladding region 24 tends to concentrate the magnetic flux in a smaller area so that the magnetic field magnitude
5 increases. Hence, MRAM device 10 is more compatible with the low currents typically produced by CMOS technology.

One embodiment of fabricating the conductive line for programming a magnetoresistive memory device is discussed hereinafter and illustrated in FIGS. 3,
10 4, 5, and 6. Turning now to FIG. 3, the method of fabrication includes the steps of providing an interconnect forming layer 30, patterning and etching a trench 34 within interconnect forming layer 30 wherein trench 34 has a bottom 39, a first side 36, and a second side 38. Trench 34 can be formed using dry etching, wet etching, or other suitable etching processes well known to those skilled in the art. Also, it
15 will be understood that the conductive line could be formed in other embodiments by standard photolithography and etching.

A ferromagnetic cladding region 33 is deposited within trench 34 and positioned on bottom 39, first side 36, and second side 38 of trench 34. Further, a
20 spacer layer 35 is positioned on ferromagnetic cladding region 33 within trench 34. Spacer layer 35 can include silicon oxide, silicon nitride, or another suitable material. Spacer layer 35 is then ion milled (See FIG. 4) within trench 34 and through spacer layer 35 and ferromagnetic cladding region 33 positioned on bottom 39 to interconnect forming layer 30 to create a trench or gap 31 within

ferromagnetic cladding region 33 (See FIG. 5). It will be understood that ion milling is an example of an anisotropic etch technique and that other anisotropic etching techniques that have chemical or reactive components may also be used.

5 Spacer material 35 from within trench 34 is removed and a conductive material 37 is deposited within trench 34 and adjacent to ferromagnetic cladding layer 33 within trench 34 (See FIG. 6). Conductive material 37 can be formed using electrochemical deposition or another suitable deposition technique. Ferromagnetic cladding region 33 is then formed on conductive material 37. In this embodiment,
10 MRAM device 10 would be positioned below conductive material 37 and adjacent to gap 31, however, gap 31 can be positioned otherwise depending on the relative placement of MRAM device 10. This embodiment has the particular advantage that the gap in the ferromagnetic cladding region is self-aligned to the etched trench.

15 In a variation of the self-aligned embodiment discussed with reference to FIGS. 3, 4, 5, and 6, the ferromagnetic cladding region is deposited only on bottom 39 of trench 34 using an anisotropic film deposition. Gap 31 in ferromagnetic cladding region 33 is then patterned as before using a spacer layer and an anisotropic etch. Further, the spacer is removed after the anisotropic etch and
20 conductive material 37 which has four sides is formed using electrochemical deposition or another suitable deposition technique. Interconnect forming layer 30 surrounding conductive material 37 is then removed to expose conductive material 37 and ferromagnetic cladding region 33 is then positioned on conductor material 37 such that ferromagnetic cladding region 33 surrounds conductive material 37 and

has gap 31 positioned adjacent to bottom 39. Ferromagnetic cladding region 33 can be deposited using electrochemical deposition or PVD combined with a subtractive etch to remove the magnetic material between adjacent bit lines. Electrochemical deposition has the advantage of being self-aligned to ferromagnetic cladding region 33 and to the conductive material 37 and eliminates the need for expensive photolithography steps. Further, electroplating has the advantage of allowing a high aspect ratio when depositing a material in a trench.

Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. To the extent that such modifications and variations do not depart from the spirit of the invention, they are intended to be included within the scope thereof which is assessed only by a fair interpretation of the following claims.

Having fully described the invention in such clear and concise terms as to enable those skilled in the art to understand and practice the same, the invention claimed is:

CLAIMS

1. A conductive line for programming a magnetoresistive memory device comprising:

5 an electrically conductive interconnect region positioned proximate to a magnetoresistive random access memory device, wherein the interconnect region is capable of conducting a current for producing a magnetic field and wherein the interconnect region includes a conductive layer with a thickness and a width and has a first side, a second side, a third side, and a fourth side;

10 a ferromagnetic cladding region with a thickness positioned on the first side, the second side, the third side, and the fourth side of the conductive layer; and

the ferromagnetic cladding region positioned on the first side defining a trench having a width less than the width of the conductive layer and a

15 depth approximately equal to the thickness of the ferromagnetic cladding region.

2. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the interconnect region is formed within a substrate.

20

3. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the ferromagnetic cladding region includes at least one layer containing Ni, Fe, or Co, combinations thereof, and another suitable ferromagnetic material.

5

4. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the ferromagnetic cladding region includes at least one layer of platinum, palladium, ruthenium, rhodium, rhenium, iridium, tantalum, combinations thereof, and another suitable conductive material.

10

5. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the conductive layer includes one of copper, aluminum, platinum, gold, silver, and another suitable conductive material.

15

6. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the width of the trench in the ferromagnetic cladding region is chosen to provide a desired magnitude of the magnetic field.

7. A conductive line for programming a magnetoresistive memory device as claimed in claim 1 wherein the magnetic field is increased by a factor approximately equal to the width of the metal layer divided by the width of the trench in the ferromagnetic cladding region.

5

8. A conductive line for programming a magnetoresistive memory device comprising:

at least one of a metal interconnect bit and digit region positioned proximate to a magnetoresistive random access memory device, the metal
5 interconnect bit and digit regions being capable of supplying a current which produces a magnetic field and wherein the metal interconnect bit and digit regions include a conductive layer with a length and a width and a first side, a second side, a third side, and a fourth side;

a ferromagnetic cladding region with a thickness positioned on the
10 first side, the second side, the third side, and the fourth side of the conductive layer; and

the ferromagnetic cladding region positioned on the first side defining a gap having a width less than the width of the conductive layer and a depth approximately equal to the thickness of the ferromagnetic cladding region, and
15 wherein the gap is positioned adjacent to the magnetoresistive random access memory device.

9. A method of fabricating a conductive line for programming a magnetoresistive memory device, the method comprising the following steps performed in any convenient order:

providing a metal forming layer;

5 patterning and etching a trench within the metal forming layer wherein the trench has a first side, a second side, and a third side;

depositing a first ferromagnetic cladding region within the trench and positioned on the first side, the second side, and the third side of the trench;

depositing a metal layer within the trench and adjacent to the first

10 ferromagnetic cladding region within the trench;

depositing a second ferromagnetic cladding region positioned on the metal layer and in contact with the first ferromagnetic cladding region;

forming a gap through one of the first and second ferromagnetic cladding regions; and

15 positioning a magnetoresistive random access memory device proximate to the gap.

10. A method of adjusting the magnitude of the magnetic field produced by a conductive line for programming a magnetoresistive memory device comprising the steps of:

forming a metal interconnect region with a first side, a second side, a third side, and a fourth side, wherein the metal interconnect region includes a metal layer with a width;

positioning a ferromagnetic cladding region with a thickness on the first side, the second side, the third side, and the fourth side of the metal interconnect region;

patterning and etching a trench through the ferromagnetic cladding region wherein the trench has a depth approximately equal to the thickness of the ferromagnetic cladding region and has a width less than the width of the metal layer; and

positioning a magnetoresistive random access memory device adjacent to the trench through the ferromagnetic cladding region.

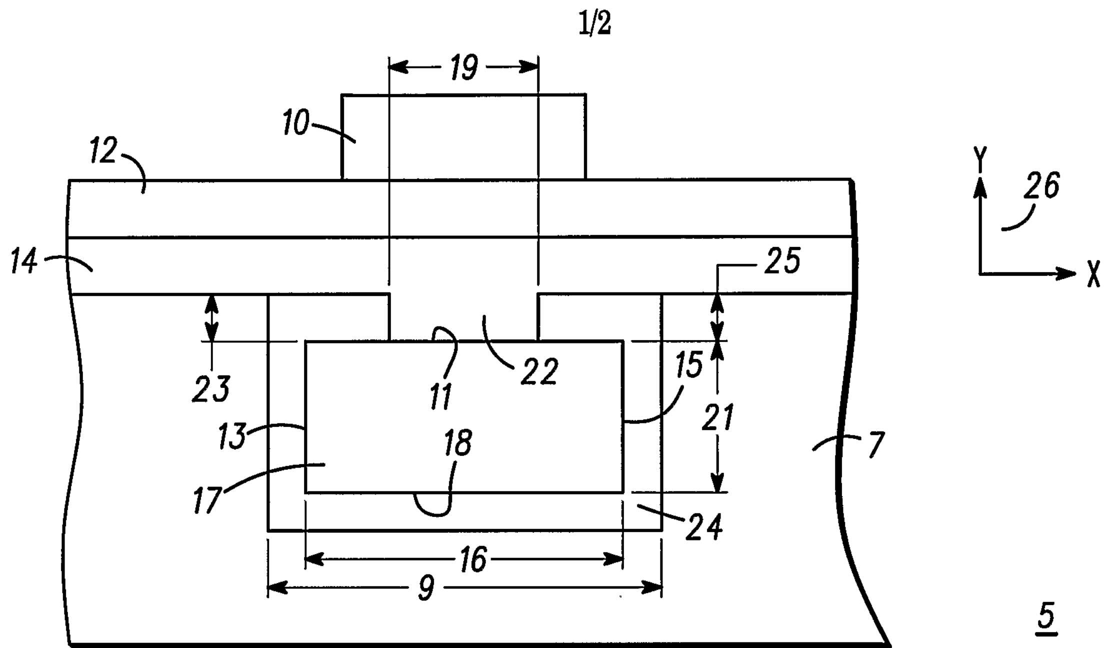


FIG. 1

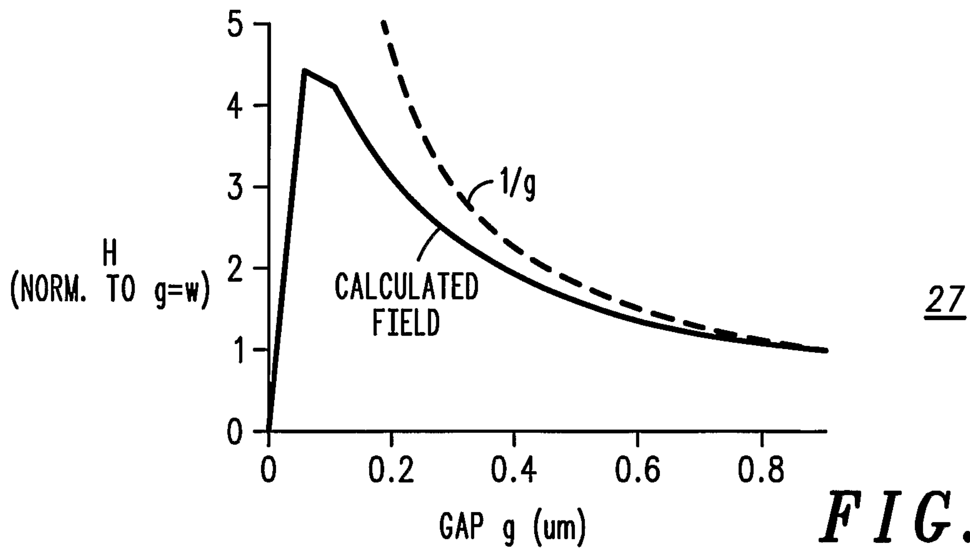


FIG. 2

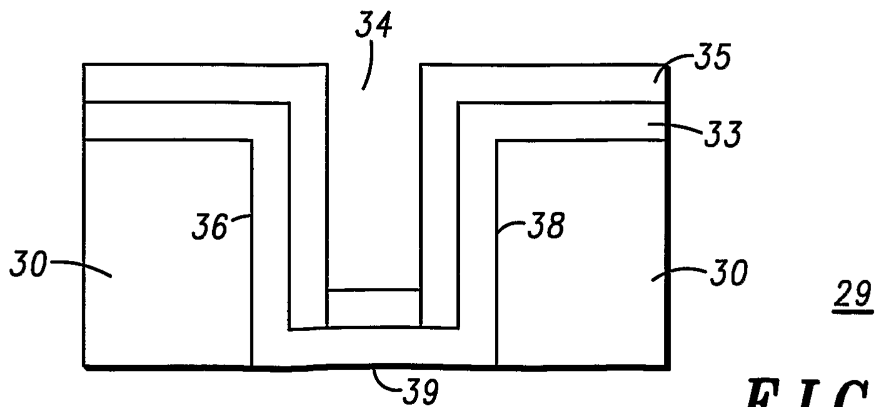


FIG. 3

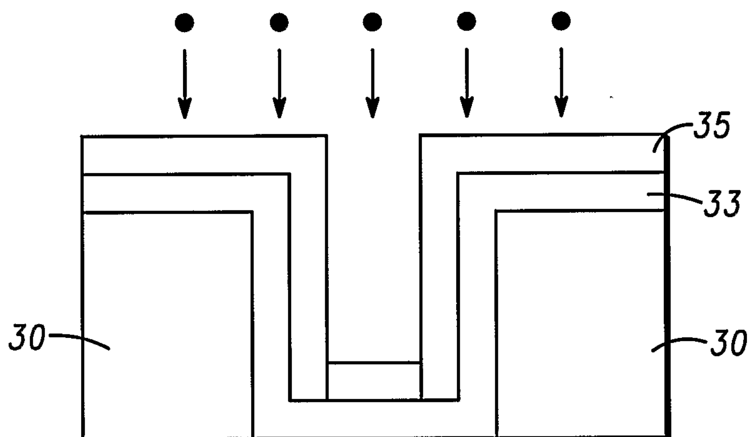


FIG. 4

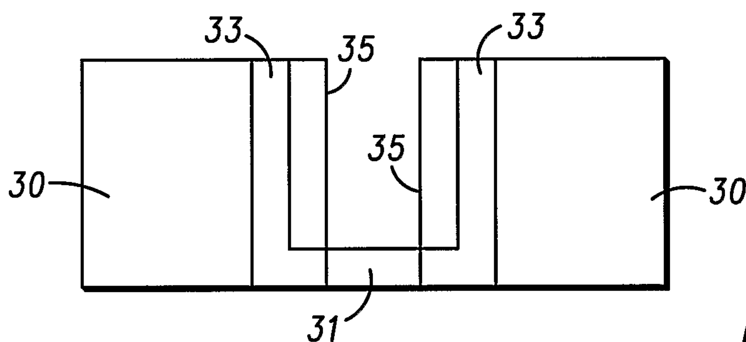


FIG. 5

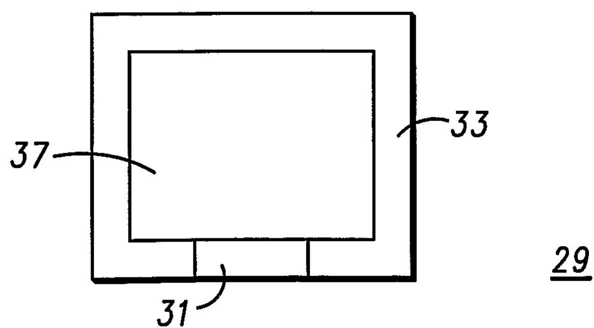


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/34954

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/16 G11C11/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 659 499 A (CHEN EUGENE ET AL) 19 August 1997 (1997-08-19) column 3, line 46 -column 4, line 6; figure 1	1-10
P,A	US 6 430 085 B1 (RIZZO NICHOLAS D) 6 August 2002 (2002-08-06) abstract; figure 3	1-10
P,A	WO 02 054407 A (MOTOROLA INC) 11 July 2002 (2002-07-11) page 14, line 14 -page 15, line 23; figure 13	1-10
A	US 3 922 651 A (KOBAYASHI TOSHIHIKO ET AL) 25 November 1975 (1975-11-25) column 1, line 50 -column 2, line 58; figure 1	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 February 2003	04/03/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Gaertner, W

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 02/34954

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5659499	A	19-08-1997	EP	0776011 A2	28-05-1997
			JP	9204770 A	05-08-1997
US 6430085	B1	06-08-2002	NONE		
WO 02054407	A	11-07-2002	US	6351409 B1	26-02-2002
			WO	02054407 A2	11-07-2002
US 3922651	A	25-11-1975	JP	49065742 A	26-06-1974
			GB	1412313 A	05-11-1975