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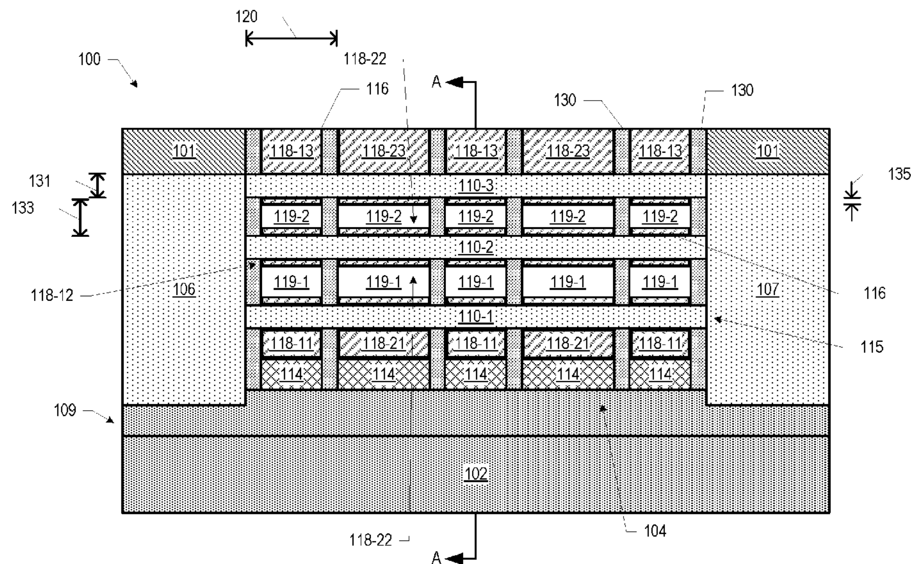

FIG. 1A

(57) Abstract: Disclosed herein are quantum nanowire devices, and related methods and computing devices. In some embodiments, a quantum nanowire device may include: a first nanowire and a second nanowire arranged in a vertical array; a first gate at least partially wrapped around the first nanowire but not around the second nanowire; and a second gate at least partially wrapped around the second nanowire but not around the first nanowire, wherein the second gate is at least partially above the first gate.

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QUANTUM NANOWIRE DEVICES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1A-1D are various views of a quantum nanowire device having embedded epi carrier reservoirs, in accordance with some embodiments.

[0004] FIGS. 1E-1F are various views of a variant of the quantum nanowire device of FIGS. 1A-1D without embedded epi carrier reservoirs, in accordance with some embodiments.

[0005] FIGS. 1G-1H are cross-sectional views of example quantum nanowire devices including multiple vertical arrays of nanowires with various gate arrangements, in accordance with some embodiments.

[0006] FIGS. 1I-1J are cross-sectional views of a variant of the quantum nanowire device of FIGS. 1A-1D in which the gates do not surround the nanowires, in accordance with some embodiments.

[0007] FIGS. 2A-2D, 3A-3D, 4A-4D, 5A-5D, 6A-6D, 7A-7D, 8A-8D, 9A-9D, 10A-10D, 11A-11D, 12A-12D, 13A-13D, 14A-14D, 15A-15D, 16A-16D, 17A-17D, 18A-18D, 19A-19D, and 20A-20D are various views of assemblies in different stages of the manufacture of a quantum nanowire device, in accordance with various embodiments.

[0008] FIGS. 21A-21D are various views of another embodiment of a quantum nanowire device having embedded epi carrier reservoirs, in accordance with some embodiments.

[0009] FIGS. 21E-21F are various views of a variant of the quantum nanowire device of FIGS. 21A-21D without embedded epi carrier reservoirs, in accordance with some embodiments.

[0010] FIG. 22 is a flow diagram of an example method of manufacturing a quantum nanowire device, in accordance with various embodiments.

[0011] FIG. 23 is a flow diagram of an example method of operating a quantum nanowire device, in accordance with various embodiments.

[0012] FIG. 24 is a cross-sectional view of a quantum nanowire device with multiple interconnect layers, in accordance with various embodiments.

[0013] FIG. 25 is a cross-sectional view of a quantum nanowire device package, in accordance with various embodiments.

[0014] FIGS. 26A and 26B are top views of a wafer and dies that may include any of the quantum nanowire devices disclosed herein.

[0015] FIG. 27 is a cross-sectional side view of a device assembly that may include any of the quantum nanowire devices disclosed herein.

[0016] FIG. 28 is a block diagram of an example quantum computing device that may include any of the quantum nanowire devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0017] Disclosed herein are quantum nanowire devices, and related methods and computing devices. In some embodiments, a quantum nanowire device may include: a first nanowire and a second nanowire arranged in a vertical array; a first gate at least partially wrapped around the first nanowire but not around the second nanowire; and a second gate at least partially wrapped around the second nanowire but not around the first nanowire, wherein the second gate is at least partially above the first gate.

[0018] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0019] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike some previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), enhanced electrostatic control over quantum dot formation, good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0020] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the disclosed subject matter. However, the order of

description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0021] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, a "high-k dielectric material" may refer to a material having a higher dielectric constant than silicon oxide.

[0022] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide.

[0023] The accompanying drawings are not necessarily drawn to scale. For ease of discussion, the term "FIG. 1" may be used to refer to the collection of drawings of FIGS. 1A-1J, the term "FIG. 2" may be used to refer to the collection of drawings of FIGS. 2A-2D, etc.

[0024] FIGS. 1A-1D illustrate various views of a quantum nanowire device 100, in accordance with some embodiments. FIG. 1A is a side cross-sectional view of the device 100 along the nanowires 110, FIG. 1B is a cross-sectional view taken through the section A-A of FIG. 1A (through the central gate electrodes 118-1), FIG. 1C is a side view taken toward the carrier reservoir 106, and FIG. 1D is a top view. Although only a single device 100 is depicted in FIG. 1, this is simply for ease of illustration, and an electrical device may include any number of the devices 100 (e.g., in an array or any other desired arrangement).

[0025] The device 100 may include a substrate 102 having a top surface 104. Embedded epi carrier reservoirs 106 and 107 may be disposed on the top surface 104 of the substrate 102, and one or more nanowires 110 may be coupled between the embedded epi carrier reservoirs 106 and 107. For illustrative purposes, three nanowires 110 (labeled 110-1, 110-2, and 110-3) are illustrated in FIGS. 1A-1D. An insulator 101 may be disposed around the embedded epi carrier reservoirs 106 and 107. The insulator 101 may be an interlayer dielectric (ILD), such as undoped silicon oxide, doped silicon oxide (e.g., borophosphosilicate glass (BPSG) or phosphosilicate glass (PSG)), silicon nitride, silicon

oxynitride, or any combination. An insulator 119 may be disposed between vertically adjacent ones of the gate electrodes 118; in FIG. 1, the insulator 119 between the nanowires 110-1 and 110-2 is labeled 119-1, and the insulator 119 between the nanowires 110-2 and 110-3 is labeled 119-2. The insulator 119 may take the form of any of the embodiments of the insulator 101.

[0026] The device 100 may include multiple gate electrodes 118. Each gate electrode 118 may at least partially wrap around one or more of the nanowires 110, and a gate dielectric 116 may be disposed between the gate electrode 118 and the adjacent portions of the associated nanowire(s) 110. As used herein, a nanowire 110 around which a gate electrode 118 at least partially wraps may be referred to as "under" the gate electrode 118. FIG. 1 illustrates fifteen gate electrodes 118, with three sets of gate electrodes 118 labeled 118-1x (e.g., 118-11, 118-12, and 118-13) and two sets of gate electrodes labeled 118-2x (e.g., 118-21, 118-22, and 118-23). The sets of gate electrodes 118-1x are arranged alternatingly with the sets of gate electrodes 118-2x; for east of exposition, a set of gate electrodes 118-1x may be referred to herein as "the gate electrodes 118-1" and a set of gate electrodes 118-2x may be referred to herein as "the gate electrodes 118-2." As discussed below with reference to FIGS. 2-20, the gate electrodes 118-1 may be formed together as part of a first group of manufacturing operations, and the gate electrodes 118-2 may be formed together as part of a second group of manufacturing operations. In some embodiments, spacers 130 may separate horizontally adjacent ones of the gate electrodes 118 from each other, and insulator 119 may separate vertically adjacent ones of the gate electrodes 118 from each other. In some embodiments, portions of sacrificial material 170 may separate horizontally adjacent gate electrodes 118 (e.g., as discussed below with reference to FIG. 21).

[0027] As noted above, the gate electrodes 118 may at least partially wrap around one or more of the nanowires 110. In the embodiment of FIGS. 1A-1D, each gate electrode 118 fully wraps around (or "surrounds") one of the nanowires 110. As used herein, a gate electrode may be said to "at least partially wrap around" a nanowire if that gate electrode at least partially wraps around a longitudinal portion of the nanowire; similarly, a gate electrode may be said to "surround" a nanowire if that gate electrode surrounds a longitudinal portion of the nanowire. For example, as shown in FIG. 1B, the gate electrodes 118-11 surround the nanowire 110-1, the gate electrodes 118-12 surround the nanowire 110-2, and the gate electrodes 118-13 surround the nanowire 110-3. Similarly, in the embodiment of FIGS. 1A-1D, the gate electrodes 118-21 surround the nanowire 110-1, the gate electrodes 118-22 surround the nanowire 110-2, and the gate electrodes 118-23 surround the nanowire 110-3. The gate electrodes 118 need not surround an associated nanowire 110; for example, FIGS. 1I and 1J are views of a device 100 in which the gate electrodes 118 do not surround the nanowires 110 with which they are associated, but partially wrap around the

nanowires 110 (e.g., around two opposing "faces" of a nanowire 110, or three "faces" of a nanowire 110), as discussed in further detail below.

[0028] The nanowires 110 included in the device 100 may be arrayed in the z-direction (i.e., the direction of the thickness 131), and may provide wires in which a two-dimensional electron gas (2DEG) may form to enable the generation of a quantum dot during operation of the device 100, as discussed in further detail below. The nanowires 110 themselves may provide a geometric constraint on the x-location (i.e., the direction into the page of the drawing of FIG. 1A) and the z-location of quantum dots. To control the y-location (i.e., the direction of the length 120) of quantum dots in the nanowires 110, voltages may be applied to the gate electrodes 118 to adjust the energy profiles along the nanowires 110 in the x-direction and thereby constrain the x-location of quantum wells (and therefore quantum dots) within the nanowires 110.

[0029] In some embodiments, the top surface 104 of the substrate 102, the embedded epi carrier reservoirs 106 and 107, and the nanowires 110 each comprise a material having a lattice constant. The lattice constant of the top surface 104 may be different from the lattice constants of the embedded epi carrier reservoirs 106 and 107 and the nanowires 110. In a particular embodiment, the lattice constants of the embedded epi carrier reservoirs 106 and 107 and the nanowires 110 may be larger than the lattice constant of the top surface 104. In one such embodiment, the top surface 104 of substrate 102 may be silicon germanium, the nanowires 110 are undoped germanium, and the embedded epi carrier reservoirs 106 and 107 are germanium. The lattice mismatch (e.g., the lattice constant mismatch) between the embedded epi carrier reservoirs 106 and 107, the nanowires 110, and the top surface 104 may result in lattice stress in the nanowires 110 and in the embedded epi carrier reservoirs 106 and 107. In one embodiment, the nanowires 110 and the embedded epi carrier reservoirs 106 and 107 may be uniaxially lattice-stressed in a direction parallel to the length 120 of the nanowires 110, and may be lattice-relaxed in a direction perpendicular to the length 120 of the nanowires 110. The lattice constant mismatch between the top surface 104 and the embedded epi carrier reservoirs 106 and 107 may also result in the embedded epi carrier reservoirs 106 and 107 providing a force on the nanowires 110. This force may help to maintain the uniaxial lattice stress in the nanowires 110.

[0030] In some embodiments, the nanowires 110 may be formed from a single-crystalline material having a carrier mobility that is greater than the carrier mobility of single crystalline bulk silicon. The higher carrier mobility allows may allow the device 100 to achieve higher drive currents and greater performance. In a particular embodiment, the nanowires 110 may be undoped germanium. The absence of dopants may reduce the scattering of charge carriers, and may help to improve carrier mobility in the nanowires 110.

[0031] In some embodiments, the top surface 104 of the substrate 102 may be recessed beneath the top surface of the shallow trench isolation (STI) layer 105, forming a trench 108 in which the embedded epi carrier reservoirs 106 and 107 are disposed. Forming the embedded epi carrier reservoirs 106 and 107 in the trench 108 may help to confine the growth of the embedded epi carrier reservoirs 106 and 107 during fabrication. However, the embedded epi carrier reservoirs 106 and 107 need not necessarily be formed in a trench; in some embodiments, for example, the top surface 104 of the substrate 102 may be planar with or above STI region 103, and the embedded epi carrier reservoirs 106 and 107 may be disposed on that top surface 104. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be <111>-faceted such that the width 122 at the bottom of the embedded epi carrier reservoirs 106 and 107 is greater than the width 124 at the top of embedded epi carrier reservoirs 106 and 107. In such an embodiment, the plane corresponding to sidewalls 126 and 128 may be the <111> lattice orientation of the embedded epi carrier reservoirs 106 and 107.

[0032] In some embodiments, the device 100 may include a bottom gate isolation material 114 disposed on the top surface 104 of the substrate 102 and under the bottom-most nanowire 115. The bottom gate isolation material 114 may serve as a capacitive isolation barrier to prevent parasitic coupling between the top surface 104 and the gate electrodes 118. The effectiveness of the bottom gate isolation material 114 as a capacitive isolation barrier may depend at least in part on its thickness and material composition. In some embodiments, the bottom gate isolation material 114 may include any dielectric material, such as silicon oxide, silicon nitride, silicon oxynitride, low-k dielectric materials, etc. In some particular embodiments, the bottom gate isolation material 114 may include a silicon oxide layer. In some embodiments, the thickness of the bottom gate isolation material 114 may be sufficiently thick so as to isolate the top surface 104 from capacitive coupling by the gate electrodes 118. In a particular embodiment, bottom gate isolation material 114 is between 100 angstroms and 300 angstroms.

[0033] In some embodiments, the substrate 102 may include one or more epitaxial single crystalline semiconductor layers (e.g., silicon, germanium, silicon germanium, gallium arsenide, indium phosphide, indium gallium arsenide, aluminum gallium arsenide, etc.) grown atop a distinct crystalline substrate (silicon, germanium, gallium arsenide, sapphire, etc.). In one such embodiment, the epitaxially grown semiconductor layers may provide one or more buffer layers 109 having lattice constants different from the distinct crystalline substrate. The buffer layers 109 may serve to grade the lattice constant from the distinct crystalline substrate to the top surface 104. For example, the substrate 102 may include epitaxially grown silicon germanium (SiGe) buffer layers 109 on a distinct crystalline silicon substrate. The germanium concentration of the SiGe buffer layers 109 may

increase their germanium content from the bottom-most buffer layer to the top-most buffer layer (e.g., from 0% germanium to 40% germanium), thereby gradually increasing the lattice constant of the substrate 102. In some embodiments, the buffer layers 109 may have a thickness between 500 nanometers and 1.5 micrometers.

[0034] STI regions 103 may be disposed on the substrate 102. STI regions 103 may serve to reduce current leakage between devices 100 formed adjacent to one another. An STI layer 105 may be disposed in the STI regions 103. The STI layer 105 may include any appropriate dielectric material, such as silicon oxide, silicon nitride, silicon oxynitride, a low-k dielectric, and any combination thereof.

[0035] The nanowires 110 may be disposed above the top surface 104 of the substrate 102, and between the embedded epi carrier reservoirs 106 and 107. Although three nanowires 110 are depicted in FIG. 1, a device 100 may include any suitable number of nanowires 110 (e.g., more or less than three). The nanowires 110 may be formed from a material that can be reversely altered from an insulating state to a conductive state by applying external electric fields. For example, the nanowires 110 may include Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, InP, and/or carbon nanotubes. In some particular embodiments, the nanowires 110 may include an undoped lattice-stressed single crystalline semiconductor material having a carrier mobility greater than single crystalline silicon. The absence of dopants in such nanowires 110 may reduce scattering of charge carriers and may help to improve carrier mobility and thus increase drive current. Lattice stress in the nanowires 110 may also enhance carrier mobility and improve device performance. In some embodiments, the nanowires 110 may be compressively stressed for enhanced hole mobility in p-type devices 100, and may be tensilely stressed for enhanced electron mobility in n-type devices 100. In some embodiments, the nanowires 110 may be a doped single crystalline semiconductor material. For example, the nanowires 110 may be formed of doped single crystalline silicon.

[0036] The nanowires 110 may run parallel to the top surface 104, and multiple nanowires 110 may form a vertical array of nanowires. In some embodiments, the number of nanowires 110 between the embedded epi carrier reservoirs 106 and 107 is between three and six. The nanowires 110 may have a thickness 131 and a width 132. In some embodiments, the thickness 131 may be between 5 nanometers and 40 nanometers (e.g., between 5 and 10 nanometers, or equal to 10 nanometers). In some embodiments, the width 132 may be between 5 nanometers and 50 nanometers. The length 120 of different ones of the gate electrodes 118 may be different, or may be the same; in some embodiments, the length 120 may be between 10 nanometers and 100 nanometers (e.g., between 20 nanometers and 40 nanometers, or equal to 30 nanometers). In some embodiments, the nanowires 110 may be ribbon-shaped nanowires in that the width 132 is greater than the

thickness 131 of the nanowires 110. In some embodiments, the spacing 133 between adjacent nanowires 110 may be between 5 and 200 nanometers (e.g., between 5 and 15 nanometers, between 5 and 20 nanometers, or between 5 and 100 nanometers). In some embodiments, the cross-section of the nanowires 110 may be circular or oval-shaped rather than rectangular; thus, while various ones of the drawings illustrate the nanowires 110 as being rectangular with distinct "faces," this is simply for ease of illustration, and the nanowires 110 may have a more rounded shape when manufactured.

[0037] In some embodiments in which a gate electrode 118 surrounds a nanowire 110, the thickness 135 of the gate electrode 118 in the region between the nanowire 110 and a vertically adjacent nanowire 110 may be relatively small so as not to compromise desired quantum interference between quantum dots that form in the nanowire 110 and the vertically adjacent nanowire 110. For example, in some embodiments, the thickness 135 may be between 5 nanometers and 20 nanometers. FIGS. 1A and 1B illustrate one such thickness 135, for ease of illustration.

[0038] In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be disposed at opposite ends of the nanowires 110 and may be electrically coupled to the nanowires 110. The embedded epi carrier reservoirs 106 and 107 may be formed of any suitable material. For example, the embedded epi carrier reservoirs 106 and 107 may include an epitaxially grown single crystalline semiconductor such as, but not limited to, Si, Ge, GeSn, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, GaN, GaP, or InP. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may include a single crystalline semiconductor material having a lattice constant different from the lattice constant of the top surface 104 of the substrate 102. As previously described, the lattice constant mismatch between the embedded epi carrier reservoirs 106 and 107 and the top surface 104 may create lattice stress in the embedded epi carrier reservoirs 106 and 107, thereby improving electron mobility. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be uniaxially lattice-stressed in a direction parallel to the length 120, but lattice-relaxed in a direction perpendicular to the length 120. The lattice constant mismatch between the embedded epi carrier reservoirs 106 and 107 and the top surface 104 of the substrate 102 may also cause the embedded epi carrier reservoirs 106 and 107 to exert a force on the nanowires 110, which may help to maintain the lattice stress in the nanowires 110. In some embodiments, the embedded epi carrier reservoirs 106 and 107 are formed from the same single crystalline semiconductor material used to form the nanowires 110.

[0039] In some embodiments, the lattice constant of the embedded epi carrier reservoirs 106 and 107 may be larger than the lattice constant of the top surface 104 of the substrate 102. In such an

embodiment, the embedded epi carrier reservoirs 106 and 107 may be compressively stressed and may provide a compressive force on the nanowires 110. In a specific example of such an embodiment, the embedded epi carrier reservoirs 106 and 107 may be epitaxial single crystalline germanium and the top surface 104 may be epitaxial single crystalline silicon germanium. In this example, the germanium carrier reservoirs 106 and 107 may exert a compressive force on the nanowires 110. In some embodiments, the top surface 104 of the substrate 102 may include a semiconductor material (e.g., silicon germanium) having a first lattice constant, the nanowires 110 may include a second semiconductor material (e.g., germanium) having a second lattice constant greater than the first lattice constant, and the embedded epi carrier reservoirs 106 and 107 may include a third semiconductor material (e.g., gallium arsenide (GaAs)) having a third lattice constant greater than the second lattice constant to further enhance the compressive stress in the nanowires 110.

[0040] In some embodiments, the lattice constant of the embedded epi carrier reservoirs 106 and 107 may be smaller than the lattice constant of the top surface 104 of the substrate 102. In such an embodiment, the embedded epi carrier reservoirs 106 and 107 may be tensilely stressed and may provide a tensile force on the nanowires 110. In some such embodiments, the top surface 104 of the substrate 102 may include a single-crystalline semiconductor material having a first lattice constant, the nanowires 110 may include a second semiconductor material having a second lattice constant less than the first lattice constant, and the embedded epi carrier reservoirs 106 and 107 may include a third semiconductor material having a third lattice constant less than the second lattice constant to further enhance the tensile stress in the nanowires 110.

[0041] The embedded epi carrier reservoirs 106 and 107 may have an n-type conductivity or a p-type conductivity. In some embodiments, the embedded epi carrier reservoirs 106 and 107 have a doping concentration between $1x10^{18}$ atoms/cm^3 to $1x10^{21}$ atoms/cm^3. The embedded epi carrier reservoirs 106 and 107 may have a uniform doping concentration or may include sub-regions of different concentrations or dopant profiles. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may have the same doping concentration profile; in other embodiments, the doping concentration profiles of the embedded epi carrier reservoirs 106 and 107 may differ from each other.

[0042] The term "embedded epi" is used herein in reference to some embodiments of the carrier reservoirs 106 and 107 when those regions are formed, as described in greater detail below, by first removing portions of the fin used to create the nanowires 110 and then epitaxially growing the carrier reservoirs 106 and 107. For example, in some embodiments, portions of the fin used to create the nanowires 110 may be removed, and then the carrier reservoirs 106 and 107 may be

epitaxially grown from the top surface 104 of the substrate 102. The lattice of this epitaxially deposited carrier reservoirs 106 and 107 may continue from the lattice of the top surface 104 of the substrate 102. That is, the lattice of the underlying substrate 102 may dictate the lattice direction and growth of the overlying "embedded epi" carrier reservoirs 106 and 107. The use of embedded epi carrier reservoirs 106 and 107 may improve device performance in some embodiments by providing an additional force to the nanowires 110. In some embodiments, the use of embedded epi carrier reservoirs 106 and 107 may also improve performance by providing anchors to the nanowires 110 that help maintain the uniaxial stress in the nanowires 110 already present from earlier fabrication processes, such as fin patterning. The embedded epi carrier reservoirs 106 and 107 may be stressed and, thus, may further stress the adjacent nanowires 110. The stress in the nanowires 110 may be further enhanced by using a material for the embedded epi carrier reservoirs 106 and 107 that has a different lattice constant than the material used to form the nanowires (e.g., different semiconductor materials).

[0043] Other embodiments of the device 100 disclosed herein do not include embedded epi carrier reservoirs 106 and 107. FIGS. 1E and 1F illustrate such an embodiment; in particular, FIG. 1E is a side cross-sectional view of the device 100 along the nanowires 110 (analogous to the view of FIG. 1A), and FIG. 1F is a side view taken toward the carrier reservoir 156 (analogous to the view of FIG. 1C). In some embodiments, as illustrated in FIGS. 1E and 1F, the device 100 may include carrier reservoirs 156 and 157 formed from a thin film stack used to create the nanowires 110. For example, the carrier reservoirs 156 and 157 may be formed from alternating layers of semiconductor material 160 and sacrificial material 170 (e.g., germanium and silicon germanium, respectively). In this example, the carrier reservoirs 156 and 157 may be formed from a heterogeneous stack of single crystalline semiconductor films. The carrier reservoirs 156 and 157 may be doped to a desired conductivity type and level. Additionally, if desired, raised carrier reservoirs 156 and 157 may be formed by depositing additional epitaxial semiconductor material (not shown) on the illustrated carrier reservoirs 156 and 157 to increase the thickness of the carrier reservoirs 156 and 157 to decrease current crowding and thereby reduce the contact resistance of the device 100.

[0044] In the device 100, a gate dielectric 116 may be disposed between each nanowire 110 and its associated gate electrode(s) 118. The gate dielectric 116 may include any suitable gate dielectric, such as, but not limited to, SiO_2, SiON, and SiN. In some embodiments, the gate dielectric 116 may include a high-k gate dielectric layer, such as a metal oxide dielectric (e.g., Ta_2O_5, TiO_2, HfO_2, $HfSiO_x$, ZrO_2, etc.). The gate dielectric 116 may also include other types of high-k dielectric layers, such as, but not limited to, lead zirconate titanate (PZT) or barium strontium titanate (BST). The gate dielectric 116 may include any combination of the above dielectric materials; in some embodiments,

the gate dielectric 116 may include multiple different layers of dielectric materials. In some embodiments, the gate dielectric 116 may have a thickness between 10 angstroms and 60 angstroms. In a specific embodiment, the gate dielectric 116 includes HfO_2 and has a thickness between 1 nanometer and 6 nanometers.

[0045] As discussed above, the device 100 may include multiple gate electrodes 118. Each gate electrode 118 may at least partially wrap around a portion of one or more of the nanowires 110, and the gate dielectric 116 may be disposed between the gate electrodes 118 and the associated nanowires 110. A gate may include a gate electrode 118 and the gate dielectric 116 disposed between the gate electrode 118 and the nanowire 110 associated with the gate electrode 118. The gate electrodes 118 may be formed of any suitable gate electrode material. For example, in some embodiments, the gate electrodes 118 may include a superconducting material. In some embodiments, the gate electrodes 118 may include a metal such as, but not limited to, Ti, TiN, TaN, W, Ru, TiAl, or any combination thereof. In some embodiments, the gate electrodes 118 may be formed from a material having a work function between 3.9 eV and 4.2 eV. In some embodiments, the gate electrodes 118 may be formed from a material having a work function between 4.8 eV and 5.2 eV. In some embodiments in which the nanowires 110 are undoped or very lightly doped, the gate electrodes 118 may be formed from a material having a mid-gap work function between 4.3 eV and 4.7 eV.

[0046] Although FIGS. 1A-1F illustrate a single "vertical" array of nanowires 110, a device 100 may include multiple vertical arrays of nanowires 110, arranged in any manner in the x-, y-, and z-directions. FIGS. 1G-1H are cross-sectional views of example quantum nanowire devices including multiple vertical arrays of nanowires with various gate arrangements, in accordance with some embodiments; in particular, FIGS. 1G and 1H are side cross-sectional views of different examples of the device 100 along the nanowires 110 (analogous to the view of FIG. 1A).

[0047] In FIG. 1G, three vertical arrays of nanowires 110 (labeled 110-xa, 110-xb, and 110-xc, respectively, where x takes the values 1, 2, and 3), are arranged parallel to the length 120 and in the same z-plane. A gate electrode 118-1 surrounds the nanowires 110-1y (where y takes the values a, b, and c, and thus the nanowires 110-1y represent a horizontal "row" of nanowires 110), a different gate electrode 118-2 surrounds the nanowires 110-2y (a different "row" of nanowires 110), and a different gate electrode 118-3 surrounds the nanowires 110-1y (a different "row" of nanowires 110). In other embodiments, one or more of the gate electrodes 118-1 may partially wrap around, but not surround, the associated nanowire 110 (e.g., as discussed below with reference to FIGS. 2I-2J). Other gate electrodes 118-2 in the device 100 may also partially wrap around or surround some or all of the nanowires 110. FIG. 1H depicts another embodiment including three vertical arrays of

nanowires 110 (labeled 110-xa, 110-xb, and 110-xc, respectively, as discussed above); in contrast to FIG. 1G, different gate electrodes 118 at least partially wrap around different ones of the nanowires 110-1y in a row, and horizontally adjacent ones of the depicted gate electrodes 118-1 are isolated by insulator 101. In particular, the gate electrode 118-11a at least partially wraps around the nanowire 110-1a, the gate electrode 118-11b at least partially wraps around the nanowire 110-1b, the gate electrode 118-11c at least partially wraps around the nanowire 110-1c, the gate electrode 118-12a at least partially wraps around the nanowire 110-2a, the gate electrode 118-12b at least partially wraps around the nanowire 110-2b, the gate electrode 118-12c at least partially wraps around the nanowire 110-2c, the gate electrode 118-13a at least partially wraps around the nanowire 110-3a, the gate electrode 118-13b at least partially wraps around the nanowire 110-3b, and the gate electrode 118-13c at least partially wraps around the nanowire 110-3c. Other gate electrodes 118-2 in the device 100 may also partially wrap around or surround some or all of the nanowires 110. Any desired number of vertical arrays of nanowires 110 may be included in a device 100, and the gate electrodes 118 may surround subsets of the different vertical arrays in any desired manner. Any of the devices 100 disclosed herein (e.g., those having non-embedded epi carrier reservoirs 106/107) may include multiple vertical arrays of nanowires 110, arranged as illustrated in FIG. 1G, FIG. 1H, or a combination thereof. Additionally, a device 100 may include multiple vertical arrays of nanowires 110 arranged at different z-heights (e.g., by repeating the fabrication operations discussed below at a different z-height in the device 100).

[0048] As noted above, the gate electrodes 118 may at least partially wrap around a portion of one or more nanowires 110, and may, in some embodiments, not surround a nanowire 110. For example, FIGS. 1I and 1J are views of a device 100 in which the gate electrodes 118 do not surround the nanowires 110 with which they are associated, but partially wrap around the nanowires 110. In particular, FIG. 1I is a side cross-sectional view of the device 100 along the nanowires 110 (analogous to the view of FIG. 1A), and FIG. 1J is a cross-sectional view taken through the section A-A of FIG. 1I (analogous to the view of FIG. 1B). In the embodiment illustrated in FIGS. 1I and 1J, the gate electrodes 118-11 wrap around three "faces" of the nanowire 110-1, the gate electrodes 118-12 wrap around two "faces" of the nanowire 110-2, and the gate electrodes 118-13 wrap around three "faces" of the nanowire 110-3. The gate electrodes 118-21, 118-22, and 118-23, although not shown in cross-section in FIGS. 1I and 1J, may wrap around the nanowires 110-1, 110-2, and 110-3, respectively, as discussed above with reference to the gate electrodes 118-11, 118-12, and 118-13, respectively. As noted above, although the nanowires 110 are illustrated herein as being rectangular in cross-section, a manufactured nanowire 110 may have a more rounded or circular cross-section; in such cases, wrapping around different numbers of "faces" may be manifested as different

percentages of the circumference of the nanowire 110 being proximate to or in contact with an associated gate electrode 118 (e.g., approximately 50% (e.g., 40-60%) for wrapping around two "faces", approximately 75% (e.g., 65-80%) for wrapping around three "faces", etc.). In some embodiments, any of the gate electrodes 118 disclosed herein may be proximate to, or in contact with, only one "face" of a nanowire 110 (e.g., approximately 25% (e.g., 15-35%) of the circumference of an associated nanowire 110).

[0049] Different gate electrodes 118 may at least partially wrap around different ones of the nanowires 110 in any desired manner in a device 100. For example, in some embodiments, all of the gate electrodes 118 may surround their associated nanowires 110. In other embodiments, none of the gate electrodes 118 may surround their associated nanowires 110. In other embodiments, some but not all of the gate electrodes 118 may surround their associated nanowires 110.

[0050] During operation of the device 100, voltages may be applied to the gate electrodes 118 to adjust the potential energy in the nanowires 110 to create quantum wells of varying depths in which quantum dots may form; decreasing the potential energy may form quantum wells, while increasing the potential energy, may form quantum barriers. The spacers 130 may themselves provide "passive" barriers between quantum wells within a nanowire 110 under horizontally adjacent ones of the gate electrodes 118; similarly, the insulator 119 may provide passive barriers between quantum wells across different nanowires 110 under vertically adjacent ones of the gate electrodes 118. In some embodiments, the thickness of the spacers 130 (i.e., in the direction of the length 120) may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers).

[0051] The devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots. Note that the polarity of the voltages applied to the gate electrodes 118 to form quantum wells/barriers depends on the charge carriers used in the device 100. In embodiments in which the charge carriers are electrons (and thus the quantum dots are electron-type quantum dots), amply negative voltages applied to a gate electrode 118 may increase the potential barrier in the nanowire 110 under the gate electrode 118, and amply positive voltages applied to a gate electrode 118 may decrease the potential barrier in the nanowire 110 under the gate electrode 118 (thereby forming potential wells in the nanowire 110 in which electron-type quantum dots may form). In embodiments in which the charge carriers are holes (and thus the quantum dots are hole-type quantum dots), amply positive voltages applied to a gate electrode 118 may increase the potential barrier in the nanowire 110 under the gate electrode 118, and amply negative voltages applied to a gate electrode 118 may decrease the potential barrier under the gate electrode 118 (thereby forming potential wells in the nanowire 110 in which hole-type quantum dots may form).

[0052] Voltages may be applied to each of the gate electrodes 118 separately to adjust the potential energy in the nanowires 110 under the gate electrodes 118, and thereby control the formation of quantum dots in the nanowires 110. Additionally, the relative potential energy profiles in the nanowires 110 under different ones of the gate electrodes 118 allow the device 100 to tune the interaction between quantum dots under different gate electrodes 118 in the nanowires 110. For example, if a first quantum dot is formed in a nanowire 110 under a first gate electrode 118 and another quantum dot is formed in the same or a different nanowire 110 under a second, different gate electrode 118, and these quantum dots are separated by only a low potential barrier, the two quantum dots may interact more strongly than if they were separated by a taller potential barrier. Since the depth of the potential wells/height of the potential barriers under each gate electrode 118 may be adjusted by adjusting the voltages on the respective gate electrodes 118 and neighboring gate electrodes 118, the differences in potential between various gate electrodes 118 may be adjusted, and thus the interaction tuned. A quantum dot formed in one nanowire 110 under one gate electrode 118 may interact with quantum dots formed in other nanowires 110 under the same gate electrode 118, quantum dots formed in the same nanowire 110 under different gate electrodes 118, and/or quantum dots formed in other nanowires 110 under the same gate electrode 118, as desired. In some embodiments, a quantum dot formed in one nanowire 110 under one gate electrode 118 may interact with another quantum dot formed in another adjacent nanowire 110 under a "diagonal" gate electrode 118; for example, a quantum dot formed in the nanowire 110-2 under the gate electrode 118-12 may interact with a quantum dot formed in the nanowire 110-3 under the gate electrode 118-23. In some applications, the gate electrodes 118-2 may be used as plunger gates to enable the formation of quantum dots under the gate electrodes 118-2, while the gate electrodes 118-1 may be used as barrier gates to adjust the potential barrier between quantum dots formed under adjacent gate electrodes 118-2 (or vice versa). Conductive vias and lines (not shown in FIG. 1) may make contact with the gate electrodes 118 and the carrier reservoirs 106 and 107 to enable electrical connections to these elements; such conductive pathways are discussed in further detail below with reference to FIGS. 24 and 25.

[0053] The devices 100 disclosed herein may be fabricated using any suitable techniques. For example, FIGS. 2-20 provide various views of assemblies in different stages of the manufacture of a quantum nanowire device, in accordance with various embodiments. In FIGS. 2-20, the "A" sub-figures represent a cross-sectional view analogous to that of FIG. 1A (and FIG. 1E), the "C" sub-figures represent a cross-sectional view analogous to that of FIG. 1C (and FIG. 1F), and the "D" sub-figures represent a top view analogous to that of FIG. 1D. In FIGS. 2-16, the "B" sub-figures

represent a cross-sectional view analogous to that of FIG. 1B; in FIGS. 17-20, the "B" sub-figures represent a cross-sectional view through the section C-C of the corresponding "A" sub-figures.

[0054] FIG. 2 depicts an assembly 200 including a substrate 102 with a fin 244 formed thereon. The substrate 102 may provide the material upon which the device 100 is formed. The substrate 102 may have a top surface 104 with a lattice constant. In some embodiments, the substrate 102 may include a top single-crystalline layer having a lattice constant. In some such embodiments, the substrate 102 may include one or more buffer layers 109 grown between a distinct single-crystalline substrate and the top single-crystalline layer. The buffer layers 109 may serve to gradually change the lattice constant from that of the distinct crystalline substrate to that of the top single-crystalline layer. The buffer layers 109 may be formed from epitaxially grown single-crystalline semiconductor materials such as, but not limited to, Si, Ge, GeSn, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, GaN, GaP, or InP. The distinct crystalline substrate on which the buffer layers 109 are formed may be any single-crystalline material having a lattice constant (e.g., silicon, germanium, gallium arsenide, sapphire, etc.). In a particular embodiment, the substrate 102 may include SiGe buffer layers 109 epitaxially grown on a distinct single-crystalline silicon substrate. The substrate 102, the buffer layers 109, and the top surface 104 of the assembly 200 may take any of the forms disclosed herein.

[0055] The fin 244 may include alternating layers of a semiconductor material 160 and a sacrificial material 170. As discussed below, the layers of semiconductor material 160 may be formed into the nanowires 110. The layers of sacrificial material 170 may induce lattice stress on the layers of semiconductor material 160 by being lattice-mismatched to the layers of semiconductor material 160. The layers of semiconductor material 160 and the layers of sacrificial material 170 may be formed from any well-known materials having different lattice constants. In some embodiments, the layers of semiconductor material 160 and the layers of sacrificial material 170 are each formed from a single-crystalline semiconductor material such as, but not limited to, Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, or InP. In some embodiments, the layers of semiconductor material 160 have a lattice constant different from the lattice constants of the layers of sacrificial material 170 and the top surface 104 of the substrate 102. The fin 244 may be lattice-stressed as a result of the lattice mismatch between the top surface 104, the layers of semiconductor material 160, and the layers of sacrificial material 170. In a particular embodiment, the lattice constant of the layers of semiconductor material 160 is larger than the lattice constant of the layers of sacrificial material 170 and the lattice constant of the top surface 104. For example, the layers of semiconductor material 160 may include undoped germanium, the top surface 104 may include silicon germanium having 30% germanium concentration, and the layers of sacrificial

material 170 may include silicon germanium having 30% germanium concentration. In such an embodiment, the lattice mismatch between the materials may result in the layers of semiconductor material 160 being compressively lattice-stressed in the fin 244. In another embodiment, the lattice constant of the layers of semiconductor material 160 is smaller than both the lattice constant of the layers of sacrificial material 170 and the lattice constant of the top surface 104. For example, the layers of semiconductor material 160 may be silicon, the top surface 104 may be silicon germanium, and the layers of sacrificial material 170 may be silicon germanium. In such an embodiment, the lattice constant between the materials may result in the layers of semiconductor material 160 being tensilely lattice-stressed in the fin 244. Since the sacrificial material 170 and the semiconductor material 160 alternate with differing lattice constants, the layers of semiconductor material 160 may be biaxially stressed by the underlying layer(s) of sacrificial material 170.

[0056] The fin 244 may be formed by first blanket-depositing alternating layers of semiconductor material 160 and sacrificial material 170 on the top surface 104 of the substrate 102 using conventional epitaxial chemical vapor deposition (CVD) methods. Next, the blanket layers of semiconductor material 160 and sacrificial material 170 may be patterned using conventional photolithography and etching methods to define the fin 244. In some embodiments, the substrate 102 may also be etched so that a bottom portion of the fin 244 includes a portion of the substrate 102 (e.g., a portion of the buffer layers 109). In this way, the portion of the substrate 102 that is included in the fin 244 may act as the bottom sacrificial material 170 of the fin 244. In an embodiment, the portion of the substrate 102 that is included in the fin 244 is thicker than the other layers of the sacrificial material 170 in order to provide additional room between the substrate 102 and the bottom-most nanowire in the device 100 (not shown) so that a bottom gate isolation material and a gate electrode/gate dielectric may be provided between the substrate 102 and bottom nanowires, as discussed below.

[0057] During patterning of the fin 244, the substrate 102 may also be patterned to form a substrate region 252 continuous with the fin 244. In some embodiments, at least part of the substrate region 252 continuous with the fin 244 may include the buffer layers 109 of the substrate 102.

[0058] The assembly 200 may include an STI layer 105 in STI regions 103; these elements may take any of the forms disclosed herein. In some embodiments, the STI layer 105 may be formed by first blanket-depositing the STI layer 105 on the substrate 102 and over the fin 244 using conventional CVD methods. The STI layer 105 may be initially deposited to a thickness greater than the combined height of the fin 244 and the substrate region 252. Next, the STI layer 105 may be planarized using a conventional chemical mechanical planarization (CMP) method, and then recessed using a

conventional etch method to expose the fin 244. In some embodiments, the STI layer 105 may be recessed below the top surface 104 of the substrate 102 so that the bottom portion of the fin 244 is formed from the substrate 102, as illustrated. In this way, the fin 244 may include a substrate portion that may act as the bottom-most layer of sacrificial material 170, as discussed above. Alternatively a distinct sacrificial layer may be formed between the top surface 104 and the bottom-most layer of semiconductor material 160.

[0059] The fin 244 may have sidewalls 242 and 246, a fin height 256, a fin width 258, and a fin length 260. In some embodiments, the sidewalls 242 and 246 may be unconstrained planes, which may allow the fin 244 to lattice-relax in the direction perpendicular to the fin length 260. That is, the above-described biaxially stressed layers may be reduced to uniaxially stressed layers upon formation of the fin 244. In some embodiments, the fin 244 may be uniaxially lattice-stressed in a direction parallel to the fin length 260 and lattice-relaxed in a direction perpendicular to the fin length 260. In some embodiments, the fin 244 may have a fin width 258 less than 30 nanometers (e.g., less than 25 nanometers). In some embodiments, the fin height 256 may be between 30 nanometers and 75 nanometers.

[0060] The thicknesses of the layers of semiconductor material 160 and the layers of sacrificial material 170 may influence the electrical characteristics of the device 100. The thicknesses of the layers of sacrificial material 170 may also affect the subsequent spacing between the nanowires 110 and thus the ability of the gate dielectric 116 and the gate electrodes 118 to form all around each nanowire 110. The thicknesses and number of the layers of semiconductor material 160 and the layers of sacrificial material 170 also affect the fin height 256. In some embodiments, the layers of semiconductor material 160 have a thickness between 5 nanometers and 50 nanometers, and the layers of sacrificial material 170 have a thickness between 5 nanometers and 30 nanometers. In some embodiments, the fin 244 may include between three and six layers of semiconductor material 160, and between three and six layers of sacrificial material 170.

[0061] FIG. 3 illustrates an assembly 202 subsequent to providing a sacrificial gate dielectric 262 and a sacrificial gate electrode material 264 over the fin 244 of the assembly 200 (FIG. 2). The sacrificial gate dielectric 262 may be blanket-deposited on top of the fin 244 and the sidewalls 242 and 246 of the fin 244. In some embodiments, the sacrificial gate dielectric 262 may be deposited to a thickness between 10 angstroms and 50 angstroms. A sacrificial gate electrode material 264 may then be blanket-deposited on the sacrificial gate dielectric 262 and over the fin 244. The sacrificial gate electrode material 264 may be deposited to a thickness that exceeds the fin height 256, and then may be planarized using conventional CMP methods.

[0062] FIG. 4 illustrates an assembly 204 subsequent to patterning the sacrificial gate dielectric 262 and the sacrificial gate electrode material 264 of the assembly 202 (FIG. 3) to form multiple sacrificial gate electrodes 266. Conventional photolithography and etching methods may be used to perform this patterning. Although three sacrificial gate electrodes 266 are illustrated in FIG. 4 (and will correspond to the three gate electrodes 118-1 in the device 100, as discussed below), any desired number of sacrificial gate electrodes 266 may be patterned on the fin 244 (and more generally, the device 100 may include any desired number of gate electrodes 118). The sacrificial gate electrodes 266 may serve to protect the underlying regions of the fin 244 during subsequent removal of sacrificial portions 272 of the fin 244, as discussed below.

[0063] During the patterning of the sacrificial gate dielectric 262 and the sacrificial gate electrodes 266, the sacrificial gate dielectric 262 on the sacrificial portions 272 of the fin 244 may be exposed on opposite sides of the sacrificial gate electrode 266. The sacrificial gate dielectric 262 may serve as an etch stop layer during the patterning and formation of the sacrificial gate electrode 266, thereby mitigating damage to the fin 244. In some embodiments, the sacrificial gate dielectric 262 and the sacrificial gate electrode material 264 may be formed from materials that have sufficiently different etch selectivity so that the sacrificial gate dielectric 262 may serve as an etch stop layer for etching the sacrificial gate electrode material 264 to form the sacrificial gate electrodes 266. In a particular embodiment, the sacrificial gate dielectric 262 may be a dielectric layer (e.g., silicon oxide, silicon nitride, and silicon oxynitride) and the sacrificial gate electrode material 264 may be a semiconductor material (e.g., polycrystalline silicon). After patterning the sacrificial gate electrode material 264, the sacrificial gate dielectric 262 may be removed from the top and the sidewalls 242 and 246 of the sacrificial portions 272 of the fin 244 (e.g., using a conventional wet etch process) to expose the sacrificial portions 272 of the fin 244. In an embodiment in which the sacrificial gate dielectric 262 is a silicon oxide layer, the sacrificial gate dielectric 262 may be removed using a dilute hydrogen fluoride (HF) wet etch.

[0064] FIG. 5 illustrates an assembly 206 subsequent to removing the sacrificial portions 272 of the fin 244 of the assembly 204 (FIG. 4) to expose carrier reservoir regions 274 of the substrate 102. The sacrificial portions 272 of the fin 244 may be removed using conventional etching methods, such as wet etching or plasma dry etching. In an embodiment in which the layers of semiconductor material 160 are germanium and the layers of sacrificial material 170 are silicon germanium, a wet etchant such as ammonium hydroxide (NH_4OH) or tetramethylammonium hydroxide (TMAH) solution may be used to selectively etch off the sacrificial portions 272 of the fin 244. The sacrificial gate electrode 266 may protect the underlying portions of the fin 244 during this etch. In an embodiment, the top surface 104 of the substrate 102 may be recessed during the removal of the

sacrificial portions 272 of the fin 244 to form a trench 108. The trench 108 may serve to contain the subsequent growth of the embedded epi carrier reservoirs 106 and 107. In an embodiment, the trench 108 may have a depth between 20 nanometers and 40 nanometers. In some other embodiments, the sacrificial portions 272 of the fin 244 may be removed so that the top surface 104 of the substrate 102 is above or planar with the STI layer 105.

[0065] FIG. 6 illustrates an assembly 208 subsequent to forming the embedded epi carrier reservoirs 106 and 107 on the carrier reservoir regions 274 of the assembly 206 (FIG. 5). In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be formed using conventional epitaxial deposition methods, such as low-pressure CVD, vapor phase epitaxy, or molecular beam epitaxy. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be formed in the trench 108. The embedded epi carrier reservoirs 106 and 107 may electrically couple with the portion of the fin 244 under the sacrificial gate electrode 266, and may rise above the top surface of the STI layer 105. The embedded epi carrier reservoirs 106 and 107 may be formed from any appropriate material, such as any of the materials discussed above.

[0066] As discussed above, the lattice constant mismatch between the embedded epi carrier reservoirs 106 and 107 and the top surface 104 of the substrate 102 may create lattice stress. The stress may take any of the forms disclosed herein. In some embodiments, the embedded epi carrier reservoirs 106 and 107 may be grown from a crystalline surface of a substrate 102 below the fin 244. In the case that the removed outer portions of the fin 244 are heterogeneous (e.g., with alternating nanowire-forming semiconductor material layers 160 and intervening sacrificial material layers 170 of differing composition), replacement of these heterogeneous layers with embedded epi carrier reservoirs 106 and 107 through epitaxial growth may generate a new lattice mismatch on either side of the etched fin 244. The embedded epi carrier reservoirs 106 and 107, then, may further enhance the uniaxial stress already present in the nanowire-forming layers 160. Furthermore, upon subsequent removal of the intervening sacrificial layers 170 (as discussed below), the embedded epi carrier reservoirs 106 and 107 act to anchor the then formed discrete nanowires 110. Since, the embedded epi carrier reservoirs 106 and 107 may be epitaxially grown from the underlying substrate 102, the anchoring may be effective for maintaining the initial uniaxial stress formed along the nanowire-forming layers 160 during patterning of the fin 244. As such, the embedded epi carrier reservoirs 106 and 107 both maintain and enhance the uniaxial stress of the ultimately formed nanowires 110. It is noted that the above substitution of heterogeneous layers with a homogeneous layer may be performed by using the same material as the nanowire-forming layers 160. However, in another embodiment, to further enhance the uniaxial stress, a material different from any of the materials used in the heterogeneous stack of layers (e.g., different from the materials 160 and 170)

may be epitaxially grown to form the embedded epi carrier reservoirs 106 and 107. For example, in one embodiment, the epitaxial carrier reservoirs 106 and 107 are formed from a material having a lattice constant greater than any of the materials in the heterogeneous fin 244. In that embodiment, a uniaxial compressive stress is further enhanced in the ultimately formed nanowires 110. In another embodiment, the epitaxial carrier reservoirs 106 and 107 are formed from a material having a lattice constant less than any of the materials in the heterogeneous fin 244. In that embodiment, a uniaxial tensile stress is further enhanced in the ultimately formed nanowires 110.

[0067] In an embodiment, the top surface 104 of the carrier reservoir regions 274 of the substrate 102 is a single-crystalline material having a <100>-orientation that serves as a seed layer for epitaxial growth of the embedded epi carrier reservoirs 106 and 107. The embedded epi carrier reservoirs 106 and 107 may thus grow in a <100>-orientation. The <111> plane corresponding to the sidewalls 126 and 128 may grow at a more favorable rate during the formation of the embedded epi carrier reservoirs 106 and 107 and may result in the embedded epi carrier reservoirs 106 and 107 being <111>-faceted.

[0068] In alternative embodiments, the sacrificial portions 272 of the fin 244 are not etched away, but are maintained to form carrier reservoirs for the device 100, as illustrated in FIGS. 1E and 1F and discussed above. Instead of removing the sacrificial portions 272, the sacrificial portions 272 of the fin 244 may be doped by any suitable techniques (e.g., ion implantation) to form carrier reservoirs of a desired conductivity type and concentration level. Additionally, an epitaxial semiconductor film may be grown on the top and sidewalls of the carrier reservoir regions 274 of the fin 244 to form raised carrier reservoirs to decrease current crowding, if desired (not shown).

[0069] FIG. 7 illustrates an assembly 210 subsequent to depositing, and then polishing back, an insulator 101 on the assembly 208 (FIG. 6). The insulator 101 may be an interlayer dielectric (ILD), and may be blanket-deposited over all structures, including the embedded epi carrier reservoirs 106 and 107 and the sacrificial gate electrode 266, using any suitable method (e.g., a CVD method, such as plasma enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD)). A CMP method may be performed to polish back the blanket-deposited insulator 101 to expose the top of the sacrificial gate electrode 266.

[0070] FIG. 8 illustrates an assembly 212 subsequent to removing the sacrificial gate electrodes 266 (and the underlying sacrificial gate dielectric 262) of the assembly 210 (FIG. 7) to expose regions 268 of the fin 244. The insulator 101 may protect the embedded epi carrier reservoirs 106 and 107 during the removal of the sacrificial gate electrodes 266. The sacrificial gate electrodes 266 may be removed using a conventional etching method, such as plasma dry etch or a wet etch. In an

embodiment in which the sacrificial gate electrodes 266 include polysilicon and the insulator 101 includes silicon oxide, a wet etchant such as a TMAH solution may be used to selectively remove the sacrificial gate electrodes 266. The sacrificial gate dielectric 262 may serve as an etch stop during the removal of the sacrificial gate electrodes 266, and may be removed using any suitable etching method to expose the regions 268 of the fin 244. In an embodiment in which the sacrificial gate dielectric 262 includes silicon oxide, a dilute HF wet etch may be used to removed sacrificial gate dielectric 262.

[0071] FIG. 9 illustrates an assembly 214 subsequent to removing portions of the layers of sacrificial material 170 between the layers of semiconductor material 160 in the fin 244 under the exposed regions 268 of the assembly 212 (FIG. 8) to form nanowires 110. The portions of the layers of sacrificial material 170 may be removed using any well-known etchant that is selective to the layers of semiconductor material 160 (e.g., the etchant etches the layers of sacrificial material 170 at a significantly higher rate than the layers of semiconductor material 160). In an embodiment, the etchant selectively etches the layers of semiconductor material 160 while not etching the layers of sacrificial material 170. In an embodiment in which the layers of semiconductor material 160 are germanium and the layers of sacrificial material 170 are silicon germanium, the layers of sacrificial material 170 may be selectively removed using a wet etchant such as, but not limited to, ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), or potassium hydroxide (KOH) solution. In an embodiment in which the layers of semiconductor material 160 are silicon and the layers of sacrificial material 170 are silicon germanium, the layers of sacrificial material 170 may be selectively removed using a wet etchant such as, but not limited to, aqueous carboxylic acid/nitric acid/HF solution and aqueous citric acid/nitric acid/HF solution. The removal of the layers of sacrificial material 170 may leave voids 282 between the nanowires 110. The voids 282 between the nanowires 110 may have a thickness between 5 nanometers and 30 nanometers. The remaining layers of semiconductor material 160 form a vertical array of nanowires 110 that are coupled to the embedded epi carrier reservoirs 106 and 107. The nanowires 110 may have a thickness between 5 nanometers and 50 nanometers. The nanowires 110 may run parallel to the top surface 104 and may be aligned with each other to form a single column of nanowires 110 with a bottom-most nanowire 115 at the very bottom of the column. In some embodiments, a timed etch may be utilized to control the removal of the sacrificial material 170.

[0072] FIG. 10 illustrates an assembly 216 subsequent to providing a bottom gate isolation material 114 on the top surface 104 of the substrate 102 under the bottom-most nanowire 115 of the assembly 214 (FIG. 9). The bottom gate isolation material 114 may be formed by first blanket-depositing the bottom gate isolation material 114 around and over the nanowires 110, filling the

voids 282 between the nanowires 110 (including the void 282 between the bottom-most nanowire 115 and the top surface 104 of the substrate 102) and covering the top surface of the insulator 101. In some embodiments, the bottom gate isolation material 114 may be deposited using a highly conformal deposition method, such as LPCVD, atomic layer deposition (ALD), or a spin-on dielectric process to improve the likelihood that the voids 282 between the nanowires 110 are completely filled. The bottom gate isolation material 114 may then be recessed from the top downward using any suitable isotropic dielectric etching method. For example, in embodiments in which the bottom gate isolation material 114 is formed of silicon oxide, a timed HF wet etch method may be used to recess the bottom gate isolation material 114. Generally, the bottom gate isolation material 114 may include any suitable dielectric material such as, but not limited to, silicon oxide, silicon nitride, and silicon oxynitride.

[0073] During the recess of the bottom gate isolation material 114, the majority of the bottom gate isolation material 114 is removed, leaving behind a thin layer on the top surface 104 of the substrate 102 and under the bottom-most nanowire 115. In some embodiments, the thickness of the final bottom gate isolation material 114 may be between 100 angstroms and 300 angstroms.

[0074] FIG. 11 illustrates an assembly 218 subsequent to providing spacers 130, providing a gate dielectric 116 around each nanowire 110 (and along the spacers 130), and providing a gate electrode material 121 on the gate dielectric 116 beneath each of the regions 268 of the assembly 216 (FIG. 10). The gate electrode material 121 may surround each nanowire 110 beneath the corresponding region 268. The gate dielectric 116 may be formed using a highly conformal deposition process (e.g., ALD) in order to ensure the formation of a gate dielectric layer having a uniform thickness around each nanowire 110. In a particular embodiment, the gate dielectric 116 may be HfO_2 and may be deposited to a thickness between 1 nanometer and 6 nanometers. The gate dielectric 116 may be blanket-deposited, and thus may also be present on the top surface of the insulator 101. Next, the gate electrode material 121 may be blanket-deposited on the gate dielectric 116. The gate electrode material 121 may be deposited using a conformal deposition process (e.g., ALD) to ensure that the gate electrode material 121 is provided on the gate dielectric 116 and around and between each nanowire 110. The blanket gate electrode material 121 and gate dielectric 116 deposited on the top of the insulator 101 may then be chemically mechanically planarized until the top surface of the insulator 101 is revealed as shown. The gate electrode material 121 may include any of the materials discussed herein with reference to the gate electrodes 118.

[0075] The assembly 218 also includes a pair of sidewall spacers 130 that bookend the intervening gate dielectric 116 and gate electrode material 121. The pair of sidewall spacers 130 may be formed using conventional methods of forming selective spacers, as known in the art. In some

embodiments, a conformal dielectric spacer layer, such as, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, and combinations thereof, is first blanket-deposited on all structures, including the fin 244. The dielectric spacer layer may be deposited in a conformal manner so that it has substantially equal thicknesses on both vertical surfaces (such as the sidewalls 242 and 246) and horizontal surfaces. The dielectric spacer layer may be deposited using conventional CVD methods such as LPCVD and PECVD, for example. In some embodiments, the dielectric spacer layer may be deposited to a thickness between 2 nanometers and 10 nanometers. Next, an unpatterned anisotropic etch may be performed on the dielectric spacer layer using conventional anisotropic etch methods, such as reactive ion etching (RIE). During the anisotropic etching process, most of the dielectric spacer layer may be removed from horizontal surfaces, leaving the dielectric spacer layer on the vertical surfaces, as shown. Next, an unpatterned isotropic etch may be performed to remove the remaining dielectric spacer layer from any horizontal surfaces, leaving pairs of spacers 130; upon formation of the gate electrodes 118-1 (as discussed below), each gate electrode 118-1 may be "bookended" by a pair of spacers 130. In some embodiments, the isotropic etch is a wet etch process. In a specific embodiment, where the dielectric spacer layer is silicon nitride or silicon oxide, the isotropic etch may employ a wet etchant solution comprising phosphoric acid (H_3PO_4) or a buffered oxide etch (BOE), respectively. In an alternate embodiment, the isotropic etch may be a dry etch process. In one such embodiment, nitrogen trifluoride (NF_3) gas may be employed in a downstream plasma reactor to isotropically etch the dielectric spacer layers.

[0076] Although the spacers 130 are illustrated as having substantially rectangular cross-sections, this is for ease of illustration; in some embodiments, the spacers 130 may be thinner farther from the substrate 102 and thicker closer to the substrate 102. In some embodiments, the spacers 130 may have a convex shape, curving inward toward the associated gate electrode 118-1.

[0077] FIG. 12 illustrates an assembly 220 subsequent to etching back the gate electrode material 121 and the gate dielectric 116 of the assembly 218 (FIG. 11) to form gates including the gate electrodes 118-11 and the remaining gate dielectric 116. The gate electrodes 118-11 may at least partially wrap around portions of the nanowire 110-3, in accordance with any of the embodiments disclosed herein. For example, in FIG. 12, the gate electrodes 118-11 may surround the nanowire 110-1. Portions of the nanowires 110-2 and 110-3 may, however, be exposed in the assembly 220. The spacers 130 may bookend the gate electrodes 118-11, as shown. Any suitable recessing technique may be used to etch back the gate electrode material 121 and the gate dielectric 116 (e.g., a dry etch such as reactive ion etching, or a wet etch).

[0078] FIG. 13 illustrates an assembly 222 subsequent to providing an insulator 119-1 on the gate electrodes 118-11 of the assembly 220 (FIG. 12). The insulator 119-1 may be provided directly on

the gate electrodes 118-11, and in some embodiments, no gate dielectric 116 may be disposed between the insulator 119-1 and the gate electrodes 118-11. In some embodiments, the top surface of the insulator 119-1 may be below the nanowire 110-2, and thus the insulator 119-1 may not contact the nanowire 110-2. In other embodiments, the insulator 119-1 may contact the nanowire 110-2. The height of the insulator 119-1 may depend on the desired geometry for the gate electrode 118-12, as discussed below. In some embodiments, the insulator 119-1 may be blanked deposited and recessed back, while in other embodiments, the insulator 119-1 may be initially deposited to its desired final height.

[0079] FIG. 14 illustrates an assembly 224 subsequent to providing a gate dielectric 116 around each exposed nanowire 110 (and along the exposed faces of the spacers 130), and providing a gate electrode material 123 on the additional gate dielectric 116 around the exposed nanowires 110 of the assembly 222 (FIG. 13). The gate dielectric 116 may take any of the forms discussed above (e.g., with reference to FIG. 11), and the gate electrode material 123 may take the form of any of the embodiments discussed above with reference to the gate electrode material 121. In some embodiments, the gate electrode material 123 may be planarized at the top surface.

[0080] FIG. 15 illustrates an assembly 226 subsequent to etching back the gate electrode material 123 and the gate dielectric 116 of the assembly 224 (FIG. 14) to form gates including the gate electrodes 118-12 and the remaining gate dielectric 116. The gate electrodes 118-12 may at least partially wrap around portions of the nanowire 110-2, in accordance with any of the embodiments disclosed herein. For example, in FIG. 14, the gate electrodes 118-12 may surround the nanowire 110-2. Portions of the nanowire 110-3 may, however, be exposed in the assembly 226. The spacers 130 may bookend the gate electrodes 118-12, as shown. The recessing of the gate electrode material 123 may take the form of any of the embodiments of the recessing of the gate electrode material 121 discussed above.

[0081] FIG. 16 illustrates an assembly 228 subsequent to providing an insulator 119-2 on the gate electrodes 118-12 of the assembly 226 (FIG. 15). The insulator 119-2 may be provided directly on the gate electrodes 118-12, and in some embodiments, no gate dielectric 116 may be disposed between the insulator 119-2 and the gate electrodes 118-12. In some embodiments, the top surface of the insulator 119-2 may be below the nanowire 110-3, and thus the insulator 119-2 may not contact the nanowire 110-3. In other embodiments, the insulator 119-2 may contact the nanowire 110-3. The height of the insulator 119-2 may depend on the desired geometry for the gate electrode 118-13, as discussed below. In some embodiments, the insulator 119-2 may be blanked deposited and recessed back, while in other embodiments, the insulator 119-2 may be initially deposited to its desired final height.

[0082] FIG. 17 illustrates an assembly 230 subsequent to providing a gate dielectric 116 around the exposed nanowire 110-3 (and along the exposed faces of the spacers 130) of the assembly 228 (FIG. 16), providing gate electrodes 118-13 on the additional gate dielectric 116 around the exposed portions of the nanowire 110-3, and removing the portions of insulator 101 between the gate electrodes 118-13 to expose regions 269 of the fin 244. The gate dielectric 116 may take any of the forms discussed above (e.g., with reference to FIG. 11), and the gate electrodes 118-13 may be formed in accordance with any of the techniques discussed above with reference to the gate electrodes 118-11 and 118-12. In some embodiments, the gate electrodes 118-13 may be planarized at the top surface. Any suitable patterning technique may be used to expose the regions 269, such as a hardmask-based lithography technique. In some embodiments, the spacers 130 may define the lateral extent of the portions of insulator 101 that are removed to expose the regions 269.

[0083] FIG. 18 illustrates an assembly 232 subsequent to removing the remaining portions of the layers of sacrificial material 170 between the nanowires 110 in the fin 244 under the exposed regions 269 of the assembly 230 (FIG. 17) to expose portions of the nanowires 110. The sacrificial material 170 may be removed using any of the techniques discussed above with reference to FIG. 9. In some embodiments, as illustrated in FIG. 18, all of the sacrificial material 170 may be removed. In some embodiments, the spacers 130 may define the lateral extent of the sacrificial material 170 that is removed.

[0084] FIG. 19 illustrates an assembly 234 subsequent to providing a bottom gate isolation material 114 on the exposed top surface 104 of the substrate 102 under the bottom-most nanowire 115 of the assembly 232 (FIG. 18). The new bottom gate isolation material 114 in the assembly 234 may be formed in accordance with any of the embodiments discussed above with reference to FIG. 10.

[0085] FIG. 20 illustrates an assembly 236 subsequent to forming gates including the gate electrodes 118-21, 118-22, and 118-23 in the assembly 234 (FIG. 19). The gate electrodes 118-21 wrap at least partially around the nanowire 110-1, the gate electrodes 118-22 wrap at least partially around the nanowire 110-2, and the gate electrodes 118-23 wrap at least partially around the nanowire 110-3. The gate electrodes 118-2 may be formed using the techniques discussed above with reference to the formation of the gate electrodes 118-1 in FIGS. 11-17 (e.g., providing dielectric material, providing a gate electrode material, recessing the dielectric material and the gate electrode material to form a gate electrode, providing an insulator, and repeating the cycle for additional gate electrodes). The assembly 236 may take the form of the device 100 discussed above with reference to FIG. 1.

[0086] In some embodiments, a device 100 may not include the gate electrodes 118-2, and the gate electrodes 118-1 may be separated by intervening insulators. For example, FIGS. 21A-21D are various views of another embodiment of a quantum nanowire device 100 having embedded epi carrier reservoirs 106 and 107, and FIGS. 21E-21F are various views of a variant of the quantum nanowire device 100 of FIGS. 21A-21D without embedded epi carrier reservoirs 106 and 107. FIGS. 21A-21F are thus analogous to FIGS. 1A-1F, respectively, and any of the embodiments of the elements common to both sets of figures may take any of the forms discussed herein. In contrast to the device 100 of FIG. 1, the device 100 of FIG. 21 may include insulator 101 and remaining sacrificial material 170 between adjacent gate electrodes 118-1 (in lieu of intervening gate electrodes 118-2). In some embodiments of the device 100 of FIG. 21, the nanowires 110 (and thus the semiconductor material 160) may be germanium, the sacrificial material 170 may be silicon germanium (e.g., with 30% silicon and 70% germanium content), the buffer layers 109 may include silicon germanium (and may have a thickness between 500 nanometers and 1.5 microns, for example), and the substrate 102 may include an underlying distinct crystalline silicon. The device 100 of FIG. 21 may be manufactured in accordance with the processes discussed above with reference to FIGS. 2-11; the assembly 218 of FIG. 11 may have the form of the device 100 of FIG. 21.

[0087] FIG. 22 is a flow diagram of an example method 1000 of manufacturing a quantum nanowire device, in accordance with various embodiments. Although the various operations discussed with reference to the method 1000 are shown in a particular order and once each, the operations may be performed in any suitable order (e.g., in any combination of parallel or series performance), and may be repeated or omitted as suitable. Additionally, although various operations of the method 1000 may be illustrated with reference to particular embodiments of the quantum nanowire devices 100 disclosed herein, these are simply examples, and the method 1000 may be used to form any suitable device.

[0088] At 1002, a first gate may be formed. The first gate may at least partially wrap around a first nanowire. For example, a gate including the gate electrode 118-11 may be formed, and may at least partially wrap around a nanowire 110-1 (e.g., as discussed above with reference to FIGS. 2-12).

[0089] At 1004, a second gate may be formed. The second gate may at least partially wrap around a second nanowire above the first nanowire. For example, a gate including the gate electrodes 118-12 may be formed, and may at least partially wrap around a nanowire 110-2 (e.g., as discussed above with reference to FIGS. 13-15).

[0090] A number of techniques are disclosed herein for operating a quantum nanowire device 100. FIG. 23 is a flow diagram of an illustrative method 1010 of operating a quantum nanowire device, in accordance with various embodiments. Although the operations discussed below with reference to

the method 1010 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1010 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1010 may be used to operate any suitable quantum nanowire device (including any suitable ones of the embodiments disclosed herein).

[0091] At 1012, electrical signals may be provided to a first gate. The first gate may at least partially wrap around a first nanowire. For example, electrical signals (e.g., voltages) may be provided to the gates including the gate electrodes 118-x1 (where x takes the values 1 and 2) at least partially wrapped around the nanowire 110-1.

[0092] At 1014, electrical signals may be provided to a second gate. The second gate may at least partially wrap around a second nanowire above the first nanowire. The first and second nanowires may be adjacent nanowires in a vertical array of nanowires. For example, electrical signals (e.g., voltages) may be provided to gates including the gate electrodes 118-x2 (where x takes the values 1 and 2) at least partially wrapped around the nanowire 110-2. The electrical signals provided to the first gate (at 1012) and to the second gate (at 1014) may contribute to causing at least one quantum dot to form in one or both of the first and second nanowires. For example, in some embodiments, quantum dots may form in a nanowire 110 under a gate electrode 118 (e.g., when the gate electrode 118 acts as a "plunger" gates). In some embodiments, a voltage applied to a gate electrode 118 may cause a potential barrier to form in a nanowire 110 under the gate electrode 118 (e.g., when the gate electrode 118 acts as a "barrier" gate).

[0093] In some embodiments, any of the quantum nanowire devices 100 disclosed herein may be included in a die and coupled to a package substrate to form a quantum nanowire device package. For example, FIG. 24 is a side cross-sectional view of a die 302 including the quantum nanowire device 100 of FIG. 1A and conductive pathway layers 303 disposed thereon, while FIG. 25 is a side cross-sectional view of a quantum nanowire device package 300 in which the die 302 is coupled to a package substrate 304. Details of the quantum nanowire device 100 are omitted from FIG. 25 for economy of illustration. As noted above, the particular quantum nanowire device 100 illustrated in FIG. 25 may take the form of the quantum nanowire device 100 illustrated in FIG. 1A, but any of the quantum nanowire devices 100 disclosed herein may be included in a die (e.g., the die 302) and coupled to a package substrate (e.g., the package substrate 304).

[0094] The die 302 may include a first face 320 and an opposing second face 322. The substrate 102 may be proximate to the second face 322, and conductive pathways 315 from various components of the quantum nanowire device 100 may extend to conductive contacts 365 disposed

at the first face 320. The conductive pathways 315 may include conductive vias, conductive lines, and/or any combination of conductive vias and lines. For example, FIG. 24 illustrates an embodiment in which a conductive pathway 315-1 (extending between a gate electrode 118-1 and associated conductive contact 365) includes a conductive via 374, a conductive line 393, a conductive via 398, and a conductive line 396. In the embodiment of FIG. 24, another conductive pathway 315-2 (extending between a gate electrode 118-2 and associated conductive contact 365) includes a conductive via 374, a conductive line 393, a conductive via 398, and a conductive line 396. More or fewer structures may be included in the conductive pathways 315, and analogous conductive pathways 315 may be provided between ones of the conductive contacts 365 and other components of the quantum nanowire device 100. In some embodiments, conductive lines of the die 302 (and the package substrate 304, discussed below) may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from various elements in the die 302.

[0095] The conductive vias and/or lines that provide the conductive pathways 315 in the die 302 may be formed using any suitable techniques. Examples of such techniques may include subtractive fabrication techniques, additive or semi-additive fabrication techniques, single Damascene fabrication techniques, dual Damascene fabrication techniques, or any other suitable technique. In some embodiments, layers of oxide material 390 and layers of nitride material 391 may insulate various structures in the conductive pathways 315 from proximate structures, and/or may serve as etch stops during fabrication. In some embodiments, an adhesion layer (not shown) may be disposed between conductive material and proximate insulator of the die 302 to improve mechanical adhesion between the conductive material and the insulator.

[0096] The gate electrodes 118, the nanowires 110, and the carrier reservoirs 106 and 107 (as well as the proximate conductive vias/lines) may be referred to as part of the "device layer" of the quantum nanowire device 100. The conductive lines 393 may be referred to as a Metal 1 or "M1" interconnect layer, and may couple the structures in the device layer to other interconnect structures. The conductive vias 398 and the conductive lines 396 may be referred to as a Metal 2 or "M2" interconnect layer, and may be formed directly on the M1 interconnect layer.

[0097] A solder resist material 367 may be disposed around the conductive contacts 365, and in some embodiments may extend onto the conductive contacts 365. The solder resist material 367 may be a polyimide or similar material, or may be any appropriate type of packaging solder resist material. In some embodiments, the solder resist material 367 may be a liquid or dry film material including photoimageable polymers. In some embodiments, the solder resist material 367 may be non-photoimageable (and openings therein may be formed using laser drilling or masked etch

techniques). The conductive contacts 365 may provide the contacts to couple other components (e.g., a package substrate 304, as discussed below, or another component) to the conductive pathways 315 in the quantum nanowire device 100, and may be formed of any suitable conductive material (e.g., a superconducting material). For example, solder bonds may be formed on the one or more conductive contacts 365 to mechanically and/or electrically couple the die 302 with another component (e.g., a circuit board), as discussed below. The conductive contacts 365 illustrated in FIG. 24 take the form of bond pads, but other first level interconnect structures may be used (e.g., posts) to route electrical signals to/from the die 302, as discussed below.

[0098] The combination of the conductive pathways and the proximate insulator (e.g., the insulator 101, the oxide material 390, and the nitride material 391) in the die 302 may provide an interlayer dielectric (ILD) stack of the die 302. As noted above, interconnect structures may be arranged within the quantum nanowire device 100 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures depicted in FIG. 24 or any of the other accompanying figures, and may include more or fewer interconnect structures). During operation of the quantum nanowire device 100, electrical signals (such as power and/or input/output (I/O) signals) may be routed to and/or from the gate electrodes 118 and/or the carrier reservoirs 106 and 107 (and/or other components) of the quantum nanowire device 100 through the interconnects provided by conductive vias and/or lines, and through the conductive pathways of the package substrate 304 (discussed below).

[0099] Any suitable materials may be used to provide the structures in the die 302 and/or the package 300. Example superconducting materials that may be used for the structures in the conductive pathways 313 (discussed below) and 315, and/or conductive contacts of the die 302 and/or the package substrate 304, may include aluminum, niobium, tin, titanium, osmium, zinc, molybdenum, tantalum, vanadium, or composites of such materials (e.g., niobium-titanium, niobium-aluminum, or niobium-tin). In some embodiments, the conductive contacts 365, 379, and/or 399 may include aluminum, and the first level interconnects 306 and/or the second level interconnects 308 may include an indium-based solder.

[0100] In the quantum nanowire device package 300 (FIG. 25), first level interconnects 306 may be disposed between the first face 320 of the die 302 and the second face 326 of a package substrate 304. Having first level interconnects 306 disposed between the first face 320 of the die 302 and the second face 326 of the package substrate 304 (e.g., using solder bumps as part of flip chip packaging techniques) may enable the quantum nanowire device package 300 to achieve a smaller footprint and higher die-to-package-substrate connection density than could be achieved using conventional wirebond techniques (in which conductive contacts between the die 302 and the package substrate

304 are constrained to be located on the periphery of the die 302). For example, a die 302 having a square first face 320 with side length N may be able to form only 4N wirebond interconnects to the package substrate 304, versus N^2 flip chip interconnects (utilizing the entire "full field" surface area of the first face 320). Additionally, in some applications, wirebond interconnects may generate unacceptable amounts of heat that may damage or otherwise interfere with the performance of the quantum nanowire device 100. Using solder bumps as the first level interconnects 306 may enable the quantum nanowire device package 300 to have much lower parasitic inductance relative to using wirebonds to couple the die 302 and the package substrate 304, which may result in an improvement in signal integrity for high speed signals communicated between the die 302 and the package substrate 304.

[0101] The package substrate 304 may include a first face 324 and an opposing second face 326. Conductive contacts 399 may be disposed at the first face 324, and conductive contacts 379 may be disposed at the second face 326. Solder resist material 314 may be disposed around the conductive contacts 379, and solder resist material 312 may be disposed around the conductive contacts 399; the solder resist materials 314 and 312 may take any of the forms discussed above with reference to the solder resist material 367. In some embodiments, the solder resist material 312 and/or the solder resist material 314 may be omitted. Conductive pathways 313 may extend through insulator 310 between the first face 324 and the second face 326 of the package substrate 304, electrically coupling various ones of the conductive contacts 399 to various ones of the conductive contacts 379, in any desired manner. The insulator 310 may be a dielectric material (e.g., an ILD), and may take the form of any of the embodiments of the insulator 101 disclosed herein, for example. The conductive pathways 313 may include one or more conductive vias 395 and/or one or more conductive lines 397, for example.

[0102] In some embodiments, the quantum nanowire device package 300 may be a cored package, one in which the package substrate 304 is built on a carrier material (not shown) that remains in the package substrate 304. In such embodiments, the carrier material may be a dielectric material that is part of the insulator 310; laser vias or other through-holes may be made through the carrier material to allow conductive pathways 313 to extend between the first face 324 and the second face 326.

[0103] In some embodiments, the package substrate 304 may be or may otherwise include a silicon interposer, and the conductive pathways 313 may be through-silicon vias. Silicon may have a desirably low coefficient of thermal expansion compared with other dielectric materials that may be used for the insulator 310, and thus may limit the degree to which the package substrate 304 expands and contracts during temperature changes relative to such other materials (e.g., polymers

having higher coefficients of thermal expansion). A silicon interposer may also help the package substrate 304 achieve a desirably small line width and maintain high connection density to the die 302.

[0104] Limiting differential expansion and contraction may help preserve the mechanical and electrical integrity of the quantum nanowire device package 300 as the quantum nanowire device package 300 is fabricated (and exposed to higher temperatures) and used in a cooled environment (and exposed to lower temperatures). In some embodiments, thermal expansion and contraction in the package substrate 304 may be managed by maintaining an approximately uniform density of the conductive material in the package substrate 304 (so that different portions of the package substrate 304 expand and contract uniformly), using reinforced dielectric materials as the insulator 310 (e.g., dielectric materials with silicon dioxide fillers), or utilizing stiffer materials as the insulator 310 (e.g., a prepreg material including glass cloth fibers).

[0105] The conductive contacts 365 of the die 302 may be electrically coupled to the conductive contacts 379 of the package substrate 304 via the first level interconnects 306. In some embodiments, the first level interconnects 306 may include solder bumps or balls (as illustrated in FIG. 25); for example, the first level interconnects 306 may be flip chip (or controlled collapse chip connection, "C4") bumps disposed initially on the die 302 or on the package substrate 304. Second level interconnects 308 (e.g., solder balls or other types of interconnects) may couple the conductive contacts 399 on the first face 324 of the package substrate 304 to another component, such as a circuit board (not shown). Examples of arrangements of electronics packages that may include an embodiment of the quantum nanowire device package 300 are discussed below with reference to FIG. 27. The die 302 may be brought in contact with the package substrate 304 using a pick-and-place apparatus, for example, and a reflow or thermal compression bonding operation may be used to couple the die 302 to the package substrate 304 via the first level interconnects 306.

[0106] The conductive contacts 365, 379, and/or 399 may include multiple layers of material that may be selected to serve different purposes. In some embodiments, the conductive contacts 365, 379, and/or 399 may be formed of aluminum, and may include a layer of gold (e.g., with a thickness of less than 1 micron) between the aluminum and the adjacent interconnect to limit the oxidation of the surface of the contacts and improve the adhesion with adjacent solder. In some embodiments, the conductive contacts 365, 379, and/or 399 may be formed of aluminum, and may include a layer of a barrier metal such as nickel, as well as a layer of gold, wherein the layer of barrier metal is disposed between the aluminum and the layer of gold, and the layer of gold is disposed between the barrier metal and the adjacent interconnect. In such embodiments, the gold may protect the barrier

metal surface from oxidation before assembly, and the barrier metal may limit the diffusion of solder from the adjacent interconnects into the aluminum.

[0107] In some embodiments, the structures and materials in the quantum nanowire device 100 may be damaged if the quantum nanowire device 100 is exposed to the high temperatures that are common in conventional integrated circuit processing (e.g., greater than 100 degrees Celsius, or greater than 200 degrees Celsius). In particular, in embodiments in which the first level interconnects 306 include solder, the solder may be a low-temperature solder (e.g., a solder having a melting point below 100 degrees Celsius) so that it can be melted to couple the conductive contacts 365 and the conductive contacts 379 without having to expose the die 302 to higher temperatures and risk damaging the quantum nanowire device 100. Examples of solders that may be suitable include indium-based solders (e.g., solders including indium alloys). When low-temperature solders are used, however, these solders may not be fully solid during handling of the quantum nanowire device package 300 (e.g., at room temperature or temperatures between room temperature and 100 degrees Celsius), and thus the solder of the first level interconnects 306 alone may not reliably mechanically couple the die 302 and the package substrate 304 (and thus may not reliably electrically couple the die 302 and the package substrate 304). In some such embodiments, the quantum nanowire device package 300 may further include a mechanical stabilizer to maintain mechanical coupling between the die 302 and the package substrate 304, even when solder of the first level interconnects 306 is not solid. Examples of mechanical stabilizers may include an underfill material disposed between the die 302 and the package substrate 304, a corner glue disposed between the die 302 and the package substrate 304, an overmold material disposed around the die 302 on the package substrate 304, and/or a mechanical frame to secure the die 302 and the package substrate 304.

[0108] Any of the devices 100 disclosed herein may include one or more magnet lines. As used herein, a "magnet line" refers to a magnetic-field-generating structure to influence (e.g., change, reset, scramble, or set) the spin states of quantum dots. One example of a magnet line, as discussed herein, is a conductive pathway that is proximate to an area of quantum dot formation and selectively conductive of a current pulse that generates a magnetic field to influence a spin state of a quantum dot in the area.

[0109] For example, FIG. 24 depicts a magnet line 377 included in the device 100. The magnet line 377 of FIG. 24 is illustrated with dashed lines to indicate that the magnet line 377 may not be in the same plane as the cross-section of the drawing. A device 100 may include one or more magnet lines 377. A magnet line 377 may be formed of a conductive material, and may be used to conduct current pulses that generate magnetic fields to influence the spin states of one or more of the

quantum dots that may form in the device 100. In some embodiments, a magnet line 377 may conduct a pulse to reset (or "scramble") nuclear and/or quantum dot spins. In some embodiments, a magnet line 377 may conduct a pulse to initialize an electron in a quantum dot in a particular spin state. In some embodiments, a magnet line 377 may conduct current to provide a continuous, oscillating magnet field to which the spin of a qubit may couple. A magnet line 377 may provide any suitable combination of these embodiments, or any other appropriate functionality.

[0110] In some embodiments, a magnet line 377 may be formed of copper. In some embodiments, a magnet line 377 may be formed of a superconductor, such as aluminum. In some embodiments, a magnet line 377 may be spaced apart from proximate gates 118 by a distance 375 that may be selected to achieve a desired strength of magnetic field interaction. In some embodiments, the distance 375 may be between 25 nanometers and 1 micron (e.g., between 50 nanometers and 200 nanometers).

[0111] In some embodiments, a magnet line 377 may be formed of a magnetic material. For example, a magnetic material (such as cobalt) may be deposited in a trench in the insulator 101 to provide a permanent magnetic field in the device 100.

[0112] A magnet line 377 may have any suitable dimensions. For example, the magnet line 377 may have a thickness (in the z-direction) between 25 and 100 nanometers. A magnet line 377 may have a width (perpendicular to the length 120) between 25 and 100 nanometers. In some embodiments, the width and thickness of a magnet line 377 may be equal to the width and thickness, respectively, of other conductive lines in the device 100 used to provide electrical interconnects (e.g., the conductive lines 393 and 396), as known in the art, and may be formed using any processes known for forming conductive lines (e.g., plating in a trench, followed by planarization, or a semi-additive process). The magnet line 377 illustrated in FIG. 24 is substantially linear, but this need not be the case; magnet lines 377 may take any suitable shape. Conductive vias (not shown) may contact the magnet line 377.

[0113] In some embodiments, a device 100 may include one magnet line 377, or no magnet lines 377; in other embodiments, a device 100 may include two, three, four, or more magnet lines 377. Magnet lines 377included in a device 100 may be oriented in any desired manner relative to the gate electrodes 118 or other structural features of the device 100; for example, one or more magnet lines 377may be oriented into and out of the plane of the drawing of FIG. 24, in addition to or instead of one or more magnet lines 377oriented left and right in the plane of the drawing of FIG. 24 (as illustrated).

[0114] FIGS. 26A-B are top views of a wafer 450 and dies 452 that may be formed from the wafer 450; the dies 452 may include any of the quantum nanowire devices 100 disclosed herein, and/or

may take the form of any of the dies 302 disclosed herein. The wafer 450 may include semiconductor material and may include one or more dies 452 having conventional and quantum nanowire device elements formed on a surface of the wafer 450. Each of the dies 452 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum nanowire device. After the fabrication of the semiconductor product is complete, the wafer 450 may undergo a singulation process in which each of the dies 452 is separated from one another to provide discrete "chips" of the semiconductor product. A die 452 may include one or more quantum nanowire devices 100 and/or supporting circuitry to route electrical signals to the quantum nanowire devices 100 (e.g., interconnects including conductive vias and lines), as well as any other IC components. In some embodiments, the wafer 450 or the die 452 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 452. For example, a memory array formed by multiple memory devices may be formed on a same die 452 as a processing device (e.g., the processing device 2002 of FIG. 28) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0115] FIG. 27 is a cross-sectional side view of a device assembly 400 that may include any of the embodiments of the quantum nanowire device packages 300 disclosed herein. The device assembly 400 includes a number of components disposed on a circuit board 402. The device assembly 400 may include components disposed on a first face 440 of the circuit board 402 and an opposing second face 442 of the circuit board 402; generally, components may be disposed on one or both faces 440 and 442.

[0116] In some embodiments, the circuit board 402 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 402. In other embodiments, the circuit board 402 may be a package substrate or flexible board.

[0117] The device assembly 400 illustrated in FIG. 27 includes a package-on-interposer structure 436 coupled to the first face 440 of the circuit board 402 by coupling components 416. The coupling components 416 may electrically and mechanically couple the package-on-interposer structure 436 to the circuit board 402, and may include solder balls (as shown in FIG. 25), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0118] The package-on-interposer structure 436 may include a package 420 coupled to an interposer 404 by coupling components 418. The coupling components 418 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 416. For example, the coupling components 418 may be the second level interconnects 308. Although a single package 420 is shown in FIG. 27, multiple packages may be coupled to the interposer 404; indeed, additional interposers may be coupled to the interposer 404. The interposer 404 may provide an intervening substrate used to bridge the circuit board 402 and the package 420. The package 420 may be a quantum nanowire device package 300 or may be a conventional IC package, for example. In some embodiments, the package 420 may take the form of any of the embodiments of the quantum nanowire device package 300 disclosed herein, and may include a quantum nanowire device die 302 coupled to a package substrate 304 (e.g., by flip chip connections). Generally, the interposer 404 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 404 may couple the package 420 (e.g., a die) to a ball grid array (BGA) of the coupling components 416 for coupling to the circuit board 402. In the embodiment illustrated in FIG. 27, the package 420 and the circuit board 402 are attached to opposing sides of the interposer 404; in other embodiments, the package 420 and the circuit board 402 may be attached to a same side of the interposer 404. In some embodiments, three or more components may be interconnected by way of the interposer 404.

[0119] The interposer 404 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 404 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 404 may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 406. The interposer 404 may further include embedded devices 414, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 404. The package-on-interposer structure 436 may take the form of any of the package-on-interposer structures known in the art.

[0120] The device assembly 400 may include a package 424 coupled to the first face 440 of the circuit board 402 by coupling components 422. The coupling components 422 may take the form of any of the embodiments discussed above with reference to the coupling components 416, and the

package 424 may take the form of any of the embodiments discussed above with reference to the package 420. The package 424 may be a quantum nanowire device package 300 or may be a conventional IC package, for example. In some embodiments, the package 424 may take the form of any of the embodiments of the quantum nanowire device package 300 disclosed herein, and may include a quantum nanowire device die 302 coupled to a package substrate 304 (e.g., by flip chip connections).

[0121] The device assembly 400 illustrated in FIG. 27 includes a package-on-package structure 434 coupled to the second face 442 of the circuit board 402 by coupling components 428. The package-on-package structure 434 may include a package 426 and a package 432 coupled together by coupling components 430 such that the package 426 is disposed between the circuit board 402 and the package 432. The coupling components 428 and 430 may take the form of any of the embodiments of the coupling components 416 discussed above, and the packages 426 and 432 may take the form of any of the embodiments of the package 420 discussed above. Each of the packages 426 and 432 may be a quantum nanowire device package 300 or may be a conventional IC package, for example. In some embodiments, one or both of the packages 426 and 432 may take the form of any of the embodiments of the quantum nanowire device package 300 disclosed herein, and may include a die 302 coupled to a package substrate 304 (e.g., by flip chip connections).

[0122] FIG. 28 is a block diagram of an example quantum computing device 2000 that may include any of the quantum nanowire devices 100 disclosed herein. A number of components are illustrated in FIG. 28 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more PCBs (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 28, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0123] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to

any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum nanowire devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum nanowire devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0124] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0125] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0126] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0127] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0128] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in

accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0129] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0130] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0131] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0132] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0133] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any

device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0134] The quantum computing device 2000 may include a GPS device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0135] The quantum computing device 2000 may include another output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0136] The quantum computing device 2000 may include another input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0137] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0138] The following paragraphs provide various examples of the embodiments disclosed herein.

[0139] Example 1 is a quantum computing device, including: a first nanowire and a second nanowire arranged in a vertical array; a first gate at least partially wrapped around the first nanowire but not around the second nanowire; and a second gate at least partially wrapped around the second nanowire but not around the first nanowire, wherein the second gate is at least partially above the first gate.

[0140] Example 2 may include the subject matter of Example 1, and may further include an insulator between the first gate and the second gate.

[0141] Example 3 may include the subject matter of Example 2, and may further specify that the first gate and the second gate are in contact with the insulator.

[0142] Example 4 may include the subject matter of any of Examples 2-3, and may further specify that the second gate includes a gate dielectric, and the gate dielectric is in contact with the insulator.

[0143] Example 5 may include the subject matter of any of Examples 1-4, and may further specify that the first gate includes a gate electrode, and the gate electrode is in contact with the insulator.

[0144] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the first nanowire and the second nanowire each extend between carrier reservoirs.

[0145] Example 7 may include the subject matter of Example 6, and may further specify that the first gate and the second gate are at least partially between the carrier reservoirs.

[0146] Example 8 may include the subject matter of any of Examples 6-7, and may further specify that the carrier reservoirs include an alternating material stack.

[0147] Example 9 may include the subject matter of any of Examples 1-8, and may further specify that the first nanowire and the second nanowire include germanium or silicon.

[0148] Example 10 may include the subject matter of Example 9, and may further specify that silicon germanium is present between the first nanowire and the second nanowire.

[0149] Example 11 may include the subject matter of any of Examples 1-10, and may further specify that the vertical array is a first vertical array of nanowires, and the quantum computing device further includes a second vertical array of nanowires spaced apart from the first vertical array of nanowires.

[0150] Example 12 may include the subject matter of Example 11, and may further specify that the first gate at least partially wraps around one or more nanowires in the second vertical array of nanowires.

[0151] Example 13 may include the subject matter of Example 12, and may further specify that the second gate at least partially wraps around one or more nanowires in the second vertical array of nanowires.

[0152] Example 14 may include the subject matter of Example 11, and may further specify that the first gate does not at least partially wrap around any nanowires of the second vertical array of nanowires, and the quantum computing device further includes a third gate at least partially wrapped around one or more nanowires of the second vertical array of nanowires.

[0153] Example 15 may include the subject matter of any of Examples 1-14, and may further specify that the first gate surrounds the first nanowire, or the second gate surrounds the second nanowire.

[0154] Example 16 may include the subject matter of any of Examples 1-15, and may further specify that the first gate does not surround the first nanowire, or the second gate does not surround the second nanowire.

[0155] Example 17 is a method of manufacturing a quantum computing device, including: forming a plurality of nanowires in a vertical array, wherein the plurality of nanowires includes a second nanowire above a first nanowire; forming a first gate at least partially wrapped around the first

nanowire; and forming a second gate at least partially wrapped around the second nanowire, wherein the first gate and the second gate are separate gates.

[0156] Example 18 may include the subject matter of Example 17, and may further specify that forming the plurality of nanowires in the vertical array includes: providing a fin having alternating layers of nanowire material and sacrificial material; forming a sacrificial structure over the fin; providing an insulator around the sacrificial structure; removing the sacrificial structure to expose a portion of the fin; and removing the sacrificial material from the exposed portions of the fin to form the plurality of nanowires in the vertical array.

[0157] Example 19 may include the subject matter of any of Examples 17-18, and may further specify that forming the first gate includes: providing a conformal gate dielectric over the first nanowire and the second nanowire; and providing a first gate electrode over the gate dielectric, wherein the first gate electrode at least partially wraps around the first nanowire.

[0158] Example 20 may include the subject matter of Example 19, and may further specify that providing the first gate electrode includes: providing a gate electrode material surrounding the first nanowire and the second nanowire; and recessing the gate electrode material to remove the gate electrode material around the second nanowire.

[0159] Example 21 may include the subject matter of any of Examples 17-20, and may further include, after forming the first gate, providing an insulator on the first gate; wherein the second gate is formed on the insulator.

[0160] Example 22 may include the subject matter of Example 21, and may further specify that the insulator is at least partially between the first nanowire and the second nanowire.

[0161] Example 23 may include the subject matter of any of Examples 21-22, and may further specify that the insulator contacts at least one of the first nanowire and the second nanowire.

[0162] Example 24 may include the subject matter of any of Examples 17-23, and may further include: forming a third gate at least partially wrapped around the first nanowire; and forming a fourth gate at least partially wrapped around the second nanowire, wherein the first gate, the second gate, the third gate, and the fourth gate are separate gates.

[0163] Example 25 may include the subject matter of any of Examples 17-24, and may further specify that the first nanowire and the second nanowire are strained.

[0164] Example 26 is a method of operating a quantum computing device, including: providing electrical signals to a first gate as part of causing a first quantum dot to form in a first nanowire, wherein the first gate at least partially wraps around the first nanowire; providing electrical signals to a second gate as part of causing a second quantum dot to form in a second nanowire, wherein the second gate at least partially wraps around the second nanowires, the second nanowire is above the

first nanowire, and the second gate is above the first gate; and allowing the first quantum dot and the second quantum dot to interact as part of a quantum computation.

[0165] Example 27 may include the subject matter of Example 26, and may further include providing electrical signals to a third gate as part of (1) causing a third quantum dot to form in a third nanowire, or (2) providing a potential barrier between the first quantum dot and the second quantum dot, wherein the third gate at least partially wraps around the third nanowire, and the third nanowire is between the first nanowire and the second nanowire.

[0166] Example 28 may include the subject matter of Example 27, and may further include adjusting the electrical signals provided to the third gate to control quantum interaction between the first quantum dot and the second quantum dot.

[0167] Example 29 may include the subject matter of any of Examples 26-28, and may further include using a magnet line proximate to the first gate to adjust a spin of the first quantum dot.

[0168] Example 30 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes a plurality of nanowires and a set of gates to control formation of quantum dots in the plurality of nanowires, the plurality of nanowires are arranged in a vertical array, and different individual gates of the set of gates are associated with different individual nanowires of the plurality of nanowires; a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the set of gates; and a memory device to store data generated by the quantum processing device during operation.

[0169] Example 31 may include the subject matter of Example 30, and may further include a cooling apparatus to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

[0170] Example 32 may include the subject matter of any of Examples 30-31, and may further specify that individual gates of the set of gates at least partially wrap around different individual nanowires of the plurality of nanowires.

[0171] Example 33 may include the subject matter of any of Examples 30-32, and may further specify that individual nanowires of the plurality of nanowires are at least partially wrapped around by multiple gates.

Claims:

1. A quantum computing device, comprising:

a first nanowire and a second nanowire arranged in a vertical array;

a first gate at least partially wrapped around the first nanowire but not around the second nanowire; and

a second gate at least partially wrapped around the second nanowire but not around the first nanowire, wherein the second gate is at least partially above the first gate.

2. The quantum computing device of claim 1, further comprising:

an insulator between the first gate and the second gate.

3. The quantum computing device of claim 2, wherein the first gate and the second gate are in contact with the insulator.

4. The quantum computing device of claim 2, wherein the second gate includes a gate dielectric, and the gate dielectric is in contact with the insulator.

5. The quantum computing device of claim 1, wherein the first gate includes a gate electrode, and the gate electrode is in contact with the insulator.

6. The quantum computing device of claim 1, wherein silicon germanium is present between the first nanowire and the second nanowire.

7. The quantum computing device of any of claims 1-6, wherein the vertical array is a first vertical array of nanowires, and the quantum computing device further includes a second vertical array of nanowires spaced apart from the first vertical array of nanowires.

8. The quantum computing device of claim 7, wherein the first gate at least partially wraps around one or more nanowires in the second vertical array of nanowires.

9. The quantum computing device of claim 8, wherein the second gate at least partially wraps around one or more nanowires in the second vertical array of nanowires.

10. The quantum computing device of claim 7, wherein the first gate does not at least partially wrap around any nanowires of the second vertical array of nanowires, and the quantum computing device further includes:

a third gate at least partially wrapped around one or more nanowires of the second vertical array of nanowires.

11. The quantum computing device of any of claims 1-6, wherein the first gate surrounds the first nanowire, or the second gate surrounds the second nanowire.

12. A method of manufacturing a quantum computing device, comprising:

forming a plurality of nanowires in a vertical array, wherein the plurality of nanowires includes a second nanowire above a first nanowire;

forming a first gate at least partially wrapped around the first nanowire; and
forming a second gate at least partially wrapped around the second nanowire, wherein the first gate and the second gate are separate gates.

13. The method of claim 12, wherein forming the first gate includes:
providing a conformal gate dielectric over the first nanowire and the second nanowire; and
providing a first gate electrode over the gate dielectric, wherein the first gate electrode at least partially wraps around the first nanowire.

14. The method of claim 13, wherein providing the first gate electrode includes:
providing a gate electrode material surrounding the first nanowire and the second nanowire; and
recessing the gate electrode material to remove the gate electrode material around the second nanowire.

15. The method of any of claims 12-14, further comprising:
after forming the first gate, providing an insulator on the first gate;
wherein the second gate is formed on the insulator.

16. The method of claim 15, wherein the insulator contacts at least one of the first nanowire and the second nanowire.

17. The method of any of claims 12-14, further comprising:
forming a third gate at least partially wrapped around the first nanowire; and
forming a fourth gate at least partially wrapped around the second nanowire, wherein the first gate, the second gate, the third gate, and the fourth gate are separate gates.

18. The method of any of claims 12-14, wherein the first nanowire and the second nanowire are strained.

19. A method of operating a quantum computing device, comprising:
providing electrical signals to a first gate as part of causing a first quantum dot to form in a first nanowire, wherein the first gate at least partially wraps around the first nanowire;
providing electrical signals to a second gate as part of causing a second quantum dot to form in a second nanowire, wherein the second gate at least partially wraps around the second nanowires, the second nanowire is above the first nanowire, and the second gate is above the first gate; and
allowing the first quantum dot and the second quantum dot to interact as part of a quantum computation.

20. The method of claim 19, further comprising:
providing electrical signals to a third gate as part of (1) causing a third quantum dot to form in a third nanowire, or (2) providing a potential barrier between the first quantum dot and the second

quantum dot, wherein the third gate at least partially wraps around the third nanowire, and the third nanowire is between the first nanowire and the second nanowire.

21. The method of claim 20, further comprising:

adjusting the electrical signals provided to the third gate to control quantum interaction between the first quantum dot and the second quantum dot.

22. The method of any of claims 19-21, further comprising:

using a magnet line proximate to the first gate to adjust a spin of the first quantum dot.

23. A quantum computing device, comprising:

a quantum processing device, wherein the quantum processing device includes a plurality of nanowires and a set of gates to control formation of quantum dots in the plurality of nanowires, the plurality of nanowires are arranged in a vertical array, and different individual gates of the set of gates are associated with different individual nanowires of the plurality of nanowires;

a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the set of gates; and

a memory device to store data generated by the quantum processing device during operation.

24. The quantum computing device of claim 23, wherein individual gates of the set of gates at least partially wrap around different individual nanowires of the plurality of nanowires.

25. The quantum computing device of claim 23, wherein individual nanowires of the plurality of nanowires are at least partially wrapped around by multiple gates.

FIG. 1A

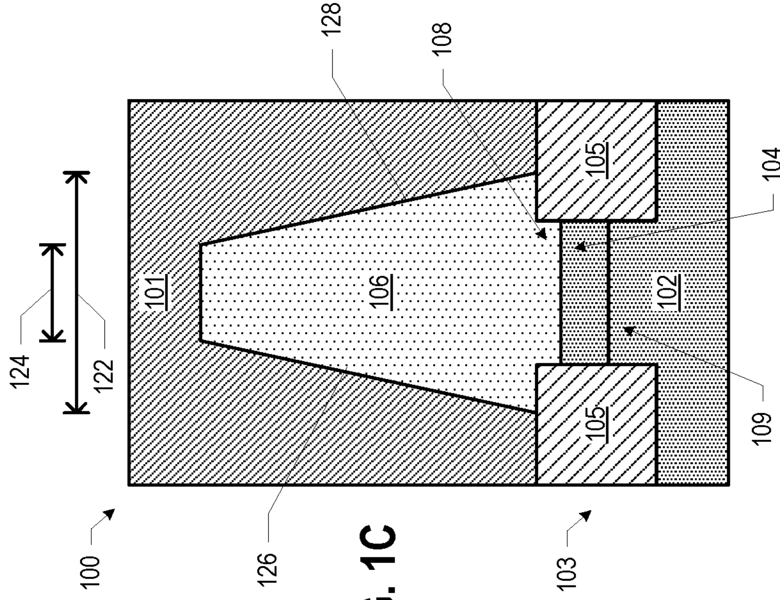


FIG. 1C

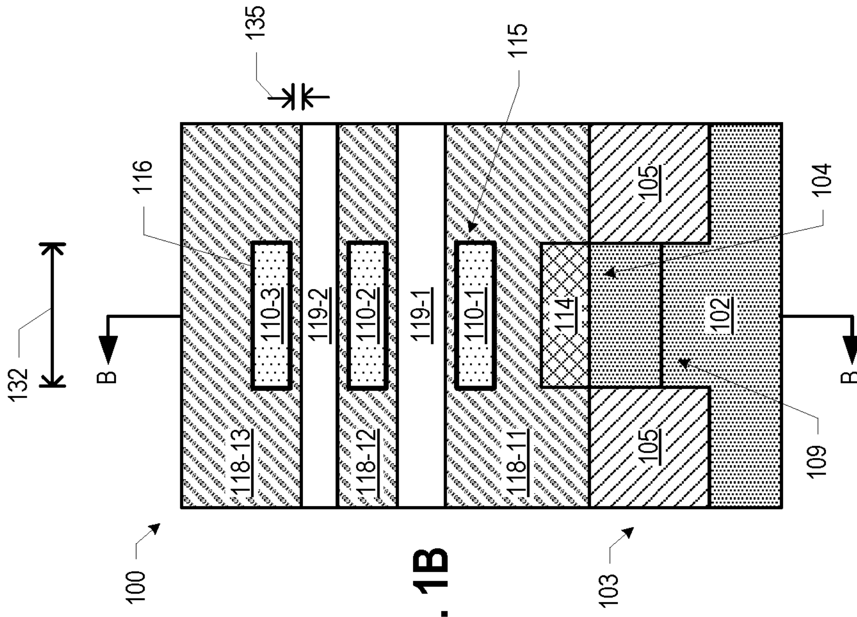


FIG. 1B

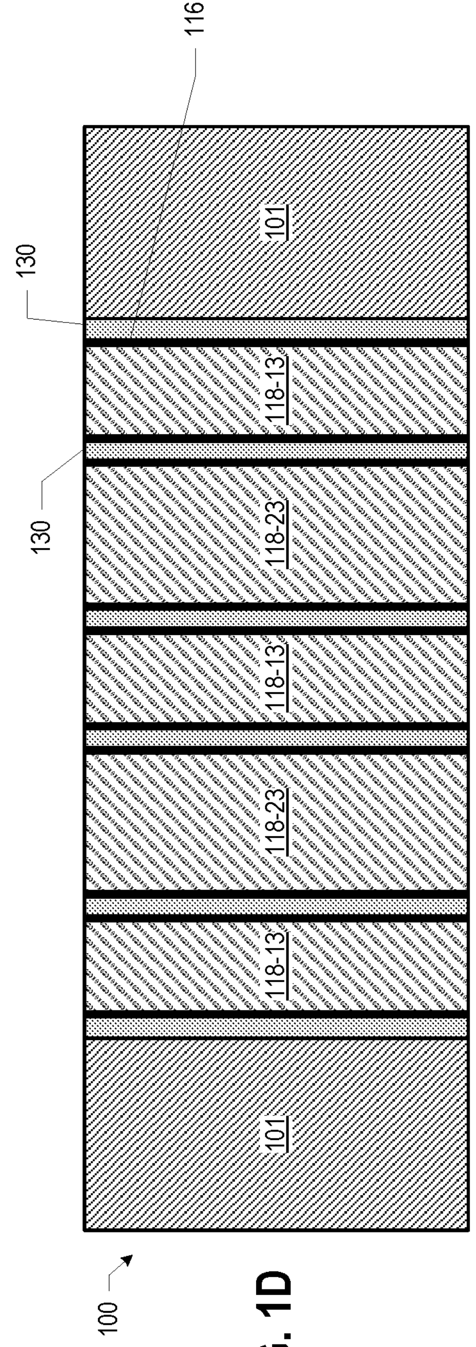
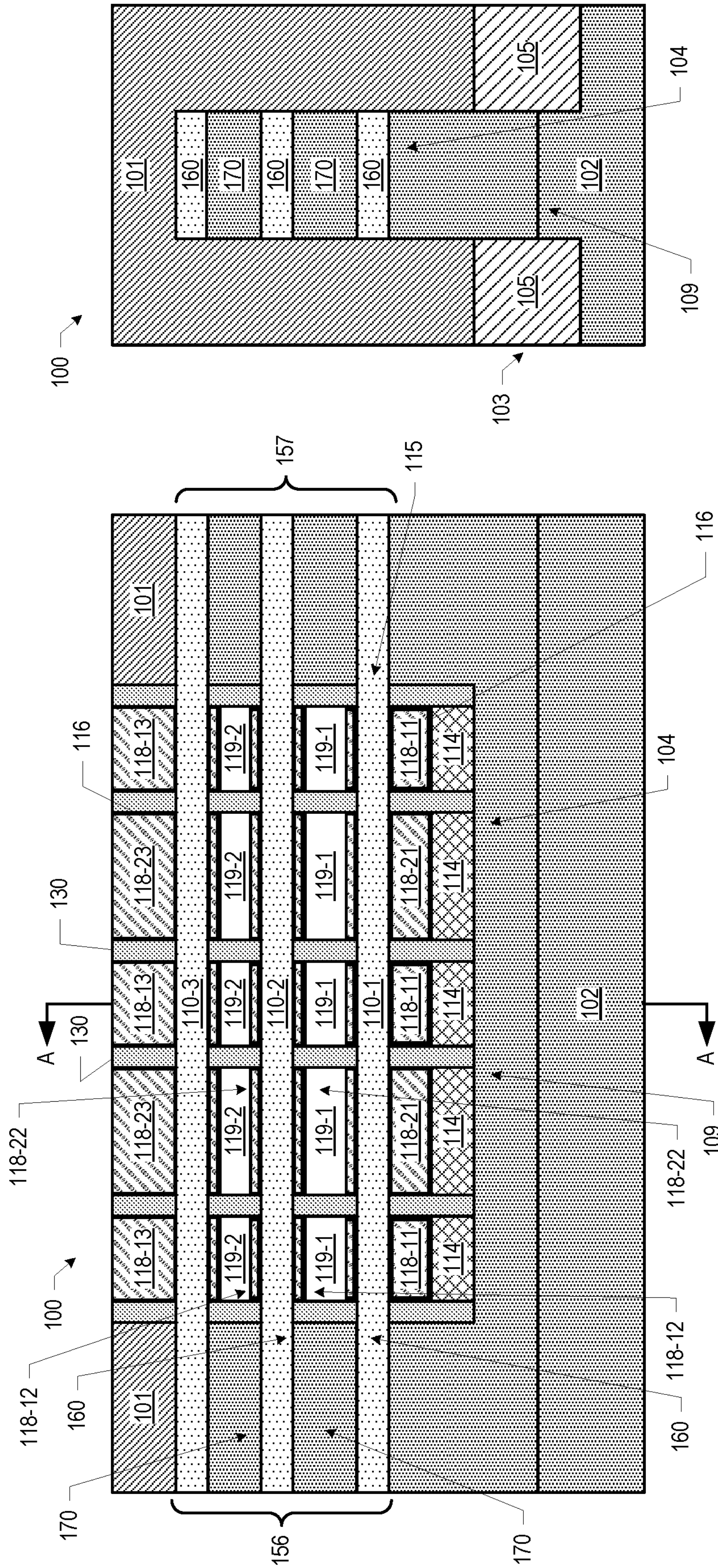


FIG. 1D


100
101
160
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160
170
160
105
104
102
109
103
FIG. 1F
157
115
116
118-13
118-23
118-21
118-11
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114
110-3
110-2
110-1
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A
118-22
118-12
109
156
FIG. 1E

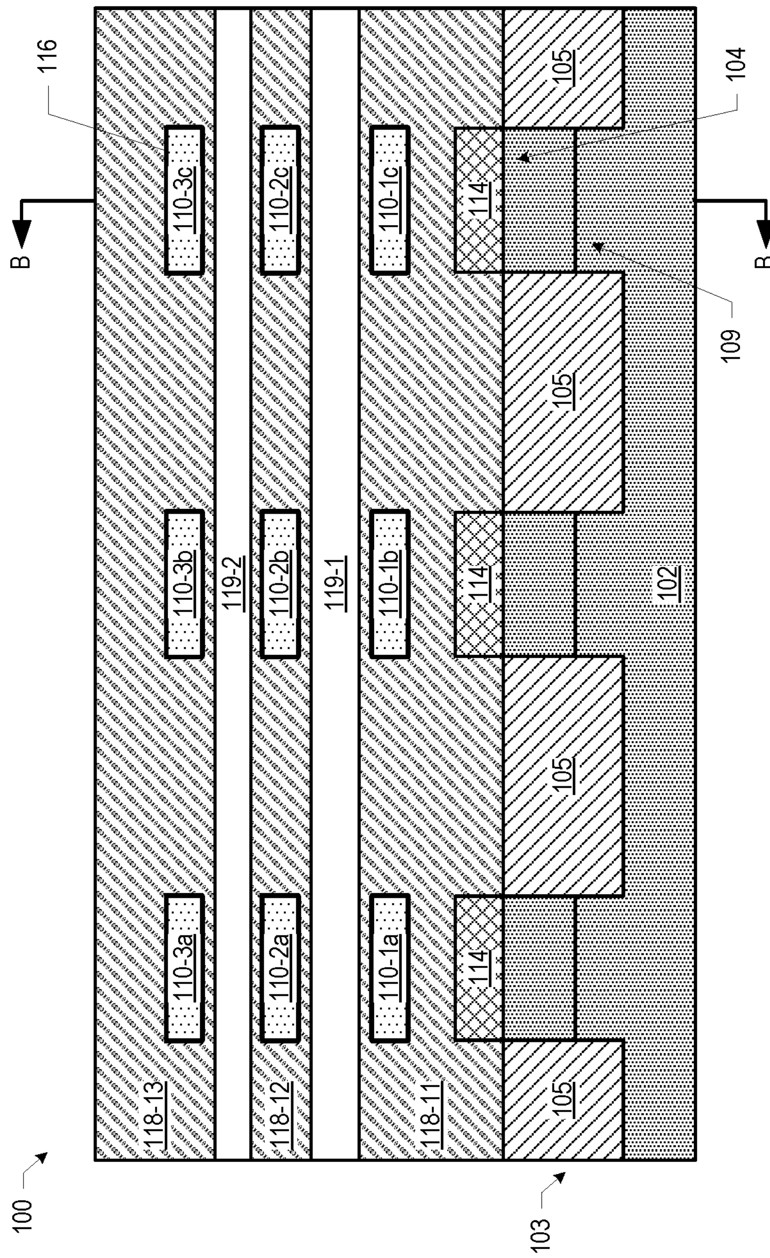


FIG. 1G

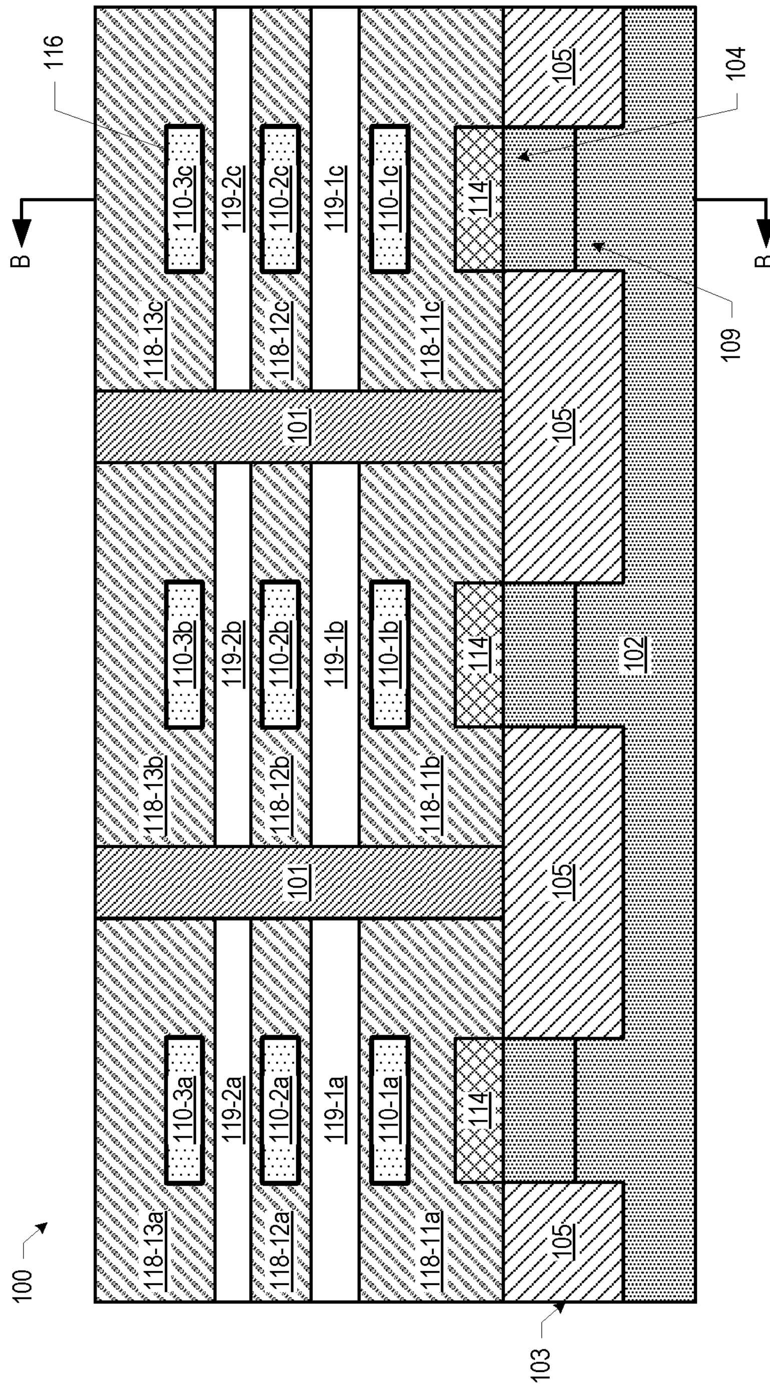
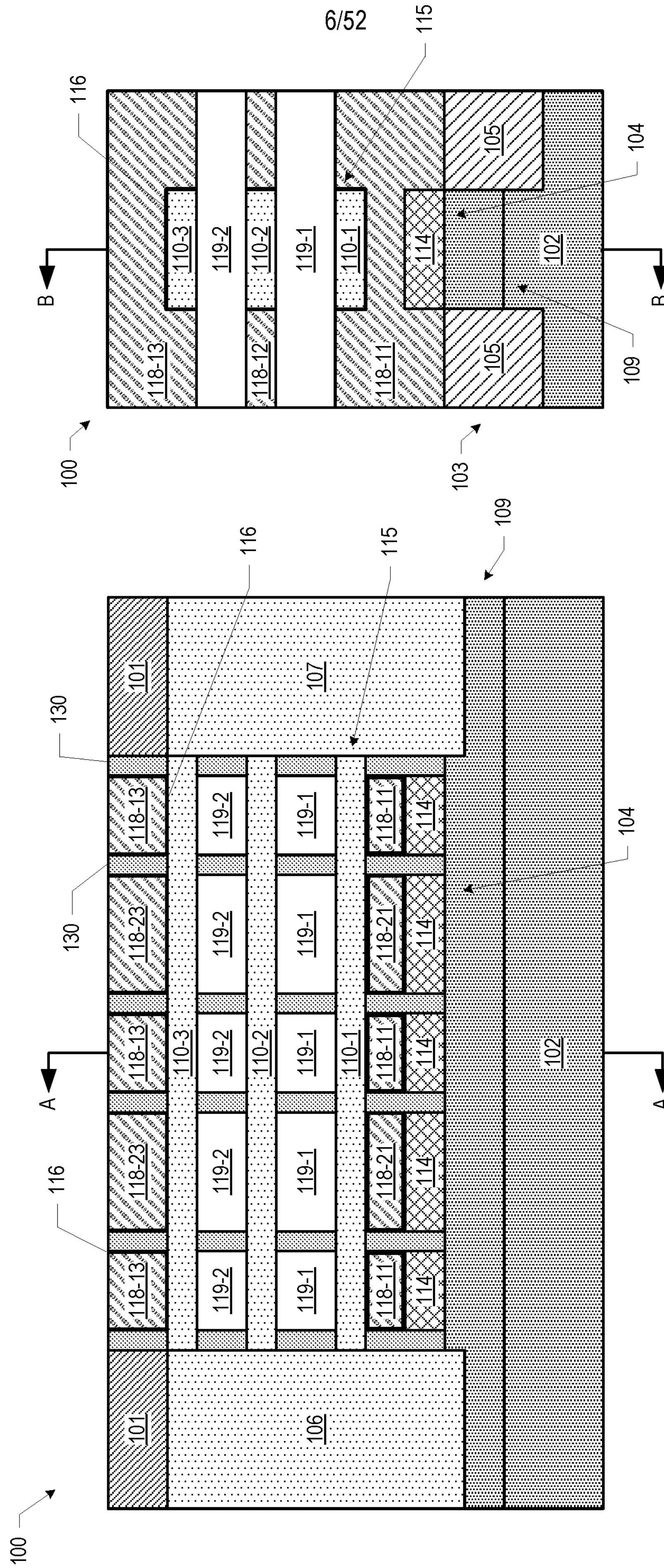


FIG. 1H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116
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118-21
118-13
118-23
114
A
A
FIG. 1I
100
103
118-11
118-12
118-13
110-1
110-2
110-3
119-1
119-2
105
104
102
109
115
116
B
B
FIG. 1J

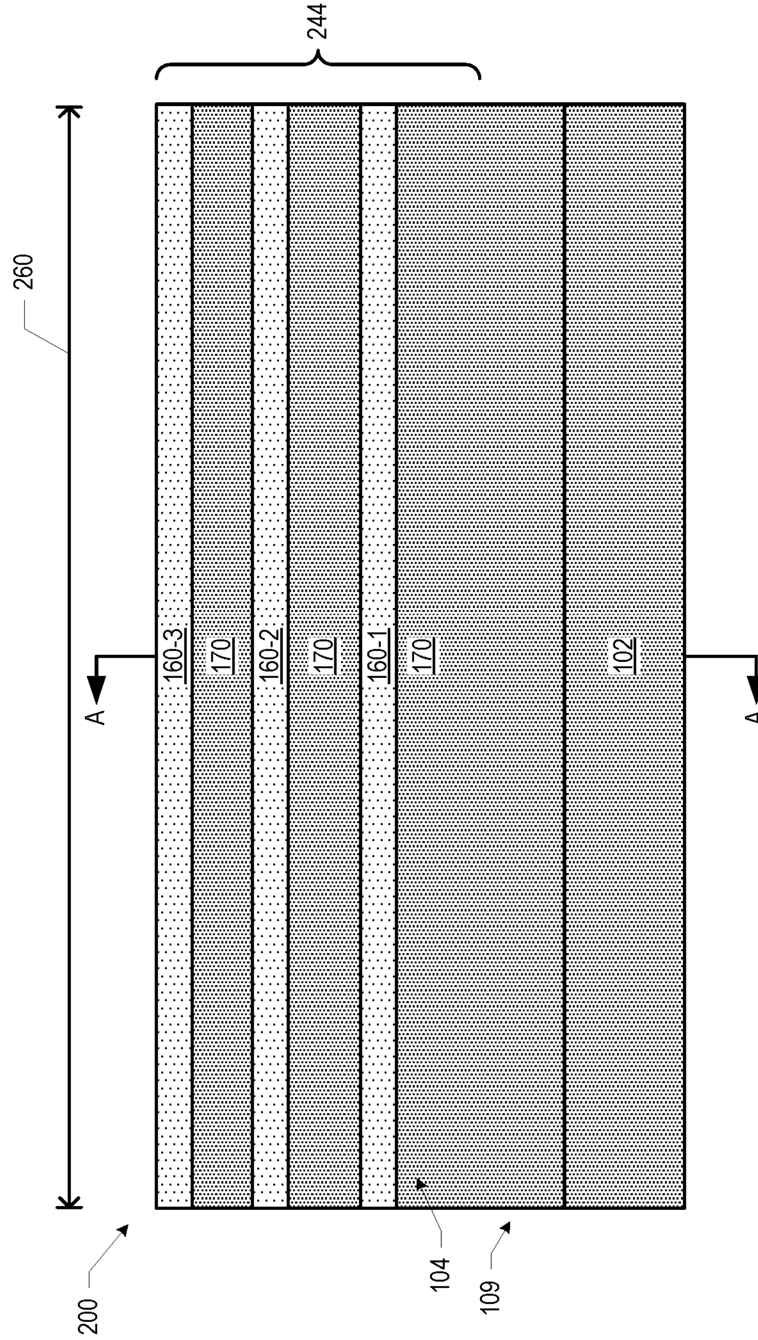


FIG. 2A

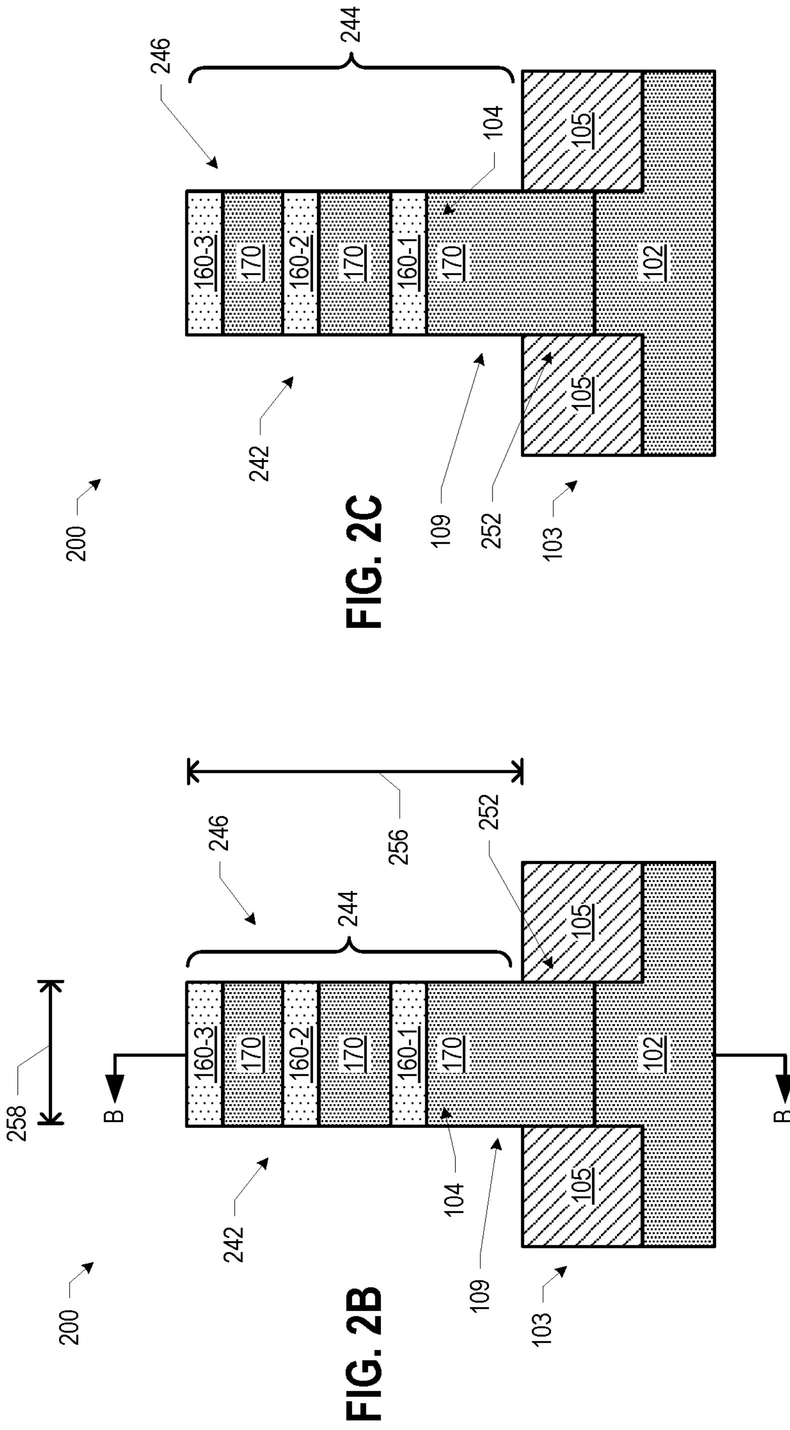


FIG. 2C

FIG. 2B

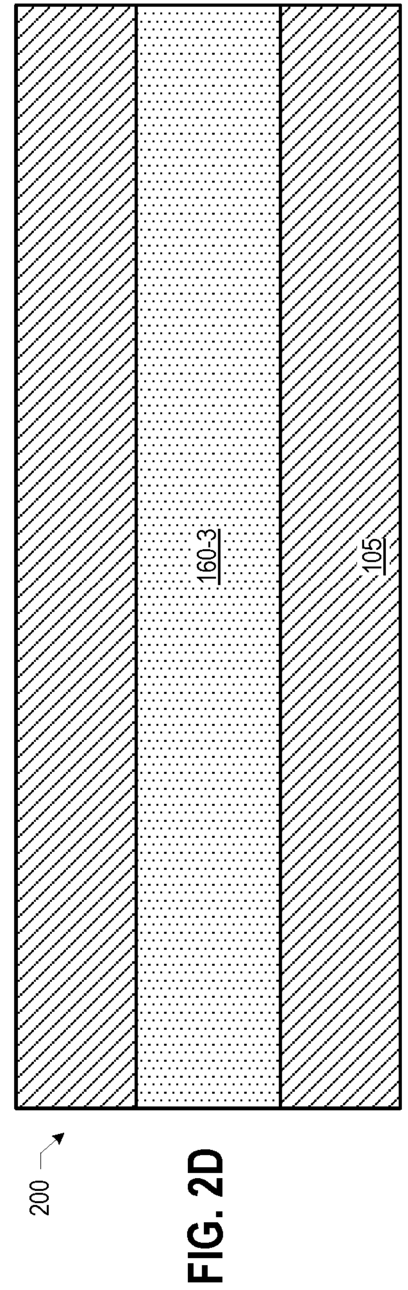


FIG. 2D

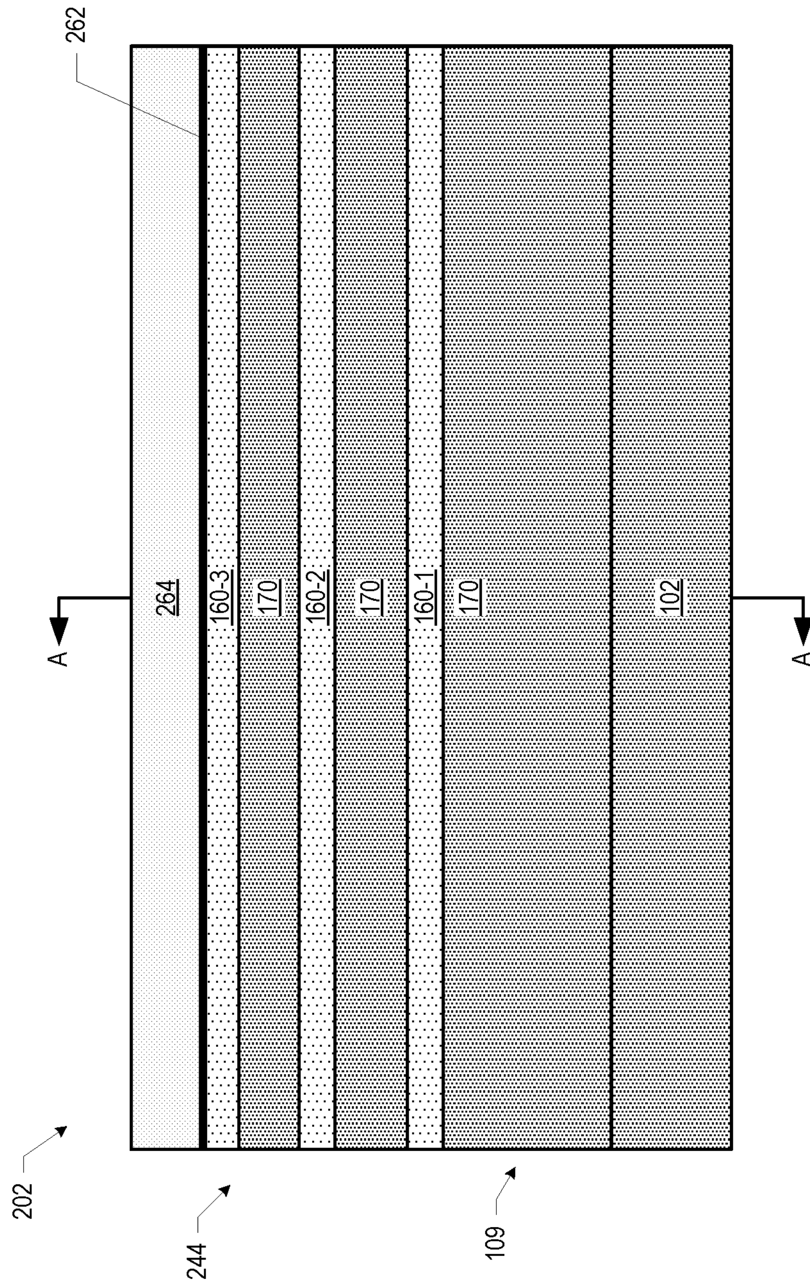


FIG. 3A

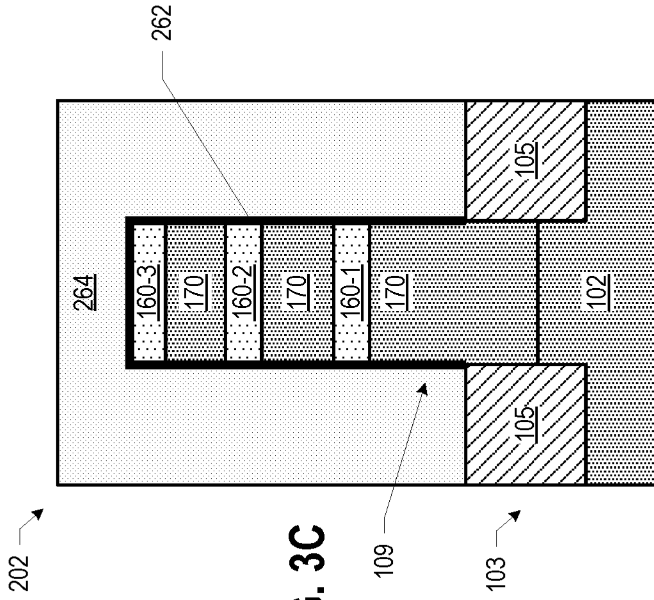


FIG. 3C

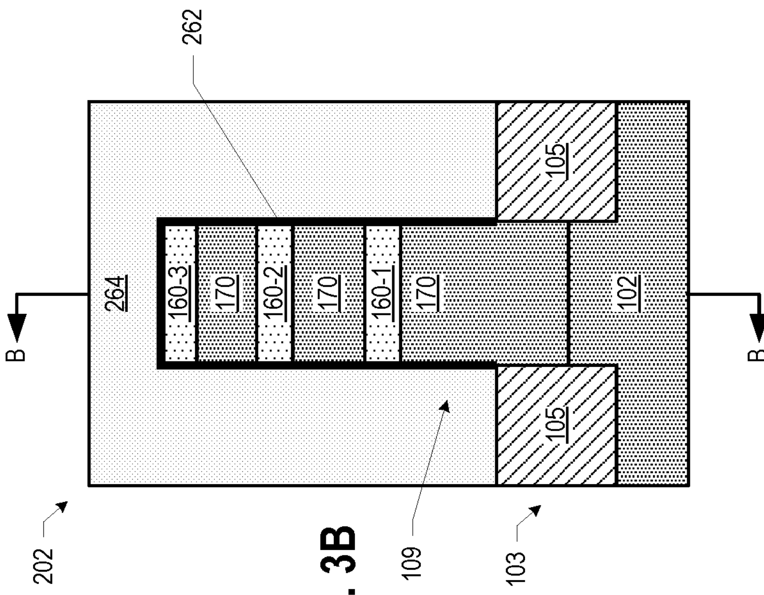


FIG. 3B

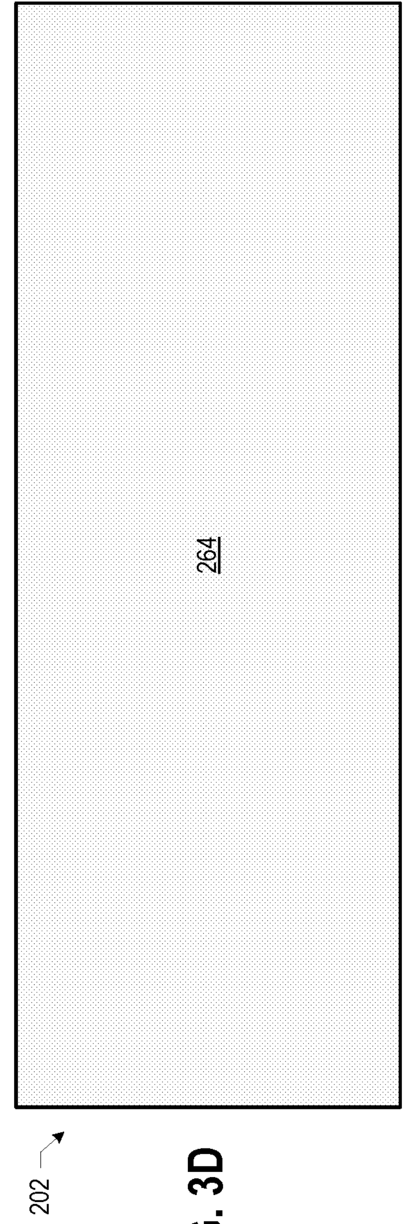


FIG. 3D

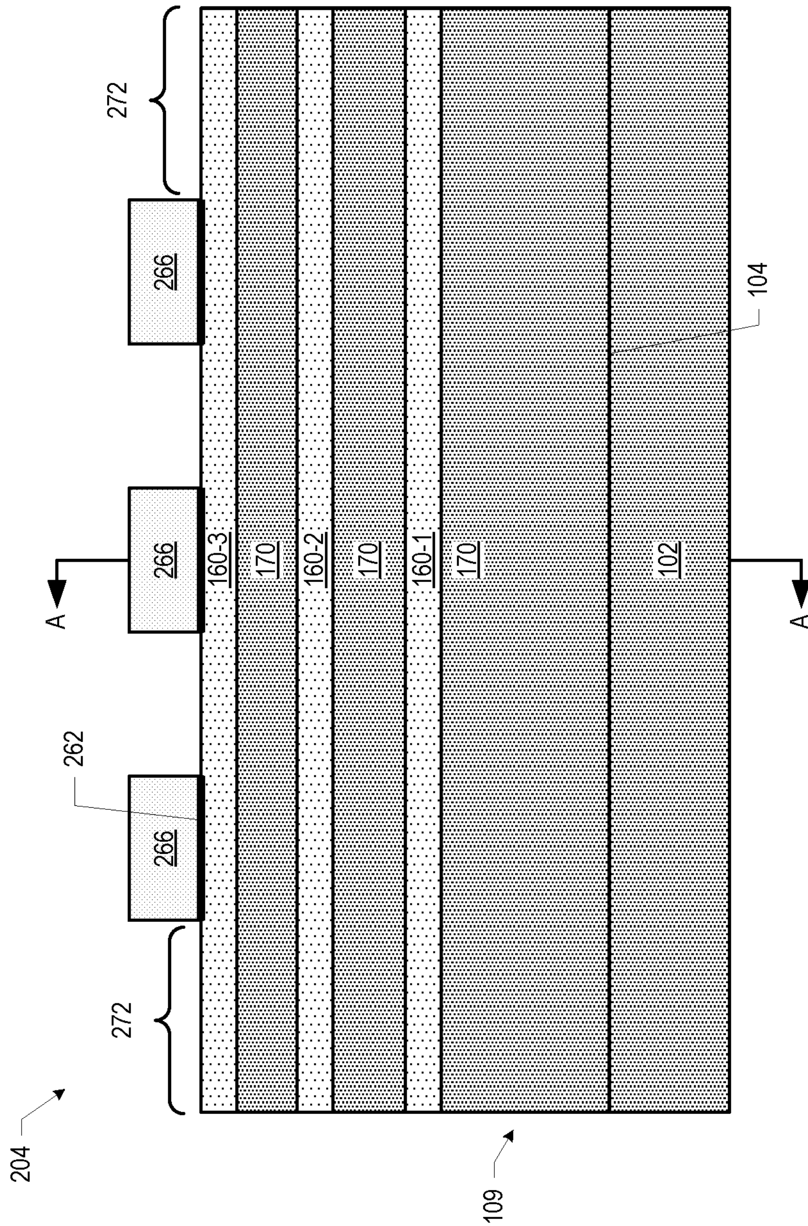
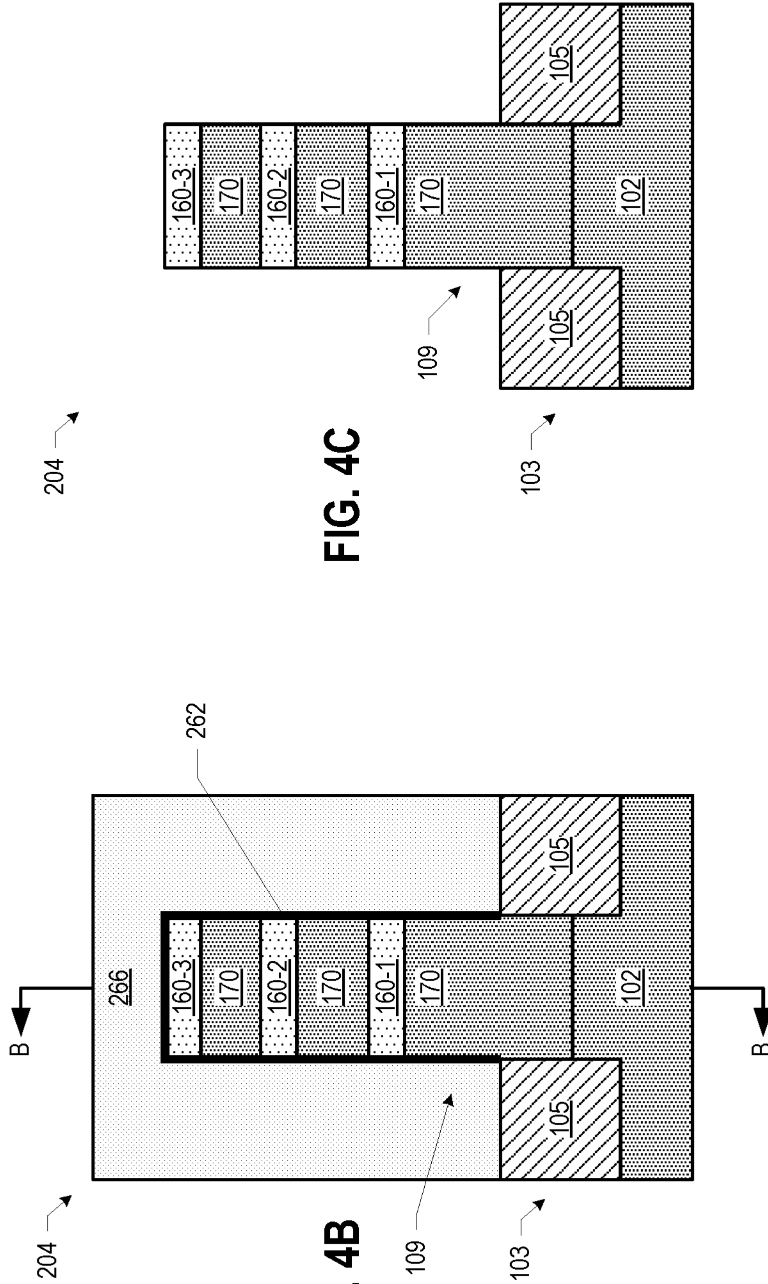
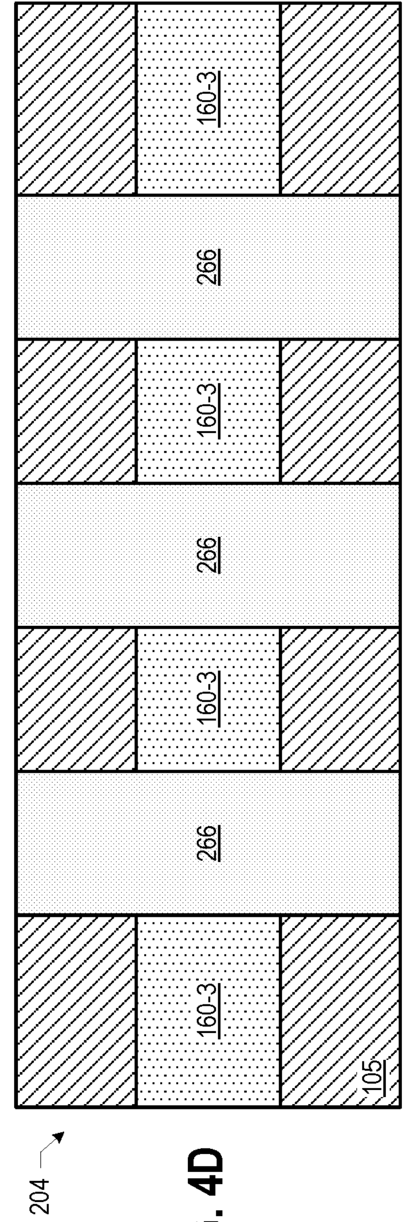


FIG. 4A


204
B
266
160-3
170
160-2
170
160-1
170
102
105
105
262
109
103
B
FIG. 4B
204
160-3
170
160-2
170
160-1
170
102
105
105
109
103
FIG. 4C


160-3
266
160-3
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160-3
266
160-3
105
204
FIG. 4D

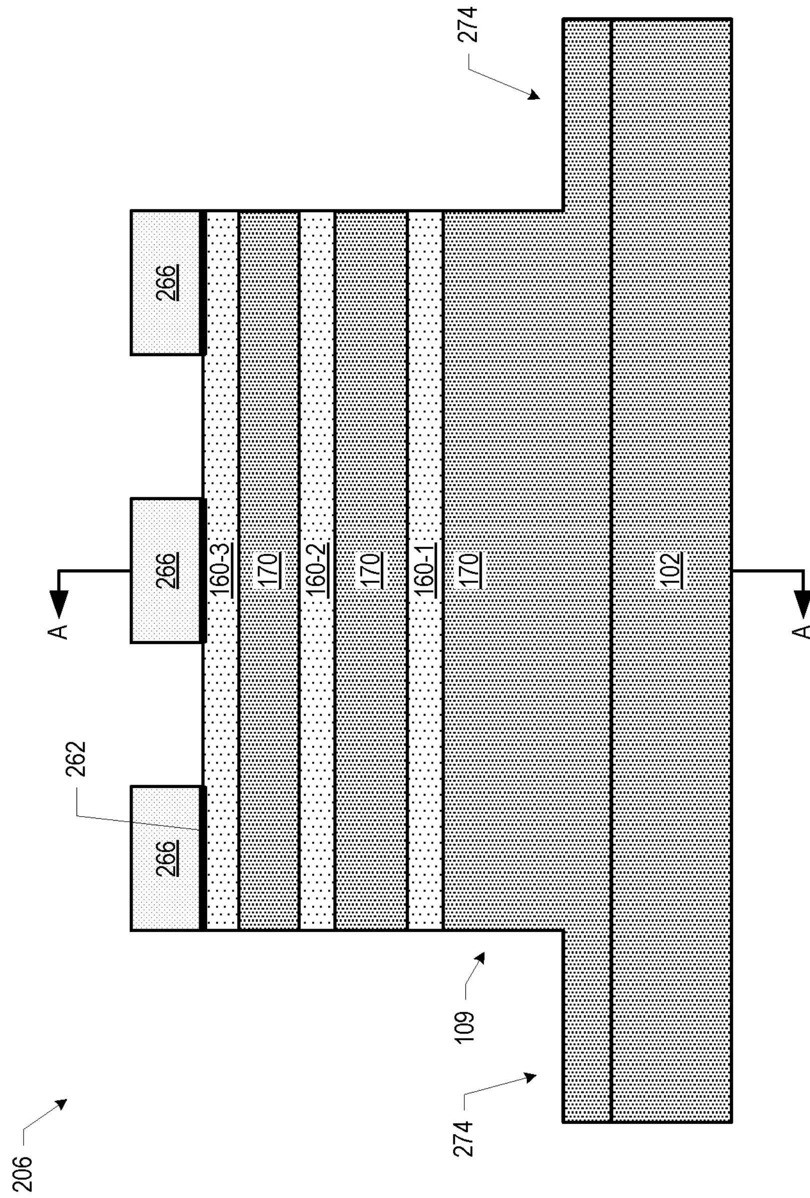


FIG. 5A

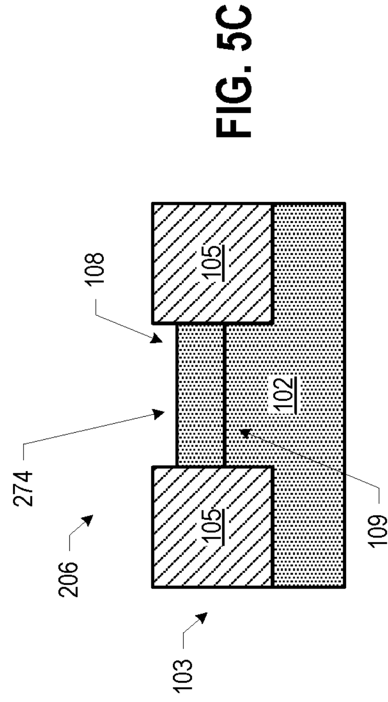


FIG. 5C

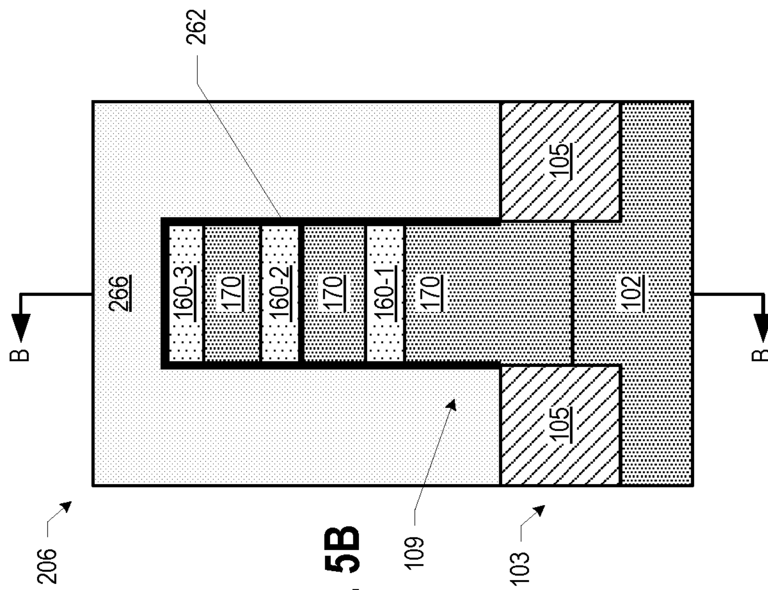


FIG. 5B

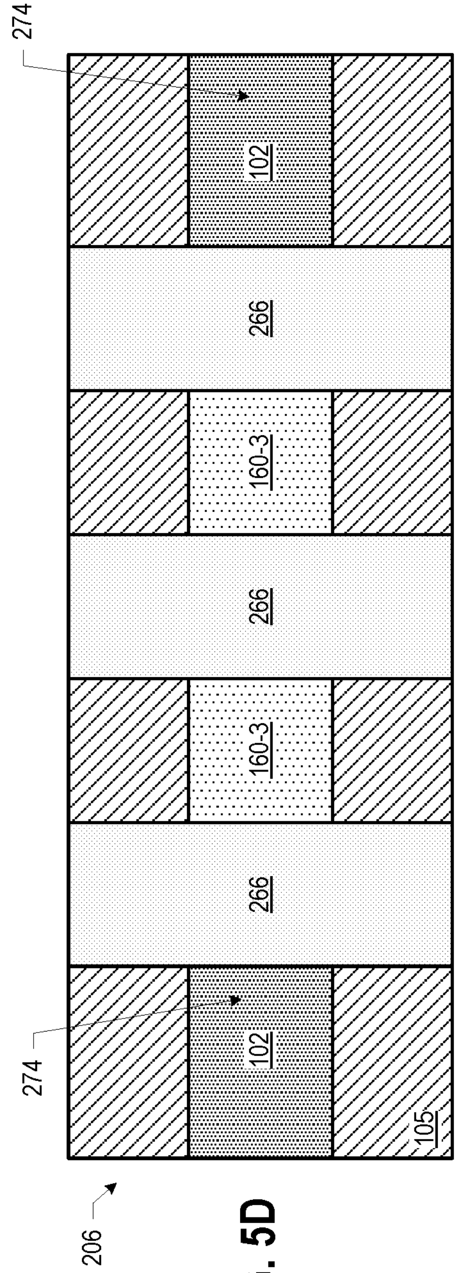


FIG. 5D

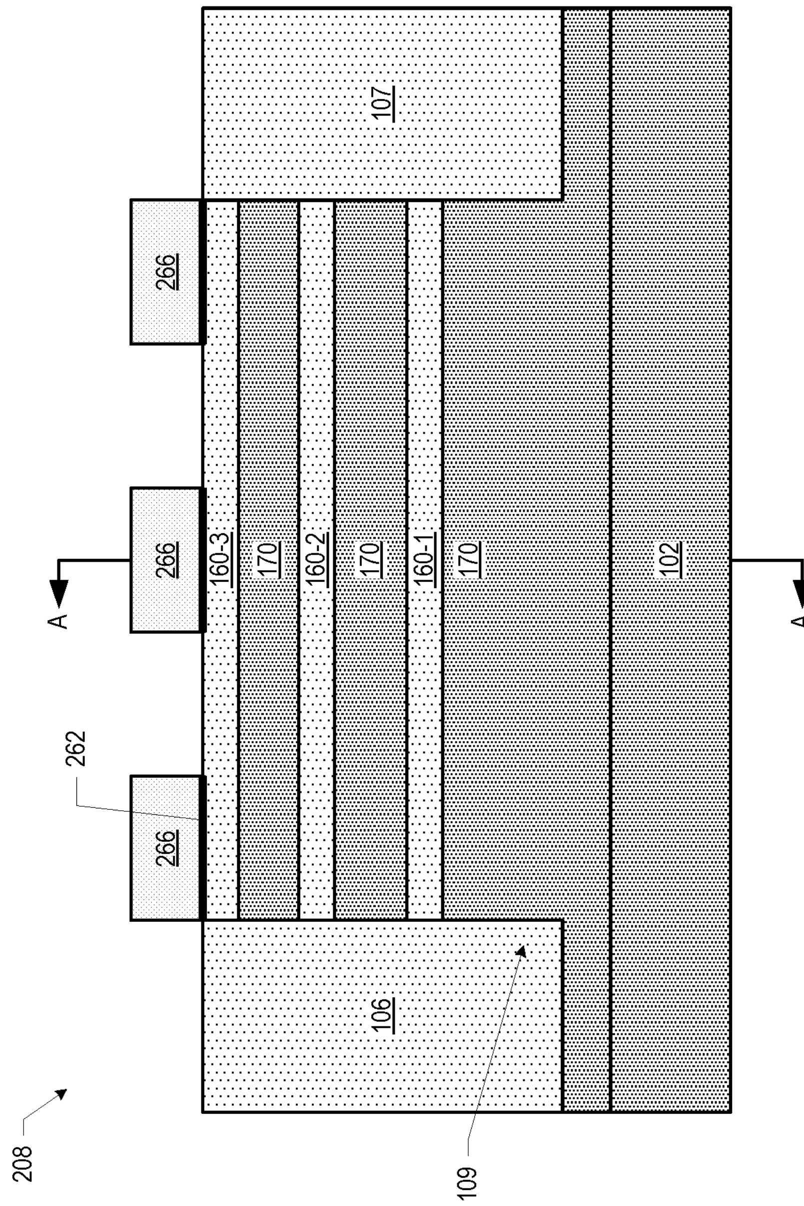


FIG. 6A

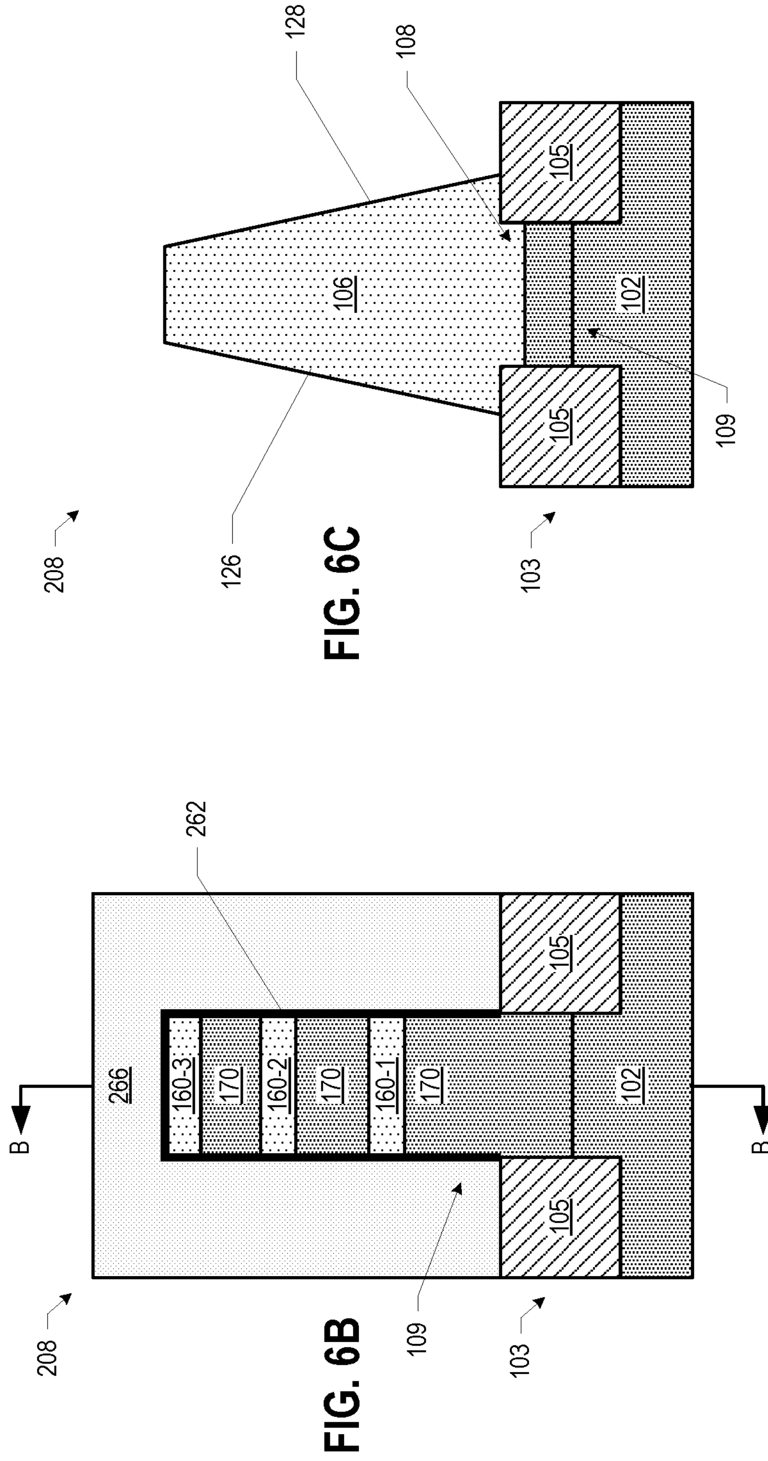


FIG. 6B

FIG. 6C

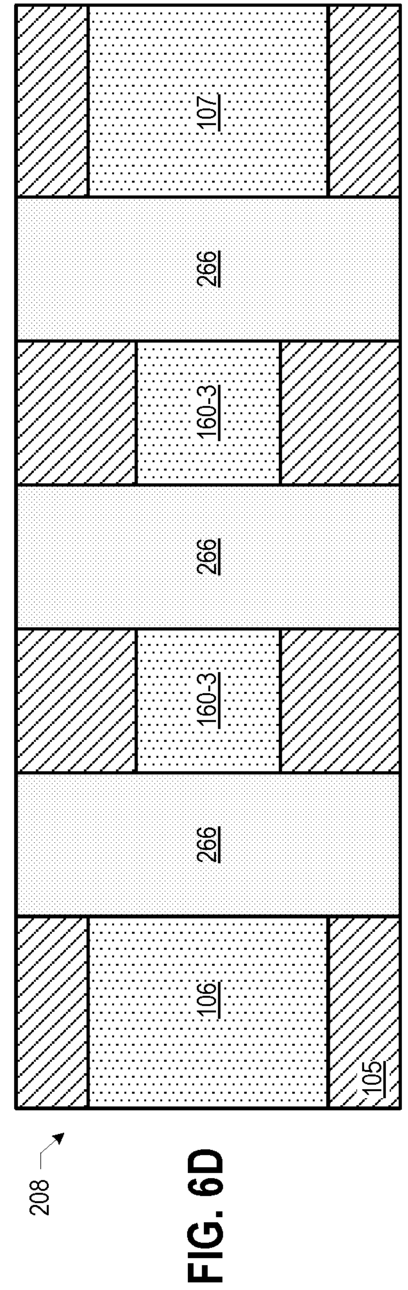


FIG. 6D

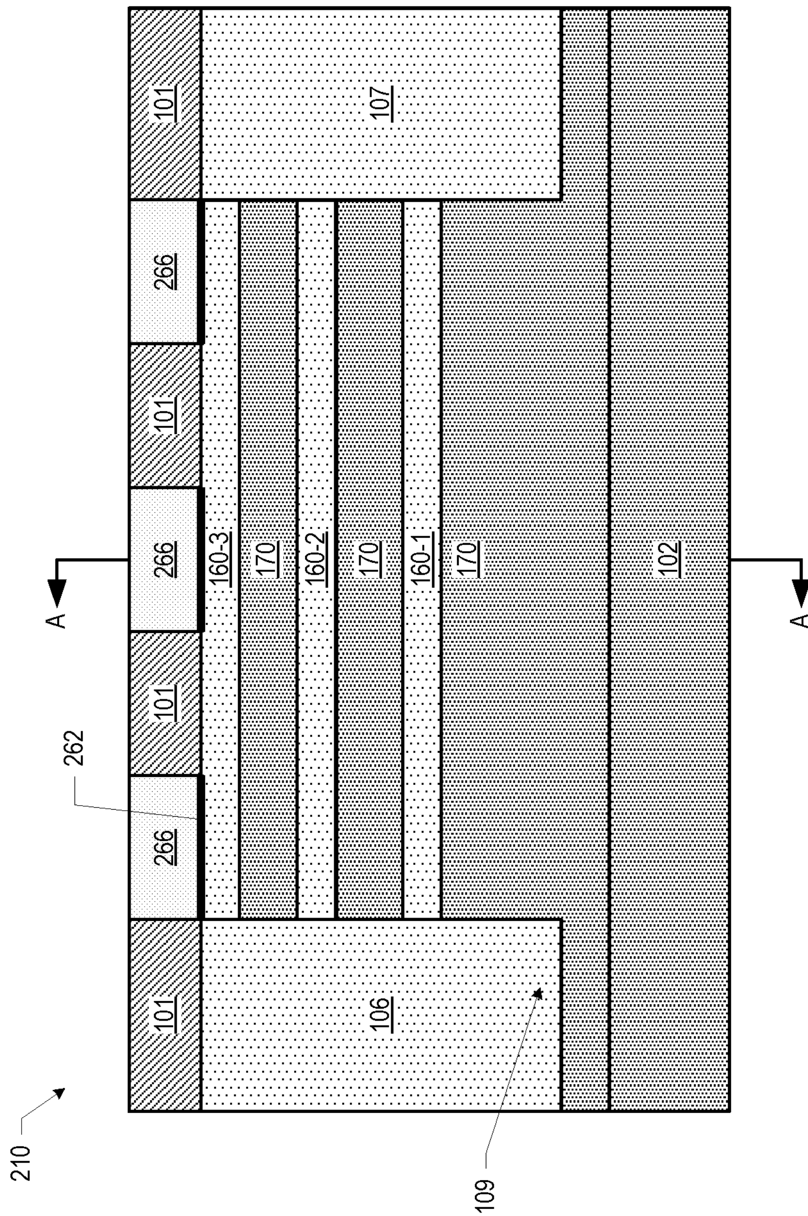


FIG. 7A

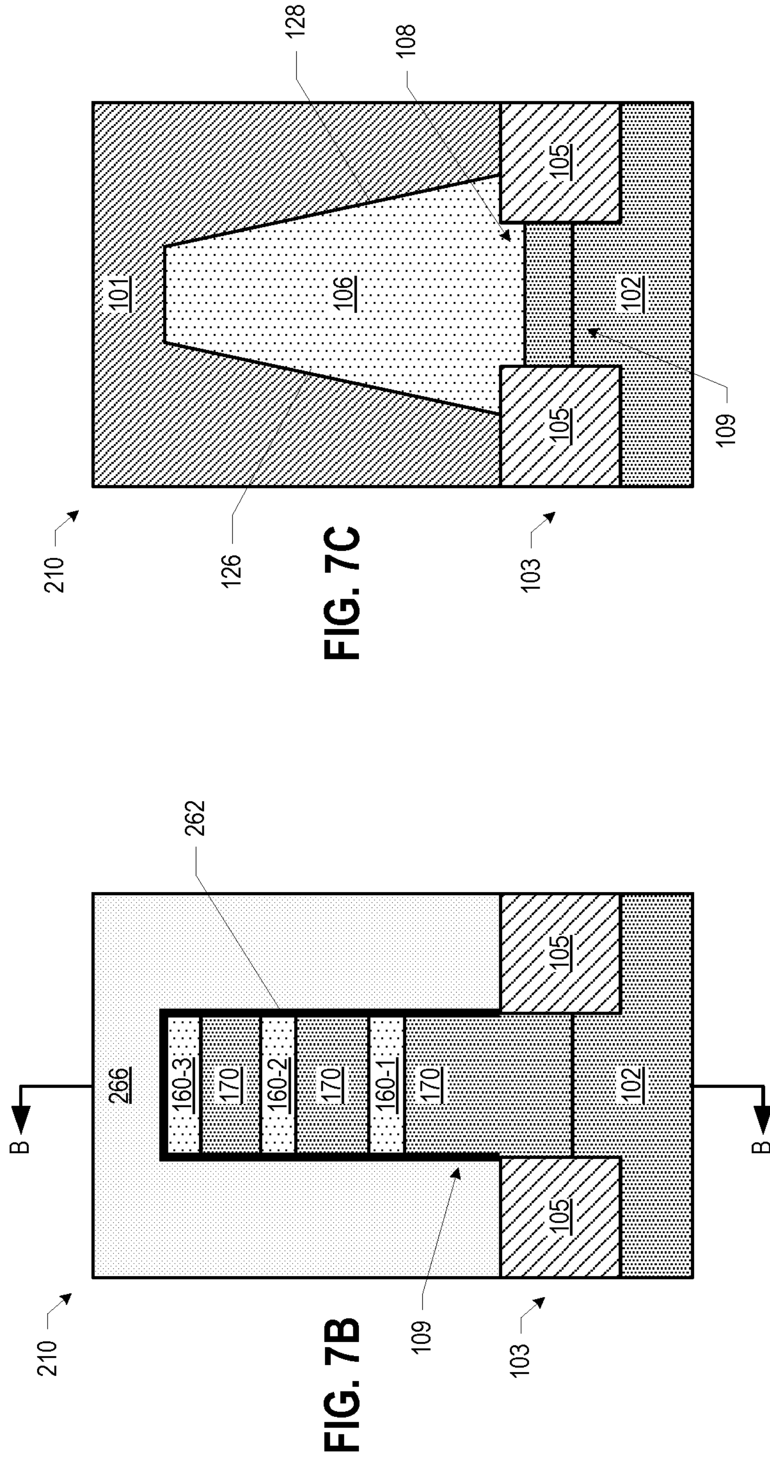


FIG. 7B

FIG. 7C

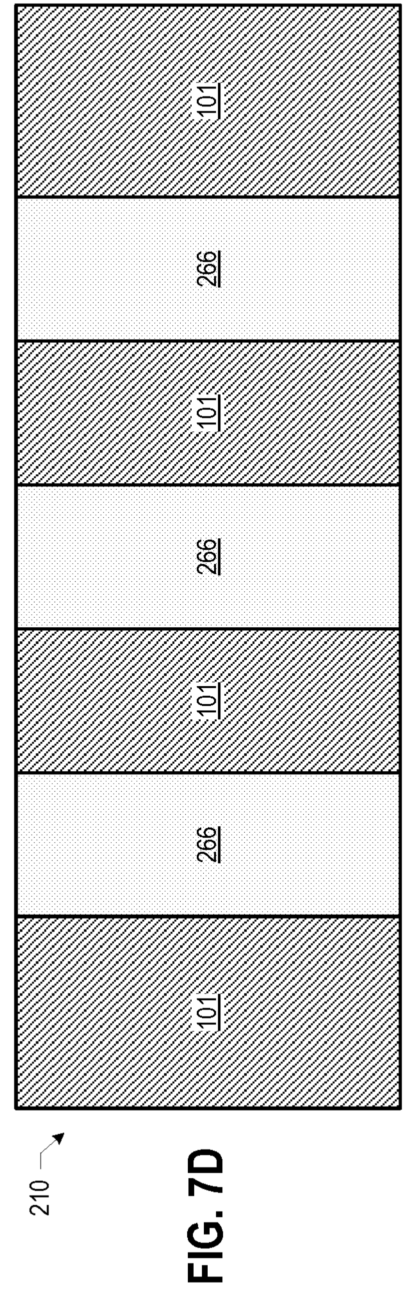


FIG. 7D

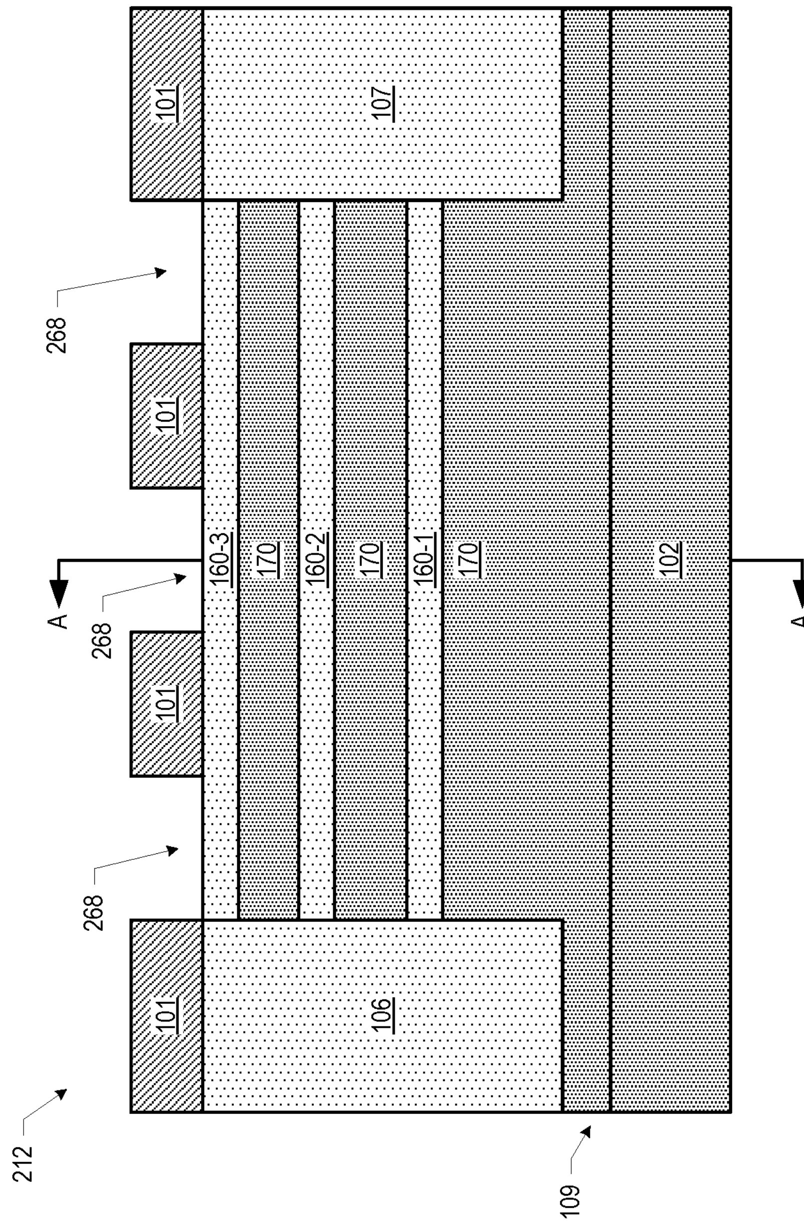


FIG. 8A

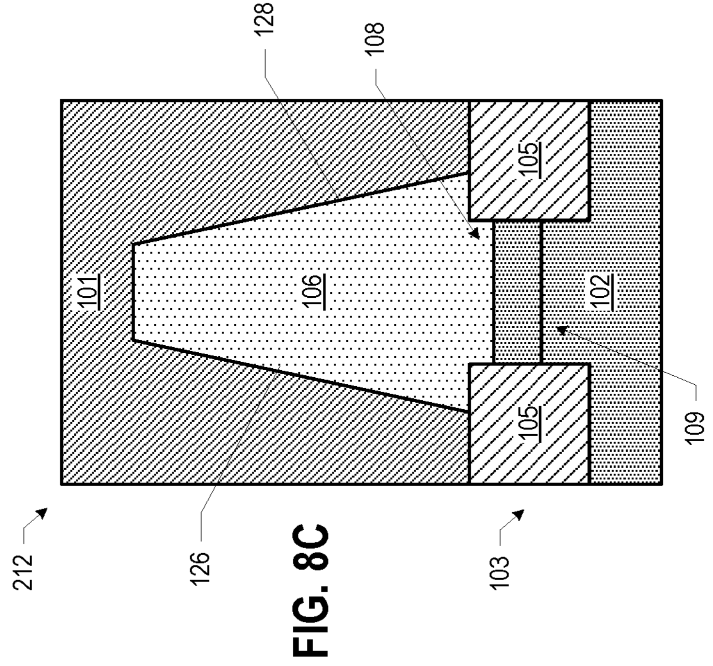


FIG. 8C

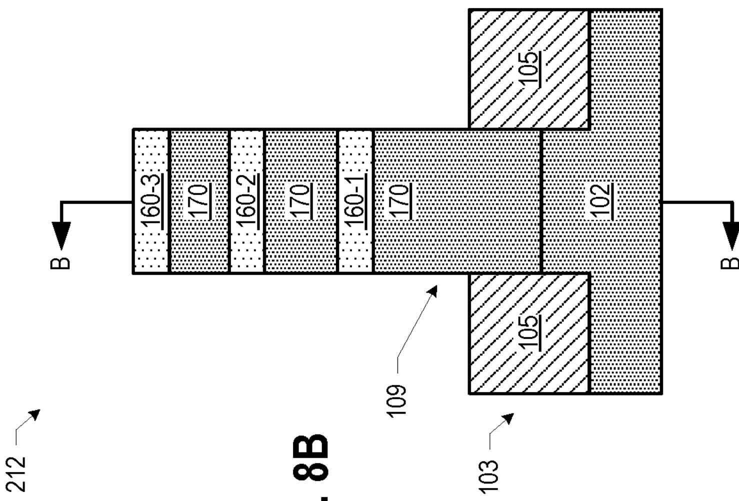


FIG. 8B

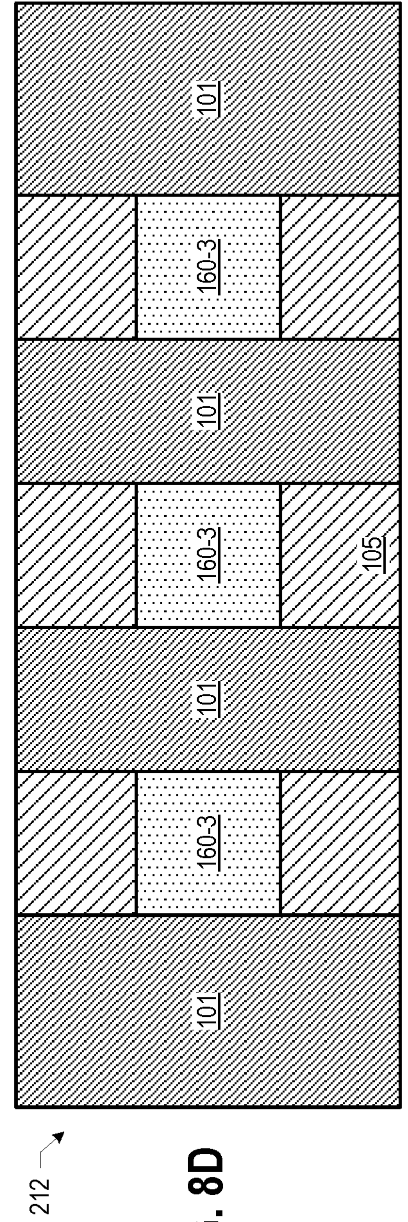


FIG. 8D

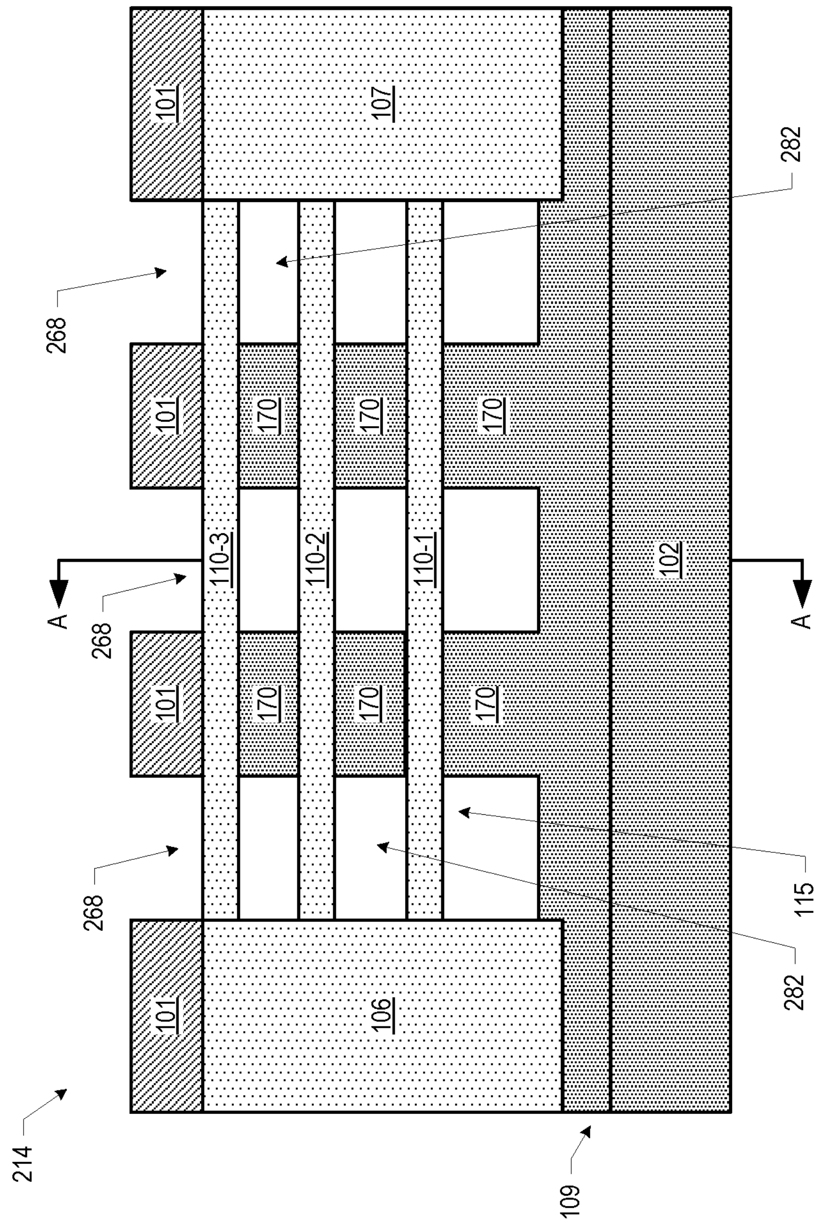


FIG. 9A

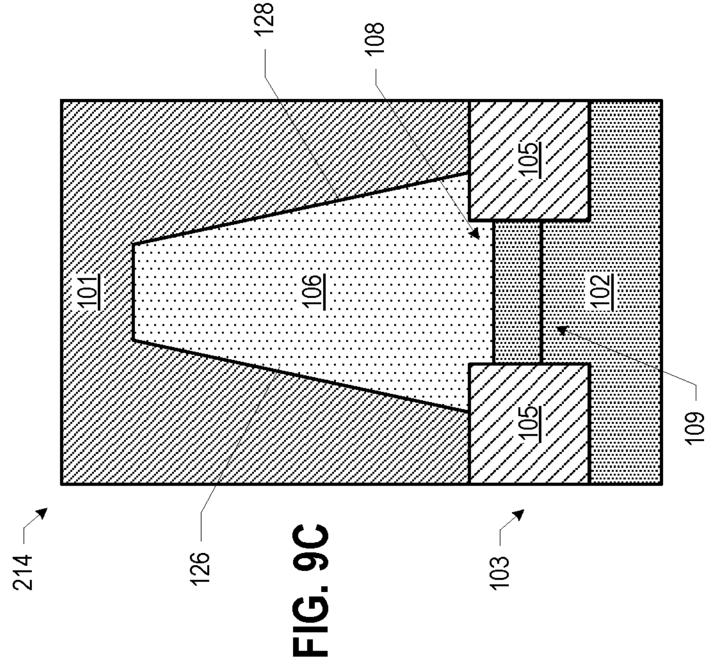


FIG. 9C

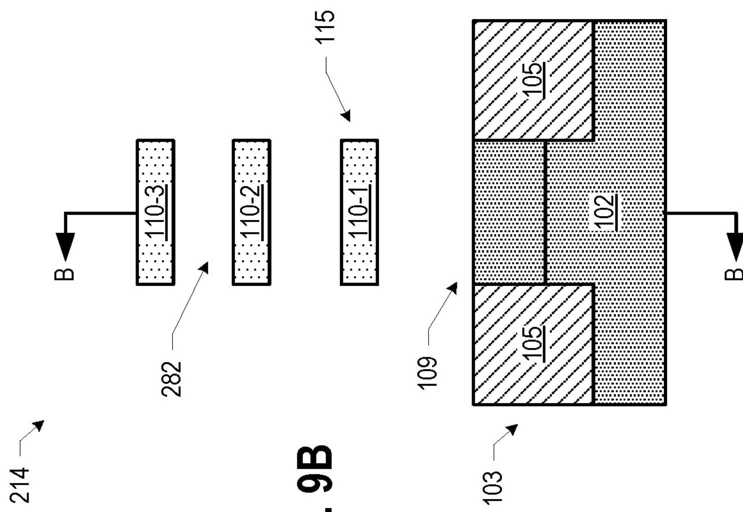


FIG. 9B

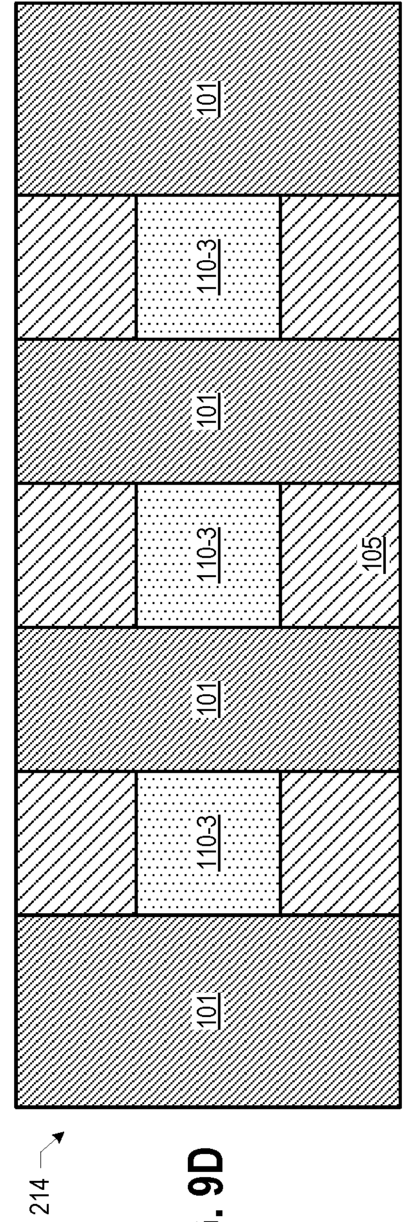


FIG. 9D

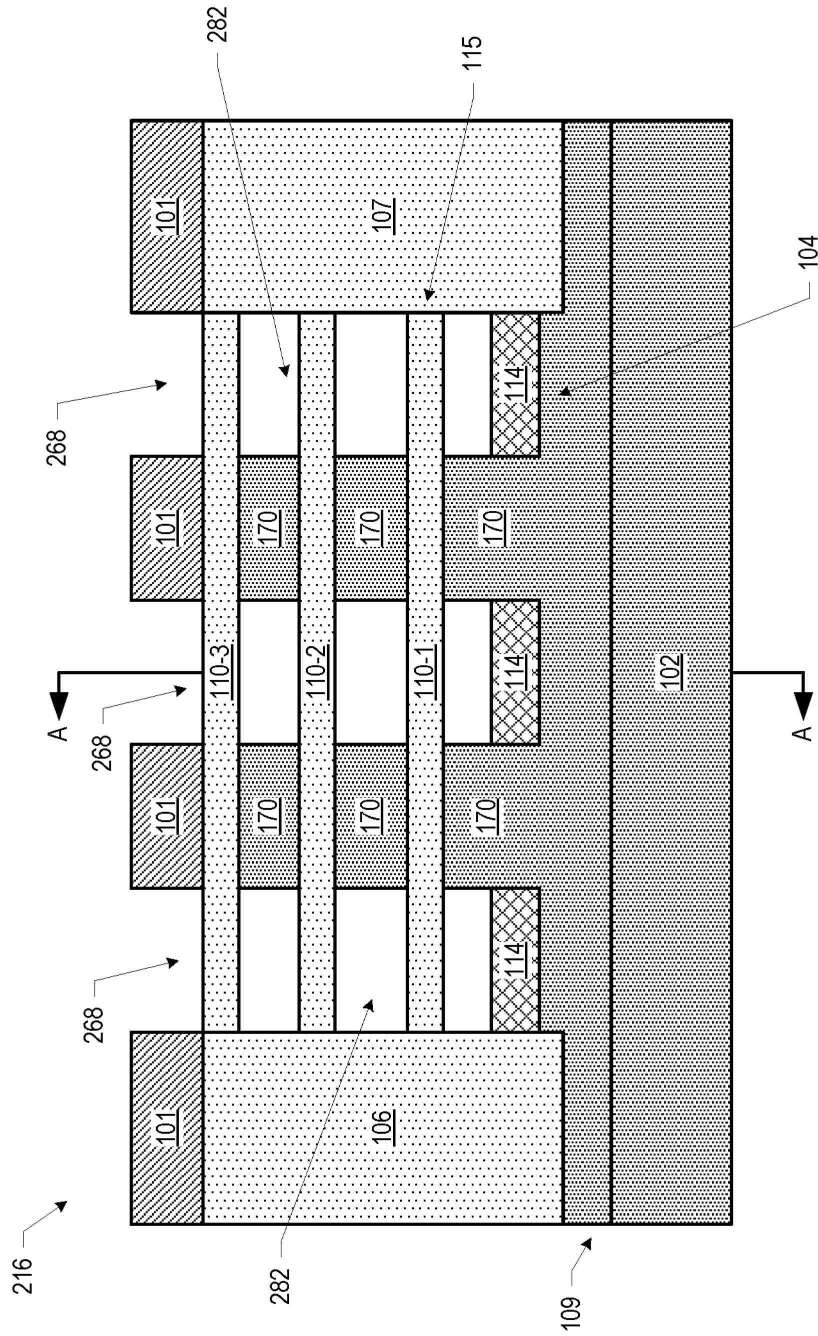


FIG. 10A

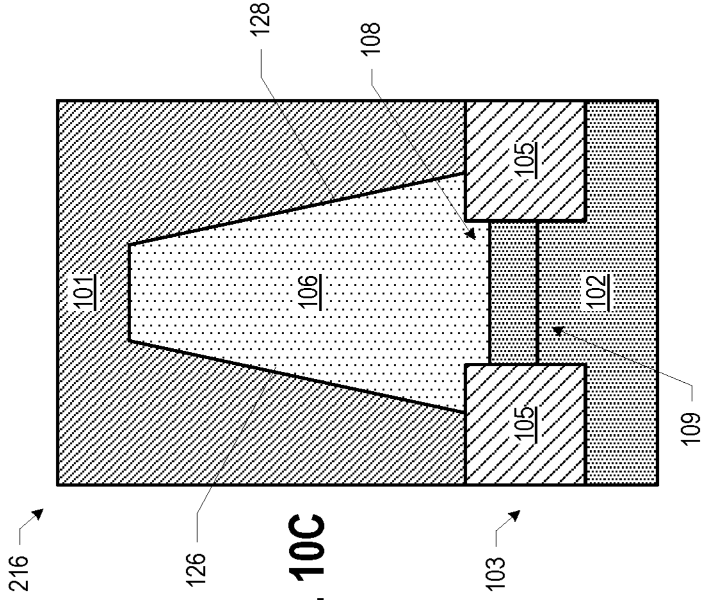


FIG. 10C

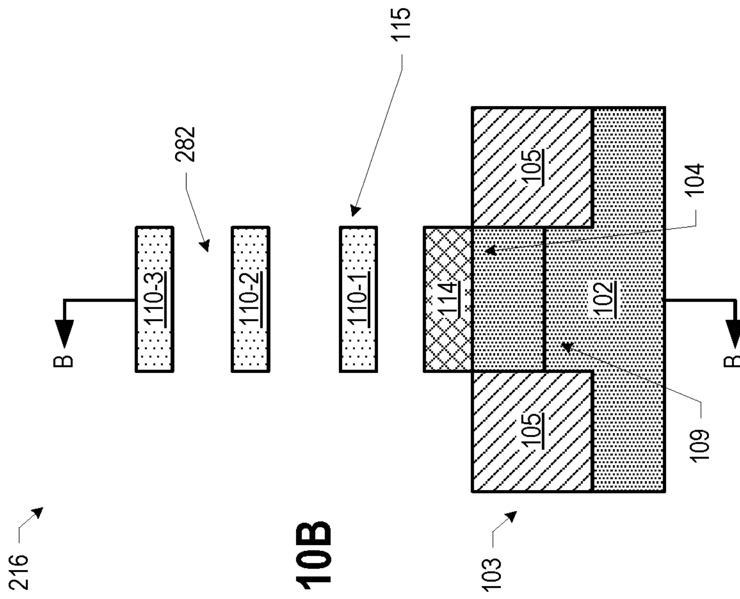


FIG. 10B

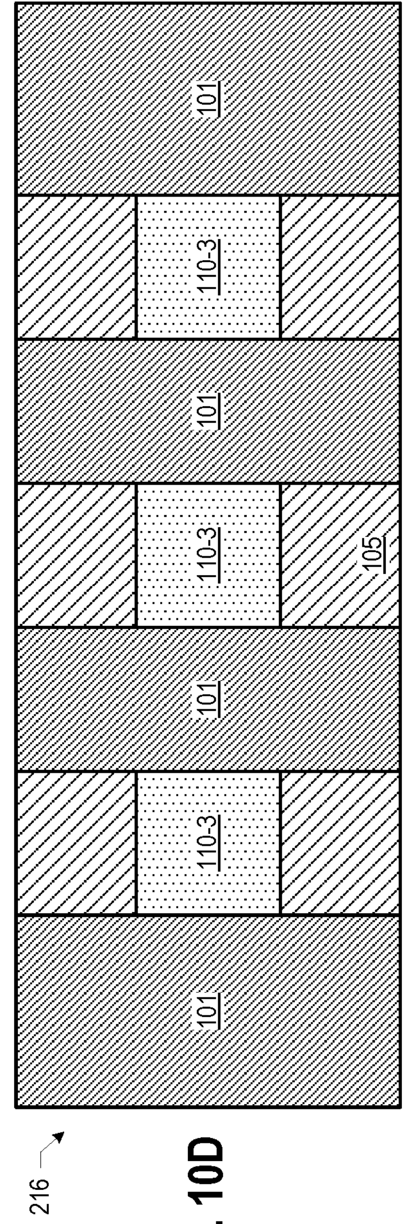


FIG. 10D

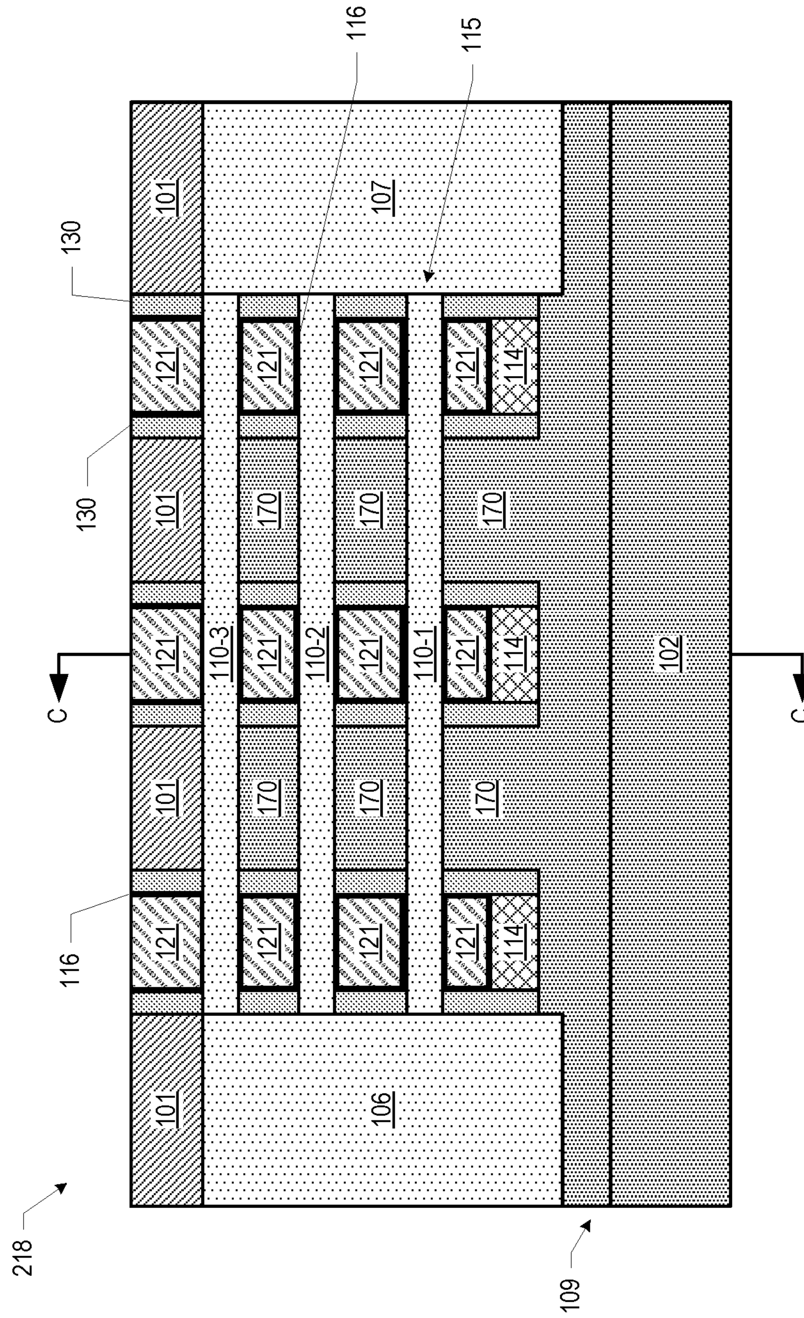
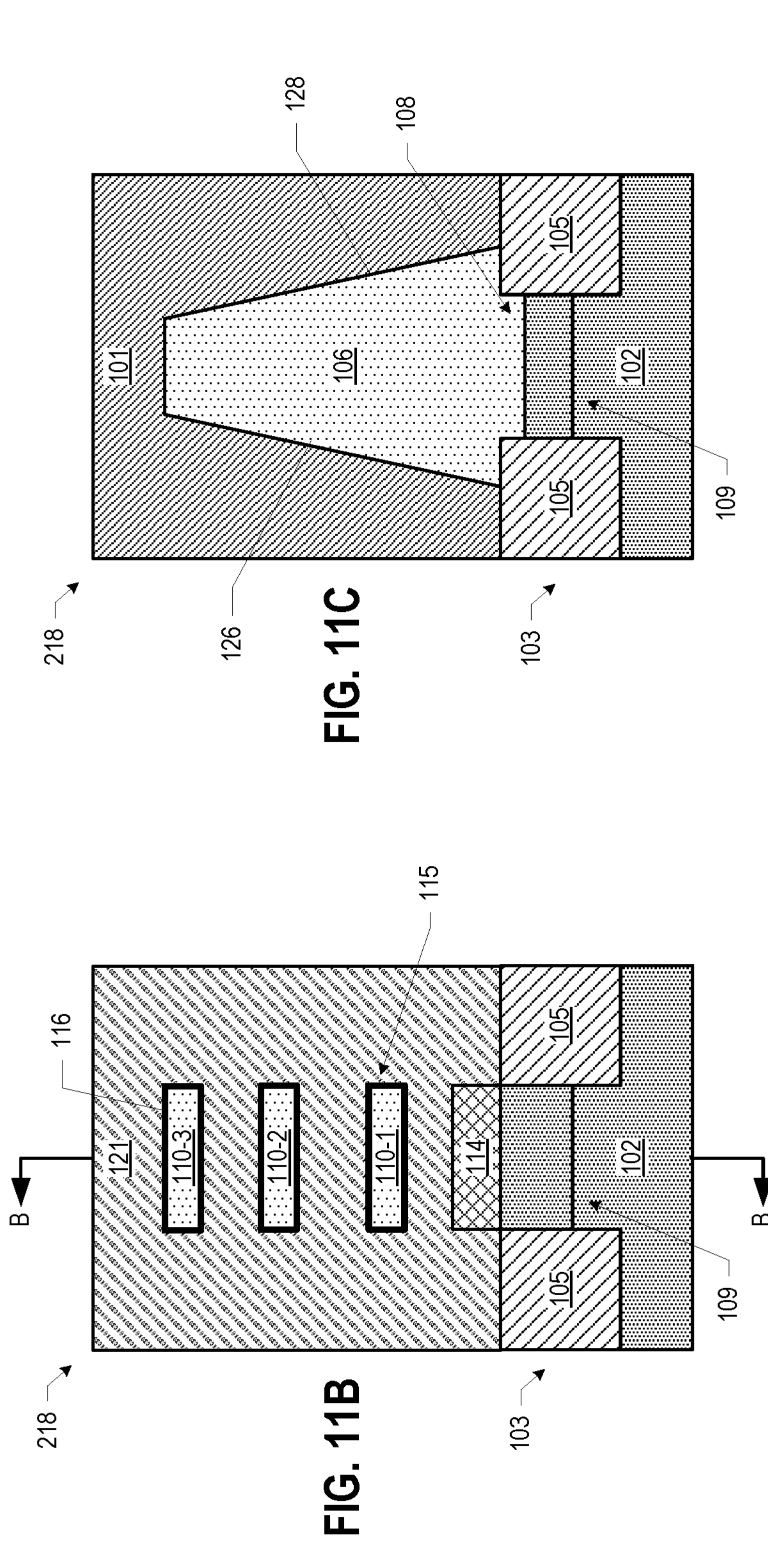
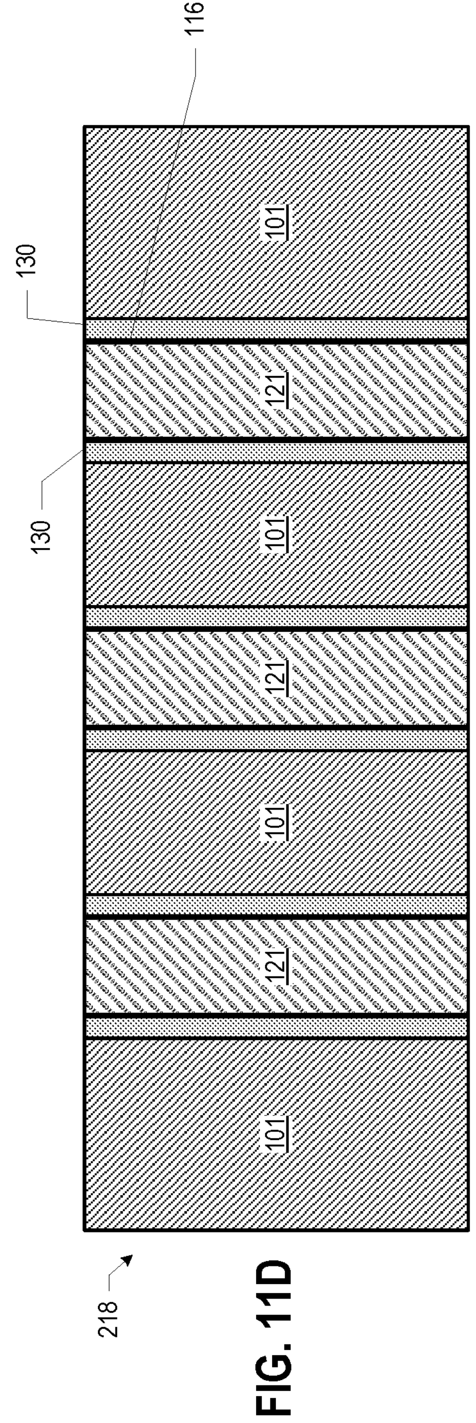


FIG. 11A


218
126
128
108
101
106
105
105
102
109
103
FIG. 11C
218
B
B
116
115
121
110-3
110-2
110-1
114
105
105
102
109
103
FIG. 11B


116
130
130
101
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101
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101
218
FIG. 11D

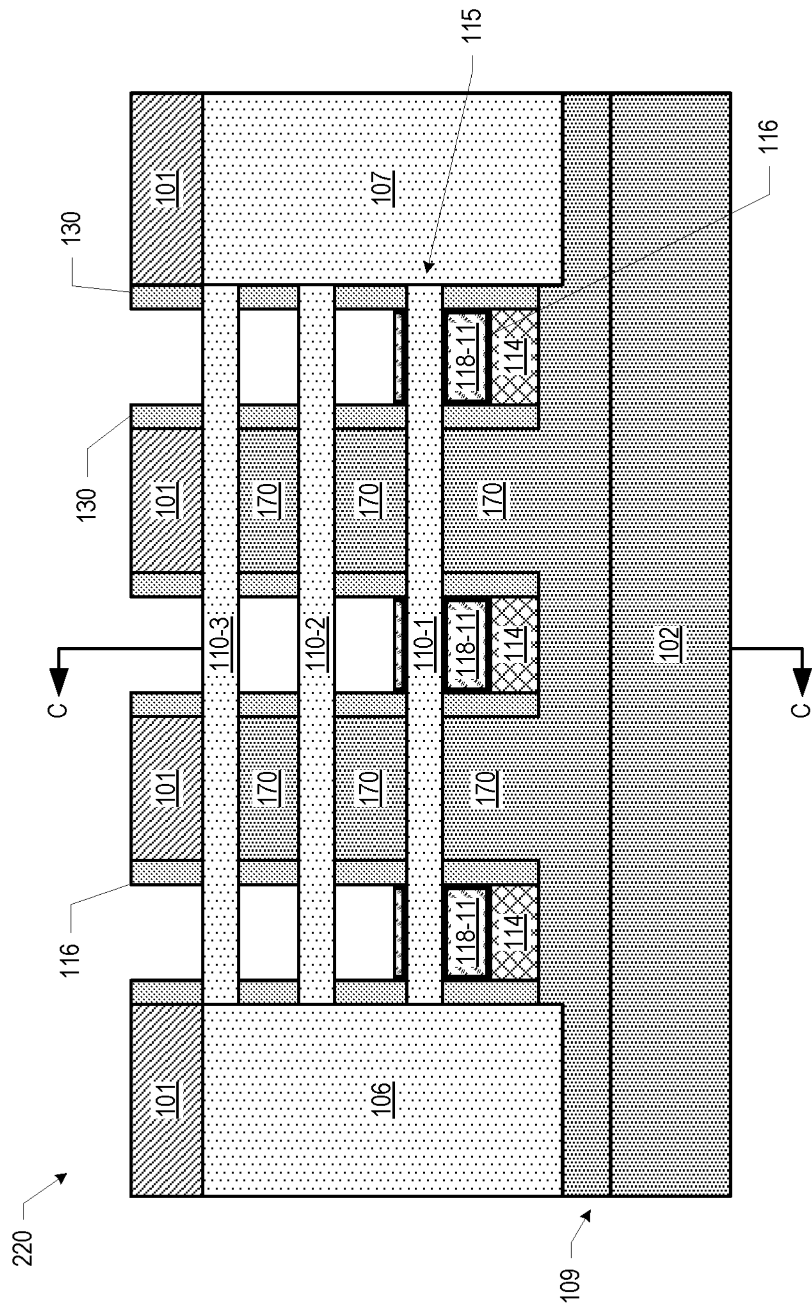


FIG. 12A

220
103
B
110-3
110-2
116
110-1
115
114
118-11
105
102
109
B

FIG. 12B

220
126
103
101
106
128
108
105
102
109

FIG. 12C

220
101
130
118-11
110-3
116
101
130

FIG. 12D

222
101
106
116
119-1
118-11
114
109
101
170
170
170
C
110-3
110-2
119-1
110-1
118-11
114
102
C
130
101
170
170
170
130
119-1
118-11
114
101
107
115
116

FIG. 13A

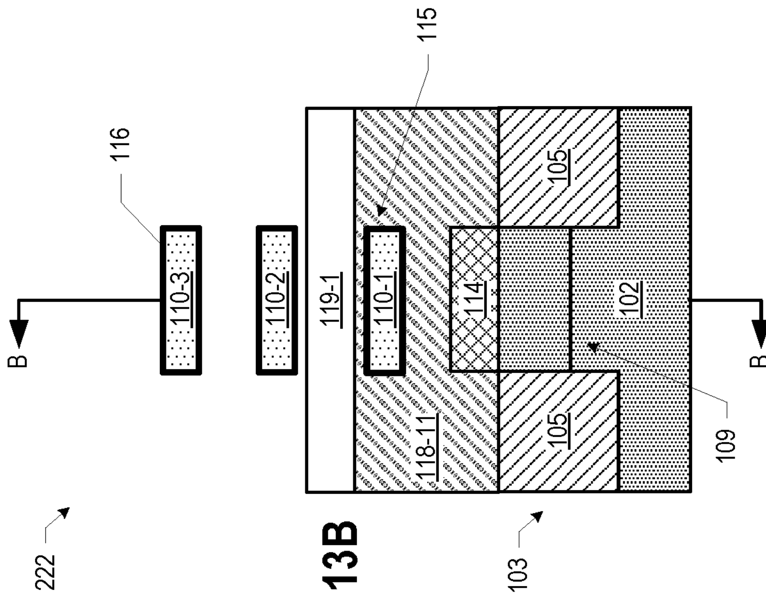


FIG. 13B

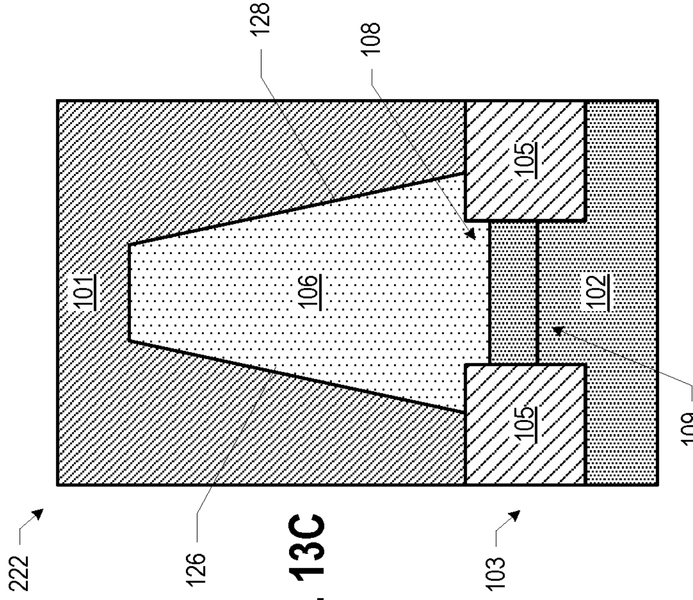


FIG. 13C

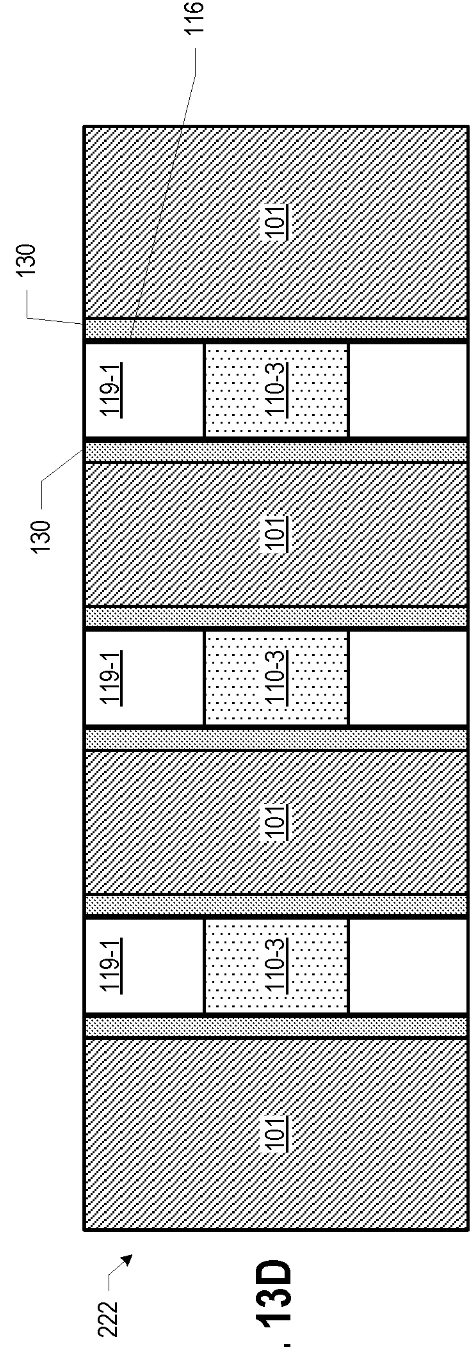


FIG. 13D

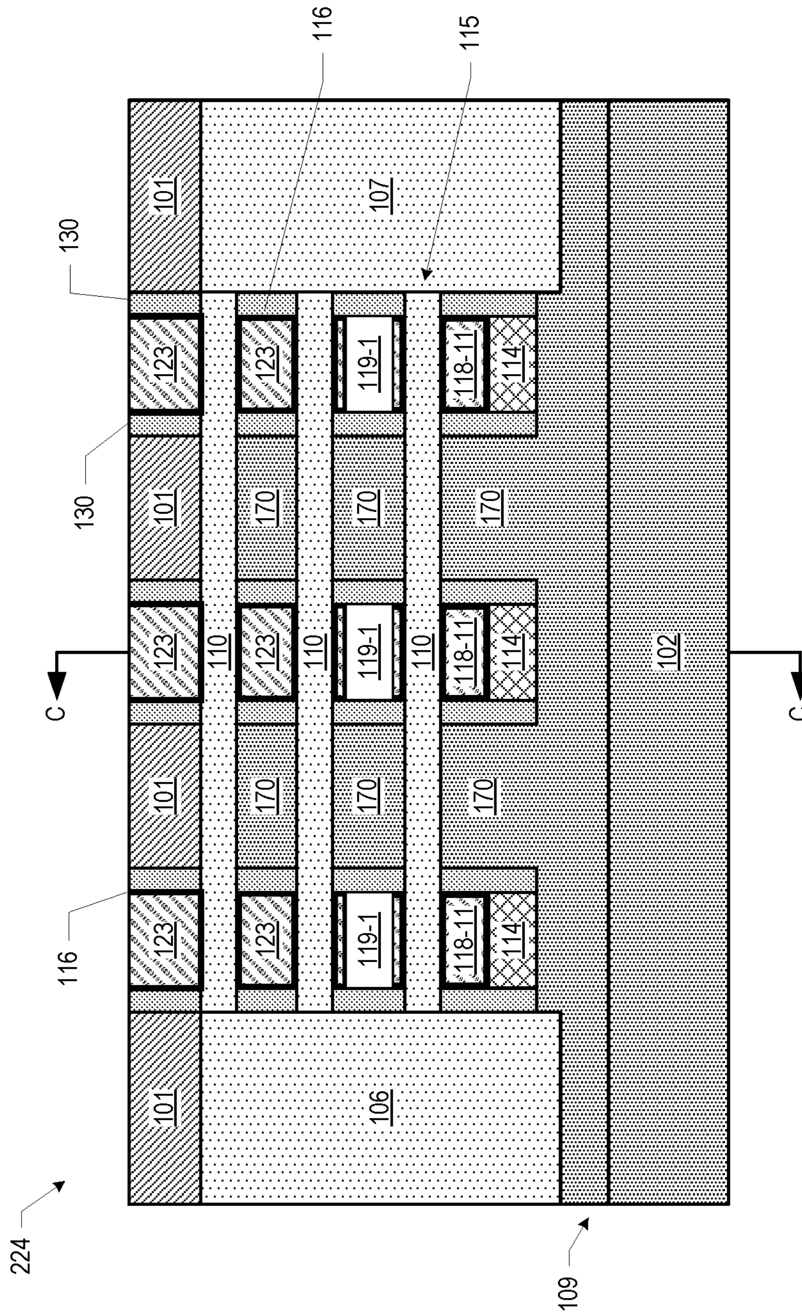


FIG. 14A

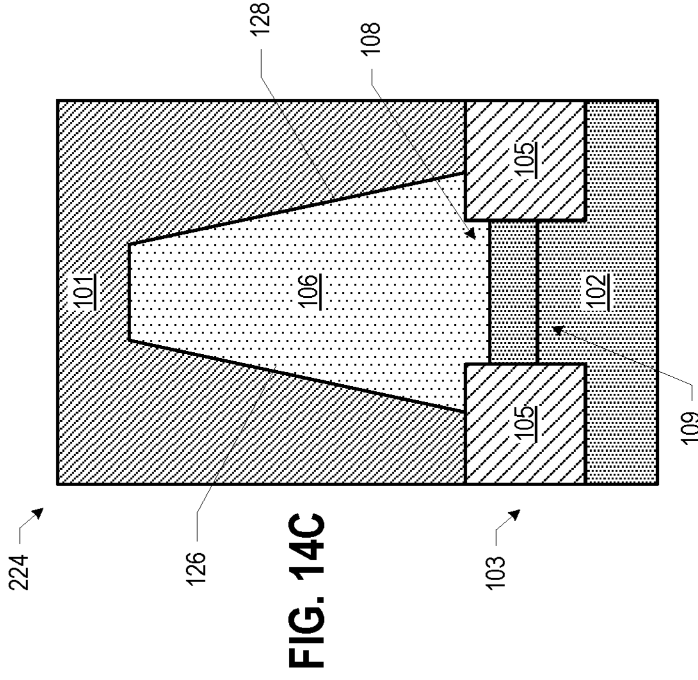


FIG. 14C

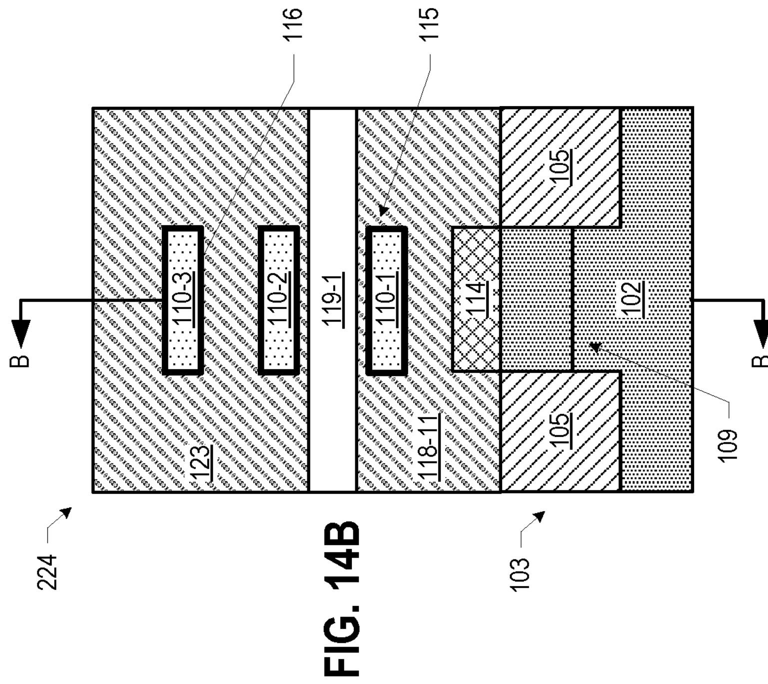


FIG. 14B

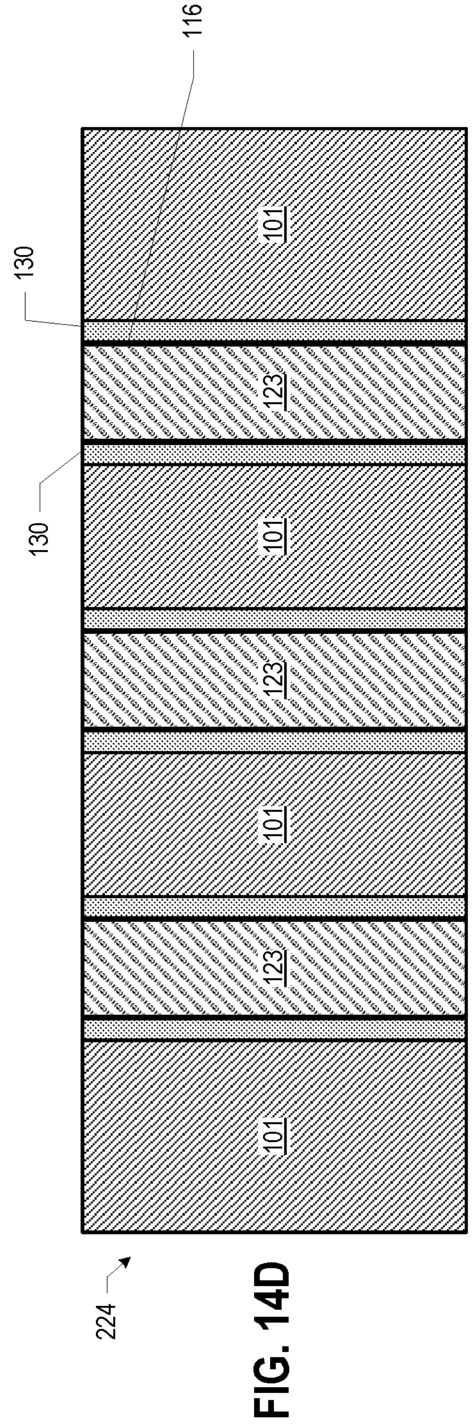


FIG. 14D

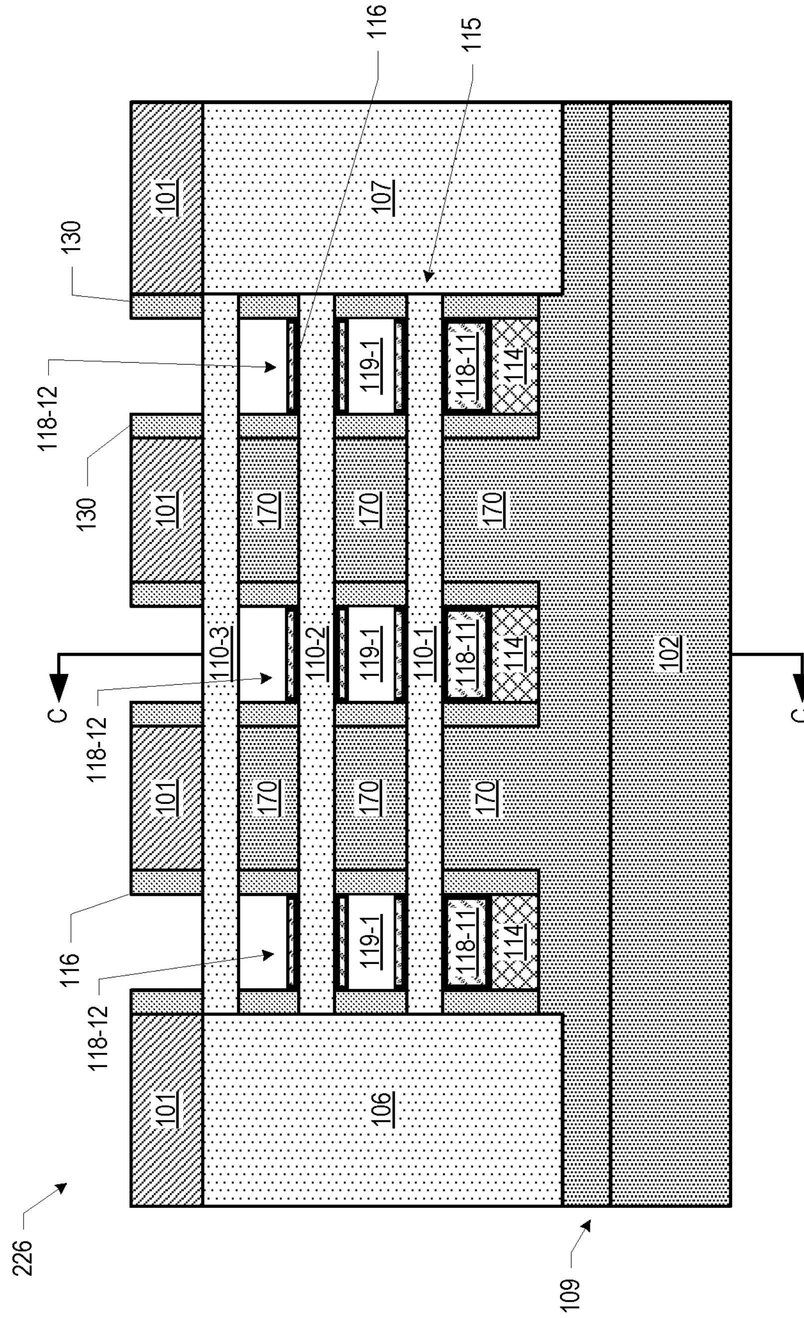


FIG. 15A

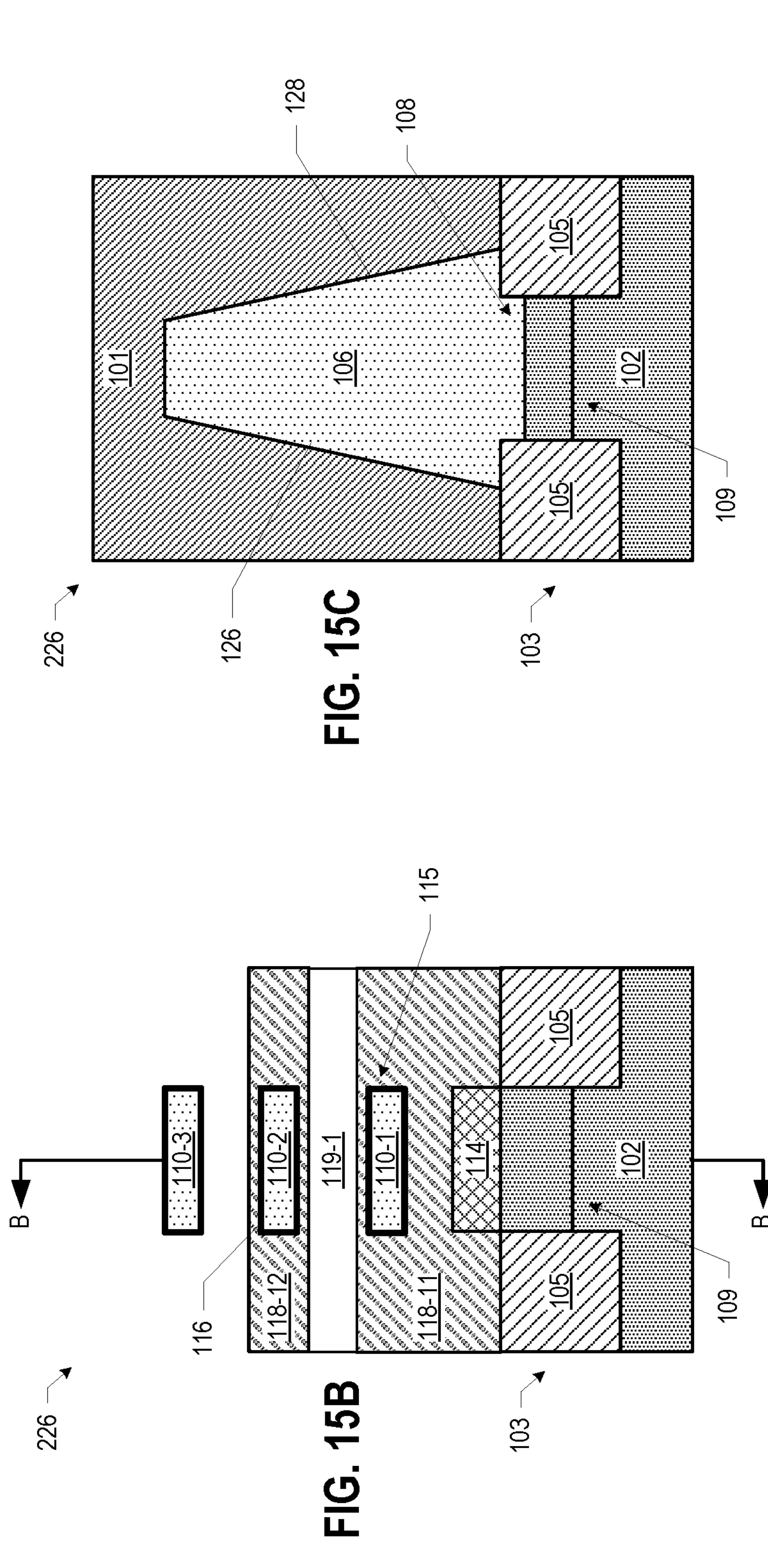


FIG. 15C

FIG. 15B

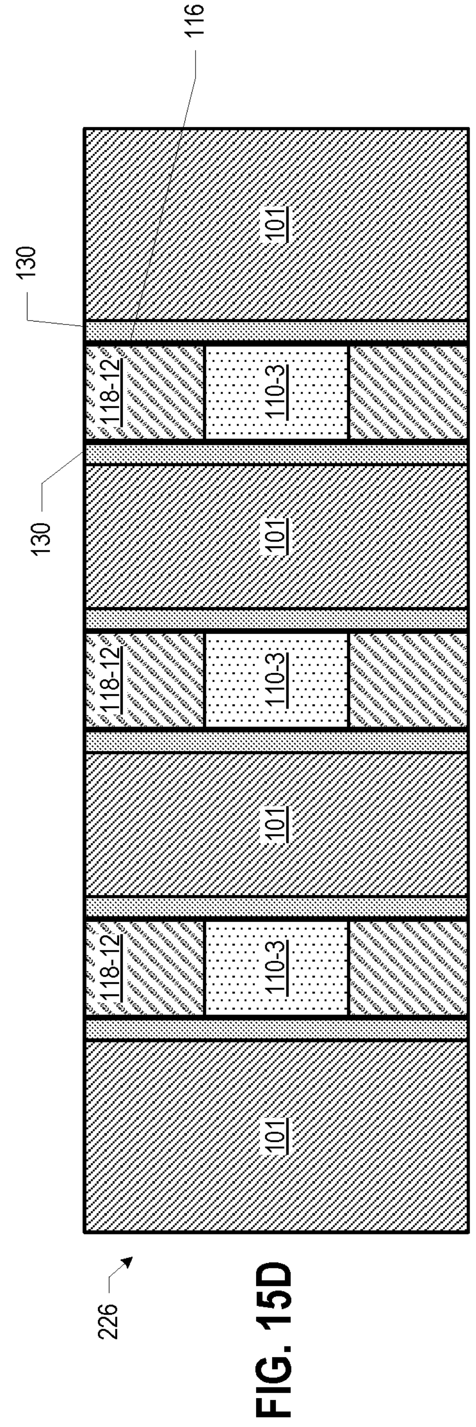
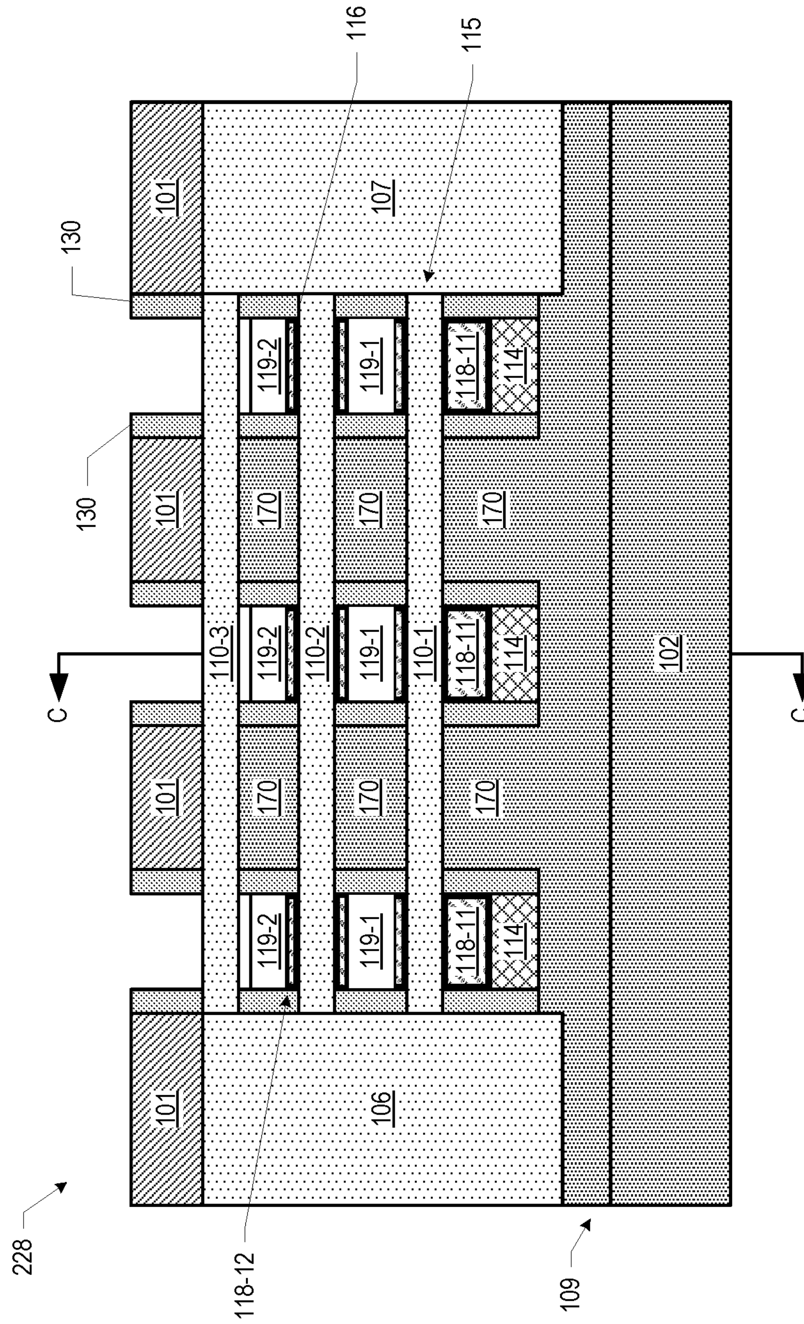


FIG. 15D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119-2
119-1
118-11
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170
C
110-3
110-2
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228
118-12
109
FIG. 16A

FIG. 16B

FIG. 16C

FIG. 16D

FIG. 17A

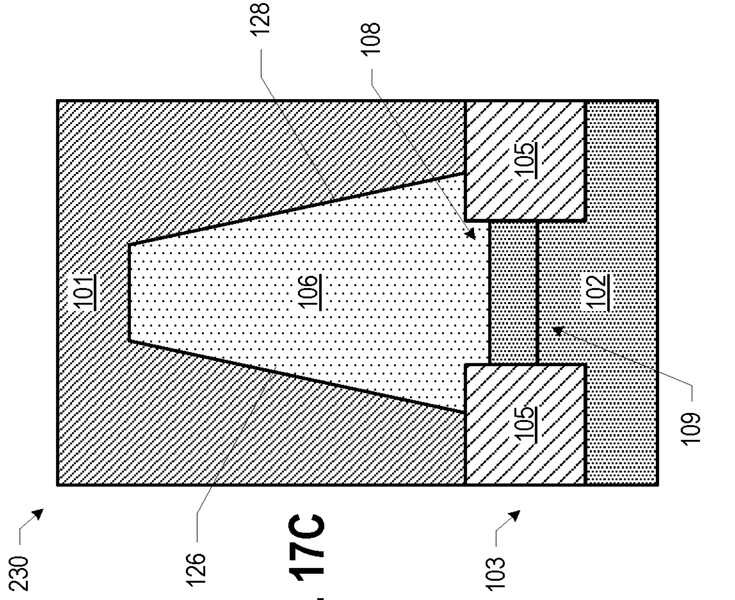


FIG. 17C

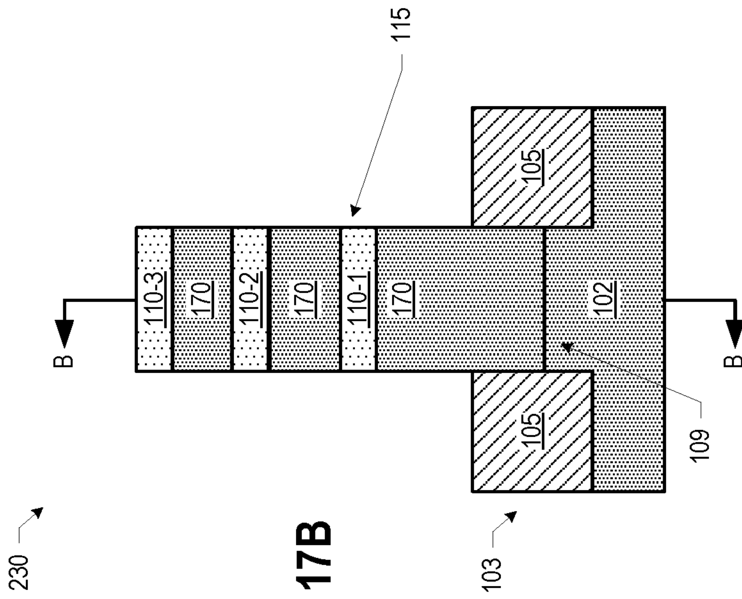


FIG. 17B

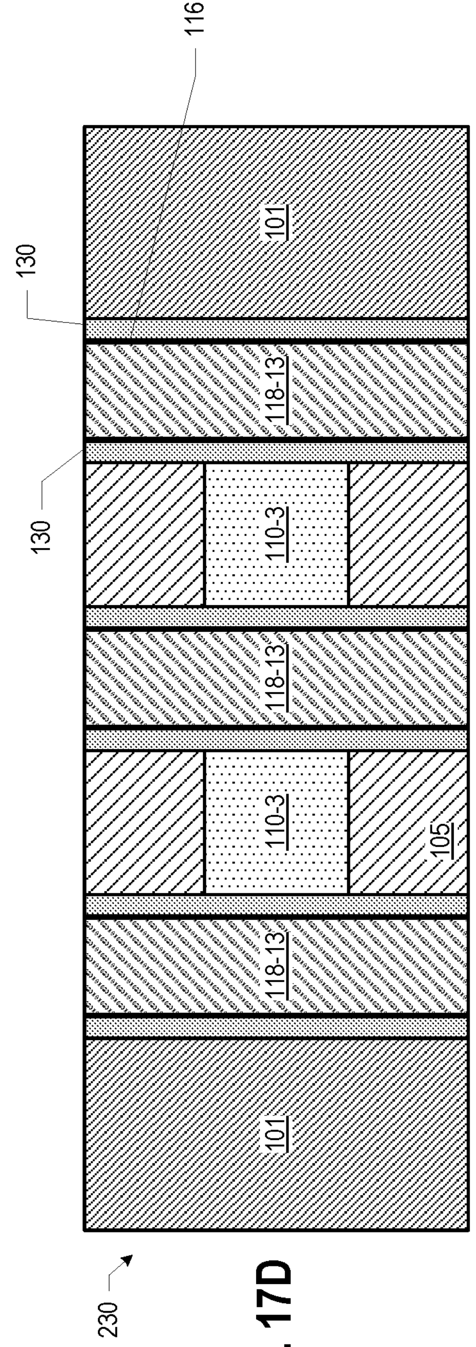
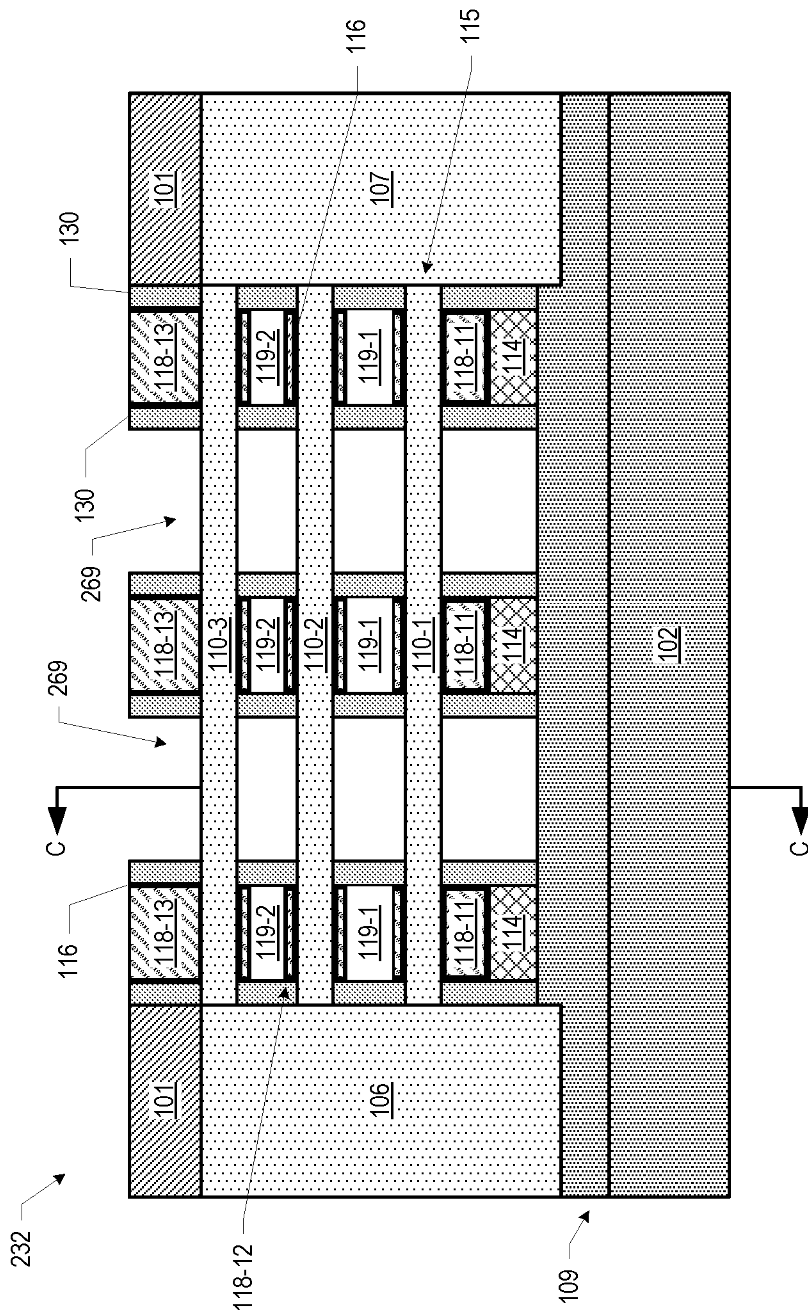


FIG. 17D


232
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C
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119-2
119-1
118-11
114
110-3
110-2
110-1
FIG. 18A

232
101
106
105
105
102
128
108
126
103
109

FIG. 18C

232
B
110-3
110-2
110-1
115
105
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102
109
103
B

FIG. 18B

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118-13
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118-13
110-3
105
118-13
101
232

FIG. 18D

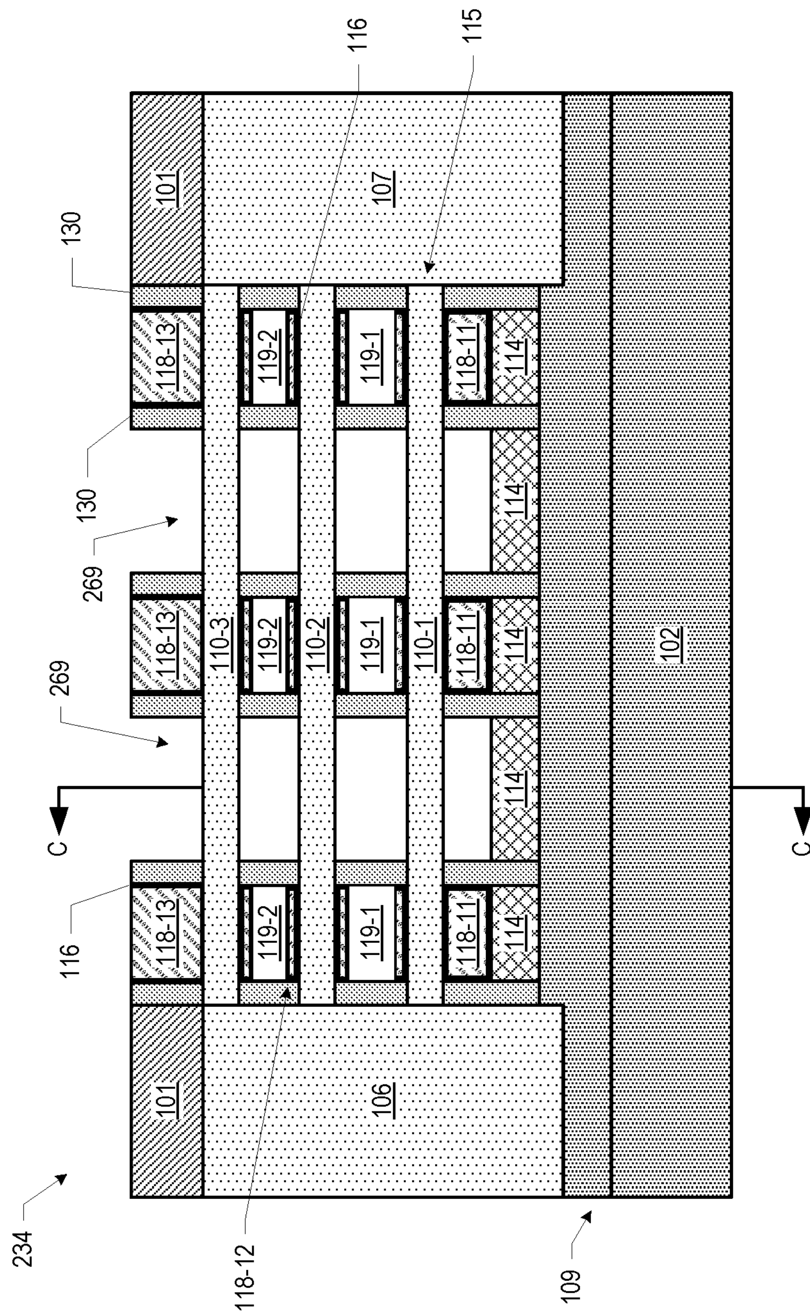

FIG. 19A

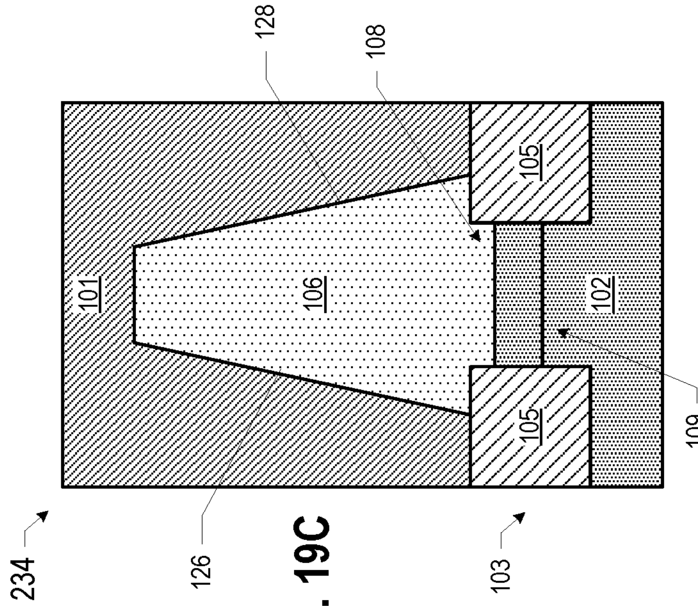

FIG. 19C

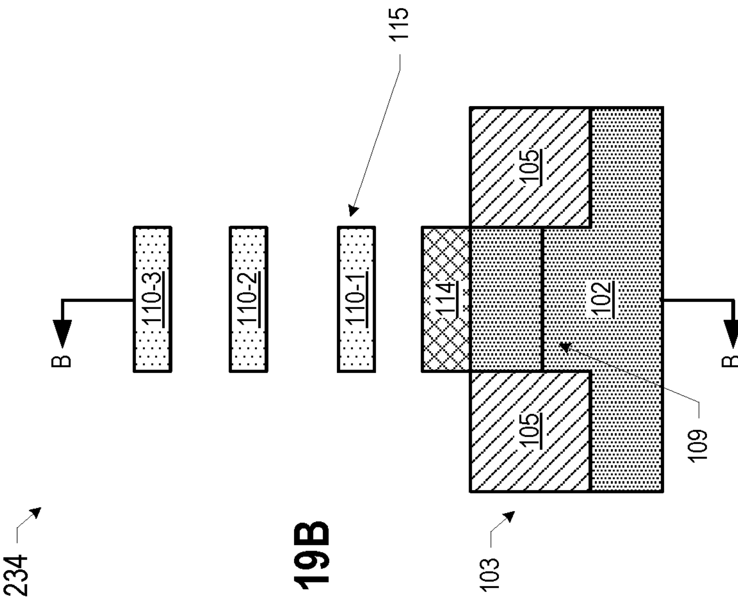

FIG. 19B

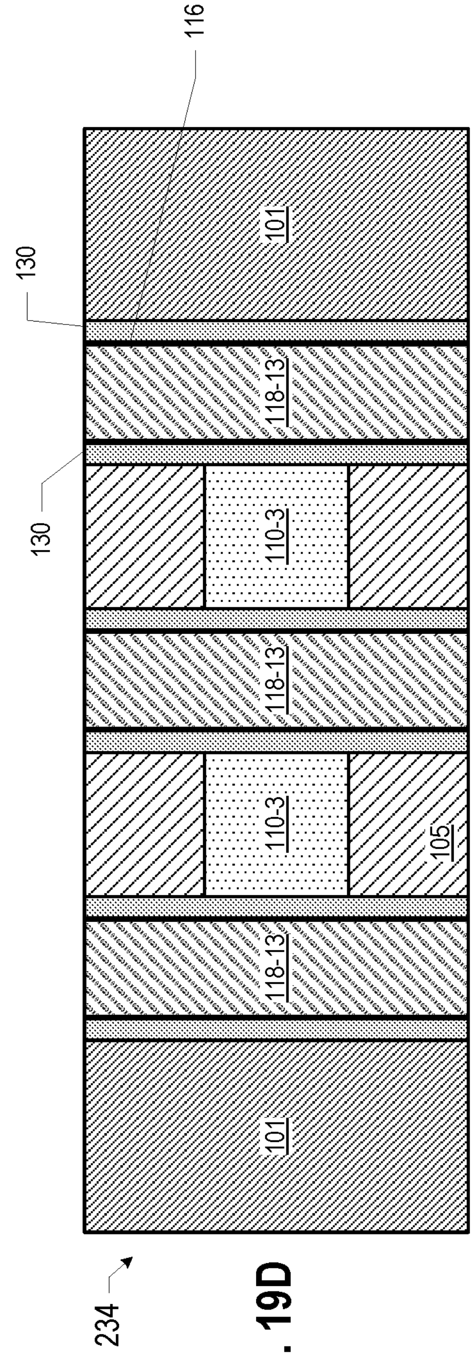

FIG. 19D

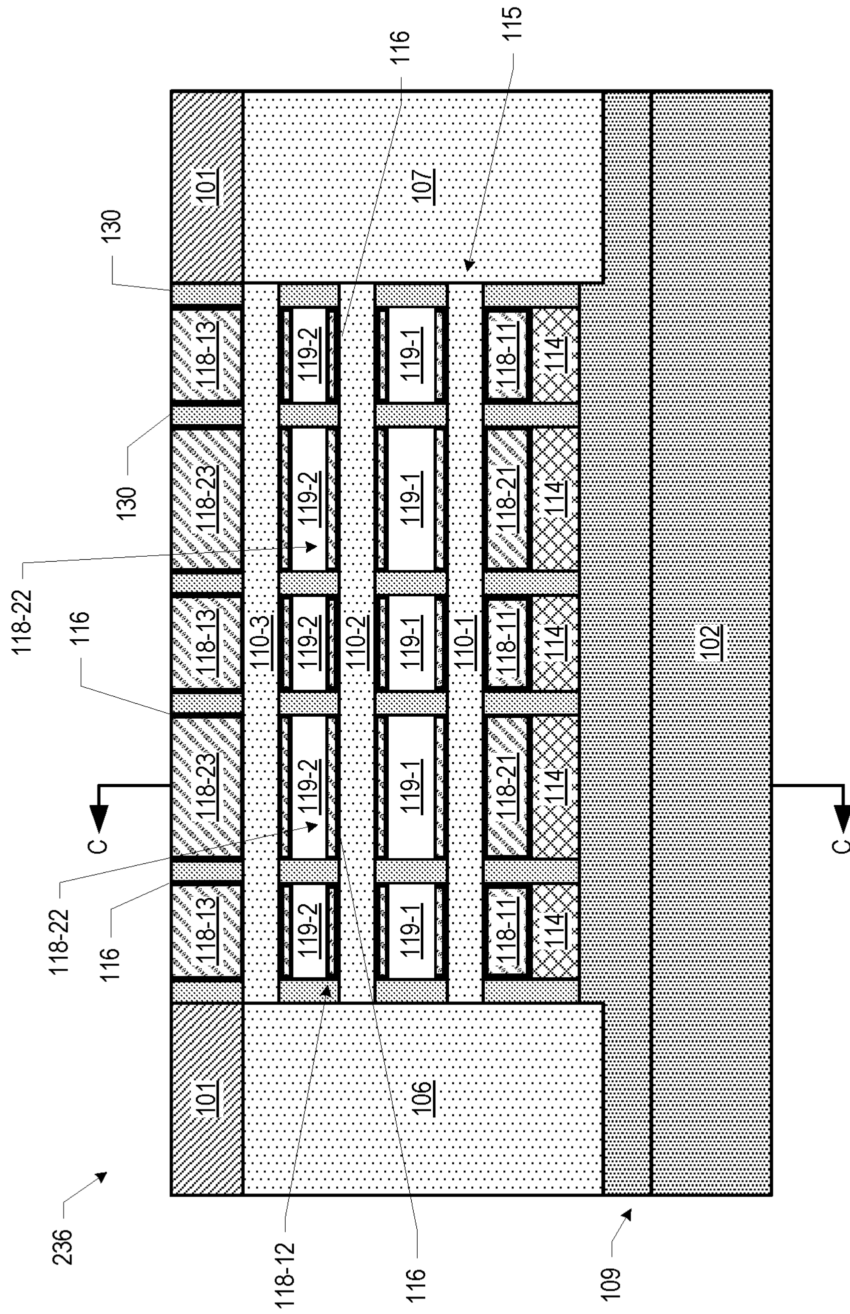

FIG. 20A

FIG. 20B

FIG. 20C

FIG. 20D

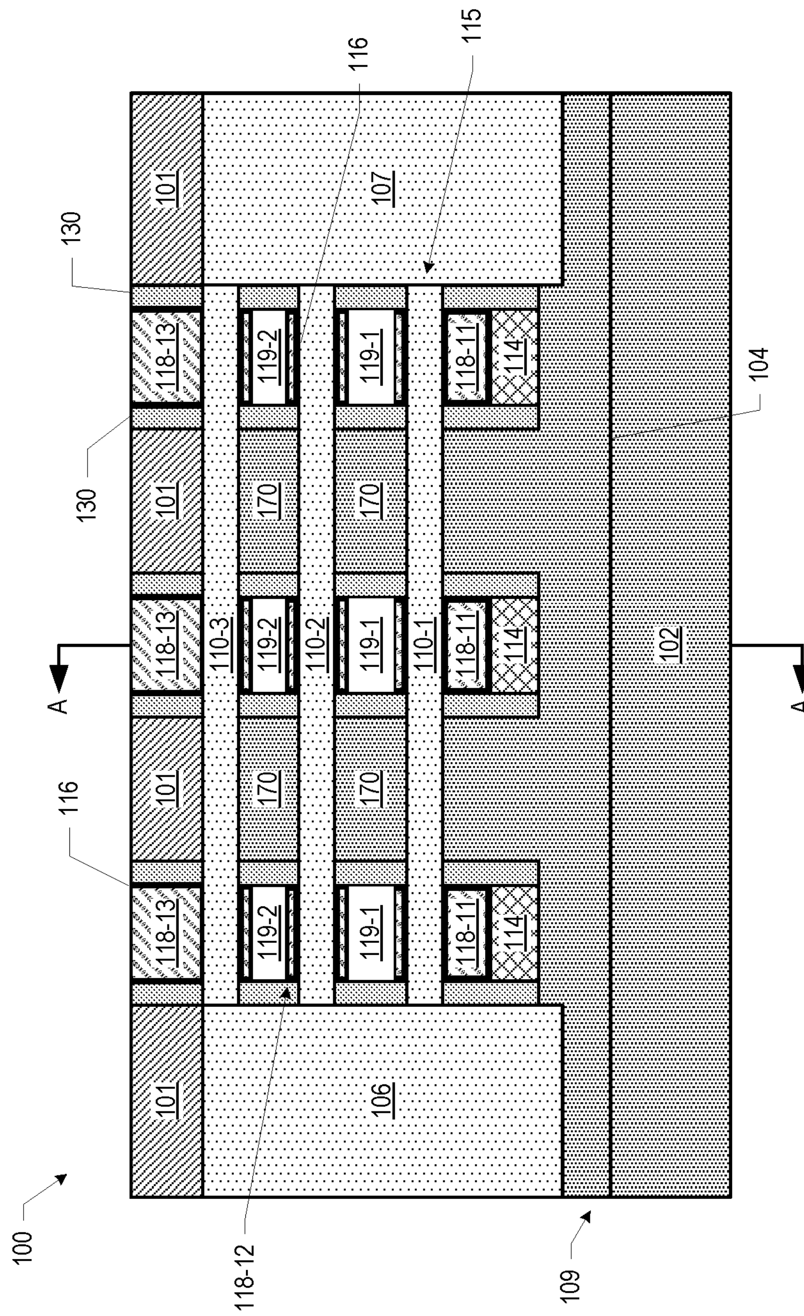

FIG. 21A

FIG. 21B

FIG. 21C

FIG. 21D

FIG. 21E

FIG. 21F

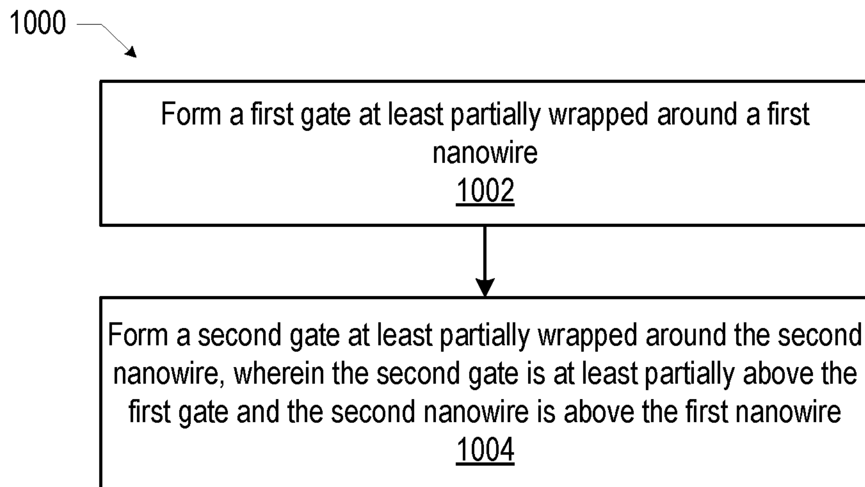

FIG. 22

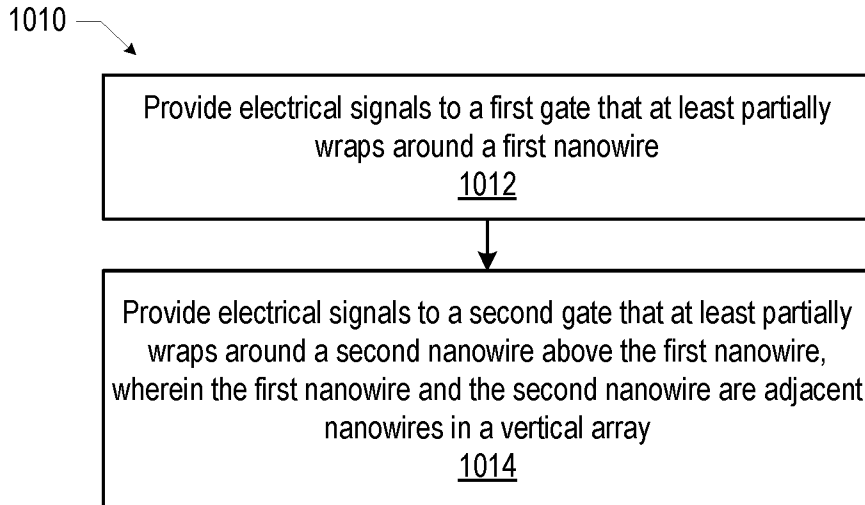

FIG. 23

FIG. 24

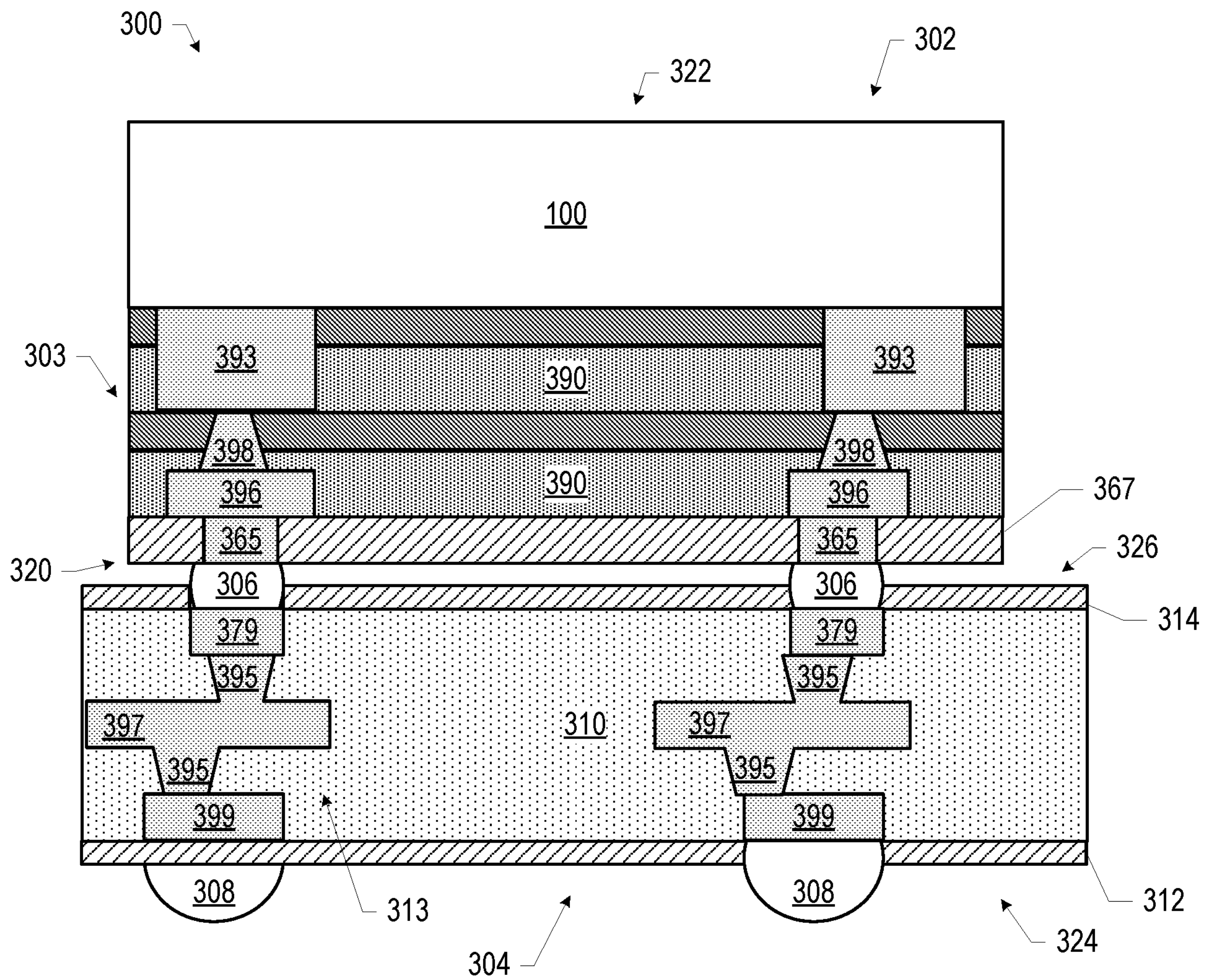

FIG. 25

450
SEE FIG. 26B
452

FIG. 26A

452

FIG. 26B

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FIG. 27

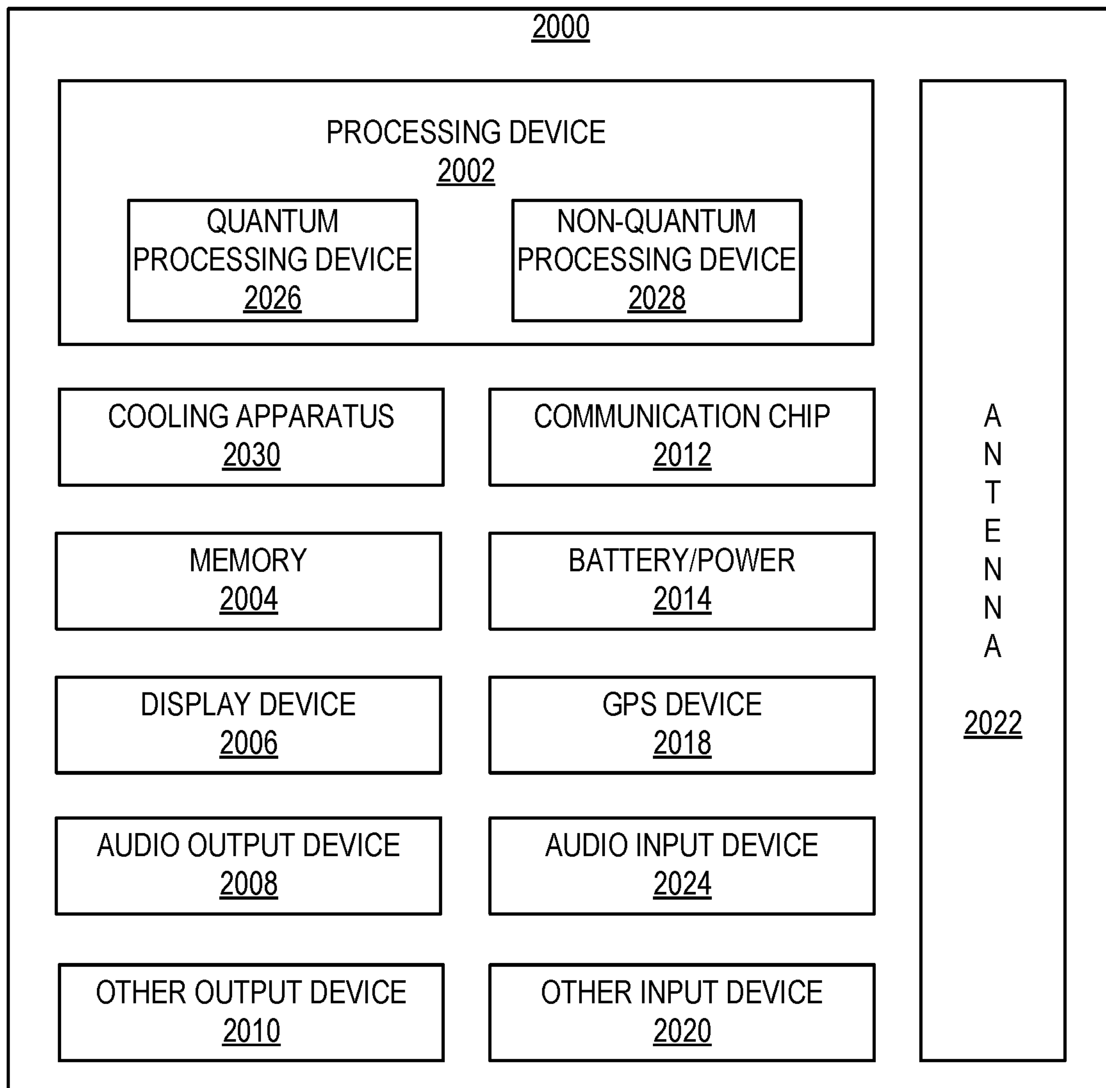

FIG. 28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/030295

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/06(2006.01)i, H01L 29/423(2006.01)i, H01L 27/088(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/06; H01L 39/02; H01L 29/49; H01L 21/336; G06N 99/00; H01L 29/12; H01L 29/786; H01L 29/74; H01L 21/8238; H01L 39/22; H01L 29/423; H01L 27/088

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: quantum, nanowire, surrounding, wrap, vertical, separate, dot, computing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008-0246021 A1 (SUNG-DAE SUK et al.) 09 October 2008 See paragraphs 11-99, claims 1-20 and figures 1A-4TT.	1-18
A		19-25
Y	US 2016-0300155 A1 (HITACHI, LTD.) 13 October 2016 See paragraphs 7-27, 74-274, claims 1-15 and figures 1-33.	1-18
A	US 2017-0047452 A1 (INTEL CORPORATION) 16 February 2017 See paragraphs 12-36 and figures 1-19.	1-25
A	US 2007-0262344 A1 (A.F.M. ANWAR et al.) 15 November 2007 See paragraphs 17-28 and figures 1-3e.	1-25
A	US 2013-0299783 A1 (MICROSOFT CORPORATION) 14 November 2013 See paragraphs 18-47 and figures 1-6.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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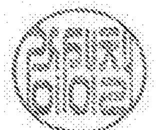

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/030295

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