

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
2 July 2009 (02.07.2009)

PCT

(10) International Publication Number
WO 2009/079752 A8

(51) International Patent Classification:
G1C 16/06 (2006.01)

(21) International Application Number:
PCT/CA2008/002180

(22) International Filing Date:
11 December 2008 (11.12.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/015,366 20 December 2007 (20.12.2007) US
12/258,056 24 October 2008 (24.10.2008) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: DUAL FUNCTION COMPATIBLE NON-VOLATILE MEMORY DEVICE

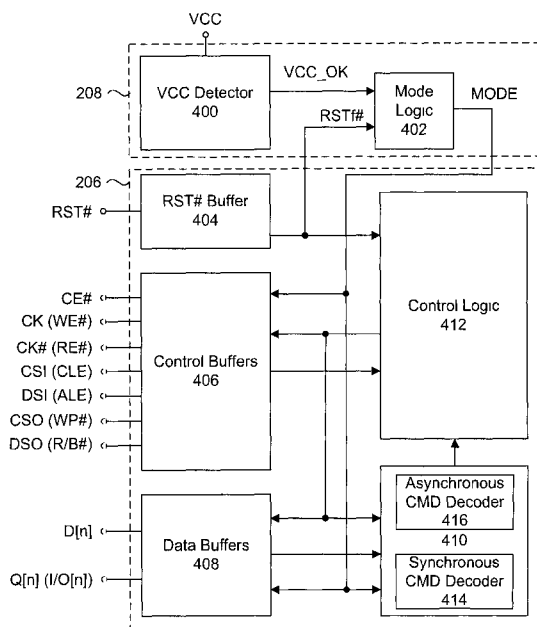


FIG. 7

(57) Abstract: A dual function memory device architecture compatible with asynchronous operation and synchronous serial operation. The dual function memory device architecture includes one set of physical ports having two different functional assignments. Coupled between the physical ports and core circuits of the memory device are asynchronous and synchronous input and output signal paths or circuits. The signal paths include shared or dedicated buffers coupled to the ports, asynchronous and synchronous command decoders, a network of switches, and a mode detector. The mode detector determines the operating mode of the dual function memory device from a port, and provides the appropriate switch selection signal. The network of switches routes the input or output signals through the asynchronous or synchronous circuits in response to the switch selection signal. The appropriate command decoder interprets the input signals and provides common control logic with the necessary signals for initiating the corresponding operation.



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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(U))*

Published:

— *with international search report (Art. 21(3))*

(48) Date of publication of this corrected version:

14 January 2010

(15) Information about Correction:

see Notice of 14 January 2010