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(54) **SWITCHED CAPACITOR CIRCUIT
CAPABLE OF MINIMIZING CLOCK
FEEDTHROUGH EFFECT IN A VOLTAGE
CONTROLLED OSCILLATOR CIRCUIT**

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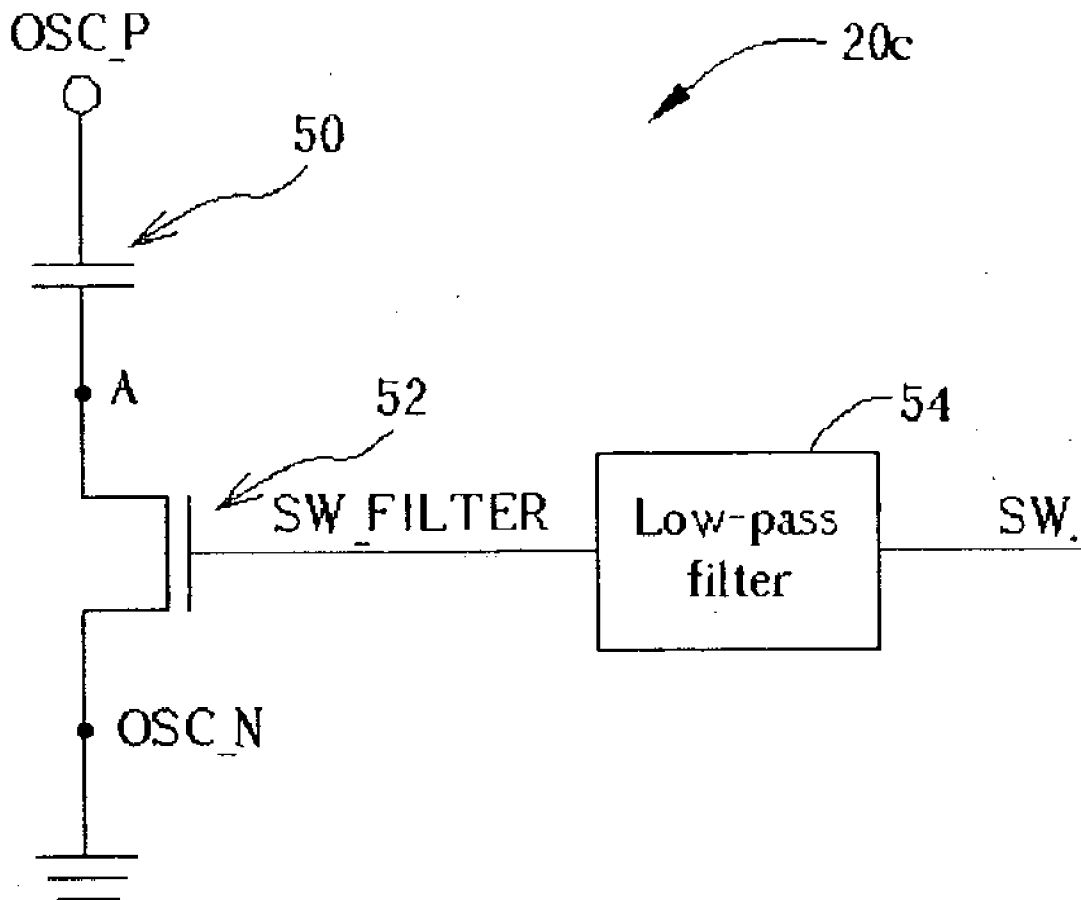
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G06G 7/19

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(57) **ABSTRACT**

A switched capacitor circuit for use in a voltage controlled oscillator (VCO) capable of minimizing clock feedthrough effect and an undesired momentary frequency drift in the VCO output frequency when the switched capacitor circuit is shut off. By gradually switching the switched capacitor circuit from an on state to an off state the clock feedthrough effect can be minimized. Several differently sized switch elements are used to selectively switch the capacitor from an internal capacitive node to ground. When switching the switched capacitor circuit to an off state, the control signals are sequenced to shut the switch elements off in order based on decreasing switch size. The smallest switch element can have a low-pass filter added to its control terminal to further decrease the clock feedthrough effect.



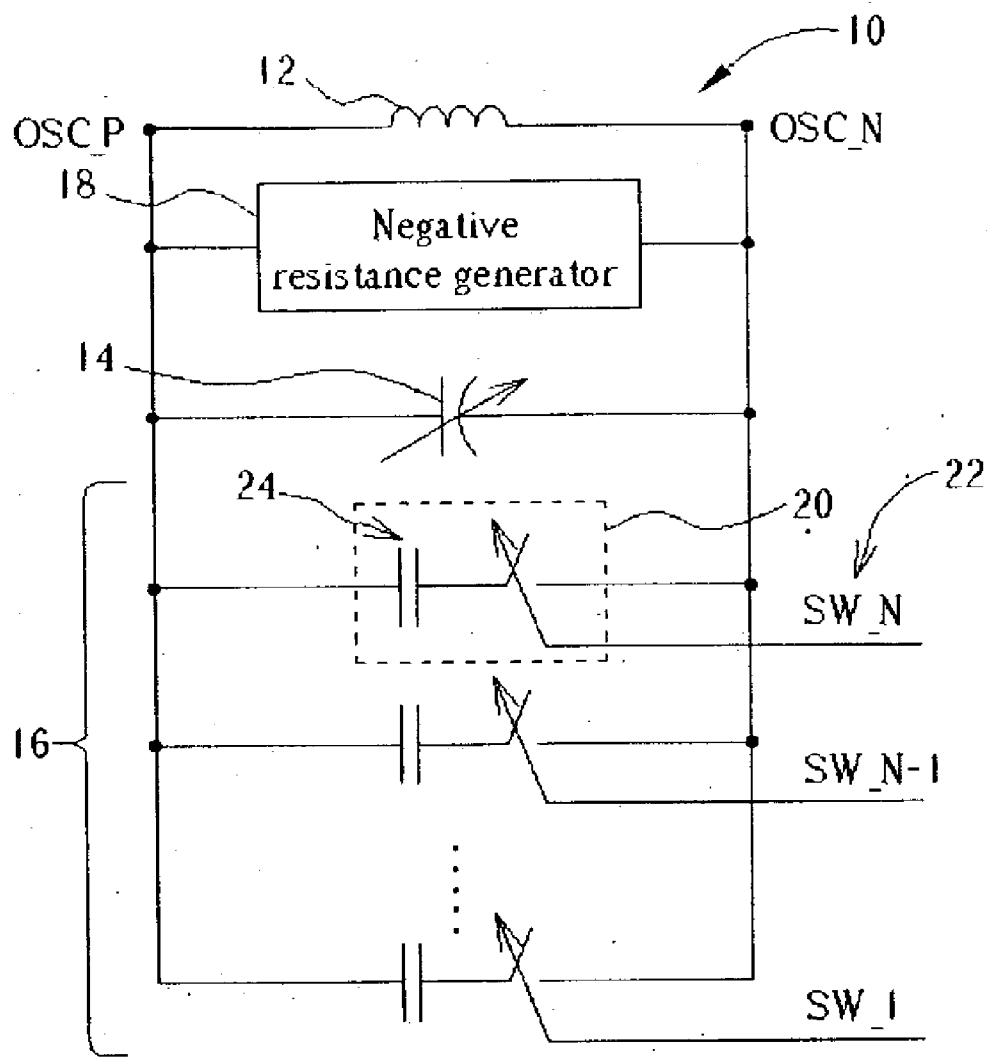


Fig. 1 Prior art

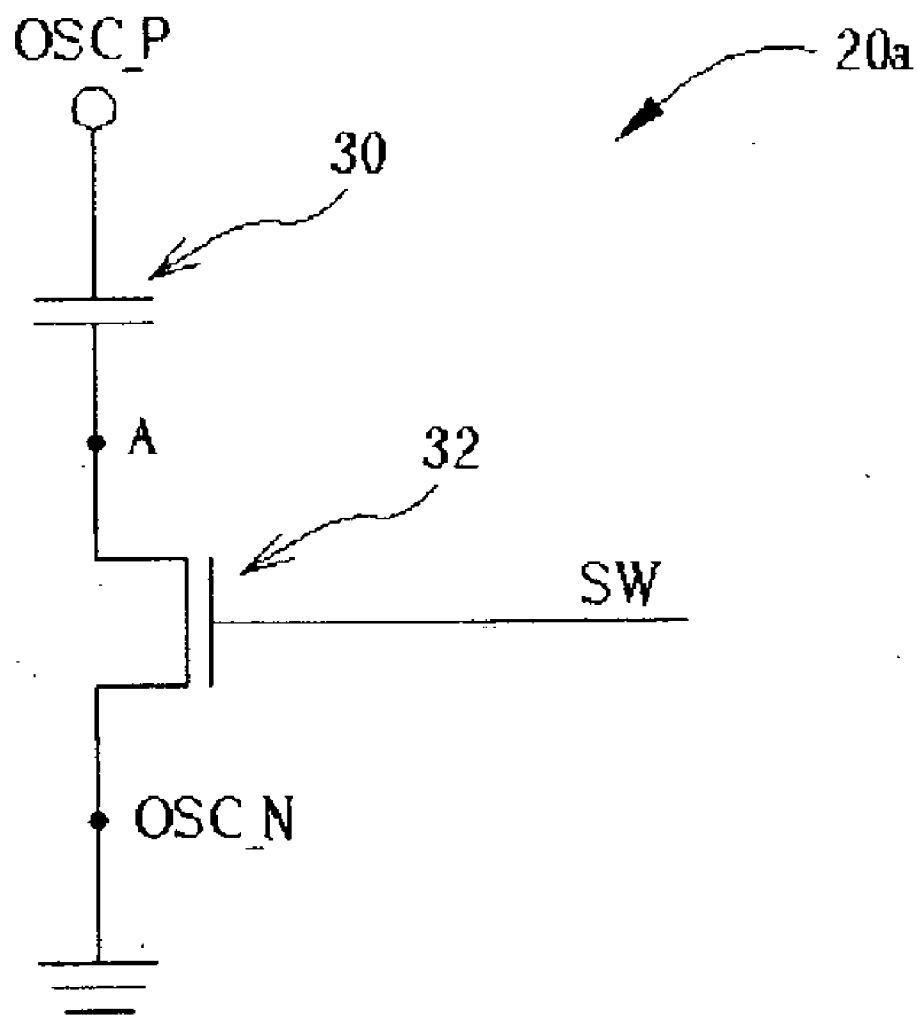


Fig. 2 Prior art

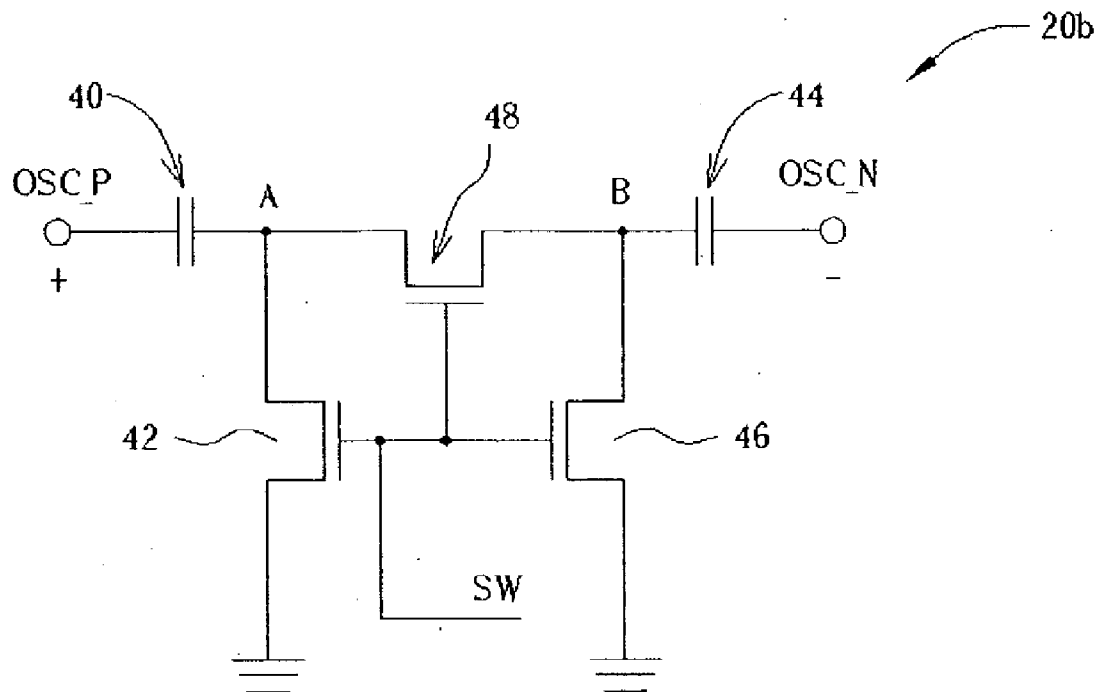


Fig. 3 Prior art

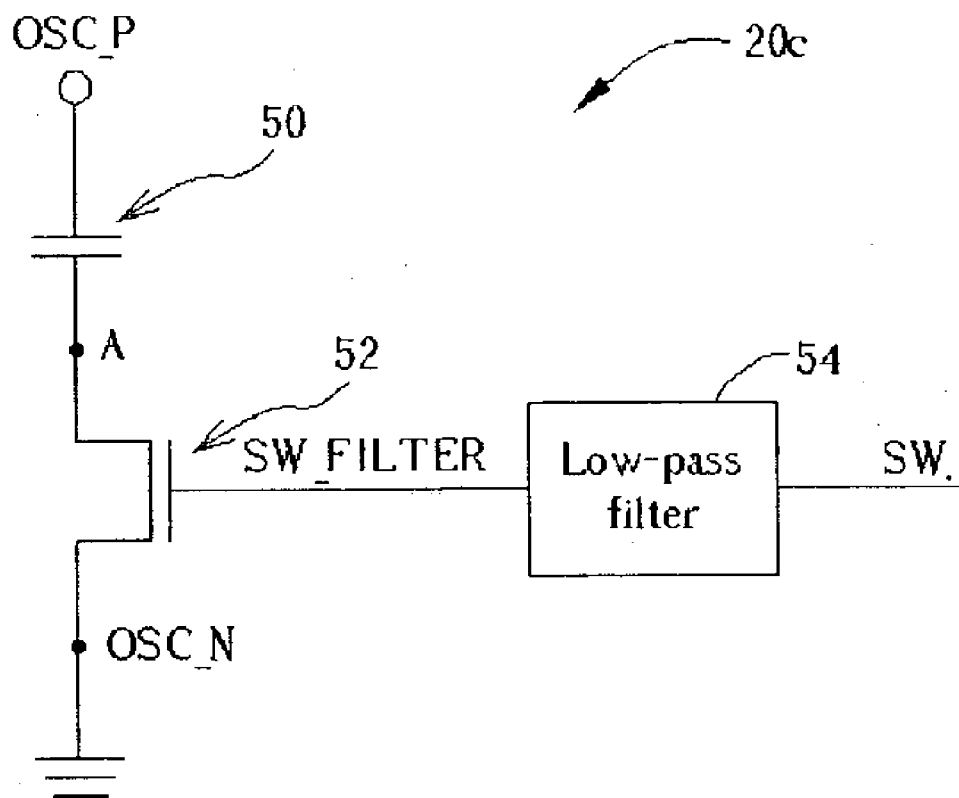


Fig. 4

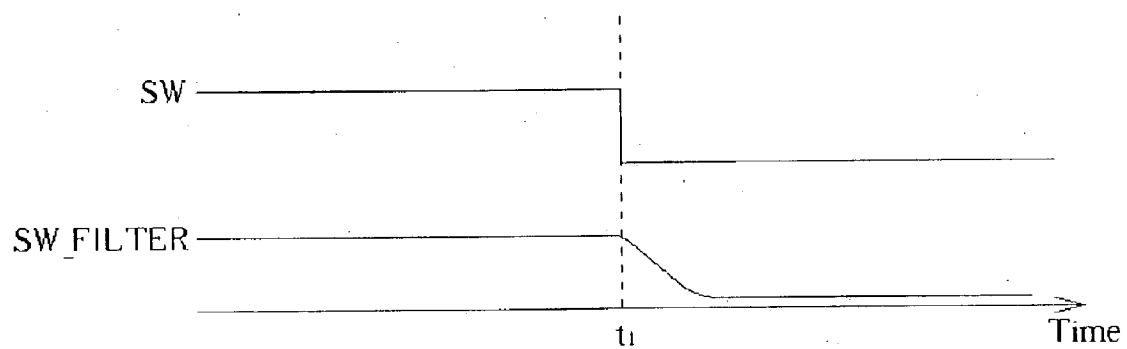


Fig. 5

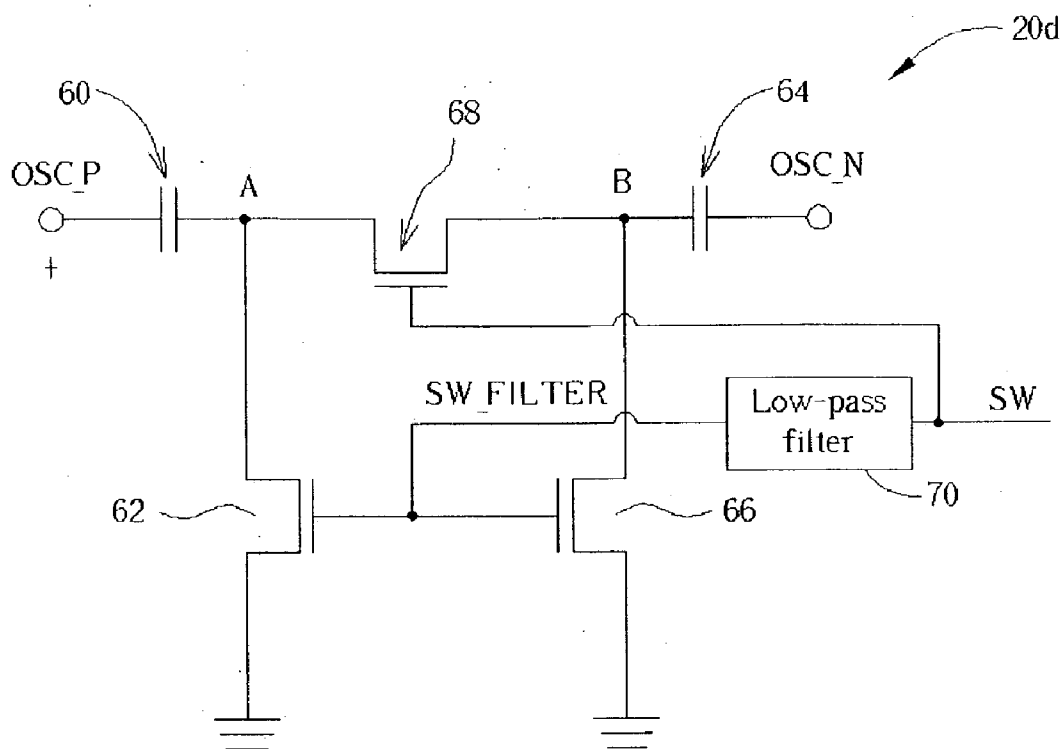


Fig. 6

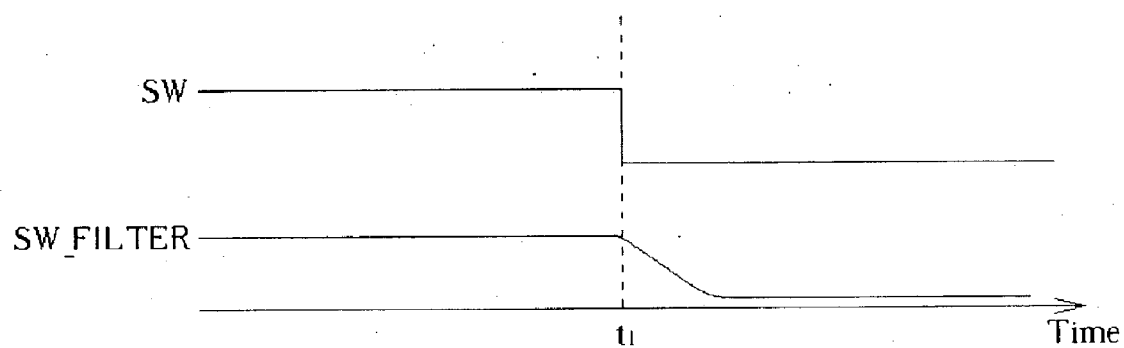


Fig. 7

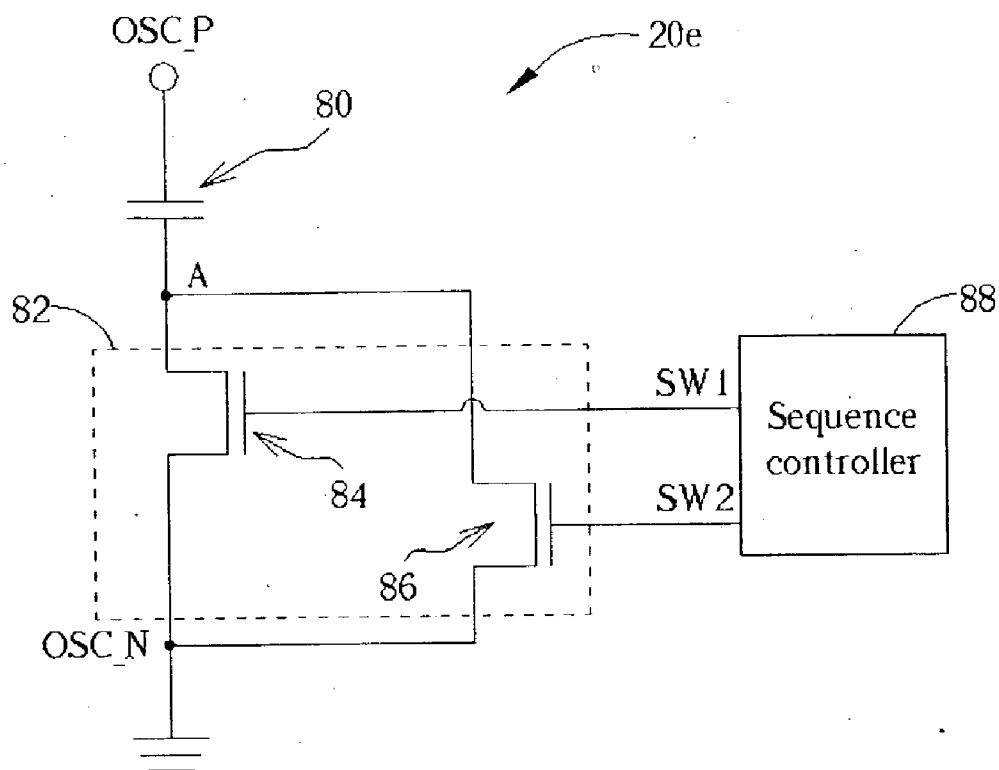


Fig. 8

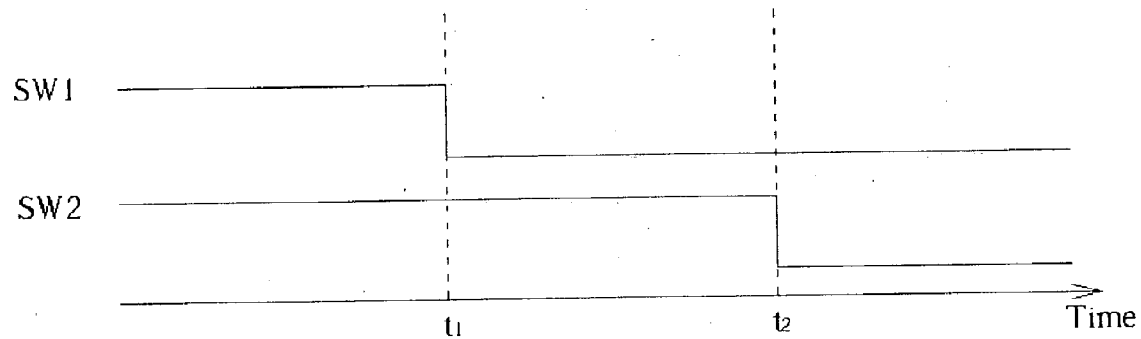


Fig. 9

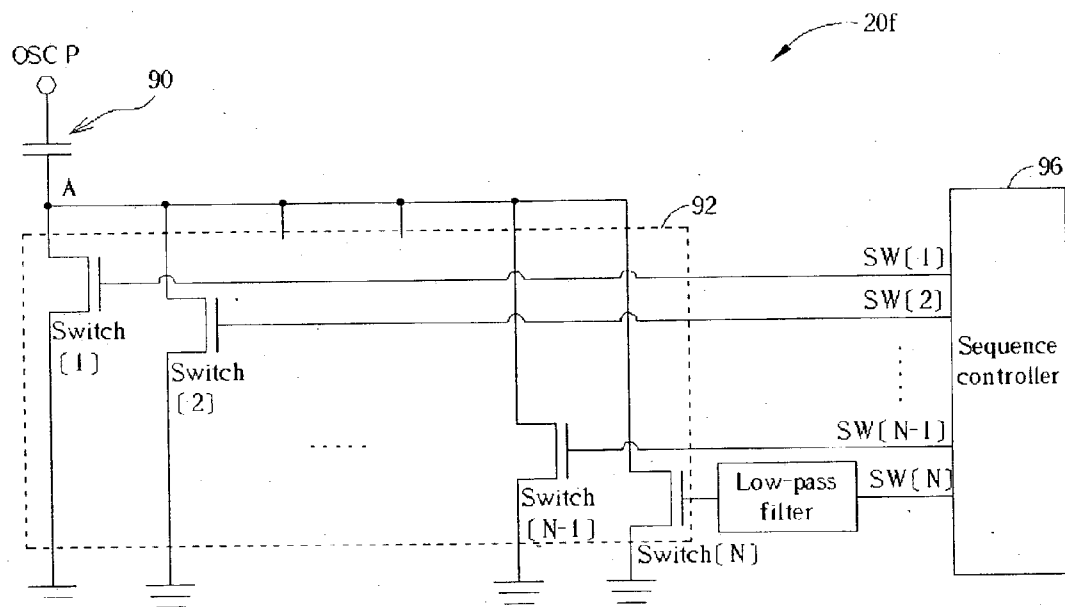


Fig. 10

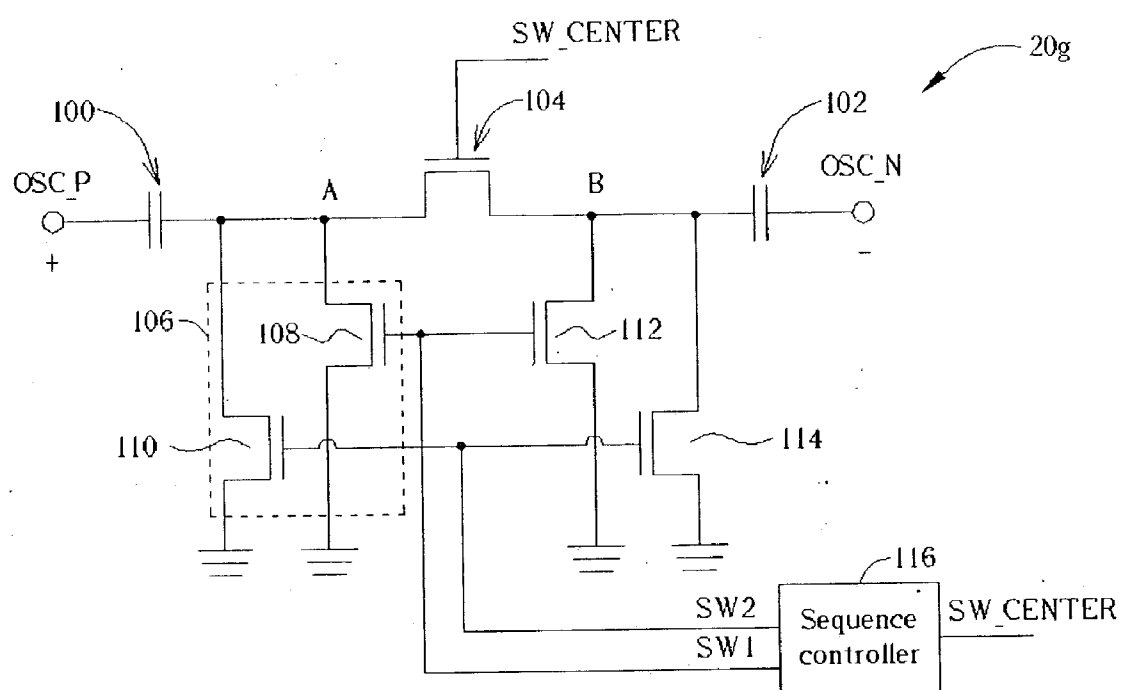


Fig. 11

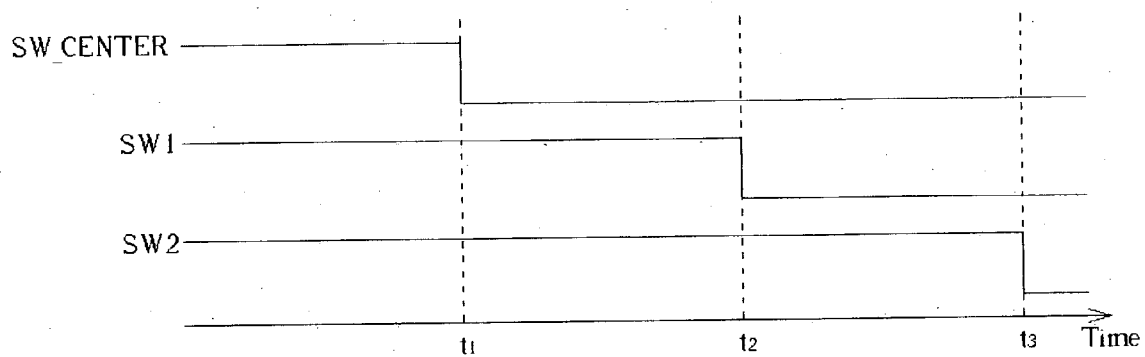


Fig. 12

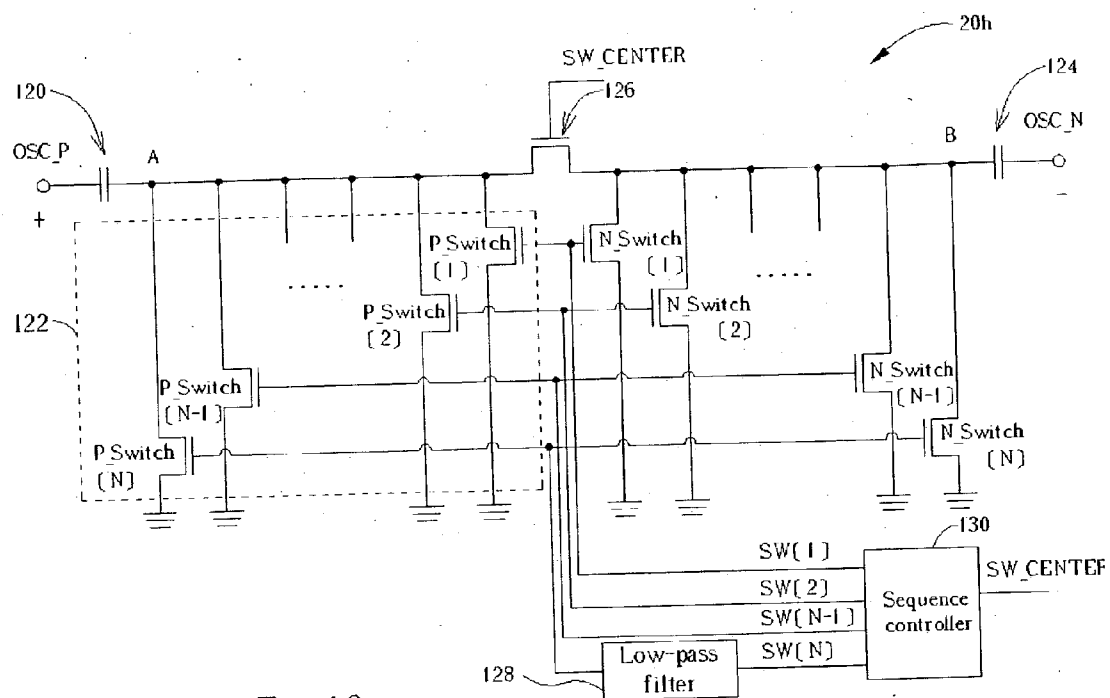


Fig. 13

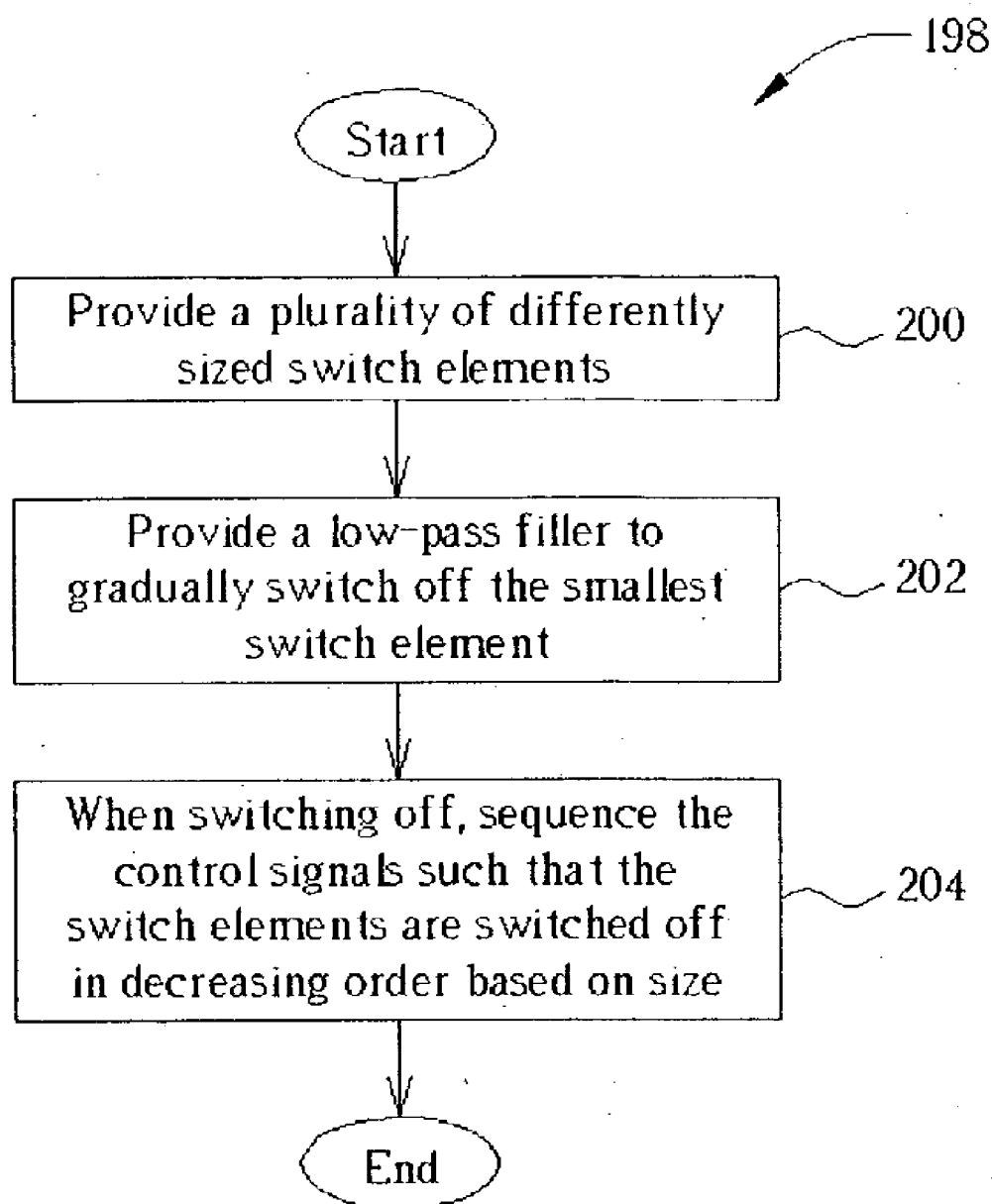


Fig. 14

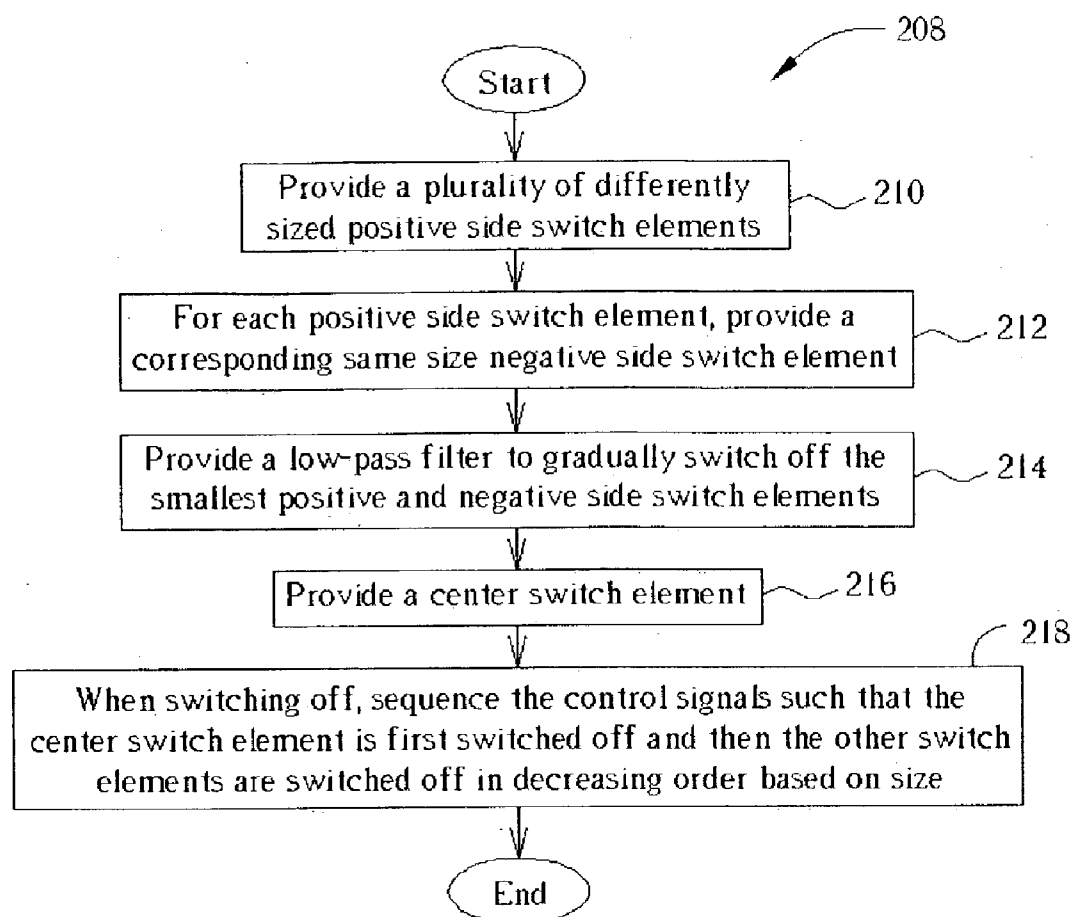


Fig. 15

SWITCHED CAPACITOR CIRCUIT CAPABLE OF MINIMIZING CLOCK FEEDTHROUGH EFFECT IN A VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Inventionbk2E001200303263

[0002] The present invention relates to a switched capacitor circuit, and more particularly, to a switched capacitor circuit used in a voltage controlled oscillator (VCO) that can minimize the clock feedthrough effect thereby preventing the VCO frequency drift phenomenon during calibration and the synthesizer phase locking period.

[0003] 2. Description of the Prior Art

[0004] A voltage controlled oscillator (VCO) is commonly used for frequency synthesis in wireless communication circuits. As Welland, et al. state in U.S. Pat. No. 6,226,506, wireless communication systems typically require frequency synthesis in both the receive path circuitry and the transmit path circuitry.

[0005] FIG. 1 shows a VCO circuit according to the prior art. An LC type VCO 10 used in a frequency synthesizer contains a resonator, the basic resonant structure includes an inductor 12 connected between a first oscillator node OSC_P and a second oscillator node OSC_N. Connected in parallel with the inductor 12 is a continuously variable capacitor 14 and a plurality of discretely variable capacitors 16. The continuously variable capacitor 14 is used for fine-tuning a desired capacitance while the plurality of discretely variable capacitors 16 is used for coarse tuning. The resistive loss of the parallel combination of inductor and capacitors is compensated by a negative resistance generator 18 to sustain the oscillation.

[0006] Each discretely variable capacitor in the plurality of discretely variable capacitors 16 is made up of a switched capacitor circuit 20 and each switched capacitor circuit is controlled by an independent control signal 22.

[0007] Based on this control signal 22 the switched capacitor circuit 20 can selectively connect or disconnect a capacitor 24 to the resonator of the VCO 10. Different on/off combinations of switched capacitor arrays results in a wider capacitance range of the LC type resonator and hence a wider VCO 10 oscillation frequency coverage.

[0008] FIG. 2 shows a switched capacitor circuit 20a according to the prior art. A capacitor 30 is connected between the first oscillator node OSC_P and a node A. A switch element 32 selectively connects node A to ground, and the switch element 32 is controlled by a control signal SW. When the switch element 32 is turned on, the capacitance associated with the capacitor 30 is added to the overall capacitance in the VCO 10 resonator. When the switch element 32 is turned off, the capacitance looking into the first oscillator node OSC_P is the series combination of the capacitor 30 and the off state capacitance associated with the switch element 32.

[0009] FIG. 3 shows a differential type switched capacitor circuit 20b according to the prior art. Differential implementations have much greater common-mode noise rejection and are widely used in high-speed integrated circuit environments. In the differential switched capacitor circuit 20b,

a positive side capacitor 40 is connected between the first oscillator node OSC_P and a node A. A positive side switch element 42 selectively connects node A to ground. A negative side capacitor 44 is connected between the second oscillator node OSC_N and a node B. A negative side switch element 46 selectively connects node B to ground. There is also a center switch element 48 used to lower the overall turn-on switch resistance connected between node A and node B. All three switch elements 42, 46, 48 are controlled by the same control signal SW. When the switch elements 42, 46, 48 are turned on, the capacitance associated with the series combination of the positive and negative side capacitors 40, 44 is added to the overall capacitance in the VCO 10. When the switch elements 42, 46, 48 are turned off, the differential input capacitance is the series combination of the positive and negative side capacitors 40, 44 and other switch parasitic capacitance. The overall input capacitance when all switch elements 42, 46, 48 are turned off is lower than that when all switch elements 42, 46, 48 are turned on. Without the center switch element 48, the switched capacitor circuit 20b is itself another embodiment of the differential type switch capacitor circuit according to the prior art.

[0010] Regardless of whether the single ended implementation shown in FIG. 2 or the differential implementation shown in FIG. 3 is used, when the switched capacitor circuit 20a or 20b is turned off, a momentary voltage step change occurs at node A (and in the case of the differential implementation shown in FIG. 3 also at node B). The momentary voltage step causes an undesired change in the overall capacitance, and ultimately, an undesired change in the VCO 10 frequency. This momentary voltage step change in FIG. 2 and FIG. 3, by using NMOS switches, is a voltage drop when the switch elements 32, 42, 46, 48 are turned off.

[0011] Using the single ended case shown in FIG. 2 as an example, when the switch element 32 is turned off, charge carriers are injected to the junction capacitance connected between the first terminal and the second terminal of the switch element 32. The injection produces an undesired voltage step change across the capacitive impedance and appears as a voltage drop at node A. This effect is known as clock feedthrough effect and appears as a feedthrough of the control signal SW from the control terminal of the switch element 32 to the first and second terminals of the switch element 32. When the switch element 32 is turned on, node A is connected to ground so the feedthrough of the control signal SW is of no consequence. However, when the switch element 32 is turned off, the feedthrough of the control signal SW causes a voltage step, in the form a voltage drop to appear at node A. Because of the dropped voltage at node A, the diode formed by the N³⁰ diffusion of switch element 32 and the P type substrate in the off state will be slightly forward biased. The voltage level at node A will spike low and then recover to ground potential as the forward biased junction diode formed by the switch element 32 in the off state allows current to flow. The voltage drop and recovery at node A changes the load capacitance of the VCO 10 resonator and causes an undesired momentarily drift in the VCO 10 frequency.

[0012] When the differential switched capacitor circuit 20b shown in FIG. 3 switches off, it suffers from the same clock feedthrough effect problem at node A and at node B. The positive side node A has an undesired voltage step change caused by the clock feedthrough effect of both the

positive side switch element **42** and the clock feedthrough effect of the center switch element **48**. Similarly, the negative side node B has an undesired voltage step caused by the clock feedthrough effect of both the negative side switch element **46** and the clock feedthrough effect of the center switch element **48**. The voltage step change and recovery at node A and node B changes the capacitance of the VCO **10** resonator and causes an undesired momentary drift in the VCO **10** frequency.

SUMMARY OF INVENTION

[0013] It is therefore a primary objective of the present invention to provide a switched capacitor circuit capable of minimizing the clock feedthrough effect, to solve the above-mentioned problem.

[0014] According to the present invention, a switched capacitor circuit capable of minimizing clock feedthrough effect. The switched capacitor circuit comprising a switch element having a first terminal connected to a capacitor, a second terminal connected to ground, and a control terminal; and a low-pass filter having an input terminal connected to a control signal and an output terminal connected to the control terminal of the switch element, wherein the low-pass filter is for making the switch element gradually switch off.

[0015] According to the present invention, a switched capacitor circuit capable of minimizing clock feedthrough effect, comprising a plurality of differently sized switch elements for selectively connecting a capacitor to a node depending upon a control signal applied to a control terminal of each of the switch elements. A sequence controller having a plurality of control signal outputs for switching off the switch elements in the plurality of differently sized pull down switch elements in sequence based on decreasing order of switch size. The switched capacitor circuit further comprising a means for making the smallest switch elements gradually switch off.

[0016] According to the present invention, a method for minimizing clock feedthrough effect when switching a switched capacitor circuit. The method comprises providing a plurality of differently sized switch elements that selectively connect a capacitor to a node depending upon a control signal applied to a control terminal of each of the switch elements. When switching the switched capacitor circuit to an off state, sequencing the control signals such that the switch elements are switched off in decreasing order based on size, whereby the largest switch element is switched off first and the smallest switch element is switched off last. The method further comprising when switching the switched capacitor circuit to an off state, providing a means for making the smallest switch element gradually switch off.

[0017] It is a further advantage of the present invention that the switched capacitor circuit is gradually switched off to minimize the clock feedthrough effect and prevent an undesired drift in the VCO **10** frequency. In the prior art, the switched capacitor circuit is instantly switched from an on state to an off state. The clock feedthrough effect in the prior art implementations causes an undesired voltage step change to slightly forward bias the junction diode formed by the switch element in the off state until the voltage potential has returned to ground.

[0018] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in

the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0019] FIG. 1 is a schematic diagram of a typical Voltage Controlled Oscillator (VCO) circuit used in a frequency synthesizer according to the prior art.

[0020] FIG. 2 shows a switched capacitor circuit used in the VCO of FIG. 1 according to the prior art.

[0021] FIG. 3 shows a differential type switched capacitor circuit used in the VCO of FIG. 1 according to the prior art.

[0022] FIG. 4 shows a switched capacitor circuit according to the first embodiment of the present invention.

[0023] FIG. 5 shows a time domain plot of the control signals for the switched capacitor circuit of FIG. 4

[0024] FIG. 6 shows a differential switched capacitor circuit according to the second embodiment of the present invention.

[0025] FIG. 7 shows a time domain plot of the control signals for the differential switched capacitor circuit of FIG. 6.

[0026] FIG. 8 shows an example switched capacitor circuit according to the third embodiment of the present invention.

[0027] FIG. 9 shows a time domain plot of the present invention control signals for switching off the switched capacitor circuit of FIG. 8

[0028] FIG. 10 shows a generalized switched capacitor circuit of FIG. 8 with a low-pass filter added to the control terminal of the smallest switch element.

[0029] FIG. 11 shows a differential switched capacitor circuit according to the fourth embodiment of the present invention.

[0030] FIG. 12 shows a time domain plot of the present invention control signals for switching off the differential switched capacitor circuit of FIG. 11.

[0031] FIG. 13 shows a generalized differential switched capacitor circuit of FIG. 11 with a low-pass filter added to the control terminal of the smallest pull down switch element at the positive side and its corresponding pull down switch element at the negative side.

[0032] FIG. 14 shows a method flowchart for minimizing clock feedthrough effect when switching off a switched capacitor circuit according to the present invention.

[0033] FIG. 15 shows a method flowchart for minimizing clock feedthrough effect when switching off a differential switched capacitor circuit according to the present invention.

DETAILED DESCRIPTION

[0034] FIG. 4 shows a switched capacitor circuit **20c** according to the first embodiment of the present invention. In the first embodiment, the switched capacitor circuit **20c** comprises a capacitor **50**, a switch element **52**, and a low-pass filter **54**. The capacitor **50** is connected between the

first oscillator node OSC_P and a node A. Depending on the control signal SW, the switch element 52 selectively connects the node A to ground. When the switch element 52 is turned on, the capacitance associated with the capacitor 50 is added to the overall capacitance in the VCO 10. When the switch element 52 is turned off, the capacitance looking into the first oscillator node OSC_P is the series combination of the capacitor 50 and the off state capacitance associated with the switch element 32. A low-pass filter 54 is connected to a control terminal of the switch element 52 for making the switch element 52 gradually switch off.

[0035] FIG. 5 is a time domain plot of the control signal SW before the low-pass filter 54 and a signal SW_FILTER after the low-pass filter 54. At time t_1 the control signal SW changes to a logic low. The low-pass filter 54 causes the signal SW_FILTER at the control terminal of the switch element 52 to gradually change from a logic high to a logic low and minimizes the voltage step change seen at node A. Because the switch element 52 is gradually switched off, node A is gradually disconnected from ground. As the switch element 52 is gradually switched off, during a period of delay time there exists a conduction path of the switch element, even with an increasing resistance, to ground to minimize the clock feedthrough effect. In contrast to the prior art, the present invention does not forward bias the diode formed by the switch element 52 in the off state. The clock feedthrough effect at each moment in time is reduced.

[0036] FIG. 6 shows a differential switched capacitor circuit 20d according to the second embodiment of the present invention. A positive side capacitor 60 is connected between the first oscillator node OSC_P and a node A. A positive side switch element 62 selectively connects node A to ground. A negative side capacitor 64 is connected between the second oscillator node OSC_N and a node B. A negative side switch element 66 selectively connects node B to ground. A center switch element 68 is used to lower the overall turn-on resistance and is connected between node A and node B. A low-pass filter 70 is connected to the control terminals of the positive side switch element 62 and the negative side switch element 66 for making the positive and negative side switch elements 62, 66 gradually switch off. Without the center switch element 68, the switched capacitor circuit 20d is itself another embodiment of the differential type switched capacitor circuit.

[0037] FIG. 7 is a time domain plot of the control signal SW before the low-pass filter and the signal SW_FILTER after the low-pass filter. The center switch element 68 is directly controlled by the control signal SW while the positive and negative side switch elements 62, 66 are controlled by the output of the low-pass filter 70, signal SW_FILTER. At time t_1 the control signal SW changes from a logic high to a logic low and the center switch element 68 immediately changes to an off state. Because the positive and negative side switch elements 62, 66 gradually switch off, during a period of delay time, node A and node B are still connected to ground and the clock feedthrough effect due to the center switch element 68 is minimized by the conduction to ground path. As in the single ended embodiment of FIG. 4, as the positive and negative side switch elements 62, 66 gradually switch off, the clock feedthrough effect produced at node A and B at each moment of time is reduced.

[0038] FIG. 8 shows an example of the switched capacitor circuit 20e according to the third embodiment of the present

invention. In the third embodiment, the switched capacitor circuit 20e comprises a capacitor 80, a sequence controller 88, and a plurality of differently sized switch elements 82. FIG. 8 shows two switch elements 84, 86 but this is meant as an example only and more switch elements could be used. In this example, switch element 84 is larger than switch element 86. The capacitor 80 is connected between the first oscillator node OSC_P and a node A. Each of the switch elements 84, 86 in the plurality of differently sized switch elements 82 selectively connects node A to ground, and each switch element 84, 86 in the plurality of differently sized switch elements 82 has its own control signal. In this example the larger switch element 84 has a control signal SW1 and the smaller switch element 86 has a control signal SW2.

[0039] FIG. 9 shows a time domain plot of the control signals of the present invention method for switching off the switched capacitor circuit 20e as shown in FIG. 8. In order to gradually switch the switched capacitor circuit 20e to an off state, the sequence controller 88 ensures that the switch elements 84, 86 are switched off in decreasing order based on switch size. Because switch element 84 is larger than switch element 86, switch element 84 is first switched off at time t_1 . At time t_2 , which is after t_1 , switch element 86 is switched off. Since the amount of voltage change at node A due to the clock feedthrough effect depends on the parasitic capacitance ratio of control terminal to first terminal and first terminal to second terminal capacitance, the smaller the control terminal to first terminal capacitance the smaller the voltage change due to the feedthrough of the control signal switching from high to low. The present invention takes advantage of this fact because the larger switch elements with larger voltage drops due to turning off the larger switch elements are switched off first. Until the last switch element is switched off, node A is connected to ground and clock feedthrough effect is not a concern. If the last switch element to be switched off is made sufficiently small, the clock feedthrough effect after the last switch is switched off can be made negligible.

[0040] FIG. 10 shows a generalized third embodiment switched capacitor circuit 20f schematic. A capacitor 90 is connected between the first oscillator node OSC_P and a node A. A plurality of differently sized switch elements 92 selectively connects node A to ground, and each switch element in the plurality of differently sized switch elements 92 has its own control signal. A largest switch element Switch[1] has a control signal SW[1] and a size of W[1]. A smaller switch element Switch[2] has a control signal SW[2] and a size of W[2], where W[2] is smaller than W[1]. A second smallest switch element Switch[N-1] has a control signal SW[N-1] and a size of W[N-1], where W[N-1] is smaller than W[N-2]. A smallest switch element Switch[N] has a control signal SW[N] and a size of W[N], where W[N] is smaller than W[N-1]. A sequence controller 96 provides the control signals SW[1] to SW[N] and ensures that the switch elements are switched off in decreasing order based on switch size. As shown in FIG. 10, a low-pass filter 94 can be added, or not added, to the control terminal of the smallest switch element Switch[N]. Similar to the circuit shown in FIG. 4, the low-pass filter 94 will gradually shut off the last switch element Switch[N] minimizing the clock feedthrough effect of the switched capacitor circuit 20f.

[0041] FIG. 11 shows an example of the differential switched capacitor circuit 20g according to the fourth embodiment of the present invention. The differential switched capacitor circuit 20g comprises a positive side capacitor 100, a negative side capacitor 102, a center switch element 104, a sequence controller 116, a plurality of differently sized positive side switch elements 106, and for each switch element in the plurality of the differently sized positive side switch elements 106, a corresponding negative side switch element having substantially the same size as the positive side switch element. FIG. 11 shows two positive side switch elements 108, 110 and two corresponding negative side switch elements 112, 114 but this is meant as an example only and more switch elements could be used. In this example, switch elements 108 and 112 are of substantially the same size and are larger than switch elements 110 and 114, which are also of substantially the same size. The positive side capacitor 100 is connected between the first oscillator node OSC_P and a node A. Each of the switch elements 108, 110 in the plurality of differently sized positive side switch elements 106 selectively connects node A to ground and each switch element in the plurality of differently sized positive side switch elements 106 has its own control signal. The negative side capacitor 102 is connected between the second oscillator node OSC_N and a node B. Node B is selectively connected to ground by each of the corresponding negative side switch elements 112, 114 depending on the control signal of the positive side switch element 108, 110 respectively. In this example, the larger switch elements 108, 112 have a control signal SW1 and the smaller switch elements 110, 114 have a control signal SW2. Without the center switch element 104, the switched capacitor circuit 20g is itself another embodiment of the differential type switched capacitor circuit.

[0042] FIG. 12 shows a time domain plot of the control signals of the present invention method for switching off the forth embodiment of the switched capacitor circuit 20g as shown in FIG. 11. In order to gradually switch the switched capacitor circuit 20g to an off state, the sequence controller 116 ensures that the center switch element 104 is first switched off (at time t_1) and then the remaining switch elements are switched off in pairs in decreasing order based on switch size. At t_2 , which is after t_1 , switch elements 108 and 112 are switched off. At t_3 , which is after t_2 , switch elements 110 and 114 are switched off. Because the positive side switch element 108 and its corresponding negative side switch element 112 are larger in size than the positive side switch element 110 and its corresponding negative side switch element 114, the positive side switch element 108 and the negative side switch element 112 are switched off next. Until the last positive and negative side switch elements 110, 114 are switched off, node A and node B are connected to ground and clock feedthrough effect is not a concern. If the last switch element pair to be switched off is made sufficiently small, the clock feedthrough effect of the differential switch circuit 20g can be made negligible.

[0043] FIG. 13 shows a generalized fourth embodiment differential switched capacitor circuit 20h. A positive side capacitor 120 is connected between the first oscillator node OSC_P and a node A. A plurality of differently sized positive side switch elements 122 selectively connects node A to ground and each switch element in the plurality of differently sized positive side switch elements 122 has its own control signal. A largest positive side switch element

P_Switch[1] has a control signal SW[1] and a size of W[1]. A smaller positive side switch element P_Switch[2] has a control signal SW[2] and a size of W[2], where W[2] is smaller than W[1]. A second smallest positive side switch element P_Switch[N-1] has a control signal SW[N-1] and a size of W[N-1], where W[N-1] is smaller than W[N-2]. A smallest positive side switch element P_Switch[N] has a control signal SW[N] and a size of W[N], where W[N] is smaller than W[N-1]. For each switch element in the plurality of the differently sized positive side switch elements 122, a corresponding negative side switch element having substantially the same size as the positive side switch element selectively connects a node B to ground depending on the same control signal as the positive side switch element. A largest negative side switch element N_Switch[1] has the control signal SW[1] and the size of W[1]. A smaller negative side switch element N_Switch[2] has the control signal SW[2] and the size of W[2]. A second smallest negative side switch element N_Switch[N-1] has the control signal SW[N-1] and the size of W[N-1]. A smallest negative side switch element N_Switch[N] has the control signal SW[N] and a size of W[N]. A negative side capacitor 124 is connected between node B and the second oscillator node OSC_N. A center switch element 126 selectively connects node A to node B depending on a control signal SW_CENTER. A low-pass filter 128 can be connected, or not connected, to the control terminals for the smallest switch element pair. Similar to the circuit in FIG. 6, the low-pass filter 128 will gradually shut off the last switch element pair P_Switch[N], N_Switch[N] minimizing the clock feedthrough effect of the differential switched capacitor circuit 20h. A sequence controller 130 provides the control signals SW_CENTER and SW[1] to SW[N] and ensures that the center switch element is first switched off and then the remaining switch elements are switched off in pairs in decreasing order based on switch size. Without the center switch element 126, the switched capacitor circuit 30h is itself another embodiment of the differential type switched capacitor circuit.

[0044] FIG. 14 shows a method flowchart 198 for minimizing clock feedthrough effect when switching off a switched capacitor circuit 20 according to the present invention. The method flowchart 198 contains the following steps:

[0045] Step 200: Provide a plurality of differently sized switch elements: Each switch element in the plurality of differently sized switch elements is for selectively connecting a first terminal of a capacitor to a node depending upon a control signal applied to a control terminal of the switch element.

[0046] Step 202: Provide a low-pass filter to gradually switch off the smallest switch element: The low-pass filter is connected to the control terminal of the smallest switch element.

[0047] Step 204: When switching off, sequence the control signals such that the switch elements are switched off in decreasing order based on size: The largest switch element is switched off first, the next largest is switched off next, and so on until the smallest switch element is switched off last. Until the smallest switch element is switched off, the first terminal of the capacitor is connected to the node and the clock feedthrough effect is not a concern. The low-pass filter will gradually switch off the last switch element minimizing

the clock feedthrough effect of the smallest switch element and the switched capacitor circuit **20** as a whole.

[0048] It should be noted that in the method flowchart **198** shown in **FIG. 14** the node is preferably connected to ground, however, the method according to the present invention is not limited to this configuration.

[0049] **FIG. 15** shows a method flowchart **208** for minimizing clock feedthrough effect when switching off a differential switched capacitor circuit **20** according to the present invention. The method flowchart **208** contains the following steps:

[0050] Step **210**: Provide a plurality of differently sized positive side switch elements: Each positive side switch element in the plurality of differently sized positive side switch elements is for selectively connecting a first terminal of a positive side capacitor to a first node depending upon a control signal applied to a control terminal of each of the switch elements.

[0051] Step **212**: For each positive side switch element, provide a corresponding same size negative side switch element: Each corresponding same size negative side switch element is for selectively connecting a first terminal of a negative side capacitor to a second node depending upon the control signal applied to the control terminal of the positive side switch element.

[0052] Step **214**: Provide a low-pass filter to gradually switch off the smallest positive and negative side switch elements: The low-pass filter is connected to the control terminal of the smallest positive and negative side switch element.

[0053] Step **216**: Provide a center switch element: The center switch element selectively connects the positive side capacitor to the negative side capacitor depending on a control signal applied to a control terminal of the center switch element.

[0054] Step **218**: When switching off, sequence the control signals such that the center switch element is first switched off and then the other switch elements are switched off in pairs in decreasing order based on switch size, whereby the largest positive side switch element and its corresponding negative side switch element are switched off first, the next largest switch element pair is switch off next, and the smallest switch element pair is switched off last. Until the smallest switch element pair is switched off, the first terminal of the positive side capacitor and the first terminal of the negative side capacitor are connected to the first node and the second respectively so that the clock feedthrough effect is not a concern. The low-pass filter gradually switches off the last switch element minimizing the clock feedthrough effect of the smallest switch element and the switched capacitor circuit **20** as a whole.

[0055] Similarly, it should be noted that in the method flowchart **208** shown in **FIG. 15** the first node and the second node are preferably connected to ground, however, the method according to the present invention is not limited to this configuration.

[0056] In contrast to the prior art, the present invention gradually switches off the switched capacitor circuit so that the clock feedthrough effect is minimized and accordingly

the undesired frequency drift of the VCO **10** frequency is properly reduced. When switching off, the prior art implementations suffer from clock feedthrough effect that causes a voltage step change to occur at an internal capacitive node of the VCO **10**. The voltage step change causes the junction diode formed by a switch element in the off state to be slightly forward biased until the dropped voltage returns to the ground potential.

[0057] According to the present invention, the voltage step change at the internal capacitive node is minimized. When switching off, the present invention can minimize the momentary change of the capacitance value of the VCO **10** resonator and the momentary drift in the VCO **10** frequency.

[0058] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.

1. A switched capacitor circuit capable of minimizing clock feedthrough effect, comprising:

a positive side switch element for selectively connecting a positive side first node to a positive side second node depending upon a signal applied to a first control terminal of the positive side switch element, wherein the positive side first node is connected to a positive side capacitor; and

a low-pass filter having an input terminal connected to a control signal and an output terminal connected to the first control terminal of the positive side switch element for making the positive side switch element gradually switch of, wherein the control signal is substantially a two-level signal with a first level for switching off the switched capacitor circuit and a second level for switching on the switched capacitor circuit.

2. The switched capacitor circuit of claim 1, wherein the positive side second node is ground and the positive side switch element is an NMOS transistor.

3. The switched capacitor circuit of claim 1, further comprising:

a negative side switch element of substantially the same size as the positive side switch element for selectively connecting a negative side first node to a negative side second node depending upon the control signal applied to the first control terminal of the positive side switch element, wherein the negative side first node is connected to a negative side capacitor.

4. The switched capacitor circuit of claim 3, further comprising:

a center switch element having a first terminal connected to the positive side first node, a second terminal connected to the negative side first node, and a third control terminal connected to the control signal.

5. The switched capacitor circuit of claim 4, wherein the positive side second node is ground, the negative side second node is ground, and the positive side switch element, the negative side switch element, and the center switch element are NMOS transistors.

6-24. (cancelled)

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