



(51) International Patent Classification:

H01L 21/56 (2006.01) H01L 23/49 (2006.01)
H01L 23/50 (2006.01) H01L 23/66 (2006.01)

(21) International Application Number:

PCT/EP2014/001822

(22) International Filing Date:

2 July 2014 (02.07.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/842,950 3 July 2013 (03.07.2013) US

(71) Applicant: **ROSENBERGER HOCHFREQUENZ-TECHNIK GMBH & CO. KG** [DE/DE]; Hauptstr. 1, 83413 Fridolfing (DE).

(72) Inventors: **CAHILL, Sean, S.**; 3350 Thomas Road, Santa Clara, CA 95054 (US). **SANJUAN, Eric, A.**; 3350 Thomas Road, Santa Clara, CA 95054 (US).

(74) Agent: **ZEITLER VOLPERT KANDBINDER**; Hermsstr. 44, 80539 München (DE).

(81) Designated States (unless otherwise indicated, for every kind of national protection available):

AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available):

ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: A SUBSTRATE LESS DIE PACKAGE HAVING WIRES WITH DIELECTRIC AND METAL COATINGS AND THE METHOD OF MANUFACTURING THE SAME

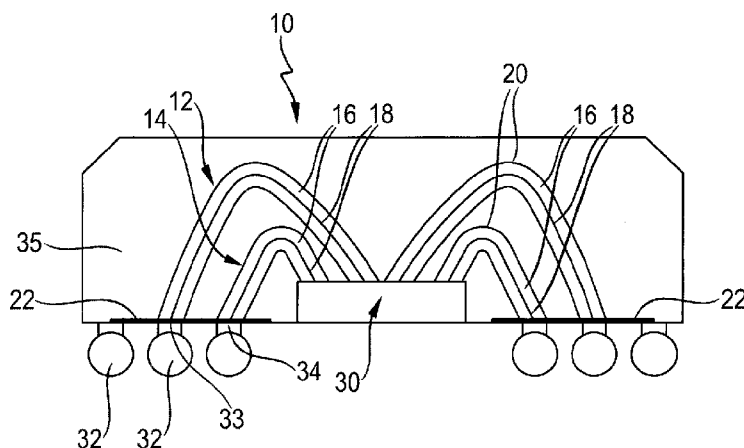


Fig. 1

(57) Abstract: The present invention relates to die packages (10) comprising a die (30) having a plurality of connection pads, a plurality of wire leads (12, 14) having metal cores (18) with a defined core diameter, and a dielectric layer (16) surrounding the metal cores having a defined dielectric thickness, at least one first connection pad (34) held in a mold compound (35) covering the die (30) and the plurality of leads (12, 14) connected to at least one metal core (18), and at least one second connection pad (33) held in the mold compound (35) covering the die (30) and the plurality of leads (12, 14) connected to at least one metal core (18). Further, the present invention relates to a method for manufacturing a substrate less die package.

WO 2015/000593 A1

5 A SUBSTRATE LESS DIE PACKAGE HAVING WIRES WITH DIELECTRIC AND METAL COATINGS AND
THE METHOD OF MANUFACTURING THE SAME

10

15 **Field of the Invention**

The present invention relates to die packages with at least one die having a plurality of connection pads and a plurality of leads extending from the connection pads, the leads having metal cores with a defined core diameter and a dielectric layer surrounding the metal cores having a defined dielectric thickness,
20 respectively.

Background

Electronic devices and components are operating at ever increasing speeds and over increasing frequency ranges. Popular semiconductor package types use wire bonds that can connect to a substrate or leadframe, which in turn can
25 connect to second level interconnects, vias, substrate or package traces, solder balls, or the like, for connection to a printed circuit board (PCB) of an electronic device.

However, packaging can be expensive, particularly if the substrate requires costly materials or precision drilling, etch, or formation of vias.

Summary of the invention

Bearing in mind the problems and deficiencies of the prior art, it is an object of the present invention to provide a die package that can be manufactured easily and with reduced overall production costs.

- 5 The above and other objects, which will be apparent to those skilled in the art, are achieved in the present invention which is directed to a die package comprising a die having a plurality of connection pads, a plurality of leads having metal cores with a defined core diameter, and a dielectric layer surrounding the metal cores
- 10 having a defined dielectric thickness, at least one first connection pad held in a mold compound covering the die and the plurality of leads, the first connection pad being connected to the metal core of a first lead, and at least one second connection pad held in the mold compound covering the die and the plurality of leads, the second connection pad being connected to the metal core of a second lead.
- 15 The die package is preferably a “coreless” package without a permanent substrate for die attachment. The die package according to the invention can be connected to a printed circuit board or to a substrate by means of solder balls, for example.

The first and/or the second connection pads can be held in the mold component

20 in such a way that they are exposed so that they can be connected to the PCB or to the substrate. In other words, the connection pads are held by the overmold compound without being supported by a die substrate.

The first connection pad may be connected to the metal core of a first lead and the second connection pad may be connected to the metal core of a second lead,

25 whereas the first lead is longer than the second lead, has a different core diameter and/or has a different dielectric diameter.

The die package can include several dies which may be arranged as stacked dies. Further, at least one of the leads may be a ribbon lead formed by total or partial fusion of the dielectric coatings of two or more leads.

The dependent claims are directed to advantageous embodiments of the invention.

Further, the present invention is directed to a method of manufacturing a die package according to the invention, the method comprising the following steps:
5 placing of one or more dies on a temporary workpiece including temporarily attached pads, using wirebonding to connect the die to the temporarily attached pads, coating of metal cores of the wirebonds with a dielectric coating, overmolding the die assembly and the leads, and removing at least part of the temporary workpiece and/or at least part of the overmold to expose the attached
10 pads for connecting them to a printed circuit board or another substrate, for example by means of solder balls.

The method may further include one or more of the additional method steps shown in Fig. 2.

According to the invention, "coreless" semiconductor die packages can be
15 produced. During manufacture, these die packages have leads attached between the die and pads on a temporary substrate. After the overmold, the temporary substrate is removed to allow exposure of the lead attached pads. The leads include a metal core surrounded by a dielectric. Preferably, they further include a metallized outer layer attached to ground pad connections.

20 **Brief Description of the Drawings**

Fig. 1 is an illustration of dielectric and metal coated leads in a coreless package,

Fig. 2 illustrates one embodiment of a method for manufacture of a coreless package,

Fig. 3 illustrates method steps for manufacture of dielectric coated leads with
25 outer ground connected metallization useful in the embodiment illustrated with respect to Fig. 1 and 2, and

Fig. 4 illustrates a subtractive method for manufacture of dielectric coated leads with outer ground connected metallization.

Detailed Description

As seen in Fig. 1, a “coreless” package 10 without a permanent substrate for die attachment can be constructed. Such a semiconductor die packaging system can be formed to have leads 12, 14 with a dielectric layer 16 deposited over an inner metal core 18, as well as an outer metal layer 20 deposited over the dielectric layer 16. In operation, the outer metal layer 20 is attached to a ground pad 22. The leads 12, 14 are attached to die 30 that can include multiple connection pads for signal, power, or other functionality required by the die 30. In the described embodiment, the die 30 does not have to be attached to a permanent substrate. Leads 12, 14 can connect to conductive pads 34, while the conductive pads can be attached by means of solder balls 32, gold bumps, or other suitable interconnects to a printed circuit board or other substrate. As illustrated, the leads 12, 14 are surrounded by an epoxy or other mold packaging compound, and may have substantially different lengths. In the illustrated embodiment, all leads have substantially the same impedance due to lead construction, even though lengths may differ. However, in other embodiments the leads can be constructed to have distinctly different impedances. For example leads that have a metal core of a defined diameter along its length can be sequentially coated with a thin dielectric layer and a conductive metal layer. Such leads are suitable for transfer of power because the consequent low impedance reduces power sag. Alternatively, leads that have a much thicker dielectric layer are more suitable for transmission of signal data. In certain embodiments, due to the superior electrical characteristics of lead construction as disclosed, leads having substantially different lengths but the same core diameter can have substantially the same impedance, within 10% of target impedance, despite having lengths that vary 50% or greater. In certain embodiments, lead differences can be even greater, with two leads having the same cross sectional structure and impedance, but one lead being as much as ten (10) times the length of the other. In still other embodiments, stacked die are contemplated, as are ribbon connections formed by total or partial fusion of dielectric coatings forming the leads.

Fig. 2 is one embodiment of a method for manufacture of a coreless package such as described with respect to Fig. 1. Multiple dies can be temporarily

attached (40) to a workpiece that can be later physically released and removed, or otherwise etched or chemically eliminated. The workpiece includes temporarily attached pad to support both metal core and outer metal ground layer attachment of each lead. Wirebonding (41) is used to connect the die to the temporarily
5 attached pads surrounding the die, followed by a dielectric coating (42) of the metal core. The dielectric layer is metallized (43), with connections to ground pads being formed, and the entire multiple die assembly and leads are overmolded (44). After curing of the overmold, the temporary workpiece is removed (45), and the overmold may be etched or otherwise removed (46) by
10 grinding or polishing to better expose the lead attached pads. Individual die and their connected leads can be singulated, and readied for solder ball or other connection to a printed circuit board (PCB) or another substrate (47).

Generally, thin dielectric layers will provide low impedance, suitable for power lines, thick dielectric is good for signal, and outer metal layers are connected to
15 same ground. Note that a combination of core diameters and dielectric thicknesses is possible and a series of such steps may be performed to achieve more than two impedances. In certain embodiments it may be desirable to have large cores on power lines to increase power handling capacity, reduce power line temperatures, and/or further compensate any inductance on power supply
20 and ground lines that would exacerbate ground bounce or power sag. Dielectric layers of intermediate thickness are also useful, since many packages could benefit from having leads of three (3) or more different dielectric thicknesses. For example, a lead have an intermediate dielectric thickness could be used to connect a source and load of substantially different impedance to maximize
25 power transfer. For example, a 10 ohm source can be coupled to a 40 ohm load with a 20 ohm lead. Also, since cost of dielectric can be high, critical signal pathways can interconnected using thick dielectric, with less critical status, reset, or the like leads can be coated with a dielectric layer having a thickness greater than the power leads, but less than (intermediate) to the critical signal leads.
30 Advantageously, this can reduces dielectric deposition material cost and time.

The precise thickness of the dielectric coating may be chosen, in combination with the wirebond diameter, to achieve a particular desired impedance value for each lead.

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\epsilon_r}} \cdot \log\left(\frac{b}{a}\right) \quad (1)$$

- 5 The characteristic impedance of a coax line is given in Eq. (1), where L is the inductance per unit length, C is the capacitance per unit length, a is the diameter of the bond wire, b is the outside diameter of the dielectric and ϵ_r is relative permittivity of the coaxial dielectric.

As illustrated in Fig. 3, in one embodiment manufacture of dielectric coated leads with outer ground connected metallization can proceed using the following steps. Connection pads are cleaned (50) on the die and the substrate and a wirebonder is used to connect the die to the connection pads (51). Optionally, a second diameter wire can be attached (52) (e.g. a larger diameter wire suitable for power connections), or areas of the die can be masked (53) or otherwise protected to allow for selective deposition. One or more layers of dielectric of the same or different composition can be deposited (54), followed by selective laser or thermal ablation, or chemical removal of portions of the dielectric to allow access to ground connections covered in the dielectric deposition step (55). This step is optional, since in some embodiments, the need for a ground via can be eliminated. This is particularly true for die operating at higher frequencies, since frequency dependence on thickness value (function of ϵ_r) allows for ground establishment through capacitive coupling. Metallization (57) follows, covering the dielectric with a metal layer that forms the outermost metallized layer of the leads, and also connecting the leads to ground. The entire process can be repeated multiple times (58), useful for those embodiments using selective deposition techniques, and particularly for those embodiments supporting multiple die or complex and varied impedance leads. In the final step, for non-cavity packages, an overmold can be used to encapsulate leads (59). Alternative embodiments and additional or variant method steps are also described in

US20120066894 and US Patent 6,770,822, the disclosures of which are fully incorporated by reference.

In certain embodiments, modifications and additions to the described process are possible. For example, providing conformal coatings of dielectric can be accomplished through a variety of methods using chemical (electrophoretic),
5 mechanical (surface tension), catalytic (primer, electromagnetic [UV, IR], electron beam, other suitable techniques. Electrophoretic polymers are particularly advantageous because they can rely on self-limiting reactions that can deposit precise thicknesses readily by adjusting process parameters and or simple
10 additive, concentration, chemical, thermal, or timing changes to an electrophoretic coating solution.

In other embodiments, dielectric precoated bondwires can be used to form leads. While commercially available coated wires typically are thinner in dielectric thickness than is necessary to create, for example, 50 ohm leads, the foregoing
15 discussed dielectric deposition steps can be used to increase dielectric thickness to set the desired impedance. Use of these precoated wires can simplify other process steps necessary to create coaxes, and can allow for thinner layers of needed vapor deposited dielectrics and faster processing times to create ground
vias. Precoated bondwires can be used to prevent shorting for narrowly spaced
20 or crossing leads. In certain embodiments the precoated bondwire can have a dielectric made from a photosensitive material to allow for selective patterning techniques.

In other embodiments, the dielectric parylene can be used. Parylene is the trade name for a variety of chemical vapor deposited poly(p-xylylene)polymers used as
25 moisture and dielectric barriers. Parylene can be formed in a growth limited condensation reaction using a modified parylene deposition system where the die, substrate, and leads are aligned to a photoplate which allows EM radiation (IR, UV or other) to strike in a precise manner causing selective growth rate of dielectric. Advantageously, this can minimize or eliminate the need for processes
30 to create contact vias, bulk removal of parylene, etc.

Parylene and other dielectrics are known to suffer from degradation due to oxygen scission in the presence of oxygen, water vapor and heat. Damage can be limited by metal layers that form excellent oxygen vapor barriers, with thin layers of 3-5 micron thickness capable of forming true hermetic interfaces.

5 Alternatively, if metal has been selectively removed, or not deposited in certain areas due to electrical, thermal, or manufacturing requirements, a wide range of polymer based vapor oxygen barriers can be used, with polyvinyl alcohol (PVA) being one widely used polymer. These polymers can be glob topped, screen printed, stenciled, gantry dispensed, sprayed onto parylene surface that will be

10 exposed to the oxygen or H₂O vapor environment. Advantageously, use of vapor barrier polymers can be a part of a cost reduction strategy, since thicker layers of high cost parylene or other oxygen sensitive might otherwise be required.

As will be appreciated, all of the described method steps can benefit from various selective deposition techniques. Selective deposition can be by physical masking,

15 directed polymer deposition, photoresist methods, or any other suitable method for ensuring differential deposition thickness on the metal core, dielectric layer, or other outermost layer at time of deposition. While selective deposition allows for additive methods to build leads, it also allows for subtractive techniques in which dielectric or metal is removed to form multiple impedance interconnects. For

20 example, a package populated by one or more die can be wire-bonded as appropriate for interconnect of all package and device pads. As seen with respect to Fig. 4, which illustrate steps and structures for manufacture of a die package, the dielectric coating 200 can be deposited (step A) to a thickness X-A over a wirebond metal conductor 202, where A is the thickness of the dielectric needed

25 for the secondary interconnect impedance. The secondary impedance wirebond dielectrics can be removed (step B) for example by an etch step, followed by a second coating 204 deposition (step C) followed by metallization 206 of both interconnects (step D). This subtractive process will create wirebonds of two distinct impedances.

30 In particular, the present invention is directed to a die package comprising a die having a plurality of connection pads, a plurality of leads having a metal cores

with a defined core diameter, and a dielectric layer surrounding the metal cores having a defined dielectric thickness, first connection pads held in a mold compound covering the die and the plurality of leads connected to the metal cores, and second connection pads held in a mold compound covering the die
5 and the plurality of leads connected to the metal cores.

The metal core diameters of the plurality of leads may differ in diameter.

The impedance of a subset of the plurality the leads may be within 10%.

Further, the invention relates to a method of manufacture the above die package, selected steps of the method being shown in Fig. 2 and elsewhere.

Claims

5

1. A die package (10) comprising

a die (30) having a plurality of connection pads,

a plurality of leads (12, 14) having metal cores (18) with a defined core diameter, and a dielectric layer (16) surrounding the metal cores having a defined

10 dielectric thickness, respectively,

at least one first connection pad (34) held in a mold compound (35) covering the die (30) and the plurality of leads (12, 14) connected to at least one metal core (18), and

15 at least one second connection pad (33) held in the mold compound (35) covering the die (30) and the plurality of leads (12, 14) connected to at least one metal core (18).

20 2. The die package of claim 1, characterized in that the first connection pad is connected to the metal core of a first lead with a first metal core diameter, and the second connection pad is connected to the metal core of a second lead with a second metal core diameter, the metal core diameters differing in diameter.

25 3. The die package of claim 1 or 2, characterized in that the first connection pad is connected to the metal core of a first lead with a first length, and the second connection pad is connected to the metal core of a second lead with a second length, the first length differing from the second length, preferably by 50% or more.

30 4. The die package of claim 2 or 3, characterized in that the first lead and the second lead have substantially the same impedance or alternatively have distinctly different impedances.

5. The die package of any of the precedent claims, characterized in that an outer metal layer is deposited over the dielectric layer of one or more leads.

6. The die package of claim 5, characterized by at least one ground pad, wherein at least one of the outer metal layers is connected to the ground pad.

7. The die package of any of the precedent claims, characterized in that the impedance of a subset of the plurality the leads is within 10%.

8. The die package of any of the precedent claims, characterized in that the package is a coreless package without a permanent substrate for die attachment.

9. Method of manufacture of a die package (10) of one of the precedent claims comprising the following steps:

Placing (40) of one or more dies on a temporary workpiece including temporarily attached pads,

Using wirebonding (41) to connect the die to the temporarily attached pads,

Coating (42) of metal cores of the wirebonds with a dielectric coating,

Overmolding (44) the die assembly,

Removing (45, 46) at least part of the temporary workpiece and/or at least part of the overmold to expose the attached pads for connecting to a printed circuit board or another substrate.

10. Method of claim 9, further including metallization (43) of the dielectric coating such that connections to ground pads of the temporary workpiece are formed.

11. Method of claim 9 or 10, wherein at least part of the temporary workpiece and/or of the overmold is removed by etching, by grinding and/or by polishing.

12. Method of any of claims 9 to 11, wherein individual dies and their connected leads are singulated (47) and readied for connection to a substrate like a printed circuit board.

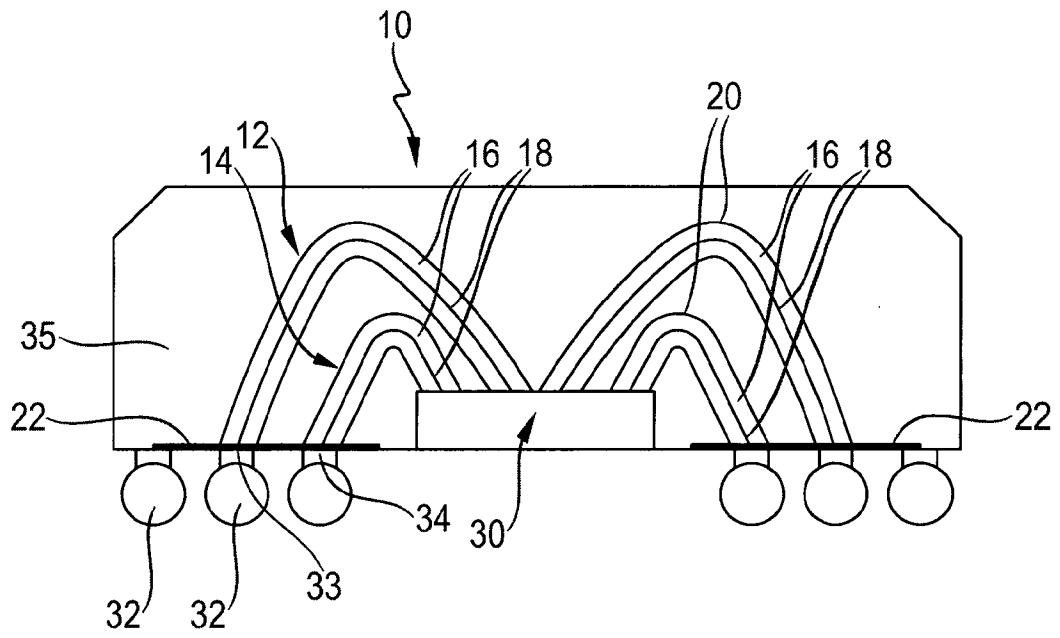


Fig. 1

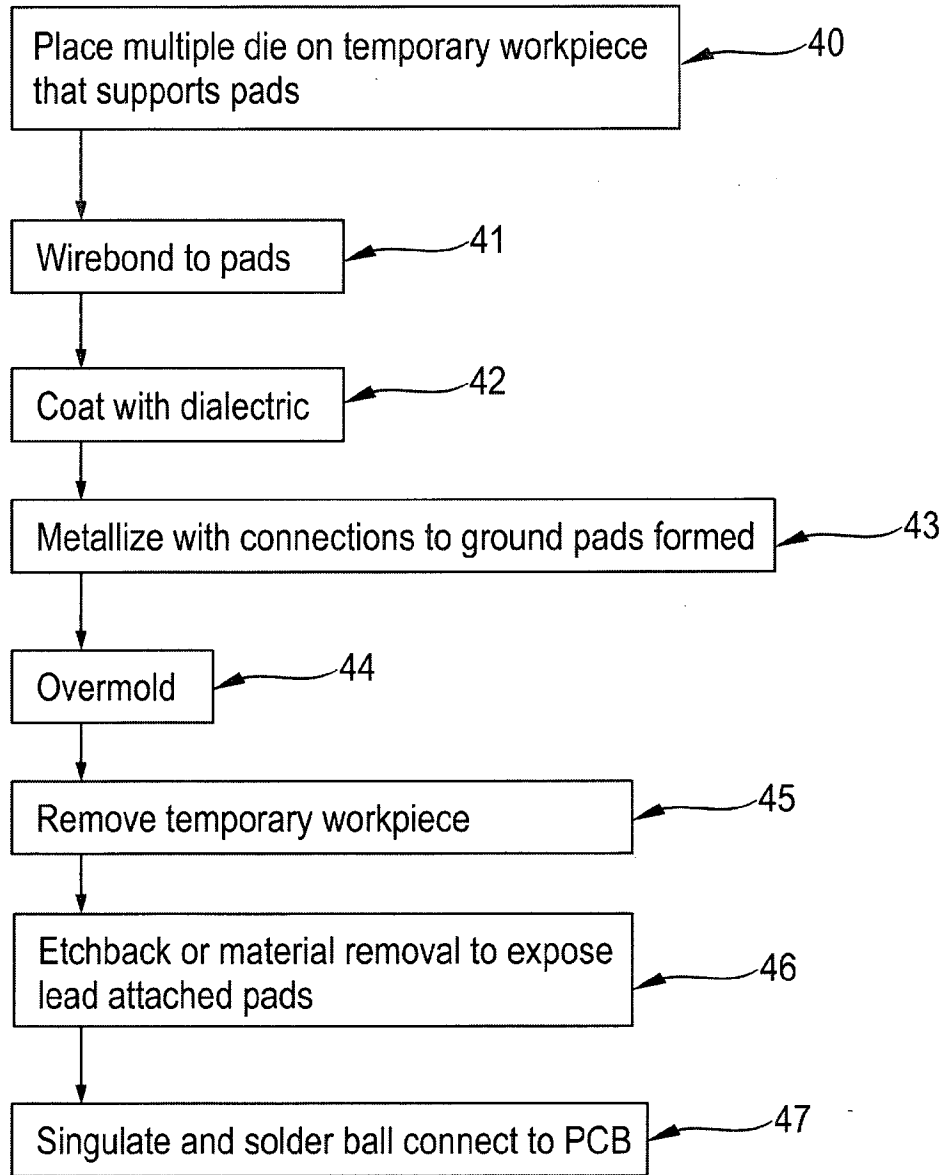


Fig. 2

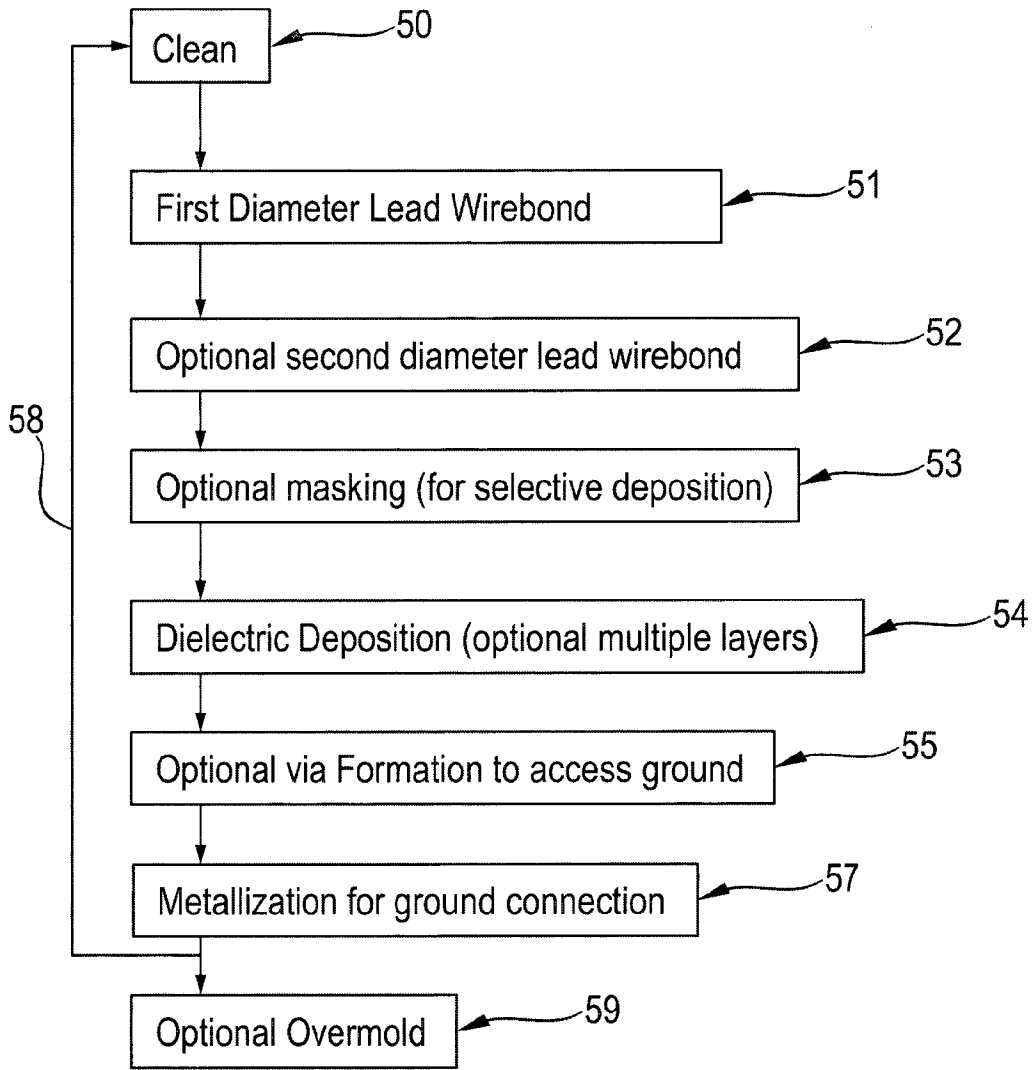


Fig. 3

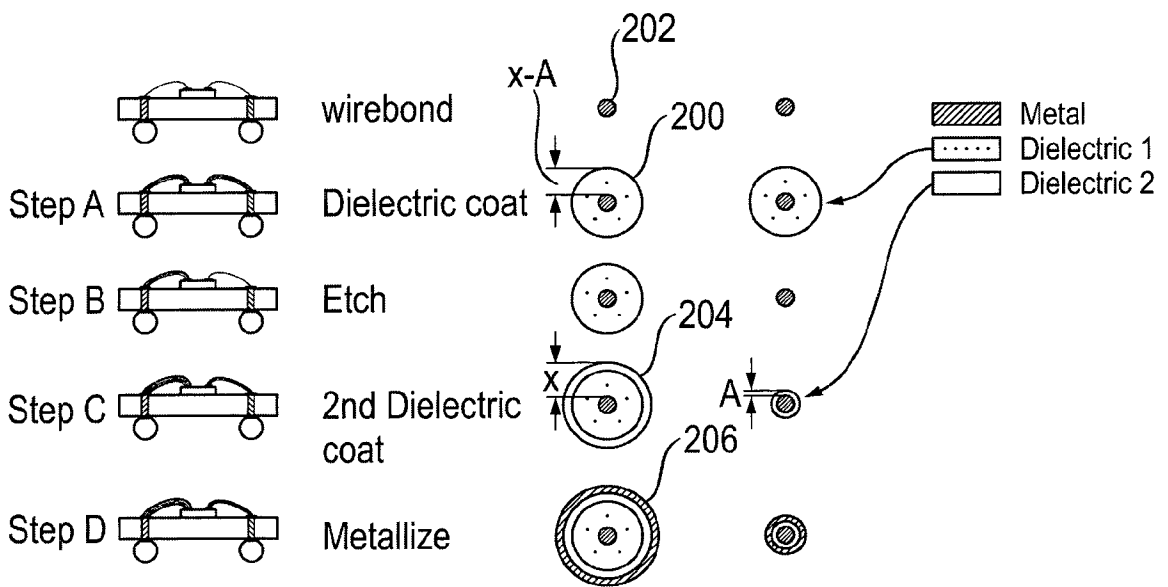


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/001822

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/56 H01L23/50 H01L23/49 H01L23/66
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/070446 A1 (HORIUCHI MICHIO [JP] ET AL) 13 June 2002 (2002-06-13)	1,3-11
Y	paragraphs [0014], [0041] - [0058], [0066], [0070] - [0075], [0085], [0089] - [0091], [0096] - [0099], [0105] - [0106], [0124] - [0126]; figures 4, 6,7,8a-8e,9	2,12
Y	----- US 2009/159320 A1 (SANJUAN ERIC A [US] ET AL) 25 June 2009 (2009-06-25)	2
A	cited in the application paragraphs [0001], [0026], [0049] - [0053]; figures 6,14,16	1,3-9
Y	----- JP 2010 206162 A (SEIKO INSTR INC) 16 September 2010 (2010-09-16)	12
A	abstract; figures 3-6,9-15 -----	1,8,9,11

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search 29 August 2014	Date of mailing of the international search report 09/09/2014
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Ahlstedt, Mattias

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/EP2014/001822

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