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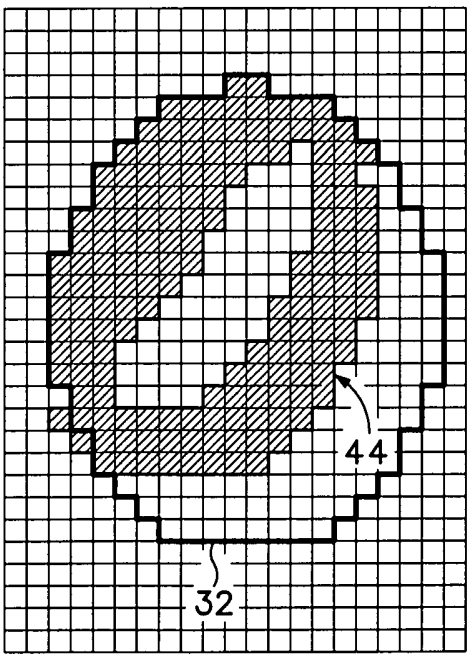
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(54) Title: PROBE HEAD ARRAYS



(57) Abstract: A probe head for testing devices formed on a semiconductor wafer includes a plurality of probe DUT (device under test) arrays. Each device under test includes pads that are urged into pressure contact with probes in a corresponding probe DUT array. The probe arrays patterns have discontinuities such as indentations, protuberances, islands and openings that are opposite at least one device when the probes contact the pads.

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PROBE HEAD ARRAYS

Field of the Invention

The present invention relates to a probe head array for testing devices on a semiconductor wafer.

Description of the Related Art

Semiconductor devices, such as microprocessors, DRAM, and flash memory, are fabricated in a well known manner on a semiconductor wafer. Depending upon the size of the wafer and of each device formed thereon, there may be only a few or more than a thousand devices on a single wafer. These devices are typically identical to one another, each including a plurality of conductive pads on the surface thereof for power and other connections to the devices such as input signals, output signals, control signals and the like.

It is desirable to test the devices on the wafer to determine which are fully functional, and therefore suitable for packaging and sale, and which are inoperative or partially functional, and therefore unsuitable for packaging. To this end, wafer testers apply power and input signals to the devices and monitor outputs during a predetermined testing routine while the devices are still on the wafer.

Because each device under test (DUT) is substantially identical to the others, there are a plurality of identical probe DUT arrays. Each probe DUT array includes probes that make discrete pressure connections to separate ones of the pads on a corresponding DUT.

These probe DUT arrays make up a single probe array that is mounted on a probe head, or multiple probe heads which are part of the wafer probe card. The wafer probe card typically includes multiple channels, one for each DUT array on the probe head. As a result, multiple DUT arrays simultaneously contact multiple DUTs on the wafer.

Obviously, the more DUTs that can be simultaneously tested, the faster the entire wafer can be tested. But there is a limit to the number of tester channels that can be connected to the DUT arrays. While some testers contain many channels, e.g., 128 channels, there may be several hundred DUTs on the wafer to be tested. The testing process consequently includes urging the probe DUT arrays into pressure contact with the pads on a first corresponding set of DUTs (i.e. a first "touchdown"), performing the test, lifting the probes from the DUTs, moving the probes relative to the wafer, bringing the probes into contact with pads on another set of DUTs (i.e. a second "touchdown"), and testing additional DUTs. This process is repeated until all the DUTs on the wafer are tested.

The testing process described above is highly time sensitive due to the cost of the test equipment being tied up during testing. In other words, if testing could be speeded up, the

production cost of finished semiconductor devices could be reduced as well. It is consequently desirable to minimize probe array touchdowns per wafer, multiple probe touchdowns per DUT, and stepping distance between touchdowns. The total number of touchdowns on a wafer is a function of how many DUT arrays are on the probe head (which in turn is often a function of how many channels the test equipment has), how many DUTs are on the wafer, and the relative configurations of the wafer DUTs and the DUT arrays. Because each testing routine takes time to run, lowering the total number of touchdowns reduces the test time for the wafer. Touchdowns typically vary between one or two on the low end to about nine on the high end.

Multiple DUT touchdowns occur when a probe DUT array is brought into contact with a particular DUT more than once. Put differently, there may be some overlap between the DUTs already tested and the probe DUT arrays as they are urged against the wafer for the second and subsequent touchdowns. It is desirable to limit the number of touchdowns for each DUT to as few as possible, preferably one. This is because when the probes are urged against the contact pads, the pads are scrubbed. Repeated scrubbing can damage the pads to the point where the DUT cannot be packaged properly. It is obviously undesirable for the testing process to damage a fully functional DUT. In addition, testing efficiency increases as the number of touchdowns decrease.

Finally, it is also desirable to minimize the stepping distance, which is the amount of relative lateral movement of the probe array and the wafer between touchdowns. Doing so further reduces the time required to completely test all the DUTs on the wafer. Touchdowns per wafer, multiple touchdowns, and stepping distance will be described in more detail with reference to the drawings.

It would be advantageous for a probe head to provide lower touchdown per wafer, lower multiple touchdowns per DUT, and reduced stepping distance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a probe card having a probe head mounted thereon.

FIG. 2 is a significantly enlarged view of a portion of a probe DUT array on the probe head of FIG. 1.

FIG. 3 is a schematic depiction of a prior art configuration of probe DUT arrays on a probe head.

FIG. 4 shows the probe DUT arrays of FIG. 3 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 5 is a view similar to FIG. 4 showing the probe DUT arrays during a second touchdown.

FIG. 6 is an enlarged version of the DUT configurations shown in FIGs. 4 and 5 illustrating the number of touchdowns per DUT.

FIG. 7 is a schematic depiction of another prior art configuration of probe DUT arrays on a probe head.

FIG. 8 shows the probe DUT arrays of FIG. 7 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 9 is a view similar to FIG. 8 showing the probe DUT arrays during a second touchdown.

FIG. 10 is a schematic view illustrating the total number of touchdowns required to test all of the DUTs on the wafer.

FIG. 11 is an enlarged version of the DUT configurations shown in FIGs. 8 and 9 illustrating the number of touchdowns per DUT.

FIG. 12 is a schematic depiction of another prior art configuration of probe DUT arrays on a probe head.

FIG. 13 shows the probe DUT arrays of FIG. 12 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 14 is a view similar to FIG. 13 showing the probe DUT arrays during a second touchdown.

FIG. 15 is a schematic view illustrating the total number of touchdowns required to test all of the DUTs on the wafer.

FIG. 16 is an enlarged version of the DUT configurations shown in FIGs. 13 and 14 illustrating the number of touchdowns per DUT.

FIG. 17 is a schematic depiction of another prior art configuration of probe DUT arrays on a probe head.

FIG. 18 shows the probe DUT arrays of FIG. 17 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 19 is a view similar to FIG. 18 showing the probe DUT arrays during a second touchdown.

FIG. 20 is a view similar to FIGs. 18 and 19 showing the probe DUT arrays during a third touchdown.

FIG. 21 is a view similar to FIGs. 18-20 showing the probe DUT arrays during a fourth touchdown.

FIG. 22 is a schematic view illustrating the total number of touchdowns required to test all of the DUTs on the wafer.

FIG. 23 is an enlarged version of the DUT configurations shown in FIGs. 18-21 illustrating the number of touchdowns per DUT.

FIG. 24 is a schematic depiction of probe DUT arrays on a probe head constructed in accordance with the present invention.

FIG. 25 shows the probe DUT arrays of FIG. 24 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 26 is a schematic view illustrating the total number of touchdowns required to test all of the DUTs on the wafer.

FIG. 27 is an enlarged version of the DUT configurations shown in FIG. 25 illustrating the number of touchdowns per DUT.

FIG. 28 is a schematic depiction of probe DUT arrays on a probe head constructed in accordance with a second embodiment of the present invention.

FIG. 29 shows the probe DUT arrays of FIG. 28 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 30 is a view similar to FIG. 29 showing the probe DUT arrays during a second touchdown.

FIG. 31 is an enlarged version of the DUT configurations shown in FIGs. 29 and 30 illustrating the number of touchdowns per DUT.

FIG. 32 is a schematic depiction of probe DUT arrays on a probe head constructed in accordance with a third embodiment of the present invention.

FIG. 33 shows the probe DUT arrays of FIG. 32 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 34 is a view similar to FIG. 33 showing the probe DUT arrays during a second touchdown.

FIG. 35 is a view similar to FIGs. 33 and 34 showing the probe DUT arrays during a third touchdown.

FIG. 36 is an enlarged version of the DUT configurations shown in FIGs. 33-35 illustrating the number of touchdowns per DUT.

FIG. 37 is a schematic depiction of probe DUT arrays on a probe head constructed in accordance with a fourth embodiment of the present invention.

FIG. 38 shows the probe DUT arrays of FIG. 37 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 39 is a view similar to FIG. 38 showing the probe DUT arrays during a second touchdown.

FIG. 40 is a view similar to FIGs. 38 and 39 showing the probe DUT arrays during a third touchdown.

FIG. 41 is an enlarged version of the DUT configurations shown in FIGs. 38-40 illustrating the number of touchdowns per DUT.

FIG. 42 is a schematic depiction of probe DUT arrays on a probe head constructed in accordance with a fifth embodiment of the present invention.

FIG. 43 shows the probe DUT arrays of FIG. 42 during a first touchdown on a wafer having a plurality of DUTs, each being represented schematically by a square within a bold line that represents the perimeter of the DUTs on the wafer.

FIG. 44 is a view similar to FIG. 43 showing the probe DUT arrays during a second touchdown.

FIG. 45 is an enlarged version of the DUT configurations shown in FIGs. 43 and 44 illustrating the number of touchdowns per DUT.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to FIGs. 1 and 2, indicated generally at 10 in FIG. 1 is a probe card that includes a probe head 12. Probe card 10 can be used to carry either a prior art probe head or a probe head constructed in accordance with the present invention. The probe head includes a probe array 14 that is made up of a plurality of probe DUT arrays, like probe DUT array 16, represented schematically by squares formed in probe array 14.

Each of the probe DUT arrays, like probe DUT array 16, includes a pattern of probes, like probes 18, 20 in FIG. 2. The probes in FIG. 2 make up only a portion of the probes in probe DUT array 16. Each DUT array, like DUT array 16, may include 60 to 80 or more probes like those shown in FIG. 2. Because the wafer to be tested typically includes DUTs

that are identical to one another, including the pad configuration on each DUT, the probe DUT arrays that make up probe array 14 are each also identical to one another. Each of the probes includes a tip, like tip 22 on probe 18 and tip 24 on probe 20. As will be soon described, during wafer testing, probes in probe array 14 are positioned opposite a wafer and the probe head and wafer are moved together until the probe tips, like tips 22, 24, contact corresponding pads on the DUTs on the wafer. The probes are preferably manufactured as described in US Patent No. 5,974,662 which is incorporated herein by reference.

Probe array 14 is mounted on a space transformer 26. The space transformer comprises a multi-layer ceramic substrate that includes a ground plane and a power plane connected to the appropriate probes in each probe DUT array for applying power to each DUT during testing. The probes in the array are connected via different ones of the layers in the space transformer to contacts (not visible) on a round printed circuit board 28. As is known in the art, this connection may be made via an interposer disposed between space transformer 26 and circuit board 28. There may be as many as several thousand such connections. The contacts on printed circuit board 28 are used to connect each probe DUT array, like probe DUT array 16, to the contacts that make up a channel on a tester (not shown). The DUT configuration on each wafer can vary as a result of a number of different factors, e.g., different manufacturers, different products, different testers, different wafer sizes, etc. As a result, probe heads must be designed according to the wafer DUT pattern that results from these factors. A more detailed description of a wafer prober test setup can be found in U.S. Published Application No. 2004/0130312, incorporated herein by reference.

Turning now to FIGs. 3-5, a prior art probe array configuration 30 is indicated by hatched lines. Probe array 30 is formed on a space transformer (not shown in FIG. 3) in the same manner that probe array 14 is formed on space transformer 26 in FIG. 1. Each of the squares contained within the shape made by probe array 30 corresponds to a different probe DUT array, like probe DUT array 31, with all of the probe DUT arrays together making up probe array 30. There are a total of 205 probe DUT arrays in probe array 30. The arrangement of DUTs on a semiconductor wafer in FIGs. 4 and 5 is indicated schematically by squares within a bold line that contains the DUT pattern 32, with each of the squares in DUT pattern 32 corresponding to a different DUT formed on the wafer. The circular shape of the wafer perimeter that contains the DUT pattern 32 is not shown in the drawings. As can be seen in FIG. 4, a number of the probe DUT arrays are registered with a corresponding number of DUTs on the wafer. But many of the DUTs are not registered with a corresponding DUT array. In addition, some of the probe DUT arrays, like probe DUT array 34and several probe

DUT arrays 36, extend beyond DUT pattern 32 and thus are not opposite a DUT. There are a total of 205 probe DUT arrays in probe array 30 and a total of 290 DUTs in DUT pattern 32 on the wafer.

To operate the prior art probe head having the configuration shown in FIG. 3, the probe head and the wafer are first positioned relative to one another as shown in FIG. 4 with probes on the DUT arrays opposite corresponding pads on DUTs in pattern 32. The wafer and the probes are moved toward one another until the probes make contact with pads on the DUTs. Each DUT is supplied with power from the appropriate probes and a predetermined test program is simultaneously run on each of the DUTs in pattern 32 that is opposite a DUT array. Various input signals are supplied to the DUT, and DUT outputs are monitored to confirm that the DUT is functioning as designed. After the test program runs and a determination is made as to which DUTs are fully functional and which cannot be utilized, the probe head and the wafer are separated from one another, and the probe head is stepped, i.e., moved laterally relative to the wafer, to the position of FIG. 5. Probe array 30 and the wafer are then again moved into contact with one another so that the probe tips in the array make a pressure connection against corresponding pads on the DUTs. Power is again applied and the same test procedure is run thereby testing the remaining DUTs on the array. As can be seen by comparing FIGs. 4 and 5, a number of DUTs in the central portion of the wafer have probes urged against them during both touchdowns. In this example, the reasons why a large probe head array is not constructed so as to contact all of the DUTs on the wafer in a single touchdown include insufficient number of tester channels, size limits in the manufacture of a space transformer 26 (shown in FIG.1), and yield issues when populating space transformer 26 with probes 18,20 (shown in FIG. 2). In this particular instance, the bottom three rows of the wafer shown in FIG. 4 cannot be contacted because the currently available space transformer 26 is not large enough.

The graphical depiction of FIG. 6 quantifies the number of DUTs that are subject to a single contact or touchdown from a probe DUT array and those that are subject to two touchdowns. Each DUT, depicted by a square in DUT pattern 32, includes either the numeral 1 or 2 thereon. The DUTs that have the numeral 1 were subject to only one touchdown as a result of the application of probe array 30 as depicted in FIGs. 4 and 5 while the DUTs bearing the numeral 2 were subject to two touchdowns.

The numbers in rows 38, 40, 42 in FIG. 6 indicate DUTs having 0, 1, and 2 touchdowns, respectively.

First, because it is undesirable to leave a DUT untested, none of the DUTs had zero touchdowns. As can be seen, for example, in the fifth column from the left, there is a 7 in the double-touchdown row and a 11 in the single-touchdown row. The number 7 was derived by summing the number of double touchdowns of the DUTs in the column above the numeral 7. Similarly, the 11 was derived by summing the number of single touchdowns from the DUTs in the same column. And each of the other columns of numbers is similarly derived. As a result, the sum of all of the touchdowns in row 42 equals 107, i.e., 107 DUTs on the wafer were subject to double touchdowns. Similarly, the sum of the numbers in row 40 equals 183, i.e., 183 DUTs were subject to a single touchdown. The sum of 107 and 183 equals 290 which is the total number of DUTs on the wafer.

In short, 205 probe DUT arrays test all of the DUTs on the wafer in two wafer touchdowns with 107 out of 290 DUTs being subject to double touchdowns.

Turning now to FIGs. 7-10, another prior art probe array configuration 11 is indicated by hatched lines. The same schematic representations are used in FIGs. 7-10 as in FIGs. 3-5. In other words, probe array 11 is formed on a space transformer (not shown in FIGs. 7-10), and each of the squares contained within the shape made by probe array 11 in FIGs. 8 and 9 correspond to a different probe DUT array with all of the probe DUT arrays together making up probe DUT array 11.

Similarly, the arrangement of DUTs on a semiconductor wafer in FIGs. 8 and 9 is indicated schematically by squares within a bold line that contains the DUT pattern with each of the squares within the bold line corresponding to a different DUT formed on the wafer. As can be see in both FIGs. 8 and 9, a number of the probe DUT arrays are registered with the corresponding number of DUTs on the wafer. But many of the DUTs are not registered with a corresponding DUT array. In addition, some of the probe DUT arrays extend beyond the probe DUT pattern and are thus not opposite a DUT.

To operate the prior art probe head having the configuration shown in FIG. 7, the probe head and the wafer are first positioned relative to one another as shown in FIG. 8 with probes on the DUT arrays opposite corresponding DUT pads. The wafer and probes are moved toward one another until the probes make contact with the pads. Testing proceeds as described above, and when finished, the probe head and the wafer are separated from one another, and the probe head is stepped to the position of FIG. 9. Probe array 11 and the wafer are then again moved into contact with one another for another round of testing.

The touchdowns of probe array 11 illustrated in FIGs. 8 and 9 are represented by a rectangle 13 in FIG. 10, with the numerals 1, 2 indicating the touchdowns of FIGs. 8 and 9,

respectively. FIG. 10 is a schematic illustration of each of the additional touchdowns that are required to complete testing of all the DUTs on the wafer. For example, after touchdowns 1, 2, which test all of the DUTs in rectangle 13, the probe head is stepped to position 3, illustrated schematically in FIG. 10 within rectangle 15. The probe head again contacts the DUTs for testing. Thereafter, the probe array and wafer are separated from one another, the probe head is stepped down one row of DUTs, similar to the one-row step between FIG. 8 and FIG. 9, to complete testing of all the DUTs within rectangle 15.

The probe array 11 is again stepped to the rectangle bearing the numerals 5, 6, and the fifth and sixth touchdowns and testing complete of all DUTs within that rectangle. Additional stepping and testing occurs as illustrated in the rectangles of FIG. 10 until all of the DUTs are tested. As illustrated in FIG. 10, this requires a total of 14 touchdowns.

A somewhat enlarged version of the DUT pattern on the wafer from FIGs. 8 and 9 is depicted in FIG. 11 with the number of touchdowns each DUT is subjected to. As can be seen, an advantageous feature of probe array 11 when used in the stepping pattern described is that each DUT is subject to only a single touchdown during testing. On the other hand, a total of 14 touchdowns are required to test all the DUTs on the wafer. This results in a relatively long time to test all of the DUTs.

Turning now to FIGs. 12-15, another prior art probe array 17 is depicted using the same schematic representations as in FIGs. 7-10. While FIGs. 7-10 may be thought of as a skipped-row approach, FIGs. 12-15 comprise a similar approach but using skipped columns. For example, the first touchdown on the wafer DUTs is illustrated in FIG. 13 with the second being illustrated in FIG. 14. The step from FIG. 13 to FIG. 14 comprises a lateral shift of one column of DUTs. Steps 1, 2 are illustrated schematically in 15 via rectangle 19. As can be seen in FIG. 15, additional steps of the probe array, first to touchdown 3, and then a lateral shift of one column to touchdown 4, then to touchdown 5, another lateral shift, etc., results in testing all of the DUTs on the wafer. As illustrated in FIG. 15, this approach requires a total of 16 touchdowns.

Turning now to FIG. 16, a slightly enlarged version of the DUT pattern on the wafer illustrates the number of touchdowns on each DUT. As in the skipped-row probe array, each DUT is subject only to a single touchdown. But a total of 16 touchdowns are required to test all 494 DUTs on the wafer. Again, this results in a relatively long time to test all the DUTs.

Turning now to FIGs. 17-22, illustrated therein is another prior art probe array 21 and testing method. The same schematic representations are used in FIGs. 17-22 as in the previous descriptions of the prior art. Depicted here is what might be thought of as a

checkerboard approach. As can be seen in FIGs. 18-21, probe array 21 touches down on a first position, shown in FIG. 18. Thereafter, it steps to the right so that each DUT array in probe array 11 is over a DUT adjacent to the one tested in the first touchdown. Next, going from the second to the third touchdown, FIG. 19 to FIG. 20, respectively, probe array 21 steps down by one DUT and one DUT array. Finally, in FIG. 21, the probe array steps one column to the left.

With reference to FIG. 22, rectangle 23 depicts all of the four touchdowns in FIGs. 18-21. As a result of completing all four touchdowns and testing after each, all of the DUTs within rectangle 23 are tested.

Probe array 21 next steps to the adjacent rectangle for the fifth, sixth, seventh, and eighth touchdowns, those being similar to the touchdowns depicted in FIGs. 18-20 and resulting in testing of all the DUTs within that rectangle. Testing continues to each of the two lower rectangles in FIG. 22 through a total of 16 touchdowns, which concludes testing of all of the DUTs on the wafer. In FIG. 23, as in the previous two embodiments, all of the DUTs are tested and are subjected to only a single touchdown. But again there are a large number of touchdowns, namely 16, which creates a long testing period for the wafer.

Turning now to FIGs. 24-26, depicted therein is a probe array 25 constructed in accordance with the present invention. Probe array 25 includes 64 DUT arrays that touch the wafer, which has the same number of DUTs in the same configuration as was illustrated with the skipped row, skipped column, and checkerboard prior art probes. Each rhombus or diamond-shaped pattern in FIG. 26, like pattern 27, represents a different touchdown of probe array 25. As can be seen in FIG. 26, a total of nine touchdowns illustrated by the correspondingly numbered patterns, like pattern 27, are required to test each of the DUTs on the wafer. As illustrated in FIG. 27, each of the DUTs is subject to only a single touchdown. But the total number of touchdowns is only nine, which is fewer than with any of the skipped row, skipped column, or checkerboard prior art probe arrays described above. For the wafer depicted in FIG. 27, a square array (not shown) comprising eight DUT arrays by eight DUT arrays (64 total DUT arrays) requires 12 touchdowns to test all the DUTs on the wafer in FIG. 27, and a rectangular array (not shown) of four DUT arrays by 16 DUT arrays (also 64 total) requires 11 touchdowns to complete testing.

Turning now to FIG. 28, a probe array 44 includes a plurality of probe DUT arrays and is also constructed in accordance with the present invention. Like the previously described probe arrays, probe array 44 is formed on a space transformer as shown in FIG. 1. Probe array 44 is applied to DUTs on a wafer having the same DUT pattern as in FIGs. 4-6,

i.e., the same number of DUTs located in the same configuration, namely DUT pattern 32. The configuration of probe array 44, however, is different, notably as a result of an opening 46.

As is the case with the prior art probe head, the DUTs in DUT pattern 32 on the wafer are all tested in two touchdowns, the first being depicted in FIG. 29 and the second in FIG. 30. As can be seen in both FIGs. 29 and 30, in both touchdowns two DUT arrays are outside pattern 32. When a DUT array is outside the boundary, it is not opposite a DUT and therefore is not used. As can be seen in FIGs. 4 and 5, a total of four DUTs in the first touchdown and three DUTs in the second touchdown are outside the boundary.

In addition, as can be seen in the schematic chart of FIG. 31, there are far fewer DUTs exposed to double touchdowns than in the prior art FIG. 6 illustration. And this is all done with fewer DUT arrays, 161 DUT arrays in probe array 44 as contrasted with 205 DUT arrays in probe array 30. As a result, fewer tester channels are utilized, fewer DUT arrays are unutilized in each touchdown, and fewer DUTs are exposed to double touchdowns. These improvements increase efficiency and reduce the likelihood of damage resulting from multiple touchdowns.

Turning now to FIGs. 32-35, another probe array 48 is constructed in accordance with the present invention and is also for use with DUT pattern 32. But because probe head 48 has only 133 DUT arrays, as contrasted with 161 DUT arrays for probe array 44, three touchdowns are necessary. The three touchdowns illustrating the respective positions of the DUT arrays and DUTs on the semiconductor wafer are depicted sequentially in FIGs. 33, 34, and 35. As can be seen in FIG. 36, there are only four DUTs subject to a triple touchdown with 75 being subject to a double touchdown and 211 to a single touchdown with all 290 DUTs being tested. While probe array 48 results in more touchdowns per wafer and in four triple touchdowns, this may still be an optimal solution where the number of tester channels are constrained to fewer than 161.

Turning now to FIGs. 37-40, a probe array 50 is constructed in accordance with the present invention. This probe array is designed for use with a wafer having a different number of DUTs and a different configuration from the previously illustrated DUT pattern. DUT pattern 52 includes a total of 169 DUTs while probe array 50 includes a total of 85 DUT arrays. Three wafer touchdowns, depicted in FIGs. 38-40, are used to test each of the DUTs in DUT pattern 52. As can be seen in FIG. 41, while three touchdowns are used, no DUTs are subject to triple touchdowns and only 31 DUTs are subject to double touchdowns with 138 DUTs being subject to only a single touchdown.

In FIGs. 42-44, another probe array 54—also constructed in accordance with the present invention—is used to test the same DUT pattern 52 as illustrated in FIGs. 38-41. Here, however, there are a total of 95 DUT arrays in probe array 54. The additional number of DUT arrays permits testing of all the DUTs in DUT pattern 52 with only two touchdowns on the wafer, illustrated in FIGs. 43 and 44, as opposed to three touchdowns used by probe array 50 and illustrated in FIGs. 38-40. In FIG. 45, it can be seen that only six of the DUTs in DUT pattern 52 are subject to double touchdowns with the remaining DUTs receiving a only single touchdown. While these results are superior to those obtained by probe array 50 for the same DUT configuration, recall that probe array 50 included only 85 DUT arrays and thus might be an optimal solution if constraints, such as limited number of tester channels, prevent use of a probe array like probe array 54, which includes 95 DUT arrays.

In summary, the probe patterns disclosed above allow for fewer touchdowns per wafer, lower multiple touchdowns per DUT, reduced number of tester channels required and reduced stepping distance between touchdowns, thereby reducing cost and processing time, and increasing quality of the semiconductor dies being tested. In one aspect of the invention, the inventive patterns can be thought of as combinations of one or more discontinuities such as openings, indentations protuberances, and islands. For example, an opening 46 and an indentation 56 are shown in FIG. 28, a protuberance 58 is shown in FIG. 32, and an island 60 is shown in FIG. 42. Note that the two DUT arrays 62 at the top of pattern 44 shown in FIG. 28 are not considered protuberances since they are merely filling out the top arcuate portion of the generally oval shape of pattern 44. Rather, what is meant by protuberance and indentation is a local discontinuity or deviation from the general shape of the perimeter of the pattern.

Other advantageous patterns (not shown) could include multiple islands each having many DUT arrays with no main or coherent perimeter in the overall probe head pattern, with one or more islands having their own openings, indentations and /or protuberances.

In another aspect of the invention, a symmetrical pattern, such as a parallelogram or other symmetrical pattern could include DUT arrays in lines that are not parallel with any of the horizontal or vertical lines of DUTs on a semiconductor wafer.

It is important to realize that the patterns shown can be built up out of multiple probe heads, such as described in U.S. Patent No. 5,806,181, which is incorporated in its entirety herein by reference. It also is the case that other methods of probe card or wafer contactor construction, including the use of tungsten needles, buckling beam or "cobra" like contacts, MEMs structures, membrane probes or the other suitable structures can be arranged in similar patterns with similar benefits. The patterns are not limited to use on probe heads testing

electronic dies on silicon wafers, but can be applied to any contactor having an array of contacts for making repeatable contact with devices for any purpose, such as for "burn-in" or testing.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variation coming within the spirit and scope of the following claims.

CLAIMS

1. A contactor for testing devices formed on a semiconductor wafer comprising a probe array for making contact with pads formed on the devices, said probe array including continguous DUT arrays disposed around an opening in the probe array, the opening being over at least one device when the probe array contacts the pads.

2. The contactor of claim 1 wherein said probe array include at least one additional opening in the DUT arrays that is opposite at least one device when the probe array contacts the pads.

3. The contactor of claim 1 wherein said contiguous DUT arrays form a generally annular pattern.

4. The contactor of claim 1 wherein said opening in the DUT arrays is bounded by 4 DUT arrays.

5. A probe head for testing devices arranged in a substantially uniform grid on a semiconductor wafer, said probe head comprising:

a plurality of probes formed in DUT arrays that are arranged substantially in a grid having the same configuration as the device grid; and

a space formed amid the DUT arrays that is opposite at least one device when the probes touch the devices.

6. The probe head of claim 5 wherein the probe head includes at least one additional space that is opposite at least one device when the probes touch the devices.

7. The probe head of claim 5 wherein said DUT arrays form a generally annular pattern.

8. The probe head of claim 5 wherein said space is bounded by 4 DUT arrays.

9. An apparatus for testing devices formed on a semiconductor wafer comprising probe DUT arrays arranged in a substantially annular pattern.

10. The apparatus of claim 9 wherein said annular pattern includes an opening and wherein said pattern includes at least one additional opening.

11. An apparatus for testing devices formed on a semiconductor wafer comprising probe DUT arrays arranged in a pattern that includes at least one opening contained within the perimeter of the pattern in which there is no probe DUT array.

12. The apparatus of claim 11 wherein said probe array pattern includes at least one additional opening contained within the perimeter of the pattern in which there is no probe DUT array

13. The apparatus of claim 11 wherein said pattern is generally annular.

14. The apparatus of claim 11 wherein said opening is bounded by 4 DUT arrays.

15. An apparatus for testing devices formed on a semiconductor wafer comprising probe DUT arrays arranged in a pattern, the pattern having a perimeter with at least one local discontinuity.

16. The apparatus of claim 15 wherein the local discontinuity is a protuberance of at least one DUT array.

17. The apparatus of claim 16 wherein the protuberance is formed by a single DUT array.

18. The apparatus of claim 16 wherein the protuberance has a minimum width and extends outwardly from the perimeter more than twice the minimum width.

19. The apparatus of claim 16 wherein the perimeter includes at least one additional protuberance.

20. The apparatus of claim 15 wherein the local discontinuity is an indentation of at least one DUT array.

21. The apparatus of claim 20 wherein the indentation is formed by a single DUT array.

22. The apparatus of claim 20 wherein the indentation has a minimum width and extends inwardly from the perimeter more than twice the minimum width.

23. The apparatus of claim 20 wherein the perimeter includes at least one additional indentation.

24. The apparatus of claim 15 wherein said pattern is symmetrical.

25. The apparatus of claim 24 wherein said pattern is substantially in the shape of a parallelogram.

26. The apparatus of claim 25 wherein said pattern is substantially in the shape of a rhombus.

27. An apparatus for testing devices arranged on a semiconductor wafer in a pattern that forms substantially parallel horizontal lines and parallel vertical lines, said apparatus comprising probe DUT arrays arranged in a symmetrical pattern, the pattern having at least one perimeter that is not parallel with any of the lines of devices when the probe DUT arrays touch the devices.

28. The apparatus of claim 27 wherein said pattern is substantially in the shape of a parallelogram.

29. The apparatus of claim 28 wherein said pattern is substantially in the shape of a rhombus.

30. A method of testing semiconductor devices on a wafer comprising the steps of:

providing an array of probes having at least one discontinuity therein;

bringing the array into contact with the wafer such that a first portion of the semiconductor devices to be tested are contacted by some of the probes and a second portion of the devices are not contacted by the probes but are opposite in position to the at least one discontinuity;

moving the wafer out of contact with the array of probes;

moving the wafer laterally with respect to the array of probes;

bringing the array into contact with the wafer such that at least some of the second portion of the devices are contacted by some of the probes.

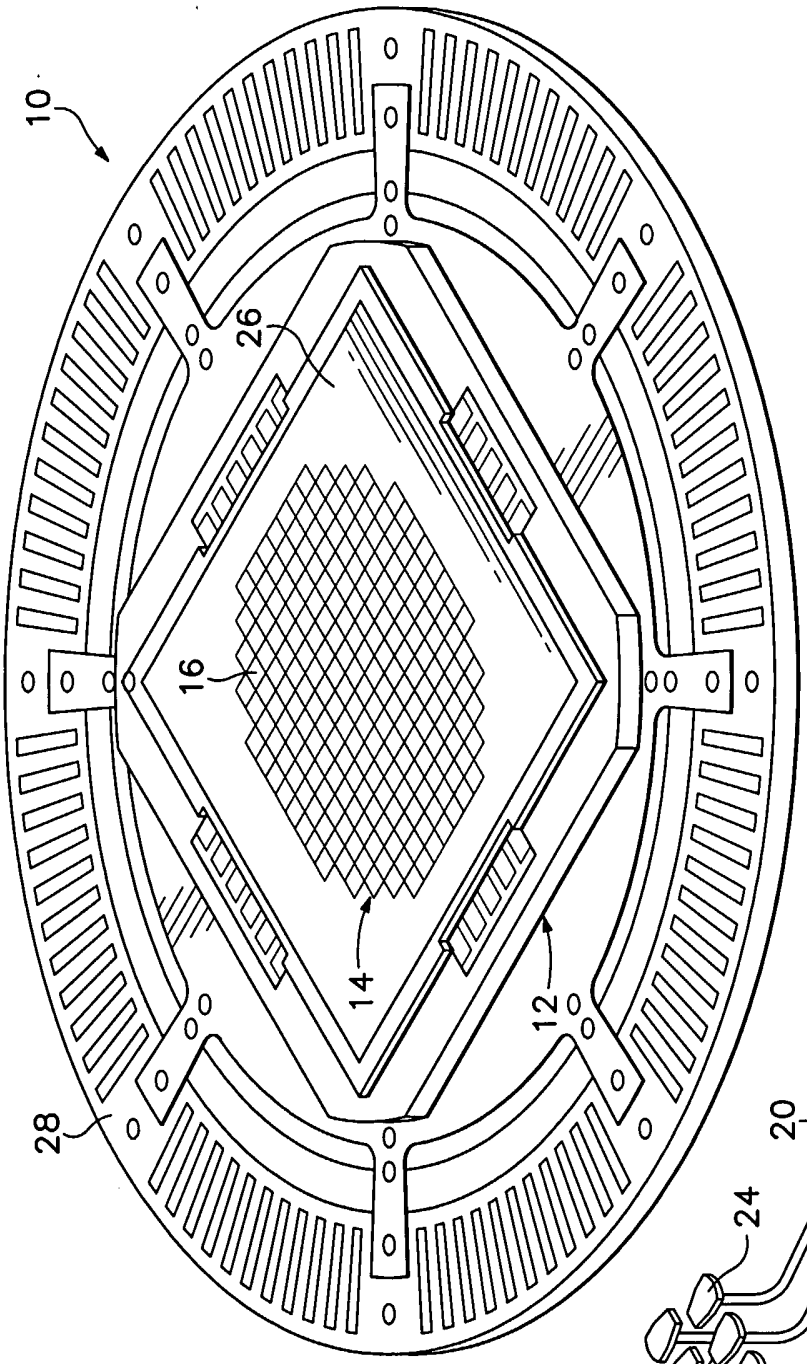


FIG.1

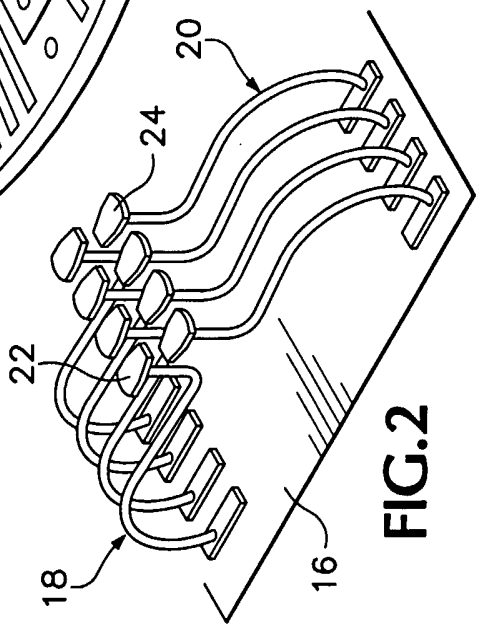


FIG.2

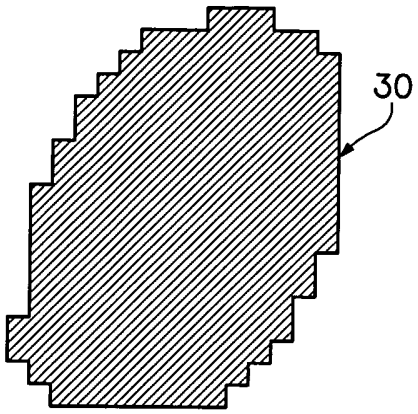


FIG.3
PRIOR ART

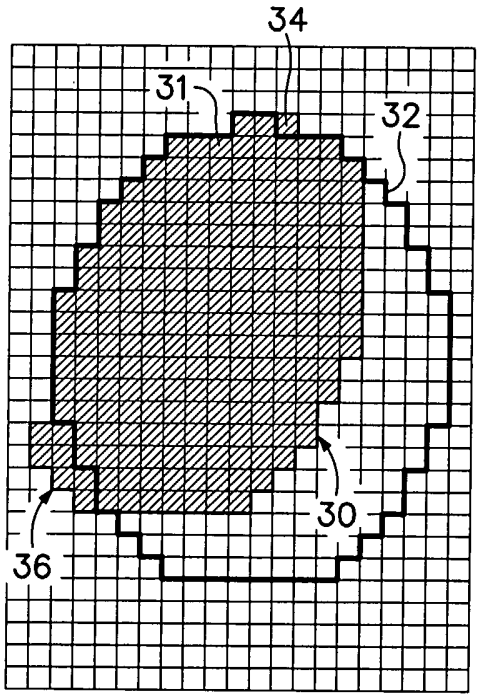


FIG.4
PRIOR ART

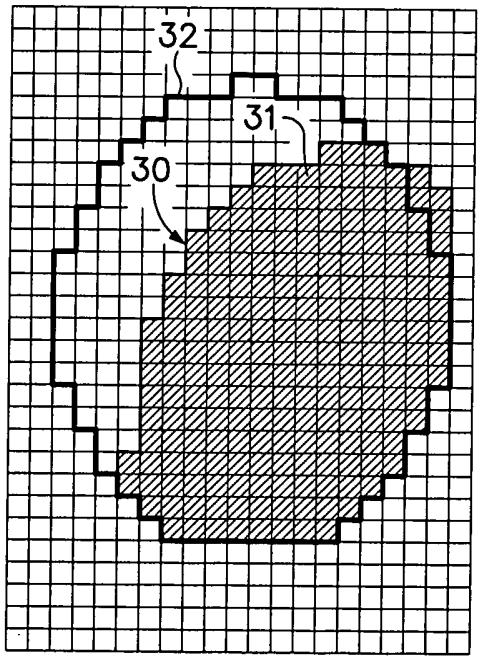


FIG.5
PRIOR ART

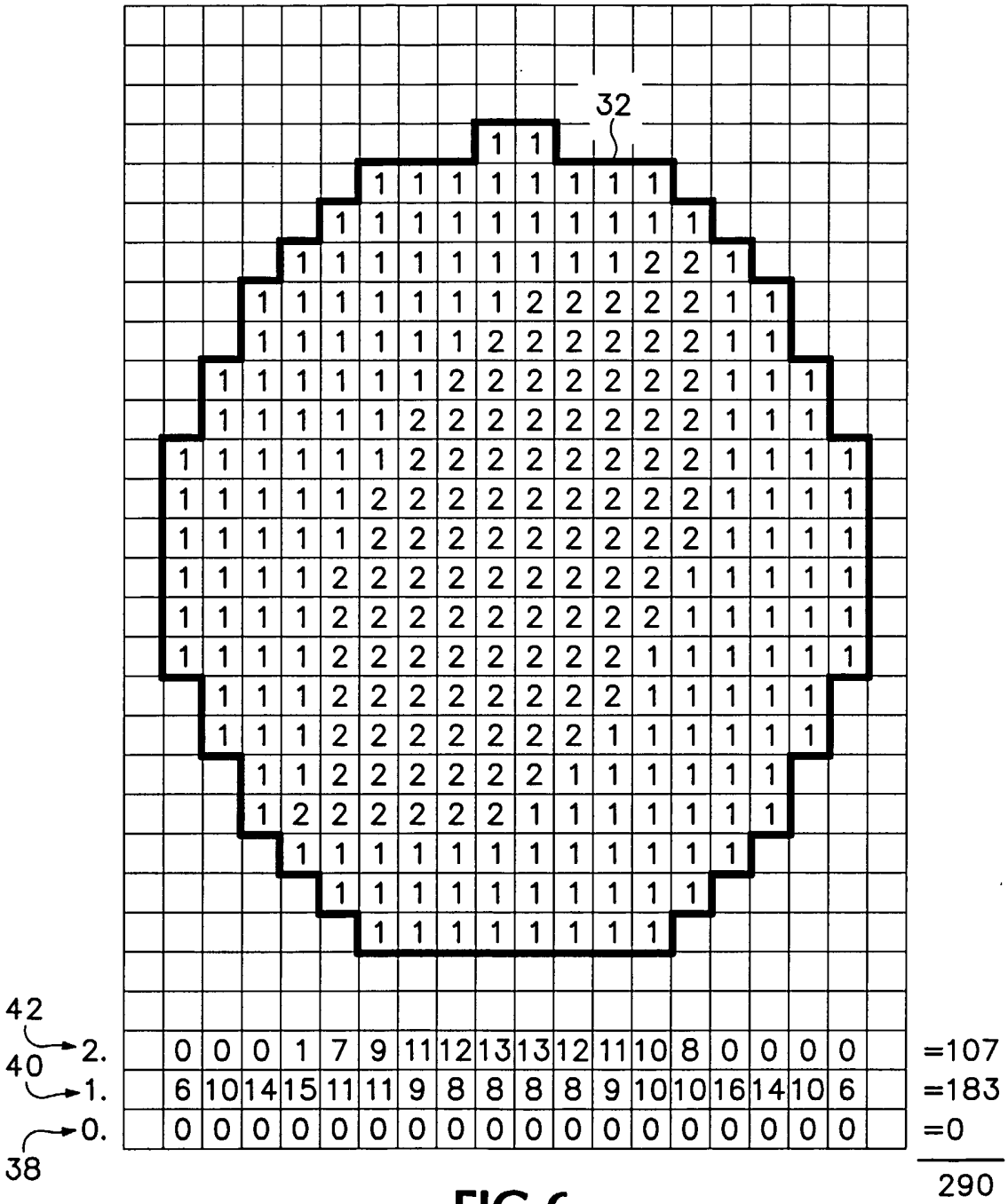
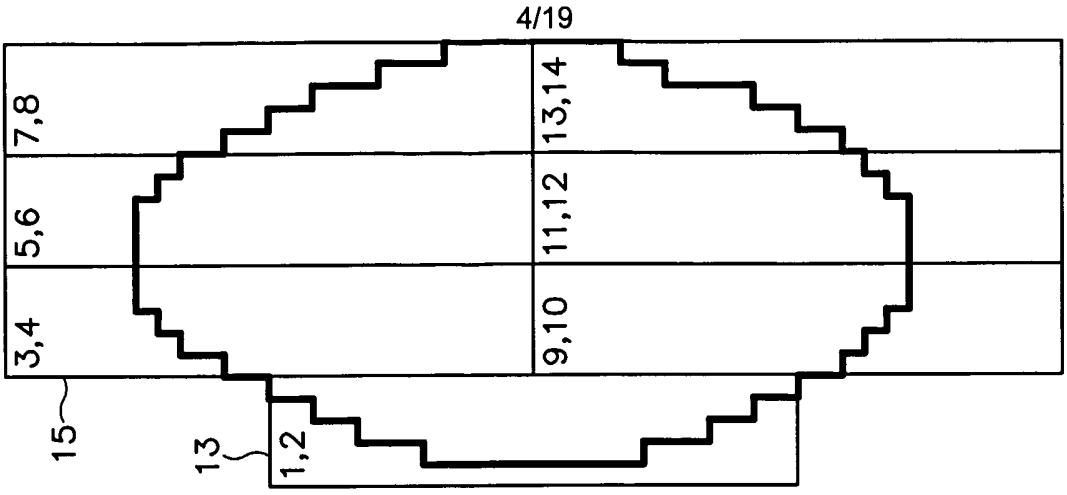


FIG.6
PRIOR ART



PRIOR ART **FIG.10**

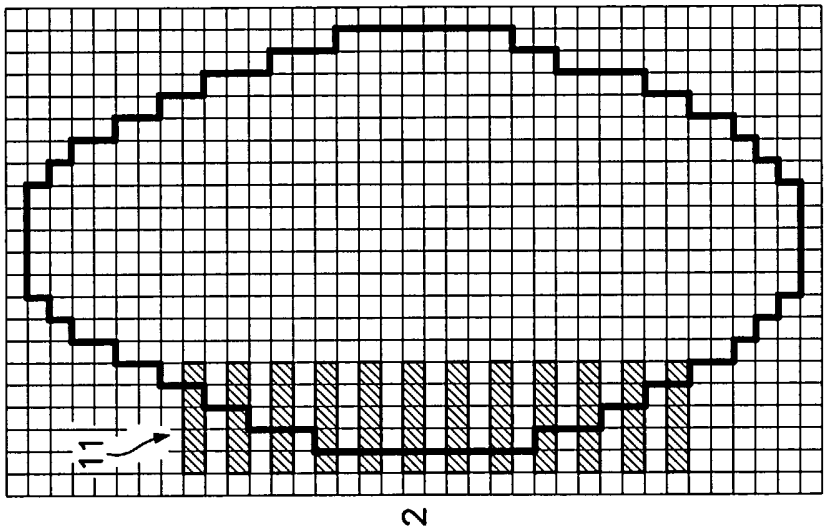


FIG.9
PRIOR ART

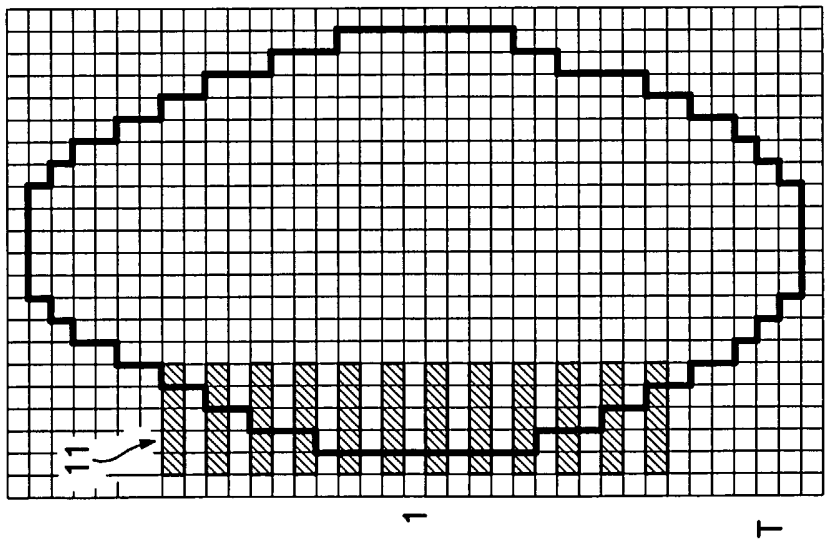


FIG.8
PRIOR ART

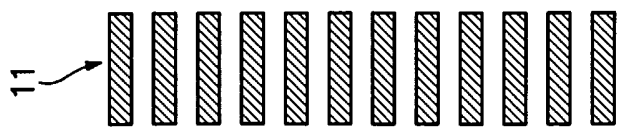


FIG.7
PRIOR ART

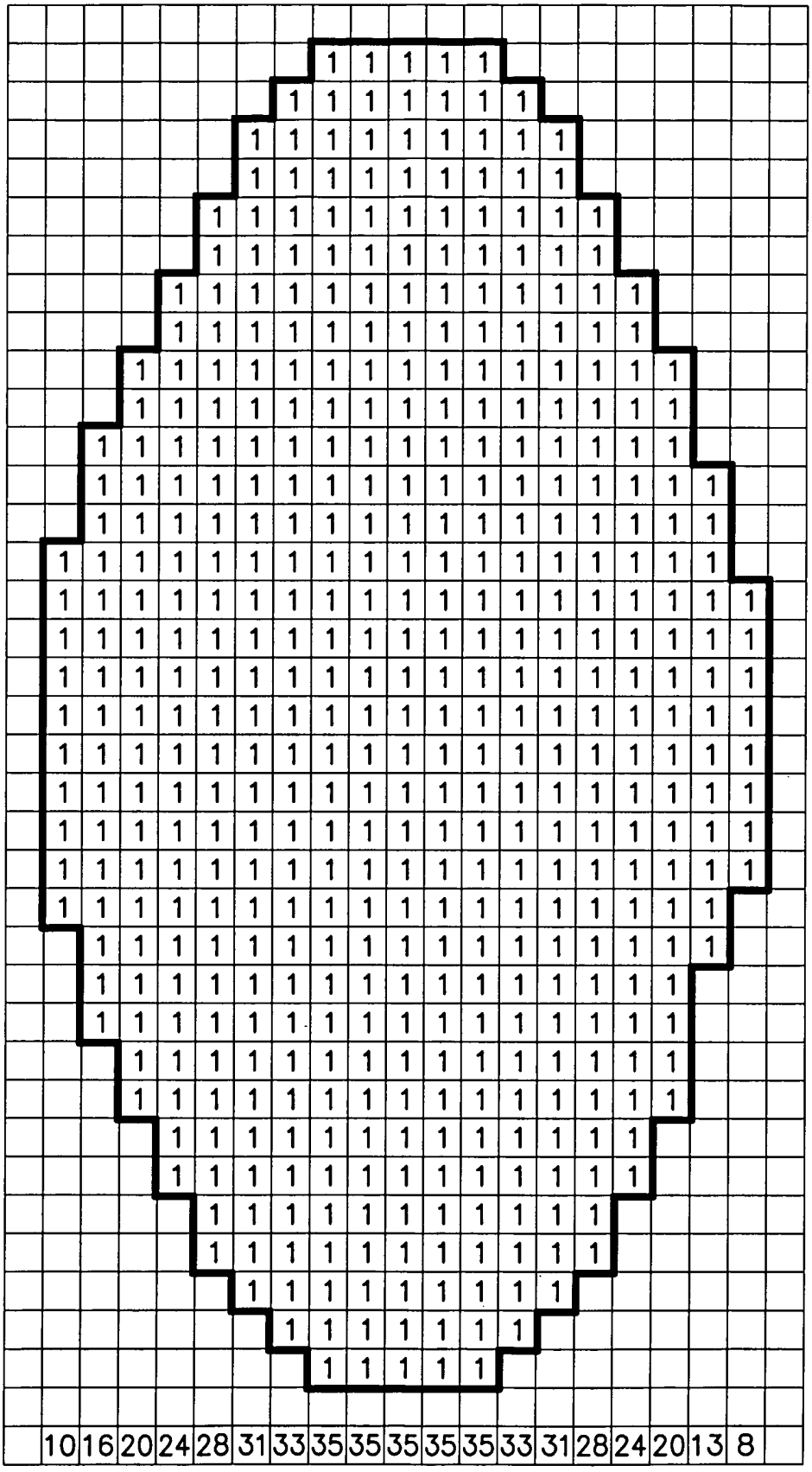


FIG.11 PRIOR ART

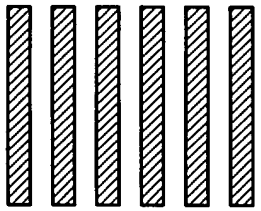


FIG.12
PRIOR ART

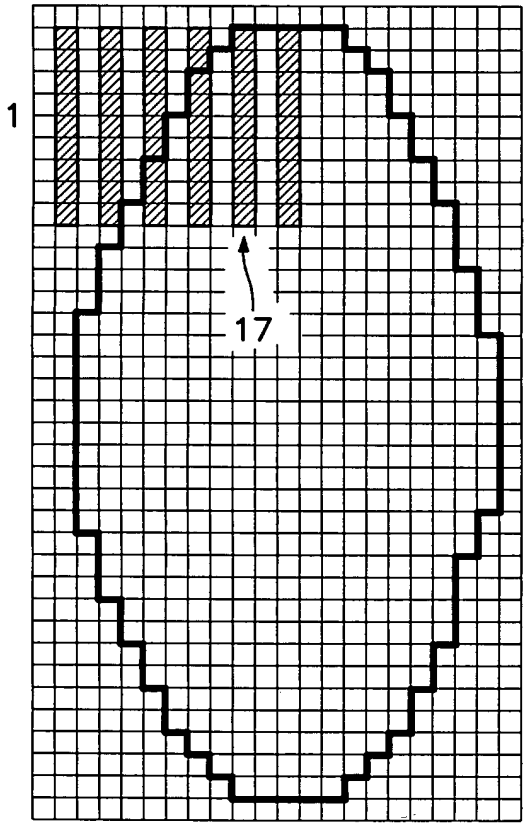


FIG.13 PRIOR ART

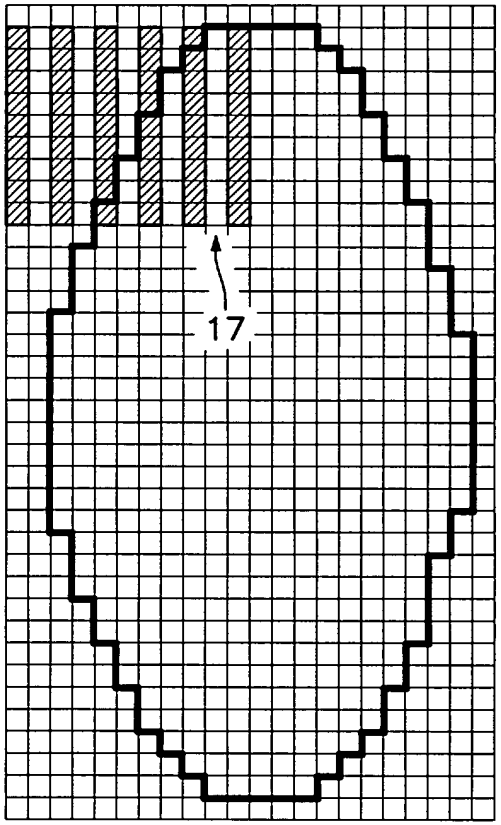


FIG.14 PRIOR ART

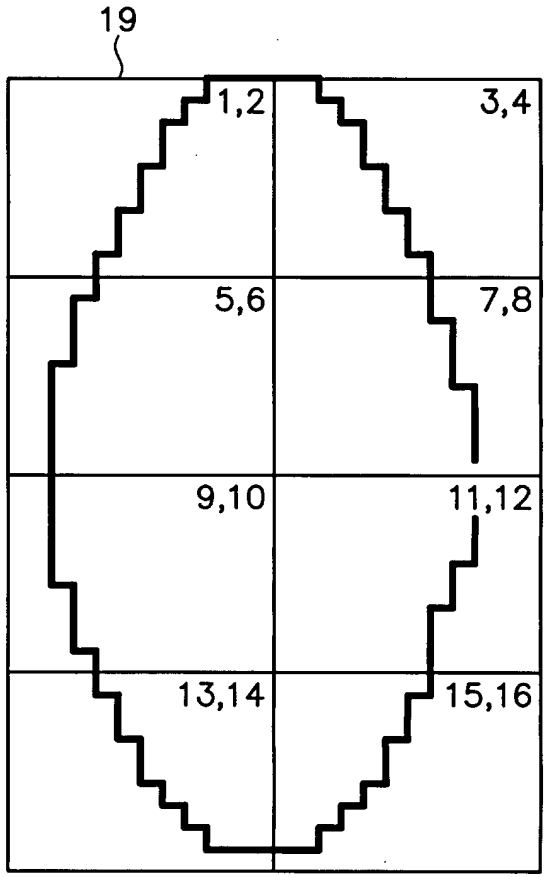


FIG.15
PRIOR ART

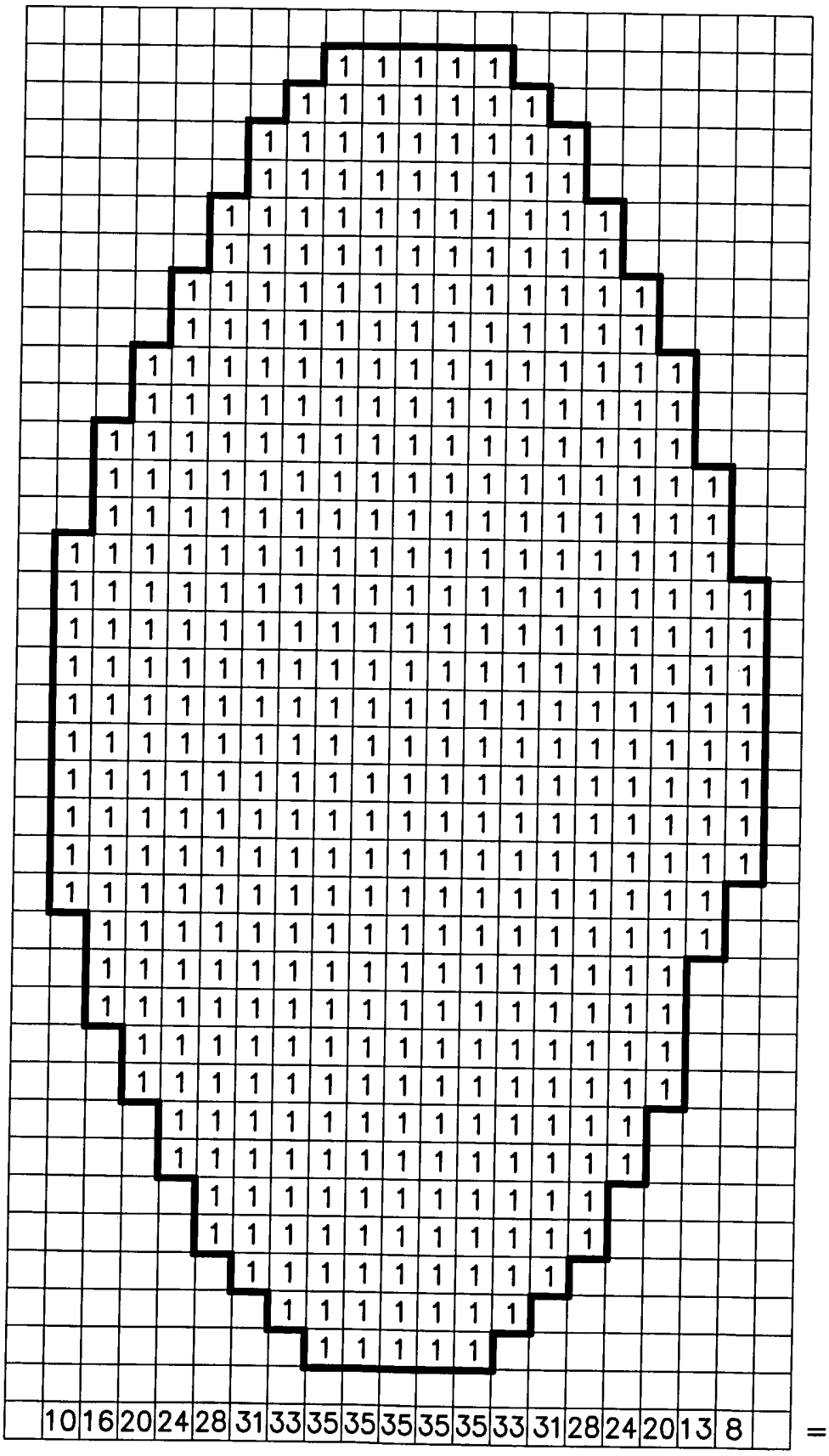


FIG.16 PRIOR ART

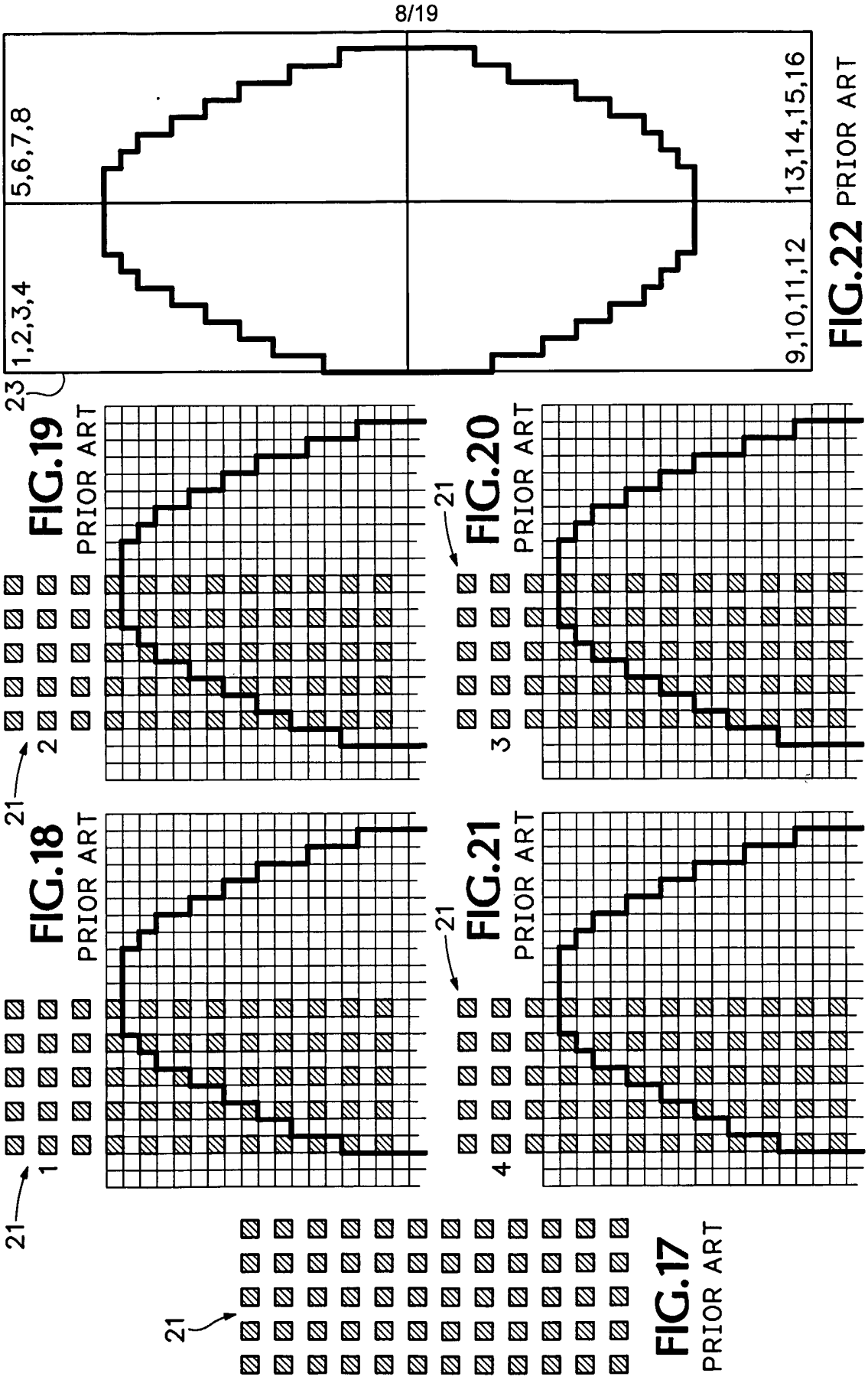


FIG.22 PRIOR ART

FIG.19 PRIOR ART

FIG.20 PRIOR ART

FIG.18 PRIOR ART

FIG.21 PRIOR ART

FIG.17 PRIOR ART

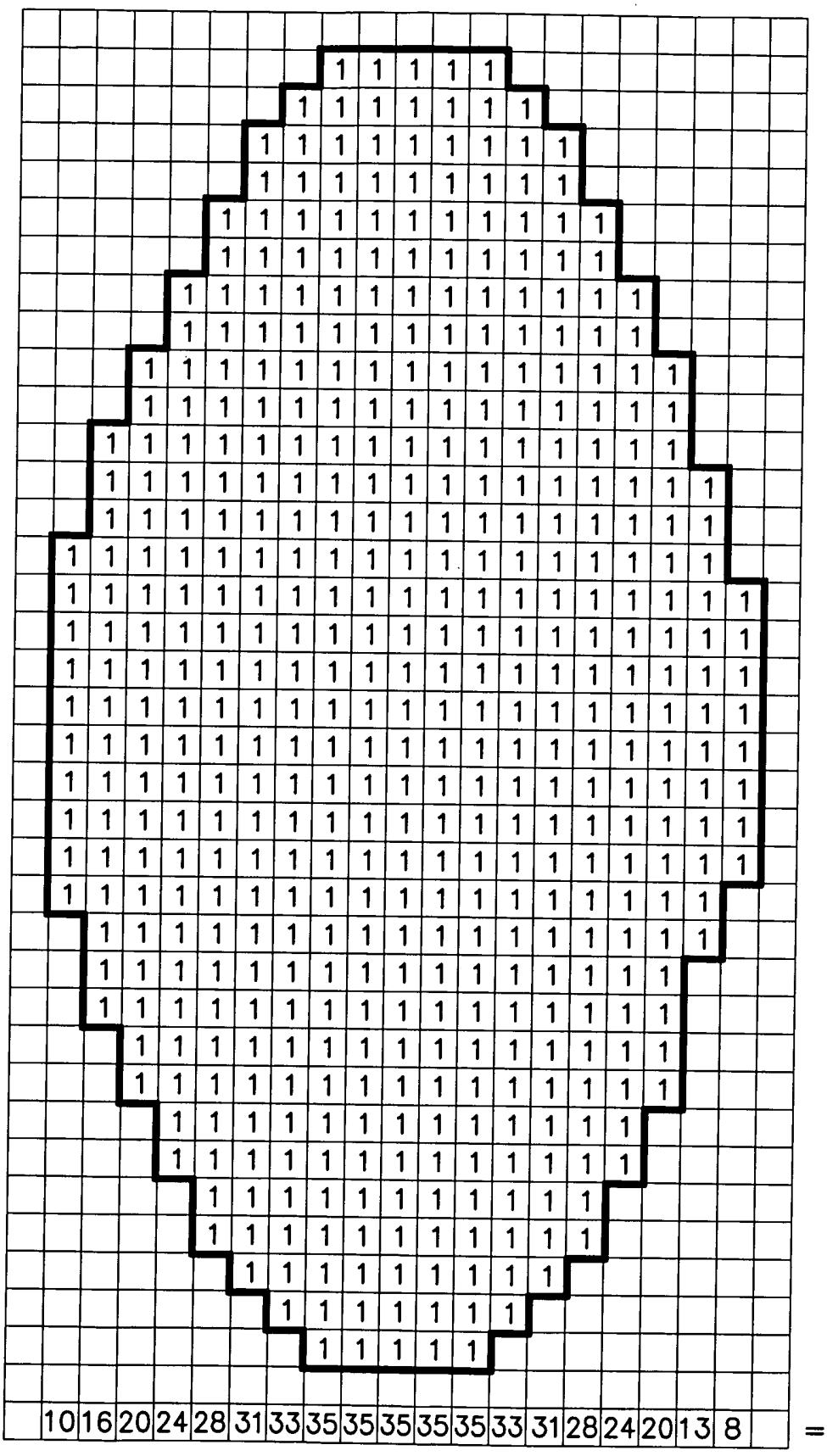


FIG.23 PRIOR ART

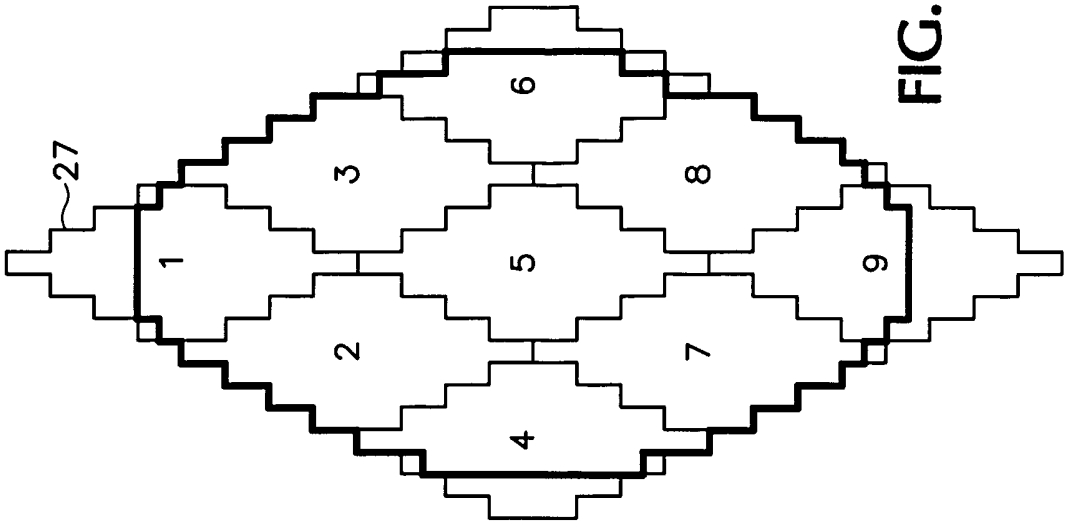


FIG.26

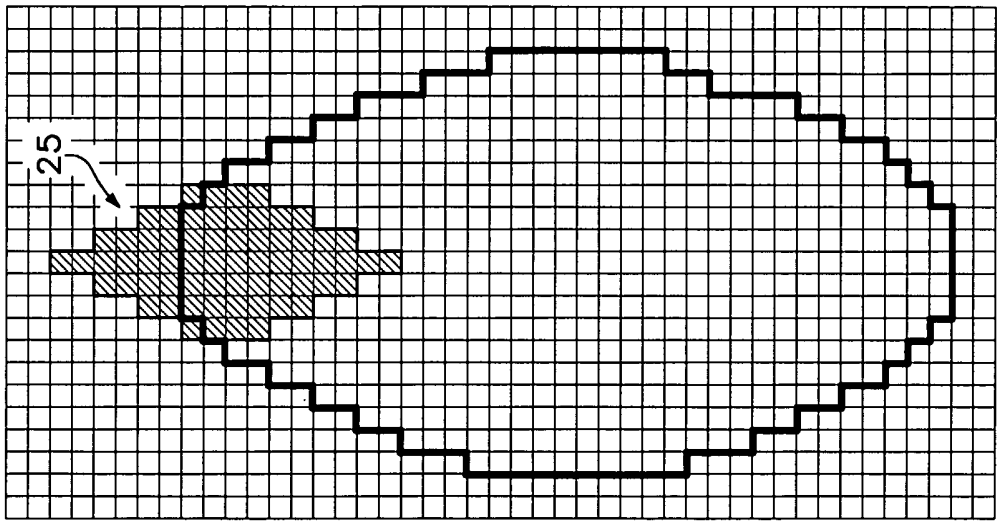


FIG.25

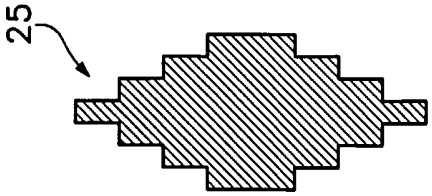
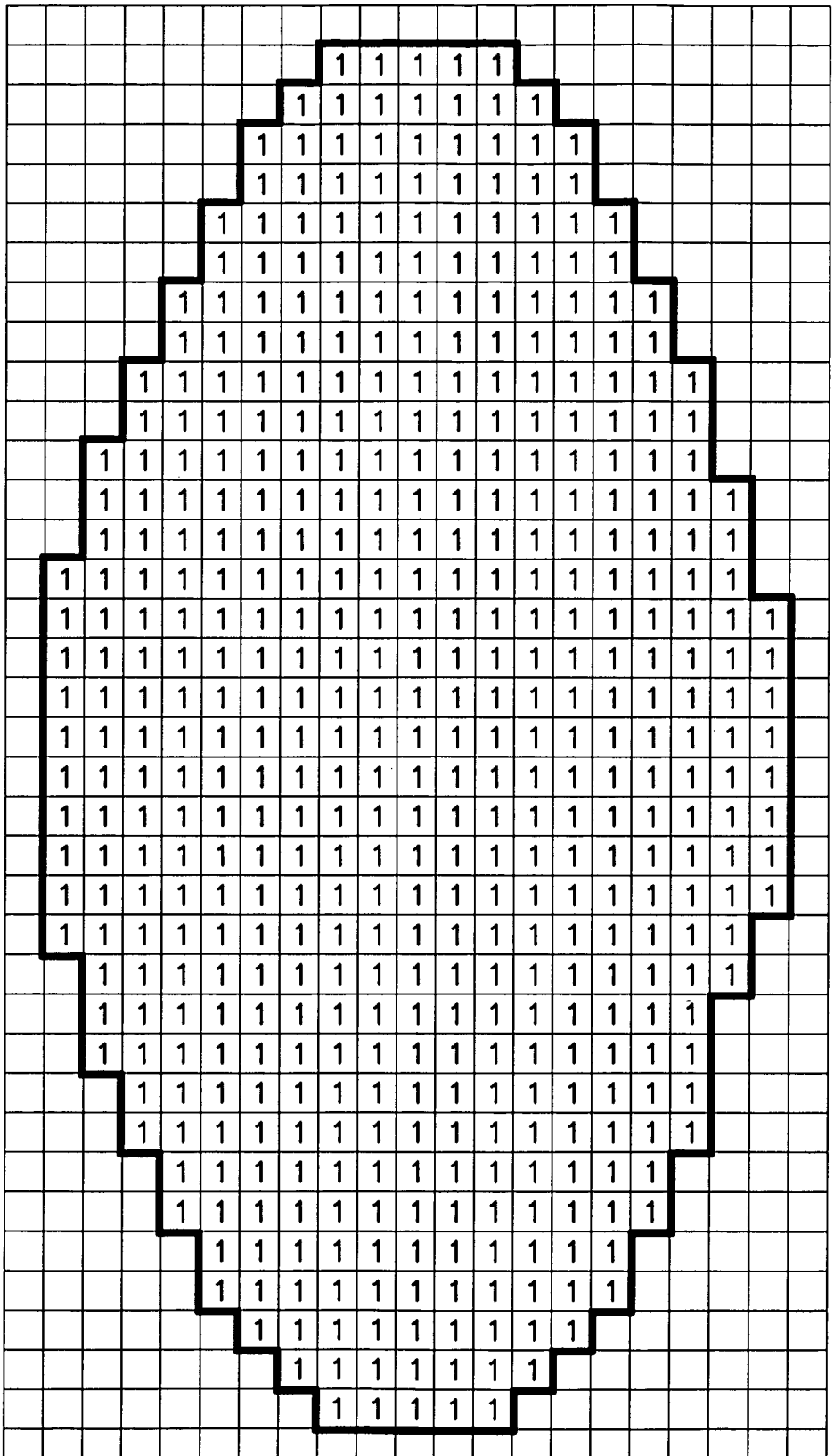


FIG.24



1. 10 16 20 24 28 31 33 35 35 35 35 35 33 31 28 24 20 13 8 =494

FIG.27

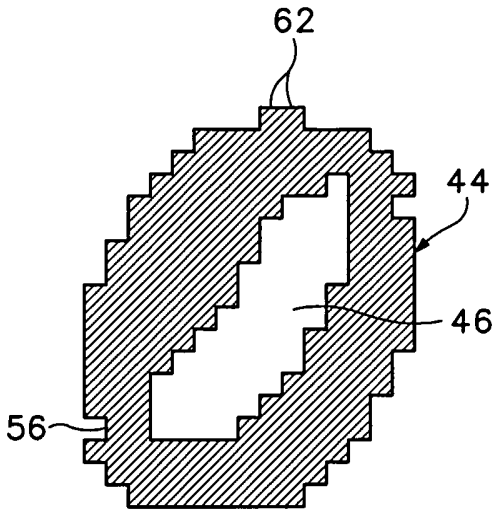


FIG.28

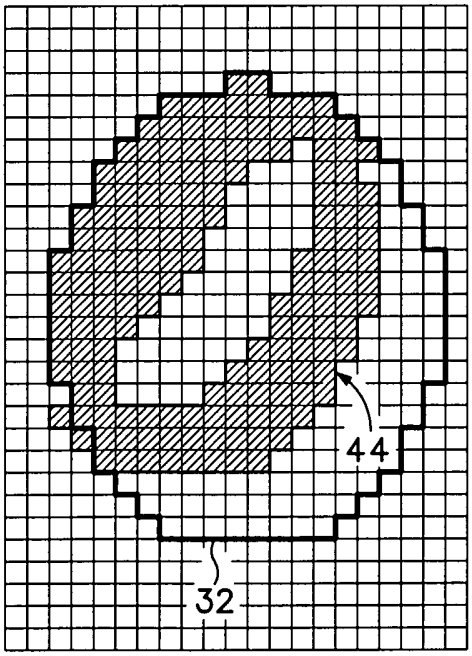


FIG.29

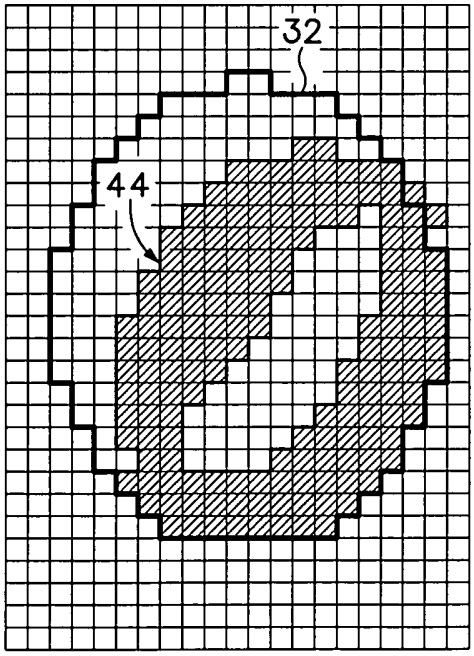
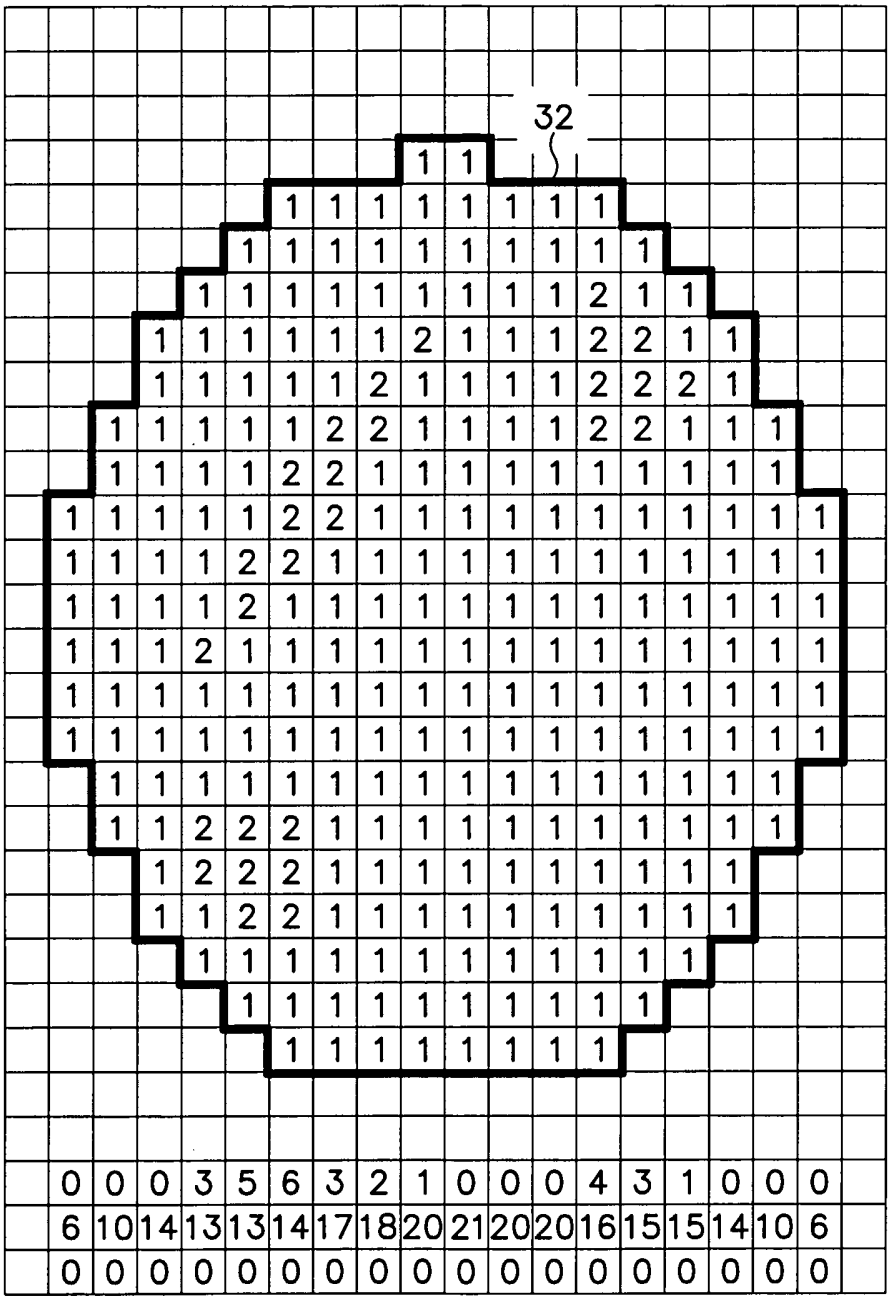


FIG.30



2.		0	0	0	3	5	6	3	2	1	0	0	0	4	3	1	0	0	0	=28
1.		6	10	14	13	13	14	17	18	20	21	20	20	16	15	15	14	10	6	=262
0.		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	=0
																				290

FIG.31

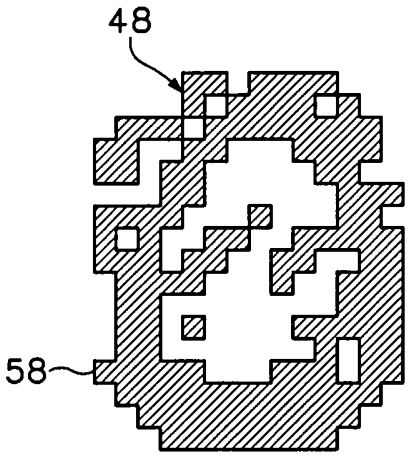


FIG.32

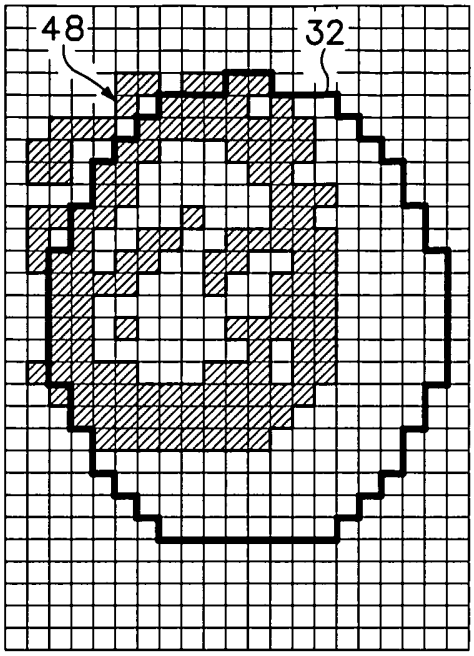


FIG.33

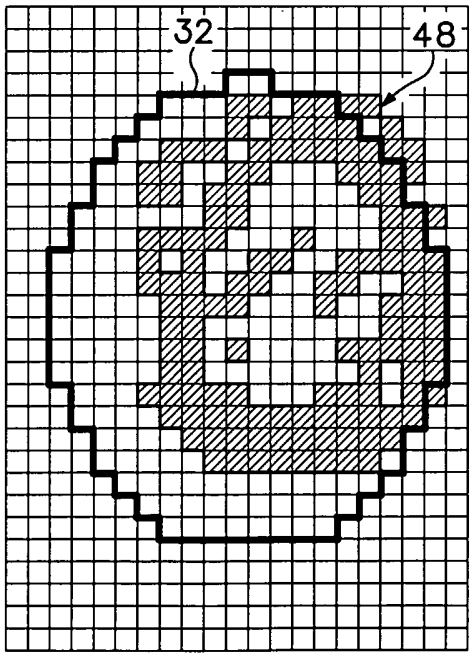


FIG.34

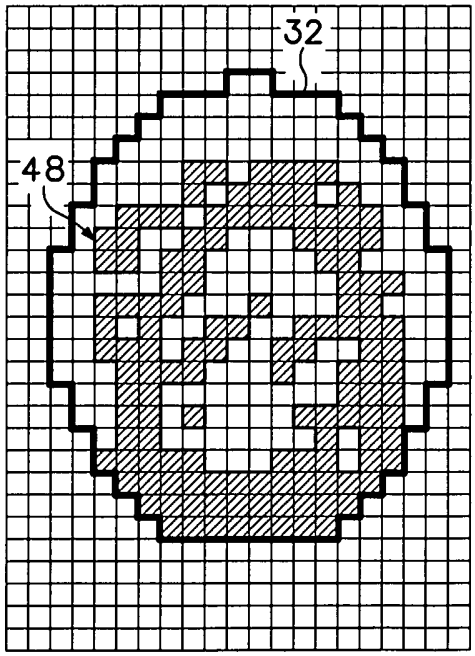
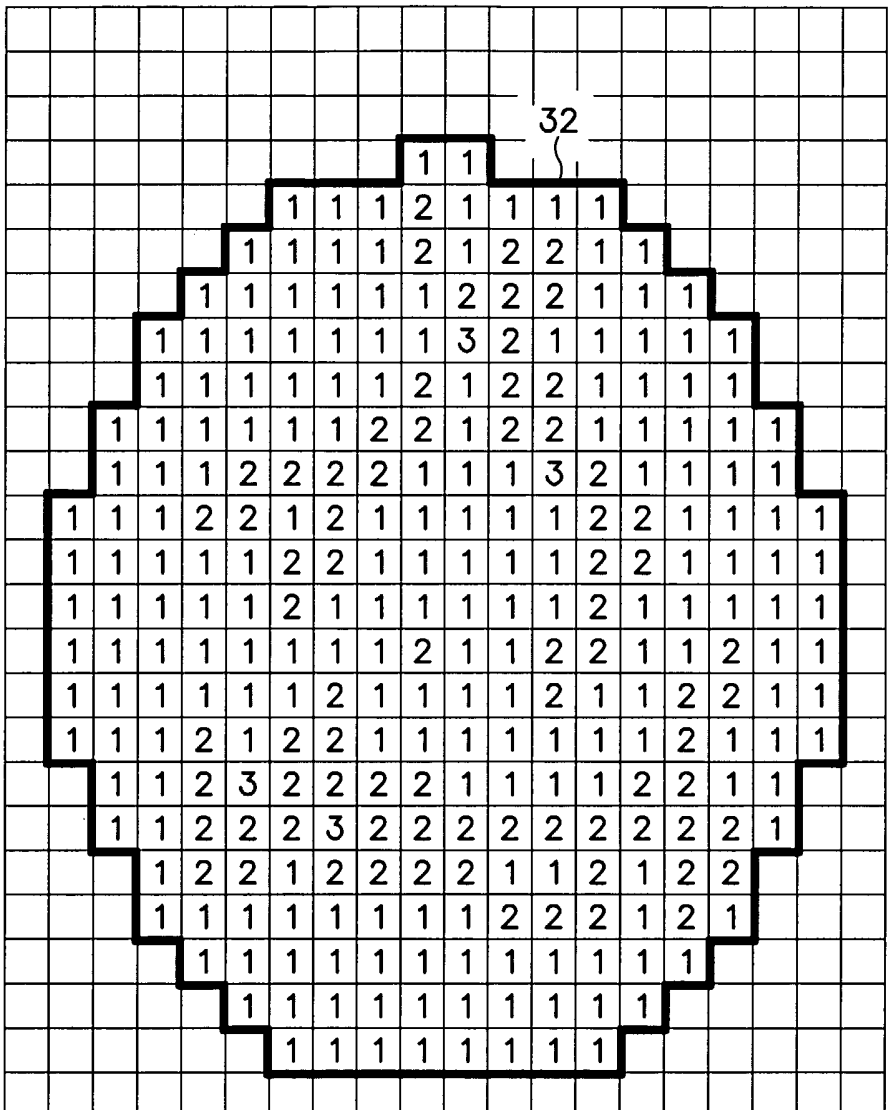


FIG.35



3.		0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	=4
2.		0	0	0	5	4	6	7	5	8	3	7	8	8	4	6	4	0	0	=75
1.		6	10	14	11	13	14	12	15	13	17	13	11	12	14	10	10	10	6	=211
0.		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	=0
																				290

FIG.36

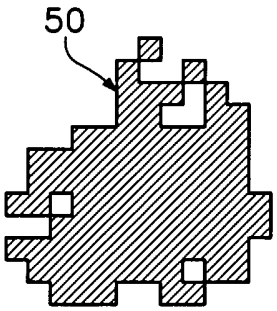


FIG.37

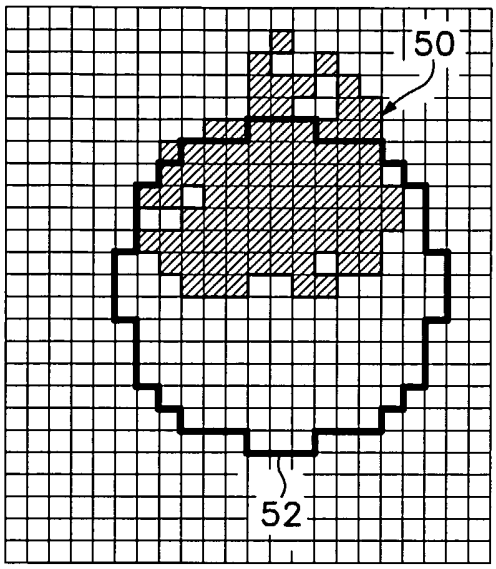


FIG.38

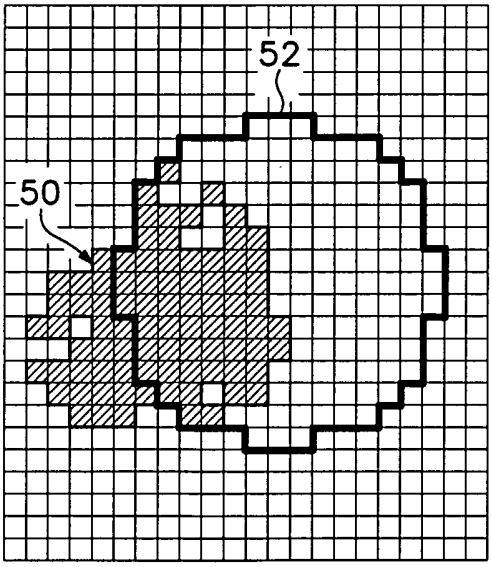


FIG.39

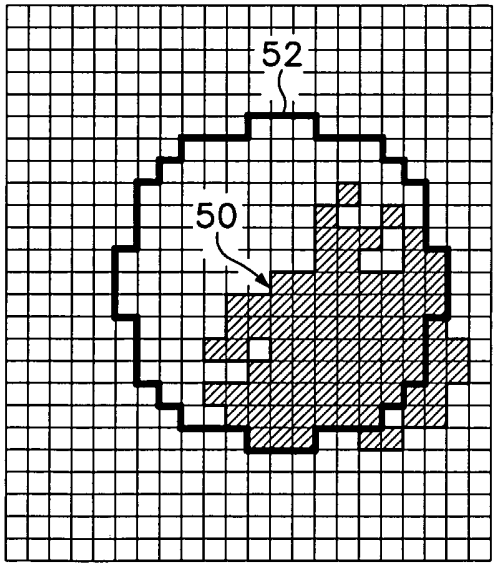
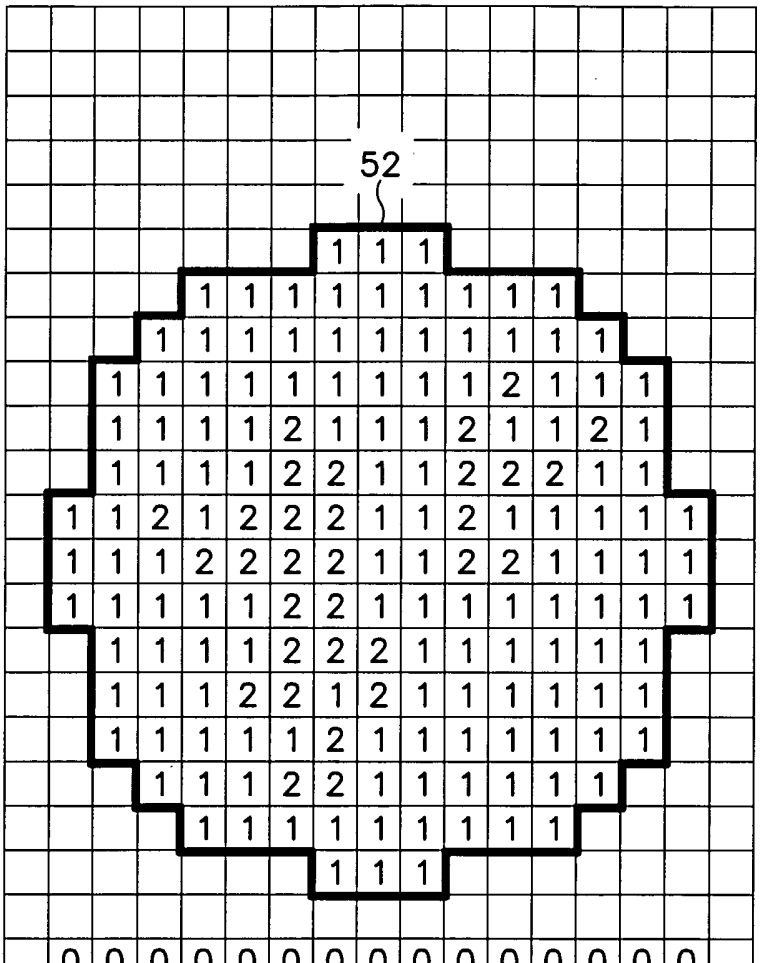


FIG.40



3.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		=0
2.	0	0	1	1	3	8	7	2	0	4	3	1	1	0	0		=31
1.	3	9	10	12	10	5	8	13	15	9	10	12	10	9	3		=138
0.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		=0
																	169

FIG.41

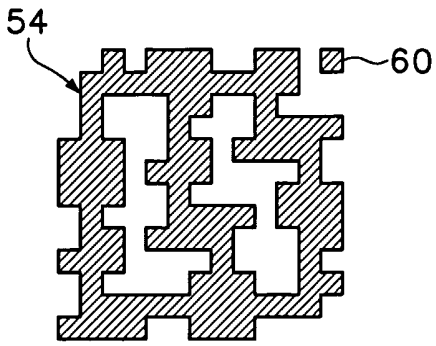


FIG.42

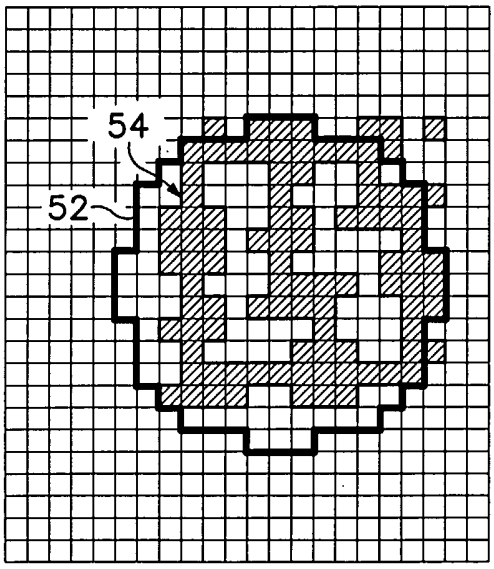


FIG.43

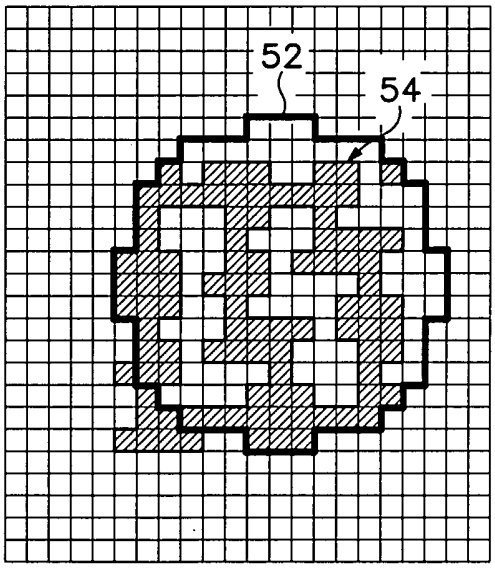
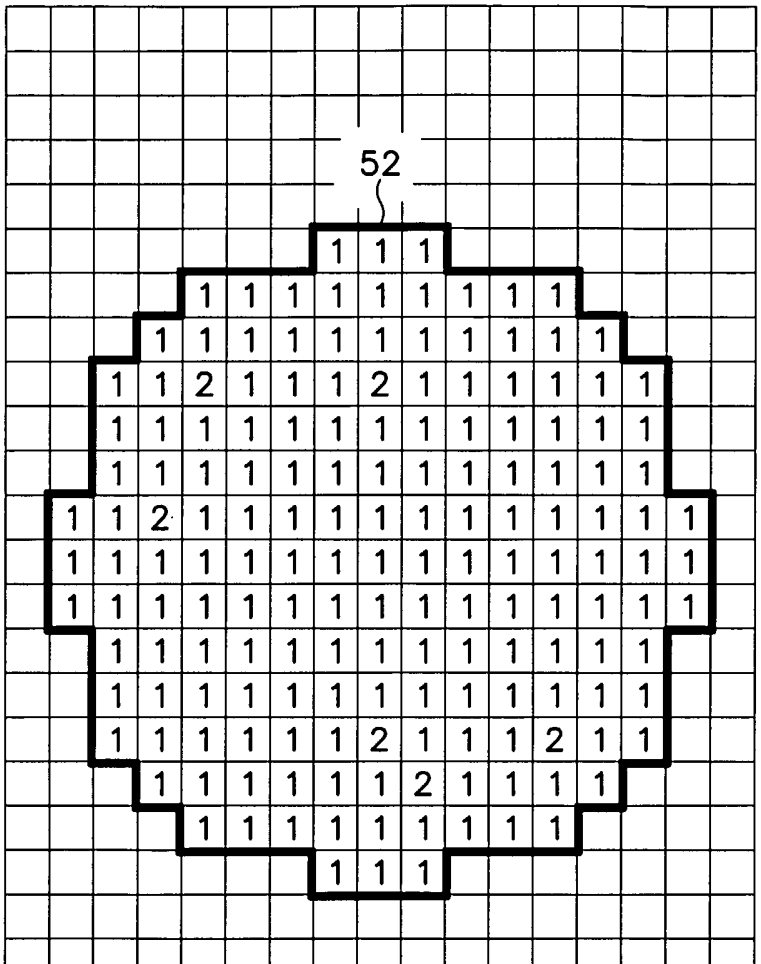


FIG.44



2.		0	0	1	1	0	0	0	2	1	0	0	1	0	0	0	=6
1.		3	9	10	12	13	13	15	13	14	13	13	12	11	9	3	=163
0.		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	=0
																	169

FIG.45