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[54] **PULSATING TIMER**

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[51] **Int. Cl....H03k 17/28,** H03k 17/30, H03k 17/72

[58] **Field of Search** ..... 307/252 F, 252 J, 283, 284, 307/268, 293, 227; 328/186; 317/141 S

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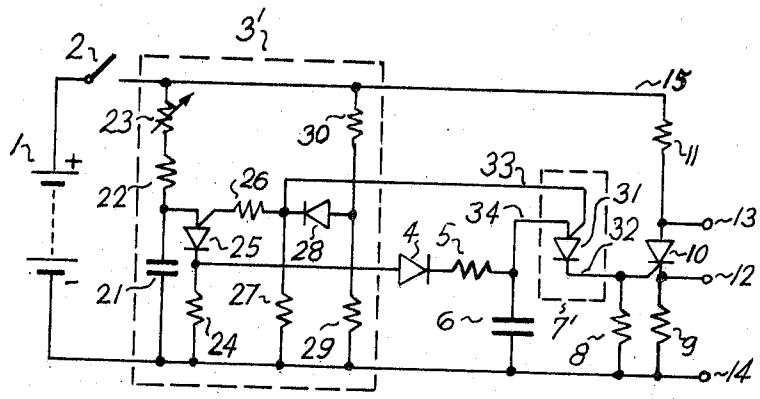
[57] **ABSTRACT**

A pulsating timer consists of two timers — first one produces repeatedly a short pulse at the end of its timing period, the second one produces a pulse at the end of the desired time period. Pulses from the first timer are fed through a diode and a resistor into a storage capacitor. Since the storage capacitor is charged with current pulses at time intervals as first timer dictates, many pulses are needed to charge it sufficiently to trigger a voltage sensing means. Said resistor, storage capacitor, and voltage sensing means form said second timer which will produce its first pulse after a long time interval and in synchronism with said first timer. Both timers are temperature compensated to assure longer and more accurate time intervals.

2 Claims, 3 Drawing Figures



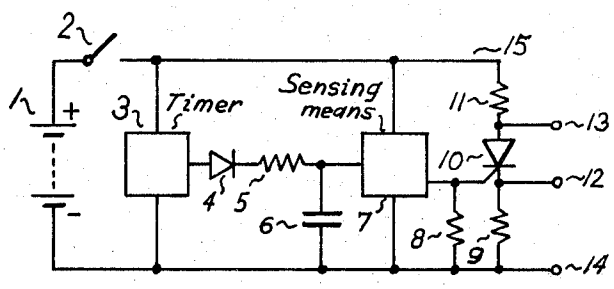


Fig. 1.

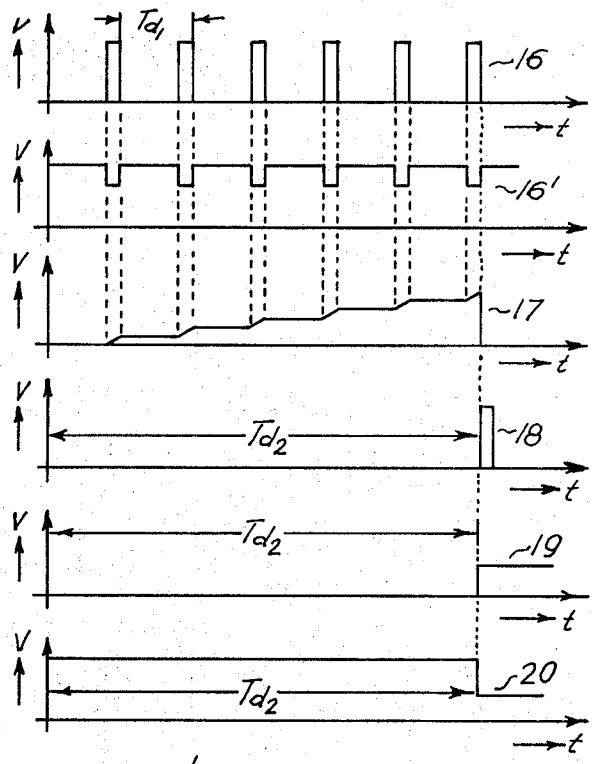


Fig. 2.

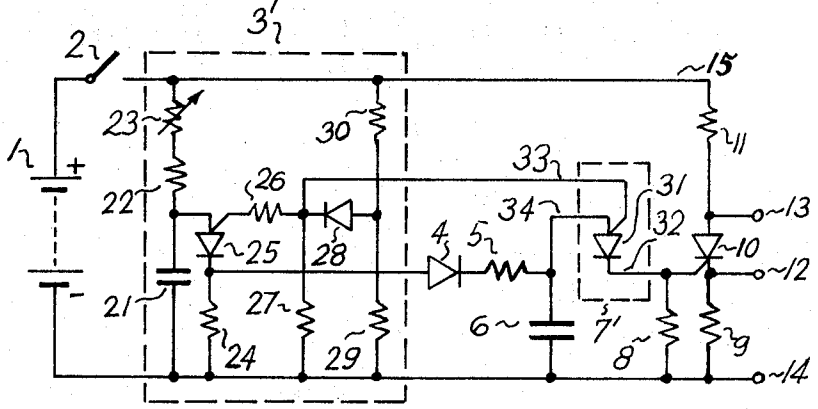


Fig. 3.

PULSATING TIMER

DETAILED DESCRIPTION OF OPERATION

The present invention relates to timing devices and more particularly to timing devices able to produce accurate and reliable long time intervals by use of solid state components.

The present and previous art devices are, generally, of the CR type where a storage capacitor is charged either continually or periodically when current pulses are produced and then stored in the capacitor.

The first type had the following disadvantages: Timing limited to maximum 10 minutes, limited accuracy, ambient temperature dependency, limited sensitivity, bulky and expensive timing capacitor, large value timing resistor, possibility of false triggering etc. The second type has complex circuitry, limited timing range, ambient temperature dependency, high production cost etc.

Objectives of the present invention were:

To produce adjustable time intervals of 1 hour and longer, over wide ambient temperature range,

timing capacitor to be about 1 microfarad, timing resistor not larger than 10 megohms,

simple circuit (small number of components),

inexpensive for production,

immune to false triggering,

sensitive,

compensated for ambient temperature change etc.

My belief is that all of these objectives were achieved thus, that this invention is an improvement over the previous art.

Referring to the drawings:

FIG. 1 represents the invention as a block diagram

FIG. 2 represents time diagrams involved,

FIG. 3 is an example of preferred embodiment.

Referring now to FIG.1 of the present invention in pulsating timers, note a DC source designated **1**, a power switch designated **2**, timer designated **3**, inhibiting diode designated **4**, current limiting resistor designated **5**, storage capacitor designated **6**, voltage sensing means designated **7**, gate resistor designated **8**, cathode resistor designated **9**, silicon Controlled Rectifier (SCR) designated **10** and having anode resistor designated **11**, terminals designated **12** and **13**, common lead designated **14** and the supply lead designated **15**. Reference to FIG.2 will be made as needed.

Operation is in the following manner: After switch **2** is closed DC source **1** supplies the power to timer designated **3**, which starts its timing interval T_{d1}. At the end of T_{d1} a positive pulse is produced as indicated by **16** in FIG.2. After each successive time interval T_{d1} a pulse is being generated, partially passed by the diode **4** and resistor **5** and stored in capacitor **6**. Initially, potential acrosss capacitor **6** is zero. Each pulse will store a certain charge in the capacitor causing potential across it to rise in increments as indicated by **17** in FIG.2. During time interval between pulses charged capacitor **6** reverse — biases the diode **4** rendering it nonconductive. Therefore, capacitor **6** can not be discharged through diode **4**, nor through voltage sensing means **7**. Its potential will rise in small increments until threshold potential of the voltage sensing means is reached. At that instant voltage sensing means starts conducting heavily causing quick discharge of capacitor **6**. The treshold potential can be reached and a pulse produced only after many time intervals T_{d1} forming thus, a long

time interval T_{d2} as indicated by **18** in FIG.2. Charge from capacitor **6** is fed through voltage sensing means **7**, for example, to the gate electrode of an SCR designated **10** triggering it into conduction. Wave forms at the cathode and anode electrode of SCR **10** are indicated by **19** and **20** in FIG.2.

Refer now to FIG.3. Note here that timer designated **3** in FIG.1 is now designated **3'**, while block **7** is designated **7'**. Circuits in **3'** and **7'** are examples and by no means the only solution as combination. The remaining elements are identical to those in FIG. 1. Diagrams of FIG.2 are valid again. Programable Unijunction Transistor (PUT) is used as the voltage sensing means in blocks **3'** and **7'** and designated **25** and **31** respectively. PUT designated **31** has its electrodes marked as follows: cathode designated **32**, anode-gate designated **33**, and anode designated **34**. Circuit in **3'** is a modified CR type timer with temperature compensation, and with synchronizing means as will be explained later. The operation of the block **3'** is as follows. Once switch **2** is closed the timing interval starts. At this moment SCR **10** is nonconductive, capacitors **6** and **21** have no charge. Note that resistors **29** and **30** represent a voltage divider, interconnection then represents a fraction of the supply voltage connected to the anode electrode of the temperature compensating diode **28**, which will be forced into conduction since its cathode is connected to resistor **27** whose remaining end is connected to the common lead **14**. Besides the connection to resistor **27**, cathode is connected also to resistor **26** and anode-gate **33**. Current through diode **28** and resistor **27** forms a voltage drop across resistor **27**, which serves as reference voltage for PUT **31** and through resistor **26** for PUT **25**. As is known from the theory of PUT operation, there will be no considerable conduction between anode and cathode electrode for as long as anode voltage is lower than peak voltage (V_p), since the current through PUT can not exceed the peak current value (I_p) (which is in the microampere range at present). In addition, PUT **25** can not trigger into conduction if resistors **22** and **23** are too large and not allowing a current flow consisting of PUT's anode-to-cathode leakage current, capacitor leakage current and of the PUT's peak current. In other words, initial PUT operating point must be located at the intersection of the load line and the negative resistance section of the PUT characteristics. Once conductive, PUT must have its new operating point i.e., intersection of new load line again —with the negative section of its characteristics in order to be able to switch back into nonconductive state through the valey point. Thus, for as long as anode voltage is lower or equal to the anode-gate reference voltage (V_a) PUT can not conduct.

Since anode of PUT **25** is tied up to series connection of resistors **22** and **23**, and to the capacitor **21**, its potential will follow the potential of capacitor **21**, which rises in an exponential manner as resistors **22** and **23** dictate. Once this potential reaches anode-gate voltage (reference voltage) plus anode-to-gate potential of 0.8 to 0.3 Volts (approximately), dependent on ambient temperature (PUT temperature coefficient being negative), PUT **25** will start conducting after time interval T_{d1}, allowing capacitor **21** to discharge following the path: Anode — cathode, then will divide into first current flowing through resistor **24** — common lead **14** to opposite plate, and a second current flowing through diode **4** — resistor **5** — capacitor **6** — common lead **14**

to opposite plate. At that time the anode-gate potential will drop as indicated by **16'** in FIG.**2.** Anode-gate potential of PUT **25** will be lower than that of PUT **31,** for a potential difference as defined by its gate current and resistor **26.** At the same time, anode-gate potential of PUT **31** will be lowered too, due to anode-gate current flowing through resistor **30.** Voltage drop across diode **28** is dependent mainly on ambient temperature and it compensates for anode — anode-gate junction voltage drop change for both PUT's. The PUT's must be of the same type and made by the same manufacturer, while diode **28** temperature coefficient must be same as PUT temperature coefficient over the desired temperature range. In addition, current through diode **28** should be slightly larger than I_p of a single PUT, during interval between pulses, for better accuracy. This assures that capacitors **6** and **21** will always charge to the same potential resulting in accurate time intervals. Discharge of capacitor **21** is fast since resistor **24,** diode **4,** resistor **5** and capacitor **6** represent low impedance. Capacitor discharge current and anode-gate current create voltage drop across resistor **24,** being positive towards common lead **14,** lasting **5** to **10** microseconds typically. Just mentioned voltage drop is that positive pulse used during explanation of operation of FIG.**1.** This pulse, and each subsequent one, will charge capacitor **6** in increments as indicated by **17** in FIG.**2.** Once charged to potential equal to anode-gate reference voltage, potential across capacitor **6** will surpass reference voltage of the PUT **31** during next pulse from **3'** so that PUT **31** will trigger into conduction allowing discharge of capacitor **6** through it where part of its current flows through resistor **8** to opposite plate. The remaining part will flow through the gate cathode junction of SCR **10,** resistor **9** to opposite plate forming a positive going pulse as indicated by **18** in FIG.**2.** Experiments have proved that time intervals T_{d2} can be over 10^4 times longer than T_{d1}.

Note that by changing T_{d1} a change in T_{d2} is imminent. If T_{d1} is shortened T_{d2} will be shortened proportionally, and if T_{d1} is made longer T_{d2} will be longer too. Interval T_{d1} is changed by varying the resistor **23.** (Another possibility is to vary resistor **5,** or instead of connecting one plate of either or both storage capacitors to potential zero i.e., common lead, connect them to a positive potential or a negative potential to get shorter or even longer time intervals. Yet another possibility is to vary the reference potential, which has adverse effects on accuracy).

An important feature is achieved, in addition, namely synchronous triggering of PUT's **25** and **31.** PUT **31** can trigger at the same time only, as PUT **25** triggers, since its reference potential is lowered and an additional charge to capacitor **6** forwarded during triggering of PUT **25.** This means that no false triggering can occur, the reliability of operation is high, and sensitivity can be made higher than for PUT **25** resulting in longer time intervals.

An additional temperature compensation exists in this circuit. Consider diode **4** and related components. During time interval between successive pulses from timer **3',** diode **4** is reverse biased by the potential across capacitor **6** through resistors **5** and **24,** and common lead **14.** The higher the ambient temperature, the larger the leakage current through diode **4,** the faster discharge of capacitor **6** between successive pulses thus, shortened time interval. This is partly opposed by the increase of incomming pulses due to decrease of voltage drop across diode **4** junction. In addition the increased leakage current through the reverse biased anode-gate — anode junction of PUT **31** acts as a charging current in intervals between the successive pulses from PUT **25.** This way a nearly complete balance of temperature effects is achieved resulting in accurate time intervals over wide temperature range. Another way of achieving even greater accuracy is by careful choice of dielectrics for capacitors and check on capacitance change versus ambient temperature change. Mylar as dielectric in capacitors will give good results. Other low leakage dielectrics like paper mylar, metalized paper-resin, metalized mylar and so on will give capacitors with satisfactory characteristics to suit good accuracy.

One skilled in the art will notice that other improvements and variations are possible within the scope of this invention.

I claim:

1. A pulsating timer for producing accurate, adjustable time intervals over wide ambient temperature range, immune to false triggering, and comprising:

a DC power source having negative terminal connected to a common lead, and a positive terminal connected to the common terminal of a power switch, whose normally open terminal is connected to a supply lead,

a series connection of two resistors, one resistor, being variable to adjust said time intervals, connected to said supply lead and having its remaining end connected to a first current limiting resistor whose other end is connected to one plate of a

first storage capacitor having remaining plate connected to said common lead,

a first programmable unijunction transistor (PUT) having an anode, anode-gate, and a cathode electrode, said anode electrode being connected to the interconnection of said first current limiting resistor and said first storage capacitor to sense the potential across it, while said cathode electrode is connected to a

first cathode resistor having its remaining end connected to said common lead,

a voltage divider consisting of a first and a second resistor, said first resistor is connected to said common lead, while its other end is connected to said second resistor whose remaining end is connected to said supply lead,

first diode having anode electrode connected to the interconnection of said first and said second resistor, its cathode electrode is connected to an

anode-gate resistor connected by its other end to said anode-gate electrode of said first PUT,

a biasing resistor connected to said common lead and having its remaining end connected to the interconnection of said cathode electrode of said first diode, and said anode-gate resistor, for purpose of allowing conduction of the biasing current through said first diode, and forming of the reference potential for said first PUT,

second diode connected by its anode electrode to said interconnection of said first PUT and said first cathode resistor, its cathode electrode is connected to a

second current limiting resistor having its other end connected to one plate of a second storage capaci-

tor having remaining plate connected to said common lead,

second programmable unijunction transistor (PUT), used as the voltage sensing means across said second storage capacitor, having anode, anode-gate, and cathode electrode, said anode electrode being connected to the interconnection of said second current limiting resistor and said second storage capacitor, to sense the potential across the last one, anode-gate electrode being connected to the interconnection of said anode-gate resistor, said biasing resistor and said cathode electrode of said first diode, to receive said reference potential and enable said second PUT to trigger in synchronism with said first PUT, and also to receive the compensating voltage for its anode — anode-gate junction voltage variance due to ambient temperature, cathode electrode of said second PUT is connected to one end of the

second cathode resistor, having its remaining end connected to said common lead, used to develop a positive going voltage pulse due to discharge current from said second storage capacitor through said second PUT, at the end of the timing interval, said positive going voltage pulse used to control other devices.

2. A pulsating timer as claimed in **1,** and further including a silicon controlled rectifier (SCR) having anode, cathode, and gate electrode in which said gate electrode is connected to the interconnection of said second cathode electrode and said second cathode resistor, said SCR cathode electrode is connected to an

SCR cathode resistor whose other end is connected to said common lead and used to develop a control voltage once SCR is conductive,

SCR anode resistor connected to said SCR anode electrode and having its remaining end connected to said supply lead in order to limit the current through said SCR (along with said SCR cathode resistor) and develop a voltage drop, while said SCR is conductive, for purpose of controlling other devices.

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