# United States Patent

**Cull et al.**

[15] **3,668,661**

[45] **June 6, 1972**


## [54] CHARACTER CODING, MEMORY, AND DISPLAY SYSTEM


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[73] Assignee: **The National Cash Register Company,** Dayton, Ohio



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[52] **U.S. Cl.** ..... **340/172.5**

[51] **Int. Cl.** ..... **G06f 13/02**

[58] **Field of Search** ..... 340/172.5; 235/157



[56] **References Cited**

UNITED STATES PATENTS

| | | | |
|---|---|---|---|
| 3,235,849 | 2/1966 | Klein | 340/172.5 |
| 3,275,993 | 9/1966 | Bartlett et al. | 340/172.5 |
| 3,328,772 | 6/1967 | Oeters | 340/172.5 |
| 3,400,377 | 9/1968 | Lee | 340/172.5 |
| 3,400,384 | 9/1968 | Hildebrandt | 340/172.5 X |
| 3,413,610 | 11/1968 | Botjer et al. | 340/172.5 |
| 3,471,835 | 10/1969 | Gribble et al. | 340/172.5 X |



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[57] **ABSTRACT**

Characters each identified by a bit code are advanced serially to a memory comprising continuously cycling shift registers, one for each bit of the code. The bits for each character enter the shift registers in parallel. The character codes are placed one behind the other in the shift register memory by operation of a character counter and a second counter which is its complement.

The memory is formatted for control of a cathode ray tube display operating to legibly display all characters in the memory. A major raster traces lines of character positions. A minor raster traces each character in a dot matrix at each character position.


**8 Claims, 30 Drawing Figures**

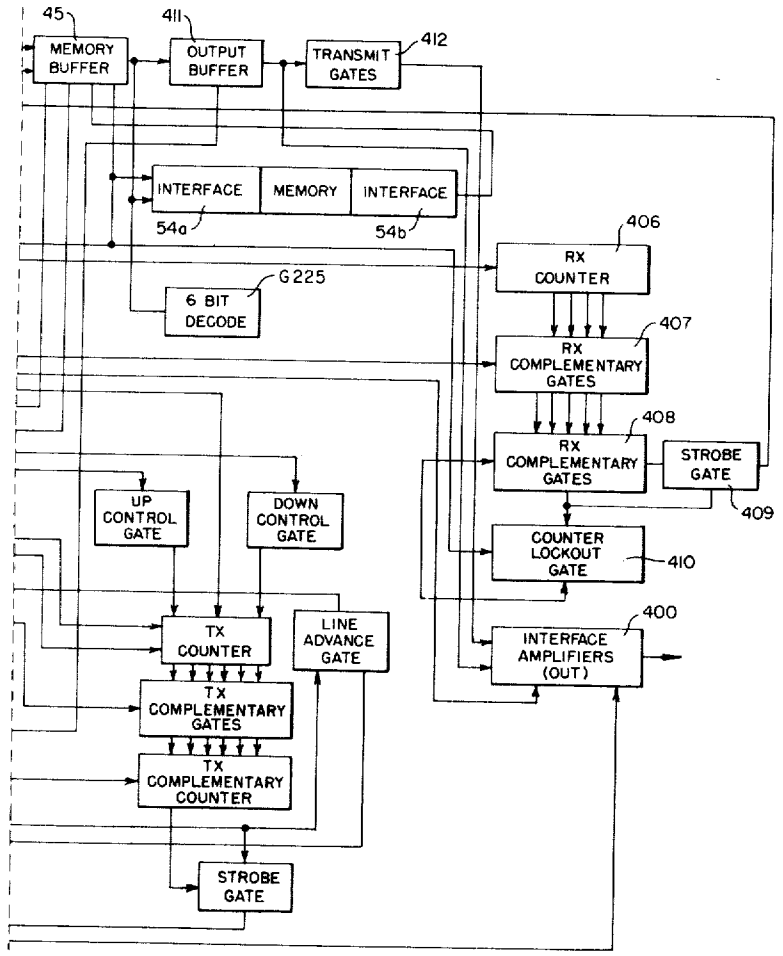


FIG. 1

| Bits 4 3 2 1 | Bits 6 5 | 1 0 | 1 1 | 0 0 | 0 1 |
|---|---|---|---|---|---|
| 0 0 0 0 | | SP | 0 | ⊠ | P |
| 0 0 0 1 | | ! | 1 | A | Q |
| 0 0 1 0 | | " | 2 | B | R |
| 0 0 1 1 | | # | 3 | C | S |
| 0 1 0 0 | | $ | 4 | D | T |
| 0 1 0 1 | | % | 5 | E | U |
| 0 1 1 0 | | & | 6 | F | V |
| 0 1 1 1 | | ' | 7 | G | W |
| 1 0 0 0 | | ( | 8 | H | X |
| 1 0 0 1 | | ) | 9 | I | Y |
| 1 0 1 0 | | * | : | J | Z |
| 1 0 1 1 | | + | ; | K | [ |
| 1 1 0 0 | | , | < | L | ⊠ |
| 1 1 0 1 | | - | = | M | ] |
| 1 1 1 0 | | . | > | N | ⊠ |
| 1 1 1 1 | | / | ? | O | ⊟ |

FIG. 4

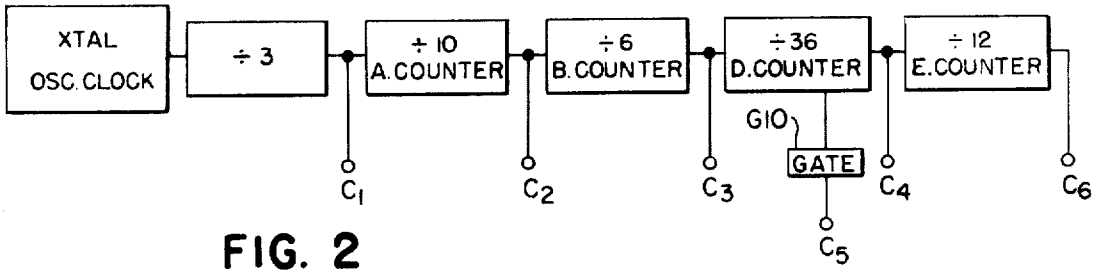
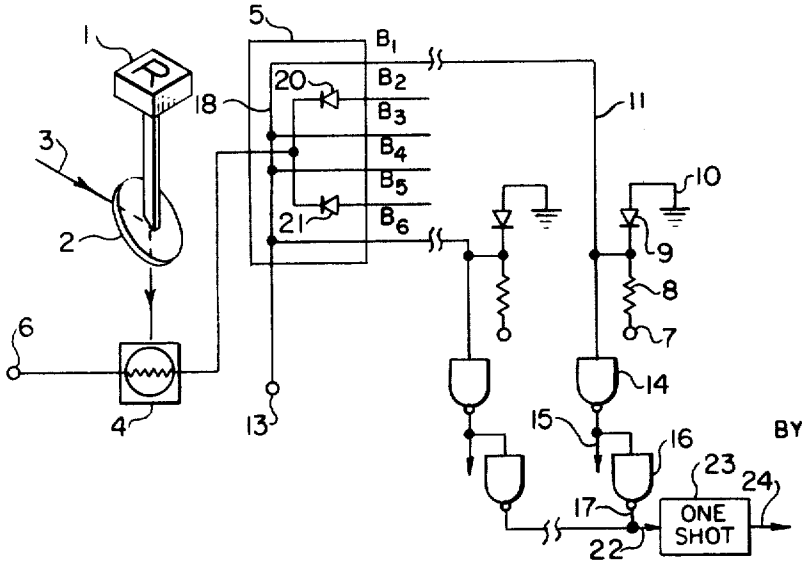
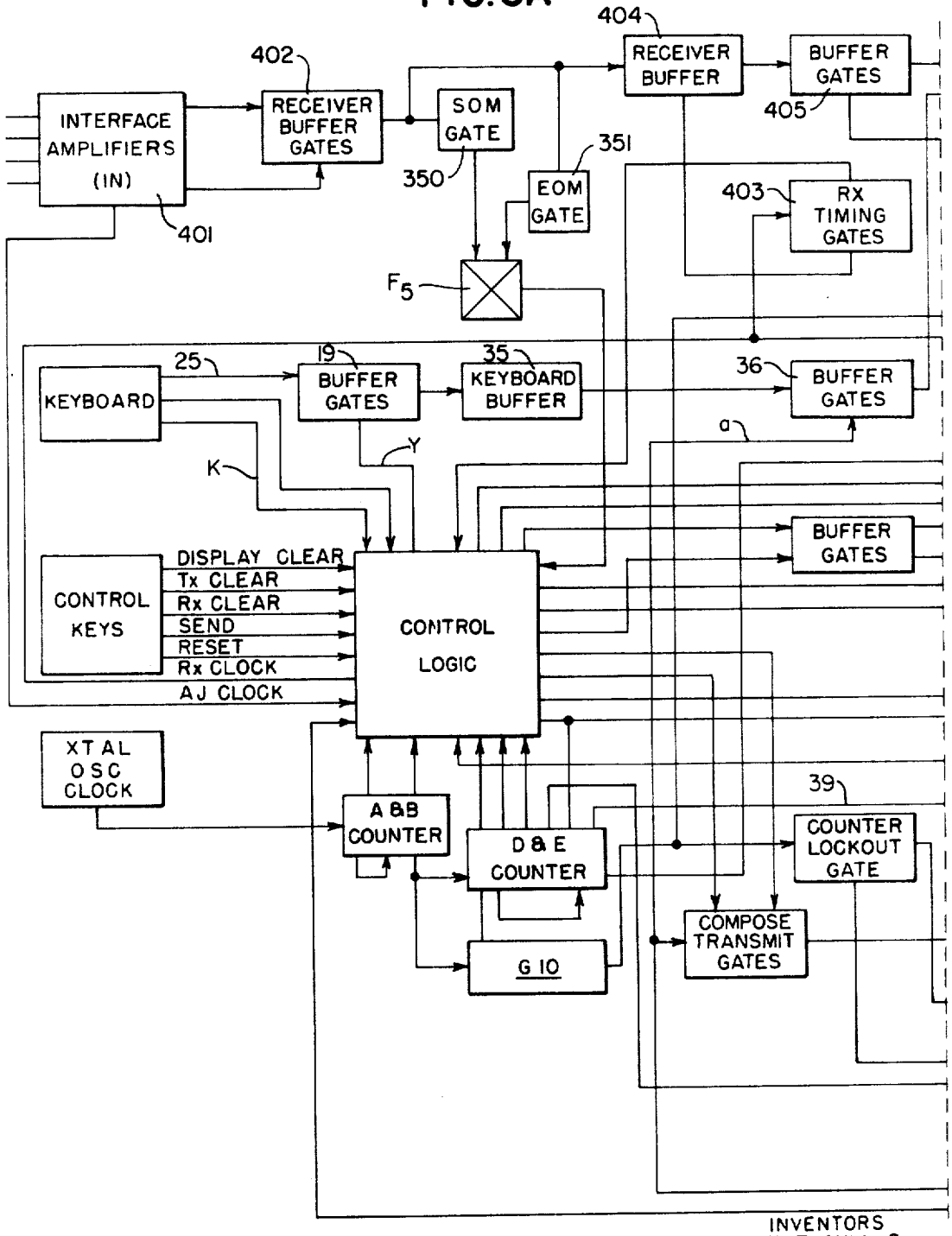



FIG. 2



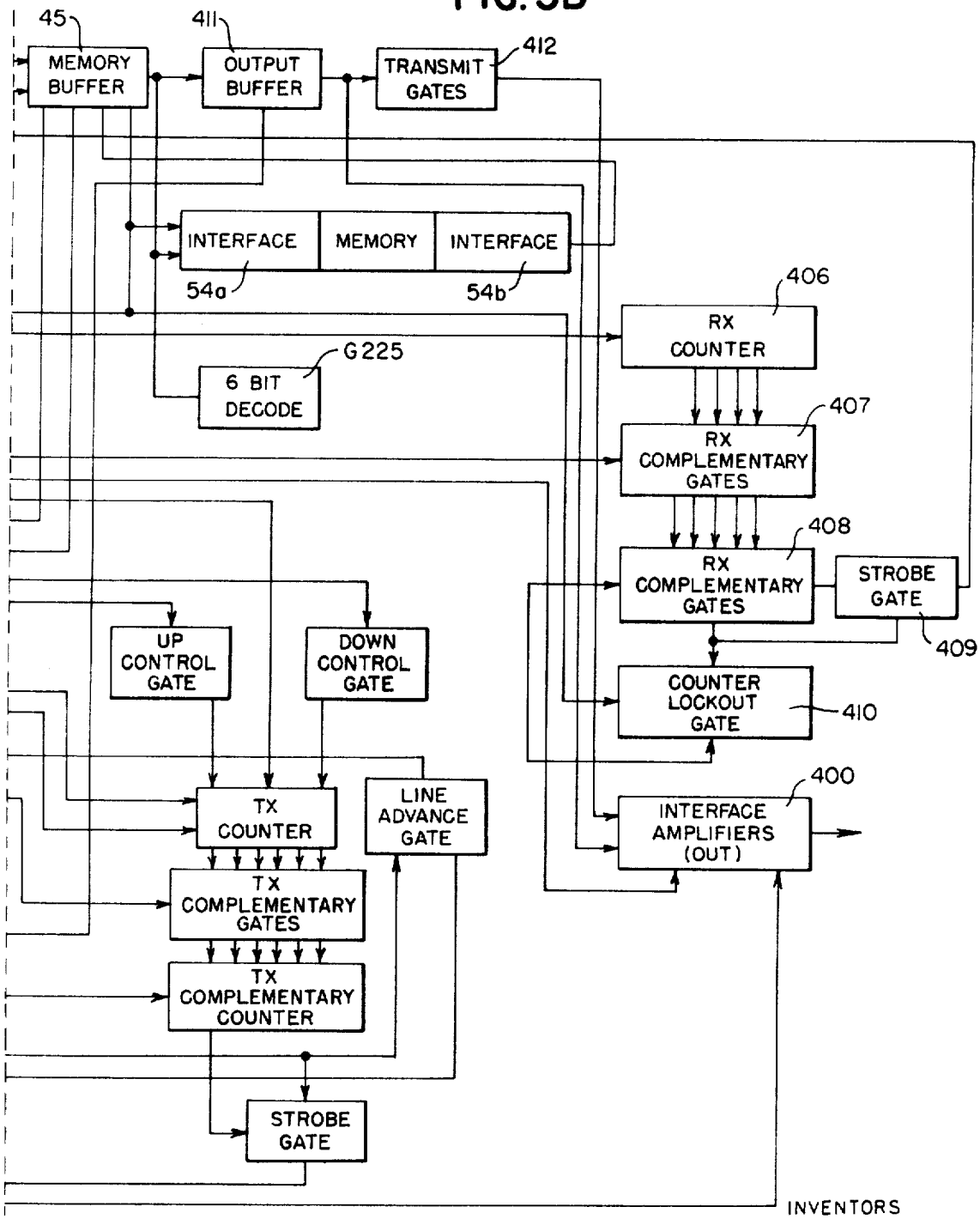

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FIG. 3A




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FIG. 3B

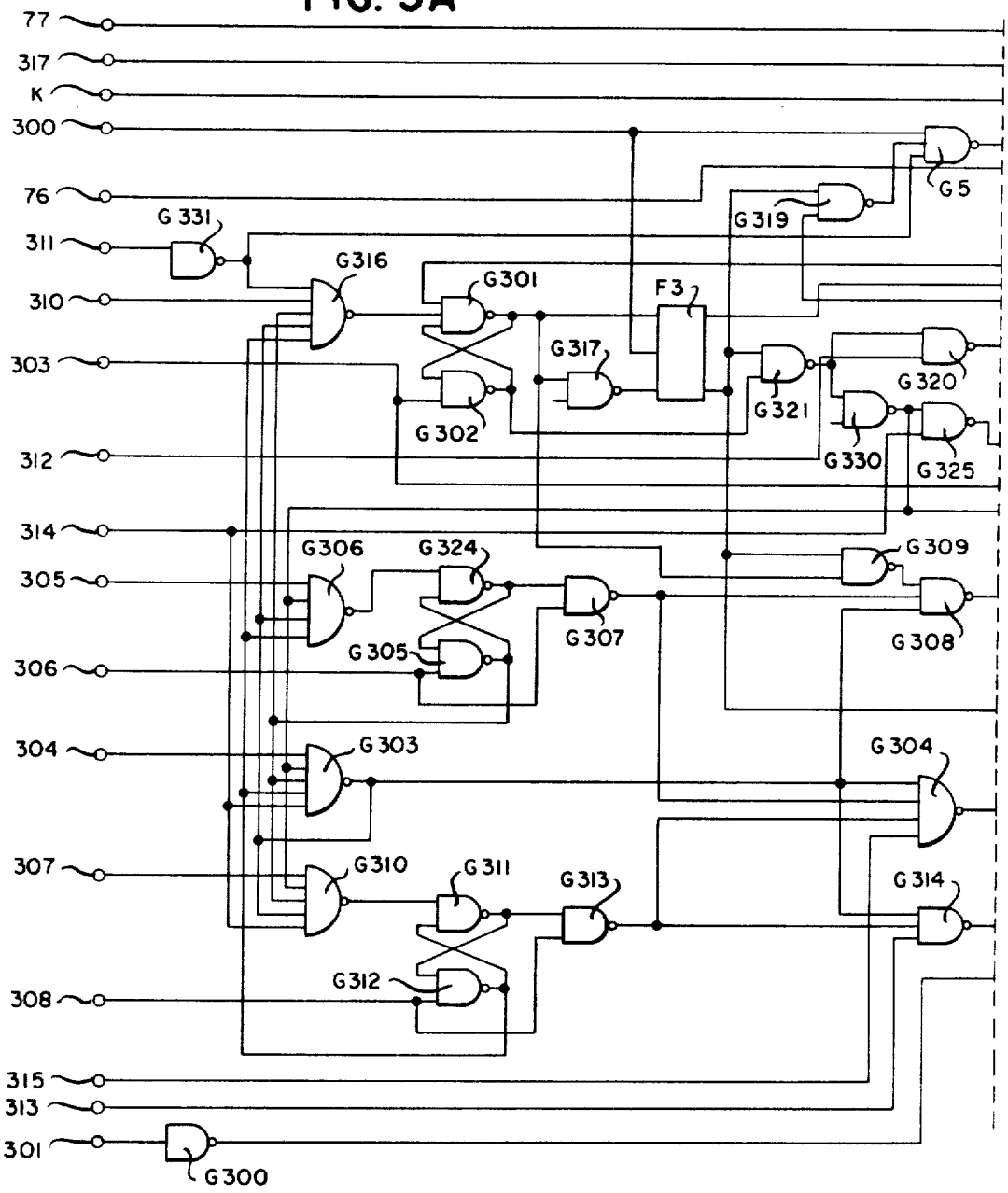



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FIG. 5A

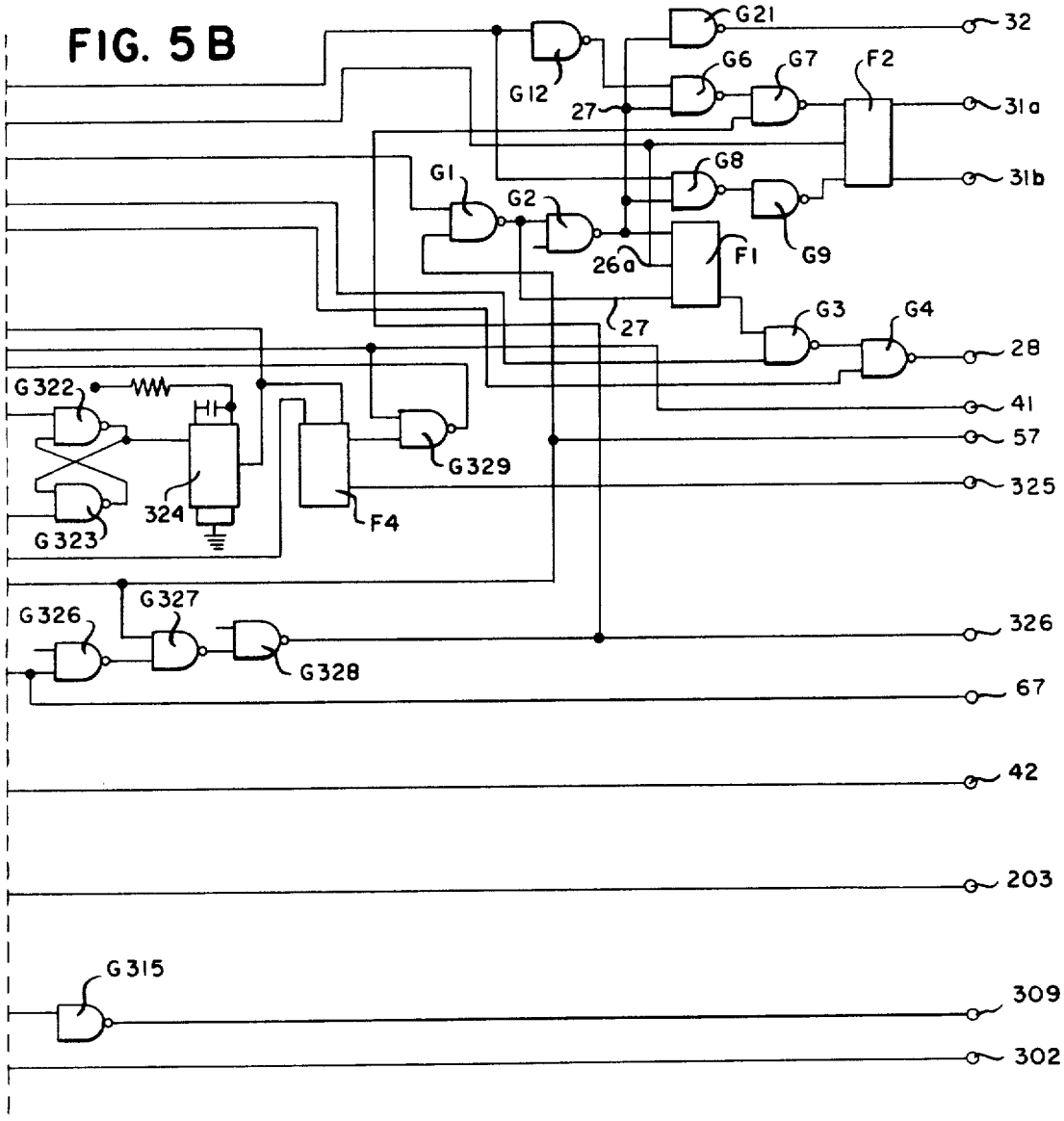



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FIG. 5B




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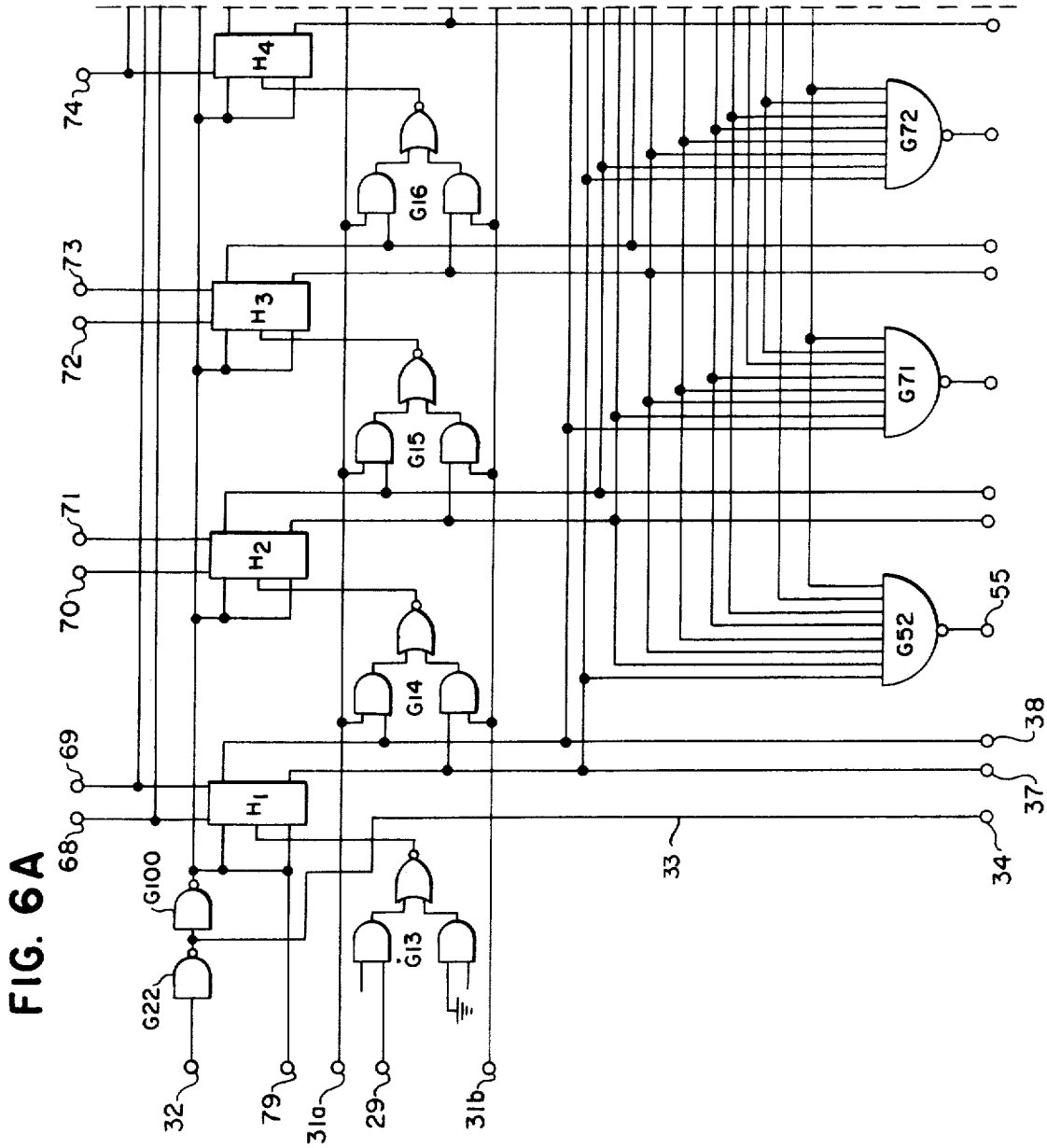



FIG. 6A

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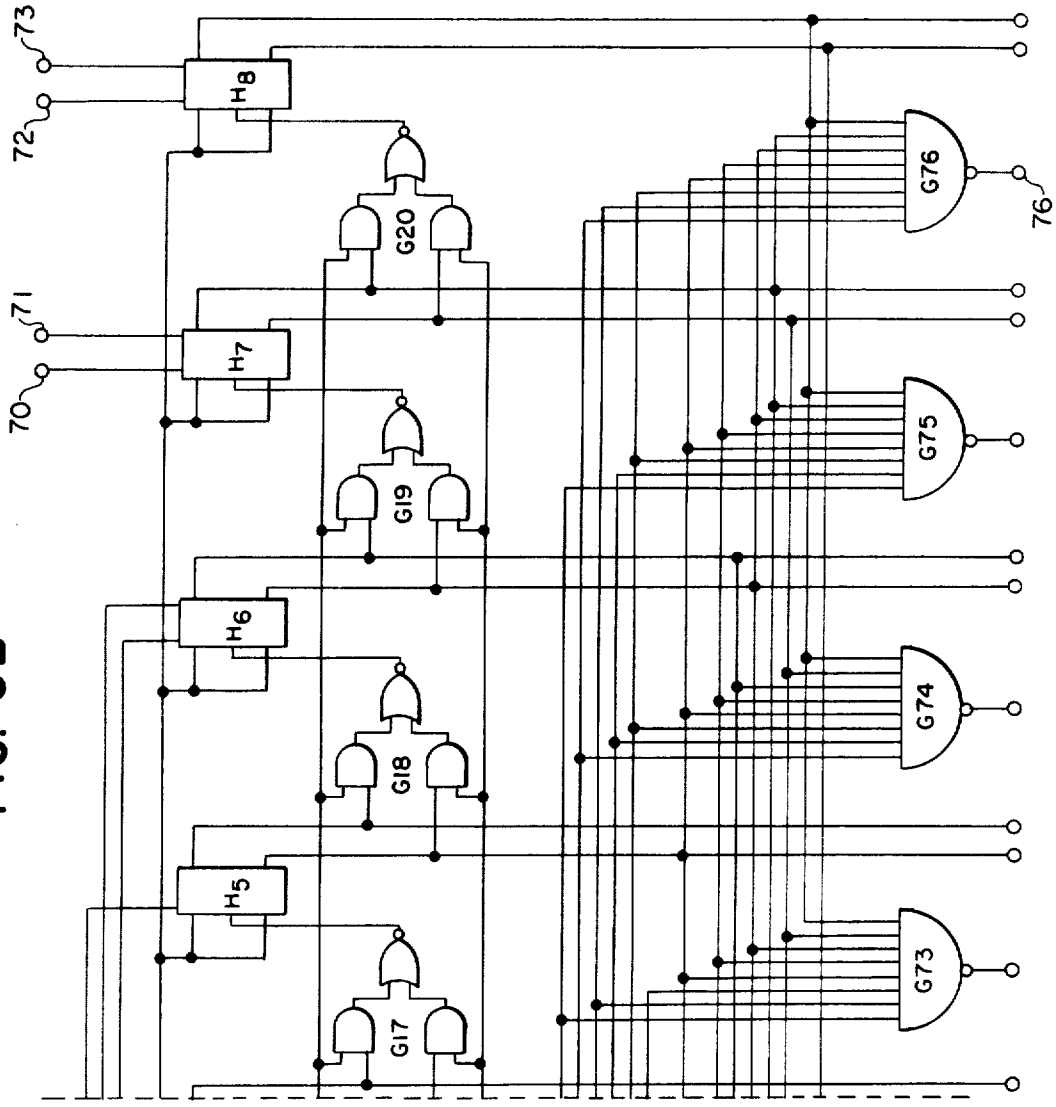



FIG. 6B

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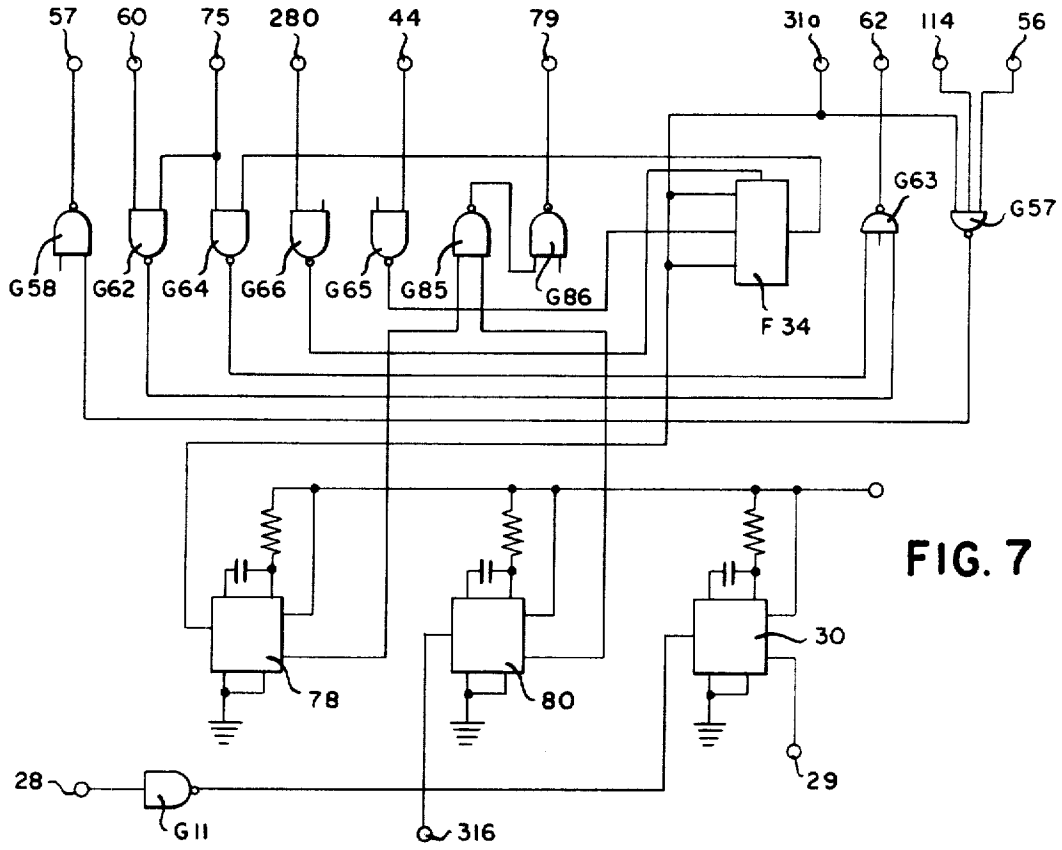



FIG. 7

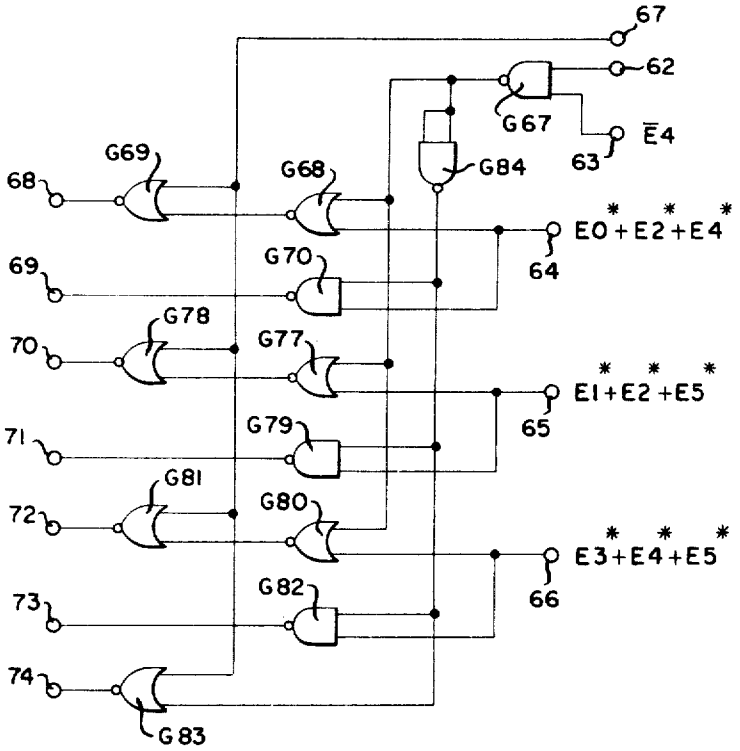


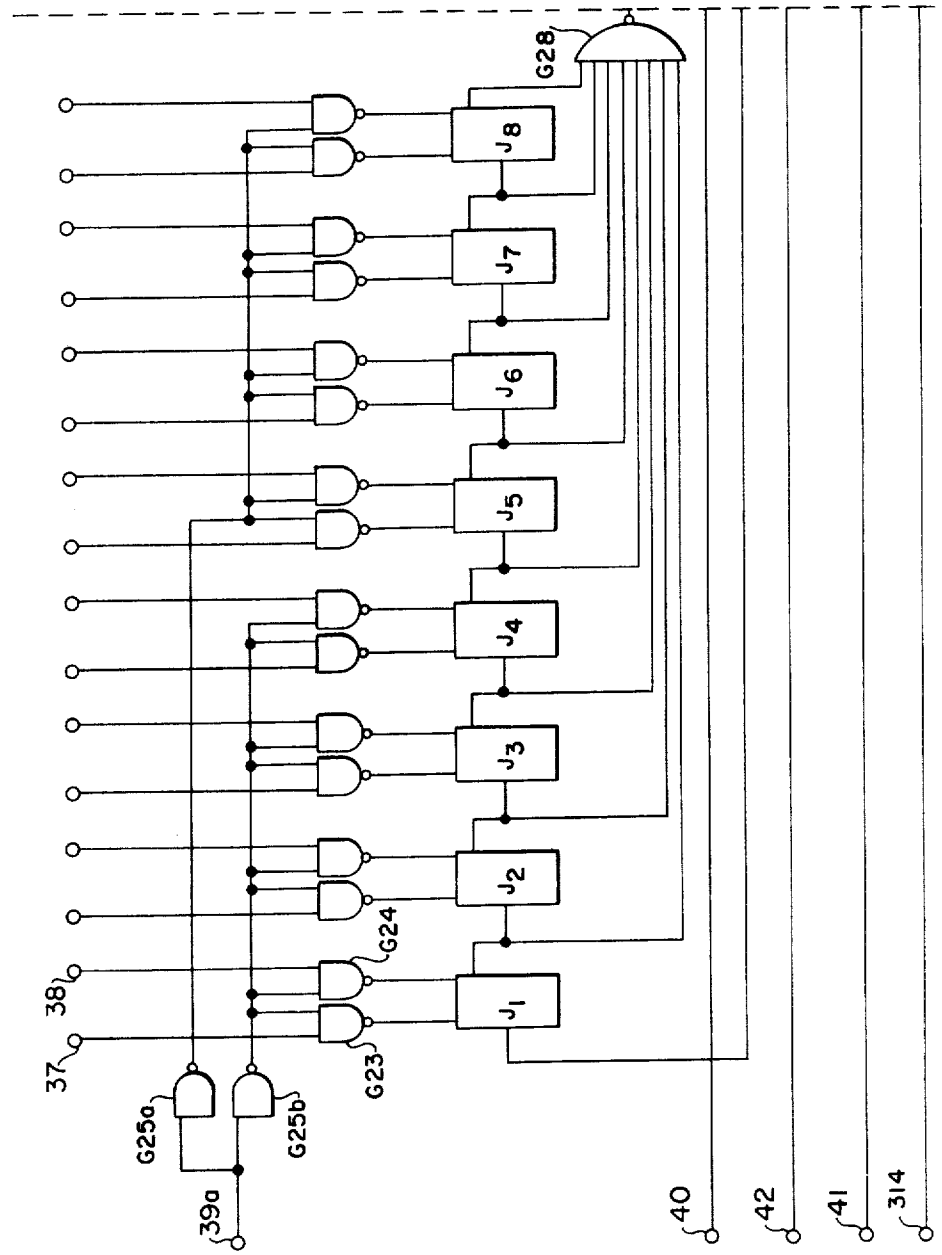

FIG. 12

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FIG. 8A




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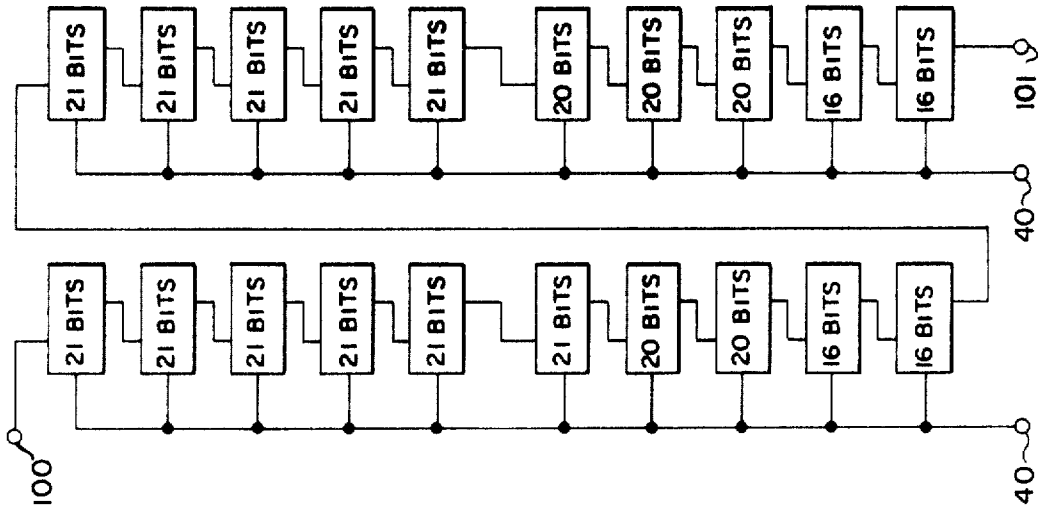



FIG. 9

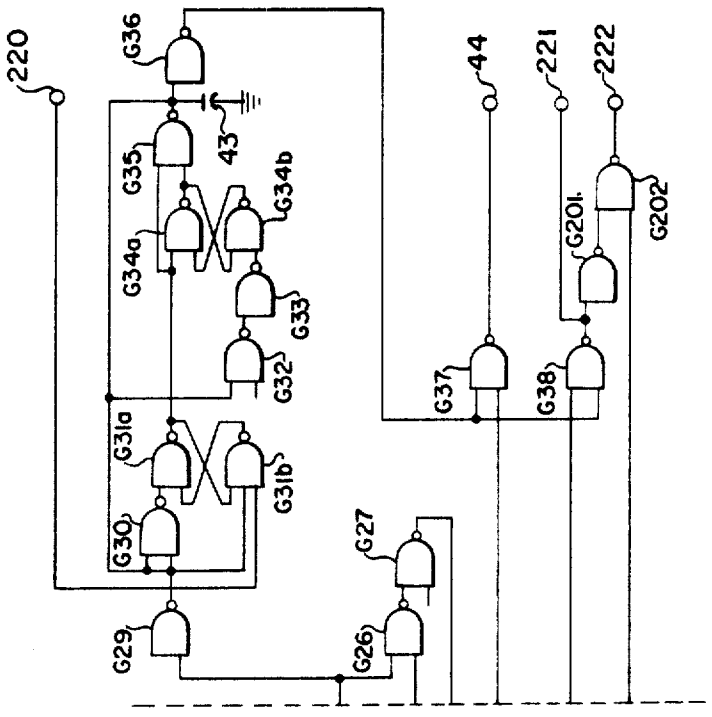


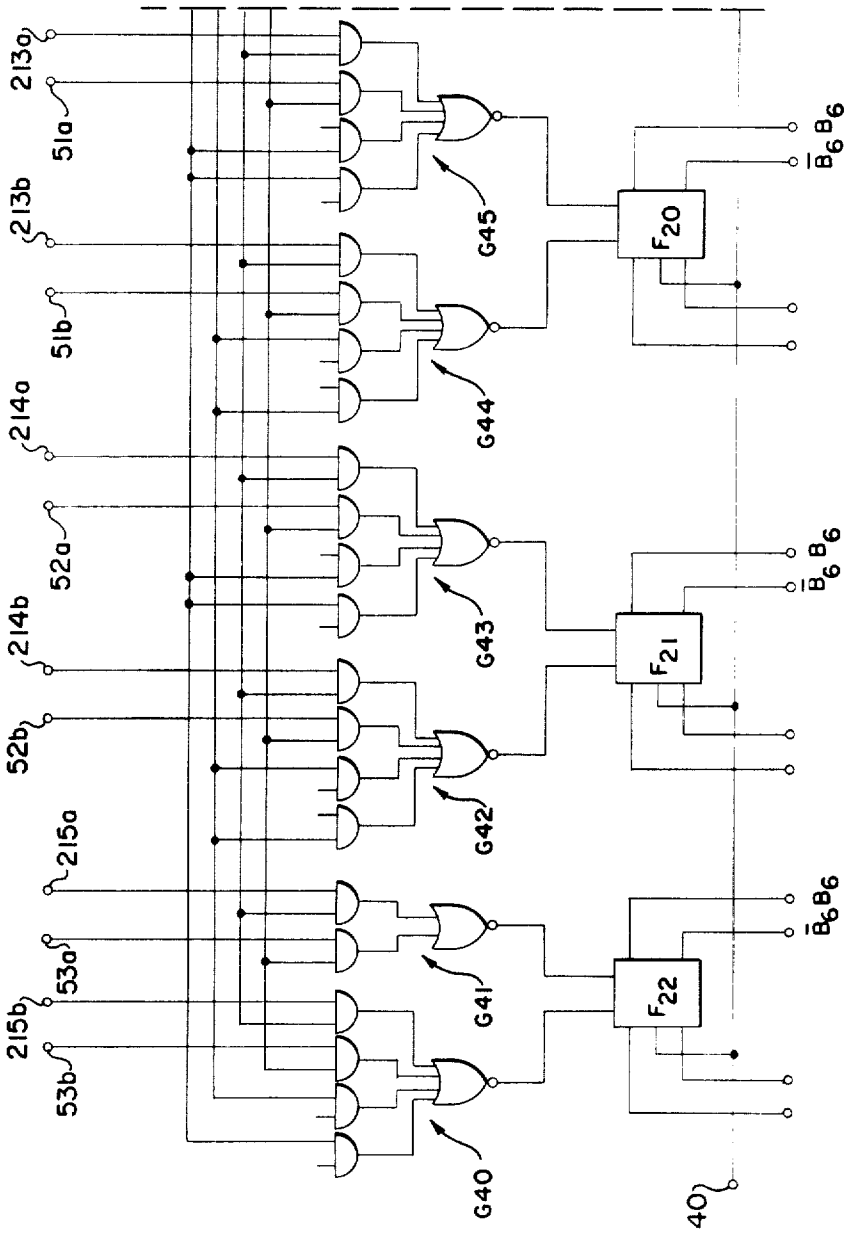

FIG. 8B

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FIG. 10A

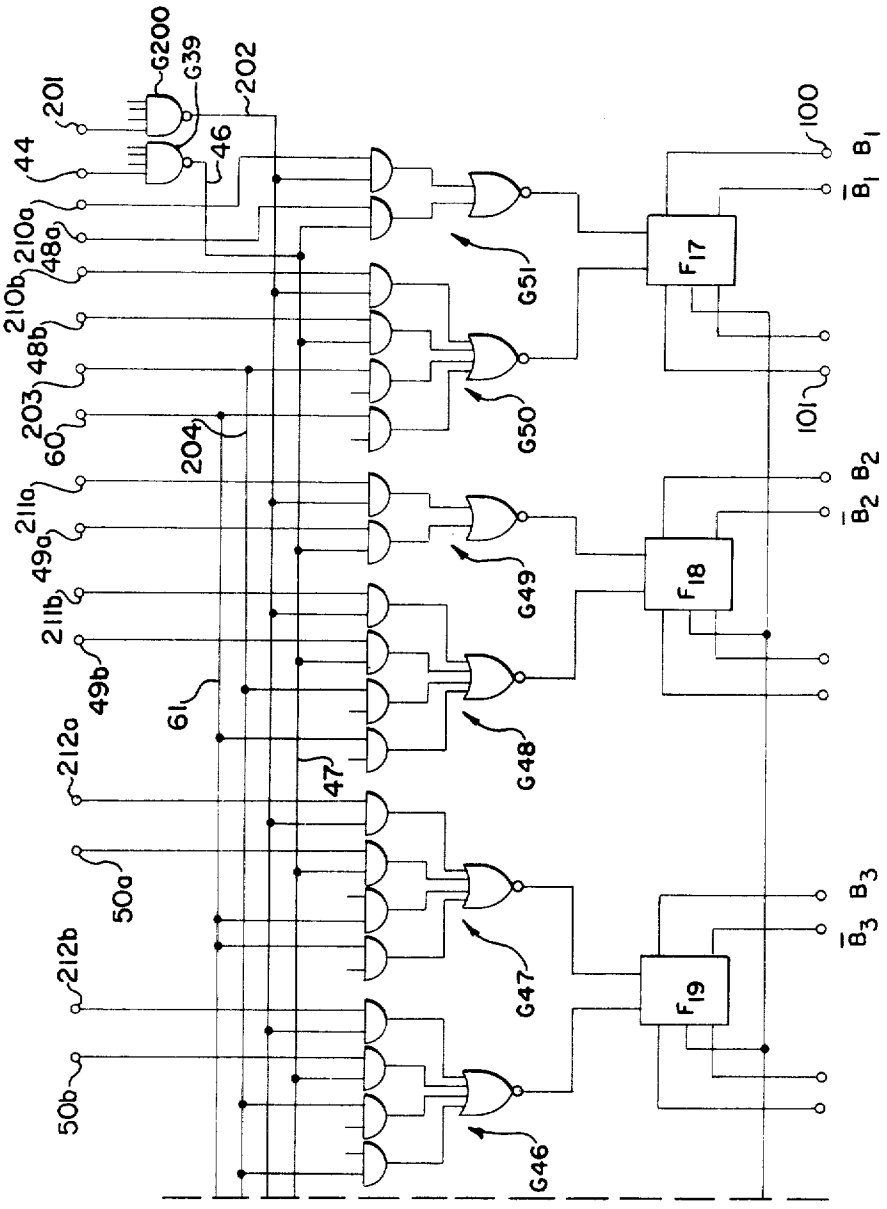



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FIG. 10B




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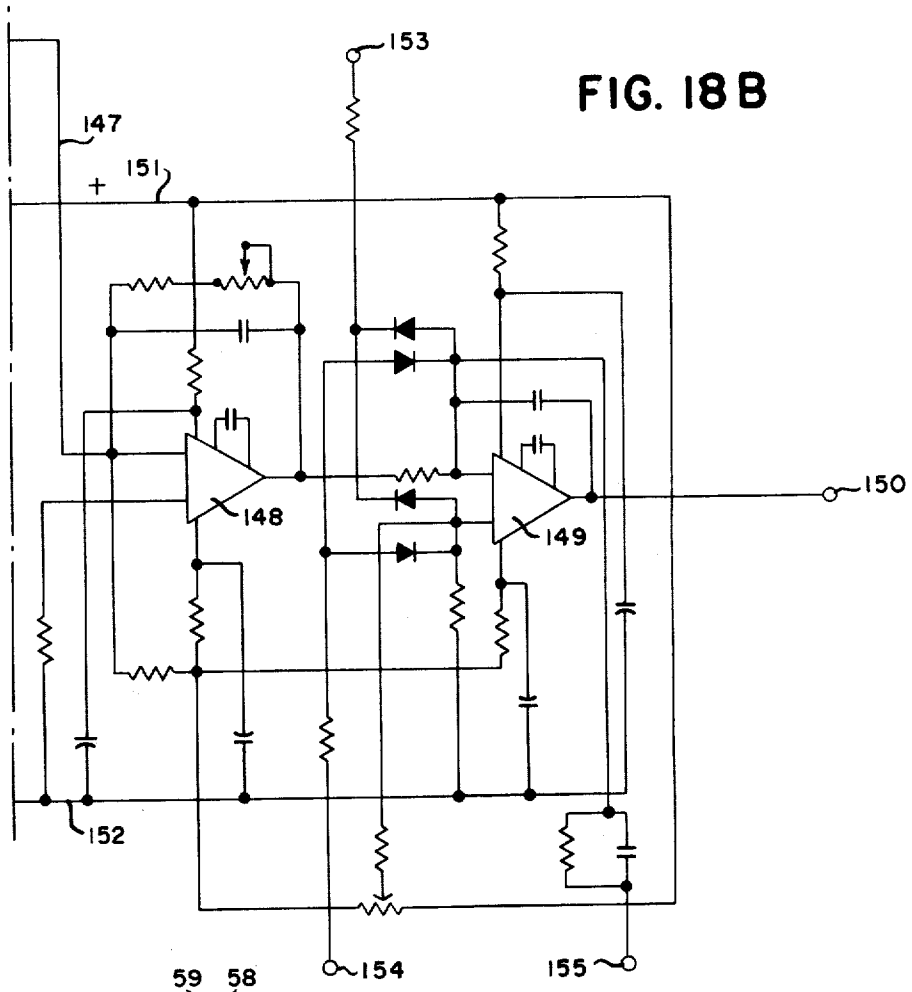



FIG. 18B

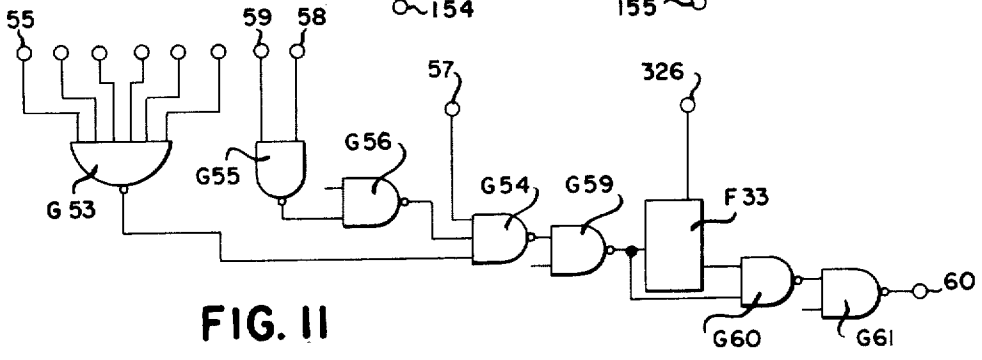



FIG. 11

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FIG. 13

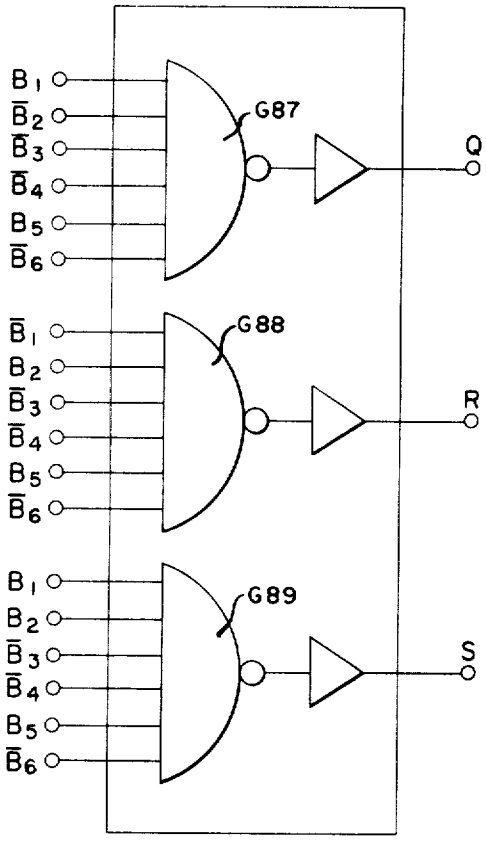
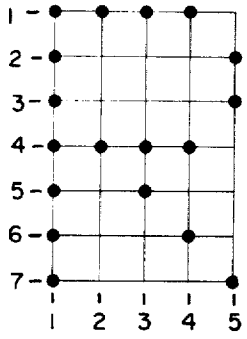



FIG. 14

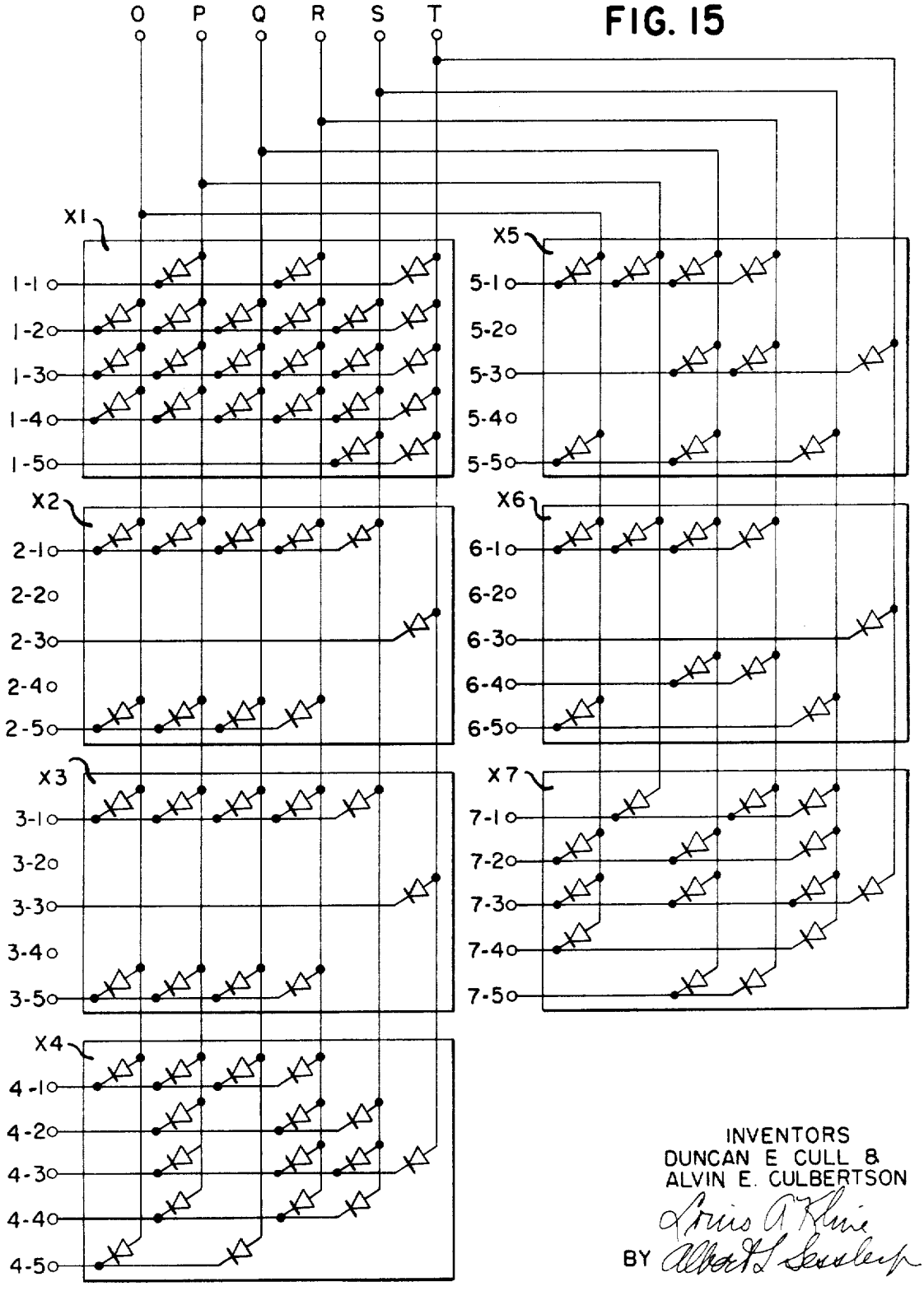
| | Q | R | S |
|---|---|---|---|
| $B_1$ | 1 | | 1 |
| $\bar{B}_1$ | | 1 | |
| $B_2$ | | 1 | 1 |
| $\bar{B}_2$ | 1 | | |
| $B_3$ | | | |
| $\bar{B}_3$ | 1 | 1 | 1 |
| $B_4$ | | | |
| $\bar{B}_4$ | 1 | 1 | 1 |
| $B_5$ | 1 | 1 | 1 |
| $\bar{B}_5$ | | | |
| $B_6$ | | | |
| $\bar{B}_6$ | 1 | 1 | 1 |

FIG. 16




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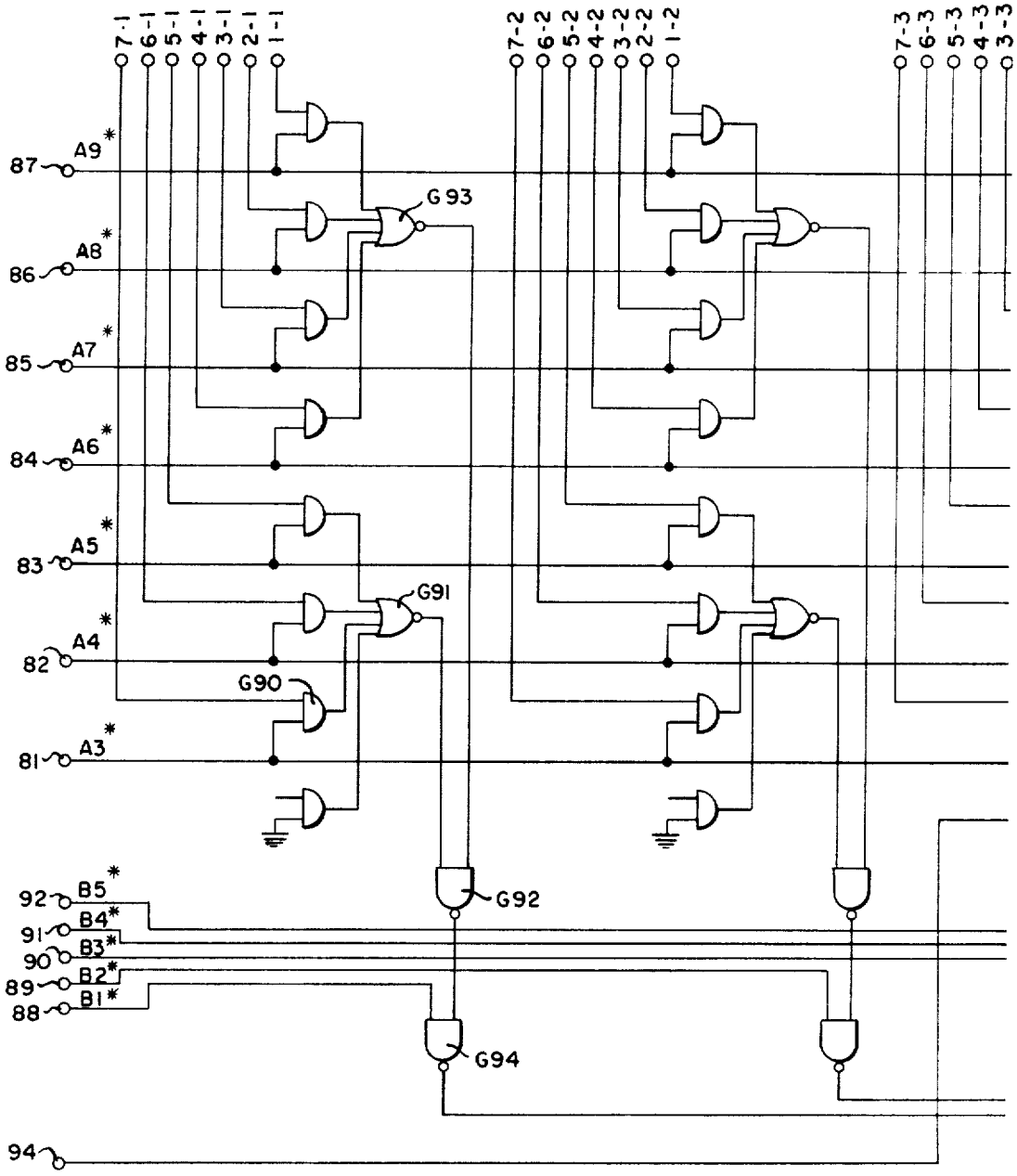
FIG. 15




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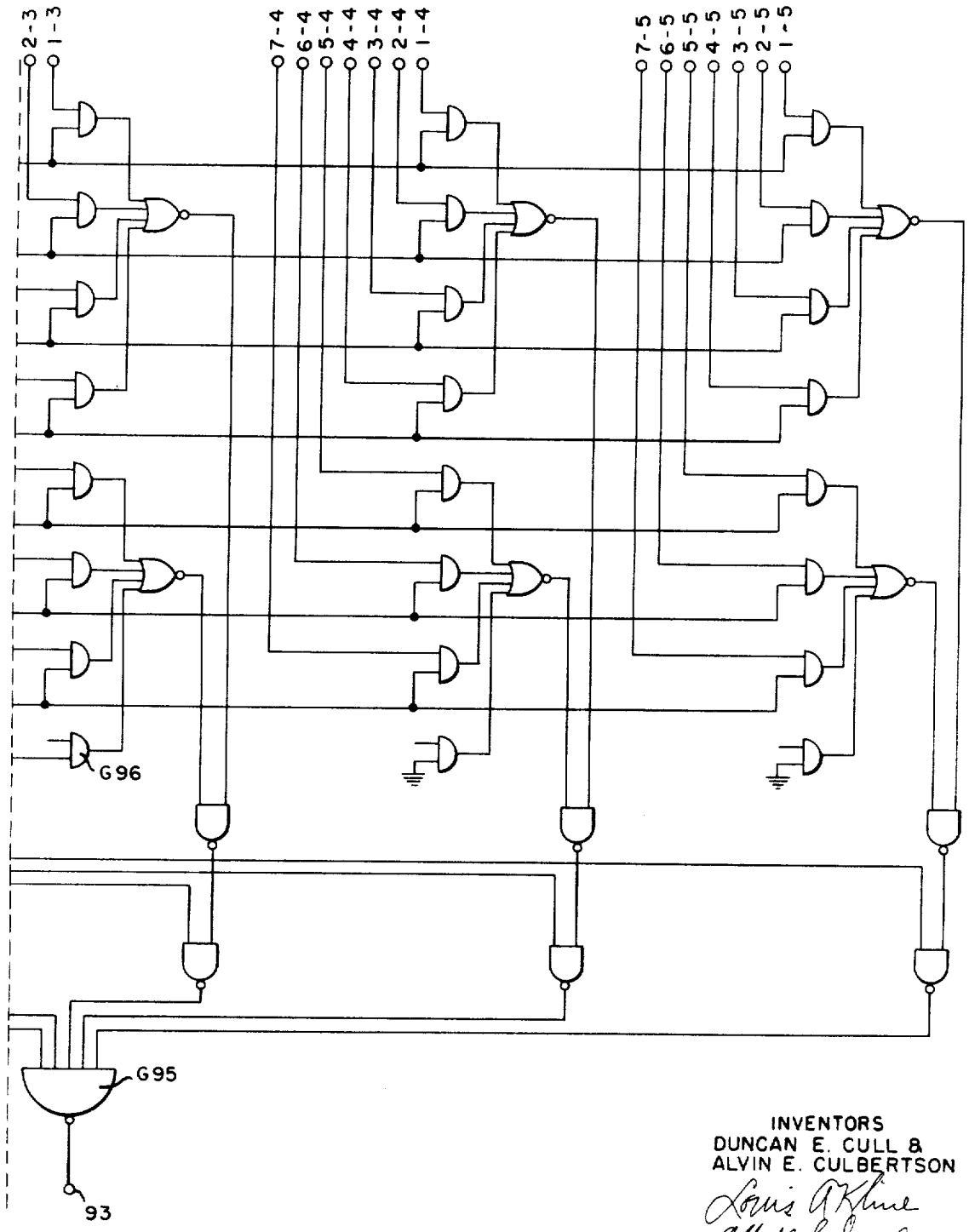
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FIG. 17A




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FIG. 17B




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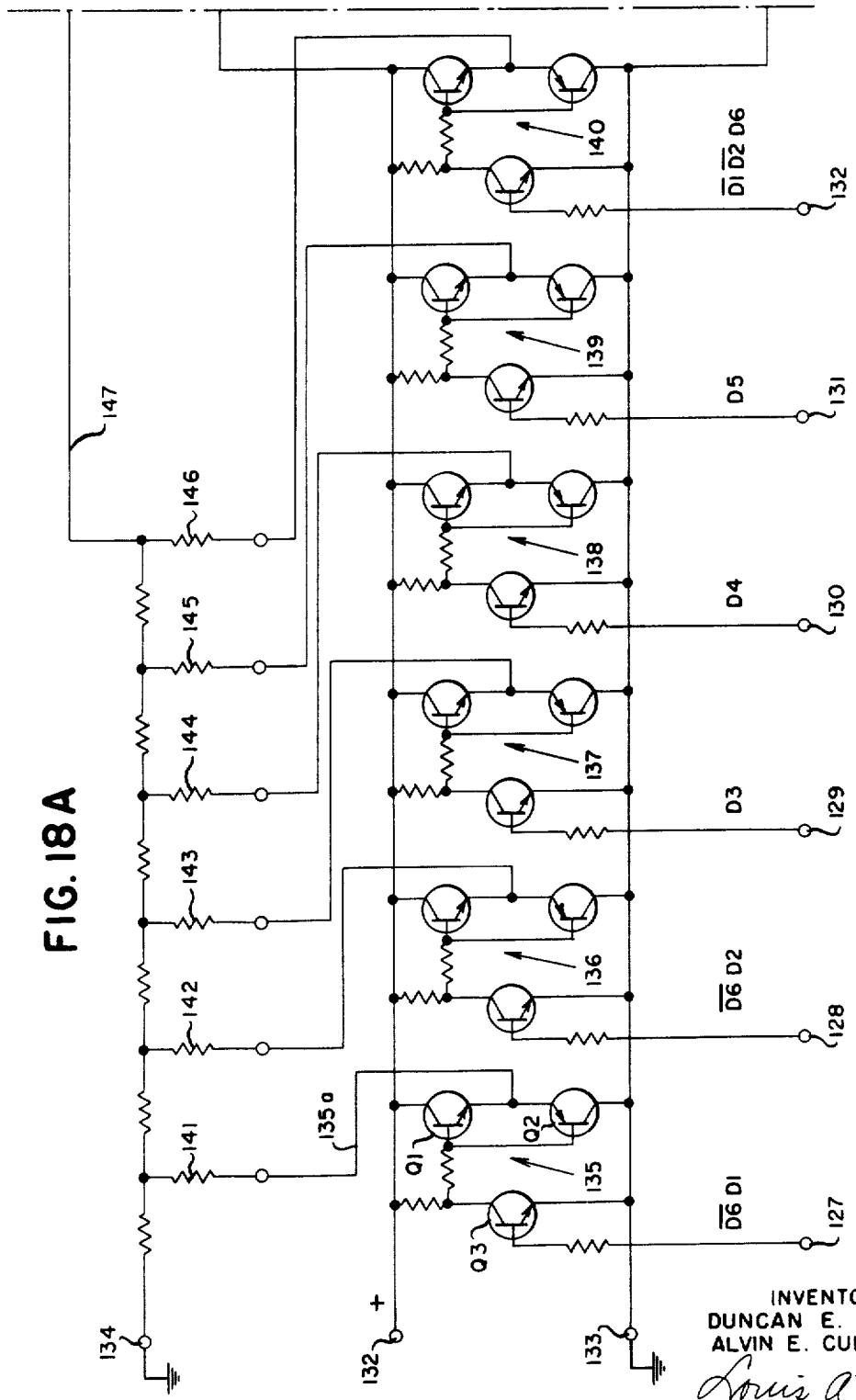
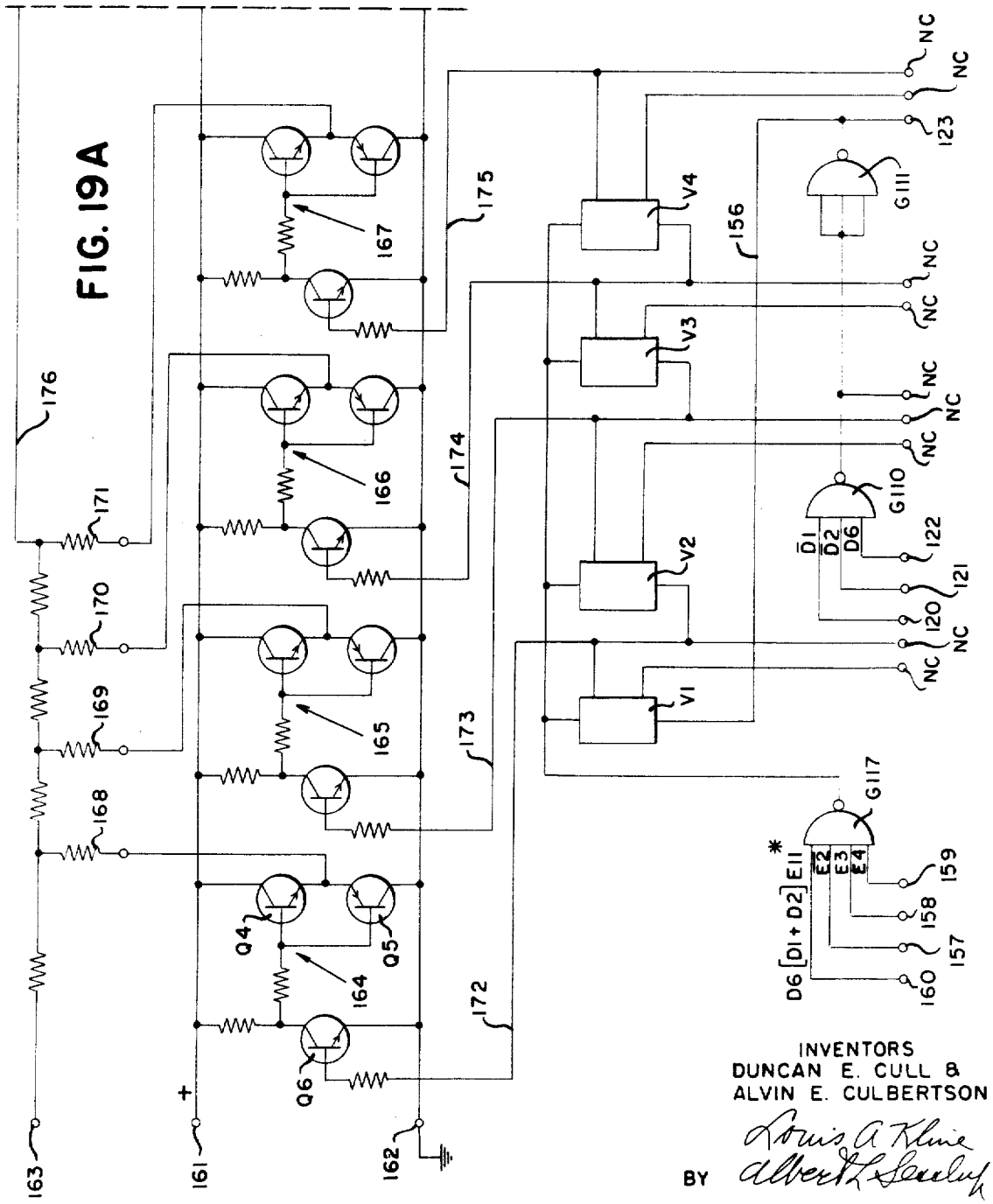



FIG. 18A

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FIG. 19A




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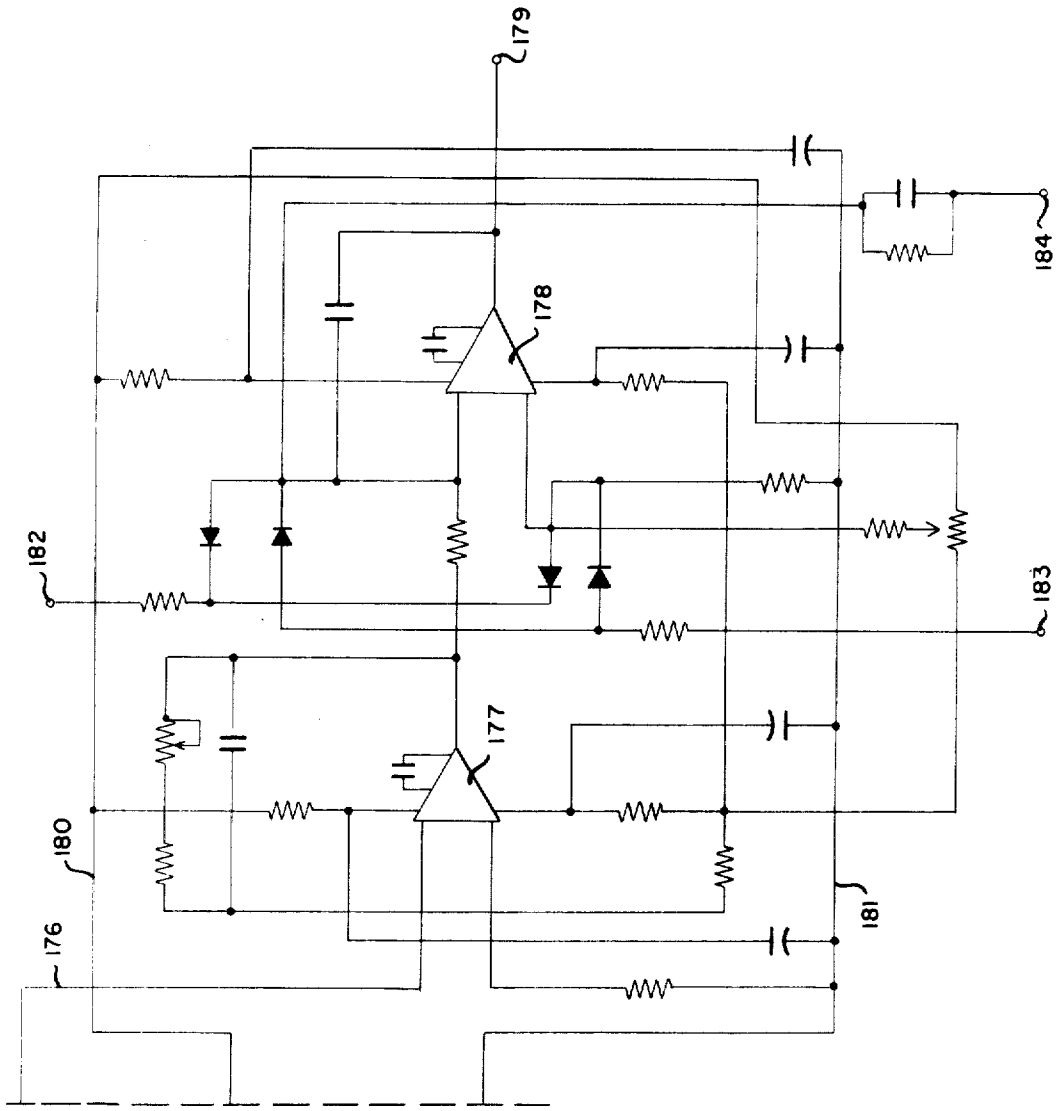



FIG. 19B

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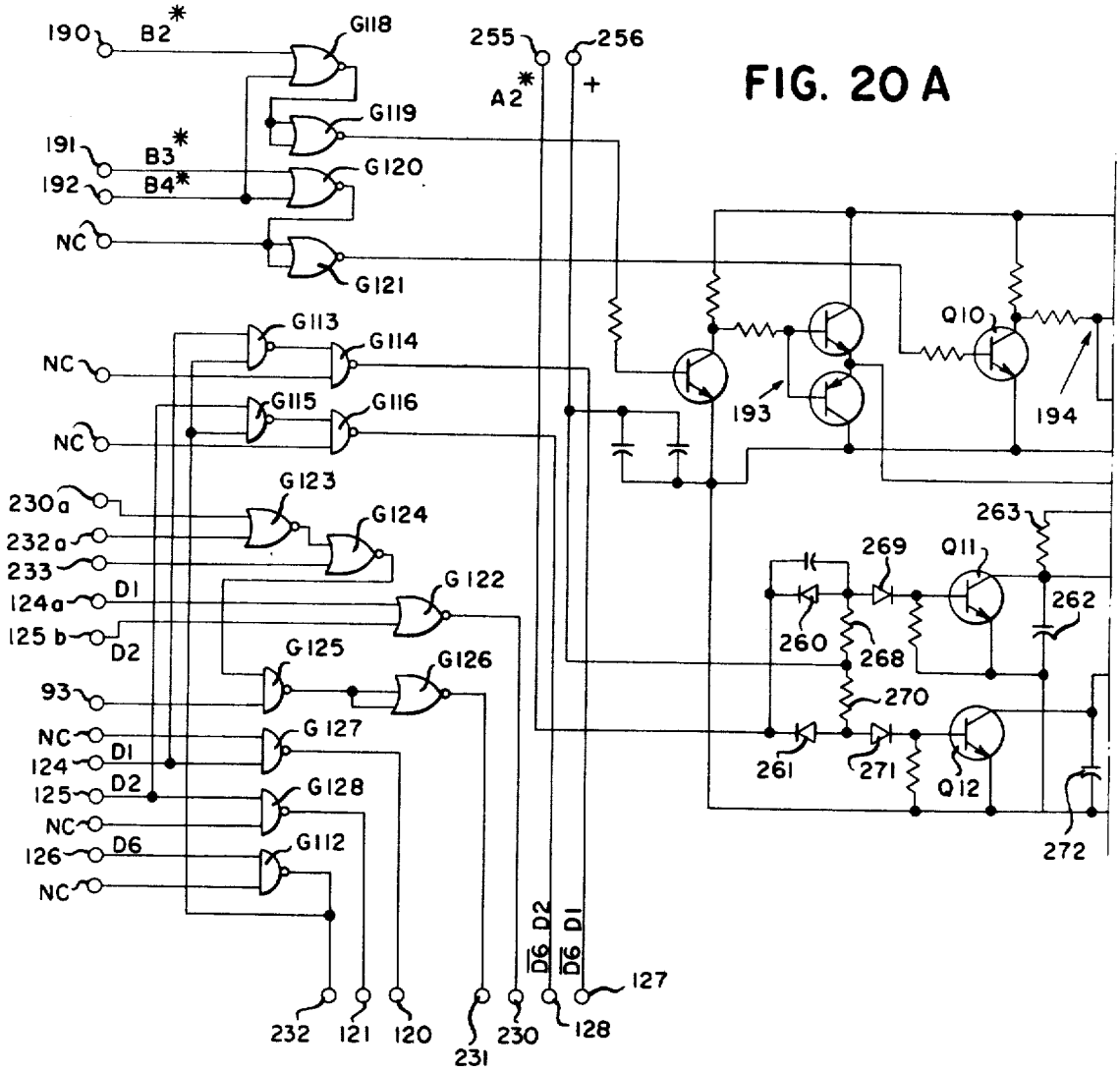


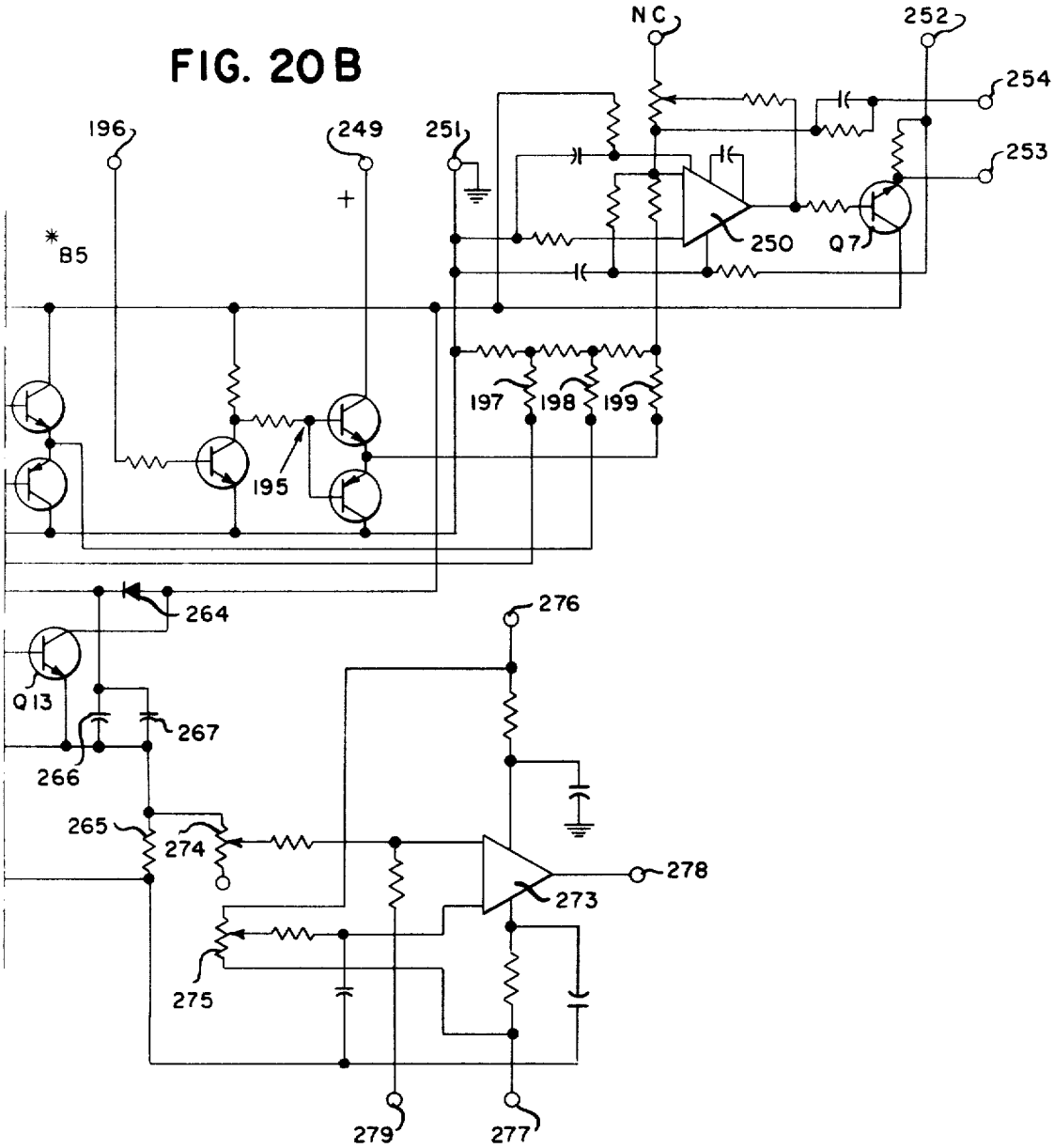

FIG. 20 A

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FIG. 20B




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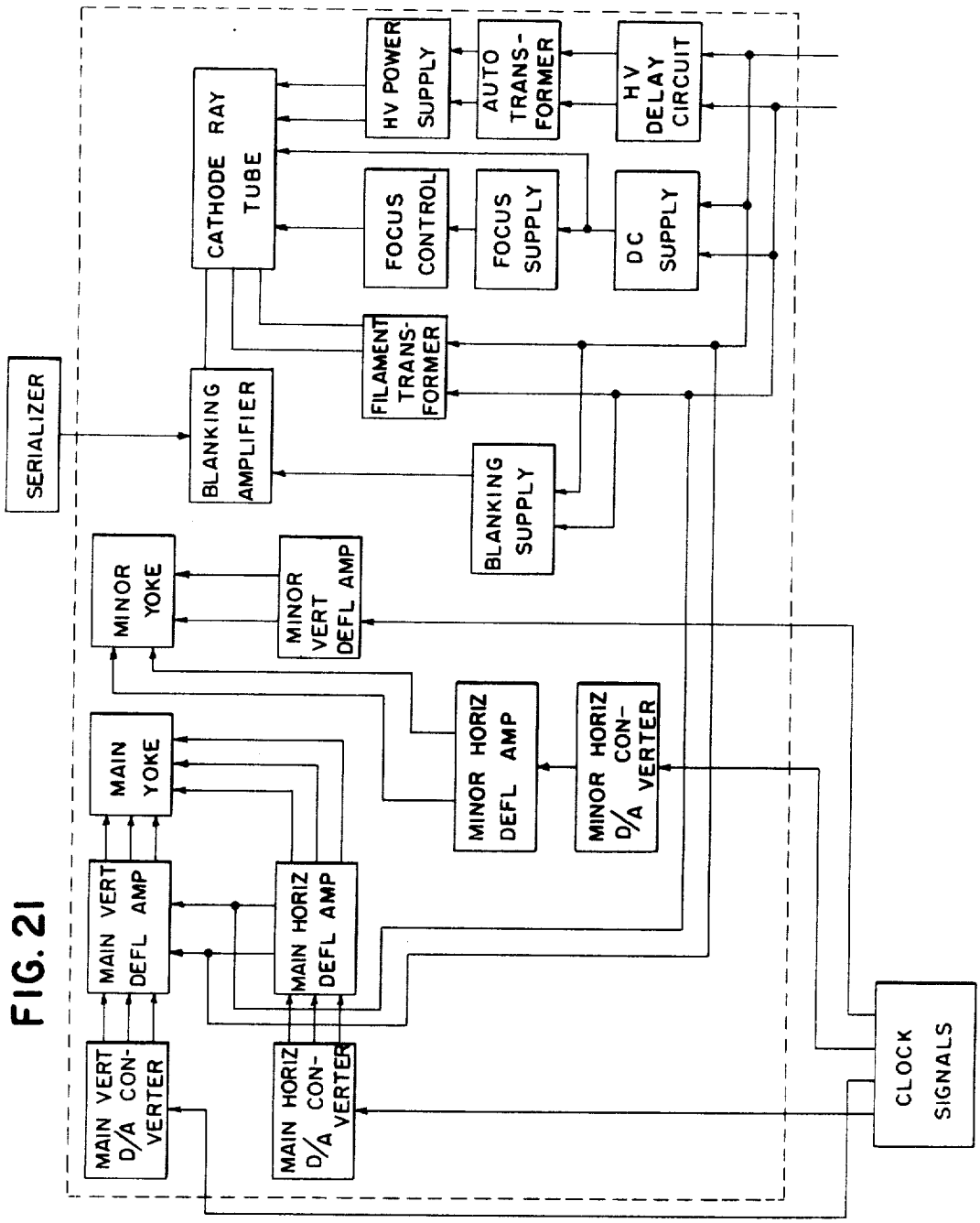



FIG. 21

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# CHARACTER CODING, MEMORY, AND DISPLAY SYSTEM

The Invention herein described was made in the course of or under a contract or subcontract thereunder, with the Department of the Air Force.

This invention relates to apparatus designed to transmit information in the form of a bit code to a remote station and which is further designed to receive and store information from said remote station. More particularly, the invention relates to a memory system and associated display circuitry which enables a message to be composed, visually displayed and edited in the memory over a relatively long period of time and, in response to an appropriate transmission order, to transmit the composed information over a relatively short period of time. However, the invention is not necessarily so limited.

The present invention has been evolved to meet the needs of a communication system in which a message is composed by introducing coded character information into a memory, inspected by using the coded information in the memory to control a character display such as can be produced with a cathode ray tube, transmitted in composed form by suitable means such as frequency modulated radio frequency signals, and imprinted in decoded character form as transmission occurs to permanently record each message transmitted. A requirement for the system is that the system equipment stand ready at all times to receive information directed to the system from a remote station. A further requirement of the system is an ability to print out in the form of a decoded permanent record any information which has been received thereby.

An important ingredient for a system having the foregoing capabilities is a memory circuit which enables retention of messages being composed, which enables editing of messages as they are being composed, which enables retrieval of the composed message an indefinite number of times for refreshing a cathode ray tube display and which at all times stands prepared to preferentially receive new information or messages from remote stations.

An object of the present invention is to provide a new and improved memory system.

Another object of the present invention is to provide a clock control operating in combination with a memory system to divide the memory capability of the memory system between composed and received messages.

Still another object of the present invention is to provide a continuously circulating or cyclic memory and means to insert new information into the memory at appropriate time intervals or slots within the circulating memory so as to enable retrieval of information from the memory always in the proper sequence.

A further object of this invention is to provide improved circuitry for converting the six bit data representing each character to a serial data stream which has its data properly organized for further conversion to a rectangular dot matrix capable of representing the actual character encoded for purposes of display, print-out, and the like.

By way of example, the present invention is adapted to convert the six data bits representing a single character to a serialized stream of thirty-five bits convertible to a 5 × 7 dot matrix.

A still further object of the present invention is to provide a cathode ray tube display unit having a major raster system for locating the positions of characters to be displayed by the cathode ray tube and having a minor raster system for converting serialized bit information to a rectangular dot display at each character position selected by the major raster system.

More particularly, the cathode ray tube display unit of the present invention has among its objects the creation of a major raster which progressively selects 384 character positions organized in twelve lines each comprising 32 character positions, and the display at each character position of a selected character arranged within a 5 × 7 dot matrix or minor raster, the display being cycled indefinitely to continuously refresh the cathode ray tube display.



Other objects and advantages reside in the construction of parts, the combination thereof, the method of manufacture and the mode of operation, as will become more apparent from the following description.

In the drawings,

FIG. 1 is a chart illustrating a six bit code employed in the present invention.

FIG. 2 is a schematic drawing of a keyboard mechanism used in the present invention to produce the appropriate six bit code for each character key depressed on the keyboard.

FIG. 3 is a block diagram split in two parts designated FIG. 3A and FIG. 3B illustrating the inter-relationship of circuits employed in the present invention.

FIG. 4 is a block diagram illustrating the inter-relationship of clock signals employed in the present invention.

FIG. 5 is a schematic illustration of input control circuits employed in the present invention, the Figure being split in two parts designated FIG. 5A and FIG. 5B.

FIG. 6 illustrates a flip-flop counter, herein designated the Tx counter, which is used to account for characters received in the memory of the present invention, this Figure being split in two parts designated FIG. 6A and FIG. 6B.

FIG. 7 is a schematic illustration of control circuitry employed in formatting the memory of the present invention.

FIG. 8 is a schematic illustration of a second flip-flop counter, herein designated the Tx complementary counter, which is employed to insert character information in proper slots of the memory of the present invention, this Figure being split in two parts designated FIG. 8A and FIG. 8B.

FIG. 9 is a diagrammatic illustration of the shift register portion of the memory employed in the present invention.

FIG. 10 is a schematic illustration of a memory buffer and associated gates employed in the present invention, this Figure being split in two parts designated FIG. 10A and FIG. 10B.

FIG. 11 is a schematic illustration of a gate assembly for use in formatting the memory.

FIG. 12 is a schematic illustration of a preset gate assembly for the Tx counter.

FIG. 13 is a schematic illustration of representative gates for decoding the six bit code employed in the present invention.

FIG. 14 is a chart illustrating the relationship between the decode gates of FIG. 13 and the six bit code diagrammed in FIG. 1.

FIG. 15 schematically illustrates circuitry for converting character data decoded with the gates of FIG. 13 to a 35 bit code.

FIG. 16 is a schematic diagram illustrating the development of the 35 bit code.

FIG. 17 is a schematic diagram of circuitry employed to serialize the foregoing 35 bit code, this Figure being split in two parts designated FIG. 17A and FIG. 17B.

FIG. 18 is a circuit diagram of the horizontal control for a major display raster, this circuit diagram being split in two parts designated FIG. 18A and FIG. 18B.

FIG. 19 is a circuit diagram of a vertical control for the major display raster, this circuit diagram being split in two parts designated FIG. 19A and FIG. 9B.

FIG. 20 is a circuit diagram of a minor raster control for tracing 5 × 7 character display matrices at character sites selected by the major raster circuitry, this Figure being split in two parts designated FIG. 20A and FIG. 20B.

FIG. 21 is a block diagram illustrating the operation of a cathode ray tube display circuit embodying the foregoing major and minor rasters.

To provide a suitable format within which to describe the present invention, FIG. 1 illustrates a representative type of code for character information which is suitable for use in the present invention. The code is conventionally referred to as a six bit code. Each bit is a binary bit which can have either a "zero" or a "one" state. The terminology used herein to describe the possible states of each bit is somewhat arbitrary since others in the trade may use such terms as "true and false" or "on and off" or "positive and negative" in reference to the states which each bit in the code can occupy.

An inspection of FIG. 1 will reveal that the six bit code has been organized to allow encoding of various alphabetic and numeric characters and punctuation symbols so as to enable encoding of conventional messages. It can be noted that the six bits 1, 0, 0, 0, 0, 0 (in order, starting with the sixth bit) represent a space as might be employed to separate two words. The letter "R" for example is represented by the bits, in order, 0, 1, 0, 0, 1, 0. In all, the six bit code is organized the represent 60 letters, numbers, punctuation marks, etc., and three control characters.

The three control characters have been enclosed in boxes for easy recognition. One of the control characters is a sinusoidal line enclosed in a box. This character is represented by the bits 0, 1, 1, 1, 0, 0. As will be more fully explained in a latter part of this description, this control character is a line advance character which causes the message to be continued on a following "line" and simulates the function of a carriage return on a typewriter.

A second control character is represented by a caret enclosed in a box and comprises the bits 0, 1, 1, 1, 1, 0. As will later be explained more fully, this control character is introduced into the memory for the purpose of reporting out of the memory the end of a message.

The third control character appears in FIG. 1 as a horizontal line enclosed in a box and is represented by the bits 0, 1, 1, 1, 1, 1. This control character is introduced into the memory to identify and report out the start of a message.

One of the "characters" which is within a box is a slanted line represented by all bits "zero." This control character is a nonfunctional "null" character which allows the system to have a keyboard arrangement which is of conventional appearance.

The preferred character source for introducing the 60 possible characters and three operative controls into the memory is a keyboard, not shown, resembling a typewriter keyboard. Instead of having keys which operate typewriter key bars, however, a keyboard useful in the present invention utilizes keys which position mirrors to reflect appropriately directed light beams upon photoresistive elements which undergo a marked change in resistance upon exposure to light. Such a keyboard arrangement is shown schematically in FIG. 2.

Thus, FIG. 2 illustrates a keyboard key 1 which represents the character "R." Attached to the key 1 is a mirror 2 which can be positioned by depressing the key 1 against a spring load (not shown) to interrupt and reflect a light beam shown schematically at 3. With the key 1 depressed, the light beam is reflected upon a photoresistive element 4 to substantially reduce the resistance thereof to a ground terminal 6. The ground terminal 6 connects through the photoresistive element 4 to an encoder board 5. The board 5 supports six conductive output lines labeled B1, B2, B3, B4, B5 and B6. These output lines deliver the six bits of information which will report that the character "R" has been depressed on the keyboard and is to be introduced into the memory system.

Referring particularly to the output line B1, this line connects through a conductor 11 and a resistor 8 to a voltage terminal 7. Within the framework of the present disclosure, this voltage terminal is a positive terminal.

The terminal 7 has reference to a ground at 10 through a diode 9 which blocks current flow to ground.

One end of the conductor 11 connects to a terminal 13 which is isolated from ground. The opposite end of the conductor 11 serves as an input to a NAND gate 14 connected as an inverter. The presence of a positive voltage on the line 11 causes the NAND gate 14 to output a low voltage, which is essentially ground, to its output 15. This voltage serves as an input to a second NAND gate 16, which also serves as an inverter, applying a positive voltage to its output at 17.

A separate voltage supply and gate structure which is identical to that described with reference to the bit line B1 is provided for each of the other bit lines B2 through B6. The voltage source and gate structures for the bit lines B2, B3, B4 and B5 have been eliminated to conserve space in the drawings.

It will be noted that the bit lines B1, B3, B4 and B6 are ganged together by the conductor 18. Since these bit lines have no connection to the photo-resistor 4, they will be unaffected by depression of the key 1 and their outputs, as at 15, will remain essentially at ground level irrespective of the position of the key 1.

The bit lines B2 and B5 on the other hand, are connected by the diodes 20 and 21, respectively, to the photo-resistor 4. When the key 1 is depressed, the reflection of light to the photo-resistor 4 substantially reduces the resistance between ground and the bit lines B2 and B5. As a result, the input to the NAND gates 14 associated with these bit lines will drop essentially to ground and the outputs from these NAND gates will shift to a positive voltage. Accordingly, the NAND gate 14 outputs from the bit lines B1 through B6 will be, in order, 0, 1, 0, 0, 1, 0 when the key 1 is depressed. Reference to FIG. 1 will show that this pattern of output lines represents the code for the character "R."

There is one NAND gate 16 for each of the bit lines. When the key 1 is not depressed, all of the NAND gates 16 have a positive voltage or "one" output. These NAND gates are ganged together as a wired OR by means of the conductor 22 which applies the positive voltages of the outputs of the NAND gates 16 to a one-shot 23.

When none of the keyboard keys are depressed, the voltage on the conductor 22 charges a capacitor in the R-C timing circuit, not shown, of the one-shot 23. When the key 1 is depressed, the NAND gates 16 associated with the bit lines B2 and B5 effectively ground the conductor 22. This releases the R-C charging circuit of the one-shot 23, causing the one-shot to generate a timed pulse on the conductor 24.

As will be more fully explained in ensuing remarks, the pulse generated by the one-shot 23 is used as a strobe to advance the six bit code generated by depression of the character "R" toward the memory system of the present invention. For convenience, the strobe will hereinafter be referred to as the strobe K.

It will be noted of course that generation of the strobe K by means of the one-shot 23 has not altered the coded information appearing on the outputs 15 of the NAND gates 14. Such information remains constant so long as the key "R" is depressed.

While FIG. 2 illustrates only the character key for encoding the letter "R," it will be understood that each of the other characters depicted in FIG. 1 has a comparable key, photo-resistor and encode board for encoding the appropriate code depicted for each character appearing in FIG. 1. Thus, all "zero" bit lines for each code are produced by isolating the bit lines as at the terminal 13 and all "one" bit lines that may be required are produced by connecting the bit lines to the photo-resistor for the particular character key that will be depressed.

Regardless of the key depressed, except the null key, it is desired that the strobe K be fired and this requires that for each key at least one of the bits produced thereby shift to a "one" when the key is depressed, thus allowing a NAND gate comparable to the gate 16 to effectively ground the line 22 and thereby trigger the one-shot 23. Since the null key previously described produces a code comprising all "zeros," the strobe K is not generated when the null key is depressed. As will appear more fully in the following, the strobe K is required to advance information generated by operation of the key toward the memory and accordingly depression of the null key, which fails to generate a strobe, has no influence on the memory.

In addition to the 64 character keys depicted in FIG. 1, the keyboard contains additional keys which perform control functions but are not advanced into the memory system. These keys are a reset key, a clear display key, a clear transmit key, a clear receive key, a send key, and a backspace key. The specific functions of these keys will be described at appropriate intervals throughout the following description. It suffices to note for the present that each of the foregoing control keys is associated with a circuit that is grounded to output

a "zero" until the key is depressed, whereupon the circuit to which the particular key depressed is associated is switched to a "one" input. Also with the exception of the backspace key, no strobe pulse is generated.

In order to advance the coded information produced at the keyboard into the memory system of the present invention, a series of clock frequencies and associated logic circuitry regulated by means of the clock frequencies is provided. Except for clock signals associated with a master control system which coordinates the present apparatus with remote apparatus, as will be explained in a later portion of this description, all clock signals used in the present apparatus are derived from a crystal controlled oscillator in a manner schematically represented in FIG. 4. The signal from the crystal controlled oscillator, which is desirably in the megacycle range, is first divided by three through a divide-by-three counter to produce a clock identified by the reference character C1. This clock C1 is divided by ten through a five flip-flop counter designated the A counter to produce a clock designated C2. This clock C2 is in turn divided by six through a three flip-flop counter designated the B counter to produce a clock designated C3.

The clock C3 is again divided by 36 through a six flop-flop counter designated the D counter to produce a clock designated C4. The clock C4 is further divided by twelve through a four flip-flop counter designated the E counter to produce a clock designated C6.

As noted, the D counter is a six flip-flop counter. By means of a gate G10 the D counter is caused to output a clock C5, which can be represented in Boolean algebra as $\overline{D6\,(D1+D2)}$ (C3). As understood by those skilled in the art, this expression tells that the state of the flip-flop representing the sixth stage of the D counter is ANDed with the state of the first stage flip-flop or the state of the second stage flip-flop, inverted, and the resultant signal ANDed with the clock C3 to produce the new clock C5. The clock C5 is essentially the clock C3, but during the time the clock C3 provides 36 pulses, the clock C5 will duplicate the clock C3 for 33 pulses, then skip three pulses. In practical effect, the clock C5 is an adjustment of the clock C3 to provide a clock which exactly conforms to the memory capacity, as will be more fully explained in succeeding remarks.

Throughout the following specification, various clock characteristics derived from the counters illustrated in FIG. 4 will be expressed in Boolean language. Whenever the Boolean expression for a clock characteristic includes a counter state, the state will be identified by an asterisk (*). The D counter, for example, has six flip-flops connected to "count" through 36 states. The expression: Do* refers to the first count level of the D counter. The expression D35* refers to the 36th state. Whenever the Boolean expression for a clock characteristic includes the state of a particular flip-flop in a particular counter, the flip-flop is designated by the letter which identifies the counter in which the flip-flop appears and a suffix identifying the position of the flip-flop in the counter. Thus, D1 expresses that the first flip-flop in the D counter is in its "one" state. $\overline{D1}$ correspondingly designates that the first flip-flop in the D counter is in its "zero" state.

For the purpose of illustrating the present invention, the memory system will be described as one capable of storing three hundred 96 characters. As discussed previously, each character is coded in the form of six bits. To enable storage of all six bits representing each character, the memory is constructed with six shift registers each capable of shifting through 395 states. The six shift registers are shifted in parallel by the clock C5 and, for convenience hereinafter, each shift register state may sometimes be referred to as a memory cell.

All information input to the memory is input from a memory input buffer which comprises six flip-flops, each flip-flop being set to represent one of the six bits of information which is to be placed into the memory. Each set of six bits (representing one character) present in the memory buffer is introduced in parallel to the six shift registers. Each set of six bits representing a character in the memory is clocked through the six shift registers in side-by-side unison relation by the C5 clock. When a given set of six bits representing one character has progressed all the way through the 395 memory cells, provided by the shift registers, it is returned to the memory buffer, where a number of different output functions may be performed, and then, unless the character is to be removed from the memory, returned to the shift registers to be clocked therethrough once again by the C5 clock. Since all the character information being clocked through the shift registers also passes through the memory buffer, the memory buffer represents in effect a 396memory cell.

There are two modes for introducing character information into the memory. One mode is by way of the keyboard previously described. With respect to the clock C5, the keyboard input is asynchronous. For each set of six bits representing a character received from the keyboard, it is first necessary to advance the six bits of information to a keyboard buffer in such fashion that the six bits of information can be synchronized with the clock C5 and then introduced to the memory at precisely the time interval required to place the information in proper relation to preceding information already present in the memory. Thus, if one is seeking to introduce the work "THE" to the memory, one would first depress the keyboard key representing "T." If this is the first character to be received in the memory, the six bits of information representing the letter "T" must be entered into the first cell available in the memory.

The clock C5 may cycle this first character through the memory any random number of times before the character "H" is depressed on the keyboard. When the character "H" is depressed, it is required for proper operation of the present circuit that the six bits representing the character "H" be introduced into the memory in precisely the next memory cell following the character "T."

Again, the "T" and the "H" may cycle one after the other through the memory a number of times before the letter "E" has been depressed on the keyboard. When the letter "E" is depressed, it is again required that the six bits of information representing the letter "E" be introduced into the memory at precisely the memory cell which immediately follows the character "H" already in the memory.

Thus, the circuitry of the present invention is required to fit characters received from the keyboard at random time intervals into precisely arranged cells within the memory system. As will appear more fully, the cells are spaced in time by the C5 clock and one challenge to the circuitry of the present invention is to determine at what pulse of the C5 clock new information should be introduced into the memory.

It was previously mentioned that there are two modes for introducing character information into the memory. The second mode comes into operation upon receipt of frequency modulated information from a remote station. This information is received in six parallel channels each representing one bit of the six bit character code. The means for encoding such information for radio frequency transmissions on six parallel channels (i.e., six RF frequencies) is well known in the art and forms no part of the present invention. For the purposes of the present invention, such information is transmitted at only random times, but in proper sequence, and introduced to the memory in substantially the same fashion as if the information had come from the keyboard.

There is one important difference between messages composed at the keyboard and messages received by broadcast from a remote station. The "E" counter is assembled with four flip-flops, of which three are connected together as a divided-by-six shift counter, causing the fourth to be "zero" for a count of six pulses of the D counter and then "one" for a count of six pulses from the D counter. During the time the fourth flip-flop is at the "zero" output level, only keyboard information can be entered into the memory. Correspondingly, when the fourth flip-flop is at the "one" level, only externally received information can be introduced into the memory. Since the preceding counter is the divide-by-thirty-six D

counter (see FIG. 4), the practical effect of the E counter is to create $6 \times 36 = 216$ time slots for entry of keyboard information and 216 time slots for entry of externally received information.

As will be more fully explained later, all information is clocked through the memory with aid of the C5 clock, which skips three out of each 36 pulses from the C3 clock. This skip feature of the C5 clock is used to remove eighteen time slots from the time allotted for keyboard memory and another eighteen time slots from the time allotted for memory of externally received information.

Thus, the memory system is so divided by operation of the E counter that only 198 keyboard characters can be stored and only 198 externally received characters can be stored.

As previously noted, the operation of any of the aforementioned 64 character keys, other than the null key, generates a positive strobe or pulse K. With reference to the block diagram of FIG. 3, it can be seen that the strobe K passes from the keyboard to a block identified "Control Logic." At the same time the six bits of information produced by depression of the key which generated the strobe K are presented to a set of "-Buffer Gates" 19 which will be used to gate the six bits of information at an appropriate time to a flip-flop storage device identified as a "Keyboard Buffer" and by the reference character 35. FIG. 3 shows a single line 25 extending between the keyboard and the aforementioned buffer gates. This single line is drawn for simplicity since in fact six parallel lines are required to present the six bits of information selected by depression of the character key to the buffer gates.

The control logic to which the strobe K is presented is schematically illustrated in FIG. 5. There it can be seen that a terminal identified by the reference character K presents the strobe K to a NAND gate G1. As will more fully appear in a succeeding portion of this description, the gate G1 inverts the strobe K and passes $\overline{K}$ to a gate G2 only when the circuit logic is in a condition to permit composition of messages from the keyboard, this being hereinafter referred to as a compose mode of operation.

Assuming the circuitry is in the compose mode of operation, the strobe $\overline{K}$ passes to gate G2 which serves as an inverter to restore the strobe K to a positive pulse. At the same time a line 27 conducts the strobe $\overline{K}$ to the "K" input of a flip-flop F1. The inverted strobe $\overline{K}$ emanating from the gate G2 is applied to the "J" input of the flip-flop F1. Throughout this application language and illustrations conventional in the art will be employed with respect to flip-flops. Thus, the flip-flop inputs will be described as "J" and "K" inputs and the flip-flop outputs, where particularly mentioned, will be described as Q and $\overline{Q}$ outputs.

The flip-flop F1 does not respond to its "J" and "K" inputs until a clock signal identified by the Boolean symbol AO* is received at its clock input 26*a* from terminal 317. This clock signal occurs each time the A counter is at its "zero" state, i.e., its first count level. Since the crystal oscillator operates in the megacycle range, the A counter will output an AO* signal thousands of times per second and the K strobe is timed by the one-shot 23 to assure clocking of F1 during the life of any K strobe. When the K strobe is clocked into F1, F1 is set to output a "zero" to a gate G3.

The gate G3 is thus forced to a "one" output, which is applied to one input of a gate G4. As will be explained later, the gate G4 will invert and pass the F1 output only when space is available in the memory to receive the character information from the key that has been depressed.

Assuming space is available in the memory, the gate G4 passes to terminal 28 a negative-going pulse designated $\overline{A}$. The $\overline{A}$ pulse has a width determined by the first AO* pulse to arrive after the K strobe has terminated. Terminal 28 also appears in FIG. 7, where the $\overline{A}$ pulse is inverted through a NAND gate G11, and applied to a one-shot 30 for the purpose of generating a reshaped and narrower strobe $\overline{A}$. The strobe $\overline{A}$ is applied to a terminal 29 which also appears in FIG. 6.

FIG. 6 schematically illustrates a counter mechanism hereinafter identified as the Tx counter. The Tx counter is employed, in part, to count the number of characters stored in the memory and report when the memory is full. In order for the strobe $\overline{A}$ to initiate action by the Tx counter, however, other events described below must have occurred.

Referring to FIG. 5, the inverter gate G2, when passing the K strobe to the flip-flop F1, also passes the K strobe to NAND gates designated G6 and G8. For reasons to be later explained, the NAND gate G6 normally has a "one" at its other input and thus outputs a "zero" to a NAND gate G7. The NAND gate G7 thus disabled outputs a "one" to the "J" input of a flip-flop F2.

The NAND gate G8 normally has a "zero" from the terminal 77 and accordingly outputs a "one" to a NAND gate G9 which operates as an inverter to apply a "zero" to the "K" input of the flip-flop F2. The "J" and "K" inputs to the flip-flop F2 are also clocked by means of the aforementioned AO* pulse.

The flip-flop F2 is used to tell the aforementioned Tx counter whether it should count up or down. With the "J" and "K" inputs "one" and "zero," respectively, as described, the flip-flop F2 outputs a "one" from its Q output to terminal 31*a* and "zero" from its $\overline{Q}$ output to terminal 31*b*. As will be described, these "one" and "zero" signals will condition the Tx counter to augment its count.

The situation is reversed when the keyboard backspace key has been depressed. As previously mentioned, the backspace key generates a K strobe when depressed. It also shifts a normal output of "zero" to a "one" on the terminal 77 in FIG. 5. The normal output of "zero" on terminal 77 is inverted through gate G12 and thus provides the normally "one" input to one terminal of the gate G6, as was previously described. At such time as the backspace key is depressed, the shift of the terminal 77 from a "zero" to a "one" disables the gate G6 and enables the gate G8, thus reversing the "J" and "K" inputs to the flip-flop F2 and thereby reversing the outputs from the flip-flop F2 to the terminals 31*a* and 31*b*. This reversal in the output of the flip-flop F2 upon depression of the backspace key is used to condition the Tx counter to decrease rather than augment its count.

It is considered for the present that the outputs of F2 are "one" and "zero" to the terminals 31*a* and 31*b*, respectively. These signals are applied to terminals 31*a* and 31*b*, respectively, of FIG. 6.

FIGS. 6*a* and 6*b* collectively represent the aforementioned Tx counter which comprises flip-flops H1, H2, H3, H4, H5, H6, H7 and H8. The previously described strobe $\overline{A}$ is applied to terminal 29 in FIG. 6, in inverted in the two wide, two input AND-OR-invert gate G13 and applied to the clock input of the flip-flop H1. The H1 flip-flop changes states since both of its "J" and "K" inputs are held at a "one" by gating to be later described. The Q output of H1 is ANDed with the "one" signal from terminal 31*a* and the $\overline{Q}$ output of H1 is ANDed in gate G14 with the "zero" from terminal 31*b*. H2 will be clocked by the output of G14 only if H1 was previously in its "one" state. Similar gates G15, G16, G17, G18, G19 and G20 are provided for clocking the flip-flops H3, H4, H5, H6, H7 and H8, respectively. Since, under the assumed conditions, terminal 31*b* is at a "zero" level, it holds off that side of all the gates G14 – G20 associated with the $\overline{Q}$ outputs of the H2 through H8 flip-flops. Terminal 31*a*, being a "one," opens up the other sides of the gates G14 – G20, allowing the Q outputs of the Tx counter flip-flops each to clock the following stage as in any binary counter operating in the "up" count direction. So long as the terminals 31*a* and 31*b* remain unchanged, the Tx counter will count upwardly one count for each successive depression of a character key on the keyboard.

As will be explained subsequently, the Tx counter has a count limit of 198 counts and, by means of gating, performs a formatting function after each 32nd count it receives, but the basic principle to be recognized now is that, as each successive character key is depressed, the Tx counter records the fact

that a new six bit character code has been made available to the memory.

For the purposes of describing the manner in which the six bit character code is put into the memory of the present invention, it will be assumed that the memory is presently empty of any character code and a first character key has been depressed so as to present the six bit code representing the character key depressed to the buffer gates **19** shown in FIG. **3**.

At the time the K pulse generated by this first character key appeared from gate G2 on line **27** in FIG. **5**, this pulse was inverted through gate G21 to produce an inverted pulse, herein identified as strobe $\overline{Y}$, on the output of gate G21 to terminal **32**. The strobe $\overline{Y}$ to terminal **32** appears in FIG. **6** where it is inverted to Y through gate G22 and passed on conductor **33** to a terminal **34** shown in FIG. **6**. This Y strobe is applied to the buffer gates **19** (see FIG. **3**) to gate the six bit information received from the keyboard to a keyboard buffer identified by the reference character **35**. Those skilled in the art will understand that the keyboard buffer is an assembly of six flip-flops which are set by the strobe Y to hold the six bit code from the keyboard for an indefinite period. The manner of gating the six bit code to the keyboard buffer and setting its six flip-flops to hold the code is well established in the art and therefore not described in further detail.

The keyboard buffer **35** presents the six bit code being held thereby to further buffer gates identified by the reference character **36** (see FIG. **3**). The foregoing events proceed in a very short increment of time as the T*x* counter is being caused to count "up." The six bit code remains in the keyboard buffer until such time as each of the timing counters A, B, D and E is simultaneously at its "zero" state.

When each of the A, B, D and E counters is simultaneously at its "zero" state, this condition is decoded by conventional gating, not shown, as $\overline{AO^*\ BO^*\ DO^*\ EO^*}$ to produce a negative-going pulse on the conductor **39** (see FIG. **3**). This pulse, hereinafter called the "transfer" pulse, is applied to a set of gates adapted to transfer the complement of whatever count then resides on the Tx counter to a counter designated the T*x* complementary counter. The aforementioned gates and the T*x* complementary counter are illustrated in FIG. **8**. The T*x* complementary counter comprises eight flip-flops labeled **J1**, **J2**, **J3**, **J4**, **J5**, **J6**, **J7** and **J8**. The transfer of a complementary count from the T*x* counter flip-flop **H1** to the T*x* complementary counter flip-flop **J1** proceeds as follows.

Referring to FIG. **6**, the $\overline{Q}$ output of flip-flop **H1** is connected to a terminal **38**. The $\overline{Q}$ output of flip-flop **H1** is connected to a terminal **37**. These terminals also appear in FIG. **8**. When the aforementioned transfer pulse appears at terminal **39***a* in FIG. **8**, this pulse enables gates G**25***a* and G**25***b* which invert the pulse. The gate G**25***b*, now outputting a positive pulse, enables gates G23 and G24 which invert the $\overline{Q}$ and Q signals from the H1 flip-flop to respectively preset and set the J1 flip-flop, thus setting the J1 flip-flop to the opposite condition of the H1 flip-flop. Thus, if **H1** is in a "zero" state at the time of the complementary transfer, **J1** will be placed in its "one" state by the transfer. In similar fashion, by the circuitry shown, the state of each of the flip-flops **H2**, **H3**, **H4**, **H5**, **H6**, **H7** and **H8** is complementarily transferred to the flip-flops **J2**, **J3**, **J4**, **J5**, **J6**, **J7** and **J8**, the NAND gate G**25***b* gating this transfer to the flip-flops **J1**, **J2**, **J3** and **J4** and the NAND gate G**25***a* gating this transfer to the flip-flops **J5**, **J6**, **J7** and **J8**.

Under the assumed condition the T*x* counter has been advanced one count by depression of a first character key, causing the flip-flops **H1** through **H8** to have the following states 1, 0, 0, 0, 0, 0, 0, 0, respectively. Upon the complementary transfer to the Tx complementary counter, the flip-flops **J1** through **J8** will have the states 0, 1, 1, 1, 1, 1, 1, 1, respectively. Obviously the complementary counter is one count away from the condition at which all of its flip-flops are in their "one" state.

The state of each of the flip-flops **J1** through **J8** is input to a NAND gate **G28**. Since at least one of these flip-flops is in a "one" after the above described complementary transfer, gate **G28** outputs a "one," enabling a NAND gate **G26**. The previously described clock **C5** is continuously applied to terminal **40** and thus to the NAND gate **G26**. When the first **C5** clock pulse following the transfer is received, this pulse is inverted and passed by the gate **G26**, re-inverted by an inverter gate **G27**, and applied to the clock input of the flip-flop **J1**. Since, under the condition described, the complementary counter is one count away from a condition in which all of the flip-flops **J1** through **J8** are at "one," this first **C5** clock pulse following the complementary transfer will drive the gate **G28** to a "zero" output since all inputs to the gate **G28** will then be at the "one" level.

When the gate **G28** thus outputs a "zero," the gate **G26** is disabled and further clock pulses to the Tx complementary counter are blocked by the gate **G26**.

The "zero" output of the gate **G28** is inverted through inverter gate **G29** to enable gates **G30** and **G31***b*. Gates **G31***a* and **G31***b* are connected back-to-back to form a NAND gate flip-flop which is set to a "one" when the gate **G28** outputs a "zero." This NAND gate flip-flop in turn sets a NAND gate flip-flop comprising gates **G34***a* and **G34***b* to a "one," with the gates **G32** and **G33** interposing a few nanoseconds delay. The foregoing NAND gate flip-flops force a "zero" on the output of gate **G35**. Gate **G35** having previously output a "one" had charged a capacitor **43**. When the output of gate **G35** switches to "zero," the capacitor discharges through gate **G36**, thus applying a pulse designated the *a* pulse to gates **G37** and **G38**. The condition of the gates **G37** and **G38** is determined by a flip-flop **F3** depicted in FIG. **5** and associated with the input control logic of the present invention. As will be explained at a later point in this description, a necessary adjunct of the compose mode of operation being discussed is that the flip-flop **F3** be in its "zero" state, i.e., its Q output is "zero" and its $\overline{Q}$ output is "one." The Q output of **F3** is applied to terminal **41** in FIG. **5**, while the $\overline{Q}$ output of **F3** is applied to terminal **42** in FIG. **5**. The terminal **41** and **42** in FIG. **5** also appear in FIG. **8**.

Since the flip-flop **F3** is in its "zero" state, terminal **41** in FIG. **8** disables NAND gate **G38**. On the other hand, terminal **42** in FIG. **8** enables NAND gate **G37**. Thus, the *a* pulse is passed, although inverted to a negative-going pulse "$\bar{a}$," by the gate **G37**. This $\bar{a}$ pulse is applied to terminal **44** appearing in FIG. **8**.

From FIG. **8** terminal **44** the $\bar{a}$ pulse is applied to terminal **44** in FIG. **10** where it forces a "one" on the output of NAND gate **G39**. The output of the NAND gate **G39** is used to gate the six bit code presently residing in the keyboard buffer **35** (see FIG. **3**) to a memory buffer **45** also appearing diagrammatically in FIG. **3**. The buffer gates **36** and memory buffer **45** are illustrated schematically in FIG. **10**. Thus, in FIG. **10** the buffer gates diagrammed at **36** in FIG. **3** comprise the AND-OR-invert gates **G40**, **G41**, **G42**, **G43**, **G44**, **G45**, **G46**, **G47**, **G48**, **G49**, **G50** and **G51**. The memory buffer **45** appears in FIG. **10** as comprising the flip-flops **F17**, **F18**, **F19**, **F20**, **F21** and **F22**.

When the gate **G39** in FIG. **10** is disabled by the $\bar{a}$ pulse so as to force a "one" on its output, a conductor **46** relays this "one" level through conductor **47** to one of the AND gates in each of the aforementioned AND-OR-invert gates. Each of the AND gates thus receiving the "one" signal from the gate **G39** which operates as a driver, is energized to transfer bit information from the keyboard buffer to the memory buffer. Recalling that the keyboard buffer comprises a series of flip-flops, not shown, set to store the six bit code received from a character key, each bit value and its complement is gated from the keyboard buffer to the memory buffer when a "one" level appears on the conductor **47**. Thus, bit **B1** as derived from the keyboard buffer is presented to the buffer gates at terminal **48***a* in FIG. **10**. The complement of bit **B1** is presented at terminal **48***b* in FIG. **10**. Likewise, bit **B2** and its complement are presented at terminals **49***a* and **49***b*, respectively, in FIG. **10**; bit **B3** and its complement are presented at terminals **50***a* and **50***b*, respectively; bit **B4** and its complement are presented at

terminals **51***a* and **51***b*, respectively; bit **B5** and its complement are presented at terminals **52***a* and **52***b*, respectively; bit **B6** and its complement are presented at terminals **53***a* and **53***b*, respectively.

Upon receipt of the "one" level on conductor **47**, all bits and their complements are transferred simultaneously through the buffer gates **36** to the memory buffer flip-flops **F17** through **F22**. In this fashion, then, the six bit information previously residing in the keyboard buffer is transferred to the memory buffer upon receipt of the $\bar{a}$ pulse at gate **G39** in FIG. **10**.

As mentioned at an earlier point in this description, the memory buffer comprises one cell of the memory. The remaining cells of the memory are supplied by six shift registers each capable of shifting through 395 states. Each shift register is assembled with twenty monolithic chips utilizing MTOS P-channel enhancement mode field effect transistors. Such chips are commercially available from the General Instrument Corporation of Hicksville, New York, which identifies the chips by the stock designation MEM 3021. By means of external connections, each chip may be connected as a 21 bit shift register, or a 20 bit shift register, or a 16 bit shift register. Other connections are possible, but the aforementioned are the connections used in the present invention.

FIG. **9** diagrammatically illustrates the entire shift register assembly for shifting a single bit of information through 395 memory cells. As displayed in this Figure, the shift register comprises 11 chips connected to shift through 21 states; five chips connected to shift through twenty states; and four chips connected to shift through 16 states. As also displayed in FIG. **9**, the chips are interconnected to shift one to another so as to provide an aggregate of 395 shift register states or memory cells. It is to be understood of course that FIG. **10** illustrates one shift register memory device for storing one bit of the six bit code such as received from the keyboard. Five other identically constructed shift register devices are required to store the other five bits, one shift register device for each bit of the entire six bit code.

For purposes of illustration, it can be assumed that FIG. **9** illustrates the shift register memory used in storing bit **B1** of each character code received from the keyboard.

In order to transfer the six bit code presently being stored in the memory buffer to the shift register memory, it is necessary first to interface the relatively low voltage level digital circuitry of the memory buffer with the relatively high voltage level MTOS circuits of the shift register. The interfacing, shown diagrammatically at **54***a* in FIG. **3**, employs only common techniques well known to those skilled in the art.

It is helpful to recall at this point the sequence of events which followed when the clock counters A, B, D and E reached their "zero" state so as to generate the aforementioned transfer pulse. When the transfer pulse occurred, the count of one in the *Tx* counter was complementarily transferred to the *Tx* complementary counter. After the transfer, the complementary counter was one count removed from its maximum count of 255, a lock-up state. Responding to the **C5** clock, the complementary counter reached its lock-up state on the first **C5** pulse following the transfer pulse. Immediately after the complementary counter reached its lock-up state, and before another **C5** pulse could arrive, the $\bar{a}$ pulse was generated to gate the six bit code residing in the keyboard buffer to the memory buffer. The memory buffer is clocked by the **C5** clock applied to terminal **40** in FIG. **10**. The **C5** clock is also applied to terminal **40** of the shift register illustrated in FIG. **9**. On the second **C5** clock pulse following the transfer pulse, the six bits of information transferred to the memory buffer after the first **C5** pulse are clocked out of the memory buffer to the six shift registers comprising the shift register portion of the memory. Thus, with reference to bit **B1**, the complementary "J" and "K" inputs of the flip-flop **F17** are applied to the interface **54***a* so as to inject the value of bit **B1** to terminal **100** of FIG. **9**, this bit value being clocked into the first cell or shift register state of the FIG. **9** shift register at substantially the same instant that the bit value is clocked out of the memory buffer. At the same time each of the bits **B2**, **B3**, **B4**, **B5** and **B6** is clocked into corresponding shift registers such as shown in FIG. **9**, the bits thus being clocked in parallel from the memory buffer to the shift register portion of the memory.

Directing attention only to the initial six bit character introduced into the memory, the character is advanced in successive steps through each cell or state of the shift register memory with successive pulses from the **C5** clock. There will be a total of 396 **C5** clock pulses following the AO* BO* CO* DO* pulse which transferred the character to the memory buffer before the clock system returns to its AO* BO* DO* EO* state. The character entered the memory buffer on the "first" **C5** pulse, which accompanied the AO* BO* DO* EO* state, entered the first cell of the shift registers on the second **C5** pulse, and will be lodged in the 395 cell of the shift registers after the 396 **C5** pulse. On the 397 **C5** pulse following the transfer, character information is returned from terminal **101** (FIG. **9**) to the memory buffer through an interface **54***b* illustrated diagrammatically in FIG. **3**. The interface **54***b* is of a conventional design well known to those skilled in the art and merely re-adjusts the signal level to one acceptable by the memory buffer. Assuming operating modes to be subsequently described will not erase the character information from the memory buffer at this time, the next ensuing pulse from the **C5** clock will return the six bit character information to the shift register portion of the memory and ensuing **C5** pulses cycle the character information again through the memory. The character information will cycle indefinitely through the memory, advancing with each pulse of the **C5** clock.

As a typical example, the crystal controlled oscillator illustrated in FIG. **4** may have a frequency of 4 megacycles per second. Based on this basic clock frequency, a given character will cycle through the memory approximately 54 times per second. As this memory cycling continues, a lock-out mechanism blocks the aforementioned transfer pulse, which will be generated by the clock system once each cycle, from again implementing a character transfer until another keyboard key has been depressed.

As the first character introduced to the memory cycles an indefinite number of times through the memory, the Tx counter holds its count of one and the Tx complementary counter remains locked up to its count of 255. Assuming a keyboard operator in the process of composing a message presses a second character key on the keyboard, a second K strobe will be generated and the six bits of information representing the character for the second key depressed will be advanced to the keyboard buffer in the manner previously described. The *Tx* counter will also have its count augmented to a count of two in the manner previously described. The first time after this second character key is depressed that the clock system reaches its state AO* BO* DO* EO*, the count of two in the Tx counter will be transferred complementarily to the Tx complementary counter, whereby the complementary counter will then have a count therein of 253. At this instant the single character already in the memory will be lodged in the 395 shift register cell. After the first **C5** pulse following the complementary transfer from the Tx counter, the *Tx* complementary counter will have advanced to count 254 and the first character introduced in the memory will have residence in the memory buffer. After the second **C5** pulse following the transfer, the first character introduced to the memory will be lodged in the first shift register cell, the *Tx* complementary counter will have reached its count of 255 generating an $\bar{a}$ pulse and the second character will be injected to the memory buffer so as to immediately follow the first character throughout the memory system.

When a third character key is depressed by the operator, the complementary transfer from the *Tx* counter to the *Tx* complementary counter, occurring under control the circuitry previously described, will automatically place the third character into the memory immediately behind the second

character. Thus, as successive character keys are depressed on the keyboard, the six bit information produced by each key will be entered in orderly fashion one character behind the other into the memory system.

It will later be described how the character information stored in the memory is used to continuously refresh a cathode ray tube display. The cathode ray tube display unit is designed to display six lines each comprising 32 characters of information received from the keyboard and an additional six lines each comprising 32 characters of information externally received. For the purpose of properly formatting the cathode ray tube display, each line of 32 characters is followed by a 33 character designated the line advance character. One function of the line advance character, as will be later explained, is to set aside time for the cathode ray tube display unit to retrace in preparation for the display of succeeding characters in the memory on a next lower line of the cathode ray tube display.

As a message is being composed from the keyboard, there are two ways the line advance characters can enter the memory. One is automatic entry of the line advance character, which occurs automatically and promptly after the 32 character of any given line has been depressed on the keyboard. In the other case, an operator may wish to display less than 32 characters in a given line. This is accomplished by depressing the keyboard character previously identified as the line advance character.

In describing the automatic insertion of the line advance character to the memory, it is helpful to assume that a keyboard operator, in composing a message has entered 31 characters into the memory and then depresses a 32 keyboard character. For reasons previously discussed, depression of the 32 character will cause production of an $\bar{A}$ strobe which will augment the count of the T*x* counter to 32. When the clock counter system has next reached the state AO* BO* DO* EO*, this count will be complementarily transferred into the T*x* complementary counter so as to select a time for entry of the six bit code representing the 32 character into the proper slot of the memory. However, before this selection can occur, a gate G52 in FIG. 6 will recognize that a count of 32 exists in the T*x* counter. The gate G52 outputs a "one" to its terminal 55 at all times except when the 32 count has been entered into the T*x* counter. When the 32 count is entered, however, the output of gate G52 goes to a "zero." This output is applied to terminal 55 of a six input NAND gate G53 illustrated in FIG. 11. This NAND gate normally outputs a "zero" but is driven to a "one" when the NAND gate G52 outputs a "zero."

The NAND gate G53 is intended ultimately to enable a NAND gate G54 (FIG. 11) for the purpose of introducing the line advance character to the memory, but because even the 32 character will not yet be in the memory, it is necessary to delay the circuitry which introduces the line advance character to the memory for a time sufficient to insure that the 32 character has entered the memory.

Several factors cooperate to afford the necessary delay. Associated with the E counter is a control flip-flop, not shown, which is used to inhibit transfers from the T*x* counter to the T*x* complementary counter at all times except those times when a new character has been entered into the keyboard buffer. This inhibition is accomplished by NANDing the state of the control flip-flop with the AO* BO* DO* EO* pulse from the clock counters. The control flip-flop is normally conditioned to its "zero" state so as to block the transfer pulse AO* BO* DO* EO*. Each time a character key is depressed so as to generate an $\bar{A}$ strobe, however, the $\bar{A}$ strobe is used to set the control flip-flop to its "one" state so that the next ensuing clock pulse, AO* BO* DO* EO*, can pass to the terminal 39*a* (FIG. 8) so as to effect a transfer from the T*x* counter to the T*x* complementary counter. A later counter state [A2* BO* DO* EO*] is permitted to reset the control flip-flop to its "zero" state. Accordingly, from the time the 32 character key is depressed until promptly after the complementary transfer from the T*x* counter to the T*x* complementary counter, the control flip-flop is in its transfer enabling state. The $\bar{Q}$ output of this flip-flop, then a "zero," is applied to terminal 66 in FIG. 7 where it disables a NAND gate G57 forcing a "one" output from gate G57 which is inverted to a "zero" by gate G58 also shown in FIG. 7. The resulting "zero" from gate G58 is passed to terminal 57 in FIG. 7 and from there to terminal 57 in FIG. 11. This "zero" from the gate G58 disables gate G54 so that the "one" output from the gate G53 is not recognized and the mechanism for introducing a line advance character to the memory is temporarily blocked.

It is to be recognized that this temporary blockage endures only from the time the $\bar{A}$ strobe is created by depression of the 32 character key until approximately the time that the 32 count of the T*x* counter is complementarily transferred to the T*x* complementary counter.

Recalling the operation of the T*x* complementary counter, the complementary transfer to this counter promptly induces a "zero" output from the gate G28 (FIG. 8) which is inverted by the gate G29 shown in FIG. 8. Gate G29 then supplies a "zero" to terminal 58 in FIG. 11, disabling a NAND gate G55 to force a "one" output therefrom. The "one" output of gate G55 is inverted by gate G56 to disable the gate G54. By this circuitry, blockage of the line advance mechanism is prolonged. This prolonged blockage continues so long as gate G28 in FIG. 8 continues to output a "one" and this output condition will exist until the complementary counter has counted to its full count of 255, thereby having selected the appropriate memory slot in which to insert the 32 character.

Even when the T*x* complementary counter has selected the appropriate memory slot for receipt of the 32 character, further means for blocking the line advance character are required to assure that the six bit code representing the 32 character has entered the memory before the line advance character will enter the memory.

This further delay occurs as follows. A clock signal designated A1* BO* which has the frequency of the C3 clock, although delayed therefrom, is applied to terminal 59 of gate G55. When the T*x* complementary counter has counted to its lock-up state (count 255), the "one" then applied to gate G55 by way of terminal 58 in FIG. 11 enables gate G55 to pass succeeding A1* BO* clock pulses applied to terminal 59 in FIG. 11. The first such clock pulse following the count out of the T*x* complementary counter to its locked-up condition is inverted by gate G55, re-inverted by gate G56, again inverted by gate G54, then again re-inverted by gate G59, clocking a flip-flop F33 to its "one" state. At this point, however, the $\bar{Q}$ output of the flip-flop F33 disables a NAND gate G60 and again, the line advance signal is delayed. On the next A1* BO* clock pulse, however, the flip-flop F33 is clocked to its "zero" state, opening the gate G60 so as to pass the A1* BO* clock signal through an inverter gate G61 to a terminal 60 shown in FIG. 11.

Terminal 60 also appears in FIGS. 7 and 10. The pulse thereon is relayed on conductor 61 in FIG. 10 to previously identified gates G41, G43, G45, G47, G48 and G50 to automatically implant the six bit character code 0, 1, 1, 1, 0, 0 in the memory buffer.

This particular character code has been designated the line advance character. As soon as this character enters the memory buffer, it is recognized by a six bit decode gate mechanism diagrammatically shown at 225 in FIG. 3, and a recognition signal from the decode gate mechanism is immediately applied to terminal 75 in FIG. 7. The signal received at terminal 75 is a positive-going signal, hereinafter referred to as a line feed pulse.

It will be recalled that in order to initiate the line feed pulse, it was necessary for the T*x* complementary counter to count out to its full count of 255 so as to generate an $\bar{a}$ pulse. This $\bar{a}$ pulse is applied to terminal 44 in FIG. 7, inverted in gate G65 and used to clock a flip-flop F34. The "J" and "K" inputs of this flip-flop receive whatever signal exists on terminal 31*a* in FIG. 5. Since the operation now being described is one of message composition from the keyboard, the signal on terminal 31*a* will be a "one" when the $\bar{a}$ pulse clocks the flip-flop

F34. Accordingly, the flip-flop F34 will be set by the clock pulse to output a "one" on its Q terminal, thus enabling a gate G64 to invert and pass the line feed pulse to a gate G63.

The gate G63 will not properly respond to the signal being received from the gate G64 unless it has been properly conditioned by gate G62. One input to the gate G62 is the previously mentioned recognition signal received from the decode gate 225. The other input to the gate G62 is the previously mentioned pulse appearing at the terminal 60 in FIG. 11. The NAND gate G62 says, in effect, that the line feed pulse should not be passed by the gate G63 unless it coincides with a signal causing the line feed character to be introduced into the memory buffer. Thus, the memory is a continuously cycling memory and the aforementioned decode gate mechanism will repeatedly recognize line feed characters, but an output from gate G63 is desired only when a line feed character is being entered into the memory.

To allow the flip-flop F34 to be reset for proper handling of the next line feed character required in the memory, the A5* state of the A clock counter, each time it occurs, is permitted to apply a "one" to terminal 280 in FIG. 7 which is inverted by gate G66 to reset the F34 flip-flop. This keeps the flip-flop F34 always in condition to recognize new $\bar{a}$ pulses from the Tx complementary counter.

At those times when a line feed pulse passes the gate G63, it is applied to terminal 62 in FIG. 7 which also appears in FIG. 12.

FIG. 12 is a gate mechanism for presetting the Tx counter, the gates being steered so as to operate under domination of the E counter. As previously mentioned, the E counter comprises four flip-flops of which three are connected together as a divide-by-six shift register. This divide-by-six shift register is used to clock the fourth flip-flop each time the shift register reaches its sixth state. The fourth flip-flop is thus "zero" for six shift register states and "one" for six shift register states. The E counter shift register states are designated EO* E1* E2* E3* E4* E5*.

By conventional gating, not shown, a signal (Boolean) EO* + E2* + E4* is applied to terminal 64 in FIG. 12. A further signal comprising E1* + E2* + E5* is applied to terminal 65. The still further signal E3* + E4* + E5* is applied to terminal 66.

For reasons more fully described in a later portion of this description, the composition of messages from the keyboard is permitted only during the six states of the E counter which occur when the fourth flip-flop of the E counter is in its "zero" state. Accordingly, all line feed signals reaching the terminal 62 in FIG. 12 are NANDed in gate G67 with a positive signal $\overline{E4}$ available in the fourth flip-flop of the E counter only when that flip-flop is in its "zero" state. Gate G67 thus permits the line feed pulse to enter the Tx counter preset gates only when the circuitry is conditioned for composition of messages.

Assuming such condition exists, the line feed pulse is passed to NOR gates G68, G77 and G80. The complement of the line feed pulse derived from gate G84 is applied to NAND gates G70, G79 and G82. A "clear" signal which is normally a "-zero" is brought from the terminal 67 to NOR gates G69, G78, G81 and G83. The various NAND and NOR gates above mentioned are interconnected as shown in FIG. 12.

FIG. 12 has seven output terminals having reference numbers 68, 69, 70, 71, 72, 73 and 74. These terminals are connected to correspondingly numbered input terminals of the Tx counter shown in FIG. 6.

As will be more fully explained later, the various states of the E counter have the ability to divide the memory into six message lines, each message line comprising 32 characters. Due to operation of the line feed mechanism presently being discussed, each line of 32 characters will be followed by a line advance character. In preceding paragraphs, it was described how the line advance character was automatically introduced to the memory buffer when a 32 keyboard character had been depressed. This character was introduced to the buffer while the Tx counter remained at a count of 32 and it is now important to advance the Tx counter to a count of 33 so as to account for the presence of a 33 character in the memory.

The line feed pulse which reached terminal 62 in FIG. 12 in consequence of a 32 character having been received from the keyboard reaches terminal 62 at a time when the E counter is in its EO* state. The line feed pulse is accordingly NORed with a "one" at gate G68 and a "zero" at gate G69 to produce a "one" at terminal 68. The line feed pulse is also inverted in gate G84 and NANDed a "one" in gate G70 to produce a "-zero" at terminal 69. By reason of these voltages on terminals 68 and 69, the Tx counter flip-flops H1 and H6 (FIG. 6) are preset to a "one" state. The remaining Tx counter flip-flops are preset to a "zero" by the gate circuitry of FIG. 12 with the result that the Tx counter is preset to a count of 33 so as to exactly match the number of characters in the memory.

This presetting of the Tx counter occurs in a very short time interval after the 32 character is depressed and before an operator would have time to depress still another character. When the operator does depress another character, it will be recognized by the circuitry as a 34 character and dropped into the memory through the memory buffer in the 34th slot of the memory.

By the procedures above described, gate G71 in FIG. 6 will recognize the 65 character depressed on the keyboard and insert a line advance character in the 66th slot of the memory while the gate circuitry of FIG. 12 presets the Tx counter to a count of 66. Gate G72 in FIG. 6 will thereafter recognize the 98 character from the keyboard and insert a line advance character on the 99 slot. Next, gate G73 will recognize the 131 character from the keyboard and insert a line advance character in the 132 memory slot; gate G74 will recognize the 164 character from the keyboard and insert a line advance character in the 165 slot of the memory, gate G75 will recognize the 197 character from the keyboard and insert a line advance character in the 198 slot of the memory.

In each case, for purposes of inserting a line advance character each of the gates G71, G72, G73, G74 and G75 has its output connected to the NAND gate G53 appearing in FIG. 11.

198 memory slots comprise the entire capacity of the memory devoted to composition of messages. When 198 characters are in the memory, as evidenced by a count of 198 on the Tx counter, this count is recognized in gate G76 which then outputs a "zero" to its terminal 76. Terminal 76 re-appears in FIG. 5 and the "zero" on this terminal is applied to gate G4 in FIG. 5 so as to disable gate G4. When disabled, gate G4 blocks all $\overline{A}$ strobes from the keyboard and by reason of this blockage no further character information can be received from the keyboard. Until the memory is cleared, as will be later described, no further information can be received from the keyboard.

It was previously mentioned that there are two ways to place a line advance character into the memory, one way being the automatic insertion of a line advance character which has been described in the foregoing paragraphs. The other way is by depressing the line advance key on the keyboard. This key can be used to introduce to the memory the six bit line advance character, 0, 1, 1, 1, 0, 0.

Assume, for example, that after 15 characters have been placed into the memory by operation of the keyboard, the keyboard key for line advance is depressed. The line advance code will then be introduced into the 16th slot of the memory, read by the decode gate mechanism 225, and by operation of the circuitry already described a line feed pulse gated to terminal 62 in FIG. 12. When the line feed pulse is received at terminal 62, the Tx counter is immediately advanced to a count of 33, effectively filling null characters in all memory slots between slots 17 and 32. The line advance character on the keyboard can thus be used to complete any line being composed in the memory with null characters, as the operator may desire.

To this point in the description there has been described a means for composing messages into the memory of the present

invention by means of a keyboard, the messages being effectively divided into six lines each comprising 32 possible characters and always a 33 line advance character. It has been assumed throughout that the operator's composition of the message has been flawless and that there is no need to correct the message. In the following paragraphs, a backspace mechanism which enables corrections of messages will be described.

The backspace or correction process is initiated by depressing a backspace key provided on the keyboard. The backspace key places a "one" on terminal **77** in FIG. **5**. The presence of a "one" on this terminal acts through gates **G12**, **G6**, **G7**, **G8** and **G9** and the clock input to flip-flop **F2** to reverse the output of the flip-flop **F2** to terminals **31***a* and **31***b*. The signal level on terminal **31***a* thus drops to a "zero" and the level on terminal **31***b* rises to a "one." This reverses the operation of the gates **G14**, **G15**, **G16**, **G17**, **G18**, **G19** and **G20** in FIG. **6** with the result that the T*x* counter is conditioned to count down rather than to count up. When the voltages of terminals **31***a* and **31***b* of FIG. **5** are reversed, a number of events follow.

The shift in voltage from a "one" to a "zero" at terminal **31***a* in FIG. **5** appears at terminal **31***a* in FIG. **7**. The presence of a "zero" at this terminal fires a one-shot **78** shown in FIG. **7** which delivers a timed strobe to a NAND gate **G85** also shown in FIG. **7**. This strobe is inverted by gate **G85**, re-inverted by gate **G86**, and applied to terminal **79** appearing in FIG. **7**.

Terminal **79** also appears in FIG. **6** and the strobe pulse received from the one-shot **78** at this terminal is applied to the "J" input of the flip-flop **H1**. The function of the strobe pulse at this flip-flop at this time is to inhibit any change in the T*x* counter as the terminals **31***a* and **31***b* reverse polarity. More particularly, the strobe from the one-shot **78** in FIG. **7** is timed to meet the $\bar{A}$ strobe also being generated by the one-shot **30** in FIG. **7** and which reaches terminal **29** in FIG. **6**. At this time gate **G100** also inhibits any change in the flip-flops **H2** – **H8**. In practical effect, the backspace key has been struck so as to initiate an $\bar{A}$ strobe which would normally signal receipt of a new character to the T*x* counter, but this strobe is being blocked from only the T*x* counter the first time the backspace key is depressed.

The backspace key nevertheless enters a null character (bits 0, 0, 0, 0, 0, 0) in the keyboard buffer and, by the T*x* and T*x* complementary counter circuitry previously described, this six bit character is transferred to the memory buffer and into the memory. Since the $\bar{A}$ strobe was blocked from the T*x* counter, however, the T*x* counter did not count up to account for the backspace character and, accordingly, the immediately previous character which had been entered into the memory is superseded or replaced by the null character from the backspace key. Thus, if the immediately previous character received from the keyboard had been entered into slot 15 of the memory, depression of the backspace key will have the effect of changing the fifteenth character in the memory to a null character, thus erasing the fifteenth character from the memory.

Since the polarity to the terminals **31***a* and **31***b* in FIG. **6** has been reversed, the gates **G14** through **G20** have been conditioned to cause the T*x* counter to count down instead of up. The T*x* counter did not count down when the backspace key was first depressed due to the blocking effect of the strobe received from the one-shot **78**. However, each succeeding time the backspace key is depressed (without depressing a different character key), the T*x* counter counts down and a null character is entered into each memory slot to which the T*x* counter counts down. Thus, previous characters entered into the memory can be erased one by one by successive depressions of the backspace key and the T*x* counter will always count downwardly for one less than the number of characters erased.

A special circumstance arises whenever, by means of backspace, an automatically inserted line feed character is erased from the memory. If this should happen, the keyboard operator must either replace the line advance character by a manual depression of the line advance key on the keyboard or the operator must also erase the next earlier letter so that when the erased portion of the message is recomposed, an automatic line feed character will enter the memory in proper sequence by processes previously described.

To further illustrate this circumstance, an operator may commence an erasure by use of the backspace key when the T*x* counter is at count 34 and accordingly a 34th character has been inserted into the memory. The first time the backspace key is depressed, the 34th character is erased from the memory. When the backspace key is next depressed, a line advance character is erased from the 33 slot of the memory. This line advance character must be replaced by the operator by depressing the line advance key on the keyboard. If, however, the operator wishes to also erase the 32 character stored in the memory, the operator is not required to replace the line advance character erased from the 33 slot of the memory. Instead, the operator continues the erasure to erase the 32 character.

Here, however, a special problem arises because the decode gate **G52** will immediately recognize the return to count 32 in the T*x* counter and seek to automatically introduce a line feed character in the 33 slot of the memory. To block this automatic insertion until after the operator has had an opportunity to replace the 32 character in the memory, the voltage at terminal **31***a* in FIG. **5** is always referred to terminal **31***a* in FIG. **7**. Since the voltage at terminal **31***a* in FIG. **7** will have dropped from a "one" to a "zero" due to operation of the backspace key, the flip-flop **F34** disables the gate **G64** so that, should a line feed advance character be read from some other part of the memory as the memory continuously cycles, this line feed advance character cannot be recognized so as to activate the preset circuitry for the T*x* counter.

After completing a backspace erasure, whether the erasure comprises only one character in the memory, or many characters in the memory, the circuitry is taken out of the erase condition as soon as the operator depresses any character key on the keyboard. Thus, as soon as a character key is depressed, the flip-flop **F2** in FIG. **5** is reset to output a "one" to terminal **31***a* and a "zero" to terminal **31***b*. As soon as this reset occurs, the voltage shift from "one" to "zero" on terminal **31***b* in FIG. **7** triggers a one-shot **80** shown in FIG. **7** which fires a strobe pulse to terminal **79** in FIG. **7**. As before, this strobe pulse inhibits the T*x* counter from recognizing the $\bar{A}$ strobe reaching terminal **29** in FIG. **6**. The character code from the key first depressed after a backspace erasure is thus entered directly into the memory in the memory slot at which the last erasure had occurred. The T*x* counter is also conditioned to count up in normal fashion with depression of further character keys as if the erasure had never occurred.

In the preceding portions of this description, it has been explained how a message can be composed in the memory of the present invention, how characters are entered into proper slots of the memory despite the fact that the memory is being continuously cycled as the message is being composed and how, when desired, the message can be edited to make corrections therein. In the following paragraphs, the cathode ray tube (CRT) display mechanism will be described, this being a mechanism which permits the operator to visually examine the message as it is being composed and to visually review the message after it has been fully composed. To simplify the description of the CRT mechanism, a fully composed message will be assumed.

The operating concept of the CRT display mechanism is as follows. By means of the D counter, a cathode ray beam is caused to progress in coarse increments through 32 horizontally spaced character positions on a cathode ray screen. The beam is then dropped downwardly on the screen a distance corresponding to the desired spacing between lines of the display, advanced horizontally through 32 more character positions, and this display process repeated to cause the cathode ray beam to coarsely trace out twelve horizontal lines each

having 32 character positions therein. Six of these horizontal lines are reserved for a display of composed messages, and the other six are reserved for display of messages that will be received in a manner yet to be described.

As the cathode ray beam is coarsely moved to each of its 384 character positions (12 lines each having 32 characters), clock signals received from the A and B counters are employed to advance the beam at each character position through a six-line by 10-line rectangular matrix. By means of blanking signals applied to the cathode ray tube cathode, luminous dots are permitted to form only at discrete points in a five by seven portion of the matrix traced out at each character position. A legible luminous character is thus traced out at each of the 384 character positions reached by the cathode ray beam.

For convenience, the coarse movement of the cathode ray beam through 384 character positions is hereinafter referred to as a major raster. The fine or vernier movement of the cathode ray beam through a six by 10 rectangular matrix at each coarse position established by the major raster is referred to as a minor raster.

While the minor raster provides a five by seven matrix of dots representing any given character, this matrix will be generated within an essentially six by 10 matrix area. The remaining portions of the six by 10 matrix area are used to provide spaces between the characters and spaces between the lines. The five by seven dot matrix which is reserved for a display of characters at each character position is controlled by a 35 bit character code supplied serially to an amplifier which blanks the filament. It is therefore necessary to convert the six bit character codes stored in the memory to 35 bit character codes which can be applied serially to the blanking amplifier. In ensuing paragraphs, the six bit to 35 bit character code conversion will be described.

It is helpful to recall at this point that all characters being stored in the memory are being clocked through the memory buffer one after the other on C5 clock time. For convenience, the Q and $\overline{Q}$ outputs of the memory buffer flip-flops F17 through F22 have been marked in relation to the bit information they convey. Thus, the flip-flops F17 through F22 represent the bits B1 through B6 of the bit code depicted in FIG. 1. As each character present in the memory is lodged in the memory buffer, the Q output of flip-flop F17 represents the value of bit B1 and the $\overline{Q}$ output of flip-flop F17 represents the value of bit $\overline{B1}$. All bit values and their complements are accordingly made available at the memory buffer and as each character from the memory is clocked into the memory buffer, the Q and $\overline{Q}$ outputs of the flip-flops of the memory buffer report the character that is being presently lodged in the memory buffer.

The circuitry includes 64 recognition gates each capable of recognizing one of the 64 possible characters that can reside in the memory. Three such gates are illustrated in FIG. 13 and are identified by the reference characters G87, G88 and G89.

The gate G87 is a NAND gate connected to recognize only the six bit code for the letter "Q." It will recognize no other code. Thus, the bits for the letter "Q" are 1, 0, 0, 0, 1, 0. For the purpose of recognizing the letter "Q," the NAND gate G87 inputs are respectively, B1, $\overline{B2}$, $\overline{B3}$, $\overline{B4}$, B5 and $\overline{B6}$, as received from the memory buffer. Whenever the character "Q" is in the memory buffer, all inputs to the gate G87 will be "one" and accordingly, the gate G86 will be forced to output a "zero." This "zero" is inverted through a conventional inverter so that an output of "one" appears on the line marked "Q" in FIG. 13. This "Q" line will be a "one" only when the six bit code for the character "Q" resides in the memory.

FIG. 14 tabulates the Q and $\overline{Q}$ values that will be received from the memory buffer when any one of the "Q," "R" and "S" characters is lodged in the memory buffer. By comparison of the inputs to the gate G88 with the Q and $\overline{Q}$ values from the memory buffer tabulated in FIG. 14, it can be seen that the gate G88 is conditioned to recognize only the character "R." Likewise, the gate G89 is conditioned to recognize only the character "S."

It will be readily understood that FIGS. 13 and 14 are merely illustrative of the technique employed to develop character recognition gates. In fact, only 63 recognition gates are required. Thus, the previously discussed null character is an essentially inoperative character and there is no need to recognize this character.

It is frequently convenient to refer to each of the output lines of the character recognition gates as bit lines. Each of the bit lines from the character recognition gates is connected to a network of diode boards which re-express the character being recognized in a 35 bit code. FIG. 15 illustrates seven diode boards labeled X1, X2, X3, X4, X5, X6 and X7 assembled to produce the 35 bit code for the characters "O," "P," "Q," "R," "S" and "T."

These diode boards are of a commercially available type in which an array of diodes is connected by fusible links between horizontal conductors insulated from vertical conductors. To conform the diode boards to the desired code, the fusible links are ruptured, or blown out, as desired. FIG. 15 illustrates only those diodes which remain in the circuitry after the fusible links have been ruptured. It will be noted that initially all horizontal conductors were brought out to terminals on the left sides of the diode boards. To simplify the drawing, those horizontal lines that have been removed from the circuitry by rupture of the fusible links have been omitted but, for convenience in description, the output terminals for such lines remain in the drawing.

Assuming the character "R" has been recognized in the memory buffer, a voltage level of "one" will appear at the terminal "R" illustrated in FIG. 15. By reason of the diode connections illustrated, horizontal conductors 7–1 and 7–5 will all rise to the "one" level when the character "R" is recognized. The horizontal conductor 7–5 on the board X7 will remain at the "zero" level.

On diode board X6 the output terminals 6–1 and 6–4 will go to a "one" level and all other output terminals from the diode board X6 will remain at "zero."

It can be noted that the seven diode boards X1 through X7 collectively provide 35 outlet terminals, each capable of having a voltage level of "one" or "zero." When the character "R" is recognized, a unique portion of the 35 outlet terminals will have a level of "one" and the remainder a level of "zero," thus providing a unique 35 bit code for the character "R."

FIG. 15 indicates the unique codes for the characters "O," "P," "Q," "R," "S" and "T." Other networks of diode boards, each comprising seven boards, are used to develop unique 35 bit codes for each character available to the memory.

FIG. 16 illustrates the manner in which the diode boards have been organized. Thus, FIG. 16 shows a matrix comprising five vertical lines and seven horizontal lines. Each of the diode boards X1 through X7 represents a horizontal display line. The five outputs from each diode board in FIG. 15 provide column information for the matrix of FIG. 16. This enables the outputs from the diode boards to be numbered in reference to the matrix position illustrated in FIG. 16. Thus, outlet 7–1 of diode board X1 can be considered as representing row 1, column 5 of the matrix illustrated in FIG. 16. The terminal designations in FIG. 15 thus depict the rows and columns in which information should be displayed as in FIG. 16. If a dot is placed in FIG. 16 at each point in the matrix where a "one" is output from the diode boards X1 through X7 when the character "R" is recognized, as has been done in FIG. 16, the character "R" appears in the matrix. Each of the 63 character codes available to the memory is thus converted to a 35 bit code in the fashion described to provide a visually recognizable character.

For purposes of the CRT display, it is required to convert the 35 bit codes, one for each character, to a 35 bit serialized stream of binary data. This is accomplished with the aid of the A and B clock counters (FIG. 4) and the circuit illustrated in FIG. 17.

The A counter is assembled as a divide-by-ten shift counter. For convenience, the ten states to which the A counter shifts are designated A0* A1* A2* A3* A4* A5* A6* A7* A8*

and A9*. The B counter is a divide-by-six shift counter and the six states of the B counter are designated B0* B1* B2* B3* B4* and B5*.

By means of conventional gating, not shown, the A3* through A9* A counter states are applied to the terminals 81 through 87, respectively, in FIG. 17. The B1* through B5* states of the B counter are applied to the terminals 88 through 92, respectively, in FIG. 17. It will be recognized by those skilled in the art that when the B counter is in its B1* state, the A counter will shift through all ten of its states and when the B counter is in its B2* state, the a counter will again shift through all ten of its states, and so on for each state of the B counter.

Assume for example that the character "R" has been detected in the memory buffer by its recognition gate G88 and, per force, the appropriate outputs of the diode boards illustrated in FIG. 15 output "ones" and "zeros" in accordance with their design, to the 35 output terminals shown in FIG. 15. The same 35 output terminals appear in FIG. 17 and, while the character "R" is being recognized in the memory buffer, the appropriate terminals in FIG. 17 will carry "ones" or "zeros" as determined by the diode boards in FIG. 15.

During the time the character "R" remains in the memory buffer, the B clock will progress through all six of its states one time, and the A clock will progress through all 10 of its states six times, this being a necessary result of the fact that the characters are clocked through the memory buffer by the C5 clock.

It can be seen that the circuitry of FIG. 17 has a single outlet at terminal 93. It also has a clock input to be described later at terminal 94.

Assuming that the character "R" has just been recognized and the B counter is in its B1* state, the A counter will shift progressively through its ten states, AO* – A9*. For the first three states of the A counter, A0* – A2*, both inputs to a NAND gate G92 will be "zeros" and this NAND gate will output a steady "one." When the A counter reaches its A3* state, terminal 81 will go to a "one" voltage. Reference to FIG. 15 shows that output 7–1 from the diode boards is also at a "one" voltage. These "one" voltages will be ANDed during the time of the A3* state through gate G90 to place a "one" on one of the five inputs to NOR gate G91. All other inputs to the gate G91 are "zeros" since the A counter is in the A3* state. NOR gate G91 accordingly outputs a "zero" to NAND gate G92 which, being disabled, outputs a "one" to NAND gate G94. This "one" is inverted by gate G94 so as to disable gate G95, causing this gate to output a "one."

From the foregoing description respecting FIG. 17, it can be recognized that the A counter will progress from its state A3* up to its state A9*, sampling the diode board outputs for the seven rows of column one in the matrix of FIG. 16. It will be noted that the sampling proceeds upwardly from row seven to row one during B1* time. The coincidence gating illustrated in FIG. 17 will cause gate G95 to output a "one" at each row where the diode boards output a "one" and to output a "zero" at each row where the diode boards output a "zero." With reference to the letter "R," for example, the diode boards output a "one" for each row in column one of the display (FIG. 16) and accordingly the NAND gate G95 will output seven regularly spaced "ones" to its terminal 93.

During B2* time, the circuitry of FIG. 17 will repeat the sampling process but this time the sampling will proceed upwardly along column two of the display matrix (FIG. 16). Accordingly, the NAND gate G95 will output 0, 0, 0, 1, 0, 0, 1.

From the foregoing description, it is evident that during B3* time the third column of the display matrix will be sampled, during B4* time the fourth column sampled and during B5* time the fifth column sampled. Since any given character remains in the memory buffer for a time equal substantially to the time separation between two successive C5 clock pulses, there is intrinsically ample time for completion of the foregoing sampling process. It will be noted that the sampling process carries the A counter six times through its ten states. During B0* time the NAND gate G95 has all inputs "one" and thus outputs a steady "zero." As will appear more fully when the CRT raster circuitry is discussed, the resulting empty column immediately to the left of each character display is used to assure adequate character spacing.

By the same reasoning, the gate G95 outputs a "zero" at A0* time, A1* time and A2* time, and this circuit characteristic is used to assure adequate spacing between lines of the display.

It is believed evident from the foregoing description that the result of the sampling process is a serialized bit stream at terminal 93 in FIG. 17 which comprises 60 bits spaced by the time interval between A counter states. Many of the bits in this stream will always be a "zero" for the reasons described. "Ones" will appear in this 60 bit stream only those sites where illumination will be desired on the CRT screen and, basically, the places where a "one" can appear in the 60 bit stream of data resulting from each sampling sequence are confined to the seven row and five column matrix used for character representation.

It was noted at the beginning of this specification that the keyboard includes a space key (bits 0, 0, 0, 0, 0, 1) which is actually placed in the memory and thus it is not a null character. It will be understood, however, that the diode boards responsive to this space character are designed to provide no illumination in the space area. It is also possible for the memory to contain null characters resulting from a line advance character having been entered into the memory from the keyboard. Such null characters also will give rise to no CRT image.

Since it is possible for relatively large areas of the CRT display to contain no image, it is found desirable to nevertheless image each character position in the array so that the keyboard operator will not be confused as to the formatting of the CRT display. This is accomplished in the present invention by gating the A2* B3* clock counter state to terminal 94 in FIG. 17. This signal is passed by an AND gate G96 in FIG. 17 and as a result each 60 bit serialized stream resulting from the sampling by the A and B counters in the manner previously described will contain a "one" in the third column of the display area (FIG. 16) and immediately below the first row of the display area. This "one" is used to always generate a luminous dot in the third column and below each character display area of the CRT, thus advising the keyboard operator of the available display area and the available character sites.

In the following paragraphs it will be described how this 60 bit serialized stream derived from the sampling operation provided by the circuitry of FIG. 17 is used to produce character displays on the screen of the cathode ray tube.

The CRT display circuitry is outlined in block diagram form in FIG. 21. As conventional, the cathode ray tube is energized through a high voltage delay circuit, auto transformer and a high voltage power supply. Energized by the high voltage input is a DC supply which supplies energy to a focus control through a focus supply circuit. Filament current for the cathode ray tube is supplied through a filament transformer. The foregoing elements are conventional to any cathode ray tube apparatus and require no further explanation, although it may be noted that the high voltage delay circuit is employed in the present cathode ray tube apparatus to delay energization of the cathode ray tube until the various display controls to be described have become operative.

As frequently conventional, the cathode ray tube includes a main yoke and a minor yoke which are used to direct the cathode ray beam to selected areas of a cathode ray screen. The beam is caused to progress horizontally across the screen in synchronized relationship to the D counter (FIG. 4) by converting selected digital clock signals from the D counter to analog voltage signals in a main horizontal digital to analog converter. The output of this converter is amplified in a main horizontal deflection amplifier which, by controlling the current in the main yoke, causes the cathode ray beam to advance from left to right on the screen, as observed by one viewing the screen.

Selected clock signals derived from the D and E counters are converted to analog voltages in a main vertical digital to analog converter, amplified in a main vertical deflection amplifier and applied to the main yoke to control the vertical elevation at which the beam progresses horizontally across the screen. The clock signals are so utilized that the cathode ray beam will progress from left to right across the screen twelve times at twelve different vertical levels as if to write 12 lines of information on the screen.

Each horizontal sweep of the cathode ray beam across the screen proceeds in a stepwise fashion so that the beam stops momentarily at 32 equally spaced positions across the screen. Each of these 32 positions represents a position at which a character can be displayed. The character display proceeds under control of the A and B counters. Selected signals derived from the B counter are applied to a minor horizontal digital to analog converter which outputs to a minor horizontal deflection amplifier driving the minor yoke to cause the cathode ray beam to shift horizontally in vernier increments to five horizontally spaced positions. As these horizontal shifts occur, a selected signal from the A counter controls the operation of a minor vertical deflection amplifier which drives the minor yoke to cause the cathode ray beam to sweep upwardly and return at each horizontally spaced position established by the minor horizontal deflection system.

It will be understood that the minor horizontal and vertical deflections occur very quickly at each of the 32 character positions reached by the cathode ray beam in each of its horizontal sweeps across the cathode ray screen. As will be more fully explained at a later point in this description, the vertical sweep of the cathode ray beam produced by the minor vertical deflection amplifier can be considered as a sweep through seven vertically spaced positions. Thus, at each of the 32 character positions reached by the cathode ray beam in each of its horizontal sweeps across the screen, a five by seven character matrix is traced.

Associated with the cathode ray tube are a blanking amplifier and a power supply therefor. The blanking amplifier normally biases the grid of the cathode ray tube so as to cut off the cathode ray beam. During each time the minor yoke is modulated so as to trace out the aforementioned five by seven matrix, the serialized sixty bit stream produced by the serializer circuitry of FIG. **17** is applied to the blanking amplifier. At each position along the stream where a "one" appears, the blanking amplifier is disabled so as to enable the cathode ray beam to strike the cathode ray screen. The serialized bit stream is thus a stream of blanking control bits.

As previously noted, a "one" will always appear at the base of the third column in each five by seven character matrix. Thus, the cathode ray beam will be unblanked at least once for each character position. Additional unblanking can occur only in a five by seven display area.

It will be recalled that the memory includes 396 memory cells. As previously discussed, these 396 cells are divided, in effect, into 12 lines each comprising 33 characters, the 33 character in each line being a line advance character which is not displayed on the cathode ray tube. The cathode ray tube display system is thus designed to display twelve lines, each comprising 32 characters. As will be subsequently explained in greater detail, each line of the display area is adapted to display 32 characters derived from the memory and as the cathode ray beam is directed through its 12 horizontal lines of display, all characters with the exception of line advance characters residing in the memory will be displayed. Thus, the display circuitry of the present invention is intended to display the entire memory at one time. Recalling also that the memory is continuously cycled through the memory buffer, it will be understood that this continuous cycling of the memory is used to continuously refresh the cathode ray tube display so that all characters present in the memory with the exception of line advance characters are continuously visible on the cathode ray beam screen.

It is convenient to consider the cathode ray tube as executing two relatively independent rasters. The first raster, herein called a major raster, comprises the left to right horizontal movements of the cathode ray tube through twelve vertically spaced horizontal lines. The second raster, herein called the minor raster, comprises the six by 10 character matrix which traces out a character at each of the 32 positions established by the major raster in each of the 12 lines of the display.

The beam control means for producing the left to right horizontal movements of the major raster is displayed primarily in FIG. **18**. The clocks for the circuit are developed as follows.

The output of the D1 flip-flop in the D clock counter is applied to terminal **124** in FIG. **20**. The output of the D6 flip-flop in the D clock counter is applied to terminal **126** in FIG. **20**. The D6 flip-flop output is inverted to $\overline{D6}$ by gate G112 and NANDed with D1 in gate G113 and the result inverted in gate G114 to produce an output $\overline{D6}$ D1 at terminal **127** in FIG. **20**. This signal appears at terminal **127** in FIG. **18** and serves as one of the clocks for the major horizontal raster.

In like fashion, $\overline{D6}$ from gate G112 is NANDed with D2 in gate G115 of FIG. **20** and the result inverted through gate G116 to produce the clock signal $\overline{D6}$ D2 at terminal **128** in FIG. **20**. Terminal **128** re-appears in FIG. **18** to supply the clock signal $\overline{D6}$ D2 to the major horizontal raster circuitry.

Clock signals D3, D4 and D5 are applied directly from the D counter to terminals **129**, **130** and **131** of FIG. **18**. A sixth clock signal for controlling the major horizontal raster is derived from the circuitry of FIGS. **19** and **20**. Referring to FIG. **20**, the output of the flip-flop D1 in the D counter brought to terminal **124** is inverted in gate G127 to bring $\overline{D1}$ to terminal **120**. This terminal re-appears in FIG. **19** where $\overline{D1}$ is used as one input to a NAND gate G110. In like fashion, the output of the flip-flop D2 in the D counter brought to terminal **125** of FIG. **20** is inverted in gate G128 so as to apply $\overline{D2}$ to terminal **121** in FIG. **20**. This terminal re-appears in FIG. **19** where it serves as the second input to the gate G110. A third input to the gate G110 in FIG. **19** is the output of the flip-flop D6 in the D clock counter which is brought to terminal **122** in FIG. **19**. The resulting output of the NAND gate G110 is inverted in gate G111 where the signal $\overline{D1}$ $\overline{D2}$ D6 is applied to terminal **123**. Terminal **123** re-appears in FIG. **18** as the sixth clock signal for the major horizontal raster circuitry.

The foregoing six clock inputs to FIG. **18** are separately applied to transistor triplets designated **135**, **136**, **137**, **138**, **139** and **140**. The triplet **135**, for example, comprises transistors Q1, Q2 and Q3. The triplets are all supplied with a positive reference voltage at terminal **132** and a ground at terminal **133**. With reference to the triplet **135**, those skilled in the art will recognize that the transistors Q1 and Q3 are normally nonconductive and the transistor Q2 conductive until a "one" voltage reaches terminal **127** whereupon the transistors Q1 and Q3 become conductive while Q2 goes off. When Q2 is conductive, the voltage on a conductor **135***a* is essentially ground. When Q2 goes off, the voltage on the conductor **135***a* rises to the positive reference voltage. The transistor triplet **135** thus behaves as a switch, switching the conductor **135**a to the reference voltage when a clock pulse arrives at terminal **127** and to ground when a clock pulse is not present on terminal **127**. The transistor triplets **136**, **137**, **138**, **139** and **140** act in the identical fashion, each being controlled by the particular clock input thereto.

The foregoing transistor triplets control the voltage inputs to an R–2R binary weighted resistance ladder grounded at terminal **134** and including the resistances **141**, **142**, **143**, **144**, **145** and **146**.

Assuming the D counter is initially in a "zero" state wherein all of its flip-flops are outputting "zeros," the operation proceeds as follows. Each of the resistances **141** through **146** in the resistance ladder is grounded at one end. When a first clock signal $\overline{D6}$ D1 is received at terminal **127**, Q2 goes off and Q1 goes on so that a small portion of the positive reference voltage appears on a conductor **147**. This condition occurs when the flip-flop D1 in the D counter first reaches its "one" state.

The flip-flop D1 then shifts to "zero" as D2 shifts to its "one" state, thus switching the positive reference voltage from the resistance 141 to the resistance 142. The conductor 147 now receives a higher voltage through the resistance 142. The circuit is so balanced that the voltage on the conductor 147 is now just twice the voltage that appeared when only the transistor triplet 135 was conducting.

In the next stage of the D counter, both the flip-flops D1 and D2 are in their "one" state and accordingly both the triplets 135 and 136 are conducting. The voltage on the conductor 147 is then three times the voltage that appeared when only the flip-flop D1 was in its "one" state. A pattern can now be recognized in which, as the D counter counts upwardly from a first count ($\overline{D6}$ D1), the voltage on the conductor 147 increases by equal increments, the voltage always being a multiple of the voltage which appeared on the conductor 147 at the first count level. It will be recognized, of course, that $\overline{D1}$ $\overline{D2}$ D6 represents a count up to 32 in the D counter and represents the highest count recognized by the circuitry of FIG. 18. Thus, the D counter count levels 33, 34, 35 and 36 do not influence the circuitry of FIG. 18 which only reacts to the first 32 count levels of the D counter. As the D counter progresses through the first 32 counts thereof, the voltage on the conductor 147 progresses upwardly in 32 equal increments. Thus, the circuitry of FIG. 18 has succeeded in converting the first 32 digital count signals from the D counter to voltage analogs.

As appears in FIG. 18, the voltage from the conductor 147 is applied to an amplifier 148, and the output of the amplifier 148 to a second amplifier 149. The second amplifier acts as a voltage to current converter. The biasing circuitry for these amplifiers is conventional and therefore not described in detail, it being sufficient to note that positive voltage is supplied on conductor 151 from terminal 132 and a ground supplied on conductor 152 from terminal 133. A separate positive voltage supply is brought in at terminal 153 and a separate negative voltage supply brought in at terminal 154. The output of the amplifier 149 to terminal 150 serves as a pre-amplifier to drive a deflection power amplifier, not shown, which is connected through a current sampling resistor, not shown, to the main horizontal yoke winding. Feedback from the sampling resistor to terminal 155 is employed to stabilize the amplifier output.

From the foregoing description, it can be recognized that as the D counter progresses from its basic one count to a count of 32, the cathode ray beam is stepped incrementally across the cathode ray screen in 32 essentially equal steps. The D counter will count on out to 36 and the last four counts of the D counter afford time for the deflection system to recover and return the cathode ray beam from its extreme right deflection to its extreme left deflection.

It was previously described that the major raster travels horizontally through twelve vertically spaced "lines" on the CRT screen. The vertical spacing is obtained by means of the beam control circuitry illustrated in FIG. 19. It will be recognized of source that a change in the vertical elevation at which the horizontal sweeps of the major raster occur is desired only after the D counter has completed its 32 count to as to complete a horizontal sweep of the major raster. The circuitry of FIG. 19 is thus clocked by the D counter flip-flop condition $\overline{D1}$ $\overline{D2}$ D6 applied to conductor 156. This clock identifies the end of each horizontal sweep from the circuitry of FIG. 18.

To cause a vertical sweep through twelve vertically spaced positions, the circuitry of FIG. 19 is equipped with a counter mechanism comprising flip-flops V1, V2, V3 and V4. The Q outputs of these four flip-flops are applied by means of conductors 172, 173, 174 and 175, respectively, to transistor triplets 164, 165, 166 and 167. As before, the triplets 164 through 167 are connected between a positive reference voltage at terminal 161 and ground at terminal 162. As before, the transistor triplets are used to switch resistances 168, 169, 170 and 171, respectively, between ground and the reference voltage. The resistances 168 through 171 are part of a resistance ladder grounded at 163. The output of the resistance ladder appears on conductor 176.

A reset circuit for the flip-flops V1 through V4 is operated by a four input NAND gate G117. The inputs to this NAND gate are $\overline{E2}$ (the zero state of the second flip-flop in the E counter) received at terminal 157, E3 received at terminal 158, E4 received at terminal 159, and a clock signal D6 (D1 + D2) E11* received at terminal 160 in FIG. 19. As those skilled in the art will recognize, the E11* state occurs at the time the E counter is outputting its 12 count. The $\overline{D1}$ $\overline{D2}$ D6 state of the D counter occurs when the major raster is completing a horizontal traverse across the screen. Accordingly, after twelve lines have been traced by the major raster across the screen, and when the 12 line across the major raster reaches its 32 (or far right) position, the flip-flops V1 through V4 are reset.

The flip-flops V1 through V4 are thus permitted to function as a counter counting $\overline{D1}$ $\overline{D2}$ D6 pulses from the D counter up to 12 counts, whereupon the counter is reset.

From the preceding description, it can be recognized that as the flip-flops V1 through V4 count through 12 stages, the output conductor 176 from the resistance ladder will pass through twelve equally spaced voltage levels, each voltage level being a multiple of the first voltage level reached when the V1 flip-flop commenced the count toward twelve by outputting a "one."

As was the case with the circuitry of FIG. 18, the circuit of FIG. 19 includes amplifiers 177 and 178 biased with the positive reference voltage on the conductor 180 and ground on the conductor 181. A separate positive voltage supply is brought in to terminal 182 and a separate negative voltage supply is brought in to terminal 183. The output of the amplifier 178, which is a voltage to current converter, is applied from terminal 179 to a main vertical deflection power amplifier, not shown, to drive the main vertical yoke through a current sampling resistor from which a stabilizing feedback is referred to terminal 184 in FIG. 19.

From the foregoing description it will be understood that the circuits of FIGS. 18 and 19 provide a major raster pattern for the cathode ray tube in which the cathode ray beam advances progressively through 32 discrete character positions on each of twelve horizontal lines of display. The circuitry for executing the minor raster at each character position reached by the major raster is shown in FIG. 20.

Horizontal deflection of the cathode ray beam through five vernier increments at each character position is accomplished with the control means illustrated in the top half of FIG. 20. The clock inputs for this circuitry are derived from the B counter which is to be recognized as progressing or counting through six states designated B0*, B1*, B2*, B3*, B4* and B5*. To implement the circuit of FIG. 20, the B2* state is applied to terminal 190, the B3* state is applied to terminal 191, the B4* state is applied to terminal 192, and the B5* state is applied to terminal 196. The B2* and B4* states are NORed in gate G118, inverted in gate G119 and applied to a first transistor triplet 193 operating in the same fashion as previously described. The B3* and B4* states are NORed through gate G120, inverted through gate G121 and applied to the transistor triplet 194. The B5* signal received at terminal 196 is applied to the transistor triplet 195.

Those skilled in the art will recognize that as the B counter progresses successively through its six states, the first state to effect a switching action in the transistor triplets 193, 194 and 195 will be the B2* state, which will switch the transistor triplet 193 so as to apply a positive reference voltage received at terminal 249 to a resistance 197 located in a resistance ladder comprising the resistances 197, 198, and 199. The B3* state will next switch the transistor triplet 194 to apply the reference voltage to the resistance 198. When the B counter proceeds next in its B4* state, both the transistor triplets 193 and 194 will apply the reference voltage to both the resistors 197 and 198. The B counter next reaches its B5* state when the reference voltage is applied only to the resistance 199.

By reason of the foregoing circuitry, the resistance ladder outputs five voltage levels to the amplifier **250**. The first voltage level occurs during the B1* state of the counter when the amplifier input is at a base level. During B2* time, the voltage increases a first increment. During B3* time, the voltage increases a second increment. During B4* time, it increases a third increment. During B5* time, it increases a fourth increment. During B0* time, the deflection system returns to the base level.

The output of the amplifier **250** is applied to the base of transistor Q7, an emitter-follower, the output of which to terminal **253** is applied to a deflection power amplifier, not shown, which drives the minor horizontal yoke windings through a current sampling resistor, not shown. Feedback from the sampling resistor is applied to terminal **254** in FIG. **20**. A negative voltage supply for the amplifier is applied to terminal **252** in FIG. **20**.

From the foregoing description it is apparent that the resistance ladder including the resistances **197**, **198** and **199** operating under control of B counter states causes the minor deflection yoke to deflect the cathode ray beam through five horizontally spaced positions. It will be understood of course that the spacing between these five horizontally spaced positions is small in relation to the horizontal spacing between the character positions established with the circuitry of FIG. **18**.

A vertical sweep of the cathode ray beam at each horizontal vernier position reached by the control means illustrated in the upper half of FIG. **20** is achieved with aid of the circuitry illustrated in the lower half of FIG. **20**. This vertical sweep circuitry is clocked by the A2* counter state. As will be described, the A2* pulse triggers a vertical sweep of the cathode ray beam during each state of the B counter and thus at each horizontal vernier position reached by the horizontal deflection circuitry of FIG. **20**.

Each A2* pulse acts as a clamping control on a boot strap circuit consisting of transistors Q11, Q112 and Q113. Operation of the circuit is as follows. Consider that the A2* input to terminal **255** is "zero." Current will be sinked through diodes **260** and **261**. This sinking of current turns off transistors Q11 and Q12, thus allowing capacitor **262** to charge through resistance **263** and diode **264**. Transistor Q13 will at first be turned off, but will come on as capacitor **262** reaches a voltage high enough to turn it on through resistor **265**.

As Q13 turns on, charging current is fed back through capacitors **266** and **267** and resistance **263** to capacitor **262** thus lifting the charging circuit "by its own boot straps" and accelerating the charging action. The charging of capacitor **262** could continue until it is fully charged. However, this is prevented from occurring because the A2* clock goes to its "one" level, causing a back bias to appear across diodes **260** and **261**. Reverse biasing of these diodes results in transistors Q11 and Q12 being turned on by the voltage applied to their bases through resistor **268** and diode **269** to the base of Q11 and through resistor **270** and diode **271** to the base of Q12. Turning on these two clamping transistors results in the rapid discharge of capacitor **262** and the rapid charging of capacitors **266** and **267** through diode **264**. Capacitor **272** acts as a small delay in the turn off of transistor Q12 which performs a "shaping" function. The outcome of this procedure is a sawtooth wave form with a nearly linear wave front and a rapid full time. This wave shape is coupled to a fast slewing operational amplifier **273** which has its pulse amplitude adjusted by a potentiometer **274**. Potentiometer **275** is an off-set adjustment and is used to center the linear portion of the ramp around the active blanking and unblanking portions of each vertical column.

The amplifier **273** has separate positive and negative voltage supplies **276** and **277**, respectively. This amplifier is coupled from output **278** to a voltage to current converter, not shown, and applied to a deflection amplifier, not shown, to drive the minor vertical yoke windings through a current sampling resistor, not shown. Feedback from the current sampling resistor is applied to terminal **279** in FIG. **20**.

It will be noted that the output of the amplifier **273** is not a sequence of carefully metered increments as was the case with the major raster deflection circuit (see FIGS. **18** and **19**), and the minor raster horizontal deflection circuitry shown in the upper half of FIG. **20**. Rather, the minor vertical deflection circuitry relies on a vertical sweep produced by the amplifier **273** which commences in A2* time and continues its rise up to A9* time, then returns to its base level as the A counter returns to A2* time.

It will be noted that the major and minor horizontal and vertical deflection systems described in the foregoing paragraphs operate at all times whether or not character information is present in the memory. Whenever a character appears in the memory, the character is traced out in its appropriate minor raster when the character reaches the memory buffer. The serial code being supplied to the blanking amplifier unblanks the amplifier at appropriate sites in the five by seven minor raster. Thus, for each horizontal beam position in the minor raster, the vertical deflection system will cause an upward sweep of the beam through at least seven vertically spaced positions to enable unblanking of the cathode ray beam at those positions required for presentation of an intelligible character image on the screen.

It will be helpful at this point to review the clock timing employed in the present invention. The memory is clocked by the C5 clock. With each successive C5 clock pulse the D counter is advanced so as to select a new character position in the CRT display. Before the next C5 pulse can occur, the minor raster will have been executed to display on the CRT whatever character then resides in the memory buffer. Since the D and E clock counters are driven, so to speak, by the C5 clock which in turn drives the memory, it is an inevitable consequence that the first character lodged in the memory will appear at the first character position in the first line of the CRT display. Succeeding characters in the memory will be displayed in an orderly fashion in the 12 lines of display available to the cathode ray tube.

It has been previously mentioned that messages composed with the circuitry of the present application are intended to be transmitted to remote stations and that, correspondingly, messages composed at remote stations may be received by the circuitry of the present invention. It is further intended that messages composed by or received into the circuitry of the present invention be permanently recorded in an off-line printer not specifically disclosed herein. Conveniently, the sixty bit serialized data produced with the circuitry of FIG. **17** may be supplied directly to a matrix type printer adapted to print character codes in a five by seven matrix. A number of matrix printers are commercially available at the present time.

The send and receive functions of the present equipment are controlled by a separate clock externally supplied in the present equipment. This external clock, designated AJ in FIG. **3**, is applied to terminal **300** in FIG. **5**. As will appear more fully, this external clock is used, in effect, to slow down the rate of data transmission or receipt with the present equipment, thus to afford adequate time in which all data transmitted or received can be recorded by the off-line printer. As an example, the AJ clock signals may be spaced in time by an amount of time allowing approximately four complete cycles of the memory, thus approximately four pulses of the 05 clock between successive AJ clock pulses. Before discussing transmit and receive capabilities of the present circuitry, however, some basic operating conditions for the present circuit will be reviewed.

When the equipment is first turned on, random characters will appear in the memory which will be visually displayed by the cathode ray tube. When the operator notes the presence of these characters, the operator depresses a keyboard reset key which applies a "one" to terminal **301** in FIG. **5**. The "one" is inverted in gate G300 to produce a "zero" at terminal **302**. By circuitry not specifically disclosed in the present application, this "zero" is relayed as a short pulse to terminal **303** in FIG. **5**. When terminal **303** momentarily goes to "zero," a NAND

gate flip-flop comprising gates G301 and G302 is reset, causing gate 302 to go to an output of "one" and gate G301 to go to an output of "zero." Upon receipt of the next ensuing external clock pulse at terminal 300, the flip-flop F3 is set to its "zero" state. This will assure that the circuitry is in its compose mode. As will appear later, the flip-flop F3 will be set to its "one" mode to initiate a send or transmit mode of operation. Hence, the flip-flop F3 may be referred to as a mode control flip-flop. The operation of the keyboard reset button has, in effect, placed the circuitry in a stand-by mode, but has not cleared the memory of the random characters that may have appeared on the cathode ray display when the equipment was first turned on.

The circuitry includes several clear mechanisms. The entire memory, and therefore the entire cathode ray tube display, can be cleared by depressing a display clear key on the keyboard. This applies a "one" to terminal 304 in FIG. 5 and, since the circuit is in a stand-by mode, forces a "zero" output from a NAND gate G303. This "zero" is inverted in gate G304 to apply a "one" to terminal 203 in FIG. 5. Terminal 203 also appears in FIG. 10. A "one" on terminal 203 in FIG. 10 causes null characters to be clocked into the memory buffer. Provided the keyboard display clear key is depressed for a sufficient time, the entire memory will be cleared as successive null characters are introduced thereto.

Recalling that the memory cells are divided, 198 cells for composed messages and 198 cells for received messages, occasions will arise when the operator wishes only to clear the memory of composed messages. This is accomplished by depressing a Tx clear key on the keyboard which places a "one" on terminal 305 in FIG. 5. This "one" at terminal 305 forces a gate G306 to output a "zero," setting a NAND gate flip-flop comprising gates G324 and G305 to output a "one" from gate G324. It was previously mentioned that all message composition must occur when the fourth flip-flop (E4) of the E counter is in its "zero" state ($\overline{E4}$). An $\overline{E4}$ signal (a "one" during $\overline{E4}$ time) derived from the E counter is applied to terminal 306 of FIG. 5. During $\overline{E4}$ time, the $\overline{E4}$ signal forces a "zero" from gate G307. While the counter system remains in $\overline{E4}$ time, gate G307 forces gate G308 to a "one." The "one" output of gate G308 is applied to terminal 67 in FIG. 5. Terminal 67 also appears in FIG. 12 and functions when receiving a "one" from gate G308 in FIG. 5 to preset the Tx counter to its "zero" count. This assures that the next character to be entered to the memory from the keyboard will be entered in the first slot of the memory.

Gate G306 can implement this Tx counter reset function only if its other inputs are at a "one." One of its other inputs comes from gate G330 which says that the circuit is not now in its send mode. Thus, if the composed message is being transmitted in a manner to be later described, it cannot be erased.

The depression of the Tx clear key on the keyboard caused gate G307 to output a "zero" during $\overline{E4}$ time. This "zero" is passed to gate G304, forcing a "one" on terminal 203, thus writing null characters into the compose section of the memory during $\overline{E4}$ time only.

Provision is also made for clearing the section of the memory which is devoted solely to the receipt and display of externally received messages. For this function, a keyboard key herein designated the Rx clear key is depressed to apply a "one" to terminal 307 in FIG. 5. This "one" forces a NAND gate G310 to output a "zero." This "zero" from gate G310 sets a NAND gate flip-flop comprising gates G311 and G312 to output a "one" from gate G311. Gate G311 outputs this "one" to gate G313. This "one" is NANDed in gate G313 with an E4 timing signal received at terminal 308 in FIG. 5. Gate G313 thus outputs a "zero" only during E4 time. The "zero" output of gate G313 disables gate G304 so as to commence an entry of null characters to the memory during E4 time.

It will be later described that externally received messages are accounted for, character by character, by means of an Rx counter performing essentially the same function that the Tx counter performs for message compositions. The Rx counter is operated in association with an Rx complementary counter performing the same function for received messages as does the Tx complementary counter for composed messages. In clearing received messages from the memory by the Rx clear signal applied to terminal 307 in FIG. 5, it is thus necessary to reset the Rx counter to its "zero" state in the same fashion as occurred with the Tx counter when the Tx clear signal was applied to terminal 305 in FIG. 5. This Rx clear function is obtained from a signal relayed from gate G313 through gates G314 and G315 to terminal 309 in FIG. 5.

Should the operator elect to clear the entire display by depressing the keyboard display clear key which applies a "one" to terminal 304 in FIG. 5, it will be noted that the resulting "zero" output of gate G303 is passed to both gates G308 and G314 to assure that both the Tx and Rx counters are properly preset to their "zero" states.

It can now be assumed that a complete message has been composed in the memory of the circuitry being described. Before any composed message can be transmitted, certain prerequisites must be met. The first prerequisite is that a start-of-message character (0, 1, 1, 1, 1, 1) occupy the first cell of the memory. Such character is encoded from the keyboard in routine fashion by the keyboard operator. As will be later described, the start-of-message character is required to implement the receive circuitry of the station to which the message is being transmitted.

An additional prerequisite is that the final character in the composed message be an end-of-message character (0, 1, 1, 1, 1, 0) that is routinely inserted to the memory by the keyboard operator. As will be more fully explained later, the receive mode implemented in a remote station by the start-of-message character is a self-perpetuating state and the end-of-message character is required to terminate this self-perpetuating state. Otherwise, unless the circuitry is reset at the remote station by a deliberate act of the remote station operator (as initiating a reset signal), a self-perpetuating receive mode at the remote station will preclude proper permanent copy recording at the remote station.

Assuming a properly composed and formatted message resides in the memory, transmission of the message proceeds as follows. A desirable requirement to transmit operation is that an off-line printer, not shown, which will print out all transmitted (and received) messages, be operatively connected to the equipment. Proper connection and availability of the off-line printer produce a "zero" at terminal 311 in FIG. 5 and therefore a "one" from gate G331. If no print-out is desired, the terminal 311 may be directly grounded instead. To initiate transmission, the operator depresses a Tx send key on the keyboard which applies a momentary "one" to terminal 310 of FIG. 5.

Assuming the off-line printer is properly connected in the circuitry, depression of the Tx send key at the keyboard will force gate G316 to a "zero." This will set the NAND gate flip-flop comprising gates G301 and G302, causing gate G301 to output a "one" and G302 to output a "zero." This "one" is immediately inverted through gate G309 and re-inverted by gate G308 to apply a "one" to terminal 67, thus presetting the Tx counter to its zero count level.

With aid of inverter gate G317, the "J" and "K" inputs to the flip-flop F3 are also conditioned to "one" and "zero," respectively. The next signal from the external clock to arrive at terminal 300 then clocks the flip-flop F3 to its "one" state. The $\overline{Q}$ output from F3 inverted through gate G319 enables gate G5, which passes the external clock to gate G3, permitting the external clock to initiate $\overline{A}$ strobes. The $\overline{Q}$ output from flip-flop F3 also acts on gates G309 and G308 to place a "zero" on terminal 67 in FIG. 5, thus removing the preset signal to the Tx counter.

As the circuit is being conditioned by the flip-flop F3 for transmission of messages, the $\overline{Q}$ output of F3 is being relayed through gates G321 and G330 to supply a "zero" to gate G1, thereby blocking further keyboard strobes and thus prevent-

ing any further message composition. This "zero" is also applied to terminal **57** in FIG. **5**. Terminal **57** appears in FIG. **11**. The "zero" on terminal **57** in FIG. **11** disables NAND gate **G54** thereby preventing any insertion of line advance characters during the transmit mode of operation. (As later apparent, this becomes necessary during the transmit mode since the T*x* counter is caused to count up during transmission and its recognition gates **G52** and **G71** through **G76** must be disabled.)

In the transmit mode, gate **G327** receives a "zero" from gate **G330**. Gate **327** thus outputs a "one" to inverter gate **G328**. The "zero" from gate **G328** is applied to the gate **G7** in FIG. **5** and to the terminal **326** in FIG. **5**. Terminal **326** in FIG. **5** also appears in FIG. **11** and the "zero" on this terminal in FIG. **11** merely conditions the flip-flop **F33** for proper handling of line feed signals when the circuitry is returned to the composed mode of operation. The "zero" applied to gate **G7** is employed to condition the flip-flop **F2** so as to cause the T*x* counter to necessarily count up during the transmit mode of operation.

When the first $\overline{A}$ pulse triggered by the external clock appears at terminal **28** in FIG. **5**, the T*x* counter will count to one. The next ensuing AO* BO* DO* EO* clock state will cause the count of one then residing in the T*x* counter to be complementary transferred to the T*x* complementary counter. The T*x* complementary counter next counts out, as described before, forcing a "zero" on gate **G28** in FIG. **8**. Due to the timing of the present circuitry, this "zero" will appear on gate **G28** in the transmit mode of operation now being described when the first character of the memory is in the memory buffer.

During the previously described compose mode of operation, the "zero" at gate **G28** gave rise to an $\bar{a}$ pulse at terminal **44** in FIG. **4**, which in turn caused entry of a new character to the memory. In the send mode now being described, a different mode of operation obtains.

Due to the "one" condition of the flip-flop **F3** in FIG. **5**, a "one" now appears at terminal **41** in FIG. **5** and a "zero" now appears at terminal **42** in FIG. **5**. These terminals appear in the T*x* complementary circuitry illustrated in FIG. **8**. The "one" on terminal **41** enables a gate **G38** to pass what would have been the $\bar{a}$ pulse to terminal **221** in FIG. **8**. At the same time the "zero" at terminal **42** in FIG. **8** disables gate **G37**, so as to prevent the compose mode of operation in which a new character would be transferred to the memory buffer.

The signal now appearing at terminal **221** in FIG. **8** is applied to an output buffer (see FIG. **3**) which gates the six bits of information residing at this instant in the memory buffer to interface amplifiers illustrated diagrammatically at **400** in FIG. **3** which transmit the six bits of information by means of a six channel frequency modulated signal.

It will be noted that the initiation of the send mode caused the first character in the memory to be presented to an output buffer which enabled the first character to be transmitted to a remote station but did not remove the first character from the memory.

When the next external clock signal arrives, the above described processes will be repeated except at this time the T*x* counter will have counted to its second count level and accordingly the second character will then be transmitted, as described. With successive signals from the external clock, successive characters will be transmitted. However, after the 197th character is transmitted from the memory, the T*x* counter, when triggered to count to its 198th count level, will lock up as before, preventing any further transmission.

It will be noted that all characters in the memory, including line advance characters, are transmitted. As previously explained, a properly formatted message composed in the memory of the present invention terminates with an end-of-message character. The end-of-message character, when in the memory buffer, is presented to the output buffer **411** which includes a decode gate, not shown, for recognizing the end-of-message character. When this character is recognized, a negative-going reset pulse is applied to terminal **303** in FIG. **5**. This pulse operates as previously described to reset the flip-flop F3 to its "zero" state, thus terminating the transmit mode of operation and resetting the circuitry, as previously described, to its compose mode of operation.

While it has been previously indicated that the present circuitry is designed for the receipt of messages being relayed from a remote station, no attempt has been made to specifically illustrate all of the message receive circuitry in the present application. This has been considered unnecessary for the reason that the receive circuitry operates substantially as does the message composition circuitry described in detail in preceding portions of the present description. It suffices therefore to discuss the message receiving circuitry by describing the analogy between the message composition circuitry and the message receiving circuitry.

The block diagram of FIG. **3** discloses interface amplifiers **401** which apply messages being received from a remote station to receive buffer gates diagrammatically shown at **402**. These buffer gates are comparable in operation to the keyboard buffer gates previously described. Any message information being broadcast to the circuitry being disclosed will be presented to the circuit at the buffer gates **402**. However, the circuit will not recognize any information presented at the buffer gates until a start-of-message character has appeared.

The interface amplifiers continuously refer the external AJ clock to the control logic and the control logic stands poised to convert the AJ clock to an R*x* clock which will be used to gate character information received at the buffer gates **402** into the circuitry of the present invention. However, until the start-of-message character has been received, the Rx clock is blocked from the receive circuitry.

As soon as a start-of-message character appears in the buffer gates **402**, it is recognized by a start-of-message gate **350**. This gate responds immediately to the start-of-message character to set a receive control flip-flop **F5** appearing in FIG. **3**. The flip-flop **F5** implements a number of circuit functions which follow one another in time.

The first function implemented by the flip-flop **F5** is application of a negative-going pulse to terminal **313** in FIG. **5**. This negative-going pulse is inverted and passed during **E4** time only by gate **G314**, re-inverted by gate **G315**, and applied to terminal **309** in FIG. **5**. Terminal **309** is associated with an Rx counter **406** shown diagrammatically in FIG. **3**.

The R*x* counter performs essentially the same function when a message is being received as does the T*x* counter when a message is being composed. A negative-going signal appearing at terminal **309** immediately following receipt of a start-of-message character is used to preset the R*x* counter to its zero count level. This preset function is analogous to the preset of the T*x* counter to its zero count level when the previously described T*x* clear function was implemented with the T*x* clear key associated with the keyboard.

Immediately after the R*x* counter has been preset to its zero condition, a delay mechanism associated with the control logic but not specifically disclosed in the present application gates the Rx clock from the control logic to the Rx timing gates **403** and to the Rx counter **406**. The Rx clock is basically analogous to the $\overline{A}$ signal previously described with reference to the compose mode. The R*x* clock thus clocks the R*x* counter to augment the R*x* counter to a count of one.

When the R*x* clock reaches the R*x* timing gates, it initiates a strobe from the timing gates to strobe the start-of-message character into the reservoir buffer **404**. The receiver buffer acts in the same fashion as does the keyboard buffer and holds the start-of-message character in readiness for entry to the memory buffer **45**. Summarizing the preceding events resulting from appearance of a start-of-message character at the receiver buffer gates **402**, the R*x* counter has been set initially to a zero count, the count of the R*x* counter has then been augmented to one, and the R*x* timing gates have responded to the R*x* clock to strobe the start-of-message character into the receiver buffer **404**.

By means of internal timing controls initiated by the flip-flop F5, a negative-going pulse is now applied to terminal 315 in FIG. 5. This negative-going pulse is inverted through gate G304 to apply a "one" to terminal 203 in FIG. 5. It will be recalled that terminal 203 in FIG. 5 also appears in FIG. 10 and a "one" on this terminal causes null characters to be written into the memory. During the receive mode, however, the gate G304 will pass the negative pulse applied to terminal 315 in FIG. 5 only during E4 time. Accordingly, the only portion of the memory that will be cleared by this mechanism is that portion of the memory which has been devoted to received messages. Thus, the logic circuitry being implemented by the flip-flop F5 at this point in time is clearing only the receive portion of the memory to prepare the memory for receipt of characters being transmitted from a remote station.

By conventional gating means not disclosed, the pulse applied to terminal 315 is so shaped that it will not clear the start-of-message character from the memory should that character have already reached the memory.

At some point after the start-of-message character has been strobed into the receiver buffer 404, the basic clock timing of the present invention will reach the clock state AO* BO* DO* E6*. Referring back to the composite mode of operation previously discussed, it will be recalled that the clock state AO* BO* DO* EO* provided a reference time for identifying slots in the memory, all compose data being entered to the memory in the first six "lines" of the memory which followed the AO* BO* DO* EO* counter state. In the receive mode the AO* BO* DO* E6* state references the first memory slot available for received messages. When the AO* BO* DO* E6* counter state occurs, the count in the Rx counter is complementarily transferred through gates G407 to an Rx complementary counter 408. The Rx complementary counter performs the same function in the receive mode of operation as did the Tx counter in the compose mode of operation. The Rx complementary counter is clocked by the C5 clock which has been previously described.

Under the conditions now being discussed, the Rx counter has a count of one. After the complementary transfer to the Rx complementary counter, the complementary counter is one C5 clock pulse removed from its lock-up position. When the first C5 clock pulse occurs, the Rx complementary counter will lock up, generating a strobe through strobe gate 409 which will strobe the start-of-message character through buffer gates 405 into the memory buffer 45. The start-of-message character thus becomes the first character in the receive portion of the memory whenever as message is being transmitted to the herein described circuitry from a remote station.

As successive received characters appear at the receiver buffer gates 402, they will be accounted for by the Rx counter and strobed into the memory buffer under timing supplied by the Rx complementary counter as driven by the C5 clock. It will be recognized that the Rx counter and the Rx complementary counter operate in the same fashion as did the Tx counter and the Tx complementary counter to place successively received characters one behind the other into the receive portion of the memory.

The present invention contemplates that any message transmitted is a perfectly composed message. This is one of the reasons for the previously described CRT display system. Thus, when the circuit is operating in its receive mode of operation, editing of a received message is entirely unnecessary and no provision is made during the receive mode of operation for editing of a received message. Since all line advance characters as well as all message characters are transmitted, the message received into the memory of the present invention from a remote station will be a perfectly formatted message.

The Rx counter is equipped with a gate 410 analogous to the gate G76 associated with the Tx counter. It was previously described that the gate G76 associated with the Tx counter recognized the 198 character composed into the memory and locked out further message composition by disabling gate G4 in FIG. 5. The gate 410 acts in similar fashion with respect to the Rx counter to limit any received message to 198 characters.

When any properly formatted message is being received, the last character in the message to be transmitted will be an end-of-message character. The end-of-message character, when appearing at the receiver buffer gates 402, is immediately recognized by an end-of-message gate 351. The end-of-message gate acts immediately to reset the flip-flop F5. The flip-flop F5 when reset terminates the receive mode of operation of the present circuitry and no further characters received at the receiver buffer gates will be recognized by the present circuitry until a new start-of-message character has been received.

It will be noted that the receive mode of operation implemented no circuitry which would modify the compose mode of operation. Thus, if the operator is composing a message when a start-of-message character is recognized by the circuitry of the present invention, the incoming message is received without any disturbance to the compose mode of operation being implemented by a keyboard operator. This is possible in the present invention because the memory is divided into two sections and one half of the memory can be used or changed independently of the other half. Insofar as an operator composing a message at the keyboard is concerned, the only noticeable effect a concurrent message receipt will have is that the operator will see the received message appear on the CRT display.

Except as will be hereinafter described, receipt of a message by the present circuitry from a remote station also has no effect on the transmission of messages from the present circuitry. In other words, message transmission and message reception can coincide. A condition imposed upon the present circuitry, however, is that all messages being transmitted be recorded by the aforementioned off-line printer. Likewise, all messages received are to be recorded on an off-line printer. To allow use of a single off-line printer for recording both messages being transmitted and messages being received, the present circuitry is uniquely adapted to give preference to received messages without losing transmitted messages.

To give a preference to received characters, the flip-flop F5, which implements the receive mode of operation, conditions gate circuitry, not shown, which changes a normal "zero" to a "one" on terminal 312 in FIG. 5 and a normal "one" to a "zero" on terminal 314 in FIG. 5. Terminal 314 also appears in FIG. 8 where the "zero" thereon inhibits gate G202. Gate G202, when inhibited, blocks transmission of the composed portion of the memory to the off-line printer.

Assume the circuit is operating in the transmit mode when a start-of-message character is recognized by the receive circuitry. As previously described, operation in the transmit mode is implemented by the flip-flop F3 in FIG. 5 which must be in its "one" or true state for transmission. Therefore, under the condition being described, the flip-flop F3 will be in its "one" state when the start-of-message character is recognized and when the "one" and "zero" signals, respectively, appear at the terminals 312 and 314 in FIG. 5. The "zero" on the $\overline{Q}$ output of F3, inverted by gate G321, applies a "one" to gate G320. The "one" appearing on terminal 312 in FIG. 5 forces the gate G320 to "zero," setting the NAND gate flip-flop comprising gates G322 and G323, thereby causing the gate G322 to place a "one" on the input to a one-shot 324. At some future point in time, either the message transmission or the message reception may terminate, but the gates G322 and G323 cannot reset until both transmission and reception terminate. When transmission terminates, the $\overline{Q}$ output of F3 will shift to a "one" applied to gate G325. When reception terminates, the "zero" on terminal 314 will shift to a "one" applied to gate G325. When both "ones" appear at the inputs to gate G325, the output of G325 is forced to a "zero." This condition causes the gates G322 and G323 to reset, removing the "one" input to the one-shot 324. This causes the one-shot 324 to fire a pulse to gate G301 and to flip-flop F4.

It will be noted that the one-shot **324** can only fire after the circuitry has been caused to transmit and receive messages simultaneously. Whenever any such simultaneous operation occurs, gate **G202**, by blocking transmitted messages, allows only the received message to pass to the printer. The transmission of a message from the present equipment is permitted to continue but obviously at least some characters are being transmitted without such characters being recorded. The one-shot **324** is used to retrieve the message characters which are being transmitted but not recorded.

When the one-shot **324** fires, its output pulse to the gate **G301** conditions the flip-flop **F3** to be reset to the transmit mode with the next AJ clock signal. Thus, as soon as both the transmission and reception modes have been terminated, following a period of simultaneity, the circuitry is returned promptly to its transmit mode. At the same time the output of the one-shot **324** forces the flip-flop **F4** to its "one" or true state. The Q output of the flip-flop **F4** is NANDed in gate **G329** with the Q output of the flip-flop **F3** forcing a "zero" on the output of the gate **G329**. This "zero" is NANDed with the $\overline{Q}$ output of the flip-flop **F3** in gate **G319** to force a "one" on the output of the gate **G319**. This "one" enables the gate **G5** to pass the AJ clock from terminal **300** thus enabling operation of the transmit mode of the present circuitry.

The $\overline{Q}$ output of the flip-flop **F4** is applied to terminal **325** in FIG. **5**. By circuitry not shown terminal **325** inhibits output buffer **411** so as to prevent re-transmission of the message composed in the memory of the present invention through the interface amplifiers **400**.

Thus, the firing of the one-shot **324** has instituted a re-transmission of the message, but this re-transmission is applied only to the printer to assure print-out of whatever message resides in the compose section of the memory. The message earlier transmitted through the interface amplifiers **400** is thus recaptured in its entirety for recordal by the printer.

In order to provide a full description of the present invention, circuit elements disclosed have been disclosed in their conventional terms. Thus, the foregoing description makes reference specifically to flip-flops, a term well understood in the art. It is to be realized however that flip-flops are merely one example of a bistable device.

Having thus described our invention, we claim:

**1**. In combination, a cyclic memory device having a number of code memory cells and including a first buffer, a first code source providing codes in serial relation and adapted to generate a strobe with each code, a first counter for counting said strobes, a second buffer, means responsive to each strobe to place the code provided therewith in said second buffer, clock means having different states, the number of different states of said clock means being equal to the number of code memory cells in said memory device, said clock means clocking said codes cyclically through said memory device, a second counter having a lock-up state, transfer means responsive to a selected state of said clock means to complementarily transfer the count of said first counter to said second counter whereby said second counter is set away from said lock-up state by a count equal to the count in said first counter, said clock means clocking said second counter whereby said second counter counts to its lock-up state following said transfer, means responsive to lock-up of said second counter to transfer the code then residing in said second buffer to said first buffer whereby successive codes received from said source enter successive cells of said memory device.

**2**. The combination of claim **1** including means to reverse the direction of count of said first counter so as to enter newly received codes in previously used memory cells.

**3**. The combination of claim **1** wherein said first counter comprises a plurality of bistable devices, said second counter comprises an equal number of bistable devices, and said means to complementarily transfer comprises means to transfer the complement of each bistable device in said first counter to a corresponding one of the bistable devices in said second counter.

**4**. The combination of claim **3** in which said bistable devices are flip-flops.

**5**. The combination of claim **1** including gate means to recognize a predetermined strobe count in said first counter, means responsive to said gate means upon recognition of said predetermined strobe count to augment the count in said first counter, and circuit delay means responsive to said gate means to enter a predetermined code in said first buffer after the code with which the strobe producing said recognized count was generated has been transferred to said first buffer.

**6**. The combination of claim **1** including a second code source providing second codes in serial relation and providing a second strobe with each second code, a third counter for counting said second strobes, a fourth counter having a lock-up state, a third buffer, means responsive to each second strobe to place the second code provided therewith in said third buffer, second transfer means responsive to a selected state of said clock means to complementarily transfer the count of said third counter to said fourth counter, said clock means clocking said fourth counter, and means responsive to lock-up of said fourth counter to transfer the second code then residing in said third buffer to said first buffer, the selected state of said clock means at which the count of said first counter is complementarily transferred to said second counter being different from the selected state of said clock means at which the count of said third counter is complementarily transferred to said fourth counter.

**7**. The combination of claim **6** including means to remove from said memory device those codes received from one only of said first and second code sources.

**8**. Circuitry for placing codes in a cyclic memory device driven by a cyclic clock having plural clock states equal in number to the cells in said memory device comprising, in combination, a code source, said source adapted to generate a strobe with each code issued therefrom, a first counter for counting said strobes, code receiver means, means responsive to each said strobe to transfer the code provided therewith to said receiver means, a second counter having a lock-up state, means responsive to a selected state of said clock means to complementarily transfer the count of said first counter to said second counter, said clock means clocking said second counter, and means responsive to lock-up of said second counter to transfer the code from said receiver means to said memory device.

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