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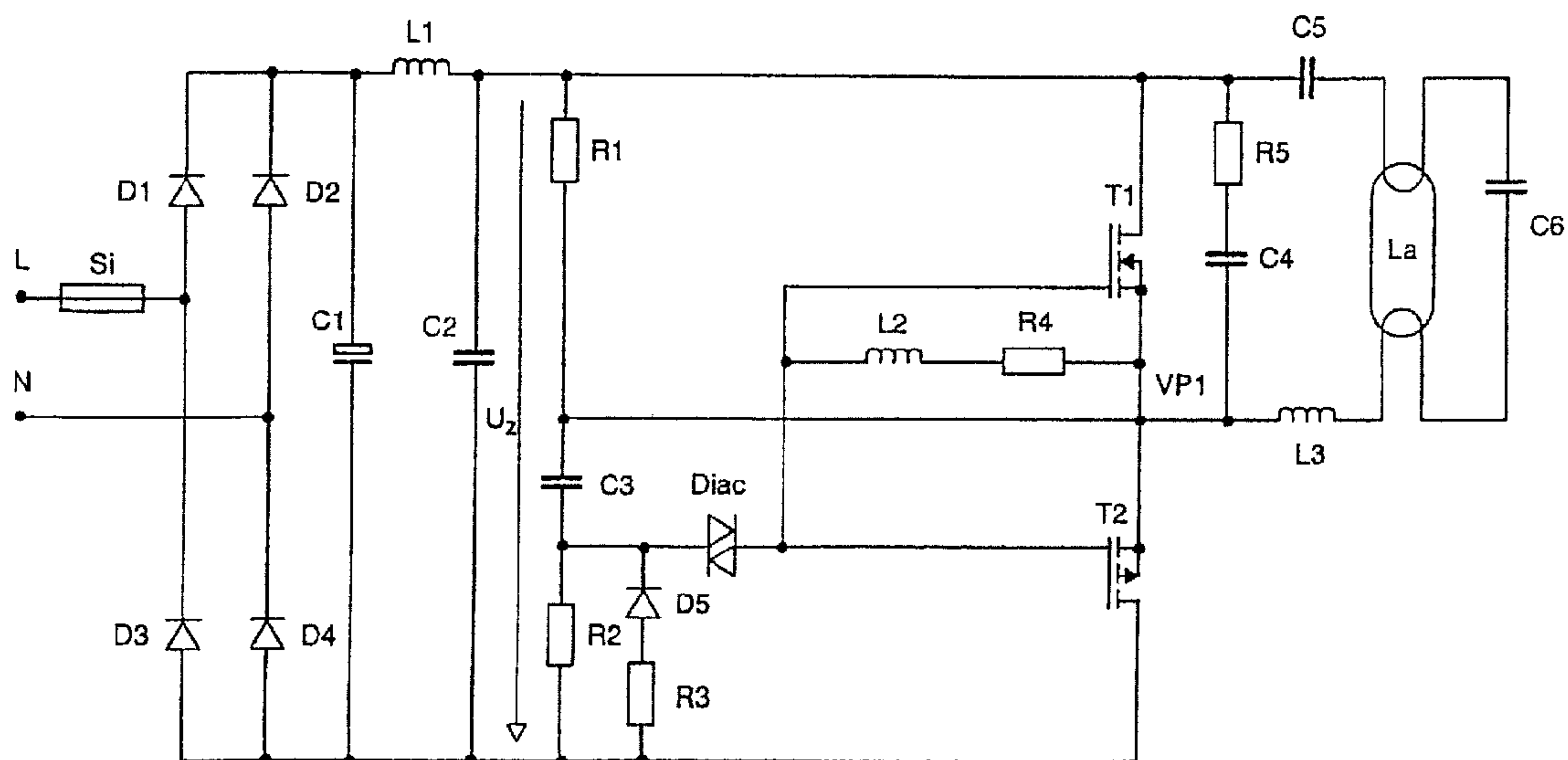
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(54) Titre : DISPOSITIF DE CIRCUIT A OSCILLATION LIBRE

(54) Title: FREE-RUNNING CIRCUIT ARRANGEMENT



(57) Abrégé/Abstract:

The present invention relates to a free-running circuit arrangement for operating a load (La), having at least one switching element (T1, T2), a freewheeling diode that is connected in an anti-parallel fashion relative to the main current direction of the at least one switching element (T1, T2), a load circuit (L3, C6, C5) and a control resonant circuit (L2, C_{E,T1}, C_{E,T2}) which comprises at least one control inductor (L2) and at least one self-capacitance (C_{E,T1}, C_{E,T2}) of the at least one switching element (T1, T2), the at least one switching element (T1, T2) having a control electrode, a working electrode and a reference electrode, there acting between the control electrode and the working electrode a capacitance (C_{M,T1}, C_{M,T2}) that is coupled to the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) in such a way that energy is fed into the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) by the charging and discharging current (I_{CM,T1}, I_{CM,T2}) of this capacitance (C_{M,T1}, C_{M,T2}), the circuit arrangement having no components for feeding energy into the control resonant circuit by electromagnetic coupling.



Abstract

Free-running circuit arrangement

The present invention relates to a free-running circuit arrangement for operating a load (L_a), having at least one switching element (T_1 , T_2), a freewheeling diode that is connected in an anti-parallel fashion relative to the main current direction of the at least one switching element (T_1 , T_2), a load circuit (L_3 , C_6 , C_5) and a control resonant circuit (L_2 , C_{E,T_1} , C_{E,T_2}) which comprises at least one control inductor (L_2) and at least one self-capacitance (C_{E,T_1} , C_{E,T_2}) of the at least one switching element (T_1 , T_2), the at least one switching element (T_1 , T_2) having a control electrode, a working electrode and a reference electrode, there acting between the control electrode and the working electrode a capacitance (C_{M,T_1} , C_{M,T_2}) that is coupled to the control resonant circuit (L_2 , C_{E,T_1} , C_{E,T_2}) in such a way that energy is fed into the control resonant circuit (L_2 , C_{E,T_1} , C_{E,T_2}) by the charging and discharging current (I_{CM,T_1} , I_{CM,T_2}) of this capacitance (C_{M,T_1} , C_{M,T_2}), the circuit arrangement having no components for feeding energy into the control resonant circuit by electromagnetic coupling.

US-Version/RAI

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Title

5 **Free-running circuit arrangement**

Technical Field

10 The present invention relates to a free-running circuit
arrangement for operating a load, having at least one
switching element, a freewheeling diode that is
connected in an anti-parallel fashion relative to the
main current direction of the at least one switching
15 element, a load circuit and a control resonant circuit
which comprises at least one control inductor and at
least one self-capacitance of the at least one
switching element.

Background Art

20 Such a generic free-running circuit arrangement is
disclosed in DE 195 48 506. The principle in accordance
with which this circuit operates can be gathered from
figure 1 there: an inductor L2, in this case the lamp
25 inductor, arranged in the load circuit is coupled to
two auxiliary windings HW1 and HW2, the auxiliary
winding HW1 being arranged in the control resonant
circuit of a first switching element T1, and the
auxiliary winding HW2 being arranged in the control
30 resonant circuit of a second switching element T2. The
oscillation of the circuit arrangement is maintained by
electromagnetic feedback of energy from the load
circuit into the respective control resonant circuit.

35 The disadvantage of this circuit arrangement consists
in that wound items are very expensive and therefore
substantially predetermine the costs of a circuit
arrangement in addition to transistors.

- 2 -

It is therefore the object of the present invention to develop the generic free-running circuit arrangement in such a way that it is possible to maintain an oscillation without this requiring electromagnetic coupling of components of the load circuit to components of the control resonant circuit.

Disclosure of the invention

10 This object is achieved according to the invention by virtue of the fact that in the case of the generic free-running circuit arrangement the at least one switching element has a control electrode, a working electrode and a reference electrode, there acting
15 between the control electrode and the working electrode a capacitance that is coupled to the control resonant circuit in such a way that energy is fed into the control resonant circuit by the charging and discharging current of this capacitance, the circuit
20 arrangement having no components for feeding energy into the control resonant circuit by electromagnetic coupling.

The invention is based on the finding that the energy
25 required to maintain the oscillation can be fed to the control resonant circuit via a capacitance. An expensive, frequently individually fabricated transformer is therefore no longer necessary.

30 A further advantage of the circuit arrangement according to the invention consists in that the circuit arrangement can be implemented with a smaller number of components.

35 In a particularly advantageous embodiment, one switching element has a Miller capacitance, the capacitance acting between the control electrode and the working electrode on the switching element comprising the Miller capacitance of the at least one

- 3 -

switching element. Miller capacitances occur, for example, in field effect transistors. Depending on the design of the circuit, it can be possible that the Miller capacitance of the at least one switching element is alone sufficient to supply energy to the control resonant circuit for maintaining the oscillation. Should the Miller capacitance not suffice alone, an additional discrete capacitance can be connected in parallel with it.

10

It is therefore particularly advantageous to tune the control resonant circuit and the Miller capacitance of the at least one switching element to one another in such a way that the oscillation of the control resonant circuit is maintained solely by the charging and discharging currents of the Miller capacitance of the at least one switching element. This results in a further saving on components. However - as mentioned - it can also be provided to connect an additional capacitance in parallel with the Miller capacitance of the at least one switching element, the oscillation of the control resonant circuit being maintained by the charging and discharging currents of the Miller capacitance and of the additional capacitance of the at least one switching element.

25

The input capacitance present between control and reference electrodes of the at least one switching element can be used as the self-capacitance of the latter.

30

It is preferred for the circuit arrangement according to the invention to have a first and a second switching element, the first and the second switching elements being of complementary design and being coupled to a common control resonant circuit. The complementary design of the switching elements permits the use of a common control resonant circuit for both switching elements. It is preferred in this case for each

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- 4 -

- switching element to have a control electrode, a working electrode and a reference electrode, the control electrodes being connected to one another with the formation of a first tie point, and the reference electrodes being connected to one another with the formation of a second tie point, the control inductor being coupled between the first and the second tie point.
- 10 However, it can also be provided that the circuit arrangement has a first and a second switching element that are of the same type, the first switching element being coupled to a first control resonant circuit, and the second switching element being coupled to a second control resonant circuit. Again, it is preferred for each switching element to have a control electrode, a working electrode and a reference electrode, the reference electrode of the first switching element being connected to the working electrode of the second switching element, and the respective control inductor being coupled between the respective control and reference electrodes of the respective switching element. This implementation has the advantage that two switching elements of identical type can be used, the electric performance thereby also being identical.

The first and the second switching element are preferably arranged in a half-bridge arrangement.

- 30 The load is preferably an illuminating means, preferably a low-pressure discharge lamp. However, it is also possible to use the circuit for other types of loads.
- 35 For the case in which the input capacitance of the at least one switching element is unfavorably dimensioned for implementing the circuit arrangement, it is preferred to connect a discrete supplementary capacitance in parallel with the input capacitance of

- 5 -

the at least one switching element. This option yields further degrees of freedom for dimensioning the control resonant circuit.

- 5 The load circuit preferably has a series tuned circuit with an inductor, a capacitance connected in parallel with the load and at least one decoupling capacitance. The inductor is preferably dimensioned as a current-limiting and resonance inductor.

10

The at least one switching element is preferably a bipolar transistor or an MOS field effect transistor. For the case in which the circuit arrangement is implemented with the aid of at least one MOS field
15 effect transistor, the body diode of the MOS field effect transistor can implement the freewheeling diode connected in an anti-parallel fashion. A discrete diode is to be provided as freewheeling diode in the case of an implementation of the at least one switching element
20 as bipolar transistor.

Further advantageous developments of the invention are defined in the subclaims.

25

Brief description of the drawings

An exemplary embodiment of the invention is described in more detail below with reference to the attached drawings, in which:

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figure 1 shows a circuit diagram of a ballast for operating an illuminating means, having a free-running circuit arrangement according to the invention;

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figure 2 shows a detail of the ballast in figure 1, transistor capacitances being illustrated by dashes;

- 6 -

figure 3 shows the detail of figure 2 with additional capacitances for increasing the input capacitances and the Miller capacitances of the transistors;

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figures 4a to 4g show a time sequence of the current flows as they occur in the detail in accordance with figure 2; and

10 figure 5 shows the time profile of some variables of the detail in figure 2.

Best mode for carrying out the invention

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The ballast illustrated in figure 1 has a supply connection L, N that is connected via a fuse Si to a rectifier comprising four diodes D1, D2, D3, D4. The DC voltage smoothed by a capacitor C1 is made available
20 via a filter having an inductor L1 and a capacitor C2 as what is termed intermediate circuit voltage U_z of the free-running circuit arrangement. Because of the voltage U_z , the capacitor C3 is charged via the resistors R1 and R2. The circuit also comprises two MOS
25 field effect transistors T1, T2, the drain terminal of the transistor T1 being connected to the positive terminal of the capacitor C2, the drain terminal of the transistor T2 being connected to the negative terminal of the capacitor C2. The source terminals of the two
30 transistors T1, T2 are connected to one another with the formation of a tie point VP1, the tie point VP1 being connected to the positive terminal of the capacitor C3. The negative terminal of the capacitor C3 is connected to frame via a diode D5 and a resistor R3,
35 the diode D5 and resistor R3 ensuring that the capacitor C3 is discharged during operation of the circuit arrangement, that is to say when the transistor T2 is turned on, so that the diac that is connected between the negative terminal of the capacitor C3 and

- 7 -

the two gate terminals of the two transistors T1, T2 is not ignited in an interfering fashion during operation of the circuit arrangement. The series connection of an inductor L2 and a resistor R4 is arranged between the tie point VP1 and the interconnected gate terminals of the transistors T1, T2. Arranged on the one hand between the drain terminal of the transistor T1 and the tie point VP1 is the series connection of a resistor R5 and a capacitor C4, the series connection being connected in parallel with the series connection of a capacitor C5, the illuminating means La and the lamp inductor L3, a capacitor C5 being connected in parallel, for its part, to the illuminating means La.

Figure 2 shows a detail of the ballast of figure 1, the transistor capacitances being illustrated by dashes. Arranged between the respective gate terminal and the respective drain terminal is the respective Miller capacitance $C_{M,T1}$ or $C_{M,T2}$, the respective input capacitance $C_{E,T1}$ or $C_{E,T2}$ is arranged between the respective gate terminal and the respective source terminal, while the respective output capacitance $C_{A,T1}$ or $C_{A,T2}$ is arranged between the respective drain terminal and the respective source terminal.

For the case in which the transistor input capacitances $C_{E,T1}$, $C_{E,T2}$ and/or the Miller capacitances $C_{M,T1}$ or $C_{M,T2}$ are not sufficiently large to maintain oscillation, figure 3 shows a preferred option for their enlargement. Here, a capacitance C_{MZ} is connected in parallel with the Miller capacitances $C_{M,T1}$, $C_{M,T2}$, while a capacitance C_{EZ} is connected in parallel with the input capacitances $C_{E,T1}$, $C_{E,T2}$.

Figure 4 shows snapshots of the current flows in the circuit detail of figure 2, in time sequence. Corresponding to this, the time profile of some variables of the circuit detail of figure 2 is illustrated in figure 5 with reference to the voltages

- 8 -

illustrated in figure 2.

Before considering the normal operation, that is to say the maintenance of an oscillation of the free-running
5 circuit arrangement, the first aim is to explain the processes that unfold until a self-maintaining oscillation is produced. The starting point is a DC voltage present across the capacitor C2 as a result of which the capacitor C3 is charged via the resistors R1,
10 R2. Because of the voltage rise across C3, the voltage present at the diac also rises. If the latter voltage exceeds the trigger threshold of the diac, the latter turns on and, as a result, a negative voltage pulse reaches the two gate terminals of the complementary
15 transistors T1 and T2. This charges the capacitances $C_{M,T1}$, $C_{E,T1}$, $C_{E,T2}$, while the capacitance $C_{M,T2}$ is discharged. The current flow illustrated in figure 4a is set up.

20 Because of the negative voltage pulse at the gate electrodes of the two transistors, which is effected by the ignition of the diac, the transistor T2 is opened, see the current flow I_{ST2} in period 4b in figure 5. Consequently, a current begins to flow in the load
25 circuit via the capacitor C5, the capacitor C6 and the inductor L3. The current I_{ST2} , increasing in absolute terms, flows against the voltage direction $U_{CA,T2}$ defined in figure 2, and therefore has a negative sign. The negative voltage pulse at the gate electrode
30 simultaneously causes the rise of a control current I_{L2} through the inductor L2, which for the most part once again reverses the charge of the two input capacitances $C_{E,T1}$, $C_{E,T2}$ of the transistors T1, T2. The current I_{L2} opposes the voltage supplied by the diac such that the
35 previously negative gate voltage is reduced.

With reference to figure 5, the start of the period 4c is typified in that after the threshold voltage of the transistor T2 is undershot the latter blows, and the

load current injected in the inductor L3 now flows via the resistor R5 and discharges the capacitor C4. At the same time as the change in the voltage across the capacitor C4, there is also a change in the voltage
 5 across the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ of the two transistors T1, T2. In particular, as a result of this the tie point of the two source electrodes is positioned virtually at the voltage U_z , the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ participating fully in this
 10 voltage excursion. The change in voltage at the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ effects a current flow in accordance with

$$I_c = C \cdot \frac{dU_c(t)}{dt}.$$

15

These charging and discharging currents $I_{CM,T1}$, $I_{CM,T2}$ effect an additional current flow through the inductor L2. In this phase, energy is fed to the control circuit via the Miller capacitances $C_{M,T1}$, $C_{M,T2}$.

20

The start of the period 4d is typified in that following the drop in the drain-source voltage across the transistor T1 the inner freewheeling diode thereof turns on, and thus takes over the main part of the
 25 current of the inductor L3. As soon as the majority of the load current is flowing via the freewheeling diode of the transistor T1, see I_{ST1} in figure 5, the charge-reversal processes of the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ are largely concluded. The current injected in the
 30 inductor L2 now chiefly reverses the charge of the two input capacitances $C_{E,T1}$, $C_{E,T2}$ of the two transistors T1, T2, and first effects a further drop in the gate voltage to zero and finally a rise to positive voltage values. After the threshold voltage of the transistor
 35 T1 is exceeded, the latter is turned on. The current injected in the inductor L2 decays to zero during the on phase of T1, the start of period 4e being defined thereby. The input capacitances $C_{E,T1}$ and $C_{E,T2}$ of the two

- 10 -

transistors T1, T2 are charged appropriately such that the current can now flow from the charged capacitances to the gate circuit L2, R4 (just as in the load circuit, in the control circuit the result is also a current reversal). The control current I_{L2} through the inductor L2, which is now flowing in the reverse direction, counteracts the still positive gate voltage. The gate voltage, which therefore decreases, finally undershoots the threshold voltage of the transistor T1, such that the latter turns off. This is the start of period 4f of figure 5. The current injected in the inductor L3 now flows again via the resistor R5 and charges the capacitor C4. At the same time as the change in the voltage across the capacitor C4, there is also a change in the voltage across the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ of the two transistors T1, T2. The charging and discharging currents $I_{CM,T1}$, $I_{CM,T2}$ thereby constrained again effect an additional current flow through the inductor L2, see the lowermost diagram in figure 5. In this phase, energy is fed to the control circuit once more via the Miller capacitances $C_{M,T1}$, $C_{M,T2}$. After a rise in the voltage via the Miller capacitance $C_{M,T2}$ of the transistor T2, the internal freewheeling diode of the transistor T2 turns on and takes over the main part of the current of the inductor L3, see the start of period 4g. As soon as the majority of the load current is flowing via the freewheeling diode of the transistor T2, the Miller charge-reversal processes are largely concluded. The current I_{L2} injected in the inductor L2 chiefly reverses the charges of the two input capacitances $C_{E,T1}$, $C_{E,T2}$ of the transistors T1, T2, and initially effects a further drop in the gate voltage to zero and, finally, a rise to negative voltage values.

35

The switching processes of periods 4b to 4g in figures 4 and 5 proceed further sequentially such that a current flow oscillating to and fro is produced in the control circuit and in the load circuit. The frequency

- 11 -

of this initial oscillation is somewhat higher than the resonant frequency of the load circuit. Finally, owing to resonance step-up the voltage across the illuminating means La rises so strongly that the latter
5 ignites. The majority of the load current is now flowing via the illuminating means La. After ignition, the illuminating means itself acts virtually like a purely ohmic consumer, and damps the resonant circuit in such a way that the voltage required for the stable
10 operation is finally set up across the illuminating means La.

The innovation of the present invention consists in principle in feeding so much energy to the control
15 resonant circuit in periods 4c and 4f owing to charging and discharging processes of the Miller capacitances $C_{M,T1}$, $C_{M,T2}$ of the two switching elements T1, T2 that an oscillation is maintained.

- 12 -

Claims

1. A free-running circuit arrangement for operating a load (La), having at least one switching element (T1, T2), a freewheeling diode that is connected in an anti-parallel fashion relative to the main current direction of the at least one switching element (T1, T2), a load circuit (L3, C6, C5) and a control resonant circuit (L2, C_{E,T1}, C_{E,T2}) which comprises at least one control inductor (L2) and at least one self-capacitance (C_{E,T1}, C_{E,T2}) of the at least one switching element (T1, T2), characterized in that the at least one switching element (T1, T2) has a control electrode, a working electrode and a reference electrode, there acting between the control electrode and the working electrode a capacitance (C_{M,T1}, C_{M,T2}) that is coupled to the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) in such a way that energy is fed into the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) by the charging and discharging current (I_{CM,T1}, I_{CM,T2}) of this capacitance (C_{M,T1}, C_{M,T2}), the circuit arrangement having no components for feeding energy into the control resonant circuit by electromagnetic coupling.
2. The circuit arrangement as claimed in claim 1, characterized in that the at least one switching element (T1, T2) has a Miller capacitance (C_{M,T1}, C_{M,T2}), and the capacitance acting between the control electrode and the working electrode of the switching element (T1, T2) comprises the Miller capacitance (C_{M,T1}, C_{M,T2}) of the at least one switching element (T1, T2).
3. The circuit arrangement as claimed in claim 2, characterized in that the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) and the Miller capacitance (C_{M,T1}, C_{M,T2}) of the at least one switching element (T1, T2) are tuned to one another in such a way that the oscillation of the control resonant circuit (L2, C_{E,T1}, C_{E,T2}) is

- 13 -

maintained solely by the charging and discharging currents ($I_{CM,T1}$, $I_{CM,T2}$) of the Miller capacitance ($C_{M,T1}$, $C_{M,T2}$) of the at least one switching element ($T1$, $T2$).

5 4. The circuit arrangement as claimed in claim 2, characterized in that an additional capacitance (C_{MZ}) is connected in parallel with the Miller capacitance ($C_{M,T1}$, $C_{M,T2}$) of the at least one switching element ($T1$, $T2$), the oscillation of the control resonant circuit
10 ($L2$, $C_{E,T1}$, $C_{E,T2}$) being maintained by the charging and discharging currents ($I_{CM,T1}$, $I_{CM,T2}$) of the Miller capacitance and of the additional capacitance (C_{MZ}) of the at least one switching element.

15 5. The circuit arrangement as claimed in claim 1, characterized in that the self-capacitance of the at least one switching element is a self-capacitance ($C_{E,T1}$, $C_{E,T2}$) of the latter present between control and reference electrodes.

20 6. The circuit arrangement as claimed in claim 1, characterized in that it has a first and a second switching element ($T1$, $T2$), the first and the second switching elements ($T1$, $T2$) being of complementary
25 design and being coupled to a common control resonant circuit ($L2$, $C_{E,T1}$, $C_{E,T2}$).

7. The circuit arrangement as claimed in claim 6, characterized in that each switching element ($T1$, $T2$)
30 has a control electrode, a working electrode and a reference electrode, the control electrodes being connected to one another with the formation of a first tie point, and the reference electrodes being connected to one another with the formation of a second tie
35 point, the control inductor ($L2$) being coupled between the first and the second tie point.

8. The circuit arrangement as claimed in claims 1, characterized in that it has a first and a second

- 14 -

switching element (T1, T2) that are of the same type, the first switching element (T1) being coupled to a first control resonant circuit, and the second switching element (T2) being coupled to a second control resonant circuit.

9. The circuit arrangement as claimed in claim 8, characterized in that each switching element (T1, T2) has a control electrode, a working electrode and a reference electrode, the reference electrode of the first switching element (T1) being connected to the working electrode of the second switching element (T2), and the respective control inductor being coupled between the respective control and reference electrodes of the respective switching element.

10. The circuit arrangement as claimed in one of claims 6 to 9, characterized in that the first and the second switching element (T1, T2) are arranged in a half-bridge arrangement.

11. The circuit arrangement as claimed in claim 1, characterized in that the load is an illuminating means (La), preferably a low-pressure discharge lamp.

12. The circuit arrangement as claimed in claim 5, characterized in that a supplementary capacitance (C_{EZ}) is connected in parallel with a input capacitance ($C_{E,T1}$, $C_{E,T2}$) of the at least one switching element (T1, T2).

13. The circuit arrangement as claimed in claim 1, characterized in that the load circuit comprises a series tuned circuit with an inductor (L3), a capacitance (C6) connected in parallel with the load and at least one decoupling capacitance (C5).

14. The circuit arrangement as claimed in claim 1, characterized in that the at least one switching

- 15 -

element (T1, T2) is an MOS field effect transistor, and the freewheeling diode connected in an anti-parallel fashion to the at least one switching element (T1, T2) is the body diode of the latter.

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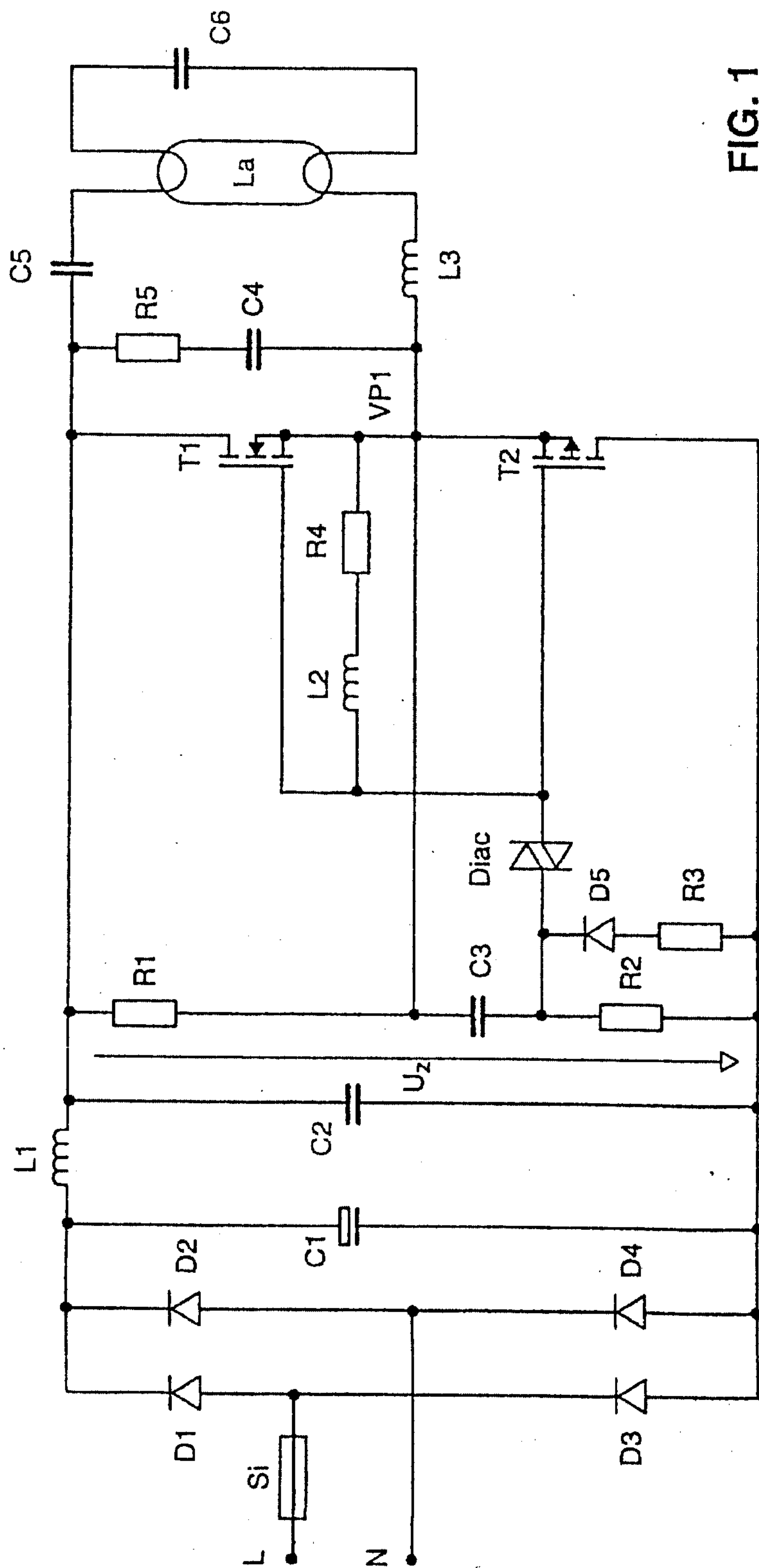
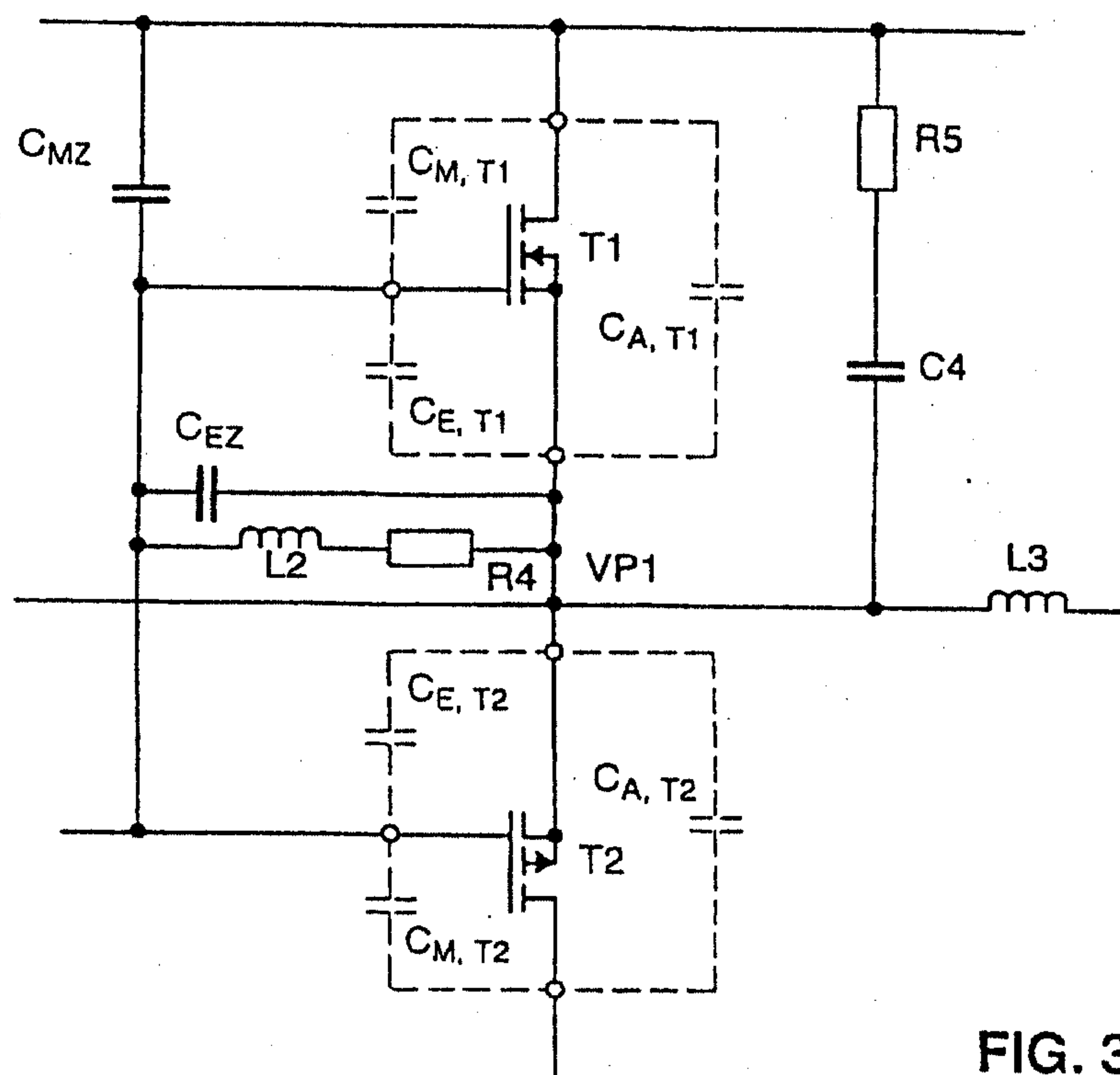
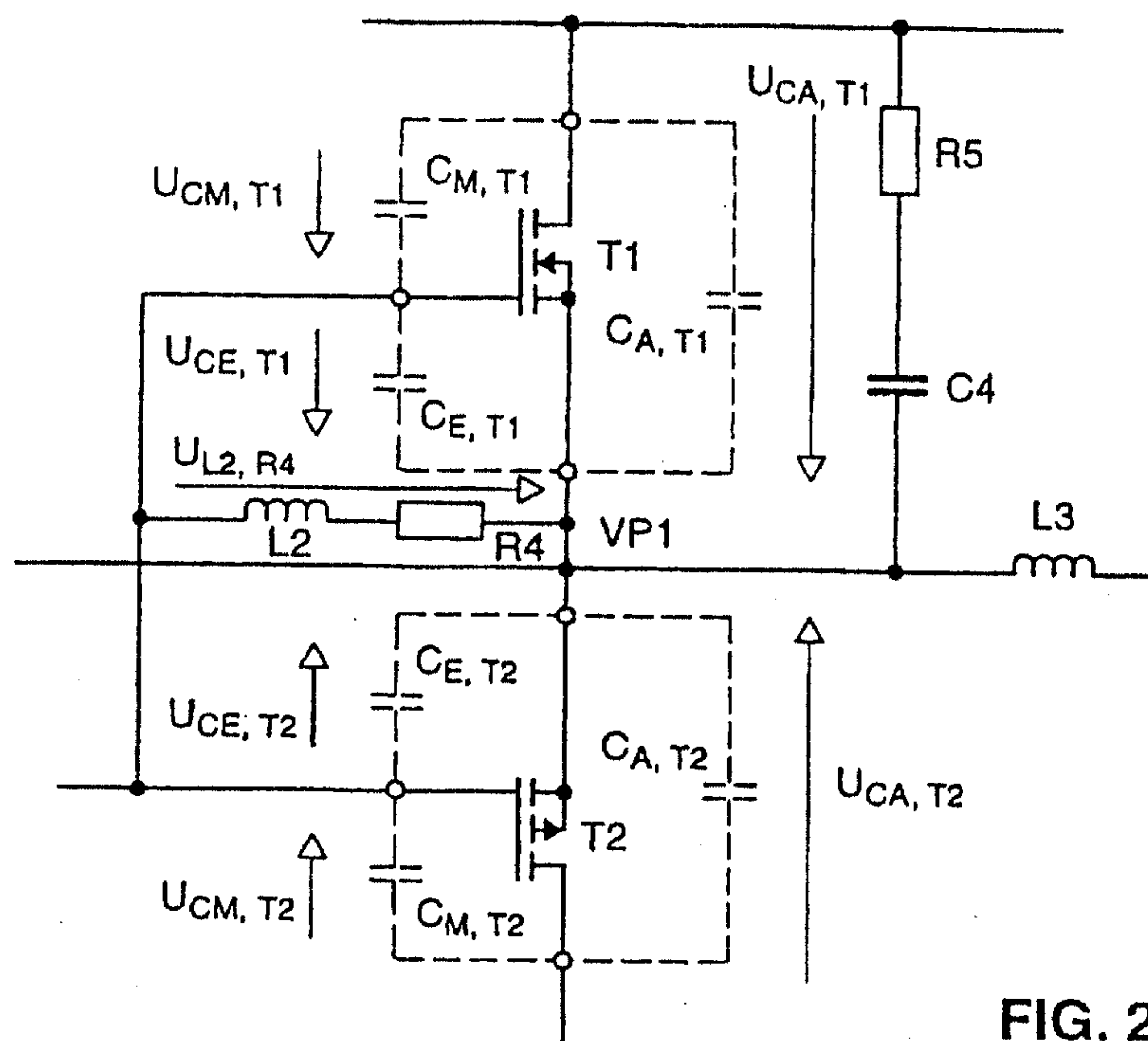
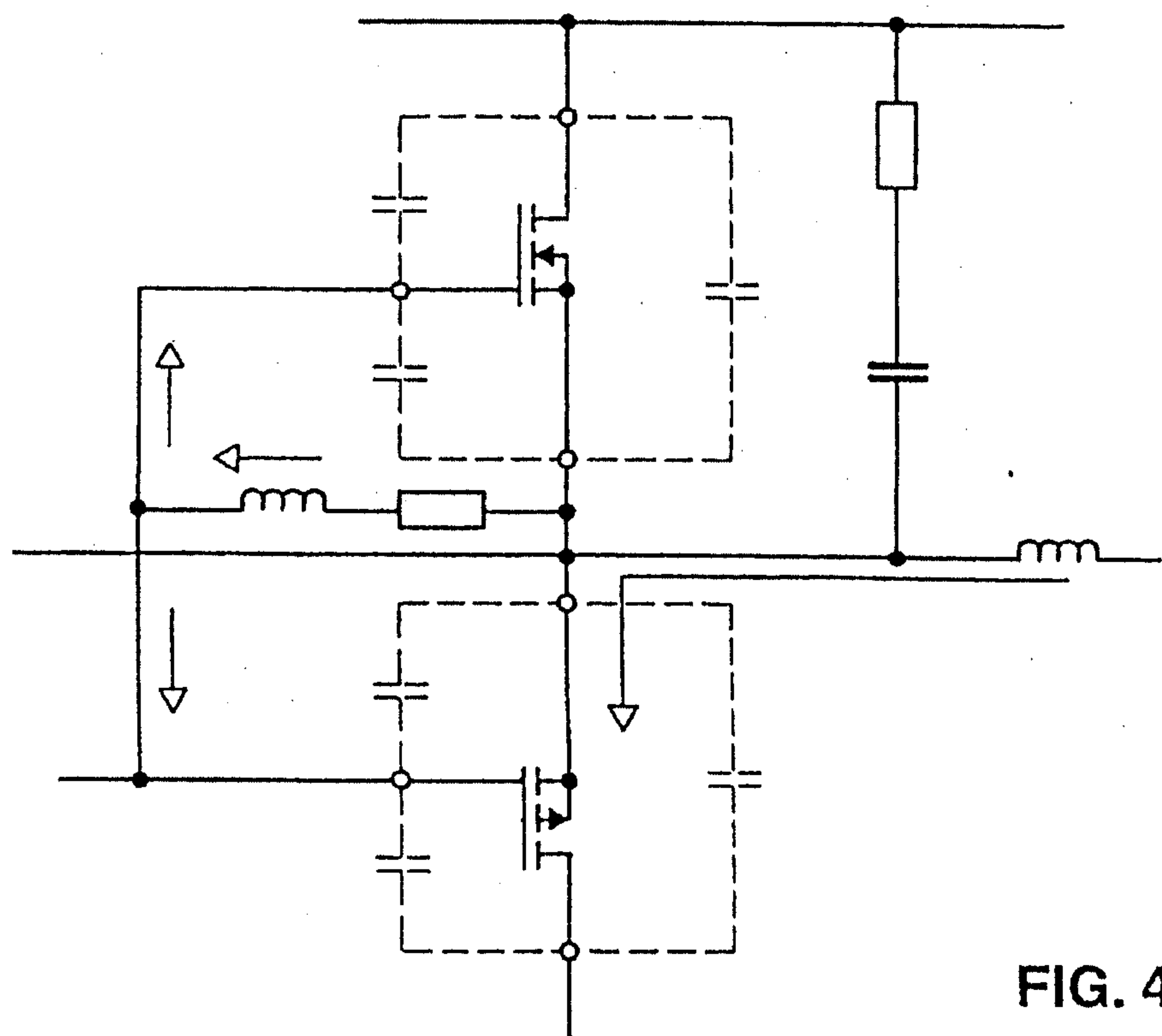
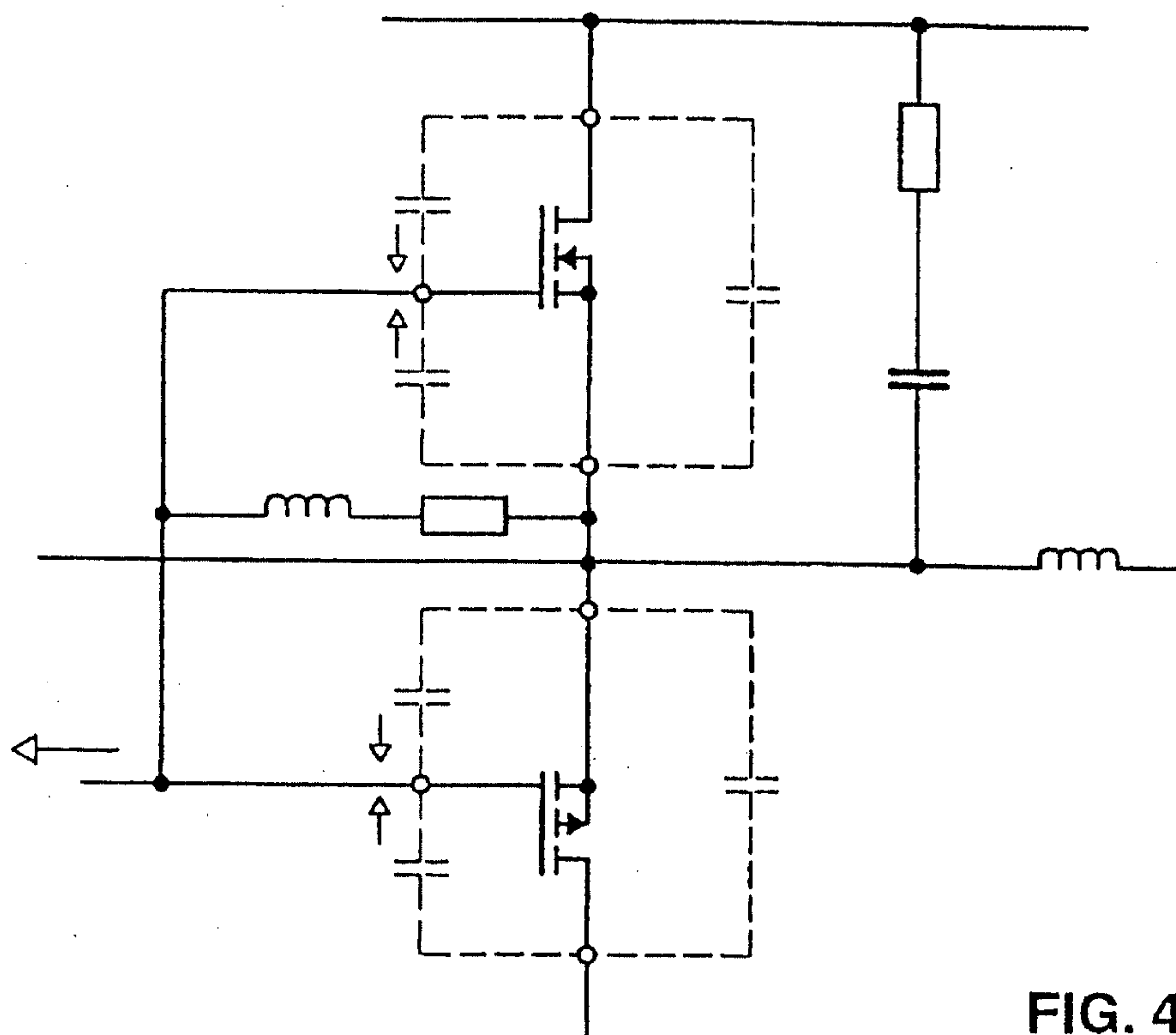


Fig. 1





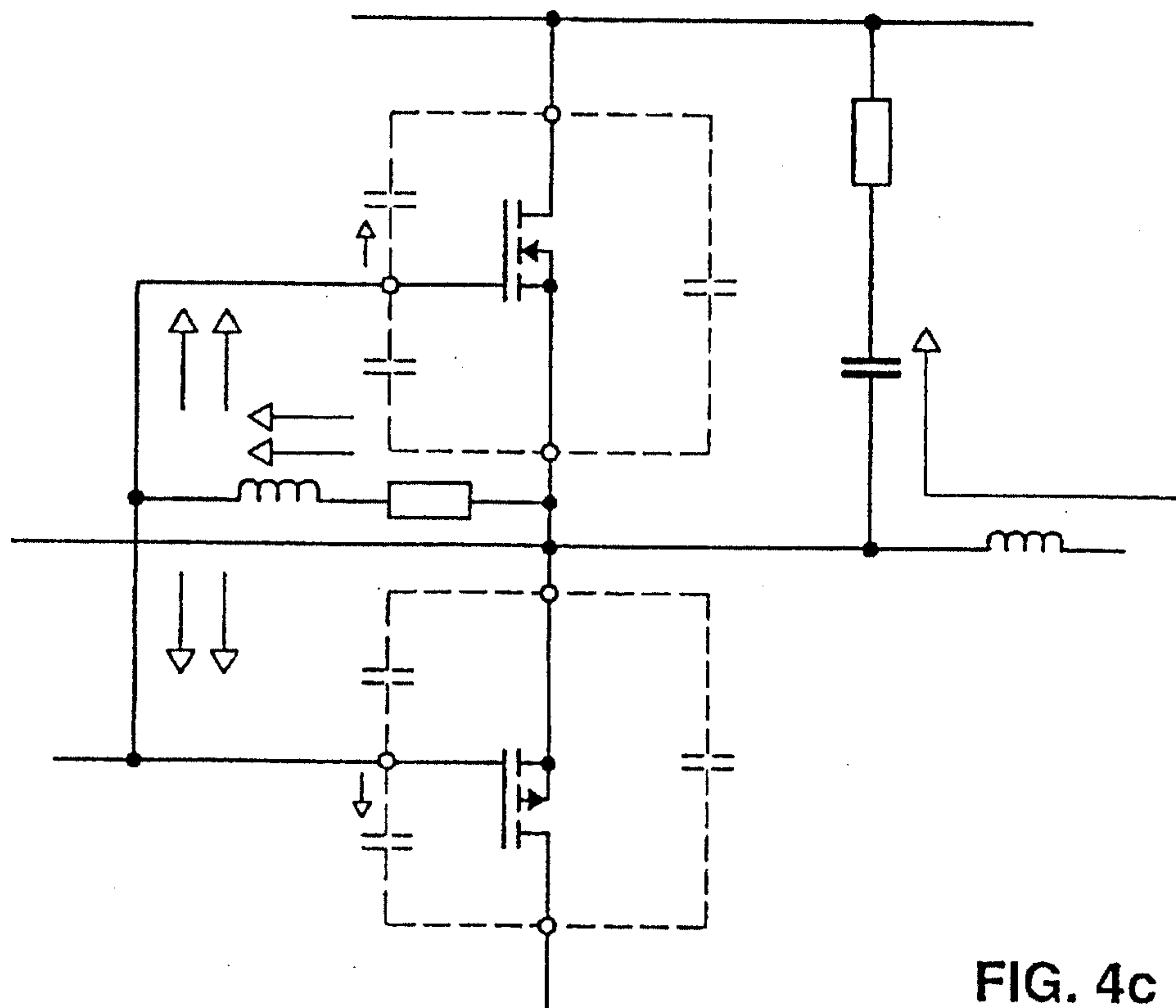


FIG. 4c

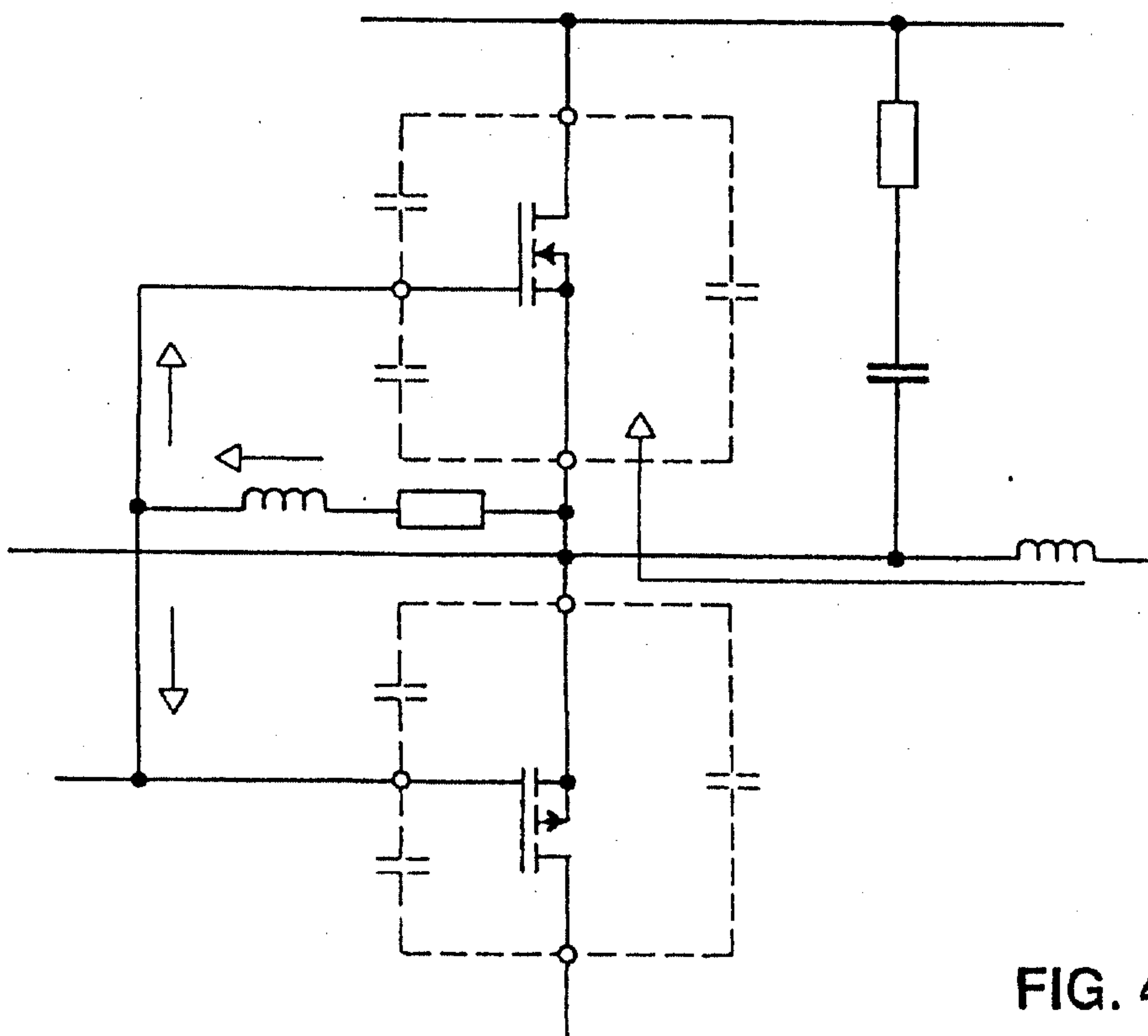


FIG. 4d

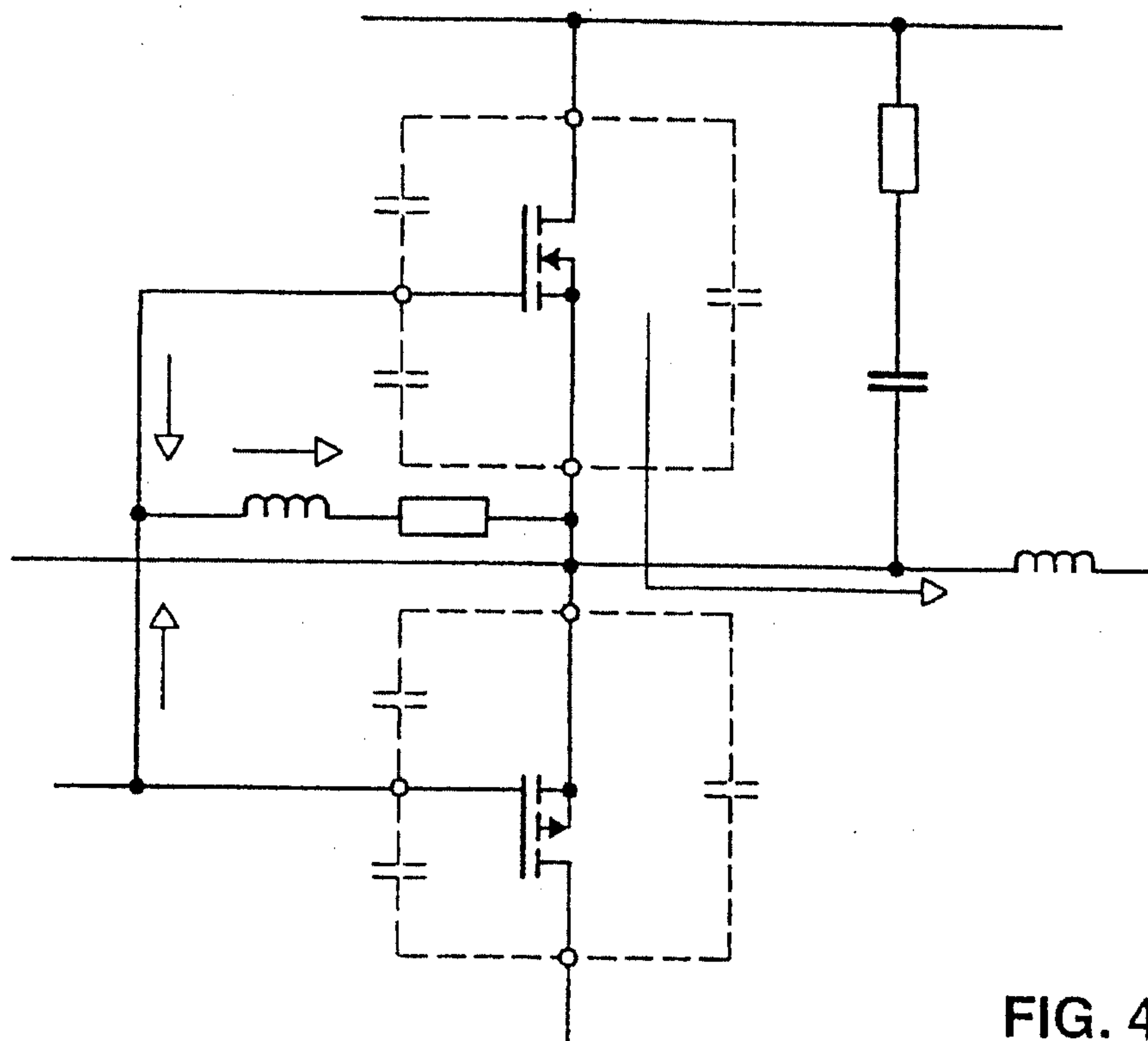


FIG. 4e

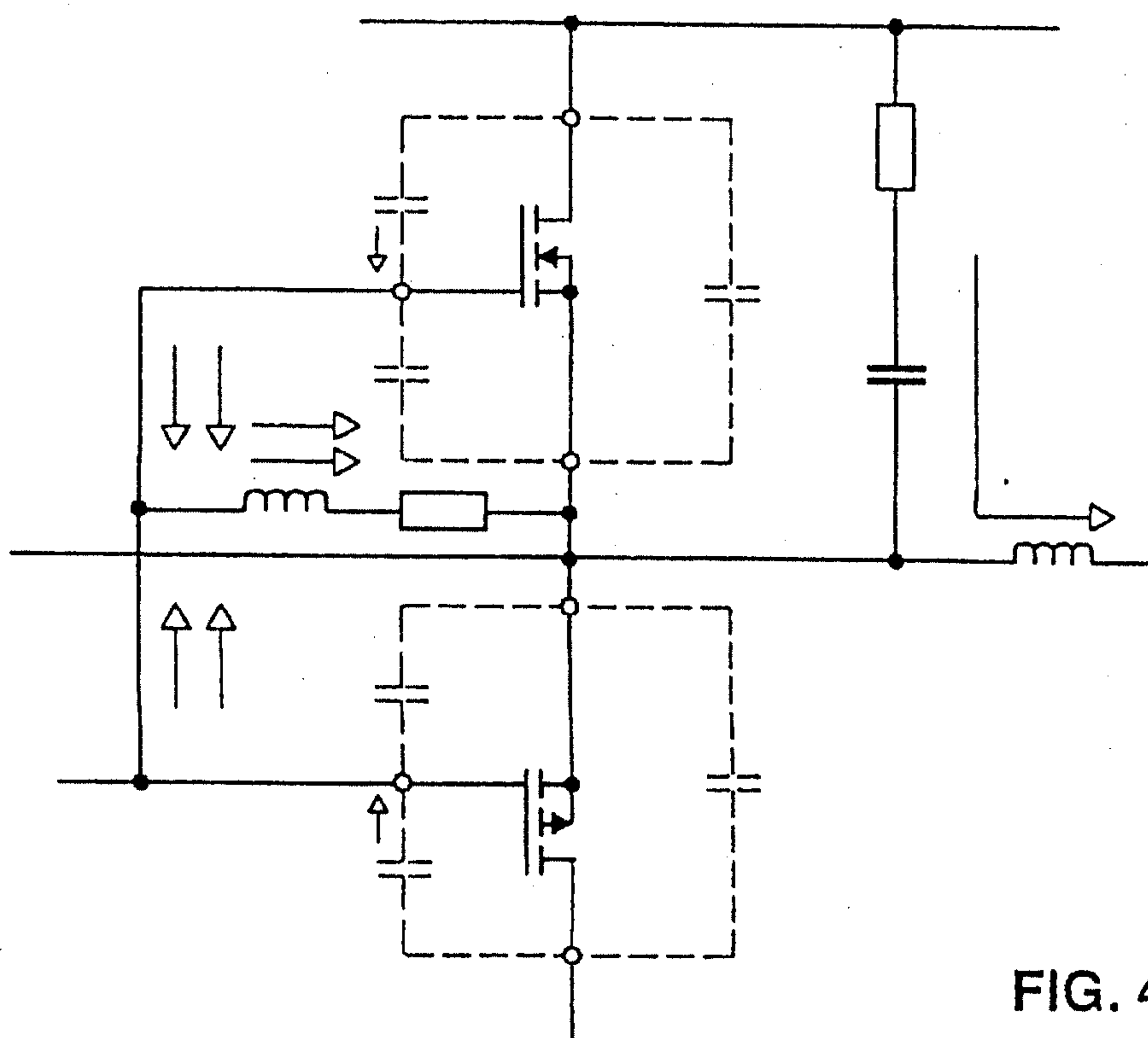
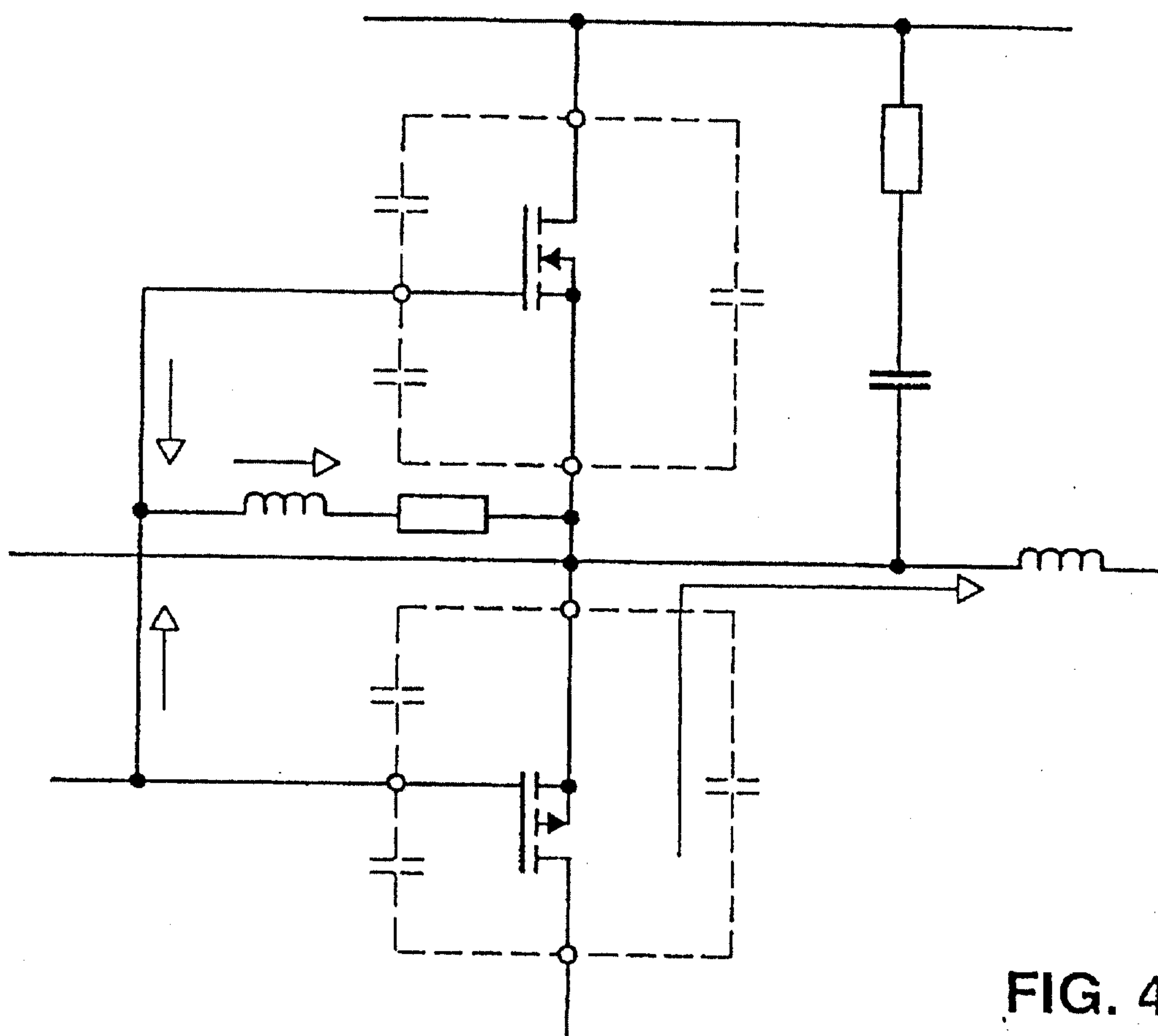


FIG. 4f



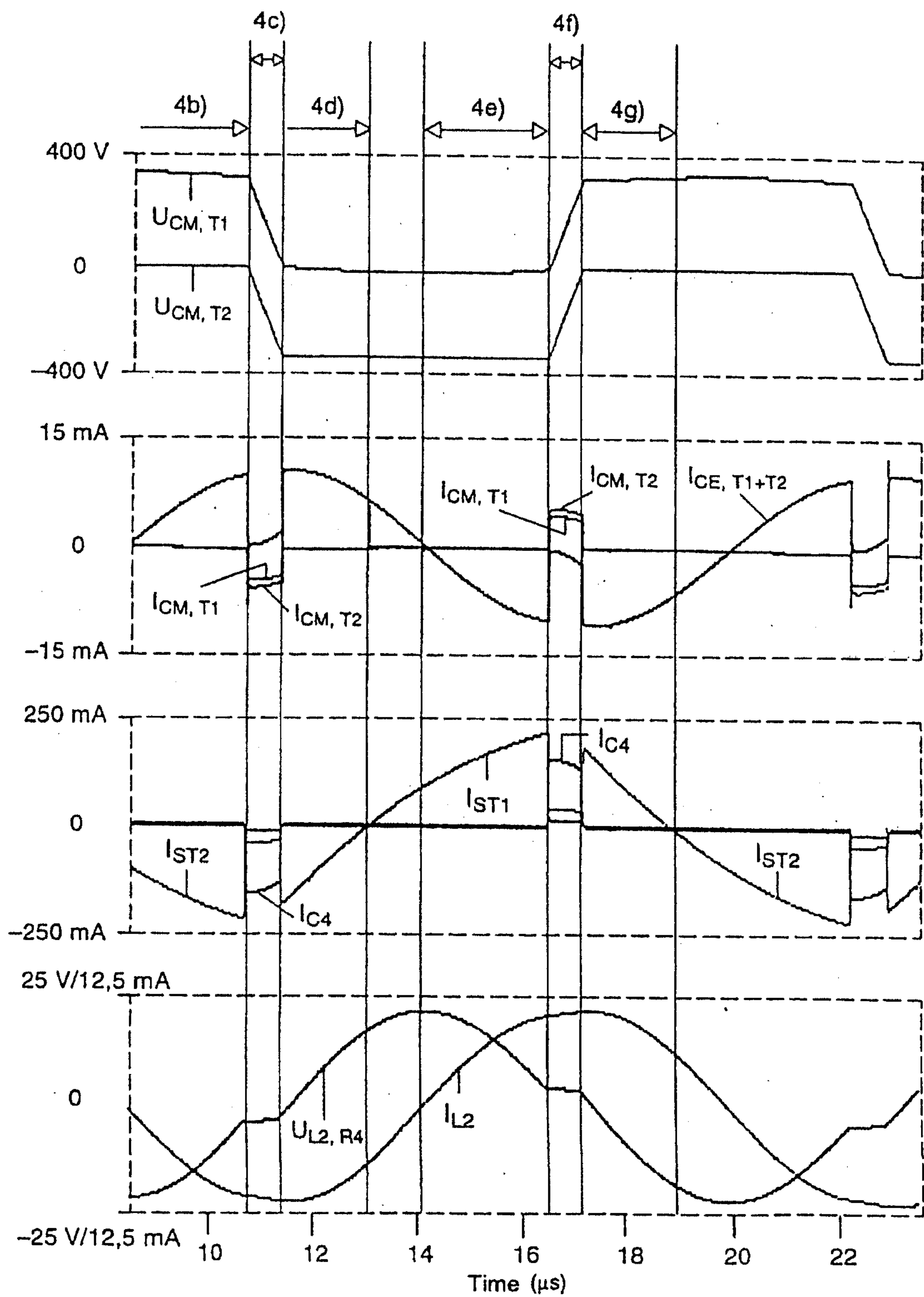


FIG. 5

