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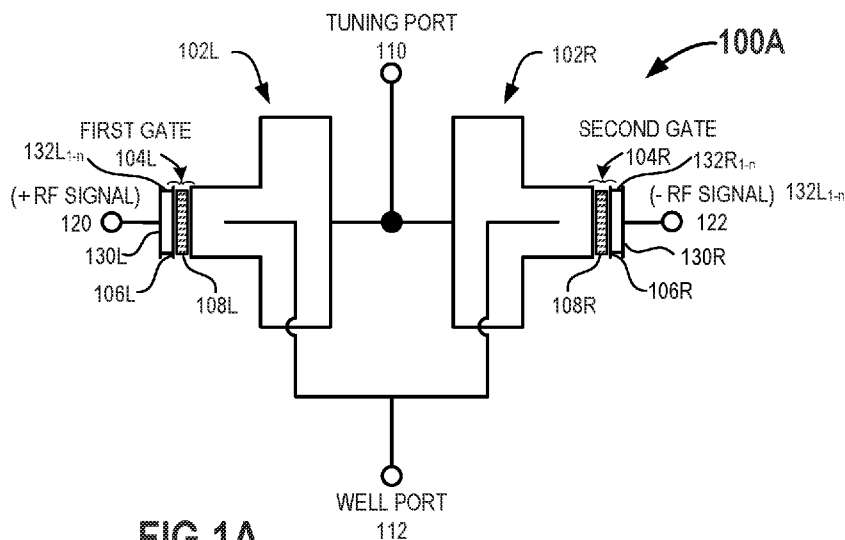


FIG 1A

(Inversion Type Differential Varactor)

(57) Abstract: A differential varactor includes a first MOS varactor conductively coupled to a second MOS varactor. A tuning port that receives a biasing or tuning voltage may be coupled to the drain junction and source junctions of the first varactor and the second varactor. Some of the drain junctions of the first varactor are merged with some of the source junctions of the second varactor. The first varactor includes a bridge conductor that is running above and parallel to the gate stack and couples both ends of the gate conductor associated with the first varactor. The second varactor includes a second bridge conductor that is running above and parallel to the gate stack and couples both ends of the gate conductor associated with the second varactor. The first bridge conductor and the second bridge conductor may be patterned on two different metal layers in a multi-layer metal stack above a semiconductor substrate.

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DIFFERENTIAL VARACTOR FOR MM-WAVE APPLICATIONS

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TECHNICAL FIELD

5 The present disclosure relates to variable metal oxide (MOS) capacitor (varactor) in complementary metal oxide semiconductor (CMOS) technology.

BACKGROUND

Oscillators represent key building blocks for many wireless systems. Often, such
10 oscillators include tunable capacitors to facilitate frequency tuning. Such frequency tuning permits the generation of either frequency-modulated or phase-modulated signals used in many communication and radar systems. At millimeter wave frequencies (*e.g.*, 30 GHz to 300 GHz) there are challenges with respect to the design and implementation of variable capacitors (*i.e.*, varactors) used to tune mm-wave signals. First, the quality factor of a
15 capacitor degrades as the frequency increases which results in quality factors of less than 5 for metal oxide semiconductor (MOS) capacitors operating at frequencies in excess of 60 GHz. Additionally, at mm-wave frequencies, digital tuning in discrete steps requires very small changes in capacitance on the order of tens of atto-farads. Such small changes in capacitance are difficult to achieve with MOS capacitors which typically have high
20 capacitance per area. But MOS capacitors offer a very small variability (*i.e.* small global variations from wafer to wafer as well as small device to device mismatch variations within an integrated circuit) thanks to the well-controlled gate dielectric formation process which is an important feature for a precise stepwise (digital) capacitance tuning and thus, frequency tuning.

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BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of various embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals designate like parts, and in which:

30 FIG. 1A provides an electrical schematic of an illustrative inversion mode differential varactor that includes two series-coupled varactors (*i.e.*, variable capacitance capacitors using a voltage controlled semiconductor MOS capacitance) with gate terminals and a tuning terminal, in accordance with at least one embodiment of the present disclosure;

FIG. 1B provides an electrical schematic of an illustrative accumulation mode differential varactor that includes two series-coupled varactors (*i.e.*, variable capacitance capacitors using a voltage controlled semiconductor MOS capacitance) with gate terminals and a tuning terminal, in accordance with at least one embodiment of the present disclosure;

5 FIG. 2 provides a layout of an illustrative multi-gate finger differential varactor such as that depicted in FIGs 1A and 1B and in which the differential varactor system includes a first varactor and a second varactor having interleaved gates and bridge conductors coupled to the gates at a first end of the gate and an opposed second end of the gate, in accordance with at least one embodiment of the present disclosure;

10 FIG. 3A provides a plan view of an illustrative differential varactor arranged such that the gate conductors and conductively coupled bridge conductors are interleaved, in accordance with at least one embodiment of the present disclosure;

FIG. 3B provides a plan view of another illustrative differential varactor arranged such that the gate conductors and conductively coupled bridge conductors are not interleaved, in accordance with at least one embodiment of the present disclosure;

15 FIG. 3C provides a schematic of an illustrative differential varactor system connecting two differential varactors such as those depicted in FIGS 1A and 1B in parallel (e.g. NMOS inversion type differential varactor in parallel with PMOS inversion type or N-well accumulation type or P-well accumulation type differential varactor or PMOS inversion type differential varactor in parallel with NMOS inversion type or N-well accumulation type or P-well accumulation type differential varactor), in accordance with at least one embodiment of the present disclosure;

FIG. 3D provides schematic of an illustrative differential varactor system connecting two differential varactors such as those depicted in FIGS 1A and 1B in parallel, in accordance with at least one embodiment of the present disclosure;

25 FIG. 4A provides a plan view of an illustrative differential MOSFET formed using NMOS or PMOS semiconductor field effect transistors (MOSFET), in accordance with at least one embodiment of the present disclosure;

FIG. 4B provides a plan view of another illustrative MOSFET formed using a PMOS or NMOS metal oxide semiconductor field effect transistor (MOSFET) having 2 drains and one common source, in accordance with at least one embodiment of the present disclosure;

30 FIG. 4C provides a plan view of a illustrative MOSFET using NMOS or PMOS metal oxide semiconductor field effect transistor (MOSFET) with two source contacts and one shared drain contact, in accordance with at least one embodiment of the present disclosure;

FIG. 5A provides a plan view of an illustrative neutralized field effect transistor (FET) that includes two amplifying and two neutralizing FETs, in accordance with at least one embodiment of the present disclosure;

FIG. 5B provides a plan view of an illustrative inverter type amplifying circuit that includes an NMOS FET and a PMOS FET connected in series, in accordance with at least one embodiment of the present disclosure;

FIG. 6 provides a perspective view of an illustrative varactor such as that depicted in FIG 1 and FIG 2 and in which the differential varactor includes a first varactor and a second varactor having interleaved gates and bridge conductors coupled to the gates at a first end of the gate and an oppose second end of the gate, in accordance with at least one embodiment of the present disclosure;

FIG. 7A provides an electrical schematic that includes a differential varactor such as described in detail with regard to FIG 1A or FIG 1B coupled in series between two linear capacitors, in accordance with at least one embodiment of the present disclosure;

FIG. 7B provides an electrical schematic that includes a differential varactor bank that includes a number of individual differential varactors such as described in detail with regard to FIG 1A or FIG 1B coupled in series between two linear capacitors, in accordance with at least one embodiment of the present disclosure;

FIG 8 provides a layout of an illustrative varactor system such as that depicted in FIG 7B and in which each of the differential varactors includes a first varactor and a second varactor having interleaved gates and bridge conductors coupled to the gates at a first end of the gate and an opposed second end of the gate, in accordance with at least one embodiment of the present disclosure;

FIG 9 provides a graph depicting a quality factor of an illustrative differential varactor as a function of applied gate and tuning voltage at a frequency of 60 GHz, in accordance with at least one embodiment of the present disclosure;

FIG 10 provides a graph depicting a capacitance of an illustrative differential varactor as a function of applied gate and tuning voltage at a frequency of 1 GHz, in accordance with at least one embodiment of the present disclosure;

FIG. 11 provides a high-level block flow diagram of an illustrative method of forming a differential varactor, in accordance with at least one embodiment of the present disclosure; and

FIG. 12 provides a block diagram of an illustrative mobile electronic device in which a differential varactors may be used in one or more tuning circuit applications.

Although the following Detailed Description will proceed with reference being made to illustrative embodiments, many alternatives, modifications and variations thereof will be apparent to those skilled in the art.

5

DETAILED DESCRIPTION

The systems and methods disclosed herein provide a differential varactor having a quality factor (*i.e.*, a ratio of the reactance of the capacitor to the resistance of the capacitor at a given frequency) in excess of 9 when operated at frequencies of 60 GHz or greater with an appropriate tuning range. The apparatuses, systems, and methods described herein

10 beneficially provide a reduction of the capacitance change per gatefinger to allow small changes in capacitance while having large enough area for providing a good matching (*i.e.* small mismatch variations) and so small capacitance (per area) variations of individual varactors in a bank of varactors which are beneficial in the operation of digital tuned oscillators in the millimeter wave frequency range while maintaining a large bandwidth, an

15 advantage of systems operated in the millimeter wave region. Furthermore, the apparatuses, systems, and methods described herein beneficially reduce or even eliminate conversion of low frequency amplitude noise into oscillator phase noise.

MOS (Metal-Oxide-Semiconductor) varactors consist in general of a gate conductor above a gate dielectric which is above a semiconductor substrate or a well in a semiconductor

20 substrate. The stack consisting of the gate conductor and gate dielectric above a semiconductor will be further denoted as gate stack. There are basically two types of MOS varactors, inversion mode varactors and accumulation mode varactors. Inversion mode varactors use field effect transistors (FET) to promote the formation of a charged inversion layer (*i.e.* electrons in case of NMOS devices, or holes in case of PMOS devices) for varying

25 the capacitance of the device. NMOS varactors use NFET gate stacks above a p-type doped semiconductor substrate or p-well and PMOS varactors use PFET gate stacks above a n-type doped semiconductor substrate or N-well. The p-well of an NMOS varactor can be placed inside an N-well in p-type semiconductor substrate.

Accumulation mode varactors use the formation of accumulation charges in a

30 semiconductor for a changing a capacitance (*i.e.* electrons in n-type substrate or n-well or holes in p-type substrate or p-well). Accumulation varactors may use NFET gate stacks over n-type doped semiconductor substrates or wells (N-well) and PFET gate stacks over p-type

doped semiconductor substrates or wells (P-well). n-type dopants are in silicon e.g. P, As, Sb and p-type dopants are B and In.

Inversion mode varactors typically contain three basic terminals. A first terminal may be coupled to the gate conductor(s), a second terminal may be coupled to the source/drain
 5 P/N-junctions and a third terminal may be coupled to the well (or semiconductor substrate) wherein the P/N-junctions are formed. Frequently, the gate conductor(s) and the source/drain P/N-junctions may be positioned nearby and parallel to each other.

An accumulation varactor contains only two terminals (while neglecting the well to substrate or to other well P/N-junction diode, which impacts the tuning port capacitive
 10 loading but maybe not the capacitance of the differential varactor under balanced excitation seen between the two gate terminals). A first terminal may be coupled to the gate conductor(s) and a second terminal may be coupled to the ohmic well contacts. Frequently, the gate conductor(s) and the ohmic well contacts may be positioned nearby and parallel to each other. The gate conductors may be connected via a gate terminal/port and the
 15 source/drain P/N-junctions (in case of inversion mode varactors) or the ohmic well contacts (in case of accumulation mode varactors) are connected via a tuning terminal/port to a circuit.

The P/N-junctions and the ohmic well contacts may contain silicided regions. These silicided regions may be connected via metal contacts (e.g. tungsten) to the metallization above providing the access terminal for the integrated circuit. The gate dielectric can be
 20 silicon oxide, nitrided silicon oxide or a high-k material (i.e. dielectric with a dielectric constant larger than 3.9 of silicon oxide) like hafnium oxide. Gate dielectrics maybe formed in at least two or more thicknesses to support devices for different supply voltages. The dielectric thickness used for the smallest supply voltage will be denoted as a thin-oxide/dielectric whereas a gate dielectric with a thickness larger as the thickness of the thin-oxide/dielectric version will be denoted as a thick-oxide/dielectric device which supports a
 25 higher supply voltage as the ones for thin-oxide/dielectric devices. The gate conductor material can be a poly silicon, a doped poly silicon, a silicided poly silicon, a silicided doped poly silicon, a silicide or a metal like TiN which is used in high-k metal gate technology.

For a MOSFET or MOS varactor there is a relation between the geometry of the
 30 channel, i.e. the semiconductor part under the gate conductor, containing inversion type or accumulation type charges, and the geometry of the gate conductor. The distance between source/drain contacts or ohmic well contacts separated by the gate conductor is related to the channel length of the inversion or accumulation channel which corresponds to the gate conductor width. The gate conductor length above the semiconductor relates to the channel

width. The resistance of the gate conductor and the channel add to a total resistance of the varactor. This total resistance impacts the quality factor of the varactor. A large channel width leads to a small channel resistance but maybe a larger gate conductor resistance as the gate conductor length and area increases. A small channel length leads to a reduced channel resistance but an increased gate conductor resistance as the width and area of the gate conductor is reduced. For a thick (gate) oxide/dielectric MOS varactor one may use shorter channel lengths compliant with a lower supply voltage compared to the larger one allowed for the gate to tuning voltage of thick oxide/dielectric MOS capacitors as the drain to source voltage is very small in a varactor due to the conductively connected (shorted) drain and source regions. A reduced channel length allows to reduce the channel resistance contribution and so maybe improve the quality factor of the varactor. The gate to tuning voltage range is not reduced by using shorter channel lengths as the gate to tuning voltage range depends only on the gate dielectric thickness and the associated breakdown voltage of the gate dielectric. The source/drain P/N-junctions or ohmic well contacts may include a silicide selected from the group of Titanium Silicide (TiSi), Cobalt Silicide (CoSi, CoSi₂), Nickel Silicide (NiSi, NiSi₂), Platinum silicide or Nickel-Platinum silicide or combinations thereof. The silicided regions of the semiconductor as well as the gate conductors are connected to the metallization above the gate conductor and silicided semiconductor regions thru contacts (e.g. usually tungsten but maybe also copper might be used). Contacts to the gate conductor are formed usually on gate conductor parts not overlapping with a gate dielectric and semiconductor below but running above a shallow trench isolation (STI) region of a bulk semiconductor technology or the combination of trench isolation and buried oxide (BOX) of a SOI technology for reliability reasons. Contacts to the gate conductor maybe formed also in areas where the gate conductor runs above the gate dielectric and semiconductor. The different metal layers of the technology (e.g. copper) are connected thru vias (e.g. copper). The varactors can be formed in a bulk semiconductor substrate where devices are isolated from each other via a shallow trench isolation (STI) or in a semiconductor on insulator (SOI) technology, which could be a partially depleted SOI or a fully depleted ultrathin body SOI technology. The STI is a hole/area formed in the semiconductor and filled with a dielectric (silicon-oxide in silicon technology) to electrical isolate different devices formed in the same bulk semiconductor substrate. A SOI technology utilizes a semiconductor substrate which contains a thinner layer of active semiconductor material wherein semiconductor devices are formed disposed above a dielectric named buried oxide (BOX → silicon oxide for silicon technology, but could be also sapphire, diamond etc.) which is disposed above a bulk

substrate material (which may be silicon in case of silicon technology). The semiconductors to be used can be silicon, germanium, silicon-germanium (SiGe), GaAs, GaN, InN, AlN, InP, InSb. Semiconductors like GaAs, GaN, InN, AlN, InP, InSb may be formed above a silicon substrate. The device geometry can be planar or three-dimensional like e.g. Fin based devices (like e.g. FinFETs).

A differential varactor is generated by at least two basic varactors by connecting the source/drain P/N-junctions (in case of inversion mode varactors) or the ohmic well contacts (in case of accumulation mode varactors) of the varactors forming the differential varactor together. These connected source/drain P/N-junctions or ohmic well contacts form the tuning port. The radio frequency alternating current flows from one gate to the other gate, *i.e.* the tuning port maybe connected via a high impedance or a low impedance to a tuning voltage source.

In a differential mode excitation applied to the first and the second gate terminals of the differential varactor the tuning port might form a virtual ground where no radio frequency alternating current exits. The gate voltage and tuning voltage determine the capacitance value of the varactor. The source/drain P/N-junctions or ohmic well contacts of both varactors can be connected via the metallization of the technology, or in a more compact and higher performance arrangement the silicided regions of the source/drain P/N-junctions or ohmic well contacts of the first and second varactor can be merged/shared (except the two most outer ones which have not a neighbor to merge with), so that no metallization is needed to transport the radio frequency alternating current from the first varactor to the second varactor as the radio frequency alternating current runs directly thru the silicided P/N-junction or ohmic well contact regions from the first varactor to the second varactor (except for the most outer P/N-junctions or ohmic well contacts which could require a metal bridge to the other P/N-junctions or ohmic well contacts if the outer P/N-junctions or ohmic well contacts should be connected to the other pn-junctions or other ohmic well contacts). The merging of the silicided source/drain or ohmic well contact regions is reducing the resistance of the differential varactor and in this way increases the quality factor (Q-factor) of the differential varactor.

The apparatuses, systems, and methods disclosed herein provide differential varactors having a gate conductor contacted at both sides/ends via a metal bridge running parallel to the gate conductor above the gate stack. Contacting both sides/ends of the gate conductor beneficially improves the quality factor of the differential varactor. Metal bridges in adjacent gate fingers may be patterned on different metal levels to advantageously improve the tuning

range and permit the use of physically smaller varactors, thereby beneficially improving the overall performance of the oscillator.

A metal oxide semiconductor (MOS) differential varactor is provided. The MOS differential varactor may include a first MOS varactor and a second MOS varactor
5 conductively coupled to a common tuning port. The first MOS varactor may include a first tuning port; a first gate conductor having a first end and a second end opposite the first end formed in a first conductive material layer of a multi-layer semiconductor; a first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; and a plurality of conductive structures
10 electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations. The second MOS varactor may include a second tuning port conductively coupled to the first tuning port; a second gate conductor having a first end and a second end opposite the first end formed in the first conductive material layer of the multi-layer semiconductor; a second bridge conductor having a first end and a second
15 end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

A metal oxide semiconductor (MOS) differential varactor system is provided. The
20 MOS differential varactor system may include a plurality of MOS differential varactors, each of the plurality of MOS differential varactors including a first MOS varactor and a second MOS varactor. The first MOS varactor in each of the plurality of MOS differential varactors may include: a first gate conductor having a first end and a second end opposite the first end formed in a first conductive material layer of a multi-layer semiconductor; a first bridge
25 conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; and a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations. The second MOS varactor in each of the plurality of MOS differential varactors may include: a second gate conductor having a first end and a
30 second end opposite the first end formed in the first conductive material layer of the multi-layer semiconductor; a second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

Further, the second gate conductor and the second bridge conductor included in each of the plurality of differential varactors forms an interleaved pattern with the first gate conductor and the first bridge connector included in each of the plurality of differential varactors.

A method of fabricating a metal oxide semiconductor (MOS) differential varactor is provided. The fabrication method may include forming a first tuning port of a first MOS varactor on a semiconductor substrate; forming a first gate conductor of the first MOS varactor in a first conductive material layer of a multi-layer semiconductor, the first gate conductor having a first end and a second end opposite the first end; forming a first bridge conductor of the first MOS varactor, the first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; forming a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations; forming a second tuning port of a second MOS varactor conductively coupled to the first tuning port of the first MOS varactor; forming a second gate conductor of the second MOS varactor in the first conductive material layer of the multi-layer semiconductor, the second gate conductor having a first end and a second end opposite the first end; forming a second bridge conductor of the second MOS varactor, the second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and forming a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

A metal oxide semiconductor (MOS) differential varactor fabrication system is provided. The MOS differential varactor fabrication system may include a means for forming a first tuning port of a first MOS varactor on a semiconductor substrate; a means for forming a first gate conductor of the first MOS varactor in a first conductive material layer of a multi-layer semiconductor, the first gate conductor having a first end and a second end opposite the first end; a means for forming a first bridge conductor of the first MOS varactor, the first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; a means for forming a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations; a means for forming a second tuning port of a second MOS varactor conductively coupled to the first tuning port of the first MOS varactor; a means for forming a second gate conductor of the second MOS varactor in the first conductive material layer of the multi-layer semiconductor,

the second gate conductor having a first end and a second end opposite the first end; a means for forming a second bridge conductor of the second MOS varactor, the second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a means for forming a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

As used herein, the terms “top,” “bottom,” “up,” “down,” “upward,” “downward,” “upwardly,” “downwardly” and similar directional terms should be understood in their relative and not absolute sense. Thus, a component described as being “upwardly displaced” may be considered “laterally displaced” if the device carrying the component is rotated 90 degrees and may be considered “downwardly displaced” if the device carrying the component is inverted. Such implementations should be considered as included within the scope of the present disclosure.

As used in this specification and the appended claims, the singular forms “a,” “an,” and “the” include plural referents unless the content clearly dictates otherwise. It should also be noted that the term “or” is generally employed in its sense including “and/or” unless the content clearly dictates otherwise.

FIG 1A depicts an illustrative inversion mode differential varactor 100A that includes two interconnected metal-oxide semiconductor (MOS) varactors 102L and 102R (collectively “varactors 102”) and FIG 1B depicts an illustrative accumulation mode differential varactor 100B (collectively “differential varactor 100”) that includes two interconnected MOS varactors 102L and 102R (collectively, “MOS varactors 102”), in accordance with at least one embodiment of the present disclosure. Each of the MOS varactors 102L and 102R includes a respective “gate” or “gate stack” 104L, 104R (collectively, “gate stacks 104”). Each gate stack 104L, 104R includes at least a respective gate conductor 106L, 106R (collectively, “gate conductors 106”) disposed above and/or proximate a respective gate dielectric 108L, 108R (collectively “gate dielectrics 108”). Each gate stack 104L, 104R may be disposed, formed, or patterned above a semiconductor substrate or a well in a semiconductor substrate. Each gate stack 104 may include at least one bridge conductor 130L, 130R (collectively, “bridge conductor 130”). A plurality of conductive structures 132L_{1-n}, 132R_{1-n} (collectively “conductive structures 132”) may be electrically couple the bridge conductor 130 to the gate conductor 106 at a respective plurality of locations. In embodiments, the bridge conductor 130 for each gate stack 104 may be disposed parallel to the respective gate conductor 106. In embodiments, the bridge conductor 130 for a respective

gate stack 104 may be disposed in a structural layer above the respective gate conductor 106. For each MOS varactor 102, source and drain pn-junction regions may be formed in the substrate as described in detail below for inversion mode differential varactors 100A and ohmic contacts for accumulation mode differential varactors 100B.

5 Differential varactors 100 may be formed using at least two inversion mode or accumulation mode varactors 102. By connecting the source/drain P/N-junctions (in case of inversion mode varactors such as depicted in FIG 1A) or the ohmic well contacts (in case of accumulation mode varactors such as depicted in FIG 1B) of the varactors together, a differential varactor is formed. These connected source/drain P/N-junctions (inversion mode) or ohmic well (accumulation mode) contacts form the tuning port 110. A radio frequency (RF) or millimeter-wave (mm-wave) alternating current may pass from a gate conductor 106L of a first varactor 102L to a gate conductor 106R of a second varactor 102R, *i.e.* the tuning port 110 maybe connected via a high impedance or a low impedance connection to a tuning voltage source.

15 The illustrative inversion type differential varactor 100A depicted in FIG 1A includes two series-coupled inversion type varactors 102L and 102R (collectively, “inversion type varactors 102”), in accordance with at least one embodiment of the present disclosure. In some embodiments, each of the inversion type varactors 102 forming inversion type differential varactor 100A may include an NMOS device that includes n^+ -doped source and drain regions and an silicided n^+ -doped polysilicon gate or metal gate, each disposed in a substrate or well that is opposite doped (*i.e.*, p^- -doped). In other embodiments, each of the inversion type varactors 102L and 102R forming inversion type differential varactor 100A may include a PMOS device that includes p^+ -doped source and drain regions and a silicided p^+ -doped polysilicon gate or metal gate, each disposed in a substrate or well that is opposite doped (*i.e.*, n^- -doped).

Each of the inversion type varactors 102 forming inversion mode differential varactor 100A may be considered a three-terminal device. The source and drain regions of each of the inversion type varactors 102 forming the inversion mode differential varactor 100A may be shorted together to provide a first terminal or tuning port 110 to receive a tuning signal or voltage; the substrate or well containing each of the inversion type varactors 102 may be coupled to a second terminal, and a third terminal may be coupled to the gate stack 104 of the inversion type varactor 102.

As depicted in FIG 1A, the shorted source/drain terminals from each of inversion type varactors 102R and 102L may be coupled together to provide the tuning port 110. Also as

depicted in FIG 1A, the well port terminals from each of inversion type varactors 102R and 102L may be coupled together to provide the well port 112. Further, a radio frequency or mm-wave alternating current 120 may be input to the differential varactor 100A at the (*i.e.*, first) gate conductor 106L of the first inversion type varactor 102L and may be output 122 by the differential varactor 100A at the (*i.e.*, second) gate conductor 106R of the second inversion type varactor 102R.

In embodiments, inversion type differential varactors 100A such as that depicted in FIG 1A may use like field-effect transistors (FET) the formation of a charge inversion layer (*i.e.* electrons in case of NMOS devices, or holes in case of PMOS devices) for altering, adjusting, or changing a capacitance. In embodiments, inversion mode NMOS varactors may use NFET gate stacks above a p-type doped semiconductor substrate or p-well. In yet other embodiments, inversion mode PMOS varactors may use PFET gate stacks above a n-type doped semiconductor substrate or n-well. The p-well of an NMOS varactor can be placed inside an n-well in p-type semiconductor substrate.

FIG. 1B depicts an illustrative accumulation type differential varactor 100B that includes a first varactor 102L coupled in series with a second varactor 102R. Each of the accumulation type varactors 102L and 102R depicted in FIG 1B may include two terminals or connections: a first terminal which may be coupled to the gate conductor(s) 106; and a second terminal which may be coupled to the ohmic well contacts. Frequently, the gate conductor(s) 106L, 106R and the ohmic well contacts may be positioned nearby and parallel to each other. The gate conductors 106L, 106R may be connected via a gate terminal/port and the ohmic well contacts are connected via a tuning terminal/port to a one or more circuits external to the accumulation type differential varactor 100B.

The illustrative accumulation type differential varactor 100B depicted in FIG 1B also includes two series-coupled accumulation type varactors 102L and 102R (collectively “accumulation type varactors 102”), in accordance with at least one embodiment of the present disclosure. In some embodiments, each of the accumulation type varactors 102 forming the accumulation type differential varactor 100B may include an N-type (conduction) device that includes silicided n⁺-doped ohmic contact regions and an silicided n⁺-doped polysilicon gate or metal gate, each disposed in a substrate or well that is similarly doped (*i.e.*, n⁻-doped). Each of the accumulation type varactors 102 forming the accumulation mode differential varactor 100B may be considered a two-terminal device (*e.g.*, if neglecting the N-well to P-substrate or generally well to well P/N-junction the tuning port is loaded with). The ohmic contact regions of each of the accumulation type varactors 102

forming the accumulation mode differential varactor 100B may be shorted together to provide a first terminal that receives the tuning voltage and a second terminal may be coupled to the gate conductor 106 of the accumulation type varactor 102. As depicted in FIG 1B, the shorted ohmic contact terminals from each of accumulation type varactors 102R and 102L may be coupled together to provide the tuning port 110. Also as depicted in FIG 1B, a radio frequency (RF) or mm-wave alternating current 120 may be input to the accumulation mode differential varactor 100B at the (*i.e.*, first) gate contact 106L of the accumulation type varactor 102L and may be output by the differential varactor 100A at the (*i.e.*, second) gate contact 106R of the accumulation type varactor 102R.

The pn-junctions of the inversion type varactors 102 used in the inversion type differential varactor 100A and the ohmic well contacts of the accumulation type varactors 102 used in the accumulation type differential varactor 100B may include, in whole or in part, one or more silicided regions. The one or more silicided regions may be conductively coupled to or otherwise connected via metal contacts (*e.g.* tungsten contacts) to the metallization above providing the access terminal for the integrated circuit.

The gate dielectric 108 used in the inversion type differential varactor 100A and/or the accumulation type differential varactor 100B may include silicon oxide, nitrided silicon oxide, or a high-k material (*e.g.*, a material having a dielectric constant larger than 3.9 of silicon oxide) such as hafnium oxide. Gate dielectrics 108 used in the inversion type differential varactor 100A and/or the accumulation type differential varactor 100B may be formed in at least two or more thicknesses to support devices for different supply voltages. The dielectric thickness used for the smallest supply voltage may be referred to as a thin-oxide/dielectric whereas a gate dielectric with a thickness larger as the thickness of the thin-oxide/dielectric version may be referred to as a thick-oxide/dielectric device which supports a higher supply voltage as the ones for thin-oxide/dielectric devices.

The gate conductor 106 used in the inversion type differential varactor 100A and/or the accumulation type differential varactor 100B may include materials such as: poly silicon, doped poly silicon, silicided poly silicon, silicided doped poly silicon, silicide, or a metal and/or metallic alloy like TiN which is used in high-k metal gate technology. The source/drain P/N-junctions used in the inversion type differential varactor 100A and/or ohmic well contacts used in the accumulation type differential varactor 100B may include a silicide selected from the group of Titanium Silicide (TiSi, TiSi₂), Cobalt Silicide (CoSi, CoSi₂), Nickel Silicide (NiSi, NiSi₂, Ni₂Si, Ni₃Si, Ni₃₁Si₁₂), Platinum Silicide or Nickel-Platinum Silicide or combinations thereof.

The inversion type differential varactor 100A and the accumulation type differential varactor 100B may be formed in, on, or about a bulk semiconductor substrate where devices, including the differential varactors 102, may be electrically and/or physically isolated from each other via a shallow trench isolation (STI) or in a semiconductor on insulator (SOI) technology, which could be a partially depleted SOI or a fully depleted ultrathin body SOI technology. The semiconductors used to provide some or all of the differential varactors 100 may include silicon, germanium, silicon-germanium (SiGe), GaAs, GaN, InN, AlN, InP, InSb. Semiconductors like GaAs, GaN, InN, AlN, InP, InSb may be formed/disposed above a silicon substrate. The device geometry used in the inversion mode differential varactor 100A and/or the accumulation mode differential varactor 100B may be planar or three-dimensional (*e.g.* Fin based devices such as FinFETs).

When an excitation voltage is applied to the differential varactor 100 the tuning port 110 may form a virtual ground where no RF or mm-wave alternating current exits. The gate voltage and tuning voltage determine the capacitance value of the varactor. The source/drain pn-junctions of the inversion mode differential varactor 102A and/or the ohmic well contacts the accumulation mode differential varactor 102B may be connected via one or more metal layers. Additionally or alternatively, the source/drain pn-junctions of the inversion mode differential varactor 102A and/or the ohmic well contacts the accumulation mode differential varactor 102B may be connected in a more compact and higher performance arrangement the silicided regions of the source/drain pn-junctions of the inversion mode differential varactor 102A or the ohmic well contacts of the accumulation mode differential varactor 102B may be merged/shared, so that no metallization is needed to transport the RF or mm-wave alternating current from the first varactor 102L to the second varactor 102R as the RF or mm-wave alternating current runs directly thru the silicided pn-junction or ohmic well contact regions from the first varactor to the second varactor. The merging of the silicided source/drain pn-junctions of the inversion mode differential varactor 100A or the ohmic well contact regions of the accumulation mode differential varactor beneficially reduces the resistance of the respective differential varactor 100 and advantageously increases the quality factor (Q-factor) of the differential varactor.

In some implementations, either or both of the varactors 102L and 102R may include a thick metal oxide semiconductor (MOS) device having a gate dielectric 108 thickness of: about 2 nanometers (nm) or more (the thickness value is an equivalent electric thickness of SiO₂, *i.e.* a gate dielectric 108 with a different dielectric constant and a different thickness but generating the same capacitance per area as SiO₂ of this thickness); about 3nm or more; about

4 nm or more; about 5nm or more; about 6nm or more; or about 7nm or more. The use of a thick oxide MOS semiconductor devices in forming the varactors 102L and 102R beneficially increases the quality factor of the varactors 102 and reduces the capacitance change per gate stack 104L, 104R. The use of two thick-oxide MOS varactors 102 connected in series may be
5 provides a voltage range that matches to the amplitude of an oscillator with a negative gm-stage constructed using high-gain, thin-oxide NMOS transistors, *i.e.* twice the supply voltage V_{dd} of the thin-oxide device. The tuning range of the varactors 102L and 102R may be reduced for digital tuning applications while the quality factor (“Q”) may be enhanced and conversion of low-frequency amplitude noise into oscillator phase noise may be reduced or
10 even eliminated by connecting linear capacitors in series with both gate signal ports of the differential varactor 100.

In some implementations either or both of the gate conductors 106L and 106R may be conductively coupled to one or more external voltage sources. In embodiments, an external voltage source 120 may be conductively coupled at a plurality of locations to the electrically
15 conductive gate conductor 106L, 106R. In such implementations, a plurality of bridge conductors 130 may conductively couple the external voltage source 120 to the gate conductor 106 using a plurality of conductive structures 132. Each of the plurality of conductive structures 132 may include any number, type, and/or combination of electrically conductive contacts, vias and/or metal layers or similar electrically conductive devices,
20 fixtures, appurtenances, members, or similar.

The bridge conductors 130 may be disposed parallel to the respective gate conductor 106 to which the bridge conductor 130 is electrically conductively coupled. In embodiments, the bridge conductor 130 may be disposed in a conductive material (*e.g.*, metal, silicide, or similar) formed above the respective gate conductor 106 to which the bridge conductor is
25 electrically conductively coupled. In embodiments, the bridge conductors 130 may electrically conductively couple the RF signal/voltage source 120 to the gate conductor 106 using conductive structures 132 disposed at or about opposite ends of the bridge conductor 130 and gate conductor 106 such that the RF signal/external voltage 120 may be supplied or otherwise applied generally more evenly/symmetrically across the gate conductor 106 and
30 hence, across the gate stack 104. In embodiments, a first conductive structure 132₁ may conductively couple the first end of the bridge conductor 130 to the first end of the respective gate conductor 106 and a second conductive structure 132₂ may conductively couple the second end of the bridge conductor 130 to the second end of the respective gate conductor 106. Providing a plurality of electrical couplings to the gate conductor 106 beneficially

improves the quality factor of the differential varactor 100. In embodiments, quality factors in excess of 9 at frequencies in excess of 60 GHz may be provided as a result of the bridge structure and multiple conductive couplings between the bridge conductor and the gate conductor 106.

5 FIG. 2 provides a layout of a multi-gate finger differential varactor 200 that includes a plurality of inversion mode differential varactors 100 arranged such that the gate stacks 104L of each of a plurality of first varactors 102L physically interleave with the gate stacks 104R of each of a plurality of second varactors 102R in each of the differential varactors 100 to form the multi gatefinger differential varactor 200 depicted in FIG 2, in accordance with at
10 least one embodiment of the present disclosure.

 In operation, one or more bias or tuning voltages (*e.g.*, a DC voltage, but also including dynamically changing voltages and digital switching voltages which switch between a number of values) may be applied or otherwise supplied to the tuning port 110. Application of the bias or tuning voltage to the tuning port 110 changes the capacitance of
15 each of the differential varactors 100A-100n which permits the multi-gate finger differential varactor 200 to provide a desired capacitance value, thereby allowing the use of the multi-gate finger differential varactor 200 in applications in which fine tuning achieved by small changes in capacitance of the multi-gate finger differential varactor 200 is desirable. Some or all of the differential varactors 100A-100n included in the multi-gate finger differential
20 varactor 200 may receive a tuning signal that alters, adjusts, or otherwise controls the capacitance of the multi-gate finger differential varactor 200.

 In embodiments, the tuning signal may be conductively coupled to the tuning port 110 of the varactors 102L and 102R via a conductive structure 210A-210n (collectively, “conductive structure 210”). Each of the conductive structures 210 may conductively couple
25 the tuning port 110 to the silicon substrate 220 in/on which the gate stacks 104L and 104R are formed. In embodiments, the conductive structure 210 may include any number and/or combination of conductive elements such as contacts, vias and/or metal layers. In embodiments, the tuning port 110 may be patterned, formed, or otherwise deposited in, on, or about a first conductive layer in a multi-layer semiconductor structure (*note*: the use of the
30 term “first conductive layer” is intended as a unique identifier for a conductive layer in the multi-layer semiconductor structure and should not be interpreted as specifically denoting metal layer 1 (or M1), in the multi-layer semiconductor structure).

 In embodiments, each of the first varactors 102L_A-102L_n includes a corresponding bridge conductor 130L_A-130L_n (collectively, “bridge conductor 130L”) formed on a second

conductive layer in the multi-layer semiconductor structure (*note*: the use of the term “second conductive layer” is intended as a unique identifier for a conductive layer in the multi-layer semiconductor structure and should not be interpreted as specifically denoting metal layer 2 (or M2), in the multi-layer semiconductor structure). Each bridge conductor 130L_A-130L_n conductively couples to a respective gate access line 202A-202n at a plurality of locations. A plurality of first conductive structures 132L_A electrically conductively couple each respective one of the plurality of bridge conductors 130L_A-130L_n to a first location (*e.g.*, a first end 224L_A-224L_n) of the respective gate conductor 106L_A-106L_n. A plurality of second conductive structures 132B electrically conductively couple each respective one of a plurality of bridge conductors 130L_A-130L_n to a second location (*e.g.*, a second end, 226L_A-226L_n) of the respective gate conductor 106L_A-106L_n.

In embodiments, each of the second varactors 102R_A-102R_n includes a corresponding bridge conductor 130R_A-130R_n formed on a third conductive layer in the multi-layer semiconductor structure (*note*: the use of the term “third conductive layer” is intended as a unique identifier for a conductive layer in the multi-layer semiconductor structure and should not be interpreted as only denoting metal layer 3 (or M3) in the multi-layer semiconductor structure). Each bridge conductor 130R_A-130R_n conductively couples to a respective gate access line 212A-212n at a plurality of locations. A plurality of first conductive structures 132A₁-132A_n electrically conductively couple each respective one of the plurality bridge conductors 130R_A-130R_n to a first location (*e.g.*, a first end, 224R_A-224R_n) of the respective gate conductor 106R_A-106R_n. A plurality of second conductive structures 132B₁-132B_n electrically conductively couple each respective one of the plurality of bridge conductors 130R_A-130R_n to a second location (*e.g.*, a second end, 226R_A-226R_n) of the respective gate conductor 106R_A-106R_n.

In some implementations the bridge conductors 130L_A-130L_n may be formed, patterned, or otherwise deposited as a conductive layer different from the conductive layer that includes bridge conductors 130R_A-130R_n. Thus, in some implementations, the bridge conductors 130L and 130R may be formed on different layers in an alternating/interleaved manner. Similarly, gate access lines 202A-202n may be formed, patterned, or otherwise deposited as metal layer different from the metal layer containing gate access lines 212A-212n. In other implementations the gate access lines 202A-202n and 212A-212n are formed in the same layer.

As depicted in FIG 2, the merged source and drain regions of the varactors 102L and 102R may be formed in, on, about, or above a silicided portion 232 of the semiconductor

substrate 220. As depicted in FIG 2, the first ends 224L, 224R and the second ends 226L, 226R of gate conductors 106L, 106R may be disposed in, on, about, or above a shallow trench isolation (“STI”) region 230 formed in the semiconductor substrate 220. As depicted in FIG 2 the well port 112 of each varactor 102 may include one or more conductive (*e.g.*, tungsten) contacts 234 disposed in, on, about, or above a silicided portion 236 of the semiconductor substrate 220.

FIG 3A provides a plan view of an illustrative a multi-gate finger differential varactor 300A that includes two differential varactors 102A, 102B in which the gate port for a first varactor 104L_A, 104L_B in each differential varactor 102 and the gate port for the second varactor 104R_A, 104R_B in each differential varactor 102 are interleaved and conductively coupled on opposing sides of the multi-gate finger differential varactor 300A and bridge conductors 130 are disposed parallel to each of the gate structures 104 such that the voltage is distributed across the gate conductor 106 of each varactor 104, in accordance with at least one embodiment of the present disclosure. The physical configuration of the multi-gate finger differential varactor 300A depicted in FIG 3A beneficially minimizes the footprint of the multi-gate finger differential varactor 300A.

In some implementations, a shallow trench isolation (STI) region 302 may be disposed at least partially about the exterior periphery of the multi-gate finger differential varactor 300A. In silicon-on-insulator (SOI) implementations, a trench isolation above a buried oxide (BOX) region 302 may be disposed at least partially about the exterior or periphery of the multi-gate finger differential varactor 300A. In such embodiments, the region at least partially surrounded or otherwise bounded by the STI/BOX region 302 may at least partially include a silicide layer disposed on the semiconductor substrate 220.

As depicted in FIG 3A, one or more conductive structures (132L_{A1}, 132L_{B1}, 132R_{A1}, 132R_{B1}) may conductively couple a first end of each of the bridge conductors 130 to a first end of a respective gate conductor 106 above the STI/BOX region 302. Also as depicted in FIG 3A, one or more second conductive structures (132L_{A2}, 132L_{B2}, 132R_{A2}, 132R_{B2}) may conductively couple a second end of each of the gate conductors 106 to a second end of a respective gate conductor 106 above the STI/BOX region 302.

The multi-gate finger differential varactor 300A includes an isolated source region 306 and an isolated drain region 308. In embodiments, the multi-gate finger differential varactor 300A may also include a number of shared source/drain PN-junctions 310 conductively coupled to a silicided region on the semiconductor substrate. In embodiments, the multi-gate finger differential varactor 300A may also include a number of shared

source/drain PN-junctions 310 conductively coupled to a silicided region on the semiconductor substrate 220.

As depicted in FIG 3A, each of the bridge conductors 130 are disposed parallel to the respective gate conductor 106 to which the bridge conductor 130 is attached. In
5 embodiments, a plurality of conductive structures 132 may conductively couple the bridge conductors 130 to the gate conductors 106 at a plurality of locations, such as the first end of the bridge conductor 130/ gate conductor 106 and the second end of the bridge conductor 130/gate conductor 106. In embodiments, each bridge conductor 130 may be disposed generally parallel to the gate conductor 106 to which it is conductively coupled – such a
10 parallel conductor arrangement advantageously reduced the resistance of the gate structure 106, beneficially improving the quality or “Q-factor” of the multi-gate finger differential varactor 300A over prior devices.

FIG 3B provides a plan view of an illustrative a multi-finger differential varactor 300B that includes two varactors 102A, 102B in which the gate stack for a first varactor
15 104A_L, 104 A_R in each varactor 102 and the gate stack for the second varactor 104B_L, 104B_R in each varactor 102 are not interleaved but still conductively coupled on opposing sides of the multi-gate finger differential varactor 300B by/thru/via bridge conductors 130 which are disposed parallel to each of the gate structures 104 such that the voltage is distributed across the gate conductor 106 of each gate stack 104 in each varactor, in accordance with at least
20 one embodiment of the present disclosure.

As depicted in FIG 3B, the bridge conductors 130A_L, 130A_R, 130B_L, and 130B_R may extend above an STI/BOX region 302. Also as depicted in FIG 3B, the gate conductors 106A_L, 106A_R, 106B_L, and 106B_R may also extend above an STI/BOX region 302. One or more conductive structures 132 may electrically conductively couple each bridge conductor
25 130 to a respective gate conductor 106. In some implementations, the one or more conductive structures 132A_{L1}, 132A_{R1}, 132B_{L1}, and 132B_{R1} may conductively couple the first end of each bridge conductor 130A_L, 130A_R, 130B_L, and 130B_R to a first end of a respective gate conductor 106A_L, 106A_R, 106B_L, and 106B_R. In some implementations, one or more conductive structures 132A_{L2}, 132A_{R2}, 132B_{L2}, and 132B_{R2} may conductively couple a
30 second end of each bridge conductor 130A_L, 130A_R, 130B_L, and 130B_R to a second end of a respective gate conductor 106A_L, 106A_R, 106B_L, and 106B_R.

FIG 3C provides a schematic of an illustrative differential varactor system 300C formed using a first pair of differential varactors 102L_A and 102R_A (collectively “first differential varactor 330”) of multi-finger varactors 100A depicted in FIG 1A or multi-finger

differential varactors 100B depicted in FIG 1B connected in electrical parallel with a second pair of differential varactors 102L_B, 102R_B (collectively “second differential varactor 340”) of multi-finger differential varactors 100A depicted in FIG 1A or multi-finger differential varactors 100B depicted in FIG 1B in accordance with at least one embodiment of the present disclosure. In some embodiments, the first differential varactor 330 may include at least two NMOS or at least two PMOS inversion type varactors arranged as in FIG 1A and the second differential varactor 340 may include at least two N-well or at least two P-well accumulation type varactors arranged as in FIG 1B. In other embodiments, the first differential varactor 330 may include at least two NMOS inversion type or at least two PMOS inversion type varactors arranged as in FIG 1A and the second differential varactor 340 may include at least two PMOS inversion type or P-well accumulation type (each of one to be connected in parallel to the first NMOS inversion type differential varactor) or at least two N-well accumulation type or NMOS inversion type varactors (each of one to be connected in parallel with the first PMOS inversion type differential varactor) arranged as in either of FIGs 1A or 1B. Such a varactor system connecting NMOS or N-well varactors in parallel with PMOS or P-well varactors may form a device with a pulse shaped capacitance voltage characteristic that maybe used in a nonlinear transmission line (NLTL). A NLT is a transmission line or differential transmission line loaded periodically with varactors or differential varactors and maybe allow the generation of very short pulses or transitions in the time domain. Such NLTL benefit from a high Q-factor and large tuning range of the varactor.

FIG 3D provides a schematic of an illustrative differential varactor system 300D formed using a multi-finger differential varactors 102L_A and 102R_A (collectively “first differential varactor 360”), such as the multi-finger differential varactors 100A depicted in FIG 1A or multi-finger differential varactors 100B depicted in FIG 1B, connected in electrical parallel with multi-finger differential varactors 102L_B and 102R_B (collectively “second differential varactor 370”), such as the multi-finger differential varactors 100A depicted in FIG 1A or multi-finger differential varactors 100B depicted in FIG 1B, in accordance with at least one embodiment of the present disclosure. In some embodiments, the first differential varactor 360 may include at least two NMOS inversion or at least two N-well accumulation type varactors arranged as in either of FIGs 1A or 1B and the second differential varactor 370 may include at least two PMOS inversion or at least two P-well accumulation type varactors arranged as in either of FIGs 1A or 1B.

As depicted in FIG 3D, a common mode tuning voltage may be applied to the tuning port 110 of the switched resistive network 380. The switched resistive network 380 may then

use a number of switches and/or resistances provide differential tuning voltages 110A and 110B to the tuning port of the first differential varactor 360 and to tuning port of the second differential varactor 370, respectively. The switched resistive network 380 may include a number of mechanical, electromechanical, semiconductor, and/or electrical switching devices 322A-322n (collectively, “switching devices 322”). The switching devices 322 may be binary (*i.e.*, ON state or OFF state) devices but may also include devices able to switch continuously between two values of resistivity. The switched resistive network may further include a plurality of resistive elements 320A-320n (collectively, “resistive elements 320”) that may be used to provide a number of temporally discrete or temporally varying differential tuning voltages 110A and 110B.

The differential varactor system 300D depicted in FIG 3D beneficially shows a reduced change in capacitance when the common mode tuning voltage applied to the tuning port 110 is changed but a strong change of capacitance if a non-zero differential tuning voltage (*i.e.*, voltage applied at 110A minus voltage applied at tuning port 110B) is applied. Such may advantageously suppress noise in the common mode tuning voltage supply.

FIG 4A provides a schematic of an illustrative differential MOSFET 400A formed using bridge conductors 130L and 130R disposed parallel to and above gate conductors 106L and 106R, respectively thereby forming a MOS channel, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 4A, the differential MOSFET 400A may include a common source region 402, a first drain region 404L and a second drain region 404R (collectively, “drain regions 404”). Each of the source region 402 and the drain regions 404 may include a conductive structure 210 electrically conductively coupled to a silicided region 310 disposed on the semiconductor substrate 220. Drain terminals 406L and 406R (collectively, “drain terminals 406”) may be conductively coupled to the first drain region 404L and a second drain region 404R, respectively. As depicted in FIG 4A, the differential MOSFET 400A may be formed using NMOS or PMOS FETs.

Bridge conductors 130 may be disposed parallel to and above each respective one of the gate conductors 106. In embodiments, a plurality of conductive structures 132L₁, 132L₂, 132R₁, 132R₂, may electrically conductively couple the bridge conductor 130L and 130R to the respective gate conductor 106L and 106R at a plurality of locations. For example, conductive structures 132L₁, and 132R₁ may conductively couple a first end of the bridge conductors 130 to a first end of the gate conductor 106. Also, conductive structures 132L₂, and 132R₂ may conductively couple a second end of the bridge conductors 130 to a second end of the gate conductor 106.

FIG 4B provides a schematic of another illustrative MOSFET 400B having two gates 106, 2 drains 404 and one common source 402 formed using bridge conductors 130L and 130R disposed parallel to and above gate conductors 106L and 106R, respectively thereby forming a MOS channel, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 4B, the MOSFET 400B may include a common source region 402, a first drain region 404A and a second drain region 404B (collectively, “drain regions 404”). Each of the source region 402 and the drain regions 404 may include a conductive structure 210 electrically conductively coupled to at least a portion of the silicided region 310 disposed on the semiconductor substrate 220. Drain terminals 406L and 406R (collectively, “drain terminals 406”) may be conductively coupled to the first drain region 404A and a second drain region 404B, respectively. As depicted in FIG 4B, the MOSFET 400B may be formed using NMOS or PMOS.

Bridge conductors 130 may be disposed parallel to and above each respective one of the gate conductors 106. In embodiments, a plurality of conductive structures 132L₁, 132L₂, 132R₁, 132R₂, may electrically conductively couple the bridge conductor 130L and 130R to the respective gate conductor 106L and 106R at a plurality of locations. For example, conductive structures 132L₁, and 132R₁ may conductively couple a first end of the bridge conductors 130 to a first end of the gate conductor 106. Also, conductive structures 132L₂, and 132R₂ may conductively couple a second end of the bridge conductors 130 to a second end of the gate conductor 106.

FIG 4C provides a schematic of another illustrative MOSFET 400C formed using bridge conductors 130L and 130R disposed parallel to and above gate conductors 106L and 106R, respectively thereby forming a MOS channel, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 4C, the MOSFET 400C may include a first source region 402A, a second source region 402B (collectively, “source regions 402”), and a common drain region 404. Each of source regions 402A, 402B and the drain region 404 may include a conductive structure 210 electrically conductively coupled to at least a portion of the silicided region 310 disposed on the semiconductor substrate 220. Drain terminal 406 may be conductively coupled to the shared drain region 404. As depicted in FIG 4C, the MOSFET 400C may be formed using NMOS or PMOS.

Bridge conductors 130 may be disposed parallel to and above each respective one of the gate conductors 106. In embodiments, a plurality of conductive structures 132L₁, 132L₂, 132R₁, 132R₂, may electrically conductively couple the bridge conductor 130L and 130R to the respective gate conductor 106L and 106R at a plurality of locations. For example,

conductive structures 132L₁, and 132R₁ may conductively couple a first end of the bridge conductors 130 to a first end of the gate conductor 106. Also, conductive structures 132L₂, and 132R₂ may conductively couple a second end of the bridge conductors 130 to a second end of the gate conductor 106.

5 FIG 5A provides a schematic of an illustrative differential neutralized field-effect transistor (FET) that includes two amplifying FETs and two neutralizing FETs, in accordance with at least one embodiment of the present disclosure. Each of the FETs include a bridge conductor 130L₁, 130R₁, 130L₂, and 130R₂ disposed parallel to and above gate conductors 106L₁, 106L₂, 106R₁, and 106R₂, respectively thereby forming a MOS channel. A first gate
10 502 of a first amplifying FET may be conductively coupled to the bridge conductor 130R₁ and/or the gate conductor 106R₁. A second gate 504 of a second amplifying FET and the conductively coupled neutralized FET may be conductively coupled to the bridge conductor 130L₂ and/or the gate conductor 106L₂. A first drain 506 may be conductively coupled to the silicided merged drains 512A of the first neutralizing FET and amplifying FET. A
15 second drain 508 may be conductively coupled to the silicided merged drains 512B of the second neutralizing FET and second amplifying FET.

As depicted in FIG 5A, the source 510A of a first neutralizing FET may be conductively coupled to the gate conductor 106L₁. In embodiments, the source 510A of a first neutralizing FET may be conductively coupled at a plurality of locations to the gate
20 conductor 106L₁. For example, the source 510A of a first neutralizing FET may be conductively coupled to the conductive structure disposed proximate the first end of the gate conductor 106L₁ and to the conductive structure disposed proximate the second end of the gate conductor 106L₁.

As depicted in FIG 5A, the source 510B of the second neutralizing FET may be
25 conductively coupled to the gate conductor 106R₂. In embodiments, the source 510B of the second neutralizing FET may be conductively coupled at a plurality of locations to the gate conductor 106R₂. For example, the source 510B of the second neutralizing FET may be conductively coupled to the conductive structure disposed proximate the first end of the gate conductor 106R₂ and to the conductive structure disposed proximate the second end of the
30 gate conductor 106R₂. The neutralized differential FET has a common source 514.

FIG 5B provides a schematic of an illustrative inverter type amplifying circuit that includes an illustrative PMOS FET 520 and an illustrative NMOS FET 522 connected in electrical series, in accordance with at least one embodiment of the present disclosure. The PMOS FET 520 includes a silicided source PMOS region 530 disposed on the semiconductor

substrate 220, a drain PMOS region 532 disposed on the semiconductor substrate 220, a PMOS gate conductor 106L, and a bridge conductor 130L that is conductively coupled to the PMOS gate conductor 106L by a plurality of conductive structures 132L₁, 132L₂. A supply voltage 534 may be conductively coupled to the source PMOS region 530. An output signal 122 may be conductively coupled to the drain PMOS region 532.

The NMOS FET 522 includes a silicided source NMOS region 542 disposed on the semiconductor substrate 220, a drain NMOS region 540 disposed on the semiconductor substrate 220, a NMOS gate conductor 106R, and a bridge conductor 130R that is conductively coupled to the NMOS gate conductor 106R by a plurality of conductive structures 132R₁, 132R₂. A circuit ground 544 may be conductively coupled to the source NMOS region 542. The output signal 122 may be conductively coupled to the drain NMOS region 540.

FIG. 6 provides a perspective view of an illustrative differential varactor 600 such as the differential varactors 100A and 100B depicted in FIG 1 and FIG 2 and in which the differential varactor 600 includes a first varactor 102L and a second varactor 102R having interleaved bridge conductors 130L and 130R that are electrically conductively coupled at a first end 132L₁, 132R₁ and an opposed second end 132L₂, 132R₂ of respective interleaved gate conductors, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 3, the first bridge conductor 130L and the second bridge conductor 130R may be formed, patterned, or otherwise deposited on different conductive material layers within a multi-layer structure.

As depicted in FIG 6, the tuning port 110 may be disposed on a conductive material layer that may differ from the conductive material layers in which bridge conductors 130L and 130R, respectively, are patterned, formed, or otherwise deposited. A number of conductive structures 210 may electrically couple the tuning port 110 to a silicided portion 232 of the semiconductor substrate 220. In some instances, the conductive structures 210 may include a number of contacts 316A-316n (collectively, "contacts 316") and/or a number of metal layers 318A-318n (collectively, "metal layers 318").

In embodiments, a plurality of gate stacks 104L, 104R may be formed in (*e.g.*, for FinFETs) or on (*e.g.*, for planar devices) a silicon substrate 220. In at least some implementations, some or all of the plurality of gate conductors 106 may be formed, patterned or otherwise deposited above an STI/BOX region of the semiconductor substrate 220. In embodiments, each of the gate stacks 104L, 104R may be formed as fingers in an alternating, physically interleaved, pattern within/on the silicon substrate 220. In

embodiments, the conductive structures 132 that conductively couple the bridge conductors 130L, 130R to gate conductors 106L and 106R, respectively, may each include the same or a differing number of members, structures, or devices such as a number of contacts 305A-305n (collectively, “contacts 305”); a number of vias 306A-306n (collectively, “vias 306”); and/or
5 a number of metal layers 308A-308n (collectively, “metal layers 308”). In embodiments, the contacts 305, vias 306 and/or metal layers 308 may be patterned, formed, or otherwise deposited in, on, or about each of a number of layers forming the differential varactor 300 using any current or future developed patterning, forming, or deposition technology.

FIG. 7A depicts an electrical schematic 700A that includes a differential varactor 100
10 such as described in detail with regard to FIG 1 coupled in series between two linear capacitors 702L and 702R, in accordance with at least one embodiment of the present disclosure. In some implementations, gate bias resistors 704A, 704B may be conductively coupled between each varactor 102 and the neighboring linear capacitor 702. In some implementations, the linear capacitors 702 may include one or more capacitive devices
15 formed by the metallization of the technology. In such an arrangement, the ability to make small or incremental adjustments in capacitance through the differential varactor 100 permits fine tuning of the oscillator. The linear capacitors 702 reduce the minimum achievable capacitance change of the varactor 100— this tuning capability is beneficial in digital tunable millimeter-wave oscillators.

The capacitive voltage divider formed by the linear capacitor and the varactor 100
20 reduces the apparent capacitance of the complete varactor to the oscillator. This series connection increases also the quality factor (“Q value”) of the complete varactor 700A if the quality factor of the linear capacitor 702 is larger compared to the quality factor of the varactor 100. In addition, the linear capacitors 702 may decouple the low-frequency
25 amplitude noise (*e.g.* flicker noise) present in the oscillator circuit from the differential varactor 100 and consequently decrease the conversion of low-frequency amplitude noise into oscillator phase noise. The capacitance value of the linear capacitors 702 may be selected based on the proposed application.

FIG 7B depicts an electrical schematic 700B that includes a plurality of parallel
30 differential varactors 100A-100n such as described in detail with regard to FIG 1 coupled in series between two linear capacitors 702L and 702R that may have a greater, equal or smaller capacitance than the capacitance value presented by each of the plurality of differential varactors 100A-100n, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 7B, each of the plurality of differential varactors 100A-100n may include

a respective tuning port 710A-710n. A larger value for the capacitance of the series connected linear capacitors compared to the capacitance of the differential varactors may be selected to achieve a more equal/linear change in capacitance if the varactor banks are equal in size and switch in a digital manner between two tuning voltage values (digital tuning). A smaller value for the capacitance of the series connected linear capacitors compared to the capacitance of the differential varactors maybe selected to achieve a higher quality factor.

FIG 8 provides a layout of an illustrative differential varactor system 800 that incorporates linear capacitors and that includes a number of differential varactors 100 arranged such that the gate stacks 104L of the first varactor 102L in each of the differential varactors 100 are interleaved with the gate stacks 104R of the second varactor 102R in each of the differential varactors 100, in accordance with at least one embodiment of the present disclosure. As depicted in FIG 7, linear capacitors 702L, 702R may be conductively coupled in series with each of the differential varactor banks 804A-804n (collectively, “varactor banks 804”).

Each of the varactor banks 804 may include a plurality of individual differential varactors 100, for example each of the varactor banks 804 may include 2 or more individual differential varactors 100; 4 or more individual differential varactors 100; 10 or more individual differential varactors 100; 16 or more individual differential varactors 100; 20 or more individual differential varactors 100; or 26 or more individual differential varactors 100. In embodiments, any number of linear capacitors may be conductively coupled in series with the varactor banks 804. In some implementations, a single first linear capacitor 702L and a single second linear capacitor 702R may be coupled in series with each of the varactor banks 804. In other implementations, a plurality of first linear capacitors 702L and a plurality of second linear capacitors 702R may be coupled in series with each of the varactor banks 804.

Although FIG 8 depicts ten varactor banks 804, the differential varactor system 800 may contain a greater or lesser number of varactor banks 804. Each varactor bank 804A-804n may receive a respective tuning signal 802A-802n. In embodiments, each of the tuning signals 802 may be similar or identical such that the capacitance value presented by each varactor bank 804 is similar or identical. In other embodiments, some or all of the tuning signals 802 may be different from other tuning signals 802 such that the capacitance value presented by each varactor bank 804 is different. In another embodiment, some of the tuning signals 802 700L may receive two different voltage levels (digital tuning) while other tuning signals in the group of tuning signals 802 receive tuning signals with a continuous range of

voltage levels (analog tuning). The gate area or number of gate fingers within the individual varactors of the varactor bank may not be equal but maybe arranged in such a way that a linear frequency change of an oscillator is achieved with subsequent switching of the tuning voltages 802A-802n of the individual varactors 804A-804n of the varactor bank. The

5 frequency of an oscillator f_{osc} is inversely proportional to the square root of a capacitance ($f_{osc} \sim 1/\sqrt{C}$). The larger the capacitance the smaller the reduction of the oscillation frequency if always an equal amount of capacitance is added (case of equal size/gate fingers in the individual varactors 804A-804n of the varactor bank). To achieve a liner reduction of the oscillation frequency the area of subsequently added capacitors needs to be increased
10 respectively. A linear change of frequency is important in radar sensors which need to detect range and velocity of a target or obstacle (e.g. people or other cars in automotive car radar). In other embodiments the gate area of the individual varactors may be selected to achieve any kind of frequency change with the subsequent switching of individual varactors. The high accuracy/small tolerance, i.e. small process/manufacturing variations, of MOS capacitors
15 support a precise frequency shaping of the oscillator frequency tuning characteristic.

FIG 9 provides a graph 900 that depicts a quality factor (“Q factor”) under a balanced excitation at both gates of an illustrative differential varactor 100 as depicted in FIG 1 as a function of DC gate bias V_{g1} and tuning bias voltages V_{TUNE} for an applied gate RF signal at a frequency of 60 GHz, in accordance with at least one embodiment of the present

20 disclosure. As depicted in FIG 9, the Q factor of the differential varactor 100 varies from a low of about 9 to a high of about 14 depending, at least in part, on the gate voltage applied to the differential varactor 100. The quality factor Q is calculated according the equation $Q=1/(2*\pi*f*R*C)$ assuming a capacitor C connected in series with a resistance R. The resistance R is measured/extracted at 60 GHz while the capacitance is measured/extracted at
25 1GHz. The frequency f is selected at 60 GHz. π is ~ 3.1415 . The quality factor Q maybe larger if a reduced measured/extracted capacitance at 60 GHz would be used in the calculation (which would lead in turn to a reduced tuning range in Fig. 10). The series connection of two linear capacitors such as depicted in FIG 7 with a higher quality factor as the pure differential varactor of FIG 1 may enhance the quality factor of the structure in FIG
30 7 compared to the standalone differential varactor of FIG 1.

FIG 10 provides a graph 1000 depicting a capacitance of an illustrative differential varactor 100 as depicted in FIG 1 as a function of applied DC gate bias V_{g1} and tuning voltage V_{TUNE} at a frequency of 1 GHz, in accordance with at least one embodiment of the

present disclosure. As depicted in FIG 10 the ratio of the maximum capacitance to the minimum capacitance ($C_{\max}/C_{\min}$) of the differential varactor 100 ranges from about 1.45 to about 1.6 depending, at least in part, on the gate, tuning (and well voltage in case of inversion mode varactors) voltage applied to the differential varactor 100 when selecting $C_{\max}$ and $C_{\min}$.

5 FIG. 11 provides a high-level block flow diagram of an illustrative method 1100 of forming a differential varactor 100 such as depicted in FIG 1, FIG 2, and FIG 6, in accordance with at least one embodiment of the present disclosure. The method commences at 1102.

10 At 1104, a plurality of gate stacks 104L, 104R that include respective gate conductors 106L, 106R and respective gate dielectrics 108L, 108R may be formed in a semiconductor substrate 220. In some implementations, some or all of the gate conductors 106L and 106R may be formed, in whole or in part, on, or about a dielectric material 108L, 108R that has been patterned, deposited, or otherwise formed in, on, or about at least a portion of the semiconductor substrate 220. In some implementations, some or all of the gate conductors
15 106L and 106R may be formed, in whole or in part, in, on, or about a dielectric material that has been patterned, deposited, or otherwise formed in, on, or about at least a portion of a shallow trench isolation region 230 or trench isolation above BOX region in case of a SOI technology.

20 In some implementations each of the gate stacks 104L, 104R may be conductively coupled to a voltage source. In some implementations, each gate stack 104 may include a respective gate conductor 106 disposed on a gate dielectric 108. Each gate stack 104 may be formed in, on, or about at least a portion of the silicon substrate 220 and may include a gate conductor 106 having a first end and an opposed second end. In such implementations, a voltage source may be conductively coupled to the gate conductor 106 using a plurality of
25 contacts, vias, metal layers or similar electrically conductive structures 132 that conductively couple to at least the first end of the respective gate conductor 106 and to the second end 226 of the respective gate conductor 106. Providing a plurality of electrical couplings to the gate conductor 106 beneficially improves the quality factor of the differential varactor 100. For example, quality factors in excess of 9 at a frequency of 60 GHz or larger at lower
30 frequencies may be achieved using a conductive bridge structure 130 to electrically conductively couple the voltage source 120 to the first end and the second end of the gate conductor 106.

At 1106, a tuning port 110 may be patterned, formed, or otherwise deposited in a metal layer, for example one or more conductive material layers (*e.g.*, metal layer 1 (M1) and

metal layer 2 (M2) as depicted in FIG 6) within a multi-layer structure. In some implementations, the tuning port 110 may be conductively coupled to the silicon substrate proximate each gate stack 104 formed in, on, or about the silicon substrate 220. In some implementations, a number of conductive structures 210 may conductively couple the tuning port 110 to the silicon substrate 220. In some implementations, each of the conductive structures 210 may include a number of vias/contacts 306/316 and a number of metal layers 318 that conductively couple the tuning port 110 to the silicon substrate 220.

At 1108, a first bridge conductor 130L may be patterned, formed, or otherwise deposited in a conductive material layer (*e.g.*, metal layer 5 (M5) as depicted in FIG 6) layer within the multi-layer structure. In some implementations, each first bridge conductor 130 may be disposed parallel to a respective one of each of the gate conductors 106L_A-106L_n included in the first gate stacks 104L_A-104L_n patterned, deposited, or otherwise formed in, on, or about the silicon substrate 220. In some implementations, the second metal layer may differ from the first metal layer.

At 1110, a second bridge conductor 130R may be patterned, formed, or otherwise deposited in a metal layer, for example a third conductive material layer (*e.g.*, metal layer 4 (M4) as depicted in FIG 6) within the multi-layer structure. In some implementations, each second bridge conductor 130 may be disposed parallel to a respective one of each of the gate conductors 106R_A-106R_n included in the second gate stacks 104R_A-104R_n patterned, deposited, or otherwise formed in, on, or about the silicon substrate 220. In some implementations, the third metal layer may differ from either or both the first metal layer and the second metal layer.

At 1112, the first bridge conductor 130L may be electrically conductively coupled to the gate conductor 106L in the first gate stack 104L. In embodiments, the first bridge conductor 130L may be conductively coupled to a plurality of discrete locations on the gate conductor 106L in the first gate stack 104L. For example, the first bridge conductor 130L may be conductively coupled to a first discrete location such as the first end of the gate conductor 106L and to a second discrete location such as the second end of the gate conductor 106L. In some implementations, the first bridge conductor 130L may be disposed parallel to the gate conductor 106L and parallel to the first gate stack 104L. In some implementations, the first bridge conductor 130L may be patterned, formed, or otherwise disposed in a conductive material layer above the first gate stack 104L, for example a fourth conductive material layer (*e.g.*, M4) or a fifth conductive material layer (*e.g.*, M5). In some

implementations, the first bridge conductor 130L may extend parallel to the entire length of the first gate conductor 106L.

In some implementations, the physical width of the first bridge conductor 130L may be greater than the first gate stack 104L. In particular, the width of the first bridge conductor 130L may be greater than the width of the respective first gate stack 104L when the first bridge conductor 130L is formed on a different metal layer within the multi-layer structure than the second bridge conductor 130R. The width of the first gate stack 104L may refer to and/or may be associated with the channel length of the respective MOS varactor or field effect transistor (FET) with shorted and/or merged source and drain terminals.

In some implementations, the physical width of the first bridge conductor 130L may be less than the width of the respective first gate stack 104L. Such implementations are possible due to the relatively lower resistance of the first bridge conductor 130L when compared to the resistance of the respective first gate conductor 106L. In some implementations, an electrically conductive structure that may include any number and/or combination of contacts 305, vias 306, and/or metal layers 308 may conductively couple the first bridge conductor 130L to a plurality of discrete locations on the first gate conductor 106L.

At 1114, the second bridge conductor 130R may be electrically conductively coupled to the gate conductor 106R in the second gate stack 104R. In embodiments, the second bridge conductor 130R may be conductively coupled to a plurality of discrete locations on the gate conductor 106R of the second gate stack 104R. For example, the second bridge conductor 130R may be conductively coupled to a first discrete location such as the first end of the second gate conductor 106R and to a second discrete location such as the second end of the second gate conductor 106R. In some implementations, the second bridge conductor 130R may be disposed parallel to the gate conductor 106R and parallel to the second gate stack 104R. In some implementations, the second bridge conductor 130R may be patterned, formed, or otherwise disposed in a metal layer above the second gate stack 104R, for example a fourth conductive material layer (*e.g.*, M4) or a fifth conductive material layer (*e.g.*, M5). In some implementations, the second bridge conductor 130R may extend parallel to the entire length of the second gate stack 104R.

In some implementations, the physical width of the second bridge conductor 130R may be greater than the second gate stack 104R. In particular, the width of the second bridge conductor 130R may be greater than the width of the respective second gate stack 104R when the second bridge conductor 130R is formed on a different metal layer within the multi-layer

structure than the first bridge conductor 130L. The width of the second gate stack 104R may refer to and/or may be associated with the channel length of the respective MOS varactor or field effect transistor (FET) with shorted and/or merged source and drain terminals.

In some implementations, the physical width of the second bridge conductor 130R
5 may be less than the width of the respective second gate stack 104R. Such implementations are possible due to the relatively lower resistance of the second bridge conductor 130R when compared to the resistance of the respective second gate conductor 106R. In some implementations, an electrically conductive structure that may include any number and/or combination of contacts 305, vias 306, and/or metal layers 308 may conductively couple the
10 second bridge conductor 130R to a plurality of discrete locations on the second gate conductor 106R. The method 1100 concludes at 1116.

FIG 12 is a block diagram of an illustrative electronic device 1200 that includes one or more components, devices, modules, and/or sub-systems that include one or more differential varactor tuning devices such as those depicted in FIGS 1-8, in accordance with at
15 least one embodiment of the present disclosure. The electronic device 1200 may include one or more of the following: a configurable circuit 1202, a connectivity subsystem 1210; an input subsystem 1220; a memory subsystem 1230; a sensor subsystem 1240; an output subsystem 1250; an audio/visual (A/V) input/output system 1260; and a power supply subsystem 1270. The various subsystems may be communicably coupled to the configurable
20 circuit 1202 via one or more communications links 1290. For example, via one or more serial or parallel buses 1290.

The connectivity subsystem 1210 may include any number and/or combination of wired and/or wireless transmitters, receivers, and/or transceivers. At least a portion of the transmitters, receivers, and/or transceivers may include a number of varactor tuning devices
25 such as those depicted in FIGS 1-8. Example transceivers include, but are not limited to, one or more IEEE 802.11 (Wi-Fi®) transceivers 1212; one or more Near Field Communication (NFC) transceivers 1214; one or more BLUETOOTH® transceivers 1216; or any combination thereof. In at least some implementations, the connectivity subsystem 1210 enables the wearable electronic device 200 to communicably couple to one or more external devices via
30 one or more networks 1218. The one or more networks 1218 may include, but are not limited to, one or more local area networks (LANs); one or more metropolitan area networks (MANs); one or more virtual private networks (VPNs); one or more wide area networks (WANs); and/or one or more worldwide area networks (WWANs, such as the Internet).

The input subsystem 1220 may include any number and/or combination of devices and/or systems capable of receiving user input and providing one or more signals including information and/or data corresponding to the received user input to the configurable circuit 1202. The input subsystem 1220 may include input devices such as one or more buttons or
5 switches 1222; one or more keyboards or similar text entry devices 1224; and/or one or more pointing devices 1226.

The memory subsystem 1230 may include any number and/or combination of any current and/or future developed devices and/or systems capable of storing or otherwise retaining digital information and/or data. The memory subsystem 1230 may include random
10 access memory (RAM) 1232 and/or read-only memory (ROM) 1234 in a fixed or removable format. In some implementations, the memory subsystem 1230 may store or otherwise retain machine-readable instruction sets such as bootstrap code to enable the loading of an operating system 1236 upon startup of the electronic device 1200. The memory subsystem 1230 may include memory configured to hold information and/or data generated during the
15 operation of the electronic device 1200. Such memory may include, but is not limited to, static RAM (SRAM) or Dynamic RAM (DRAM). The ROM 1234 may include storage devices such as basic input/output system (BIOS) memory configured to provide instructions when the wearable electronic device 1200 activates, programmable memories such as electronic programmable ROMs, (EPROMs), Flash, etc. The memory subsystem 1230 may
20 include other fixed and/or removable memory such as floppy disks, hard drives, *etc.*, electronic memories such as solid state flash memory (e.g., eMMC), removable memory cards or sticks (e.g., uSD, USB), optical memories such as compact disc-based ROM (CD-ROM), or combinations thereof. The memory subsystem 1230 may further include the one or more storage devices 1238.

The sensor subsystem 1240 may include any number and/or combination of current and/or future developed devices and/or systems capable of detecting one or more internal and/or external parameters and/or conditions and generating one or more signals containing information and/or data representative of the respective detected parameter and/or condition. The sensor subsystem 1240 may include, but is not limited to, one or more temperature
25 sensors 1242; one or more acceleration sensors 1244 (or also one or more radar sensors detecting range, velocity and acceleration); one or more light sensors 1246; one or more proximity sensors 1248; or any combination thereof. In embodiments, the sensor subsystem 1240 may provide the configurable circuit 1202 with information and/or data indicative of one or more operational parameters of the electronic device 1200; one or more motion,
30

direction, or orientations parameters of the electronic device 1200; one or more external conditions about the electronic device 1200; or any combination thereof.

The output subsystem 1250 may include any number and/or combination of current and/or future developed devices and/or systems capable of generating one or more user perceptible outputs. The output subsystem 1250 may include one or more touchscreen output devices 1252 and/or one or more display devices 1254, or combinations thereof.

The A/V Input/Output (I/O) subsystem 1260 may include any number and/or combination of current and/or future developed devices and/or systems capable of receiving and/or transmitting audio data and/or video data. The A/V I/O system 1260 may include, but is not limited to, one or more audio coders; one or more audio decoders; one or more audio codecs 1262; one or more video capture devices 1264; or combinations thereof. In some implementations, the one or more video capture devices may include one or more visible spectrum video capture devices and/or one or more infrared video capture devices, and/or one or more millimeter wave imaging/video devices.

The power supply subsystem 1270 may include any number and/or combination of any current and/or future developed devices and/or systems capable of providing the electronic device 1200 with operating power. The power supply subsystem 1270 may include, but is not limited to, one or more power management control circuits 1272; one or more power sensors 1274 (voltage sensors, current sensors, *etc.*); one or more wireless charging systems 1276; one or more wired charging systems 1278; one or more energy storage devices 1280 (secondary batteries, supercapacitors, ultracapacitors, *etc.*) or combinations thereof.

Additionally, operations for the embodiments have been further described with reference to the above figures and accompanying examples. Some of the figures may include a logic flow. Although such figures presented herein may include a particular logic flow, it can be appreciated that the logic flow merely provides an example of how the general functionality described herein can be implemented. Further, the given logic flow does not necessarily have to be executed in the order presented unless otherwise indicated. In addition, the given logic flow may be implemented by a hardware element, a software element executed by a processor, or any combination thereof. The embodiments are not limited to this context.

Various features, aspects, and embodiments have been described herein. The features, aspects, and embodiments are susceptible to combination with one another as well as to variation and modification, as will be understood by those having skill in the art. The present

disclosure should, therefore, be considered to encompass such combinations, variations, and modifications. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

5 The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Accordingly, the claims are intended to cover all such equivalents. Various features,
10 aspects, and embodiments have been described herein. The features, aspects, and embodiments are susceptible to combination with one another as well as to variation and modification, as will be understood by those having skill in the art. The present disclosure should, therefore, be considered to encompass such combinations, variations, and modifications.

15 As described herein, various embodiments may be implemented using hardware elements, software elements, or any combination thereof. Examples of hardware elements may include processors, microprocessors, circuits, circuit elements (e.g., transistors, resistors, capacitors, inductors, coils, transmission lines, slow-wave transmission lines, transformers, and so forth), integrated circuits, application specific integrated circuits (ASIC), wireless
20 receivers, transmitters, transceivers, smart antenna arrays for beamforming and electronic beam steering used for wireless broadband communication or radar sensors for autonomous driving or as gesture sensors replacing a keyboard device for tactile internet experience, screening sensors for security applications, medical sensors (cancer screening), programmable logic devices (PLD), digital signal processors (DSP), field programmable gate array (FPGA), logic gates, registers, semiconductor device, chips, microchips, chip sets, and
25 so forth.

 The varactors, transistors, MOSFETs, devices, circuits, systems, and methods described herein are beneficial in devices, circuits and systems compliant with millimeter wave based wireless communication and connectivity standards such as: 5th generation
30 wireless systems (5G); 802.11ad, WiGig; next-generation 60 GHz connectivity; IEEE 802.11ay (WiGig 2); millimeter wave sensors such as millimeter wave based radar and imaging.

 The systems may communicate media and control information in accordance with one or more protocols. A protocol may comprise a set of predefined rules or instructions to

control how the nodes communicate information between each other. The protocol may be defined by one or more protocol standards as promulgated by a standards organization, such as the Internet Engineering Task Force (IETF), International Telecommunications Union (ITU), the Institute of Electrical and Electronics Engineers (IEEE), the 3GPP standardization body, the 5GPPP work group and so forth.

Systems may be implemented as a wireless communication system and may include one or more wireless nodes arranged to communicate information over one or more types of wireless communication media. An example of a wireless communication media may include portions of a wireless spectrum, such as the radio-frequency (RF) spectrum or frequency spectrum in the millimeter wave range (30-300 GHz). The wireless nodes may include components and interfaces suitable for communicating information signals over the designated wireless spectrum, such as one or more antennas, wireless transmitters/receivers ("transceivers"), amplifiers, filters, control logic, and so forth. Examples for the antenna may include an internal antenna, an omni-directional antenna, a monopole antenna, a dipole antenna, an end fed antenna, a circularly polarized antenna, a multi polarization plane antenna with electronically steered polarization, a micro-strip antenna, a micro-strip patch antenna, an endfire antenna, a diversity antenna, a dual antenna, an antenna array for beamforming reasons or electronic beam steering functionality, and so forth.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

The following examples pertain to further embodiments. The following examples of the present disclosure may comprise subject material such devices, systems, methods, and means for performing acts that include inversion type differential varactors 100A, accumulation type differential varactors 100B, varactor banks 200 comprising any number of inversion type and/or accumulation type differential varactors 100A, 100B, and fabrication methods for same. Specifically, the differential varactors 100 disclosed herein feature a bridge conductor 222 that conductively couples to each gate conductor 106 at a plurality of locations, such as a first end 224 and a second end 226 of the gate conductor 106. Further, such bridge conductors 222 may be disposed on a different metal layer than the gate

conductor 106 and may be formed parallel to the respective gate conductor 106. The embodiments are not limited to planar bulk CMOS integration but can include usage of silicon/semiconductor on insulator (SOI) technology. Varactors may be formed as planar devices but also as 3D FinFET devices. Varactors may be formed as inversion mode/type or
5 as accumulation mode/type MOS varactors. Semiconductors to be used for the formation of the varactor device can include silicon, germanium, silicon-germanium (SiGe), GaAs, InAs, GaN, InN, AlN, InSb, InP. Semiconductors like GaAs, GaN, InN, AlN, InP, InSb may be formed/disposed above a silicon substrate.

According to example 1, there is provided a metal oxide semiconductor (MOS)
10 differential varactor. The MOS differential varactor may include a first MOS varactor and a second MOS varactor conductively coupled to a common tuning port. The first MOS varactor may include a first tuning port; a first gate conductor having a first end and a second end opposite the first end formed in a first conductive material layer of a multi-layer semiconductor; a first bridge conductor having a first end and a second end, the first bridge
15 conductor disposed a distance from, and parallel to, the first gate conductor; and a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations. The second MOS varactor may include a second tuning port conductively coupled to the first tuning port; a second gate conductor having a first end and a second end opposite the first end formed in the first
20 conductive material layer of the multi-layer semiconductor; a second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

25 Example 2 may include elements of example 1 and may additionally include a shallow trench isolation region disposed about a periphery of the MOS differential varactor.

Example 3 may include elements of example 1 where the first bridge conductor is parallel to and coextensive with the first gate conductor and where the second bridge conductor is parallel to and coextensive with the second gate conductor.

30 Example 4 may include elements of example 1 where the first bridge conductor is formed in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer and where the second bridge conductor is formed in a conductive material layer of the multi-layer semiconductor disposed a second distance from the first conductive material layer.

Example 5 may include elements of example 4 where the first distance is different from the second distance.

Example 6 may include elements of example 4 where the first tuning port and the second tuning port are formed in a conductive material layer of the multi-layer semiconductor
5 disposed a third distance from the first conductive material layer.

Example 7 may include elements of example 6 where the third distance is less than the first distance.

Example 8 may include elements of example 1 where the plurality of conductive structures that electrically conductively couple to the first gate conductor and to the first
10 bridge conductor at a corresponding plurality of locations may include a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor and a second conductive structure electrically
conductively coupling the second end of the first bridge conductor to the second end of the first gate conductor. Additionally, the plurality of conductive structures that electrically
15 conductively couple to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations may include a first conductive structure electrically conductively coupling the first end of the second bridge conductor to the first end of the second gate conductor and a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate
20 conductor.

Example 9 may include elements of any of examples 1 through 8 and may additionally include a first linear capacitor conductively coupled directly to the first MOS varactor; and a second linear capacitor conductively coupled directly to the second MOS varactor.

Example 10 may include elements of example 9 and may additionally include a first
25 gate bias resistor conductively coupled between the first MOS varactor and the first linear capacitor; and a second gate bias resistor conductively coupled between the second MOS varactor and the second linear capacitor.

According to example 11 there is provided a metal oxide semiconductor (MOS)
30 differential varactor system. The MOS differential varactor system may include a plurality of MOS differential varactors, each of the plurality of MOS differential varactors including a first MOS varactor and a second MOS varactor. The first MOS varactor in each of the plurality of MOS differential varactors may include: a first gate conductor having a first end and a second end opposite the first end formed in a first conductive material layer of a multi-

layer semiconductor; a first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; and a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations. The second MOS varactor in each of the plurality of MOS differential varactors may include: a second gate conductor having a first end and a second end opposite the first end formed in the first conductive material layer of the multi-layer semiconductor; a second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations. Further, the second gate conductor and the second bridge conductor included in each of the plurality of differential varactors forms an interleaved pattern with the first gate conductor and the first bridge connector included in each of the plurality of differential varactors.

Example 12 may include elements of example 11 and may additionally include a shallow trench isolation region disposed about a periphery of the plurality of differential varactors forming the differential varactor system.

Example 13 may include elements of example 11 where the first bridge conductor in the first MOS varactor included in each differential varactor may be parallel to and coextensive with the first gate conductor and where the second bridge conductor in the second MOS varactor included in each differential varactor may be parallel to and coextensive with the second gate conductor.

Example 14 may include elements of example 11 where the first bridge conductor in the first MOS varactor included in each differential varactor may be formed in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer and where the second bridge conductor in the second MOS varactor included in each differential varactor may be formed in a conductive material layer of the multi-layer semiconductor disposed a second distance from the first conductive material layer.

Example 15 may include elements of example 14 where the first distance is different from the second distance.

Example 16 may include elements of example 14 where the first tuning port in the first MOS varactor included in each differential varactor and the second tuning port in the second MOS varactor included in each differential varactor may be formed in a conductive

material layer of the multi-layer semiconductor disposed a third distance from the first conductive material layer.

Example 17 may include elements of example 16 where the third distance is less than the first distance.

5 Example 18 may include elements of example 11 where the plurality of conductive structures that electrically conductively couple to the first gate conductor and to the first bridge conductor in the first MOS varactor included in each differential varactor at a corresponding plurality of locations may include a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first
10 gate conductor and a second conductive structure electrically conductively coupling the second end of the first bridge conductor to the second end of the first gate conductor and where the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor in the second MOS varactor included in each differential varactor at a corresponding plurality of locations may include a
15 first conductive structure electrically conductively coupling the first end of the second bridge conductor to the first end of the second gate conductor and a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

 Example 19 may include elements of any of examples 11 through 18 and may
20 additionally include a first linear capacitor conductively coupled directly to respective ones of the first MOS varactor included in at least some of the plurality of MOS differential varactors; and a second linear capacitor conductively coupled directly to respective ones of the second MOS varactor included in at least some of the plurality of MOS differential varactors.

25 Example 20 may include elements of example 19 and may additionally include a first gate bias resistor conductively coupled between the first MOS varactor included in at least some of the plurality of MOS differential varactors and the first linear capacitor and a second gate bias resistor conductively coupled between the second MOS varactor included in at least some of the plurality of MOS differential varactors and the second linear capacitor.

30 According to example 21, there is provided a method of fabricating a metal oxide semiconductor (MOS) differential varactor. The fabrication method may include forming a first tuning port of a first MOS varactor on a semiconductor substrate; forming a first gate conductor of the first MOS varactor in a first conductive material layer of a multi-layer semiconductor, the first gate conductor having a first end and a second end opposite the first

end; forming a first bridge conductor of the first MOS varactor, the first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; forming a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a
5 corresponding plurality of locations; forming a second tuning port of a second MOS varactor conductively coupled to the first tuning port of the first MOS varactor; forming a second gate conductor of the second MOS varactor in the first conductive material layer of the multi-layer semiconductor, the second gate conductor having a first end and a second end opposite the first end; forming a second bridge conductor of the second MOS varactor, the second bridge
10 conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and forming a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

Example 22 may include elements of example 21 and the method may additionally
15 include forming a shallow trench isolation region disposed about a periphery of the plurality of differential varactors forming the differential varactor system.

Example 23 may include elements of example 21, where forming a first bridge conductor of the first MOS varactor may include forming the first bridge conductor of the first MOS varactor included in each differential varactor parallel to and coextensive with the
20 first gate conductor of the first MOS varactor and where forming a second bridge conductor of the second MOS varactor may include forming the second bridge conductor of the second MOS varactor included in each differential varactor parallel to and coextensive with the second gate conductor.

Example 24 may include elements of example 21 where forming a first bridge
25 conductor of the first MOS varactor may include forming the first bridge conductor in the first MOS varactor included in each differential varactor in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer and where forming a second bridge conductor of the second MOS varactor may include forming the second bridge conductor in the second MOS varactor included in each
30 differential varactor in a conductive material layer of the multi-layer semiconductor disposed a second distance from the first conductive material layer.

Example 25 may include elements of example 24 where the first distance is different from the second distance.

Example 26 may include elements of example 24 where forming a first tuning port of a first MOS varactor and forming a second tuning port of a second MOS varactor may include: forming the first tuning port in the first MOS varactor included in each differential varactor and the second tuning port in the second MOS varactor included in each differential
5 varactor in a conductive material layer of the multi-layer semiconductor disposed a third distance from the first conductive material layer.

Example 27 may include elements of example 26 where the third distance is less than the first distance.

Example 28 may include elements of example 21 where forming the plurality of
10 conductive structures that electrically conductively couple to the first gate conductor and to the first bridge conductor in the first MOS varactor included in each differential varactor at a corresponding plurality of locations may include: forming a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor; and forming a second conductive structure electrically conductively
15 coupling the second end of the first bridge conductor to the second end of the first gate conductor. Additionally, forming the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor in the second MOS varactor included in each differential varactor at a corresponding plurality of locations may include: forming a first conductive structure electrically conductively coupling
20 the first end of the second bridge conductor to the first end of the second gate conductor; and forming a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

Example 29 may include elements of any of examples 21 through 28 and the method may additionally include conductively coupling a first linear capacitor directly to the first
25 MOS varactor; and conductively coupling a second linear capacitor directly to the second MOS varactor.

Example 30 may include elements of example 29 and the method may additionally include conductively coupling a first gate bias resistor between the first MOS varactor and the first linear capacitor; and conductively coupling a second gate bias resistor between the
30 second MOS varactor and the second linear capacitor.

According to example 31, there is provided a metal oxide semiconductor (MOS) differential varactor fabrication system. The MOS differential varactor fabrication system may include a means for forming a first tuning port of a first MOS varactor on a semiconductor substrate; a means for forming a first gate conductor of the first MOS varactor

in a first conductive material layer of a multi-layer semiconductor, the first gate conductor having a first end and a second end opposite the first end; a means for forming a first bridge conductor of the first MOS varactor, the first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; a means for forming a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations; a means for forming a second tuning port of a second MOS varactor conductively coupled to the first tuning port of the first MOS varactor; a means for forming a second gate conductor of the second MOS varactor in the first conductive material layer of the multi-layer semiconductor, the second gate conductor having a first end and a second end opposite the first end; a means for forming a second bridge conductor of the second MOS varactor, the second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and a means for forming a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

Example 32 may include elements of example 31 and the system may additionally include a means for forming a shallow trench isolation region disposed about a periphery of the plurality of differential varactors forming the differential varactor system.

Example 33 may include elements of example 31 where the means for forming a first bridge conductor of the first MOS varactor may include a means for forming the first bridge conductor of the first MOS varactor included in each differential varactor parallel to and coextensive with the first gate conductor of the first MOS varactor; and where the means for forming a second bridge conductor of the second MOS varactor may include a means for forming the second bridge conductor of the second MOS varactor included in each differential varactor parallel to and coextensive with the second gate conductor.

Example 34 may include elements of example 31 where the means for forming a first bridge conductor of the first MOS varactor may include a means for forming the first bridge conductor in the first MOS varactor included in each differential varactor in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer; and where the means for forming a second bridge conductor of the second MOS varactor may include a means for forming the second bridge conductor in the second MOS varactor included in each differential varactor in a conductive material layer of

the multi-layer semiconductor disposed a second distance from the first conductive material layer.

Example 35 may include elements of example 34 where the first distance is different from the second distance.

5 Example 36 may include elements of example 34 where the means for forming a first tuning port of a first MOS varactor and forming a second tuning port of a second MOS varactor may include a means for forming the first tuning port in the first MOS varactor included in each differential varactor and the second tuning port in the second MOS varactor included in each differential varactor in a conductive material layer of the multi-layer
10 semiconductor disposed a third distance from the first conductive material layer.

Example 37 may include elements of example 36 where the third distance is less than the first distance.

Example 38 may include elements of example 31 where the means for forming the plurality of conductive structures that electrically conductively couple to the first gate
15 conductor and to the first bridge conductor in the first MOS varactor included in each differential varactor at a corresponding plurality of locations may include a means for forming a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor; and a means for forming a second conductive structure electrically conductively coupling the second end of the first bridge
20 conductor to the second end of the first gate conductor. Additionally, the means for forming the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor in the second MOS varactor included in each differential varactor at a corresponding plurality of locations may include a means for forming a first conductive structure electrically conductively coupling the first end of the
25 second bridge conductor to the first end of the second gate conductor; and a means for forming a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

Example 39 may include elements of any of examples 31 through 38, and the system may additionally include a means for conductively coupling a first linear capacitor directly to
30 the first MOS varactor; and a means for conductively coupling a second linear capacitor directly to the second MOS varactor.

Example 40 may include elements of example 39, and the system may additionally include a means for conductively coupling a first gate bias resistor between the first MOS

varactor and the first linear capacitor; and a means for conductively coupling a second gate bias resistor between the second MOS varactor and the second linear capacitor.

The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and
5 expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Accordingly, the claims are intended to cover all such equivalents.

WHAT IS CLAIMED:

1. A metal oxide semiconductor (MOS) differential varactor, comprising:

a first MOS varactor including:

- 5 a first tuning port;
a first gate conductor having a first end and a second end opposite the first end
formed in a first conductive material layer of a multi-layer semiconductor;
a first bridge conductor having a first end and a second end, the first bridge
conductor disposed a distance from, and parallel to, the first gate conductor; and
10 a plurality of conductive structures electrically conductively coupled to the
first gate conductor and to the first bridge conductor at a corresponding plurality of locations;
and

a second MOS varactor including:

- a second tuning port conductively coupled to the first tuning port;
15 a second gate conductor having a first end and a second end opposite the first
end formed in the first conductive material layer of the multi-layer semiconductor;
a second bridge conductor having a first end and a second end, the second
bridge conductor disposed a distance from, and parallel to, the second gate conductor; and
a plurality of conductive structures electrically conductively coupled to the
20 second gate conductor and to the second bridge conductor at a corresponding plurality of
locations.

2. The MOS differential varactor of claim 1, further comprising:

- a shallow trench isolation region disposed about a periphery of the MOS differential
25 varactor.

3. The MOS differential varactor of claim 1:

- wherein the first bridge conductor is parallel to and coextensive with the first gate
conductor; and
30 wherein the second bridge conductor is parallel to and coextensive with the second
gate conductor.

4. The MOS differential varactor of claim 1:

wherein the first bridge conductor is formed in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer; and

5 wherein the second bridge conductor is formed in a conductive material layer of the multi-layer semiconductor disposed a second distance from the first conductive material layer.

10 5. The MOS differential varactor of claim 4 wherein the first distance is different from the second distance.

6. The MOS differential varactor of claim 4 wherein the first tuning port and the second tuning port are formed in a conductive material layer of the multi-layer semiconductor disposed a third distance from the first conductive material layer.

15 7. The MOS differential varactor of claim 6 wherein the third distance is less than the first distance.

8. The MOS differential varactor of claim 1:

20 wherein the plurality of conductive structures that electrically conductively couple to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations comprise:

a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor; and

25 a second conductive structure electrically conductively coupling the second end of the first bridge conductor to the second end of the first gate conductor; and

wherein the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations comprise:

30 a first conductive structure electrically conductively coupling the first end of the second bridge conductor to the first end of the second gate conductor; and

a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

9. The MOS differential varactor of any of claims 1 through 8, further comprising:

a first linear capacitor conductively coupled directly to the first MOS varactor; and
a second linear capacitor conductively coupled directly to the second MOS varactor.

5

10. The MOS differential varactor of claim 9, further comprising:

a first gate bias resistor conductively coupled between the first MOS varactor and the first linear capacitor; and

a second gate bias resistor conductively coupled between the second MOS varactor
and the second linear capacitor.

10

11. A metal oxide semiconductor (MOS) differential varactor system, comprising:

a plurality of MOS differential varactors, each of the plurality of MOS differential varactors including a first MOS varactor and a second MOS varactor;

15

wherein the first MOS varactor in each of the plurality of MOS differential varactors includes:

a first gate conductor having a first end and a second end opposite the first end formed in a first conductive material layer of a multi-layer semiconductor;

20

a first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor; and

a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations; and

25

wherein the second MOS varactor included in each of the plurality of MOS differential varactors includes:

a second gate conductor having a first end and a second end opposite the first end formed in the first conductive material layer of the multi-layer semiconductor;

a second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and

30

a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations; and

wherein the second gate conductor and the second bridge conductor included in each of the plurality of differential varactors forms an interleaved pattern with the first gate

conductor and the first bridge connector included in each of the plurality of differential varactors.

12. The MOS differential varactor system of claim 11, further comprising:
5 a shallow trench isolation region disposed about a periphery of the plurality of differential varactors forming the differential varactor system.

13. The MOS differential varactor system of claim 11:
wherein the first bridge conductor in the first MOS varactor included in each
10 differential varactor is parallel to and coextensive with the first gate conductor; and
wherein the second bridge conductor in the second MOS varactor included in each differential varactor is parallel to and coextensive with the second gate conductor.

14. The MOS differential varactor system of claim 11:
15 wherein the first bridge conductor in the first MOS varactor included in each differential varactor is formed in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer; and
wherein the second bridge conductor in the second MOS varactor included in each differential varactor is formed in a conductive material layer of the multi-layer semiconductor
20 disposed a second distance from the first conductive material layer.

15. The MOS differential varactor system of claim 14 wherein the first distance is different from the second distance.

25 16. The MOS differential varactor system of claim 14 wherein the first tuning port in the first MOS varactor included in each differential varactor and the second tuning port in the second MOS varactor included in each differential varactor are formed in a conductive material layer of the multi-layer semiconductor disposed a third distance from the first conductive material layer.

30 17. The MOS differential varactor system of claim 16 wherein the third distance is less than the first distance.

18. The MOS differential varactor system of claim 11:

wherein the plurality of conductive structures that electrically conductively couple to the first gate conductor and to the first bridge conductor in the first MOS varactor included in each differential varactor at a corresponding plurality of locations comprise:

5 a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor; and

a second conductive structure electrically conductively coupling the second end of the first bridge conductor to the second end of the first gate conductor; and

10 wherein the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor in the second MOS varactor included in each differential varactor at a corresponding plurality of locations comprise:

a first conductive structure electrically conductively coupling the first end of the second bridge conductor to the first end of the second gate conductor; and

a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

15

19. The MOS differential varactor system of any of claims 11 through 18, further comprising:

a first linear capacitor conductively coupled directly to respective ones of the first MOS varactor included in at least some of the plurality of MOS differential varactors; and

20 a second linear capacitor conductively coupled directly to respective ones of the second MOS varactor included in at least some of the plurality of MOS differential varactors.

20. The MOS differential varactor of claim 19, further comprising:

25 a first gate bias resistor conductively coupled between the first MOS varactor included in at least some of the plurality of MOS differential varactors and the first linear capacitor; and

a second gate bias resistor conductively coupled between the second MOS varactor included in at least some of the plurality of MOS differential varactors and the second linear capacitor.

30

21. A method of fabricating a metal oxide semiconductor (MOS) differential varactor, the method comprising:

forming a first tuning port of a first MOS varactor on a semiconductor substrate;

forming a first gate conductor of the first MOS varactor in a first conductive material layer of a multi-layer semiconductor, the first gate conductor having a first end and a second end opposite the first end;

5 forming a first bridge conductor of the first MOS varactor, the first bridge conductor having a first end and a second end, the first bridge conductor disposed a distance from, and parallel to, the first gate conductor;

forming a plurality of conductive structures electrically conductively coupled to the first gate conductor and to the first bridge conductor at a corresponding plurality of locations;

10 forming a second tuning port of a second MOS varactor conductively coupled to the first tuning port of the first MOS varactor;

forming a second gate conductor of the second MOS varactor in the first conductive material layer of the multi-layer semiconductor, the second gate conductor having a first end and a second end opposite the first end;

15 forming a second bridge conductor of the second MOS varactor, the second bridge conductor having a first end and a second end, the second bridge conductor disposed a distance from, and parallel to, the second gate conductor; and

forming a plurality of conductive structures electrically conductively coupled to the second gate conductor and to the second bridge conductor at a corresponding plurality of locations.

20

22. The MOS differential varactor fabrication method of claim 21, further comprising:

forming a shallow trench isolation region disposed about a periphery of the plurality of differential varactors forming the differential varactor system.

23. The MOS differential varactor fabrication method of claim 21:

wherein forming a first bridge conductor of the first MOS varactor comprises forming the first bridge conductor of the first MOS varactor included in each differential varactor parallel to and coextensive with the first gate conductor of the first MOS varactor; and

5 wherein forming a second bridge conductor of the second MOS varactor comprises forming the second bridge conductor of the second MOS varactor included in each differential varactor parallel to and coextensive with the second gate conductor.

24. The MOS differential varactor fabrication method of claim 21:

10 wherein forming a first bridge conductor of the first MOS varactor comprises forming the first bridge conductor in the first MOS varactor included in each differential varactor in a conductive material layer of the multi-layer semiconductor disposed a first distance from the first conductive material layer; and

15 wherein forming a second bridge conductor of the second MOS varactor comprises forming the second bridge conductor in the second MOS varactor included in each differential varactor in a conductive material layer of the multi-layer semiconductor disposed a second distance from the first conductive material layer.

25. The MOS differential varactor fabrication method of claim 24 wherein the

20 first distance is different from the second distance.

26. The MOS differential varactor fabrication method of claim 24 wherein forming a first tuning port of a first MOS varactor and forming a second tuning port of a second MOS varactor comprises:

25 forming the first tuning port in the first MOS varactor included in each differential varactor and the second tuning port in the second MOS varactor included in each differential varactor in a conductive material layer of the multi-layer semiconductor disposed a third distance from the first conductive material layer.

30 27. The MOS differential varactor fabrication method of claim 26 wherein the third distance is less than the first distance.

28. The MOS differential varactor fabrication method of claim 21:

wherein forming the plurality of conductive structures that electrically conductively couple to the first gate conductor and to the first bridge conductor in the first MOS varactor included in each differential varactor at a corresponding plurality of locations comprises:

5 forming a first conductive structure electrically conductively coupling the first end of the first bridge conductor to the first end of the first gate conductor; and

 forming a second conductive structure electrically conductively coupling the second end of the first bridge conductor to the second end of the first gate conductor; and

10 wherein forming the plurality of conductive structures that electrically conductively couple to the second gate conductor and to the second bridge conductor in the second MOS varactor included in each differential varactor at a corresponding plurality of locations comprise:

 forming a first conductive structure electrically conductively coupling the first end of the second bridge conductor to the first end of the second gate conductor; and

15 forming a second conductive structure electrically conductively coupling the second end of the second bridge conductor to the second end of the second gate conductor.

29. The MOS differential varactor fabrication method of any of claims 21 through 28, further comprising:

20 conductively coupling a first linear capacitor directly to the first MOS varactor; and
 conductively coupling a second linear capacitor directly to the second MOS varactor.

30. The MOS differential varactor fabrication method of claim 29, further comprising:

25 conductively coupling a first gate bias resistor between the first MOS varactor and the first linear capacitor; and

 conductively coupling a second gate bias resistor between the second MOS varactor and the second linear capacitor.

30

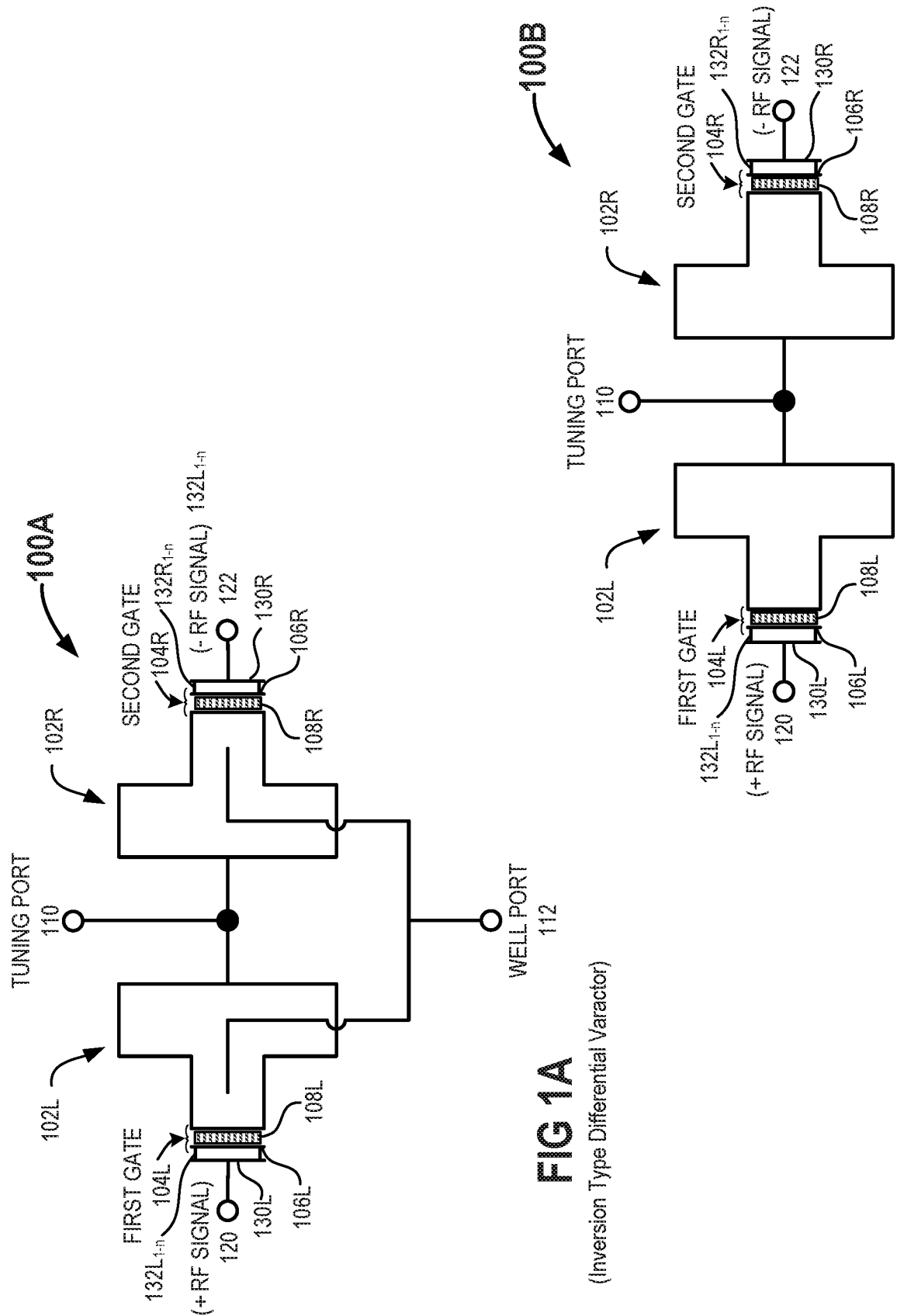
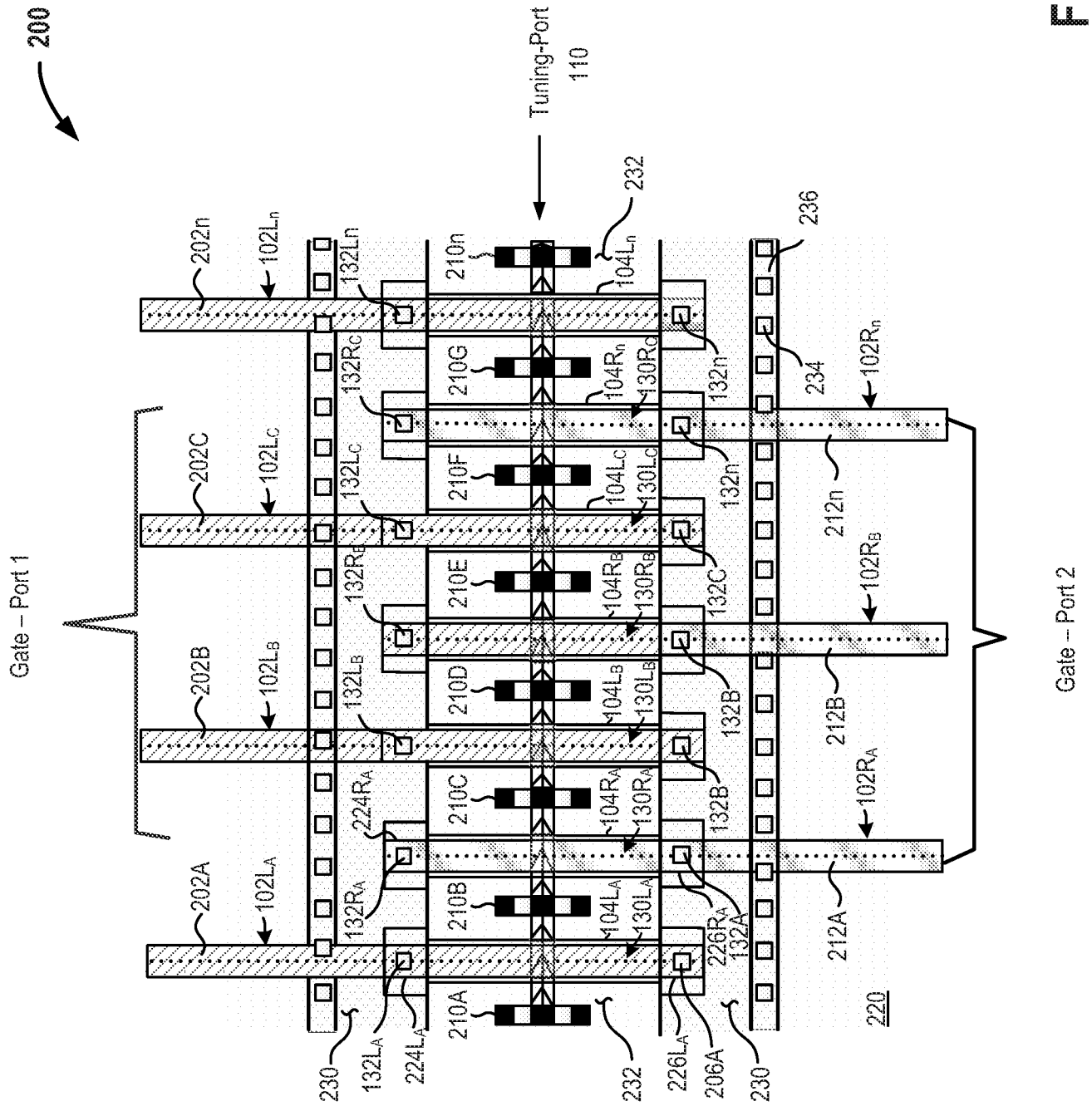


FIG 1B

Accumulation Type Differential Varactor



2GLL

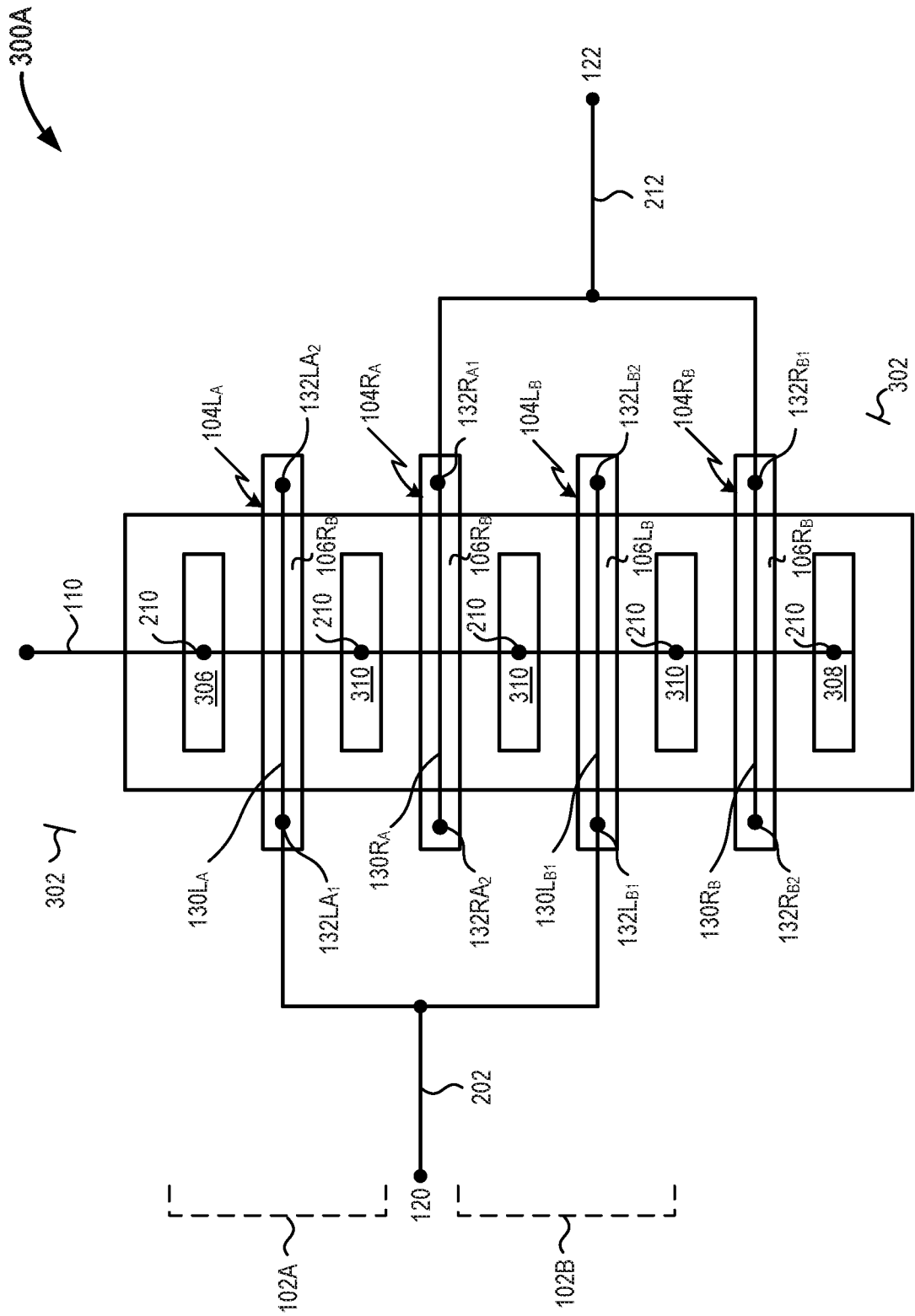
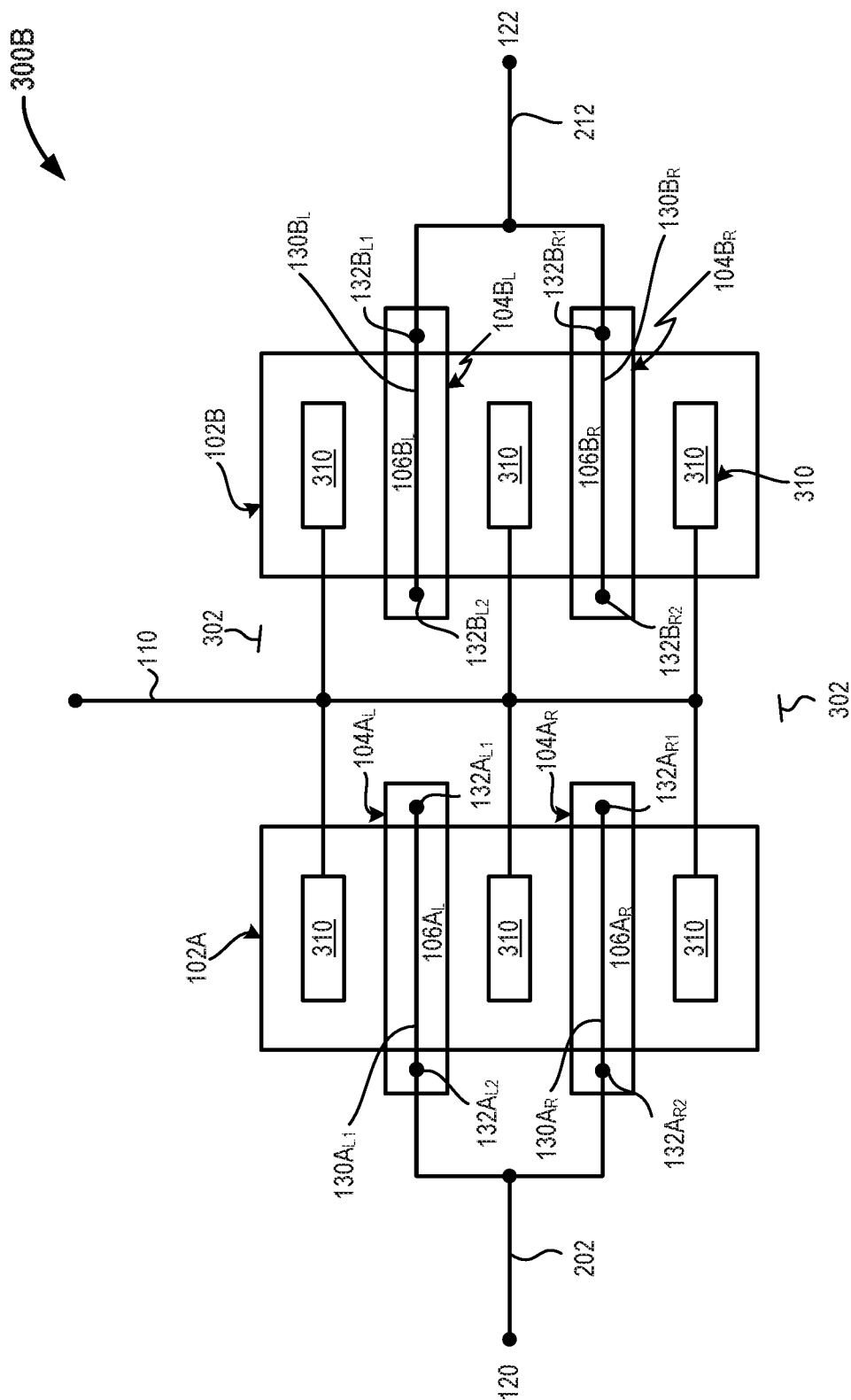


FIG 3A



300C

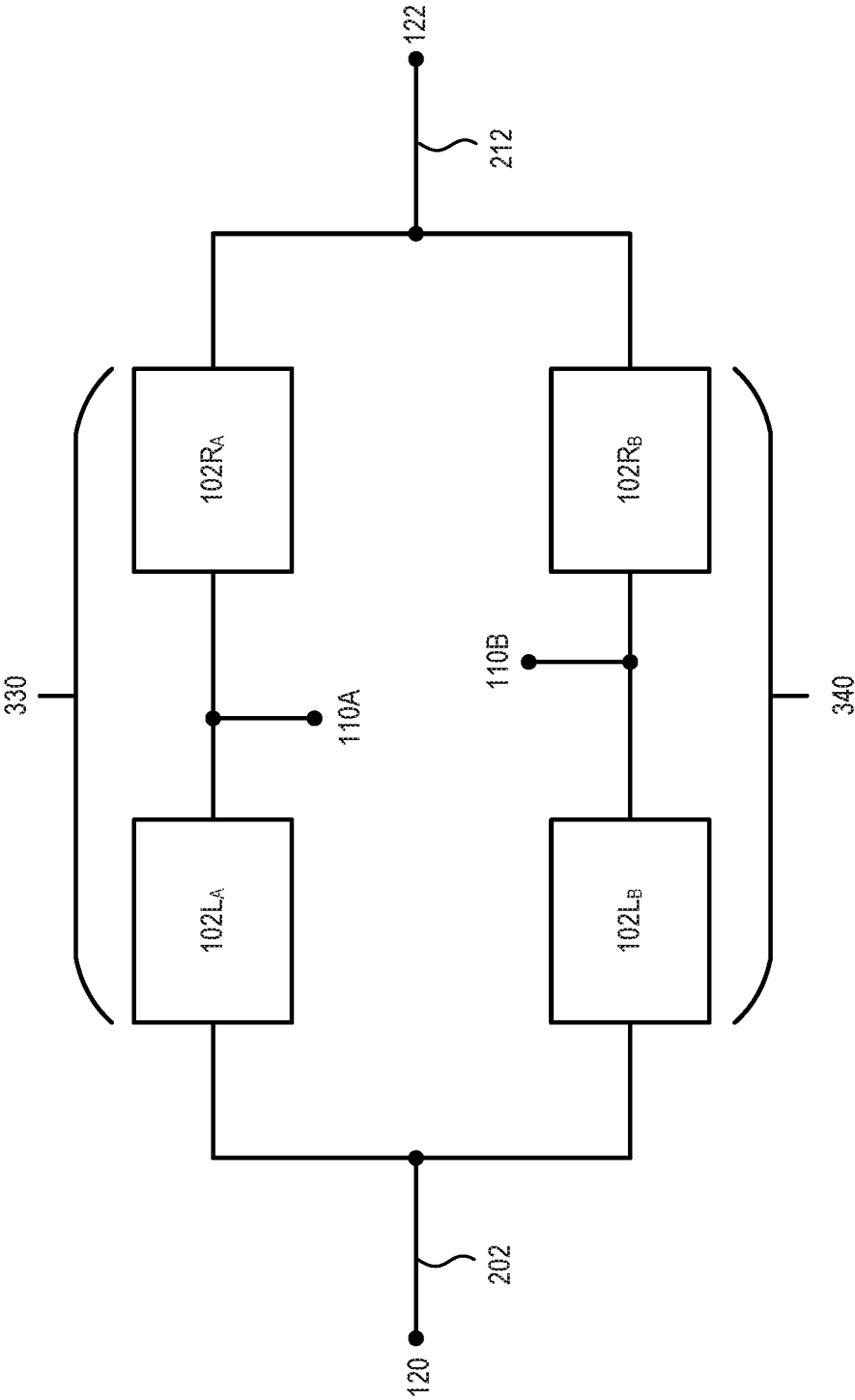


FIG 3C

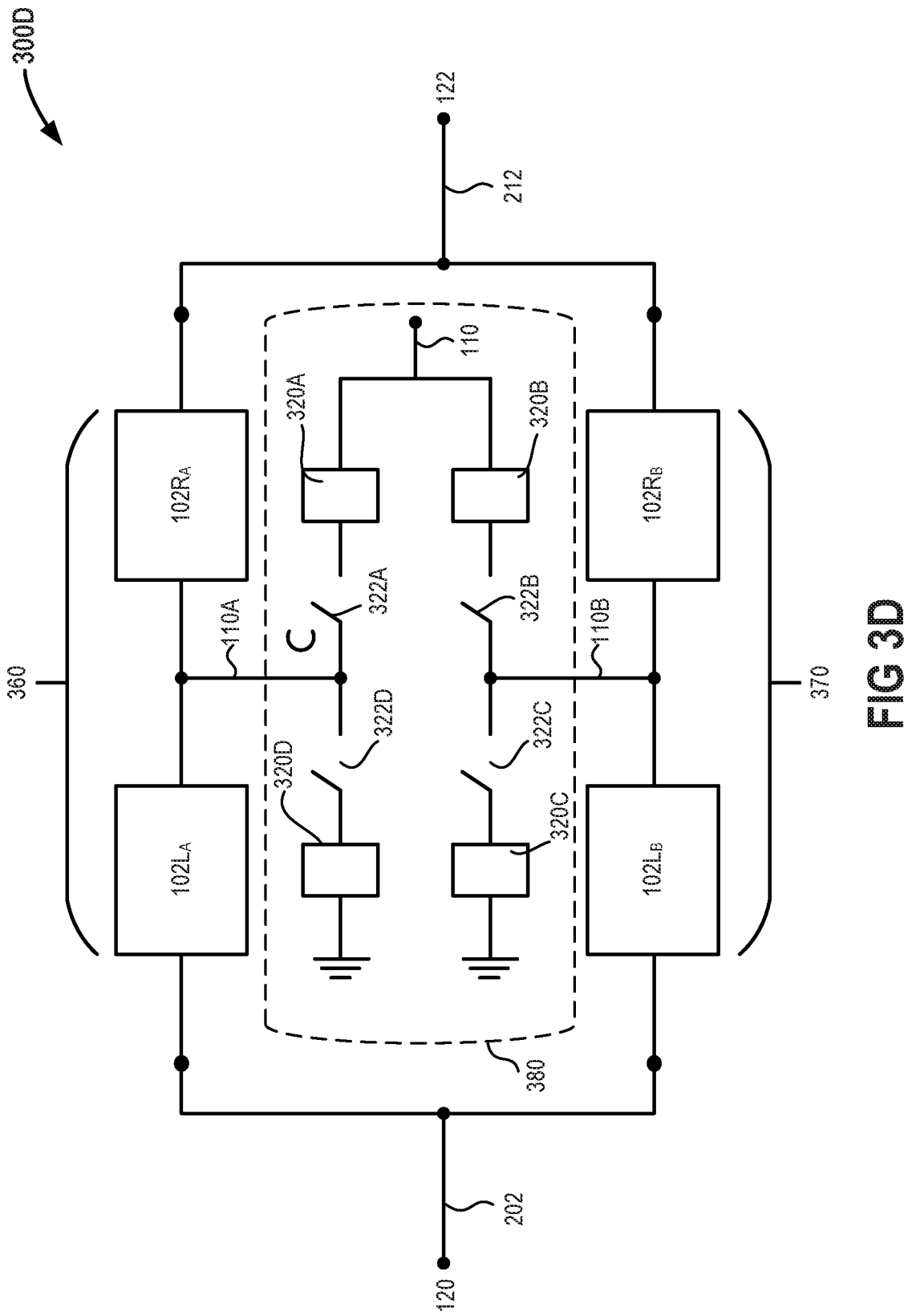


FIG 3D

400A

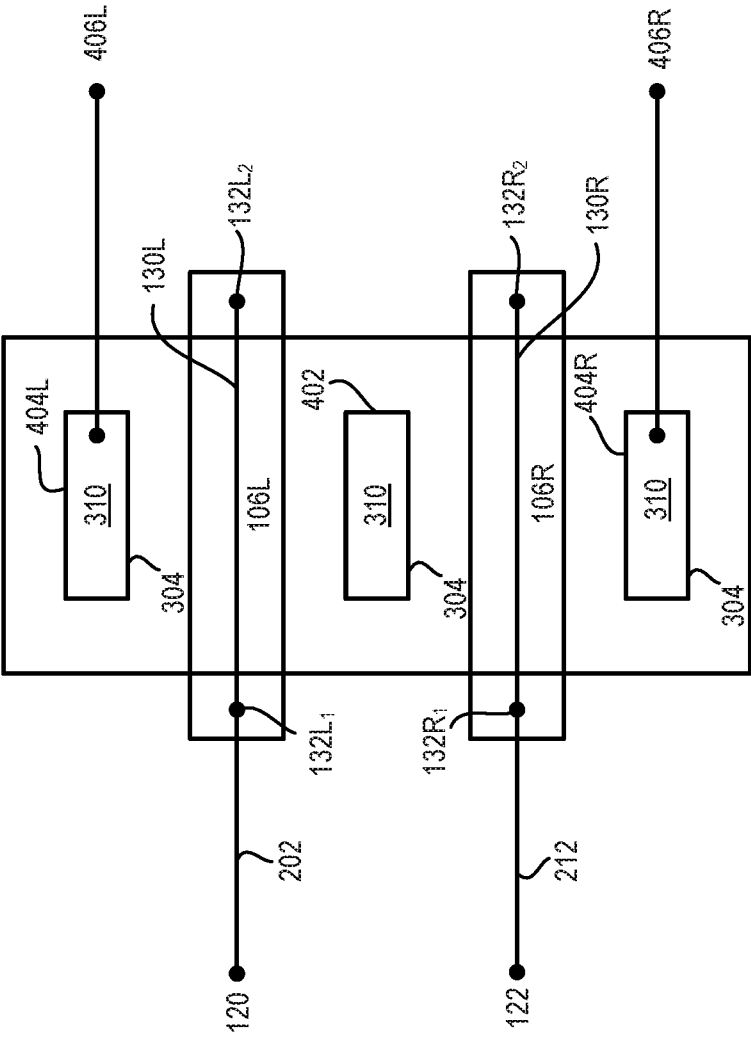


FIG 4A

400B

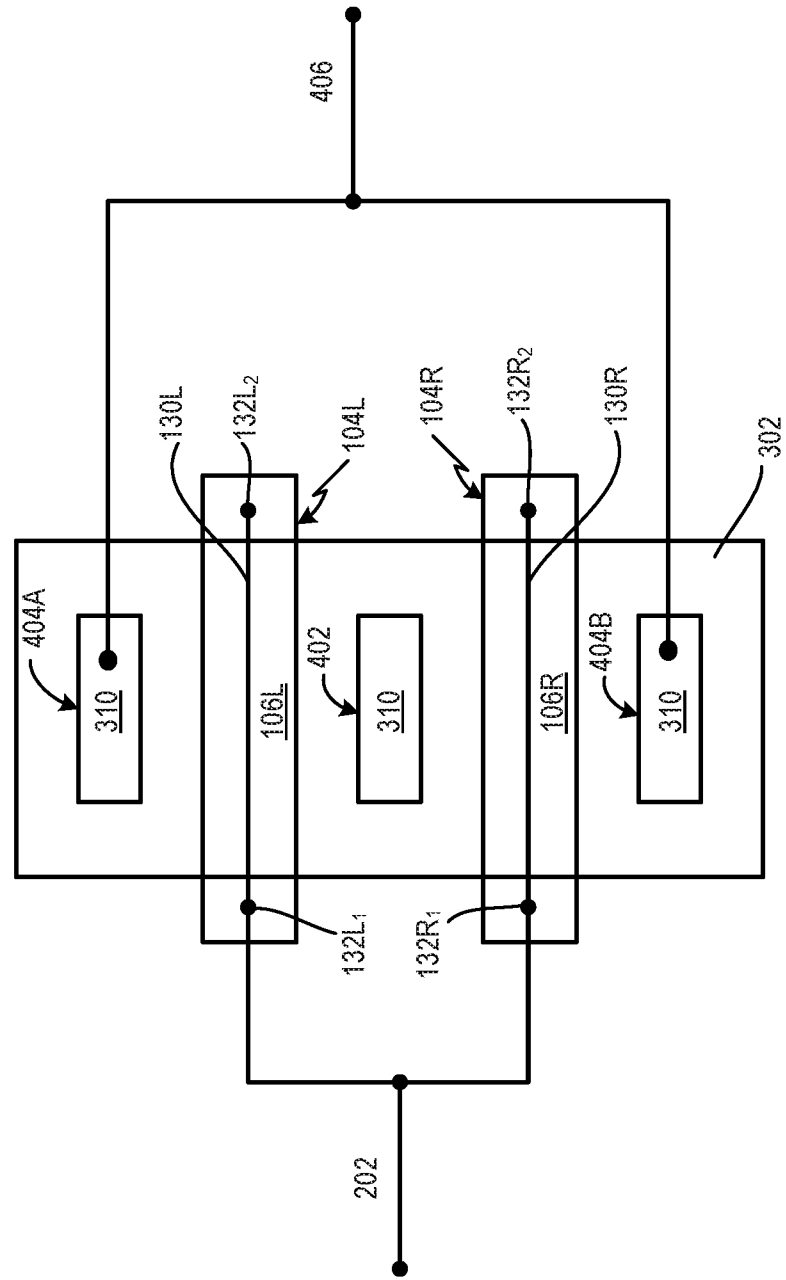


FIG 4B

400C

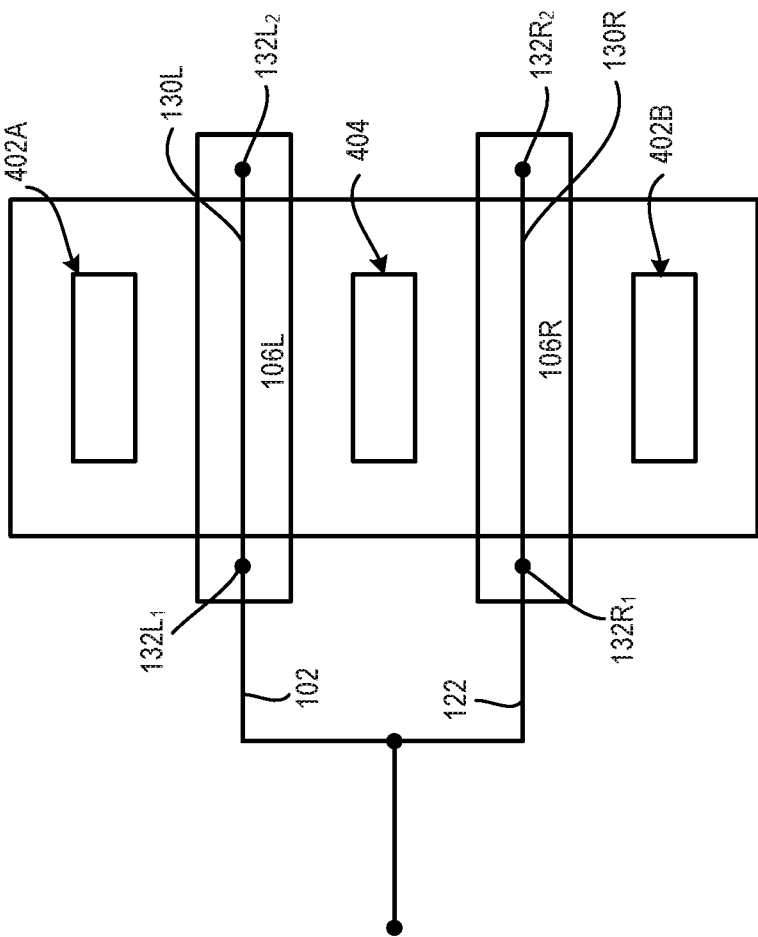


FIG 4C

500A

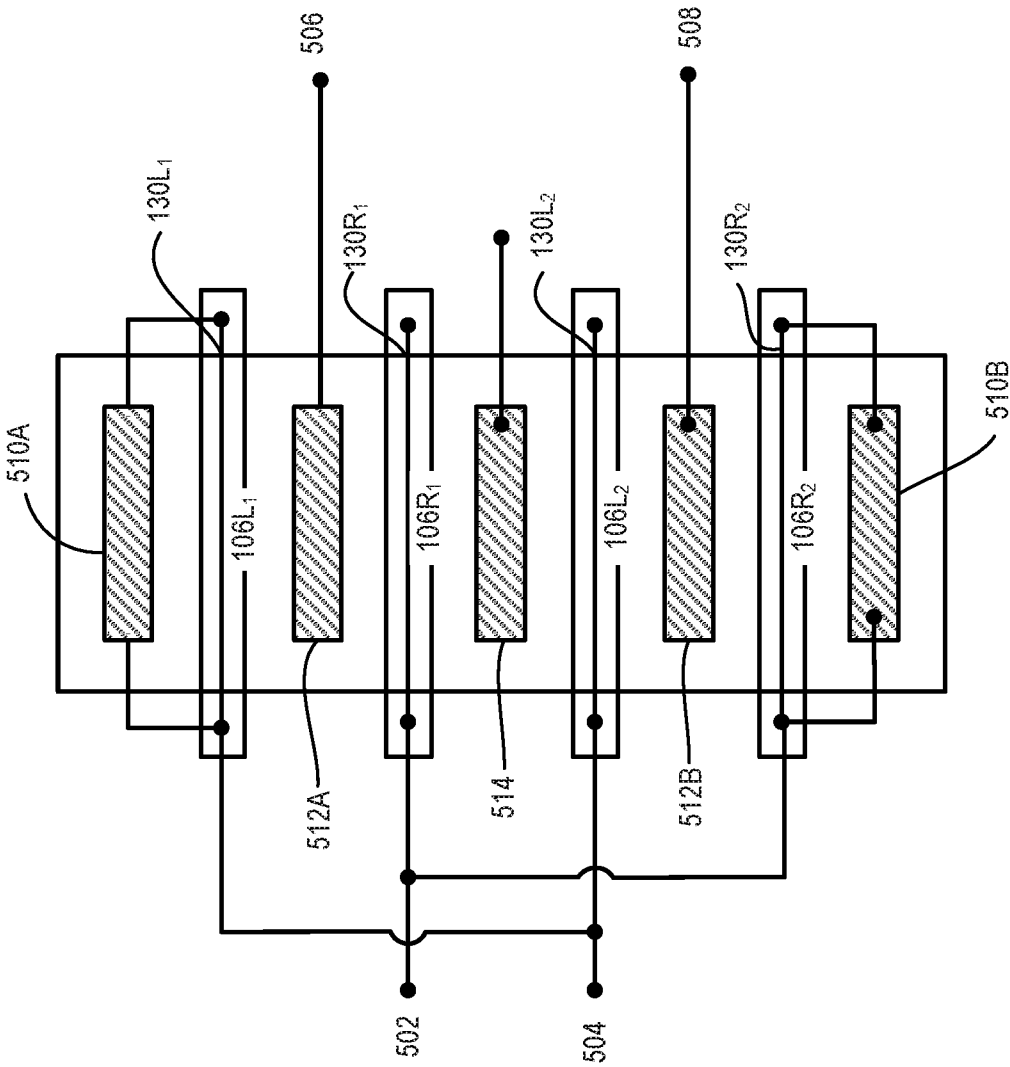


FIG 5A

500B

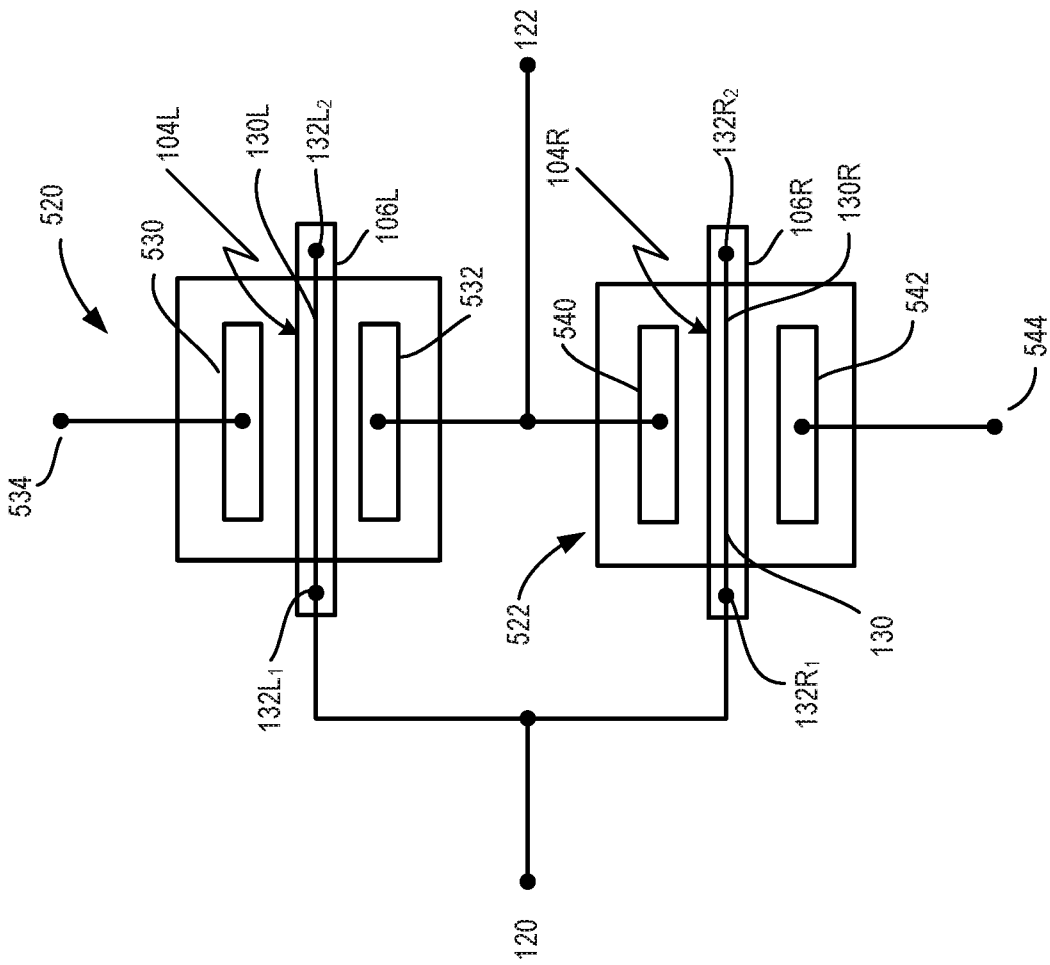


FIG 5B

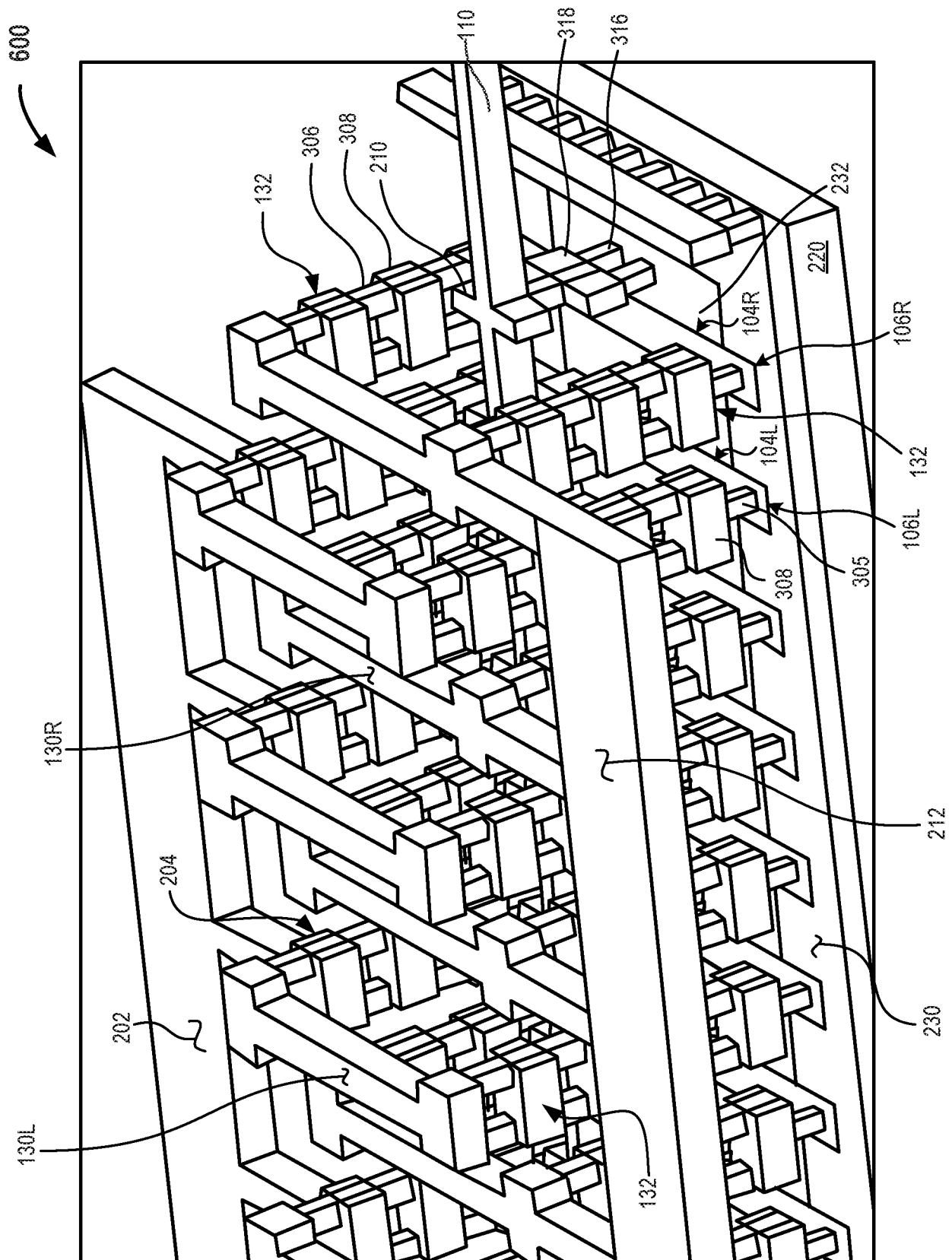


FIG 6

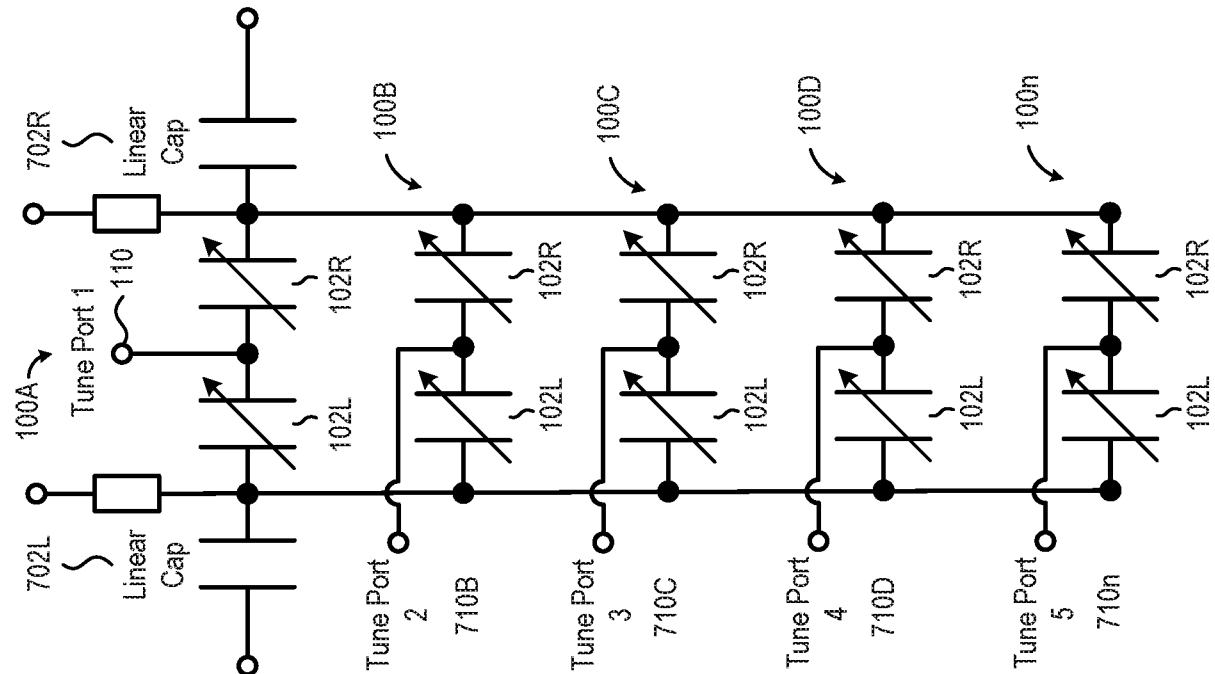


FIG 7B

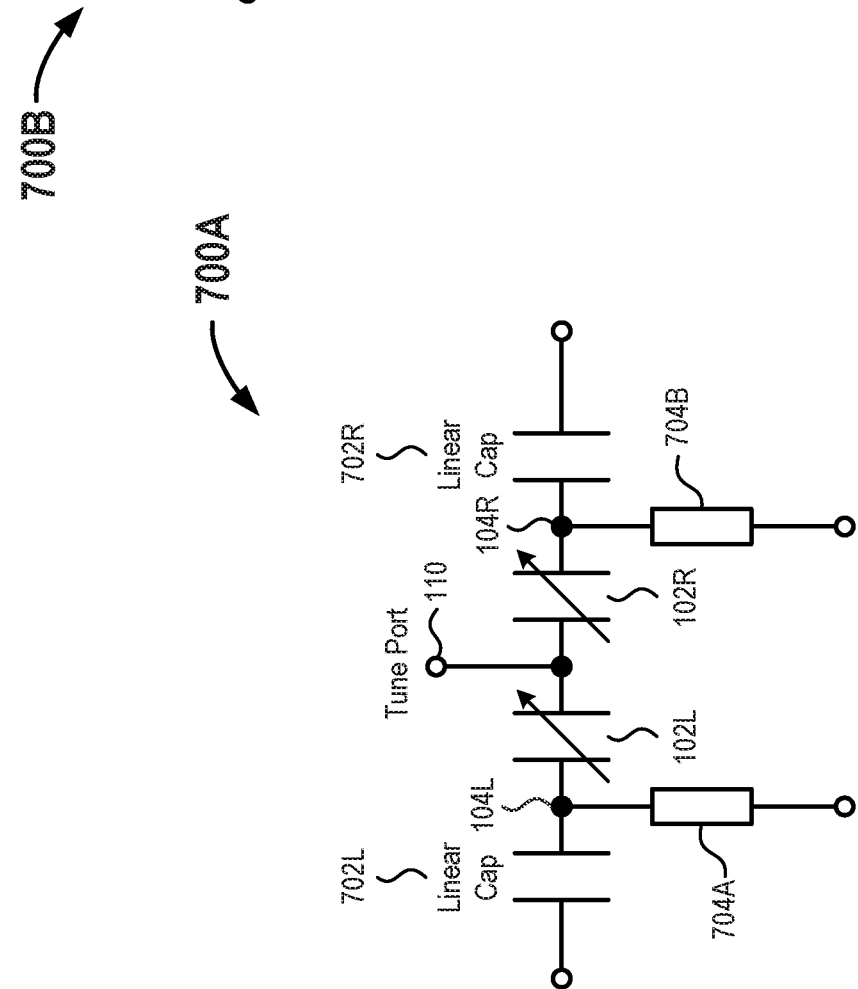


FIG 7A

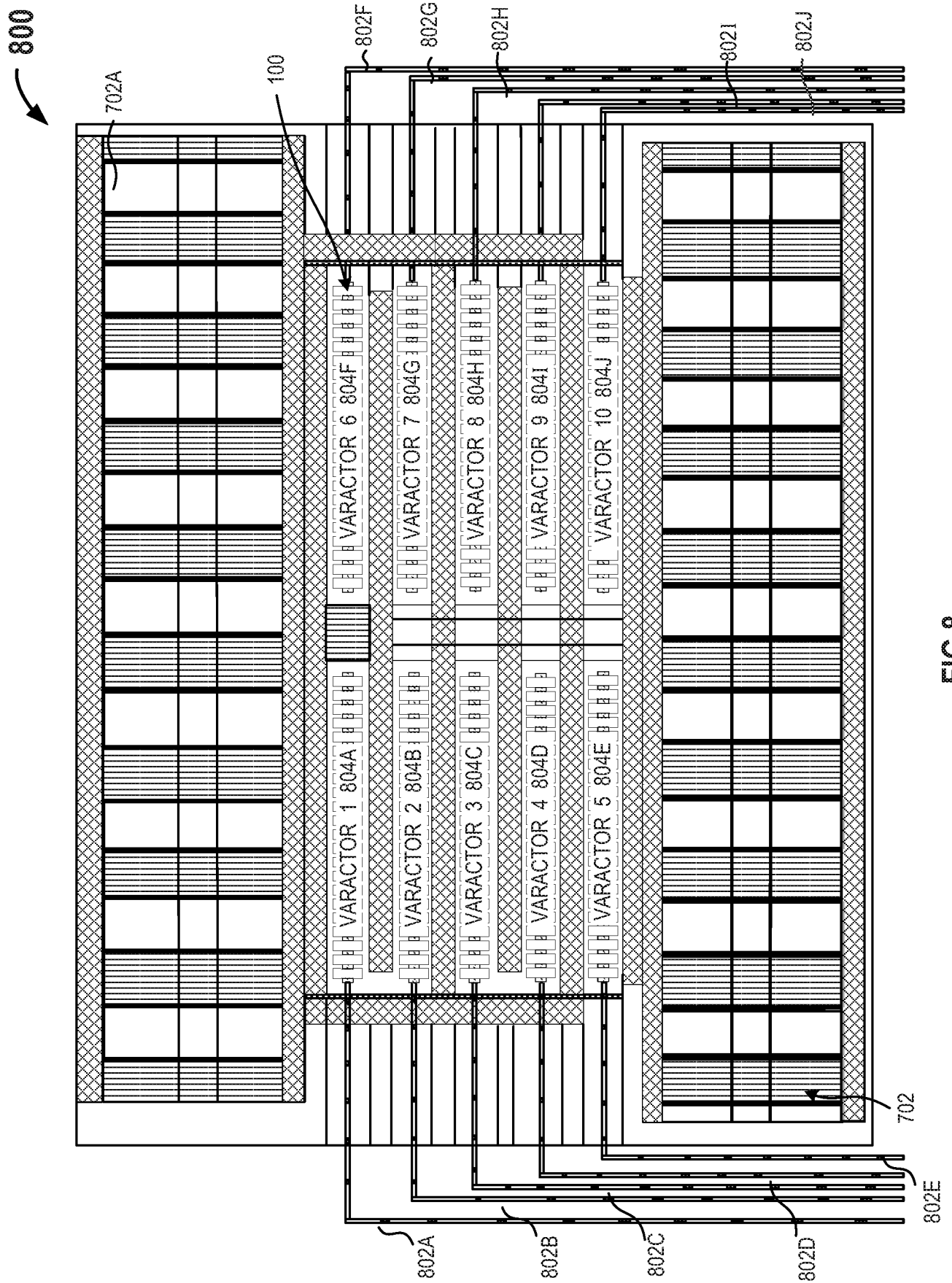


FIG 8

900

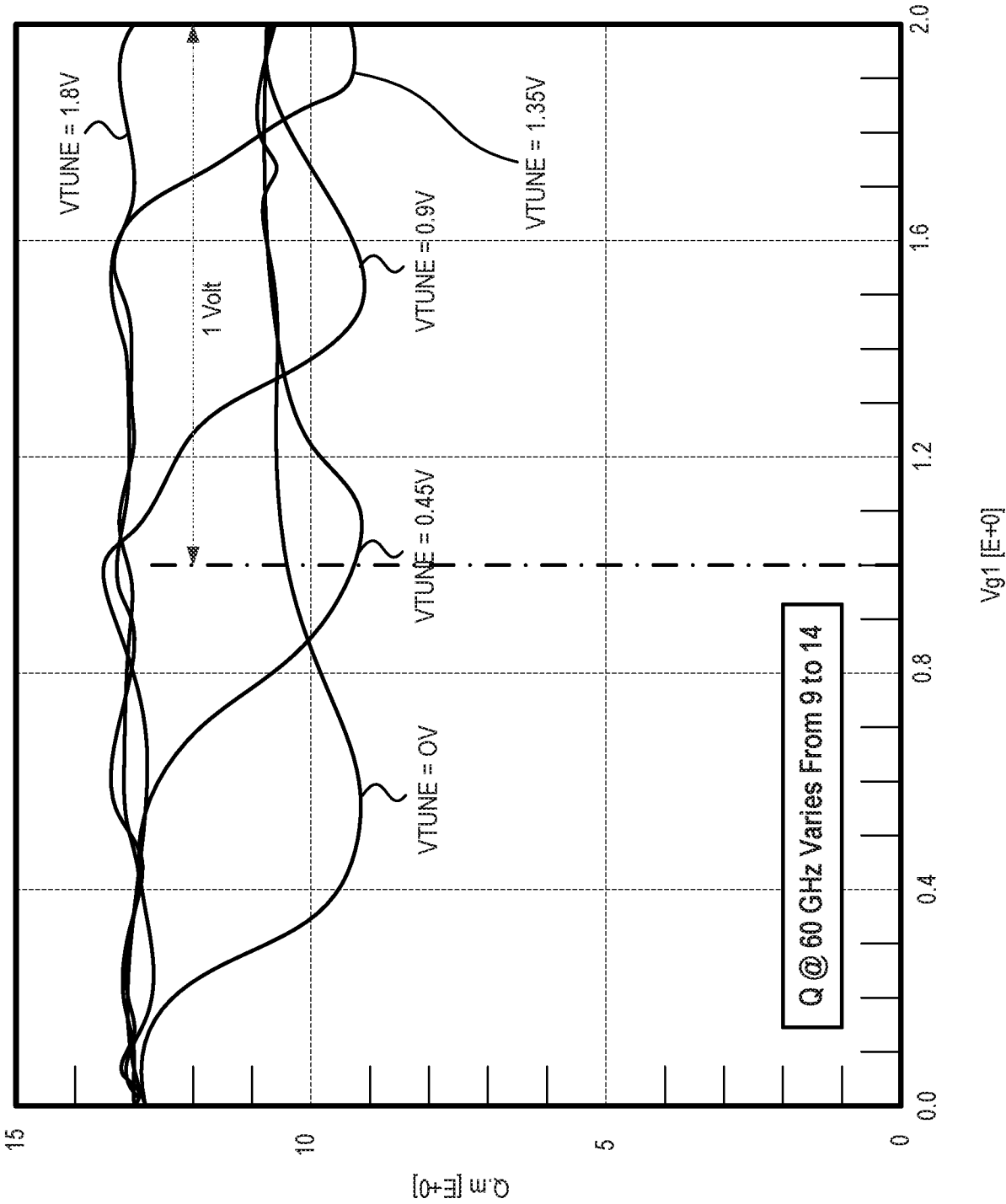


FIG 9

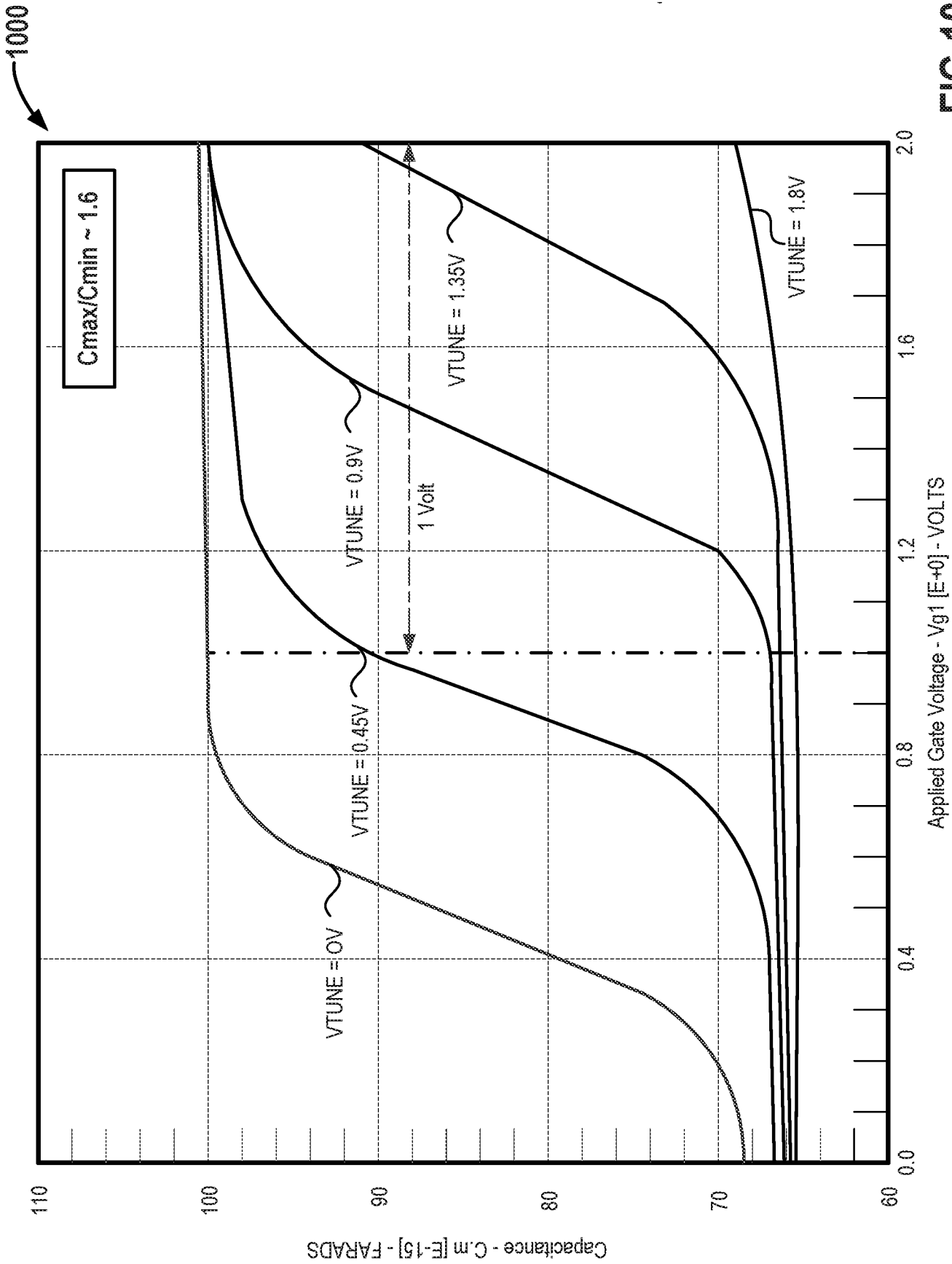


FIG 10

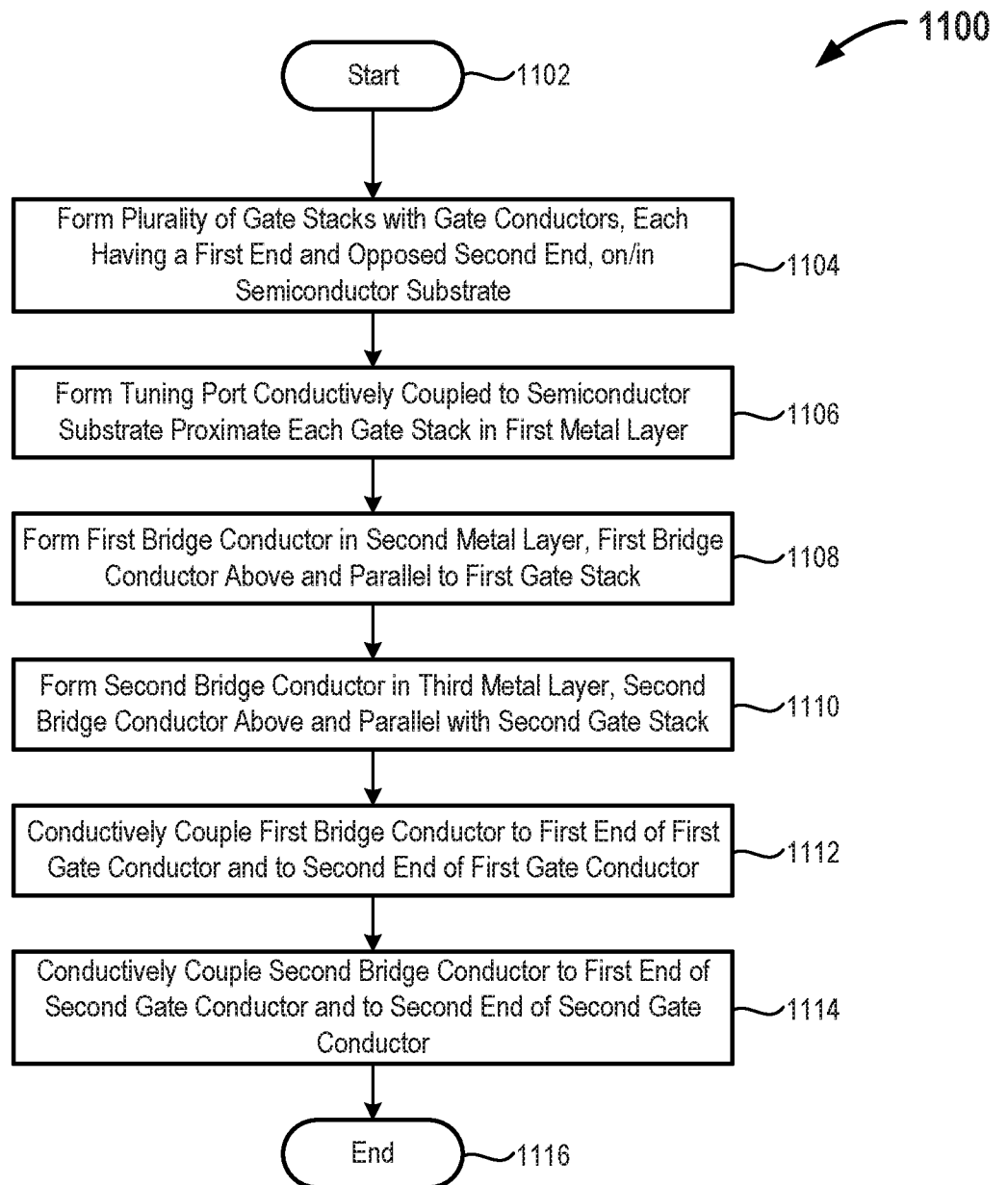


FIG 11

1200

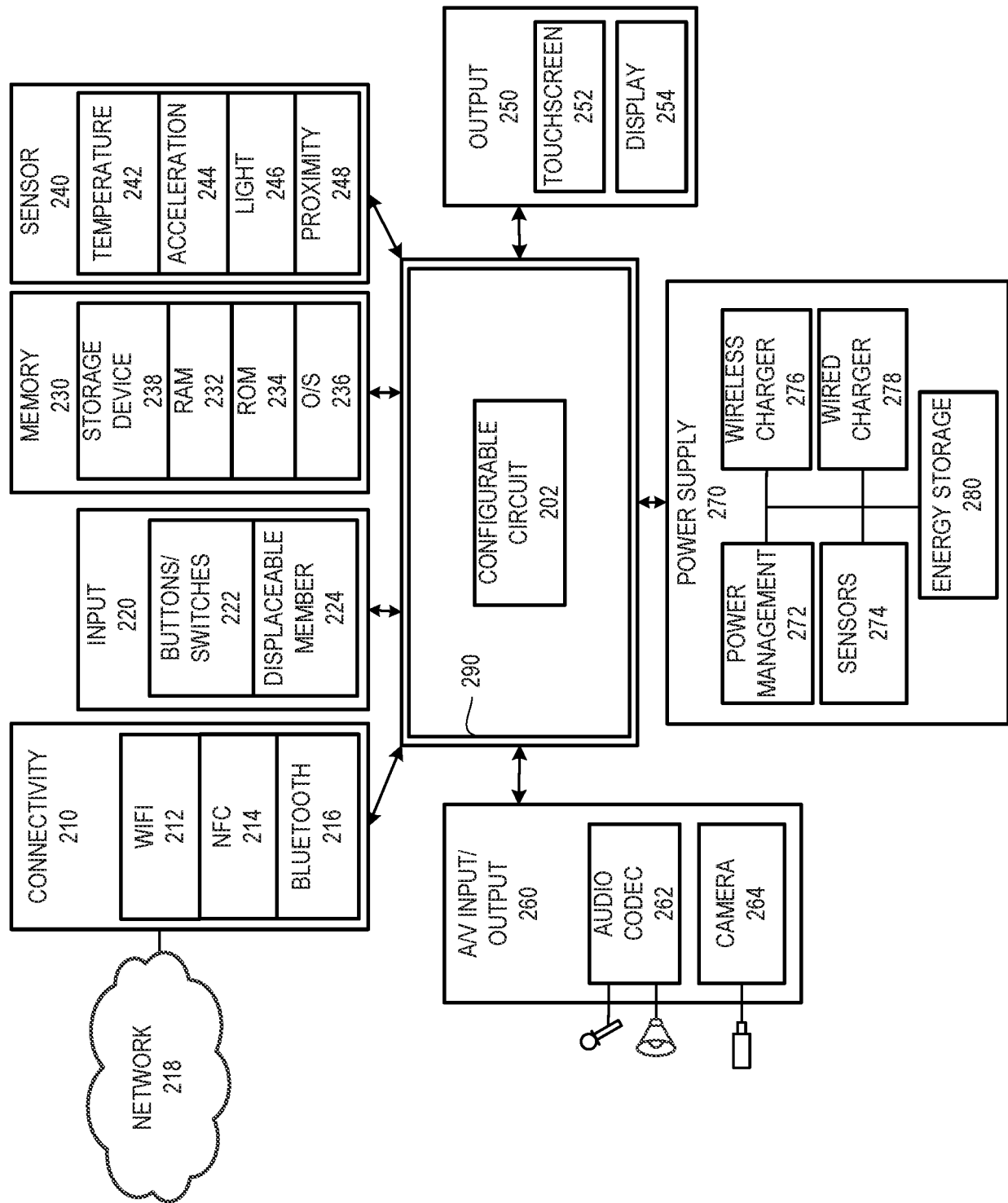


FIG 12

A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/93(2006.01)i, H03B 5/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/93; H01L 27/088; H01L 21/329; H01L 29/66; H03B 5/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: differential varactors ,bridge conductor, improve, Q-factor, parallel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0009228 A1 (YUE-SHIUN LEE et al.) 10 January 2013 See paragraphs [0026]-[0029 and figures 1-2.	1-30
A	US 2014-0264628 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 September 2014 See paragraph [0019] and figures 2A-2B.	1-30
A	US 2009-0289329 A1 (ADAM H. PAWLIKIEWICZ et al.) 26 November 2009 See paragraphs [0014]-[0026] and figure 1.	1-30
A	US 2016-0079444 A1 (TRIQUINT SEMICONDUCTOR, INC.) 17 March 2016 See paragraphs [0053]-[0064] and figure 2b.	1-30
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Further documents are listed in the continuation of Box C.



See patent family annex.

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10 March 2017 (10.03.2017)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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