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(54) ANALOG TO DIGITAL CONVERSION

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German company of Berlin and Munich, Germany (Federal Republic), do hereby declare the invention, for which we

pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement—:

This invention relates to analog to digital conversion.

According to one aspect of the invention there is provided a method of converting an analog quantity into a digital quantity, comprising applying an analog signal representing said analog quantity to conversion circuitry which comprises integrating circuitry and which provides digital signals at the ends of successive conversion periods, wherein each conversion period comprises a first phase during which said analog signal is applied to a first integrator of said integration circuitry and a second phase, immediately succeeding said first phase, during which the content of the first integrator accumulated in said first phase, and the analog signal, are applied to a second integrator of said integration circuitry, and wherein the first phase of said conversion period a reference signal is temporarily applied to said second integrator for a period of time during which the second integrator is relieved of its content accumulated in the preceding conversion period and a counter counts pulses from a pulse generator to provide an indication of said content of said second integrator, and thus of said analog quantity, in said preceding conversion period.

According to a second aspect of the invention there is provided circuitry for use in converting an analog quantity into a digital quantity, comprising a first input for an analog signal to represent said analog quantity, a second input for receiving a reference signal, integration circuitry comprising first and second integrators coupled to said first input *via* respective first and second switch means, and timing means operable to control said switch means such that operation of the circuitry comprises successive conversion periods each of which comprises a first phase during which said first integrator is connected to said first input *via* said first switch means and a second phase, immediately succeeding said first phase, during which said second integrator is connected to said first input *via* said second switch means, the circuitry further comprising a pulse generator and a counter, the latter being provided in common for the two integrators and the pulse generator and the counter being arranged such that the counter will count pulses from said pulse generator during a period of time in which said reference signal is applied temporarily to said integration circuitry *via* a third switch means coupling said second input to said integration circuitry.

By the use of two integrators, it is possible to apply the analog signal alternately to the integrators and to apply the reference signal to one of the integrators in a time interval in which the analog signal is not applied to this particular integrator.

The conversion result obtained in each integrator may be arranged to relate to a fixed integration time for the analog signal. In this case, due to the effective addition of the two conversion results in the common counter the total conversion result will also relate to a fixed integration time.

The reference signal may be isolated from the second integrator synchronously with the pulse succeeding the passage through zero of the output signal of the second integrator, and by applying the residual signal set up at this integrator to the other integrator. Since the zero point of the output signal of the second inte-

grator generally does not coincide with a pulse from the pulse generator, quantising errors would otherwise arise at a cut-off which is synchronous with the zero crossing point.

In accordance with a further development, the output of the first integrator is applied to the second integrator in addition to the analog signal during the second phase of the conversion period, and the input of the first integrator is brought to zero by negative feedback of its output signal during this phase, the reference signal being applied only to the second integrator during the first phase of the conversion period. In this mode of carrying the invention into effect, the output signal of the first integrator is not de-integrated or reduced with the aid of the reference signal, but is fed into the second integrator. In this way, the output signal of the second integrator corresponds to the integral of the analog signal over the whole conversion period. It is also possible with this mode of applying the invention to improve the conversion accuracy by cutting-off the reference signal synchronously with the pulse succeeding the passage through zero of the output signal of the second integrator and by transferring the resultant residual signal into the integration process of the next conversion period.

The cost of components can be kept low by applying the output signal of the first integrator to an inverting output thereof and to an inverting input of the second integrator, to which second integrator the analog signal is simultaneously applied *via* a non-inverting input. By the use of an inverting first integrator, the negative feedback is achieved by means of a simple short-circuiting between the output and the inverting input of this integrator.

The effect of internal errors on the accuracy of the conversion result may be reduced in accordance with a further development by virtue of the fact that auxiliary voltages are applied to the integrators for drift compensation. It is particularly advantageous for the auxiliary voltages applied for drift compensation to be automatically adjusted in such manner that the output signal of the respective integrator remains constant when the zero signal is present at its input. By means of the automatic adjustment of the auxiliary voltage, the effect of internal errors may be reduced even when the conditions of use of the integrators vary. The automatic adjustment of the auxiliary voltage is preferably achieved by means of a controller to which the rate of change of the output signal of the respective integrator or a quantity proportional to this rate of change is applied as actual value, and zero as desired value, the desired and actual values being periodically applied-to and cut-off from the controller during a conversion period, and the manipulated variable remaining effective with the aid of a store throughout the conversion period.

For a better understanding of the invention and to show how it may be put into effect reference will now be made, by way of example, to the accompanying drawing, the single figure of which shows analog-to-digital circuitry which is, and which operates, in accordance with the invention.

The illustrated circuit arrangement comprises a first integrator having an inverting input (−) and a second integrator 2 having an inverting input (−) and a non-inverting input (+). Connected to the output of the second integrator 2 is a comparator 3 which has two outputs, at one of which a signal appears in dependence upon the polarity of the output signal of the second integrator 2. The two outputs of the comparator 3 are connected to the forward and backward counting control inputs respectively of a counter 4. Depending upon which output of the comparator 3 carries a signal, the counter 4 is switched to forward or backward counting. The counting input of the counter 4 is connected to an AND stage 5.

There are also connected to the outputs of the comparator 3 two inputs of a control stage 6 which monitors the polarity of the output signals of the comparator 3. The control stage 6 has an output which carries a signal on change of polarity of the comparator output signals and which is connected to a stop input of the counter 4.

The circuit arrangement further comprises a pulse generator 7 which is connected to a timing signal generator 8 having two outputs 8*a* and 8*b*. The output 8*a* carries a signal during a first phase of a conversion period and the output 8*b* carries a signal during a second phase of the conversion period. The total duration of the two phases corresponds to the duration of a conversion period. The output 8*a* is connected to one input of the AND stage 5. The other input of the AND stage is connected to the output of the pulse generator 7. Consequently, pulses from the pulse generator 7 can reach the counter 4 during the time when the output 8*a* of the timing signal generator 8 is carrying a signal.

By means of an output signal present at the output 8*a* of the timing signal generator 8, a first switching element 9 is actuated, by which an analog signal U_X representing an analog quantity is applied to the inverting input of the first integrator 1. Also by means of the output signal of the output 8*a*, the comparator 3 is set into operation. The output signal of the output

8*b* controls switching elements 10, 11 and 12, the analog signal U_X being applied through switching element 10 to the non-inverting input of the second integrator 2, the output of the first integrator 1 being connectable to its own interting input by way of the switching element 11, and the output of the first integrator 1 being connectable to the inverting input of the second integrator 2 by way of the switching element 12. Also, a switching element 13 is provided which is desirably constructed as a change-over device. The switching element 13 can be connected either to the inverting input or to the non-inverting input of the second integrator 2 in dependence upon an output signal from the control stage 6, depending upon the polarity of the output signal from the comparator 3, whereby a reference quantity U_R may be applied to the corresponding input of the second integrator 2.

In addition, a control circuit 14 is connected to the first integrator 1 and a control circuit 15 to the second integrator 2. The control circuits 14 and 15 supply auxiliary voltages for the drift compensation of the two integrators 1 and 2. Switching devices for connecting the control circuits 14 and 15 to the integrators 1 and 2 respectively are not specifically shown in the drawing. Such switching devices may in fact be incorporated in the integrators 1 and 2 themselves.

The circuit arrangement operates as follows: Initially in a conversion period the output 8*a* of the timing signal generator 8 carries a control signal, by means of which the first switching element 9 is closed and applies the analog signal U_X to the inverting input of the first integrator 1. In addition, the switching element 13 is connected either to the inverting input or to the non-inverting input of the second integrator 2, depending upon the polarity of the output signal of the second integrator 2. Consequently, the reference signal U_R is present at the corresponding input of the second integrator 2. Also, by means of the control signal at the output 8*a* of the timing signal generator 8, the pulses from the pulse generator 7 are passed through the AND stage 5 to the counter 4. By means of the output signal of the comparator 3, the counter 4 is switched either to forward or backward counting.

When the switching element 9 is closed, the analog signal U_X is integrated in the first integrator 1. On application of the reference signal U_R to the second integrator 2, the content of the latter from the preceding conversion period starts to be deintegrated or reduced. Simultaneously with the application of the refernece signal U_R to the second integrator 2, the counter 4 has been started by the control signal at the output 8*a* of the timing signal generator 8.

As soon as the output signal of the second integrator 2 has been reduced to zero, a polarity change of the output signal of the comparator 3 takes place in synchronism with the next pulse from the pulse generator 7. Such a polarity change results in an output signal from the control stage 6, whereby the counter 4 is stopped. The digital counter reading reached is thus a measure of the analog signal associated with said preceding conversion period. Simultaneously with the stopping of the counter 4, the reference signal U_R is cut-off from the input of the integrator 2. Since the counter 4 is not stopped instantly when the output signal of the integrator 2 becomes zero, but only at the pulse succeeding the zeroising, a residual signal remains at the output of the second integrator 2. This residual signal is included in the next integrating action in order to avoid inaccuracies. In an embodiment which is not illustrated, this residual signal could be applied to the first integrator 1.

After a predetermined period of time, the control signal vanishes at the output 8*a* of the timing signal generator 8, whereby the first phase of the conversion period is terminated. Immediately thereafter, a control signal appears at the output 8*b*, whereby the second phase of the conversion period commences. With the disappearance of the control signal at the output 8*a*, the switching element 9 is opened and the analog quantity U_X is thus isolated from the first integrator 1. By means of the control signal at the output 8*b*, the switching element 10 is closed and the analog quantity U_X is applied to the non-inverting input of the second integrator 2. In addition, the output signal of the first integrator 1 is negatively fed back to its inverting input through the switching element 11 and is also applied through the switching element 12 to the inverting input of the second integrator 2. The control of the switching elements 10, 11 and 12 by the timing signal generator 8 is indicated by a chain line between these switching elements and the output 8*b* of the timing signal generator 8.

During the second phase of a conversion period, the analog quantity U_X is integrated by the second integrator 2. Simultaneously, the second integrator 2 takes up *via* the switching element 12 that value of the analog quantity U_X which has been integrated by the first integrator 1 in the first phase of the conversion period.

At the end of the second phase, therefore, the output signal of the second integrator 2 corresponds to the integral of the

analog quantity U_X over a complete conversion period. At the end of the second phase, the control signal at the output 8*b* of the timing signal generator 8 disappears and the switching elements 10, 11 and 12 are opened again. At the same time, a control signal appears at the output 8*a*, whereby the first pulse of the next conversion period is initiated.

By the use of the first integrator 1 and of the second integrator 2, it is possible continuously to integrate the analog quantity U_X and nevertheless to effect a drift compensation at the integrators 1 and 2. This is possible because there exists for each of the integrators 1 and 2 in one of the two phases of a conversion period a period of time in which the respective integrator is not operative. In the case of the first integrator 1, this occurs during the second phase of a conversion period after the zeroising of its input signal by the negative feedback of its output signal, and in the case of the second integrator 2 during the first phase of a conversion period after the de-integration or reduction of its output signal to zero. During this period of time in which the respective integrator is not operative, the rate of change of its output signal or a quantity proportional to this rate of change is measured at its output. In accordance with this measured quantity, there is set up in the respective control circuit 14 or 15 an auxiliary voltage which is applied to the respective integrator 1 or 2 as a constant value during the time when the integrator is operative. In this way, the drift error is corrected both at integration and at de-integration or reduction, and hence high accuracy of the conversion result is attained. Due to the constantly repeated measurement of the rate of change of the output signal, any change in the drift error due to any influence is immediately detected and the auxiliary voltage is correspondingly adjusted.

In the described and illustrated circuitry the analog signal U_X is continuously monitored and the converted result is related to a fixed period of time, i.e. a conversion period.

WHAT WE CLAIM IS:—

1. A method of converting an analog quantity into a digital quantity, comprising applying an analog signal representing said analog quantity to conversion circuitry which comprises integrating circuitry and which provides digital signals at the ends of successive conversion periods, wherein each conversion period comprises a first phase during which said analog signal is applied to a first integrator of said integration circuitry and a second phase, immediately succeeding said first phase, during which the content of the first integrator accumulated in said first phase, and the analog signal, are applied to a second integrator of said integration circuitry, and wherein in the first phase of said conversion period a reference signal is temporarily applied to second integrator for a period of time during which the second integrator is relieved of its content accumulated in the preceding conversion period and a counter counts pulses from a pulse generator to provide an indication of said content of said second integrator, and thus of said analog quantity, in said preceding conversion period.

2. A method according to claim 1, wherein in each conversion period said reference signal is applied to said second integrator for a time which terminates in dependence upon the passage through zero of the output signal of the second integrator.

3. A method according to claim 2, wherein said time terminates in synchronism with the first pulse from said pulse generator immediately after said passage through zero, and the resulting residual signal at said second integrator is applied to the first integrator.

4. A method according to claim 1, wherein in the first phase of each conversion period the analog signal is applied to the first integrator and the reference signal is applied to the second integrator only, and in the second phase the analog signal is applied to the second integrator as is the output signal of the first integrator.

5. A method according to claim 4, wherein in said second phase the output signal of the first integrator, while being applied to the second integrator, is brought to zero by negative feedback across the first integrator.

6. A method according to claim 4 or 5, wherein in each conversion period the time for which said reference signal is applied to said second integrator terminates in dependence upon the passage through zero of the output signal of said second integrator.

7. A method according to claim 6, wherein said time terminates in synchronism with the first pulse from said pulse generator immediately after said passage through zero, and the resulting residual signal at said second integrator is transferred into the integration action of the next conversion period.

8. A method according to claim 5, or claim 6 or 7 when appended to claim 5, wherein in said second phase the output signal of the first integrator is applied to an inverting input thereof and to an inverting input of the second integrator, to which second integrator said analog signal is simultaneously applied *via* a non-

inverting input thereof.

9. A method according to any one of the preceding claims, wherein auxiliary voltages are applied to said integrators for drift compensation.

10. A method according to claim 9, wherein for each respective integrator the auxiliary voltage applied thereto for drift compensation is automatically adjusted in such manner that the output signal of the respective integrator remains substantially constant when there is a zero signal at its input.

11. A method according to claim 10, wherein the automatic adjustment of each respective one of the auxiliary voltages takes place by means of a control means to which there is applied as actual value to be controlled the rate of change of the output signal of the respective integrator or a quantity proportional to said rate of change and as desired value the value zero, these actual and desired values being periodically applied-to and cut-off from the control means during a conversion period, while the manipulated variable remains effective throughout the conversion period with the aid of a store.

12. Circuitry for use in converting an analog quantity into a digital quantity, comprising a first input for an analog signal to represent said analog quantity, a second input for receiving a reference signal, integration circuitry comprising first and second integrators coupled to said first input *via* respective first and second switch means, and timing means operable to control said switch means such that operation of the circuitry comprises successive conversion periods each of which comprises a first phase during which said first integrator is connected to said first input *via* said first switch means and a second phase, immediately succeeding said first phase, during which said second integrator is connected to said first input *via* said second switch means, the circuitry further comprising a pulse generator and a counter, the latter being provided in common for the two integrators and the pulse generator and the counter being arranged such that the counter will count pulses from said pulse generator during a period of time in which said reference signal is applied temporarily to said integration circuitry *via* a third switch means coupling said second input to said integration circuitry.

13. Circuitry according to claim 12 and comprising control circuitry, for said third switch means, coupled to one of said integrators and arranged to operate such that in each conversion period said second input will be connected *via* said third switch means to said one of said integrators and such that the time for which said second input is connected to said one integrator will be terminated by said third switch means in dependence upon the passage through zero of the output signal of said one integrator.

14. Circuitry according to claim 13, wherein said control circuitry is arranged to operate such that said time will terminate in synchronism with the first pulse from said pulse generator immediately after said passage through zero, and the resulting residual signal at said one integrator will be applied to the other integrator.

15. Circuitry according to claim 12, wherein said timing means is arranged to operate such that in the first phase of each conversion period said first input will be connected to the first integrator *via* said first switch means, said second input being connected to the second integrator only *via* said third switch means, and in the second phase said first input will be connected to the second integrator *via* said second switch means, there being fourth switch means arranged to be controlled by the timing means to connect the output of the first integrator to the input side of the second integrator in said second phase.

16. Circuitry according to claim 15, and comprising a fifth switch means connected in a negative feedback path from the output to the input of said first integrator, the fifth switch means being arranged to be controlled by said timing means to make said negative feedback path in said second phase.

17. Circuitry according to claim 15 or 16, and comprising control circuitry, for said third switch means, coupled to said second integrator and arranged to operate such that in a conversion period said second input will be connected to said second integrator *via* said third switch means and the time for which said second input is connected to said second integrator will be terminated by said third switch means in dependence upon the passage through zero of the output signal of said second integrator.

18. Circuitry according to claim 17, wherein said control circuitry is arranged to operate such that said time will terminate in synchronism with the first pulse from said pulse generator immediately after said passage through zero, and the resulting residual signal at said second integrator will be transferred into the integration action of the next conversion period.

19. Circuitry according to claim 16, or claim 17 or 18 when appended to claim 16, wherein said timing means is arranged to operate such that in said second phase said negative feedback path will be made by

said fifth switch means, said fourth switch means controlled by said timing means will be operated to connect the output of said first integrator to an inverting input of said second integrator, and said first input will be connected to a non-inverting input of said second integrator by operation of said third switch means.

20. Circuitry according to any one of claims 12 to 19, and comprising respective control means for applying to respective ones of said integrators auxiliary voltage for drift compensation.

21. Circuitry according to claim 20, wherein each of said control means is arranged to operate such that the auxiliary voltage supplied thereby will be automatically adjusted in such manner as to maintain substantially constant the output signal of the respective integrator when there is a zero signal at its input.

22. Circuitry according to claim 21, wherein said control means is arranged to produce a desired value of zero from, as actual value, either the rate of change of the output signal of the respective integrator or a quantity proportional to said rate of change, the control means being arranged such that these actual and desired values will be periodically applied-to and cut-off from the control means during a conversion period, while the manipulated variable remains effective throughout the conversion period with the aid of a store.

23. Circuitry according to claim 17 or any one of claims 18 to 22 when appended to claim 17, wherein said control circuitry is operable to control said third switch means to connect said second input either to the inverting or non-inverting input selectively of the second integrator in dependence upon the polarity of the output signal thereof.

24. A method of converting an analog quantity into a digital quantity substantially as hereinbefore described with reference to the single figure of the accompanying drawing.

25. Circuitry for use in converting an analog quantity into a digital quantity, substantially as hereinbefore described with reference to the single figure of the accompanying drawing.

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1578261 COMPLETE SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*