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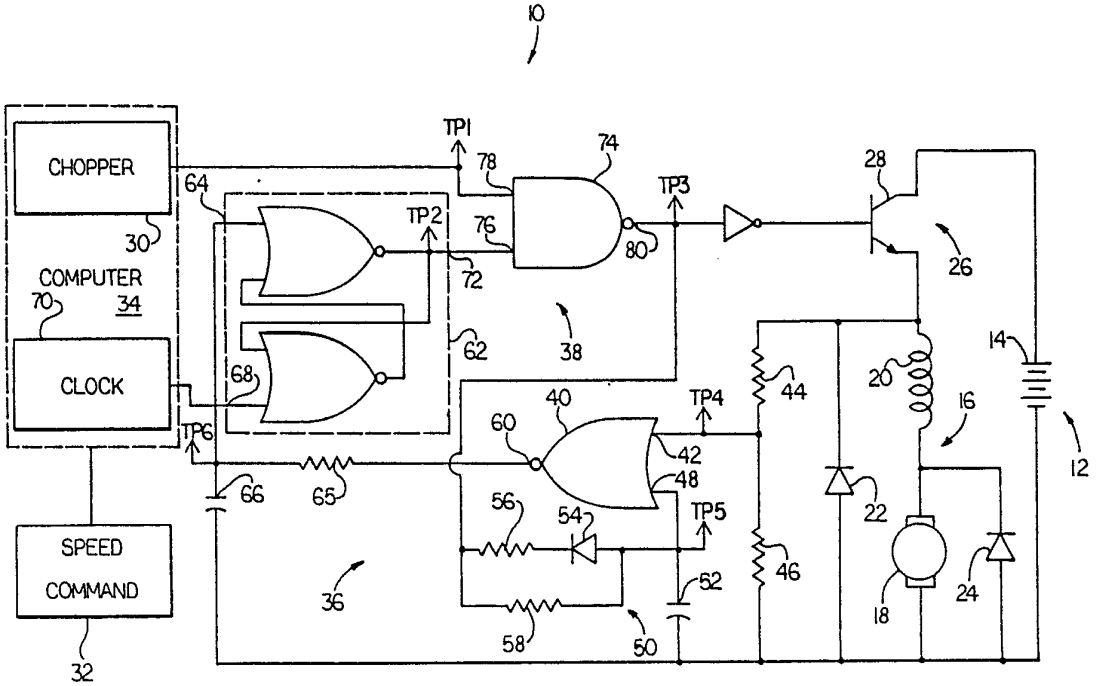

(57) Abstract

Motor control circuits having solid-state switching elements are commonly used on industrial vehicles such as lift trucks. A short circuit condition in the motor circuit can cause catastrophic failure of the semiconductor switching element. The instant invention detects such a short circuit condition and modifies the motor control signals supplied by a chopper circuit (30) to a switching element (26). The apparatus (10) includes a trigger circuit (36) for receiving the motor control signals and sensing a voltage across the motor (16) produced in response to electrical power delivered from a power supply (12).

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Description

Apparatus and Method For Protecting A Motor Control Circuit

Technical Field

This invention relates generally to an apparatus and method for detecting a shorted condition of an electrical circuit, and, more particularly, to an apparatus and method for protecting an electrical motor control circuit from damage caused by a shorted circuit component.

Background Art

Various motorized systems in use today include an electric motor powered by a battery or other source of electrical energy. The speed of the electric motor is commonly controlled by supplying power from the power source to the motor through a serially connected solid-state switching element. The switching element can be, for example, a transistor or silicon controlled rectifier. The switching element is typically pulse controlled by a signal chopper of conventional design.

In such systems, various circuit elements are commonly connected in parallel with the motor. A short circuit condition in one of these circuit elements can lead to excessive current flow through the switching element. Owing to the fact that such switching elements are designed for specific maximum current flows, the excessive current flow caused by a short circuit condition is likely to damage the switching element.

In a typical motor control circuit, the power source is connected through a transistor switching element to one side of the motor, with the other side

of the motor being connected to the opposite pole of the power source. A flyback diode is typically connected across the combined field and armature of the motor to form a circulating current path for motor current during the period of time that the switching element is turned "off". The flyback diode is subjected to particularly difficult operating conditions, and occasionally fails as a result of being overstressed during operation. A shorted flyback diode causes excessive current to flow from the power source, through the switching element and the shorted diode, back to the opposite pole of the power source. Such extreme magnitudes of current flow are known to quickly destroy the solid-state switching element.

It is desirable to sense the presence of such a short circuit condition and exercise appropriate control strategies in the event such a short circuit condition is detected. It is known, for example, to sense a short circuit condition by monitoring the magnitude of current flowing through a shunt in series with the motor in a meter control circuit, and to interrupt the flow of current in the event it becomes excessive. However, in some situations it is not desirable to interpose a current shunt in the motor control circuit, and in any event, a shunt in series with the motor cannot detect a shorted flyback diode. Likewise, it may be undesirable to shut down the motor control circuit permanently as it is possible that the short circuit condition is only temporary and that the motor control circuit can resume proper operation after a temporary interruption.

The present invention is directed to overcoming one or more of the problems as set forth above.

Disclosure of the Invention

In one aspect of the present invention, an apparatus for sensing a short circuit condition of a motor control circuit is provided. The apparatus includes a power supply for providing a source of electrical power, and a motor connected across the power source. A chopper controllably produces motor control signals. A switching element receives the motor control signals and responsively delivers electrical power from the power source to the motor. The switching element is serially connected between the motor and the power source. A trigger circuit also receives the motor control signals, senses a voltage across the motor produced in response to the delivered electrical power, and controllably produces a trigger signal in response to receiving the motor control signals and failing to sense the produced motor voltage. An inhibit circuit controllably modifies the motor control signals in response to receiving the produced trigger signal.

In a second aspect of the present invention, a method for sensing a short circuit condition of a motor control circuit is provided. The motor control circuit includes a source of electrical power, a motor connected across the power source, a chopper circuit for controllably producing motor control signals, and a switching element for receiving the motor control signals and responsively delivering electrical power from the power source to the motor. The switching element is serially connected between the motor and the power source. The method comprises the steps of receiving the motor control signals and sensing the voltage across the motor produced in response to the delivered electrical power. In response to receiving the motor control signals and failing to sense the

produced motor voltage, a trigger signal is produced, and the motor control signals are controllably modified in response to the trigger signal.

The present invention provides a fast reacting circuit for protecting a motor control. The circuit advantageously requires no serial current measuring device in the motor circuit, and is capable of discriminating between a continuous short circuit condition and a temporary short circuit condition.

Brief Description of the Drawings

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

Fig. 1 is a schematic diagram of a motor control system incorporating an embodiment of the present invention; and

Figs. 2 and 3 are illustrative waveforms used to explain the operation of the circuit shown in Fig. 1.

Best Mode For Carrying Out the Invention

Referring first to Fig. 1, an apparatus embodying certain of the principles of the present invention is generally indicated by the reference numeral 10. It should be understood that the following detailed description relates to the best presently known embodiment of the apparatus 10. However, the apparatus 10 can assume numerous other embodiments, as will become apparent to those skilled in the art, without departing from the appended claims.

The apparatus 10 includes a power supply means 12, for example, a battery 14, for providing a source of electrical power. A motor 16 having an armature 18 and a field 20 is connected across the power supply means 12. The motor 16 is, for example, a pump motor

used to operate an hydraulic pump in an industrial vehicle such as a lift truck. A flyback diode 22 is connected across the series combination of armature 18 and field 20. Some motor circuits also include a plugging diode 24 connected across the motor armature 18.

A switch means 26 is serially connected between the power supply means 12 and the motor 16. The switch means 26 is preferably a solid-state switch, for example, a high power transistor 28, having a collector connected to one terminal of the power supply means 12 and an emitter connected to the motor 16. A chopper means 30 controllably produces motor control signals, for example, a time modulated pulse train signal. The pulse modulated motor control signals are ultimately delivered from the chopper means 30 to a base terminal of the transistor 28.

In a typical embodiment, a speed command is supplied to the chopper means 30 from a speed command means 32. The time modulated motor control signals are produced responsive to the speed command signal, and the switch means 26 is responsively turned on and off to vary the speed of the motor 16. In the preferred embodiment, the chopper means 30 is an integral part of a computer 34. It is known in the art to produce time modulated signals utilizing a microprocessor or other form of computer in this manner. It is also known to provide equivalent chopper means via conventional hard wired circuitry.

A trigger means 36 receives the motor control signals, senses a voltage across the motor 16 produced in response to the delivered electrical power, and controllably produces a trigger signal in response to receiving the motor control signals and to failing to sense the produced motor voltage. An inhibit means 38 then controllably modifies the motor control signals in

response to receiving the trigger signal. The trigger means 36 includes a first logic gate 40. The logic gate 40 has a first input terminal 42 connected through a resistor 44 to the junction of the switch means 26 and the motor 16. A second resistor 46 is connected from the first input terminal 42 of the first logic gate 40 to circuit ground.

The first logic gate 40 also has a second input terminal 48 connected through a time delay circuit 50 to the inhibit means 38. The time delay circuit 50 includes a capacitor 52 connected from the second input terminal 48 to circuit ground. A diode 54 is also connected to the second input terminal 48 and is connected in series with a resistor 56. The combination of the diode 54 and resistor 56 are connected in parallel with a resistor 58. Finally, the first logic gate 40 has an output terminal 60. The first logic gate 40 is, for example, a two input NOR gate of conventional design.

The inhibit means 38 includes a latch 62. In the preferred embodiment, the latch 62 is an R/S flip-flop composed of dual cross-coupled NOR gates. A first input terminal 64 of the latch 62 is connected to the output terminal 60 of the first logic gate 40 through a resistor 65, and is also connected through a capacitor 66 to circuit ground. A second input terminal 68 is connected to a clock means 70. The clock means 70 periodically produces a reset signal, and the inhibit means 38 ceases to modify the mode of control signals in response to receiving the clock signal in the absence of the trigger signal. The clock means 70 is, for example, a portion of the microprocessor 34. The clock means 70 can also be implemented as an individual hard wired circuit. The latch 62 also includes an output terminal 72.

The inhibit means 38 also includes a second logic gate 74 having a first input terminal 76 connected to the latch output terminal 72. A second input terminal 78 is connected to the chopper means 30, and an output terminal 80 is connected to the base of the switch means 26 and to the second input terminal 48 of the first logic gate 40 through the time delay circuit 50. The second logic gate 74 is, in the preferred embodiment, a two input NAND gate of conventional design.

The ratings and values discussed above with respect to the various electrical elements are for exemplary purposes only. Alterations of the circuit and the use of electrical elements of different constructions or ratings will be readily apparent to those skilled in the art. Such alterations or substitutions can be implemented without departing from the appended claims.

Industrial Applicability

Operation of the instant invention is best described in conjunction with its use in a typical industrial application, for example, in association with an hydraulic pump motor of an industrial lift truck. The speed requirements of such a pump motor typically vary according to the functions being performed at any point in time by the hydraulic circuitry. For example, power steering requires a relatively low pump motor speed as opposed to elevation of the mast which can require a relatively fast motor speed. The variety of different motor speeds is typically controlled by a chopper control circuit, for example, the chopper means 30, which produces a time duration modulated pulse control signal in a conventional manner. This pulse control signal is

utilized to rapidly switch "on" and "off" a switching element, for example, the switch means 26. Responsively, power is delivered from a power supply to the motor in a series of current pulses, with the mean power delivered over a period of time determining the speed at which the motor operates.

A plurality of test points, labeled TP1-TP6, are indicated on the schematic diagram of Fig. 1. Representative waveforms found at each of these test points under various operating conditions are set forth in Figs. 2 and 3. In the case of waveforms representing signals at points in the circuit having significant reactance, for example TP4-TP6, the actual DC waveforms are omitted and only the logic switching waveforms are shown for clarity and ease of understanding. The exact switching voltage of the various logic components varies with the components selected, and for this discussion is assumed to be approximately 50% of the supply voltage. Reference to the waveforms and to Fig. 1 throughout the following discussion will be of value.

The waveforms of Fig. 2 are representative of a normal operating condition of the chopper and motor circuit. Motor control signals produced by the chopper means 30 are delivered to the second logic gate 74 at the second input terminal 78. This is depicted at TP1 in Fig. 2. These motor control signals are normally delivered to the switch means 26, as seen at TP3. The motor control signals are readily transferred through the second logic gate 74 so long as the signal at TP2 is "high" throughout the period that the motor control signal at TP1 is "high".

The signal at TP3 is also delivered through the time delay means 50 to the second input terminal 48 of the first logic gate 40, as shown at TP5. The

signal at the first input terminal 42 of the first logic gate 40, as shown at TP4, is responsive to the voltage developed across the motor 16 and its parallel connected circuit components, for example, the flyback diode 22. The voltage magnitude of the signal at TP4 is reduced by the voltage divider comprised of a pair of resistors 44,46. This voltage divider is a level shifting device for producing a suitable logic level signal from the voltage present across the motor 16. The value of the resistors 44,46 is selected to deliver a logic "high" signal at TP4 in response to substantially full battery voltage across the motor 16, and a logic "low" signal in response to less than substantially full battery voltage across the motor 16. So long as both input terminals 42,48 of the first logic gate 40 are not simultaneously "low", the output terminal 60 remains "low" at TP6, and the latch 62 is not set. Owing to the reset signal being produced by the clock means 70 and periodically delivered to the reset terminal 68 of the latch 62, the latch 62 is maintained in the reset condition, and the output signal delivered to the second logic gate 74 remains "high".

The reset signal is delivered from the clock means 70 at periodic intervals of, for example, 10 milliseconds. In the preferred embodiment, the motor 16 is pulsed at a maximum rate of 7800 hertz. Assuming a minimum pulse duty factor of 8 microseconds, the 10 millisecond reset pulse insures that a short circuit condition is adequately protected against, while providing a reasonably short reset time interval.

Referring now to the waveforms shown in Fig. 3, a short circuit condition is described. In response, for example, to a shorted flyback diode 22, the resistance between the switching element 26 and

circuit ground is considerably reduced from normal operating conditions. Consequently, the voltage across the pair of voltage divider resistors 44,46 is reduced sufficiently to produce a logic "low" signal at the input terminal 42 of the first logic gate 40, shown at TP4. Responsively, the first logic gate 40 delivers a logic "high" signal to the first input terminal 64 of the latch 62. In turn, the latch 62 delivers a logic "high" signal to the first input terminal 76 of the second logic gate 74. This logic "high" signal interrupts or blocks the motor control signal from the chopper means 30 and prevents it from continuing to be delivered, at TP3, to the switch means 26. Therefore, the switch means 26 is turned "off" before the excessive current flowing through the shorted flyback diode 22 can damage the transistor 28 and associated components.

Periodically, for example, approximately every 10 milliseconds, a reset signal is delivered by the clock means 70 to the second input terminal 68 of the latch 62, and the motor control signal from the chopper means 30 is again delivered to the switch means 26. If the short circuit condition was temporary and no longer exists, circuit operation returns to normal and the waveforms shown in Fig. 2 again apply. However, assuming that the short circuit condition continues to exist, only a brief current pulse is supplied by the switch means 26 before the motor control signals are again inhibited by the second logic gate 74. Therefore, the apparatus 10 quickly detects a short circuit condition in the motor circuit and prevents damage to the switch means 26 and associated circuitry.

Other aspects, objects, advantages, and uses of this invention can be obtained from a study of the drawings, the disclosure, and the appended claims.

Claims

1. Apparatus (10) for sensing a short circuit condition of a motor control circuit, comprising:

power supply means (12) for providing a source of electrical power;

a motor (16) connected across said power supply means (12);

chopper means (30) for controllably producing motor control signals;

switch means (26) for receiving said motor control signals and delivering electrical power from said power supply means (12) to said motor (16) in response to said received motor control signals, said switch means (26) being serially connected between said motor (16) and said power supply means (12);

trigger means (36) for receiving said motor control signals, sensing a voltage across said motor (16) produced in response to said delivered electrical power, and controllably producing a trigger signal in response to receiving said motor control signals and failing to sense said produced motor voltage; and

inhibit means (38) for controllably modifying said motor control signals in response to receiving said trigger signal.

2. Apparatus (10), as set forth in claim 1, including clock means (70) for periodically producing a reset signal, and wherein said inhibit means (38) ceases to modify said motor control signals in response to receiving said clock signal in the absence of said trigger signal.

3. Apparatus (10), as set forth in claim 2, wherein said trigger means (36) includes a first logic gate (40) having a first input terminal (42) connected

to the junction of said switch means (26) and said motor (16), a second input terminal (48) connected to said inhibit means (38), and an output terminal (60), and said inhibit means (38) includes a latch (62) having a first input terminal (64) connected to said first logic gate output terminal (60), a second input terminal (68) connected to said clock means (70), and an output terminal (72), and a second logic gate (74), having a first input terminal (76), connected to said latch output terminal (72), a second input terminal (78) connected to said chopper means (30), and an output terminal (80) connected to said switch means (26) and said first logic gate second input terminal (48).

4. Apparatus (10) for sensing a short circuit condition of a motor control circuit, comprising:

a battery (14) having first and second battery poles;

a transistor (28) having an emitter terminal, a base terminal, and a collector terminal connected to one of said battery first and second poles;

a motor (16) having a first motor terminal connected to the other of said battery first and second poles, and a second motor terminal connected to said transistor emitter terminal;

chopper means (30) for controllably producing motor control signals;

clock means (70) for periodically producing a reset signal;

a first logic gate (40) having a second input terminal, an output terminal, and a first input terminal (42) connected to said transistor emitter terminal;

a latch (62) having an output terminal, a first input terminal (64) connected to said first logic gate output terminal (60), and a second input terminal (64) connected to said clock means (70); and

a second logic gate (74) having a first input terminal (76) connected to said latch output terminal (72), a second input terminal (78) connected to said chopper means (30), and an output terminal (80) connected to said transistor base terminal and said first logic gate second input terminal (48).

5. A method for sensing a short circuit condition of a motor control circuit, said motor control circuit including a source of electrical power (12), a motor (16) connected across said power source (12), chopper means (30) for controllably producing motor control signals, and switch means (26) for receiving said motor control signals and responsively delivering electrical power from said power source (12) to said motor (16), said switch means (26) being serially connected between said motor (16) and said power source (12), comprising the steps of:

receiving said motor control signals;

sensing the voltage across said motor (16) produced in response to said delivered electrical power;

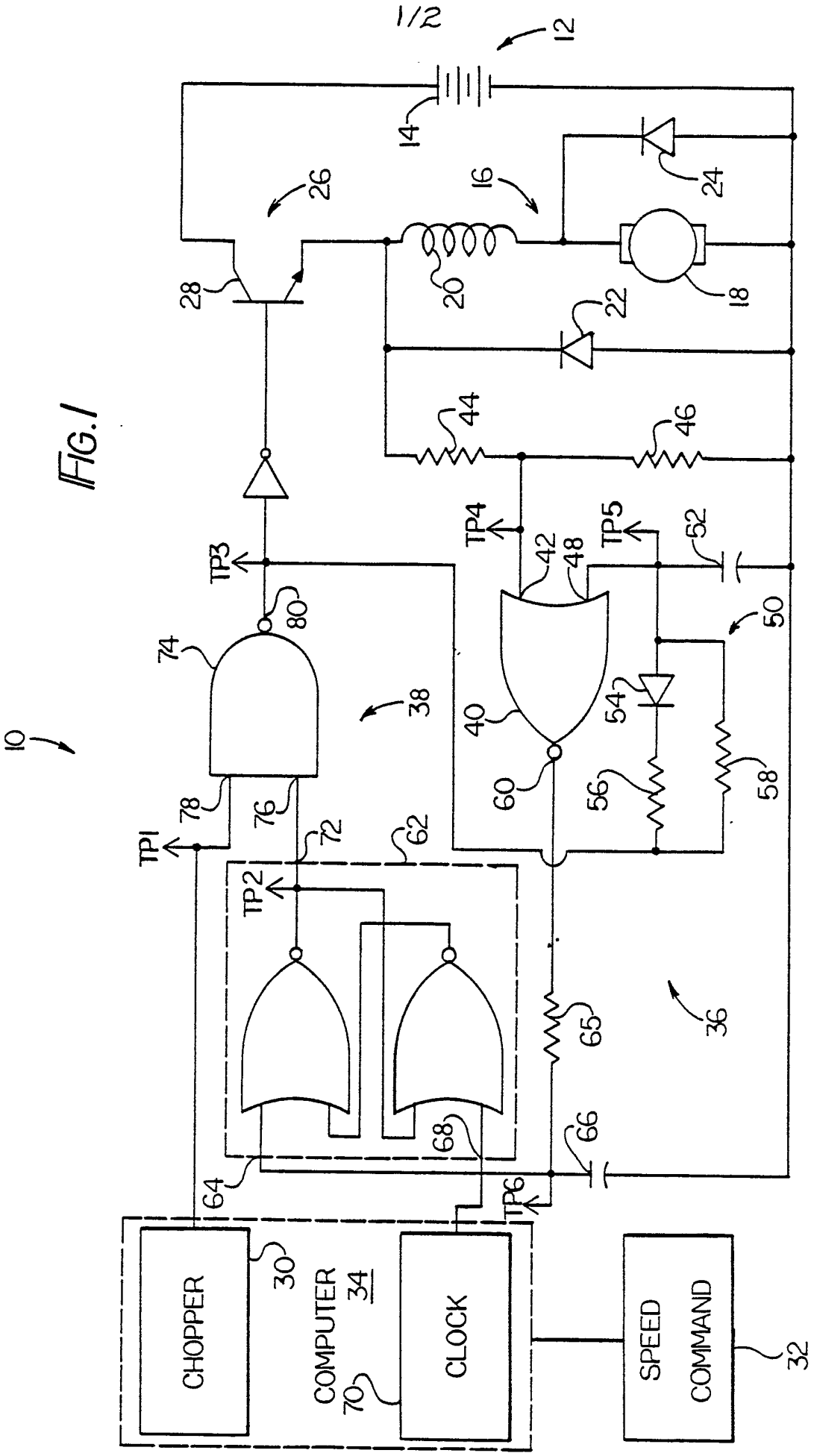
controllably producing a trigger signal in response to receiving said motor control signals and failing to sense said produced motor voltage; and

controllably modifying said motor control signals in response to said trigger signal.

6. A method, as set forth in claim 5, including the steps of:

periodically producing a reset signal; and

ceasing to modify said motor control signals in response to receiving said reset signal in the absence of said trigger signal.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TP1
TP2
TP3
TP4
TP5
TP6
CHOPPER
COMPUTER
CLOCK
SPEED COMMAND

FIG. 1

FIG.2
(NORMAL OPERATION)

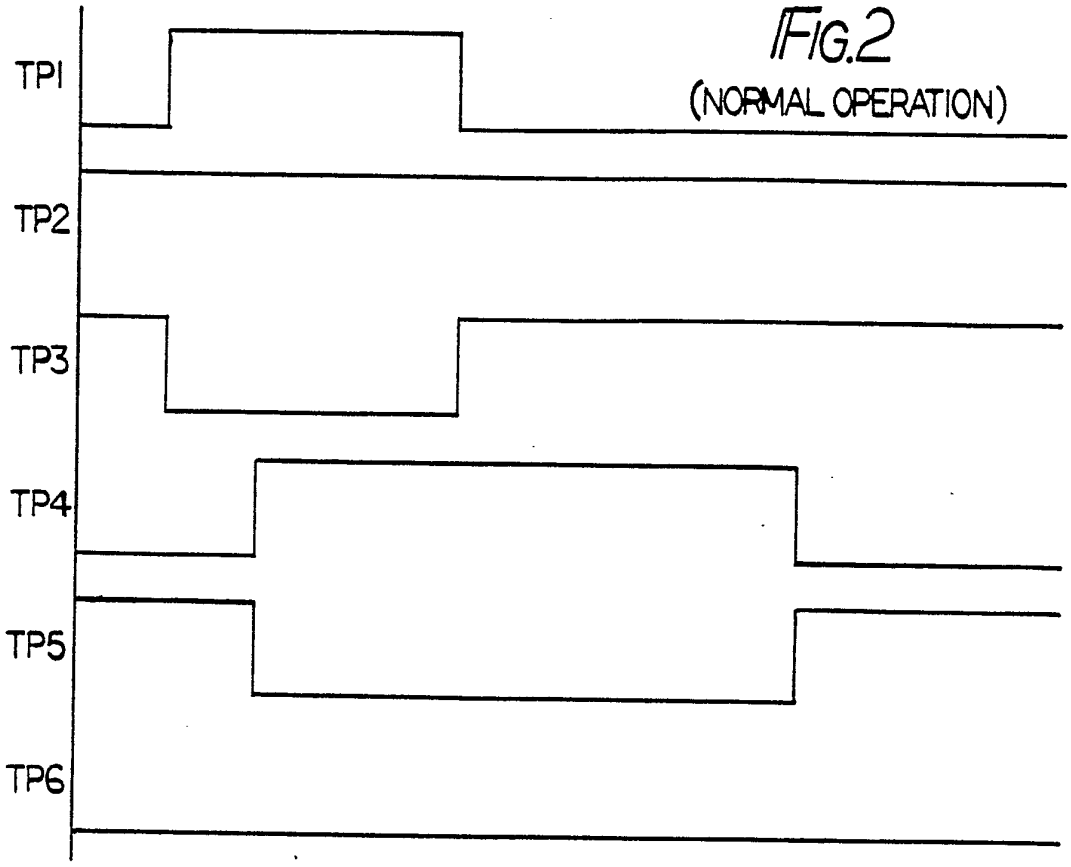
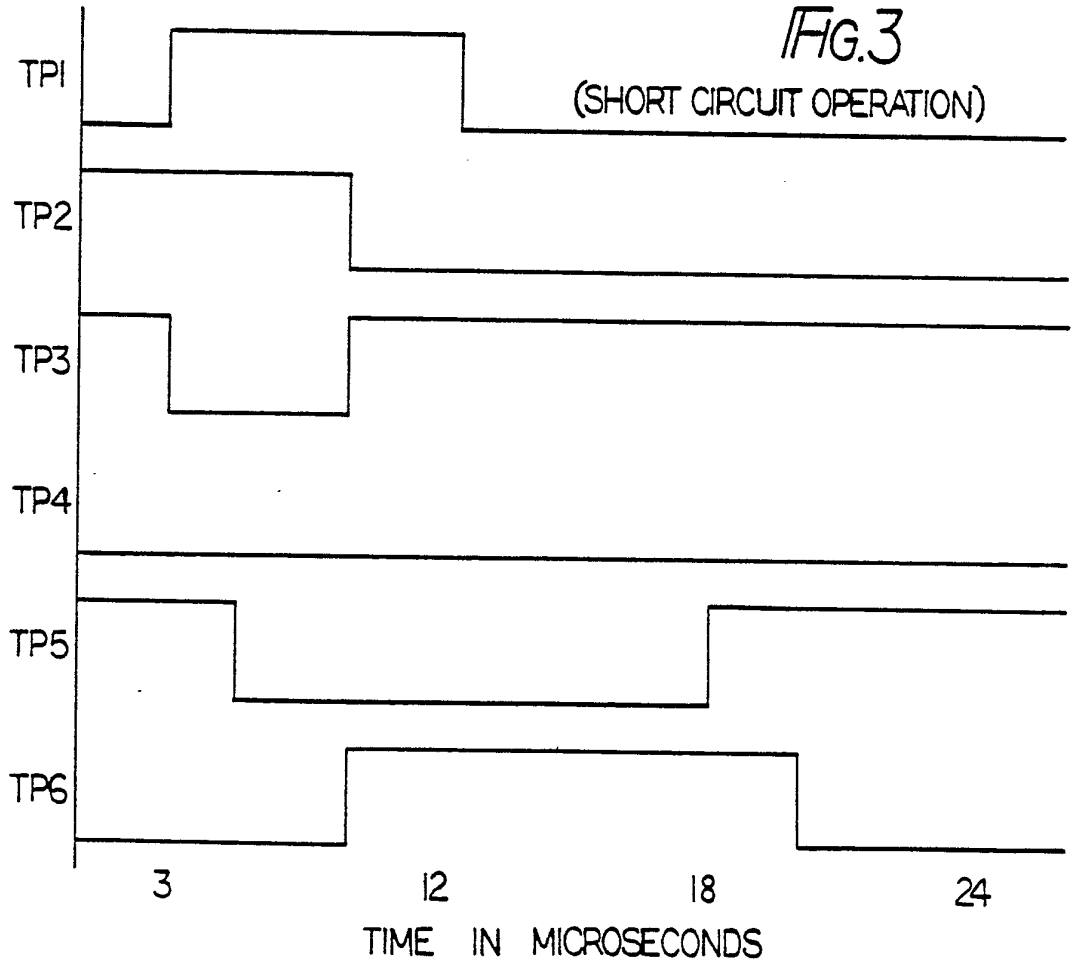


FIG.3
(SHORT CIRCUIT OPERATION)



INTERNATIONAL SEARCH REPORT

International Application No PCT/US.86/00079

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 02 H 7/08; H 03 K 17/08

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 02 H H 03 K H 02 P

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 4484127 (SALIHI et al.) 20 November 1984, see figure 4; column 5, line 24 - column 6, line 52 --	1-3,5,6
A	DE, B, 2441316 (SIEMENS) 22 January 1976, see figures 1,2; column 6, line 43 - column 7, line 40 --	1-3,5,6
A	Patents Abstracts of Japan, volume 4, no. 145 (E-29)(627), 14 October 1980 & JP, A, 5596728 (TOKYO SHIBAURA DENKI K. K.) 23 July 1980 --	1-3,5,6
A	Patents Abstracts of Japan, volume 7, no. 45 (E-160)(1190), 23 February 1983 & JP, A, 57194627 (MATSUSHITA DENKI SANGYO K.K.) 30 November 1982	1-3,5,6

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
4th June 1986	09 JUL 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/00079 (SA 11995)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 23/06/86

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4484127	20/11/84	FR-A-	2527853	02/12/83
		DE-A-	3318134	01/12/83
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		JP-A-	58215976	15/12/83
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DE-B- 2441316	22/01/76	None		