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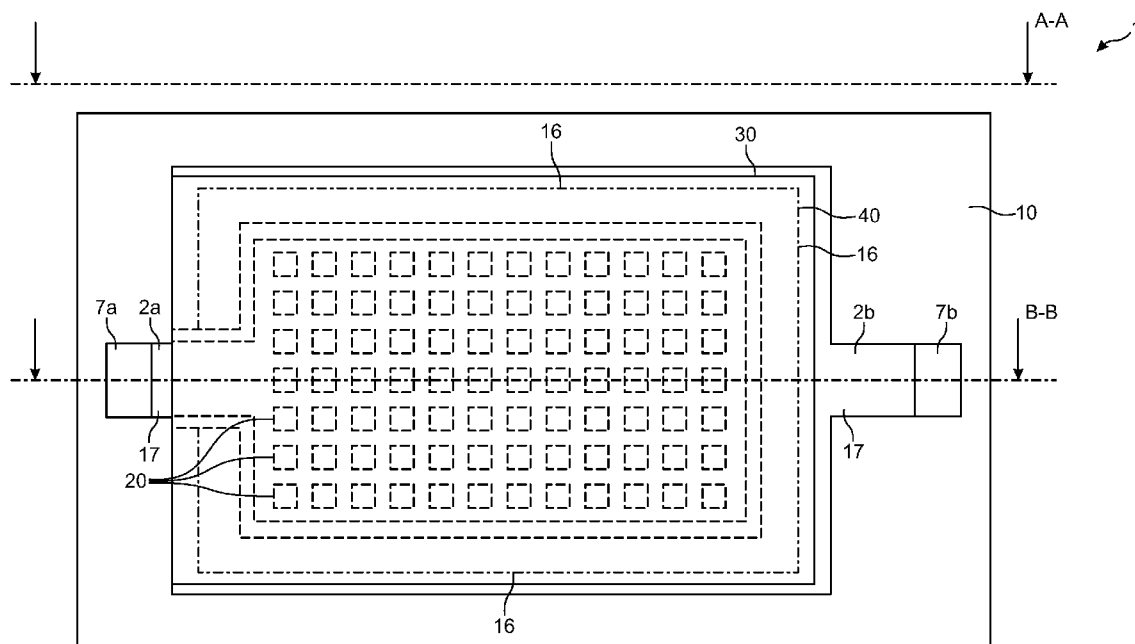


FIG. 6

(57) Abstract: The invention concerns a test arrangement comprising a carrier substrate with a top surface; a first common contact element and a second common contact element arranged on the top surface distant from each other, wherein the first and the second common contact element each comprise a metal layer on the top surface covered by a conductive transparent layer; at least one vertical optoelectronic component, in particular μ LED, arranged on the first common contact element in such a way, that a first contact area of the at least one vertical optoelectronic component connects the first common contact element, wherein the at least one vertical optoelectronic component comprises a second contact area opposite the first contact area; a dielectric material embedding the at least one vertical optoelectronic component, wherein the dielectric material extends adjacent to and/or partially onto the first and/or the second common contact element; a conductive transparent top contact layer that is arranged on the dielectric material covering the at

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least one vertical optoelectronic component, extending along at least one sidewall of the dielectric material thereby contacting the second common contact element; and a test circuit connected to the first and the second common contact element and configured to provide a test signal to the at least one vertical optoelectronic component.

ARRANGEMENT AND METHOD FOR PROCESSING AN ARRANGEMENT HAVING μ LEDs

The present invention concerns an optoelectronic arrangement including at least one optoelectronic component and in particular μ LED, as well as a method for manufacturing an optoelectronic arrangement having at least one optoelectronic component and in particular μ LED.

BACKGROUND

The testing of one or several optoelectronic components, also herein referred to as μ LEDs due to their small sizes of less than 70 μ m, at once and at various stages of its manufacturing process is necessary to avoid larger batches of broken components and to increase the yield during production. While it is possible to conduct some tests on directly wafer level, it is also common to provide dedicated test arrangements, referred to as test vehicles.

For preparing such test vehicles, one or a plurality of μ LEDs is taken from the production wafer and placed on a respective carrier test substrate. The μ LED(s) is then processed further to implement the test vehicle, which is subsequently used for a variety of electrical and optical tests. However, the preparation and implementation of such testing vehicles, being an arrangement with one or a plurality of μ LEDs is error-prone.

Particularly, the step of back etching a dielectric material as SOG (spin-on-glass) on the carrier can create a contamination of the etching chamber when exposed metal areas such as contact areas for the μ LED(s) are present on the carrier. However metal areas or at least large contacting areas are necessary to on the one hand provide a supply current to the μ LED(s) to be tested and on the other hand to connect the test arrangement to a test circuit for supply of the supply current.

While conventional techniques are available, the effort required is high increasing the costs not only for the test vehicle and test arrangement, but also in large scale production.

Consequently, there is a desire to improve an arrangement with one or a plurality of μ LEDs, resulting in a less error-prone structure with higher reproducibility and reduced costs.

5 SUMMARY OF THE INVENTION

This and other objects are addressed by the subject matter of the independent claims. Features and further aspects of the proposed principles are outlined in the dependent claims.

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The inventor proposes a new approach in which a first common contact element as well as a second common contact element is provided on a carrier substrate, whereas both the first and second common contact element comprise a metal layer as well as a conductive transparent layer covering the metal layer. By means of the conductive transparent layer which is in particular not a metal layer but for example a transparent conductive oxide (TCO) layer, the metal layers on the carrier substrate can be "protected" by encapsulating them to reduce the risk of a contamination within an etching chamber during a later etching step conducted on the carrier substrate. The combination of TCO and metal layer thereby provides on the one hand a good conductivity to homogeneously provide a supply current to the μ LED(s) to be tested as well as the metal layers provide a good reflectivity acting as a mirror below the μ LED(s). Optional metal contact(s) to provide contact area(s) for a test circuit for supply of the supply current to the μ LED(s) can then be provided at a respective position and reduced at a minimum in size after all etching steps have been conducted so that no longer a contamination of an etching chamber can occur.

30 Some aspects of the proposed principle are related to a method for manufacturing an arrangement with at least one or a plurality of optoelectronic components and in particular μ LEDs that prevent a potential contamination of an etching chamber during manufacture of the arrangement. The Process results in a less error-prone structure with higher reproducibility and reduced costs.

35

For this purpose, the method comprises a step of providing a carrier substrate with a first and a second common contact element arranged on a top surface of the carrier substrate distant from each other, wherein the first and the second common contact element each comprise a metal layer on the top surface covered by a conductive transparent layer. Both the first and second common contact element in particular comprise a metal layer directly arranged on a top surface of the carrier substrate as well as a conductive transparent layer covering the metal layer thus encapsulating the metal layers together with the top surface of the carrier substrate. By means of the conductive transparent layer which is in particular not a metal layer but for example a transparent conductive oxide (TCO) layer, the metal layers on the carrier substrate are "protected" by encapsulating them to reduce the risk of a contamination within an etching chamber during a later etching step conducted on the carrier substrate. The combination of a TCO and metal layer thereby provides on the one hand a good conductivity to homogeneously provide a supply current to later arranged μ LED(s) on the carrier substrate as well as the metal layers provide a good reflectivity acting as a mirror below the μ LED(s).

In a subsequent step at least one or a plurality of vertical optoelectronic components is provided on the carrier substrate and in particular on the first common contact element. The vertical optoelectronic components can be implemented as μ LEDs and comprise a second contact area on the top surface opposite the carrier substrate. After arranging the vertical optoelectronic component(s) thereupon, a first contact area of the respective vertical optoelectronic components is electrically connected to the first common contact element on the carrier substrate.

In this regard a μ LED is an optoelectronic component that comprises a very small size, i.e. a diameter of less than 50 μ m and down to 2 μ m or even below. Typical diameter may include, but are not limited to 25 μ m, 20 μ m, 15 μ m 10 μ m and 5 μ m. For the purpose of the present application the term vertical optoelectronic component and μ LED are used synonymously, although vertical optoelectronic components are generally not limited to those small sizes. Thus, the method can be

applied also for larger dimensions. The expression "vertical" refers to an optoelectronic component that comprises its respective contact areas on two opposing sides.

5 In case of a plurality of vertical optoelectronic components the vertical optoelectronic components can be arranged in rows and columns on the carrier substrate and in particular on the first common contact element. Furthermore, the second common contact element that is arranged adjacent to the plurality of vertical optoelectronic
10 components, for example directly next to an array of such components but spaced apart from it. In particular the optoelectronic components are due to their arrangement between the first common contact element and the top contact layer all connected in parallel.

15 The vertical optoelectronic component(s) are embedded into a dielectric material, whereas the dielectric material at least partially covers the first and/or second common contact element. By means of a back etching/cleaning step, any contact area on the top surface of the vertical optoelectronic component(s) are exposed, and thus any of the
20 dielectric material arranged on the second contact areas on the top surface of the vertical optoelectronic component(s) is removed exposing them. At the same time or in a subsequent step by means of an etching step, for example a plasma etching process, the second common contact element is exposed from dielectric material potentially arranged on
25 the second common contact element.

As the first and the second common contact element comprising a cover of a conductive transparent and in particular non-metal layer such as for example a TCO, no contamination of metal material in the etching
30 chamber occurs during etching of the dielectric material.

In a subsequent step, a conductive transparent top contact layer is deposited onto the dielectric material, onto the second contact areas of the vertical optoelectronic components as well as on the exposed
35 second common contact element and extends along sidewalls of the dielectric material, thereby contacting the second contact areas on

the top surface of the vertical optoelectronic components as well as the second contact element on the carrier substrate.

Therefore, and in contrast to conventional techniques no additional contact material, like a metal, for the conductive transparent layer on the top surface is necessary. Moreover, as the top contact layer can in particular be of the same material as the cover layer of the second common contact element a connection between these two components can be very strong compared to a connection of different materials such as a metal contacting for example a TCO.

Finally, a test circuit connected to the first and the second common contact element is provided, whereas the test circuit is configured to provide a test signal to the at least one vertical optoelectronic component and in case of a plurality of vertical optoelectronic components a test signal to all vertical optoelectronic components at the same time, as due to their arrangement the vertical optoelectronic components can in particular all be connected in parallel to each other.

According to some aspects, the method further comprises a step of depositing a photomask layer onto the dielectric material before the conductive transparent top contact layer is deposited onto the dielectric material. Subsequently, the photomask layer is structured such that the portion of the dielectric material adjacent to or above the second common contact element is exposed. This will provide access to the area adjacent to or above the second common contact element for a subsequent etching step.

In some aspects a contact angle between the photomask layer and a portion of the dielectric material is less than 90° and particularly less than 60° . In some instances, it is between 35° to 55° . In other words, the sidewalls of the photomask layer arranged adjacent to or above the second common contact element are inclined but not perpendicular in regards to a plane parallel to the dielectric material.

The subsequent etching step transforms the slope of the sidewall of the photomask layer on the dielectric material adjacent to or above the second common contact element at least partially onto the etched sidewalls of the dielectric material. As a consequence, the dielectric material is not etched perpendicular to its top surface, but in an inclined way such that a slope is generated along the edges of the dielectric material adjacent to or above the second common contact element. This slope can be adjusted, for example and not limited thereto, by either using etch parameters but also by the selectivity of the photomask layer onto the etch process, such that the shape of the structured mask layer on the edges is transformed by the etching process onto the dielectric material.

Some aspects are related to the issue of adjusting or controlling the contact angle between the material of the photomask layer and the dielectric material. It has been found that due to the surface tension, the contact angle between the photomask layer and the dielectric material can be different. In order to reduce the contact angle between the photomask layer and the dielectric material several measures can be taken. In some aspects, the dielectric material or the photomask layer can be selected from a group of materials, which provide a certain material-phil surface with regards to the respective other material. For example, the dielectric material may comprise a material-phil surface with regards to the material of the photomask layer.

Alternatively, the material of the photomask layer may comprise a solvent which simplifies the dispense or deposition of the photomask material onto the dielectric layer. The amount or concentration can be used to adjust the contact angle in some aspects. In addition, the solvent may cause the material of the photomask to form a contact angle between the photomask and the dielectric layer of less than 60°. Consequently, the solvent is used to adjust the surface tension between the photomask material and the dielectric material. In some aspects, the photomask material may be processed to adjust the proper contact angle along its circumferential etch.

Another aspect concerns the deposition of the material of the photomask layer on the dielectric layer. For example, the photomask material may be dispensed onto the dielectric layer, particularly above the vertical optoelectronic components, such that the dispensed material forms the edge above or adjacent to the second common contact element. The amount of the photomask material being dispensed allows to some extent forming the edge adjacent to or above the second common contact element and adjusting its shape. For example, in some instances, the photomask material may be first dispensed above or adjacent to the second common contact element to form of the respective edge and contact angle. Further photomask material may be dispensed subsequently to cover the dielectric material layer above the vertical optoelectronic components. In this regard, the portion of the photomask material used for forming the edges of the second common contact element may comprise a slightly different material composition including for example a different solvent concentration such that the dispensed material forms a proper contact angle.

The photomask material may also be jetted onto the dielectric material above the vertical component with a portion of the jetted material forming the edges of the second common contact. The same principles and adjustments used during the dispense process can be also applied during the exemplary jetting process. In this regard, the deposition of the photomask layer may therefore be divided into several sub-steps to ensure proper adjustment of the edge and the contact angle adjacent to or above the second common contact element.

Some aspects relate to the etching step and the results thereof. In some aspects, the etching is performed by a plasma etching, a chemical etching or a combination thereof. Due to the inclined sidewalls of the photomask layer, the inclination and slope is transformed during the etching process, resulting in a sidewall of the dielectric layer adjacent to or above the second common contact element, which comprises at least partially the same angle as the contact angle between the photomask material and the dielectric layer. Hence in some aspects, the etching of the sidewalls of the dielectric layer may follow the

slope of the sidewalls of the photomask layer during the step of etching.

In addition, the conductive transparent top contact layer is deposited after removing the photomask layer and optionally opening the second contact areas on the top surface of the vertical optoelectronic component(s). This latter step is necessary in case, the dielectric layer has not been pre-processed before to open the respective second contact areas on the top surface of the vertical optoelectronic components. When using a photoactive layer as a dielectric material, portions of the photoactive material of the top surface of the vertical optoelectronic component(s) can be illuminated and subsequently removed in a simple photoresist removal process.

In some aspects, the step of embedding the vertical optoelectronic component(s) comprises spinning a dielectric material onto the carrier substrate and the optoelectronic components. Alternatively, the dielectric material can be sputtered, dispensed or jetted. In some aspects, particularly during a dispensing or jetting operation of the dielectric material, the material can be deposited between adjacent optoelectronic components but also on the surface of some of those components. The dielectric material during the deposition may comprise a solvent, which is subsequently evaporated to form a planar dielectric material plane.

Any spin-on-glass material can be used for this purpose, but is not limited thereto. In some aspects, the dielectric material can be a photo active material and in particular an inactivated photoactive material. This may simplify the etching process later on. Some aspects concern further different possible dielectric materials. In some aspects, the dielectric material may comprise a resin, a siloxane or a glass material. The latter can be deposited with spin-on-glass techniques.

In some aspects, the step of providing a carrier substrate comprises at least one of the steps of:

- Providing a layer stack of at least a semiconductor layer and a dielectric layer, the dielectric layer forming the top surface of the carrier substrate;
- providing a first metal layer on the top surface and a second metal layer on the top surface, the first and second metal layer being distant from each other;
- covering the first and second metal layer each by means of a conductive transparent layer such that in particular the conductive transparent layer each encloses the first and second metal layer together with the carrier substrate.

In some aspects, the second common contact at least partially surrounds the first common contact on the top surface in a circumferential direction spaced to the first common contact. By this a supply current can be supplied via a large area surrounding the first common contact area into the opposing top contact layer to homogeneously provide the supply current to the optoelectronic component(s). In particular the first contact element can be a sheet-like contact that is at least partially surrounded by a ringlike second common contact element.

In some aspects, the conductive transparent top contact layer encapsulates the dielectric material except from a contact region of the first common contact and the dielectric material. By this almost the whole dielectric material is protected from external influences and potential damages or cracks between the dielectric material and the top contact layer can be prevented as far as possible.

In another aspect, a test arrangement comprises a carrier substrate with a top surface. On the top surface a first common contact element and a second common contact element are arranged distant from each other. The first and the second common contact element each comprise a metal layer on the top surface covered by a conductive transparent layer. The arrangement further comprises at least one or a plurality of vertical optoelectronic components in particular μ LEDs, which are positioned on the carrier substrate and in particular on the first common contact element in such way that a first contact area of each

of the vertical optoelectronic component(s) connects the first common contact element.

Each of the vertical optoelectronic component(s) also comprises a second contact area, which is opposite the first contact area. In case of a plurality of vertical optoelectronic components, these can be arranged in rows and columns to form an array. A dielectric material is deposited on the carrier substrate embedding the vertical optoelectronic component(s) therein. Furthermore, the dielectric material extends adjacent to and/or partially onto the first and/or the second common contact element.

In accordance with the proposed principle, a conductive transparent top contact layer is arranged on the dielectric material covering the second contact area(s) of the vertical optoelectronic component(s) and extending along at least one sidewall of the dielectric material thereby contacting the second common contact element. In other words, the conductive transparent top contact layer covers the second contact area(s) of the optoelectronic component(s), a top surface of the dielectric layer (at least partially) and extends along the sidewalls of the dielectric layer down to the second common contact element.

In addition, the arrangement comprises a test circuit connected to the first and the second common contact element which is configured to provide a test signal to the at least one vertical optoelectronic component.

In some aspects, the sidewall(s) of the dielectric material comprises a contact angle to a plane parallel to the second common contact element of less than 60° and particularly between 35° and 55° . The small contact angle prevents rupturing or breaking of the conductive transparent top contact layer during the deposition process enabling to extend the conductive transparent top contact layer onto the second common contact element without the need of an additional metallic contact.

In some aspects, the carrier substrate comprises a layer stack of at least a semiconductor layer and a dielectric layer, wherein the dielectric layer is forming the top surface of the carrier substrate.

5 In some aspects, the second common contact element surrounds at least partially the first common contact element on the top surface in a circumferential direction spaced to the first common contact element. In some aspects, the second common contact element surrounds the first common contact element on the top surface in a circumferential
10 direction except for a contact lug extending from the first common contact element toward a side surface of the carrier substrate. By this a supply current can be supplied via a large area surrounding the first common contact area into the opposing top contact layer to homogeneously provide the supply current to the optoelectronic
15 component(s). In particular the first contact element can be a sheet-like contact that is at least partially surrounded by a ringlike second common contact element, whereas for example a contact lug can cross the ringlike second common contact element spaced from the second common contact element.

20 The term contact lug can in particular be understood in such that the first and/or second common contact element comprises a portion protruding from a main body of the first and/or second common contact element in lateral direction, whereas the protruding portion is in particular small compared to the main body. By means of the contact
25 lug(s) a supply current can in particular be supplied to the respective common contact element.

In some aspects, a contact pad is arranged on each or at least one of
30 the first and second common contact element and in particular on a contact lug of the respective common contact element. By means of the contact pad(s) for example the test circuit can be electrically connected to the common contact element(s) by means of for example contact pin(s) contacting the contact pad(s).

35 In some aspects, the conductive transparent top contact layer encapsulates the dielectric material except from a contact region of

the first common contact element and the dielectric material. By this almost the whole dielectric material is protected from external influences and potential damages or cracks between the dielectric material and the top contact layer can be prevented as far as possible.

5 In addition by exposing the contact region(s) of the first common contact element and the dielectric material from the conductive transparent top contact layer a short between the first common contact element and the conductive transparent top contact layer can be prevented.

10 In some aspects, the first common contact element and/or the second common contact element comprise a contact lug extending in particular on the carrier substrate from the respective common contact element toward a side surface of the carrier substrate. In addition or as an
15 alternative, a contact lug of the first common contact element and a contact lug of the second common contact element can be arranged on the same side with regard to the at least one vertical optoelectronic component on the carrier substrate, or they can be arranged on different sides with regard to the at least one vertical optoelectronic component
20 on the carrier substrate, for example adjacent sides with regard to the at least one vertical optoelectronic component on the carrier substrate, or they can be arranged on opposing sides with regard to the at least one vertical optoelectronic component.

25 In some aspects, the carrier substrate comprises a supply circuit being in electric contact with the first and/or second common contact element. By means of this for example contact lug(s) or contact pad(s) can be dispensed with, as the test circuit can for example be connected to the supply circuit being in electric contact with the first and/or
30 second common contact element to supply a respective supply current to the first and/or second common contact element via the supply circuit. In such a case, the conductive transparent top contact layer can for example encapsulate the dielectric material completely together with the carrier substrate and an electrical connection of the first common
35 contact element results from the supply circuit within the carrier substrate.

In some aspects, a distance between the second common contact element and the top surface of the at least one vertical optoelectronic component is substantially the height of the at least one vertical optoelectronic component.

Different dielectric materials as mentioned above can be used for the embedding of the vertical optoelectronic components. For example, spin-on-glass material can be used, but also inactivated photo active material.

The conductive transparent top contact layer may comprise indium tin oxide (ITO) with an optional thickness that is smaller than the distance between the second common contact element and the top surface of the optoelectronic component(s). Hence, the conductive transparent top contact layer is thinner than the distance between the second common contact element and top surface of the optoelectronic component(s).

SHORT DESCRIPTION OF THE DRAWINGS

Further aspects and embodiments in accordance with the proposed principle will become apparent in relation to the various embodiments and examples described in detail in connection with the accompanying drawings in which

Figure 1 illustrates a test arrangement with a plurality of optoelectronic components;

Figure 2 shows a top view of an embodiment of a test arrangement with an optoelectronic component in accordance with some aspects of the proposed principle;

Figures 3A and 3B show a side view and a cross section of the test arrangement of Figure 2;

Figure 4 shows a top view of a further embodiment of a test arrangement with an optoelectronic component in

accordance with some aspects of the proposed principle;

Figure 5 shows a cross section of the test arrangement of Figure 4;

Figure 6 shows a top view of a further embodiment of a test arrangement with a plurality of optoelectronic components in accordance with some aspects of the proposed principle;

Figures 7A and 7B show a side view and a cross section of the test arrangement of Figure 6;

Figure 8 shows a top view of a further embodiment of a test arrangement with a plurality of optoelectronic components in accordance with some aspects of the proposed principle;

Figures 9A to 9C show a side view and cross sections of the test arrangement of Figure 8;

Figure 10 shows a top view of a further embodiment of a test arrangement with a plurality of optoelectronic components in accordance with some aspects of the proposed principle; and

Figure 11 shows a cross section of the test arrangement of Figure 10;

DETAILED DESCRIPTION

The following embodiments and examples disclose various aspects and their combinations according to the proposed principle. The embodiments and examples are not always to scale. Likewise, different elements can be displayed enlarged or reduced in size to emphasize individual aspects. It goes without saying that the individual aspects of the

embodiments and examples shown in the figures can be combined with each other without further ado, without this contradicting the principle according to the invention. Some aspects show a regular structure or form. It should be noted that in practice slight differences and deviations from the ideal form may occur without, however, contradicting the inventive idea.

In addition, the individual figures and aspects are not necessarily shown in the correct size, nor do the proportions between individual elements have to be essentially correct. Some aspects are highlighted by showing them enlarged. However, terms such as "above", "over", "below", "under", "larger", "smaller" and the like are correctly represented with regard to the elements in the figures. So it is possible to deduce such relations between the elements based on the figures.

It is suitable to provide a common conductive plane or common conductive element during the processing of arrangements including a plurality of optoelectronic components, contacting the plurality of optoelectronic components at once.

Figure 1 illustrates such arrangement in a sideview thereof. The arrangement comprises a carrier structure 10 including a carrier substrate 10a and a dielectric layer 11 arranged on the carrier substrate 10a. On top of the carrier structure 10, a metal contact plane layer 13 is arranged. Further a plurality of optoelectronic components 20 is arranged with respective contacts on the metal contact plane layer 13.

The optoelectronic components are implemented as vertical optoelectronic components 20 having a bottom surface and a top surface opposite to the bottom surface, respectively. Each of those top and bottom surfaces comprise a respective contact area. More particularly, the contact areas of the bottom surfaces 22 of the plurality of vertical optoelectronic components 20 are connected to the metal contact plane layer 13. The top surfaces 21 of the optoelectronic components also each comprise a contact area. The optoelectronic components 20 are

implemented as μ LEDs having a diameter of less than 50 μm down to approximately 2 μm for example. Typical dimensions and sized for μ LEDs range between 30 μm and 10 μm but can be also slightly smaller, for example 5 μm .

5

The optoelectronic components 20 are positioned above the metal contact plane layer 13 and attached thereupon. A small dielectric material 14, for example SiO_2 is deposited on the surface of carrier structure 10 as well as on the sidewalls of the plurality of the vertical optoelectronic components. The remaining space between of the
10 optoelectronic components is filled up with a dielectric material 40, thereby embedding the optoelectronic components 20 completely. The top surfaces of the optoelectronic components as well as the dielectric material 40 is now covered by a conductive transparent top contact
15 layer 30, for example ITO. As illustrated herein the conductive transparent top contact layer 30 contacts the respective contact on the top surfaces of the optoelectronic components and extends over the material portion 40 as well as the optoelectronic components to a structure depicted on the right.

20

A contact 15 made of gold or similar metal is deposited on the conductive transparent top contact layer 30 to provide an electrical contact to a common contact element 12 arranged on the dielectric material 11 of the carrier structure 10. This element encircled in
25 Figure 1 provides a so-called contact ramp for the common contact of μ LEDs and optoelectronic components used for display applications, for example. As a result, the metal structure has to be deposited across the edge given by the height difference between the top of conductive transparent top contact layer 30 caused by the application of the
30 plurality of optoelectronic components onto the carrier system. As shown in Figure 1, the step is quite steep and approximately 90° . The metal contact 15 in particular requires a height which is in the same range as the height of the respective optoelectronic components.

35 For very small optoelectronic components arranged in rows and columns such formation of the metal contacts is difficult to realize as the transparent conductive material 30 as well as the metal contact tends

to rupture and form a potential a breakage points resulting in a higher resistance or even a complete short-open. In addition, a step of back etching the dielectric material(s) 40 and 14 creates a contamination of the etching chamber due to exposed metal areas, particularly the metal contact plane layer 13, are present on the carrier.

Consequently, the inventor proposes a new method for providing such structure and contacting the optoelectronic elements or μ LEDs on the carrier structure using common contact elements comprising a metal layer encapsulated by a non-metal cover layer as well as by extending the transparent top contact layer directly down to such a common contact element with the non-metal cover layer being of for example the same material as the transparent top contact layer. By this a contamination of the etching chamber while back etching the dielectric material(s) can be prevented as well as the risk of a rupture of the connection between the transparent top contact layer and a respective contact element can at least be reduced.

Figures 2, 3A and 3B illustrate a respective embodiment of an arrangement with an optoelectronic component and in particular μ LED. Figure 2 thereby illustrates a top view of the arrangement whereas Figures 3A and 3B show a cross section/side view of the arrangement at a position indicated in Figure 2 by means of the cutting lines A-A and B-B.

The test arrangement 1 comprises a carrier structure 10 with a carrier substrate 10a and a dielectric material layer 11 forming a top surface 3 of the carrier structure 10. For reasons of simplicity the carrier structure 10 may in the following also be called carrier substrate but may be not limited to a single carrier substrate 10a of for example silicon. On the top surface 3, a first common contact element 2a and a second common contact element 2b are arranged distant from each other. In particular the first common contact element 2a is in form of a plate like element with a contact lug 17 extending from the plate like element to a side of the carrier substrate 10. The second common contact element 2b on the other hand partially surrounds the first common contact element 2a in a ring like manner, with the contact lug 17 of the first

common contact element 2a crossing the ring like element spaced from the second common contact element 2b. The second common contact element 2b as well comprises a contact lug 17 extending from the ring like element to a side of the carrier substrate 10. On the contact lugs each
5 a contact pad 7a, 7b is arranged by means of which a test circuit (not shown) can be connected to the first and second common contact element 2a, 2b.

As shown in the cross-sectional view in Figure 3B, the first and the
10 second common contact element 2a, 2b each comprise a metal layer 4a, 4b on the top surface 3 of the carrier substrate covered by a conductive transparent layer 5a, 5b, in particular a non-metal conductive transparent layer 5a, 5b such as for example ITO. By means of the conductive transparent layer 5a, 5b the metal layers 4a, 4b are together
15 with the carrier substrate 10 encapsulated, such that in a later etching step no metals areas are exposed and a contamination of the etching chamber due to exposed metal areas is prevented.

The test arrangement 1 further comprises a vertical optoelectronic
20 component 20, in particular μ LED, arranged on the first common contact element 2a in such a way, that a first contact area 6a of the vertical optoelectronic component 20 connects the first common contact element 2a. In addition the vertical optoelectronic component 20 comprises a second contact area 6b opposite the first contact area 6a facing away
25 from the carrier substrate 10. The vertical optoelectronic component 20 is embedded in a dielectric material 40 such that the first and second contact area 6a, 6b are exposed and such that the vertical optoelectronic component 20 is laterally surrounded by the dielectric material 40. In addition, the dielectric material 40 extends adjacent
30 to and partially onto the first and the second common contact element 2a, 2b filling spaces between the first and the second common contact element 2a, 2b on the carrier substrate 10 and covering the first and the second common contact element 2a, 2b adjacent to the vertical optoelectronic component 20.

35 On top of the dielectric material 40 as well as on the top surface of the vertical optoelectronic component 20 a conductive transparent top

contact layer 30 is arranged electrically contacting the second contact area 6b. The dielectric material 40 covers the vertical optoelectronic component 20 as well as the dielectric material and extends along sidewalls 16 of the dielectric material 40 thereby contacting the second common contact element 2b. By means of the conductive transparent top contact layer 30 the second common contact element 2b is electrically coupled to the second contact area 6b such that a respective test signal can be provided to the vertical optoelectronic component 20 via the first and second common contact element 2a, 2b.

The test signal can be provided to the vertical optoelectronic component 20 by means of a not shown test circuit connected to the first and the second common contact element 2a, 2b. The test circuit can for example comprise contact pins contacting the contact pads 7a, 7b and can provide a test signal to the vertical optoelectronic component 20 to test its functionality. The test signal can for example comprise a sequence of different current pulses whereby the properties of the test signal can be chosen/adapted as required according to known embodiments from the state of the art.

The conductive transparent top contact layer 30 in particular covers/encapsulates the dielectric material completely except of the contact region of the contact lug 17 of the first common contact element 2a and the dielectric material 40, in which the conductive transparent top contact layer 30 is arranged only on the dielectric material but does not extend down to the contact lug 17 of the first common contact element 2a. By this the dielectric material 40 is almost completely covered by the conductive transparent top contact layer 30 such that the dielectric material is protected by means of the conductive transparent top contact layer 30 from external influences. The dielectric material 40 can as shown be a single layer but can also be as shown in Figure 1 be of more than one layer embedding the optoelectronic component.

The conductive transparent top contact layer 30 can thereby in particular be of a conductive transparent oxide such as ITO which together with the conductive transparent layer 5b of the second common

contact element 2b provides a better bonding strength than a non-metal with a metal as it would be the case of the second common contact element 2b not being covered with the conductive transparent layer 5b. This can in particular be of advantage right in the transition region of the conductive transparent top contact layer 30 from the top of the dielectric material 40 along the sidewalls 16 and onto the second common contact element 2b, where the greatest stresses and strains prevail.

To receive such a shown test arrangement 1, the carrier substrate 10 is provided with the first and second common contact element 2a, 2b arranged on the top surface 3 of the carrier substrate 10 distant from each other. Therefore, a first and a second metal layer 4a, 4b is provided on the top surface 3 each covered by a conductive transparent layer 5a, 5b together forming the first and second common contact element 2a, 2b. On the first common contact element 2a an optoelectronic component 20 is arranged. The second common contact element 2a comprises a slightly larger size than the first contact area 6a of the optoelectronic component 20 being placed thereupon. The size difference allows for a small misalignment during the transfer of the optoelectronic component onto the second common contact element 2a. In such case, the first contact area of the optoelectronic component still connects to the second common contact element 2a.

A dielectric material layer is then deposited on the carrier substrate 10 covering the sidewalls of the optoelectronic component as well as the top surface thereof. This material, for example SiO₂ can be sputtered or deposited by other means onto the carrier substrate and the optoelectronic component. It is used for protection but also to improve the sticking of a spin-on-glass material deposited later, as such certain spin-on-glass materials tend to delaminate if deposited directly on the optoelectronic device or the carrier substrate. Hence, the dielectric material layer is optional depending on the material used later on. A spin-on-glass material is then deposited on the dielectric material layer, as well as on the top surfaces of the optoelectronic component 20 together forming dielectric material 40 as shown in the Figures. For example a spin-on-glass material is used,

although any other suitable dielectric material can be applied as well. The proposed principle is neither limited to the specific material nor to the deposition process of such material onto the optoelectronic component and the surrounding space. The dielectric material 40 fills the surrounding space of the optoelectronic component as well as a space between the first and second common contact element 2a, 2b and at least partially also the first and second common contact element 2a, 2b. The dielectric material 40 also covers the optoelectronic component's top surface 21 and the second contact area of the same. In a subsequent step, a back etching process or mechanical means is therefore applied to remove the dielectric material 40 on the top surface 21 of the optoelectronic component, thereby opening the top surface as well as the second contact area 6b thereupon. Due to the fact that the first and a second metal layer 4a, 4b are covered by means of the conductive transparent layers 5a, 5b as well as no further exposed metal areas there is no risk of contamination of the etching chamber during the back etching step.

Then the conductive transparent top contact layer 30 can be provided on the dielectric material 40, on the second contact area 6b as well as along the resulting side sidewalls 16 of the dielectric material 40 connecting the second contact area 6b with the second common contact element 2b before the contact pads 7a, 7b are arranged on the contact lugs 17 of the first and second common contact element 2a, 2b.

Figures 4 and 5 show a further embodiment of an arrangement with an optoelectronic component and in particular μ LED. Figure 4 thereby illustrates a top view of the arrangement whereas Figure 5 shows a cross section of the arrangement at a position indicated in Figure 4 by means of the cutting line A-A.

Compared to the embodiment shown in Figures 2, 3A and 3B, the carrier substrate 10 in addition comprises a supply circuit 18 electrically coupled to the first common contact element 2a and the second common contact element 2b. Due to the supply circuit 18 the contact lug(s) 17 can be dispensed with, as an electrical contact with the test circuit can be provided via the supply circuit 18. Thus also the contact pads

7a, 7b can on the contact lugs 17 can be dispensed with. In the embodiment shown "only" the contact lug 17 of the first common contact element 2a is removed, however also the contact lug 17 of the second common contact element 2b can be removed as for example also shown for the embodiment shown in Figure 10. By means of such a design, the dielectric material 40 can be covered completely by the transparent top contact layer 30, as no connection of the first common contact element 2a has to be routed to the outside under or next to the dielectric material 40.

Figures 6 and 7A and 7B show a further embodiment of an arrangement with a plurality of optoelectronic components and in particular μ LEDs. Figure 6 thereby illustrates a top view of the arrangement whereas Figures 7A and 7B show a side view and a cross section of the arrangement at a position indicated in Figure 6 by means of the cutting lines A-A and B-B.

Compared to the embodiment shown in Figures 2, 3A and 3B, a plurality of optoelectronic components 20 is placed on the first common contact element 2a, whereas the optoelectronic components 20 are arranged on the first common contact element 2a in rows and columns. Due to the first common contact element 2a as well as the second common contact element 2b contacting all first and second contact areas 6a, 6b at the same time, the optoelectronic components are connected in parallel to each other and can thus be tested simultaneously when providing a test signal to the first and second common contact element 2a, 2b.

In the embodiment shown, the contact lugs 17 of the first and second common contact element 2a, 2b direct into opposing directions with regard to the optoelectronic components 20, however the contact lugs 17 can also be arranged/oriented differently.

Figures 8 and 9A to 9C show a respective further embodiment of an arrangement with a plurality of optoelectronic components and in particular μ LEDs. Figure 8 thereby illustrates a top view of the arrangement whereas Figures 9A to 9C show a side view and cross sections

of the arrangement at a position indicated in Figure 8 by means of the cutting lines A-A, B-B and C-C.

5 In the embodiment shown, the contact lugs 17 of the first and second common contact element 2a, 2b direct into the same direction with regard to the optoelectronic components 20 being arranged next to each other on the carrier substrate 10. By means of such an arrangement, the connection of the test circuit to the contact pads 7a, 7b can be simplified and a manufacture and encapsulation of the dielectric
10 material 40 can be improved.

Figures 10 and 11 show a further embodiment of an arrangement with a plurality of optoelectronic components and in particular μ LEDs. Figure 10 thereby illustrates a top view of the arrangement whereas Figure 11
15 shows a cross section of the arrangement at a position indicated in Figure 10 by means of the cutting line A-A.

As for the embodiment shown in Figures 4 and 5, the carrier substrate 10 in addition comprises a supply circuit 18 electrically coupled to
20 the first common contact element 2a and the second common contact element 2b. Due to the supply circuit 18 the contact lugs 17 can be dispensed with, as an electrical contact with the test circuit can be provided via the supply circuit 18. Thus, also the contact pads 7a, 7b can on the contact lugs 17 can be dispensed with. By means of such a
25 design, the dielectric material 40 can be covered completely by the transparent top contact layer 30, as no connection of the first common contact element 2a has to be routed to the outside under or next to the dielectric material 40.

30

LIST OF REFERENCES

	1	test arrangement
5	2a, 2b	common contact element
	3	top surface
	4a, 4b	metal layer
	5a, 5b	conductive transparent layer
	6a, 6b	contact area
10	7a, 7b	contact pad
	10	carrier structure
	10a	carrier substrate
	11	dielectric layer
	12	contact element
15	13	contact plane layer
	14	dielectric material
	15	metal contact
	16	sidewall
	17	contact lug
20	18	supply circuit
	20	optoelectronic component
	21	top surface
	22	bottom contact
	30	transparent conductive material
25	40	dielectric material

CLAIMS

1. Method for manufacturing a test arrangement (1) with at least one optoelectronic component (20), in particular μ LED, comprising the steps of:

- providing a carrier substrate (10, 10a) with a first and a second common contact element (2a, 2b) arranged on a top surface (3) of the carrier substrate (10, 10a) distant from each other, wherein the first and the second common contact element (2a, 2b) each comprise a metal layer (4a, 4b) on the top surface (3) covered by a conductive transparent layer (5a, 5b);
- providing at least one vertical optoelectronic component (20) onto the first common contact element (2a), the at least one vertical optoelectronic component (20) having a first contact area (6a) electrically connecting the first common contact element (2a) and a second contact area (6b) opposite the first contact area (6a);
- embedding the at least one vertical optoelectronic component (20) into a dielectric material (40), whereas the dielectric material (40) at least partially covers the first and/or second common contact element (2a, 2b);
- depositing a conductive transparent top contact layer (30) onto the second contact area (6b) of the at least one vertical optoelectronic component (20), such that it extends along at least one sidewall (16) of the dielectric material (40) thereby contacting the second common contact element (2b); and
- providing a test circuit connected to the first and the second common contact element (2a, 2b) and configured to provide a test signal to the at least one vertical optoelectronic component (20).

2. Method according to claim 1, wherein the step of embedding comprises one of the steps of:

- Spinning the dielectric material (40);
- Sputtering the dielectric material (40);

- Dispensing the dielectric material (40), in particular onto a top surface (21) of the at least one vertical optoelectronic component (20);
- Jetting the dielectric material (40), in particular onto a top surface (21) of the at least one vertical optoelectronic component (20).

3. Method according to any of the preceding claims, wherein the step of embedding comprises the step of:

- Removing portions of the dielectric material (40) from a top surface (21) of the at least one vertical optoelectronic component (20) to expose at least the second contact area (6b) thereof.

4. Method according to any of the preceding claims, wherein the dielectric material (40) is a photoactive material or a glass material, in particular an inactivated photoactive material or a Spin-on-glass material.

5. Method according to any of the preceding claims, wherein the step of providing a carrier substrate (10, 10a) comprises at least one of the steps of:

- Providing a layer stack of at least a semiconductor layer (10a) and a dielectric layer (11), the dielectric layer (11) forming the top surface (3) of the carrier substrate (10);
- providing a first metal layer (4a) on the top surface (3) and a second metal layer (4b) on the top surface (3), the first and second metal layer (4a, 4b) being distant from each other;
- covering the first and second metal layer (4a, 4b) each by means of a conductive transparent layer (5a, 5b) such that in particular the conductive transparent layer (5a, 5b) each encloses the first and second metal layer (4a, 4b) together with the carrier substrate (10, 10a).

6. Method according to any of the preceding claims, wherein the second common contact element (2b) at least partially surrounds the first

common contact element (2a) on the top surface (3) in a circumferential direction.

7. Method according to any of the preceding claims, wherein the
5 conductive transparent top contact layer (30) encapsulates the dielectric material (40) except from a contact region of the first common contact element (2a) and the dielectric material (40).

8. Test arrangement (1) comprising:

- 10 - a carrier substrate (10, 10a) with a top surface (3);
- a first common contact element (2a) and a second common contact element (2b) arranged on the top surface (3) distant from each other, wherein the first and the second common contact element (2a, 2b) each comprise a metal layer (4a, 4b) on the top
15 surface (3) covered by a conductive transparent layer (5a, 5b);
- at least one vertical optoelectronic component (20), in particular μ LED, arranged on the first common contact element (2a) in such a way, that a first contact area (6a) of the at
20 least one vertical optoelectronic component (20) connects the first common contact element (2a), wherein the at least one vertical optoelectronic component (20) comprises a second contact area (6b) opposite the first contact area (6a);
- a dielectric material (40) embedding the at least one vertical
25 optoelectronic component (20), wherein the dielectric material (40) extends adjacent to and/or partially onto the first and/or the second common contact element (2a, 2b);
- a conductive transparent top contact layer (30) that is arranged on the dielectric material (40) covering the at least
30 one vertical optoelectronic component (20), extending along at least one sidewall (16) of the dielectric material (40) thereby contacting the second common contact element (2b); and
- a test circuit connected to the first and the second common contact element (2a, 2b) and configured to provide a test
35 signal to the at least one vertical optoelectronic component (20).

9. Test arrangement according to claim 8, wherein the carrier substrate (10) comprises a layer stack of at least a semiconductor layer (10a) and a dielectric layer (11), the dielectric layer (11) forming the top surface (3) of the carrier substrate (10).
- 5
10. Test arrangement according to claim 8 or 9, wherein the second common contact element (2b) surrounds at least partially the first common contact element (2a) on the top surface (3) in a circumferential direction.
- 10
11. Test arrangement according to any one of claims 8 to 10, wherein the second common contact element (2b) surrounds the first common contact element (2a) on the top surface (3) in a circumferential direction except for a contact lug (17) extending from the first common contact element (2a) toward a side surface of the carrier substrate (10, 10a).
- 15
12. Test arrangement according to any one of claims 8 to 11, wherein the conductive transparent top contact layer (30) encapsulates the dielectric material (40) except from a contact region of the first common contact element (2a) and the dielectric material (40).
- 20
13. Test arrangement according to any one of claims 8 to 12, wherein the first common contact element (2a) and/or the second common contact element (2b) comprise a contact lug (17) extending in particular on the carrier substrate (10, 10a) from the respective common contact element toward a side surface of the carrier substrate (10, 10a); and/or wherein optionally a contact lug (17) of the first common contact element (2a) and a contact lug (17) of the second common contact element (2b)
- 25
- are arranged on the same side with regard to the at least one vertical optoelectronic component (20), or
 - are arranged on different sides with regard to the at least one vertical optoelectronic component (20), or
 - are arranged on opposing sides with regard to the at least one vertical optoelectronic component (20).
- 30
- 35

14. Test arrangement according to any one of claims 8 to 13, wherein the carrier substrate (10, 10a) comprises a supply circuit (18) being in electric contact with the first and/or second common contact element (2a, 2b) and wherein the test circuit is connected to the supply circuit (18) being in electric contact with the first and/or second common contact element (2a, 2b).
15. Test arrangement according to any one of claims 8 to 14, wherein a distance between the second common contact element (2b) and the top surface (21) of the at least one vertical optoelectronic component (20) is substantially the height of the at least one vertical optoelectronic component (20).
16. Test arrangement according to any one of claims 8 to 15, wherein the dielectric material (40) comprises an inactivated photoactive material or a Spin-on-glass material.
17. Test arrangement according to any one of claims 8 to 16, wherein the conductive transparent top contact layer (30) comprises ITO, and optionally wherein a thickness of the conductive transparent top contact layer (30) is smaller than a distance between the second common contact element (2b) and the top surface (21) of the at least one vertical optoelectronic component (20).

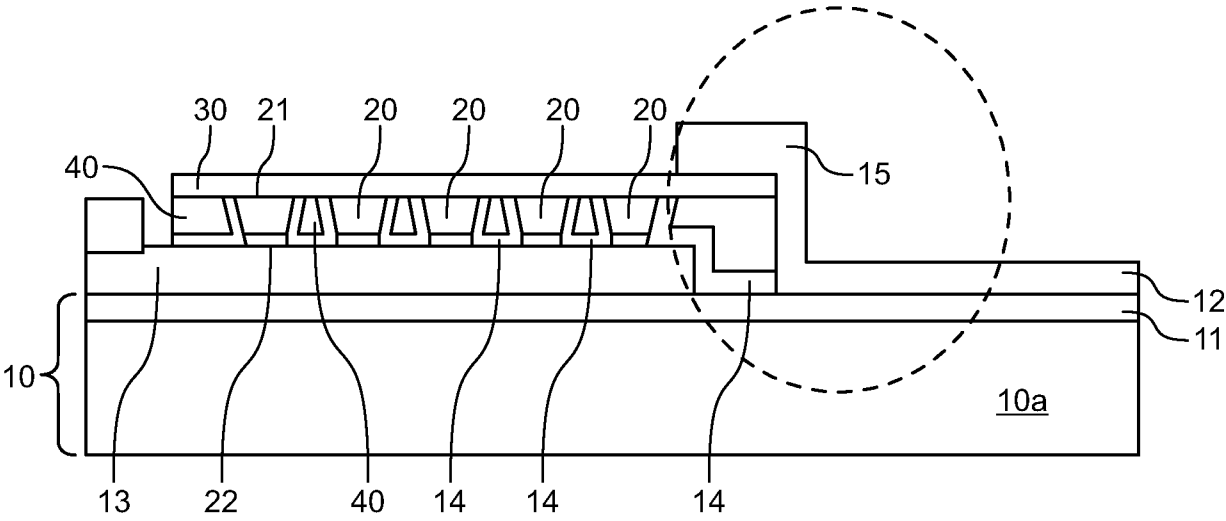


FIG. 1

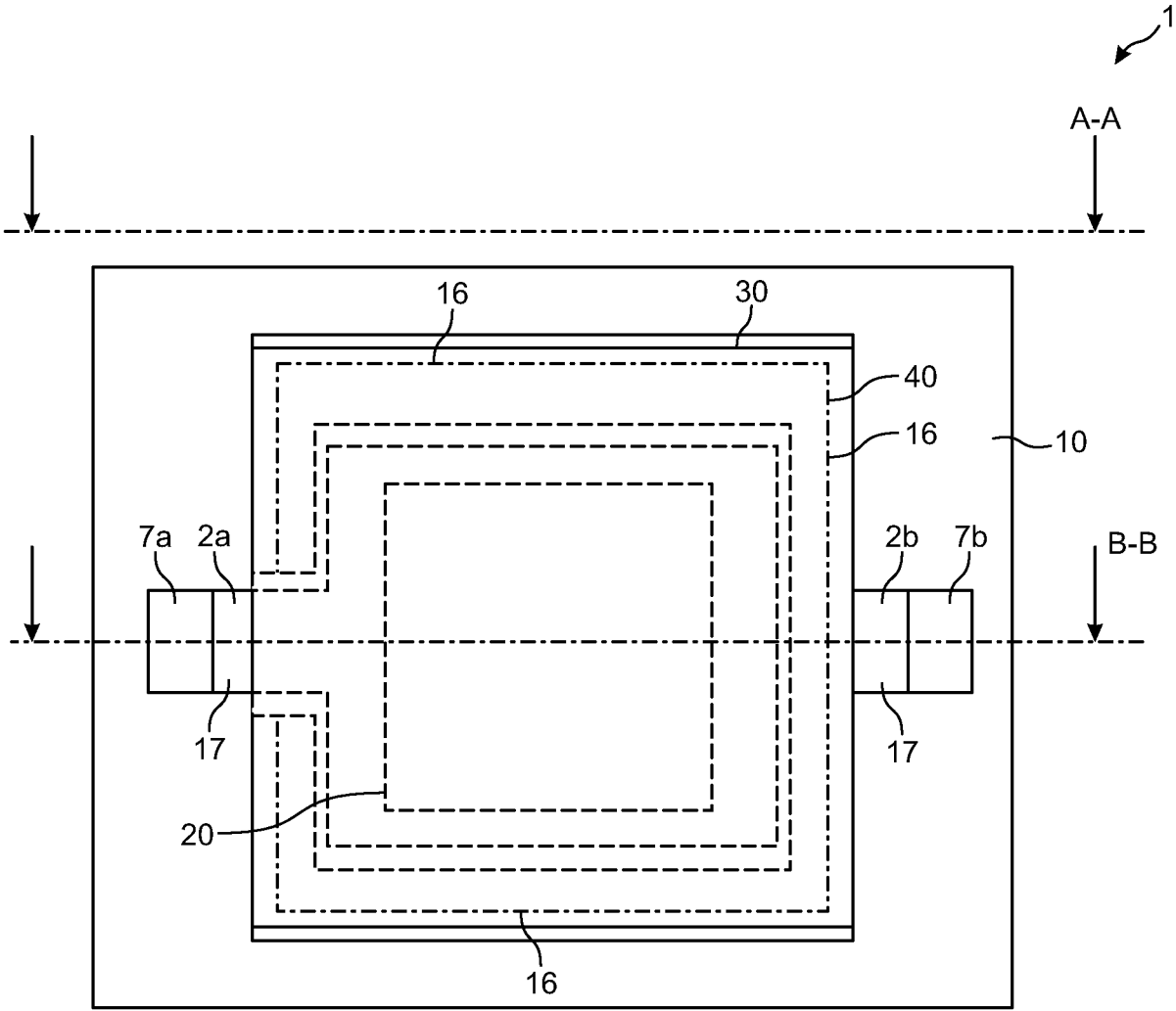


FIG. 2

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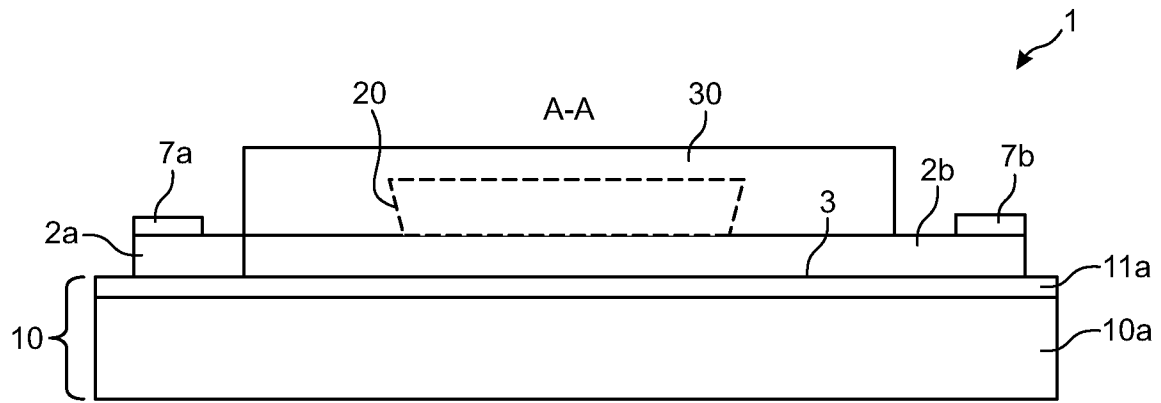


FIG. 3A

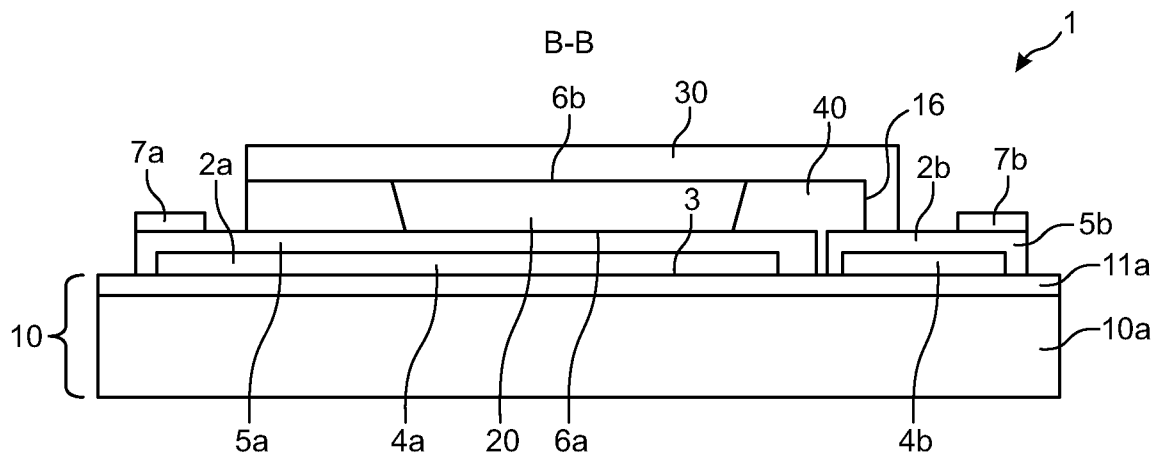


FIG. 3B

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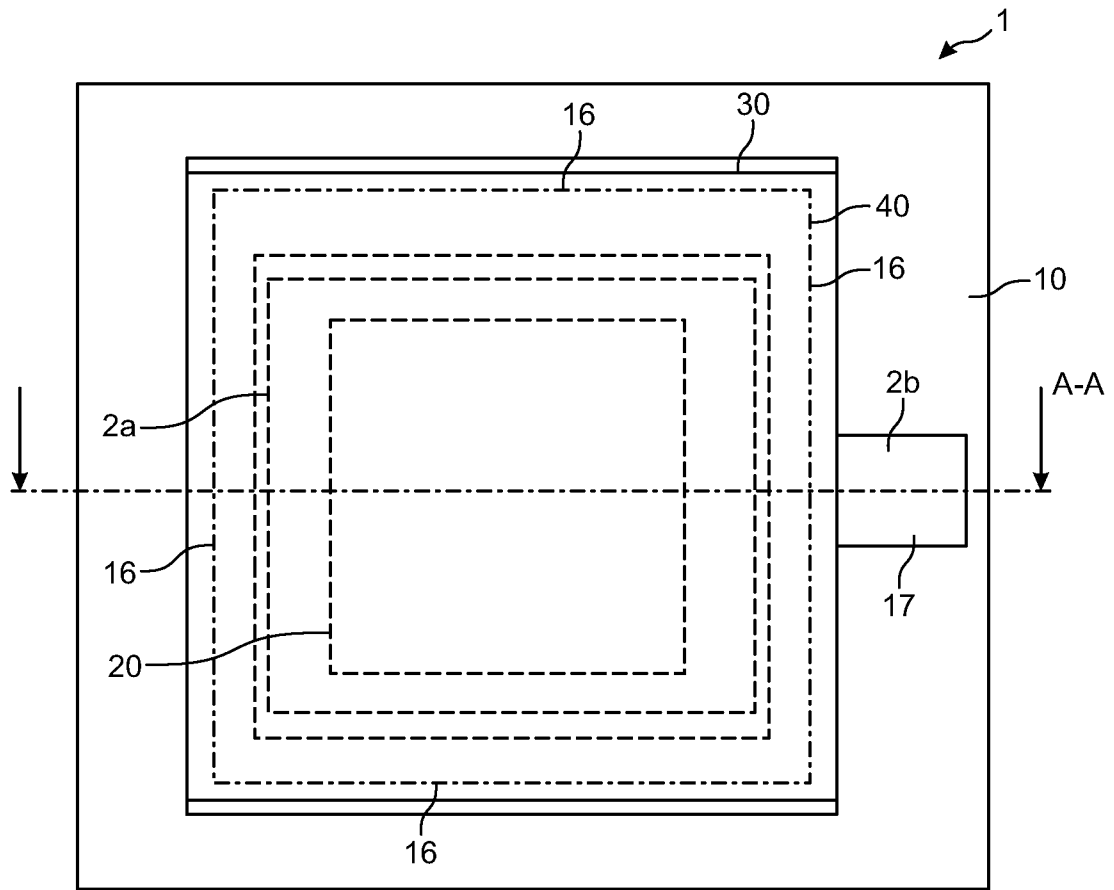


FIG. 4

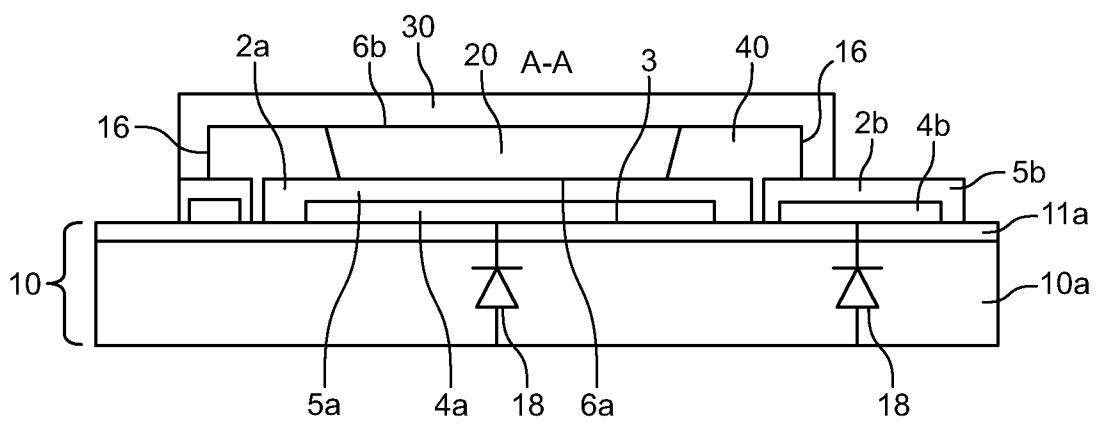


FIG. 5

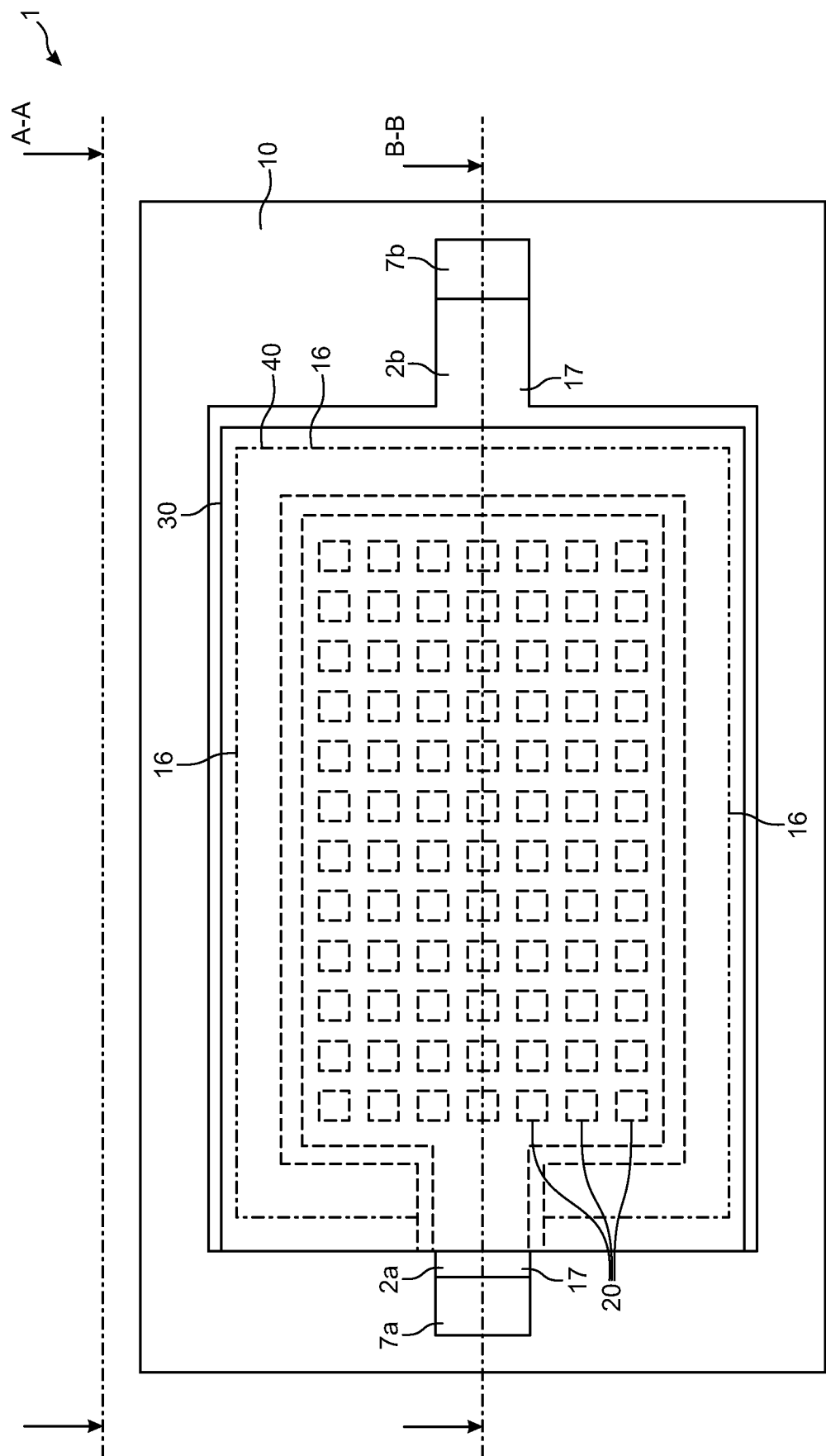


FIG. 6

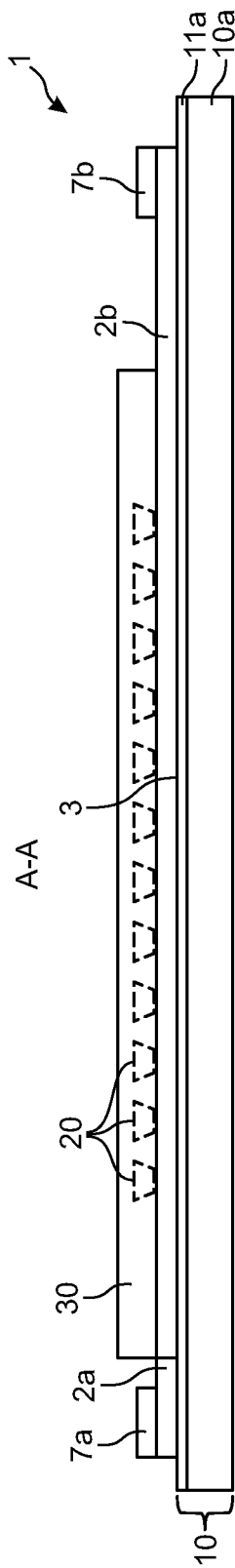


FIG. 7A

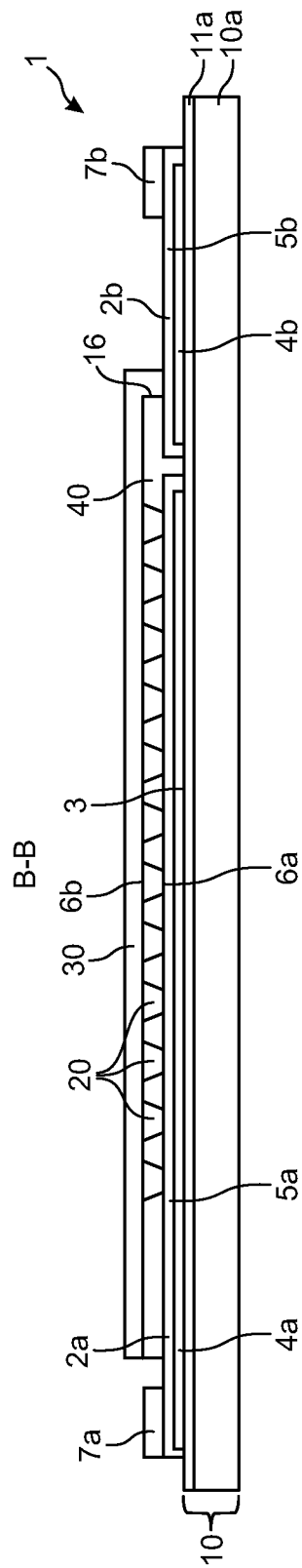


FIG. 7B

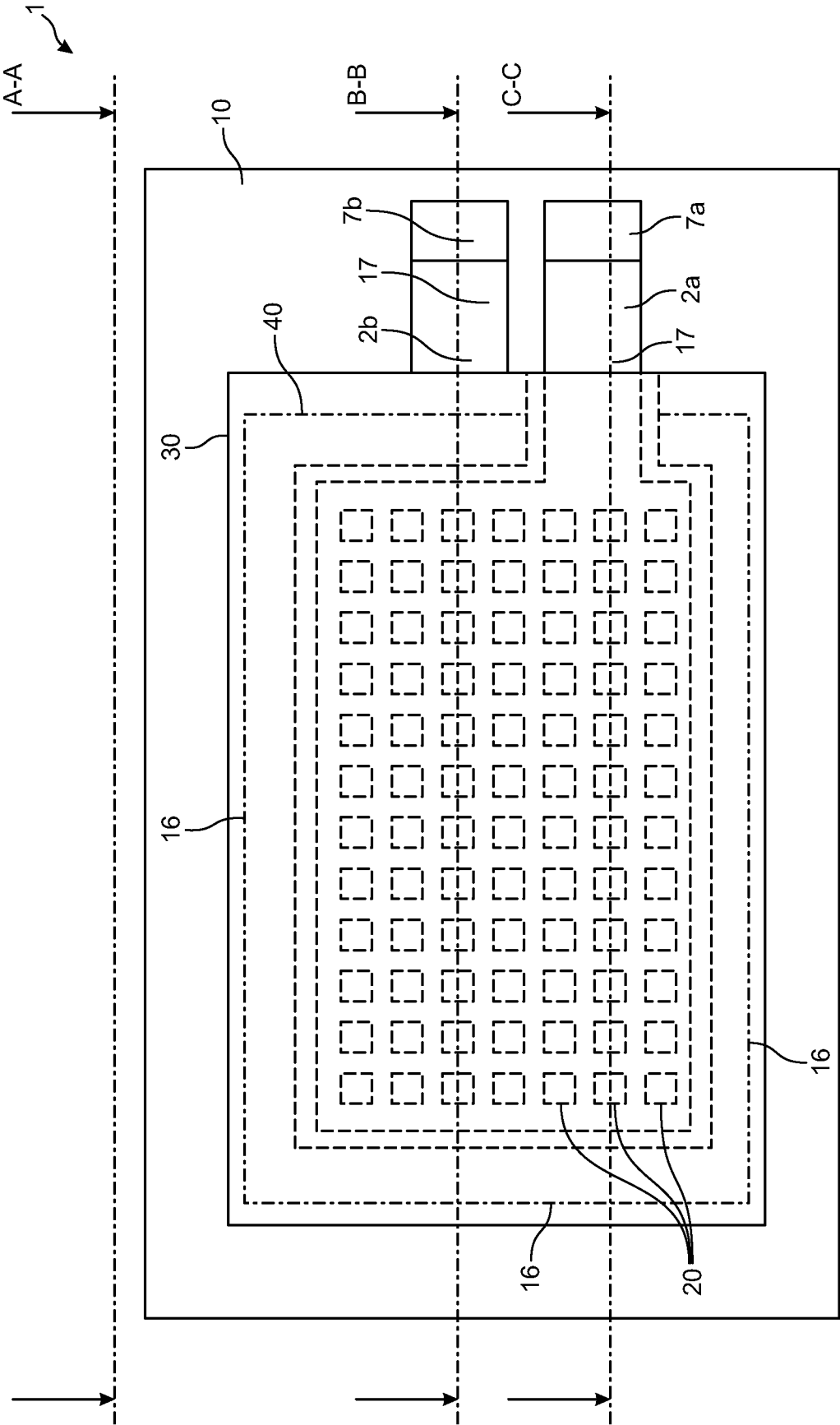


FIG. 8

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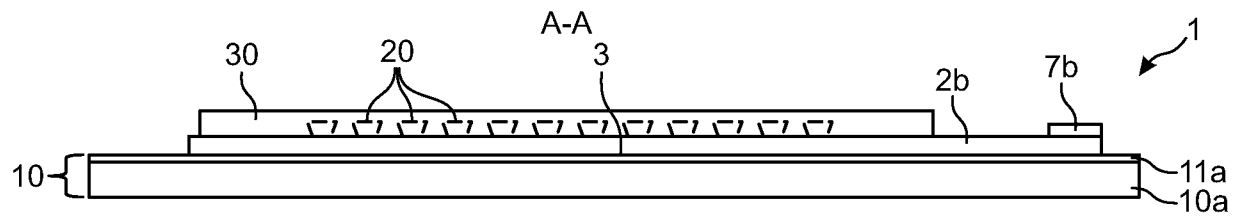


FIG. 9A

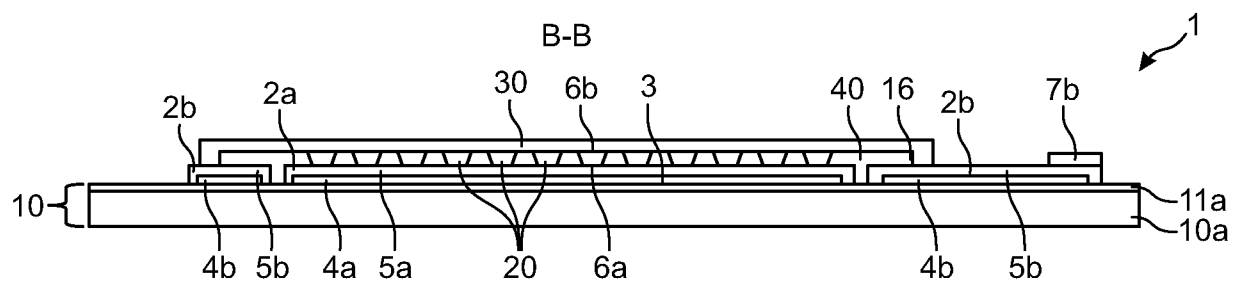


FIG. 9B

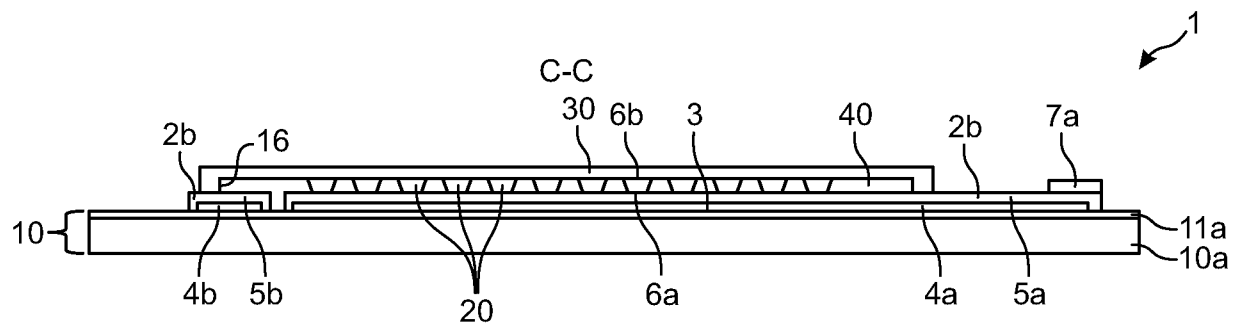


FIG. 9C

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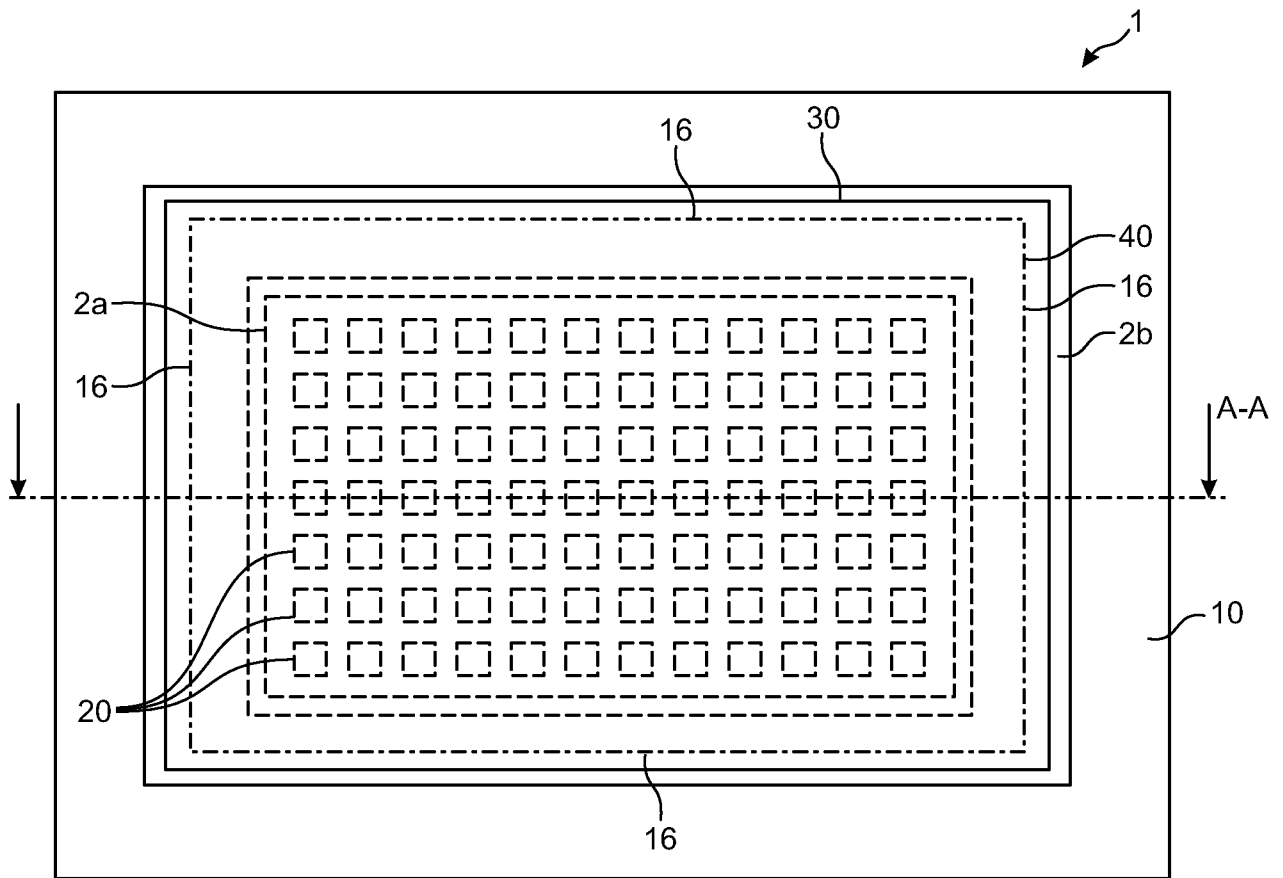


FIG. 10

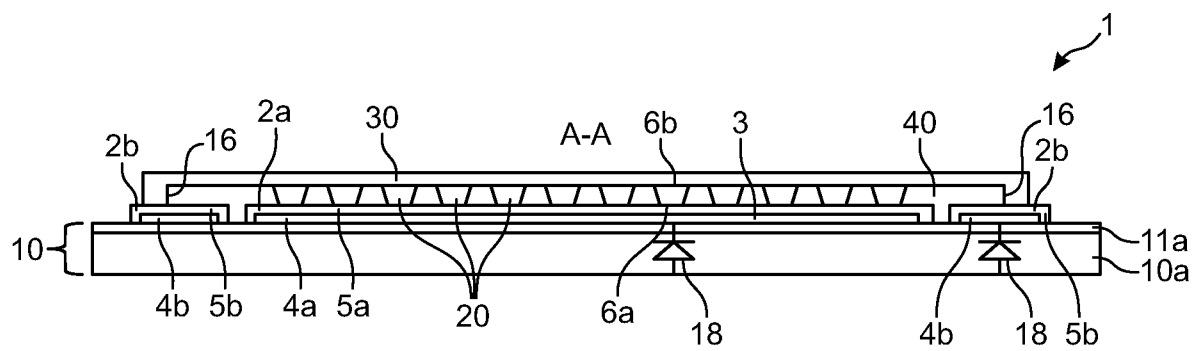


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2023/066004**A. CLASSIFICATION OF SUBJECT MATTER****INV. H01L33/00****ADD.**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, IBM-TDB, WPI Data**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017/269146 A1 (REGAU KILIAN [DE]) 21 September 2017 (2017-09-21) figures 1,2 paragraphs [0056] - [0069], [0121], [0142] -----	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

15 December 2023

Date of mailing of the international search report

05/01/2024

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Adams, Richard

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2023/066004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017269146 A1	21-09-2017	CN 106574944 A	19-04-2017
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