(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 January 2013 (17.01.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/007965 A1

(51) International Patent Classification:
G09G 3/32 (2006.01) *G09G 3/20* (2006.01)

(21) International Application Number:
PCT/GB2012/000557

(22) International Filing Date:
29 June 2012 (29.06.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1111738.9 8 July 2011 (08.07.2011) GB

(71) Applicant *(for all designated States except US)*: **CAMBRIDGE DISPLAY TECHNOLOGY LIMITED** [GB/GB]; Building 2020, Cambourne Business Park, Cambridgeshire CB23 6DW (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SMITH, Euan** [GB/GB]; 10 Rampton Drift, Longstanton, Cambridgeshire CB24 3EH (GB).

(74) Agent: **SHARP, Alan**; c/o IP Department, Cambridge Display Technology Limited, Building 2020, Cambourne Business Park, Cambridgeshire CB23 6DW (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

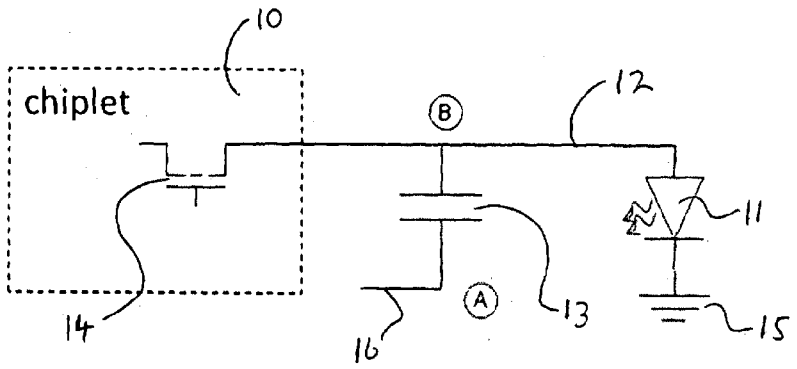
Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: PIXEL DRIVER CIRCUIT FOR ORGANIC ELECTRO - LUMINESCENT DISPLAY

Fig. 1



(57) Abstract: A drive circuit for an OLED comprises: a capacitor having a first terminal and a second terminal, the second terminal connected to an OLED element; a voltage source adapted to selectively provide a control voltage V_P lower than the switch on voltage of the OLED element to the second terminal of the capacitor; and a voltage square wave signal source adapted to provide a square wave voltage signal alternating between a high voltage V_H and a low voltage V_L to the first terminal of the capacitor- The voltage source provides the control voltage V_P to the second terminal of the capacitor when the square wave voltage signal provided to the first terminal of the capacitor is at the low voltage VL; and when the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H, the voltage at the second terminal of the capacitor is increased to a voltage higher than the switch on voltage of the OLED element so that the OLED element emits light.

WO 2013/007965 A1

PIXEL DRIVER CIRCUIT FOR ORGANIC ELECTRO - LUMINESCENT DISPLAY

FIELD OF THE INVENTION

This invention relates to active matrix OLED (Organic Light Emitting Diode) displays, in particular to a system and method for driving pixels of an OLED display.

BACKGROUND

Recent years have seen very substantial growth in the market for displays as the quality of displays improves, their cost falls, and the range of applications for displays increases. This includes both large area displays such as for TVs or computer monitors and smaller displays for portable devices.

The most common classes of display presently on the market are liquid crystal displays and plasma displays although displays based on organic light-emitting diodes (OLEDs) are now increasingly attracting attention due to their many advantages including low power consumption, light weight, wide viewing angle, excellent contrast and potential for flexible displays.

The basic structure of an OLED is a light emissive organic layer, for instance a film of a poly (p-phenylenevinylene) ("PPV") or polyfluorene, sandwiched between a cathode for injecting negative charge carriers (electrons) and an anode for injecting positive charge carriers (holes) into the organic layer. The electrons and holes combine in the organic layer generating photons. In WO90/13148 the organic light- emissive material is a conjugated polymer. In US 4,539,507 the organic light-emissive material is of the class known as small molecule materials, such as (8-hydroxyquinoline) aluminium ("Alq3"). In a practical device one of the electrodes is transparent, to allow the photons to escape the device.

A typical organic light-emissive device ("OLED") is fabricated on a glass or plastic substrate coated with a transparent anode such as indium-tin-oxide ("ITO"). A layer of a thin film of at least one electroluminescent organic material covers the first electrode.

CONFIRMATION COPY

Finally, a cathode is provided over the layer of electroluminescent organic material. The cathode is typically a metal or alloy and may comprise a single layer, such as aluminium, or a plurality of layers such as calcium and aluminium. Additional layers may be provided between the anode and cathode, in particular charge transporting and / or charge blocking layers.

The device may be pixellated with red, green and blue electroluminescent subpixels in order to provide a full colour display.

Full colour liquid crystal displays typically comprise a white-emitting backlight, and light emitted from the device is filtered through red, green and blue colour filters after passing through the LC layer to provide the desired colour image.

A full colour display may be made in the same way by using a white or blue OLED in combination with colour filters. Moreover, it has been demonstrated that use of colour filters with OLEDs even when the pixels of the device already comprises red, green and blue subpixels can be beneficial. In particular, aligning red colour filters with red electroluminescent subpixels and doing the same for green and blue subpixels and colour filters can improve colour purity of the display (for the avoidance of doubt, "pixel" as used herein may refer to a pixel that emits only a single colour or a pixel comprising a plurality of individually addressable subpixels that together enable the pixel to emit a range of colours).

Downconversion, by means of colour change media (CCMs) for absorption of emitted light and reemission at a desired longer wavelength or band of wavelengths, can be used as an alternative to, or in addition to, colour filters.

One way of addressing displays such as LCDs and OLEDs is by use of an "active matrix" arrangement in which individual pixel elements of a display are activated by an associated thin-film transistor. The active matrix backplane for such displays can be made with amorphous silicon (a-Si) or low temperature polysilicon (LTPS). LTPS has high mobility but can be non-uniform and requires high processing temperatures which limits the range of substrates that it can be used with. Amorphous silicon does not

require such high processing temperatures, however its mobility is relatively low, and can suffer from non-uniformities during use due to aging effects. Moreover, backplanes formed from either LTPS or a-Si both require processing steps such as photolithography, cleaning and annealing that can damage the underlying substrate. In the case of LTPS, in particular, a substrate that is resistant to these high-energy processes must be selected.

An alternative approach to patterning is disclosed in, for example, Rogers et al, Appl. Phys. Lett. 2004, 84(26), 5398-5400; Rogers et al Appl. Phys. Lett. 2006, 88, 213101- and Benkendorfer et al, Compound Semiconductor, June 2007, in which silicon on an insulator is patterned using conventional methods such as photolithography into a plurality of elements (hereinafter referred to as "chiplets") which are then transferred to a device substrate. The transfer printing process takes place by bringing the plurality of chiplets into contact with an elastomeric stamp which has surface chemical functionality that causes the chiplets to bind to the stamp, and then transferring the chiplets to the device substrate. In this way, chiplets carrying micro- and nano-scale structures such as display driving circuitry can be transferred with good registration onto an end substrate which does not have to tolerate the demanding processes involved in silicon patterning.

The activation of the individual pixel, or sub-pixel, elements of the display by the associated thin-film transistors can be controlled by the display driving circuitry of the chiplets controlling the amount of charge supplied to the OLED by controlling the current supplied to the OLED. A problem which has been encountered with this approach is that the amount of current passing through the transistors of the display driving circuitry of the chiplets to the OLED display elements can be variable, and the present inventors have found that this variability may be due at least in part to a variation in the conductance (or matching) of the transistors resulting in uneven brightness.

This variation in the amount of current supplied by transistors of different chiplets can arise, for example, because the chiplets are formed from different regions of a semiconductor wafer, or from different wafers, so that there are differences in their performance characteristics due to variations in the manufacturing process.

Conventionally, these differences can be corrected by current mirroring techniques using pairs of transistors formed close together on a single semiconductor wafer so that their properties are closely matched, however this is undesirably costly and complicates the backplane layout.

SUMMARY OF THE INVENTION

According to one aspect of the invention there is provided a drive circuit as specified in claim 1. The drive circuit comprises:

a capacitor having a first terminal and a second terminal, the second terminal being connected to the OLED element;

a voltage source adapted to selectively provide a control voltage V_P lower than the switch on voltage of the OLED element to the second terminal of the capacitor; and

a voltage square wave signal source adapted to provide a square wave voltage signal alternating between a high voltage V_H and a low voltage V_L to the first terminal of the capacitor;

wherein the voltage source provides the control voltage V_P to the second terminal of the capacitor when the square wave voltage signal provided to the first terminal of the capacitor is at the low voltage V_L; and

when the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H, the voltage at the second terminal of the capacitor is increased to a voltage higher than the switch on voltage of the OLED element so that the OLED element emits light.

Preferably, the voltage source comprises or consists of a transistor.

Optionally, the voltage source is a chiplet.

Optionally, the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H, the voltage at the second terminal of the capacitor is increased to a voltage of $V_P + k(V_H - V_L)$, where k is a constant less than one.

Optionally, after the voltage at the second terminal of the capacitor is increased to a voltage higher than the switch on voltage of the OLED element, the circuit is arranged to allow the capacitor to discharge through the OLED element until the voltage of the second terminal of the capacitor reaches the switch on voltage of the OLED element before the square wave voltage signal provided to the first terminal of the capacitor reduces to the low voltage V_L.

Optionally, after the voltage source provides the control voltage the circuit is arranged to allow the capacitor to charge until the voltage of the second terminal of the capacitor reaches the control voltage V_P before the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H.

Optionally, the voltage square wave signal source is adapted to provide a square wave voltage signal spending an equal time at the high voltage V_H and at the low voltage V_L.

Optionally, wherein the voltage square wave signal source is adapted to provide a square wave voltage signal spending a different time at the high voltage V_H and at the low voltage V_L.

Optionally, the drive circuit is to drive a plurality of OLED elements, the drive circuit comprising:

a plurality of capacitors, each having a first terminal and a second terminal, the second terminal of each capacitor being connected to a respective OLED element;

a plurality of voltage square wave sources adapted to provide a plurality of square wave voltage signals, each voltage square wave source providing a respective square wave voltage signal alternating between a high voltage V_H and a low voltage V_L to the

first terminal of a respective one of the plurality of capacitors, the plurality of voltage square wave sources being adapted so that the plurality of square wave voltage signals are out of phase; the voltage source adapted to selectively provide a control voltage V_P to the respective second terminal of each capacitor when the square wave voltage signal provided to the first terminal of said capacitor is at the low voltage V_L.

Optionally, the voltage source is adapted to selectively provide a control voltage V_P to the respective second terminal of each capacitor when the square wave voltage signal provided to the first terminal of said capacitor is at the low voltage V_L, and the square wave voltage signals provided to the first terminals of the other capacitors of the plurality of capacitors is at the high voltage V_H.

Optionally, the drive circuit further comprises a plurality of isolating diodes each arranged to isolate a high voltage at the first terminal of one of said plurality of capacitors from the voltage source.

Optionally, the capacitor comprises a diode arranged to always be in reverse bias.

Optionally, each said capacitor comprises a diode formed in a single stack with the respective OLED.

Optionally, said stack further comprises an isolating diode.

Optionally, the drive circuitry comprises a-Si or LTPS.

In a second aspect the invention provides a backplane of an OLED display comprising a plurality of drive circuits according to any preceding claim.

In a third aspect the invention provides an active matrix display comprising:a backplane according to the second aspect; and a plurality of OLED elements.

Further advantages and novel features can be found in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention and as to how the same may be carried into effect, reference will now be made, by way of example only, to the accompanying drawings, in which:

Figure 1 shows an OLED and a driving circuit according to a first aspect of the present invention;

Figure 2 shows an OLED and driving circuit according to a second embodiment of the invention;

Figure 3 shows a circuit arrangement according to a third embodiment of the invention which can be used in the second embodiment; and

Figure 4 shows a physical structure according to a fourth embodiment of the invention which can be used to provide the third embodiment.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates a drive circuit arrangement according to an embodiment of the present invention. The drive circuit comprises a chiplet 10 of a backplane of an active matrix OLED display which drives a pixel OLED 11. The chiplet 10 is connected to the OLED 11 by a conductive line 12, and the conductive line 12 is also connected to a capacitor 13. The OLED 11 is connected between the conductive line 12 and an earth plane 15.

The capacitor 13 is also connected to a capacitor driver line 16, which is driven with a voltage square wave alternating between a low voltage level V_L and a high voltage level V_H. The low voltage level V_L can conveniently be 0V, but this is not essential.

Thus, the capacitor 13 has a first terminal A connected to the capacitor driver line 16, and a second terminal B connected to the driver circuit of the chiplet 10 and the OLED 11.

In operation, when it is desired to illuminate the OLED 11, a driver circuit of the chiplet 10 is activated when the square wave voltage on the capacitor driver line 16 is at the low

voltage level V_L. The driver circuit typically comprises a transistor 14, and the driver circuit is activated by switching on the transistor 14. The driver circuit applies a control voltage V_P to the terminal B of the capacitor 13, the control voltage V_P is lower than the turn-on voltage of the OLED 11. The chiplet 10 driver circuit is then deactivated by switching off the transistor 14 before the square wave voltage on the capacitor driver line 16 changes to the high voltage level V_H.

When the square wave voltage on the capacitor driver line 16 applied to the terminal A of the capacitor 14 increases to the high voltage level V_H the voltage at the terminal B of the capacitor 13 will also increase. The voltage at the terminal B will increase from V_P to $V_P + k(V_H - V_L)$. Thus, the circuit is driven to act as a charge pump.

The constant k is less than one so that the increase in the voltage at the terminal B will be leas than the difference between V_H and V_L. The value of k is determined by the relative values of parasitic capacitance, which in this example is mainly parasitic capacitance of the OLED 11, and the capacitance of the capacitor 13. In practice the OLED 11 will generally have a relatively large parasitic capacitance because of its geometry. The voltage $k(V_H - V_L)$ is arranged to be lower than the turn on voltage of the OLED 11.

The voltage $V_P + k(V_H - V_L)$ is arranged to be higher than the turn-on voltage of the OLED 11. Accordingly, the capacitor 13 will discharge through the OLED 11 so that charge will flow from the capacitor 12 through the OLED 11 to earth 15, causing the OLED 11 to emit light. This flow of charge will cause the voltage at the terminal B of the capacitor 13 to drop as the capacitor 13 discharges. The charge will continue to flow, and the OLED 11 will remain illuminated, until the voltage at the terminal B is reduced to, or below, the turn-on voltage of the OLED 11.

The voltage at the terminal B may be reduced to the turn-on voltage of the OLED 11, switching off the OLED 11, as a result of the discharge of the capacitor 13 through the OLED 11. In this case the OLED 11 will switch off and stop passing current and emitting light when the voltage at terminal B reaches the turn-off voltage of the OLED 11, and

subsequently the square wave voltage on the capacitor driver line 16 will transition back to V_L.

Alternatively, the voltage at the terminal B may be reduced below the turn-on voltage of the OLED 11, switching off the OLED 11, by the transition of the square wave voltage on the capacitor driver line 16 back to V_L. This transition will reduce the voltage at the terminal B to below V_P, which is below the turn-on voltage of the OLED 11.

Which of these two alternatives will be followed by any particular system in practice will depend on the specific parameter values of the different parts of the system, for example the voltage and frequency values of the square wave voltage.

Once the square wave voltage on the capacitor driver line 16 has changed back to V_L the cycle is repeated.

When it is not desired to illuminate the OLED 11, the driver circuit in the chiplet 10 is not activated. Accordingly, when the square wave voltage increases to V_H the voltage at the terminal B of the capacitor 13 only increases to $k(V_H - V_L)$, which is below the turn on voltage of the OLED 11.

In the present invention the amount of charge passing through the OLED 11, and thus the amount of light emitted, during each cycle of the square wave voltage signal will be proportional to the voltage difference $V_H - V_L$ and the capacitance of the capacitor 13. Provided that the current passing through the transistor 14 of the chiplet 10 is sufficient to charge the terminal B of the capacitor 13 to the control voltage V_P during the period when the square wave voltage signal is at the low voltage V_L, the variation in the conductance (or matching) of transistor 14 has no effect on the amount of charge passing through the OLED 11.

In practice it is straightforward to design the drive circuit to have values for the voltages, currents, capacitances and square wave signal frequency which will ensure that the range of variation in the current passed by the chiplets 10 encountered in practice will still allow the terminal B of the capacitor 13 to be charged to the control voltage V_P during the

period when the square wave voltage signal is at the low voltage V_L. It will be understood that this allows a much larger range of currents passed by the chiplets 10 to be tolerated without affecting the performance of the OLED display than a convention arrangement where the chiplets 10 drive the OLEDs directly.

It is expected that it will usually be preferred to arrange for the capacitor 13 to be discharged to the switch-off voltage of the OLED 11 before the square wave voltage signal makes the transition back to the low voltage VL. This will ensure that the matching of the transistor 14 has no effect on the amount of charge passing through the OLED 11.

In practice it is straightforward to design the drive circuit to have values for the voltages, currents, capacitances and square wave signal frequency which will ensure that the range of variation in the current passed by the OLED 11 encountered in practice will still allow the terminal B of the capacitor 13 to be discharged to the switch on voltage of the OLED 11 during the period when the square wave voltage signal is at the high voltage V_H.

Over time, the charge passing through the OLED 11, and thus the amount of light emitted, will be proportional to the voltage difference $V_H - V_L$, the capacitance of the capacitor 13, the frequency of the square wave drive signal, and the number of cycles of the square wave drive signal for which the driver circuit in the chiplet 10 is activated to apply control voltage V_P to the terminal B of the capacitor 13. Thus, provided that the frequency of the square wave voltage is sufficiently high that persistence of vision will cause the OLED 11 to appear to be continuously illuminated to a human observer, the apparent, or perceived brightness of the OLED 11 can be controlled by changing the proportion of the cycles of the square wave voltage for which the chiplet 10 is activated to switch on the OLED 11, or by changing the frequency of the square wave voltage signal. The frequency of the square wave voltage signal may be referred to as the pump rate.

In order to ensure that the drive circuit is operating correctly and that the capacitor 13 is charged to the control voltage V_P while the square wave voltage signal is at the low voltage V_L, before the square wave voltage signal transitions to the high voltage V_H, and

also that the capacitor 13 is fully discharged to the switch-off voltage of the OLED 11 while the square wave voltage signal is at the high voltage V_H, before the square wave voltage signal transitions to the low voltage V_L, the current being drawn by the circuit can be monitored. The relationship between the current drawn and the frequency of the square wave signal can then be assessed to confirm that this is a linear relationship. Any nonlinearity identified can then be corrected for. The assessment can also take into account changes in the voltages V_P, V_H and V_L, and the proportion of cycles of the square wave voltage signal for which the chiplet 10 switches the OLED 11 on, if necessary.

It is not necessary that the square wave voltage signal spends equal lengths of time at the high voltage V_H and at the low voltage V_L. In some circumstances it may be convenient to have the time at the high voltage V_H different from the time at the low voltage V_L in order to allow the desired charging and discharging of the capacitor 13 to be completed before the square wave voltage signal changes state. In one arrangement, V_L is as short as possible in order to maximise the duty cycle of the OLED.

For simplicity and clarity only a single chiplet 10, OLED 11 and capacitor 13 are shown in figure 1. However, it will be appreciated that an active matrix OLED display will typically comprise a large number of chiplets driving a large number OLEDs. Further, it will be appreciated that each chiplet may drive one or a plurality of pixels or subpixels; that the pixels or subpixels driven by a given chiplet may have the same or different colours; and that a pixel driven by a given chiplet may comprise subpixels other than red, green and blue subpixels.

In an OLED display comprising a plurality of chiplets driving a plurality of OLED's, there may be a number of drive circuit arrangements as described above driven by a single square wave voltage. Conveniently, this can be arranged by connecting the second terminals B of the capacitors of the different drive circuits to a common square wave voltage line. All of the OLEDs making up the display could be driven by a common square wave voltage line, alternatively, a number of square wave voltage lines could be provided, with each square wave voltage line driving all of the OLEDs in a particular line, column or region of the display.

This driving arrangement provides a number of advantages. The amount of charge passing through the OLED, and thus the amount of light emitted by the OLED and its brightness, is controlled by the voltages V_P, V_H and V_L and the capacitance of the capacitor 13, and not by the amount of current passing through the transistor 14 of the chiplet 10. As is well known to the person skilled in the art, it is much easier to control the voltage and capacitance of electronic, and particularly microelectronic, components to specific desired values, and keep them constant, than it is to control the current passed by devices. Accordingly, the problem of variations between the current passed by different chiplets affecting the appearance of an OLED display does not generally arise, because variations in the current passed by the different chiplets does not directly affect the luminosity of their respective OLEDs.

Further, since the amount of charge passing through the OLED, and thus the amount of light emitted, is controlled by changing the voltages V_P, V_H and V_L the present invention allows the amount of charge to be controlled by setting appropriate reference voltages, which are easier to distribute across the display than reference currents.

The brightness or greyscale of the OLED 11 can be controlled by varying the number, or proportion, of cycles of the square wave voltage for which the chiplet 10 is switched on to illuminate the OLED 11.

In an OLED display comprising a plurality of OLED's the global brightness or greyscale of the OLED display as a whole can be varied and controlled by adjusting the voltage difference $V_H - V_L$. When the low voltage V_L is 0V, this can conveniently be done by adjusting the high voltage V_L. The brightness or greyscale of the individual OLEDs can be separately controlled by varying the number of cycles of the square wave voltage for which they are illuminated, as explained above.

Advantageously, a separate square wave voltage can be provided to the pixels, or subpixels, of each colour on the display, for example providing a separate square wave voltage to each of the Red, Green and Blue pixels, or subpixels. The global colour balance of the OLED display as a whole can be varied and controlled by adjusting the

voltage difference $V_H - V_L$ of each of the separate colour dedicated square wave voltages. Conveniently, each of the separate colour dedicated square wave voltages can be supplied through a dedicated square wave voltage line connected to the pixels, or subpixels, of the relevant colour.

A further advantage of the present invention is that there is no requirement to adjust the voltage or current supplied by the chiplet 10 through the transistor 14 in order to control or adjust the brightness of the OLED 11. In a conventional drive arrangement where the current passing through the chiplet transistor directly controls the brightness of the OLED, it is necessary to provide analogue components in the chiplet to allow the OLED brightness to be adjusted, typically by adjusting the output voltage of the transistor 14. Such analogue components are large and complex compared to the digital components required to just switch the transistor on and off, so that including such analogue components to the chiplet is expensive and undesirable. Further, in such a conventional drive arrangement it is generally necessary to set the voltage supplied by the chiplet to be below the drive voltage of the display, typically by about 1V, in order to allow the drive voltages of the individual chiplets to be adjusted to control the supplied current. In contrast, in the present invention the control voltage V_P can be kept constant at the drive voltage of the display.

Figure 2 illustrates a drive circuit arrangement according to another embodiment of the present invention. The drive circuit comprises a chiplet 20 of a backplane of an active matrix OLED display which drives three pixel OLEDs 21a-c. The chiplet 20 is connected to each of the three OLEDs 21a-c by a respective conductive line 22a-c, and each conductive line 22a-c is also each connected to a second terminal B of a respective capacitor 23a-c. Each capacitor 23a-c has a first terminal A connected to a respective capacitor driving line 26a-c. Each OLED 21a-c is connected between the respective conductive line 22a-c and an earth plane 25. Each capacitor 23a-c and OLED 21a-c is isolated from the chiplet 20 by a respective isolating diode 27a-c having its cathode connected to the second terminal B of the capacitor 23a-c.

Similarly to the embodiment of figure 1, each of the three capacitors 23a-c is driven to act as a charge pump by a respective voltage square wave alternating between a low voltage level V_L and a high voltage level V_H, which is supplied to the first terminal A of the capacitor 23a-c by the respective capacitor driving line 26a-c. The three square wave driving voltages are out of phase with one another so that only one of the three square wave signals is at the low voltage level V_L at any time.

The drive circuit of the chiplet 20 is switched in synchrony with the three square wave driving voltages so that the chiplet 20 supplies the control voltage V_P to the second terminal B of the capacitor 23a-c connected to the one of the OLEDs 21a-c which it is desired to illuminate when the respective voltage square wave supplied to the first terminal A of that capacitor 23a-c is at the low voltage level V_L.

The voltage of the second terminal B of this capacitor 23a-c is then raised to $V_P + k(V_H - V_L)$ when the respective voltage square wave supplied to the first terminal A of that capacitor 23a-c transitions to the high voltage level V_H, causing charge to flow through the desired OLED 21a-c, illuminating it.

When the voltage of a terminal A of a capacitor 23a-c is raised to $V_P + k(V_H - V_L)$, the respective diode 27a-c isolates the capacitor 23a-c from the other capacitors 23a-c, and from the chiplet 20, ensuring that the different OLEDs 21a-c can be independently driven without any "cross-talk" between them.

Accordingly, this embodiment allows three OLEDs 21a-c to be separately controlled and addressed by a single drive circuit, for example a single transistor 24, of a single chiplet 20.

This embodiment provides the advantage that the number of chiplets on the backplane of the display can be reduced relative to the number of independently controllable pixels, or sub-pixels, making up the OLED display. This allows the number of chiplets to be reduced, allowing the cost of the backplate to be reduced. It will be understood that the cost of chiplets, or other semiconductor microelectronic circuits, is relatively high compared to the cost of other parts of the backplate.

This embodiment has a single chiplet independently controlling three pixel, or sub-pixel, OLEDs, the controlling of three pixels, or sub-pixels, is only an example and different numbers of pixels, or sub-pixels, such as two, four, or more, could be independently controlled.

In the above embodiment the square wave driving voltages are out of phase with one another so that only one of the square wave signals is at the low voltage level V_L at any time. This is convenient, but not essential. It is possible for more than one of the voltage signals to be at the low voltage level V_L at the same time provided that the chiplet 20 is not supplying the control voltage V_P at this time. The general requirement in order to allow independent control of the different OLEDs is that only one of the square wave signals is at the low voltage level V_L at any time when the chiplet 20 is supplying the control voltage V_P. Moreover, any two of diodes 27a, 27b and 27c are arranged back-to-back and so current cannot flow between any of capacitors 23a, 23b and 23c.

The above embodiments show one OLED being driven by a single chiplet or three OLEDs being independently driven by a single chiplet. It will be understood that a plurality of OLEDs connected in parallel could be driven simultaneously by a single chiplet.

Figure 3 illustrates a third embodiment of the invention comprising a specific arrangement of a part of the drive circuit arrangement according to the second embodiment.

In figure 3 a capacitor corresponding to the capacitors 23a-c of the second embodiment, is formed by a diode 33 arranged with its cathode 33b connected to an OLED 31 through a conductive line 32, and its anode 33a connected to a capacitor driving line 36. The diode 33 will be permanently reverse biased during operation, and accordingly, the diode 33 will act as a capacitor.

An isolation diode 37 having an anode 37a and a cathode 37b is provided to isolate the diode 33 from the chiplet 10, the two diodes 33 and 37 having their respective cathodes

33b and 37b connected together by the conductive line 32. The anode 37a of the diode 37 provides a terminal C for connection to a chiplet.

The diodes 33 and 37 can conveniently be hole-only devices based on a similar material to the OLEDs.

Figure 4 illustrates a fourth embodiment of the invention comprising a possible physical structure for the third embodiment.

The conductive line 32 of the third embodiment provides a common connection between the cathodes 33a and 37a of the diodes 33 and 37 and the OLED 31. This common connection is at a floating voltage, and so does not need to be isolated from the diodes 33 and 37 and the OLED 31. Accordingly, the diodes 33 and 37 and the OLED 31 can be formed as a single stack.

In figure 4, a stack 40 comprises an OLED 31 formed by an OLED semiconductor layer 41 sandwiched between a first conductive layer 42 and a second conductive layer 43. The second conductive layer 43 provides the earth plane. The stack 40 further comprises diodes 33 and 37 formed by a diode semiconductor layer 44 sandwiched between the first conductive layer 42 and a third conductive layer 45. The third conductive layer 45 is patterned to define the anodes 33a and 37a of the diodes 33 and 37, and provide the terminals A and C for connection to the capacitor driving line and the chiplet.

The fourth embodiment provides a compact and easily fabricated structure for the combined OLED and diodes.

The third and fourth embodiments relate an arrangement according to the second embodiment where the capacitor is provided by a diode arranged to always be reverse biased. It will be understood that the capacitor of the first embodiment could also be replaced

The chiplets may be formed from semiconductor wafer sources, including bulk semiconductor wafers such as single crystalline silicon wafers, polycrystalline silicon

wafers, germanium wafers; ultra thin semiconductor wafers such as ultra thin silicon wafers; doped semiconductor wafers such as p-type or n-type doped wafers and wafers with selected spatial distributions of dopants; semiconductor on insulator wafers such as silicon on insulator (e.g. Si-SiO2, SiGe); and semiconductor on substrate wafers such as silicon on substrate wafers. In addition, printable semiconductor elements of the present invention may be fabricated from a variety of nonwafer sources, such as a thin films of amorphous, polycrystalline and single crystal semiconductor materials (e.g. polycrystalline silicon, amorphous silicon, polycrystalline GaAs and amorphous GaAs) that is deposited on a sacrificial layer or substrate (e.g. SiN or SiO2) and subsequently annealed, and other bulk crystals, including, but not limited to, graphite, MoSe2 and other transition metal chalcogenides, and yttrium barium copper oxide.

The chiplets may be formed by conventional processing means known to the skilled person.

Preferably, each chiplet is up to 500 microns in length, preferably between about 15-250 microns, and preferably about 5-50 microns in width, more preferably 5-10 microns.

Transfer Process

The stamp used in transfer printing is preferably a PDMS stamp.

The surface of the stamp may have a chemical functionality that causes the chiplets to reversibly bind to the stamp and lift off the donor substrate, or may bind by virtue of, for example, van der Waals force. Likewise upon transfer to the end substrate, the chiplets adhere to the end substrate by van der Waals force and / or by an interaction with a chemical functionality on the surface of the end substrate, and as a result the stamp may be delaminated from the chiplets.

Chiplet and Display Integration

The chiplets patterned with drive circuitry for addressing pixels or subpixels of a display may be transfer-printed onto a substrate carrying tracking for connection of the chiplets to

a power source and, if required, drivers outside the display area for programming the chiplets.

To ensure accurate transfer onto a prepared end substrate, the stamp and end substrate may be registered by means known to the skilled person, for example by providing alignment marks on the substrate.

Alternatively, tracking for connection of the chiplets may be applied after the chiplets have been transfer printed.

In the case where the chiplets drive a display such as an LCD or OLED display, the backplane comprising the chiplets is preferably coated with a layer of insulating material to form a planarisation layer onto which the display is constructed. Electrodes of the display device are connected to the output of the chiplets by means of conducting through-vias formed in the planarisation layer.

Organic LED

In the case where the display is an OLED, the device according to the invention comprises a glass or plastic substrate onto which the backplane (not shown) has been formed, an anode and a cathode. An electroluminescent layer is provided between anode and cathode.

In a practical device, at least one of the electrodes is semi-transparent in order that light may be emitted. Where the anode is transparent, it typically comprises indium tin oxide. Preferably, the cathode is transparent in order to avoid the problem of light emitted from the electroluminescent layer being absorbed by the chiplets and other associated drive circuitry in the case where light is emitted through the anode. A transparent cathode typically comprises a layer of an electron injecting material that is sufficiently thin to be transparent. Typically, the lateral conductivity of this layer will be low as a result of its thinness. In this case, the layer of electron injecting material is used in combination with a thicker layer of transparent conducting material such as indium tin oxide.

It will be appreciated that a transparent cathode device need not have a transparent anode (unless, of course, a fully transparent device is desired), and so the transparent anode used for bottom-emitting devices may be replaced or supplemented with a layer of reflective material such as a layer of aluminium. Examples of transparent cathode devices are disclosed in, for example, GB 2348316.

Suitable materials for use in the electroluminescent layer include small molecule, polymeric and dendrimeric materials, and compositions thereof. Suitable electroluminescent polymers for use in the electroluminescent layer include poly(arylene vinylenes) such as poly(p-phenylene vinylenes) and polyarylenes such as: polyfluorenes, particularly 2,7-linked 9,9 dialkyl polyfluorenes or 2,7-linked 9,9 diaryl polyfluorenes; polyspirofluorenes, particularly 2,7-linked poly-9,9-spirofluorene; polyindenofluorenes, particularly 2,7-linked polyindenofluorenes; polyphenylenes, particularly alkyl or alkoxy substituted poly-1,4-phenylene. Such polymers as disclosed in, for example, Adv. Mater. 2000 12(23) 1737-1750 and references therein. Suitable electroluminescent dendrimers for use in layer 3 include electroluminescent metal complexes bearing dendrimeric groups as disclosed in, for example, WO 02/066552.

Further layers may be located between the anode and the cathode, such as charge transporting, charge injecting or charge blocking layers.

The device is preferably encapsulated with an encapsulant (not shown) to prevent ingress of moisture and oxygen. Suitable encapsulants include a sheet of glass, films having suitable barrier properties such as alternating stacks of polymer and dielectric as disclosed in, for example, WO 01/81649 or an airtight container as disclosed in, for example, WO 01/19142. A getter material for absorption of any atmospheric moisture and / or oxygen that may permeate through the substrate or encapsulant may be disposed between the substrate and the encapsulant.

Those skilled in the art will appreciate that while this disclosure has described what is considered to be the best mode and, where appropriate, other modes of performing the invention, the invention should not be limited to the specific configurations and methods disclosed in this description of the preferred embodiment

CLAIMS

1. A drive circuit for an organic light emitting diode 'OLED' element, the drive circuit comprising:

a capacitor having a first terminal and a second terminal, the second terminal being connected to the OLED element;

a voltage source adapted to selectively provide a control voltage V_P lower than the switch on voltage of the OLED element to the second terminal of the capacitor; and

a voltage square wave signal source adapted to provide a square wave voltage signal alternating between a high voltage V_H and a low voltage V_L to the first terminal of the capacitor;

wherein the voltage source provides the control voltage V_P to the second terminal of the capacitor when the square wave voltage signal provided to the first terminal of the capacitor is at the low voltage V_L; and

when the square wave voltage signal provided to the first terminal of the capacitor is at the high voltage V_H, the voltage at the second terminal of the capacitor is higher than the switch on voltage of the OLED element so that the OLED element emits light.

2. A drive circuit according to claim 1 wherein the voltage source is a transistor.

3. A drive circuit according to claim 1 or 2 wherein the voltage source is a chiplet.

4. The drive circuit according to any preceding claim wherein, when the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H, the voltage at the second terminal of the capacitor is increased to a voltage of $V_P + k(V_H - V_L)$, where k is a constant less than one.

5. The drive circuit according to any preceding claim wherein after the voltage at the second terminal of the capacitor is increased to a voltage higher than the switch on voltage of the OLED element, the circuit is arranged to allow the capacitor to discharge

through the OLED element until the voltage of the second terminal of the capacitor reaches the switch on voltage of the OLED element before the square wave voltage signal provided to the first terminal of the capacitor reduces to the low voltage V_L.

6. The drive circuit according to any preceding claim wherein after the voltage source provides the control voltage the circuit is arranged to allow the capacitor to charge until the voltage of the second terminal of the capacitor reaches the control voltage V_P before the square wave voltage signal provided to the first terminal of the capacitor increases to the high voltage V_H.

7. The drive circuit according to any preceding claim wherein the voltage square wave signal source is adapted to provide a square wave voltage signal spending an equal time at the high voltage V_H and at the low voltage V_L.

8. The drive circuit according to any one of claims 1 to 7 wherein the voltage square wave signal source is adapted to provide a square wave voltage signal spending a different time at the high voltage V_H and at the low voltage V_L.

9. The drive circuit according to any preceding claim to drive a plurality of OLED elements, the drive circuit comprising:

a plurality of capacitors, each having a first terminal and a second terminal, the second terminal of each capacitor being connected to a respective OLED element;

a plurality of voltage square wave sources adapted to provide a plurality of square wave voltage signals, each voltage square wave source providing a respective square wave voltage signal alternating between a high voltage V_H and a low voltage V_L to the first terminal of a respective one of the plurality of capacitors, the plurality of voltage square wave sources being adapted so that the plurality of square wave voltage signals are out of phase;

the voltage source adapted to selectively provide a control voltage V_P to the respective second terminal of each capacitor when the square wave voltage signal provided to the first terminal of said capacitor is at the low voltage V_L.

10. The drive circuit according to claim 9 wherein the voltage source is adapted to selectively provide a control voltage V_P to the respective second terminal of each capacitor when the square wave voltage signal provided to the first terminal of said capacitor is at the low voltage V_L, and the square wave voltage signals provided to the first terminals of the other capacitors of the plurality of capacitors is at the high voltage V_H.

11. The drive circuit according to claim 9 or claim 10 and further comprising a plurality of isolating diodes each arranged to isolate a high voltage at the first terminal of one of said plurality of capacitors from the voltage source.

12. The drive circuit according to any preceding claim wherein the capacitor comprises a diode arranged to always be in reverse bias.

13. The drive circuit according to claim 12 wherein each said capacitor comprises a diode formed in a single stack with the respective OLED.

14. The drive circuit according to claim 13 wherein said stack further comprises an isolating diode.

15. The drive circuit according to any preceding claim wherein the drive circuitry comprises a-Si or LTPS.

16. A backplane of an OLED display comprising:
a plurality of drive circuits according to any preceding claim.

17. An active matrix display comprising:
a backplane according to claim 16; and
a plurality of OLED elements.

Fig. 1

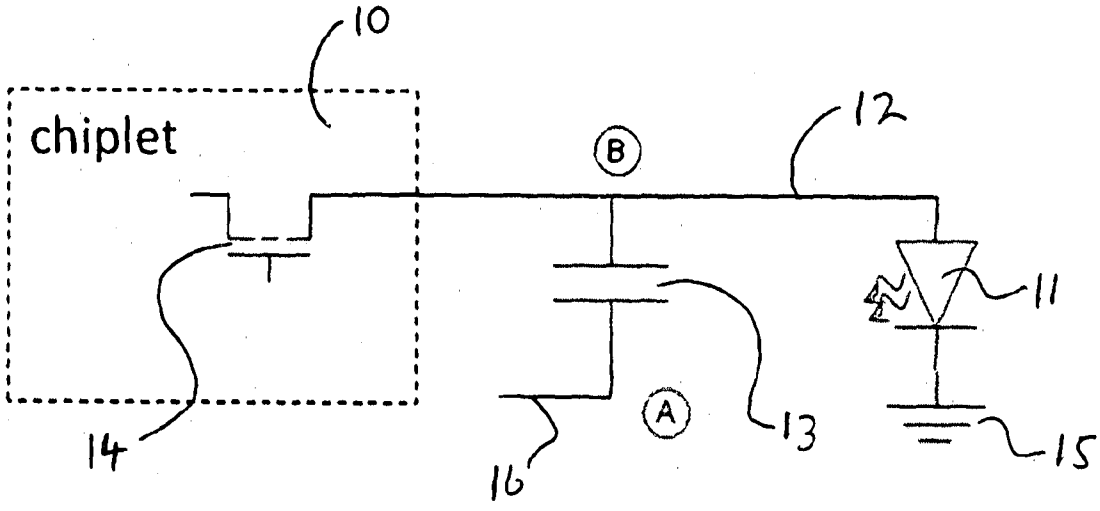

10
chiplet
12
B
11
13
A
14
16
15

Fig. 2

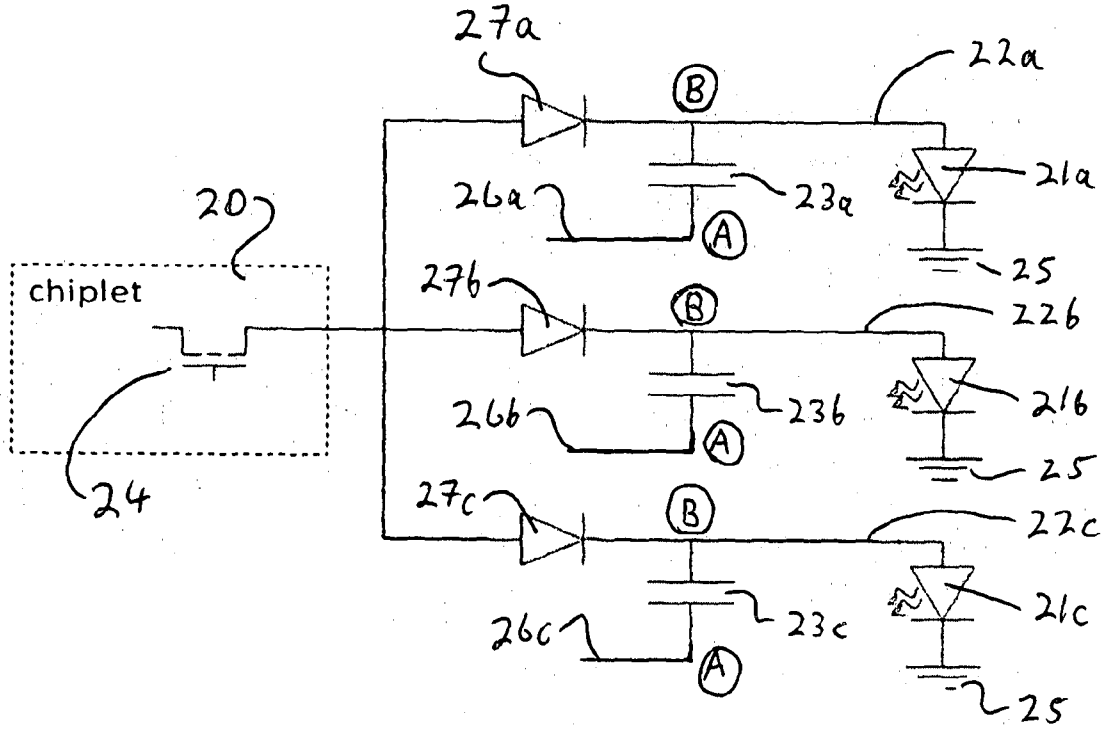

27a
22a
B
21a
23a
26a
A
20
25
chiplet
27b
22b
B
21b
23b
26b
A
24
25
27c
22c
B
21c
23c
26c
A
25

Fig. 3

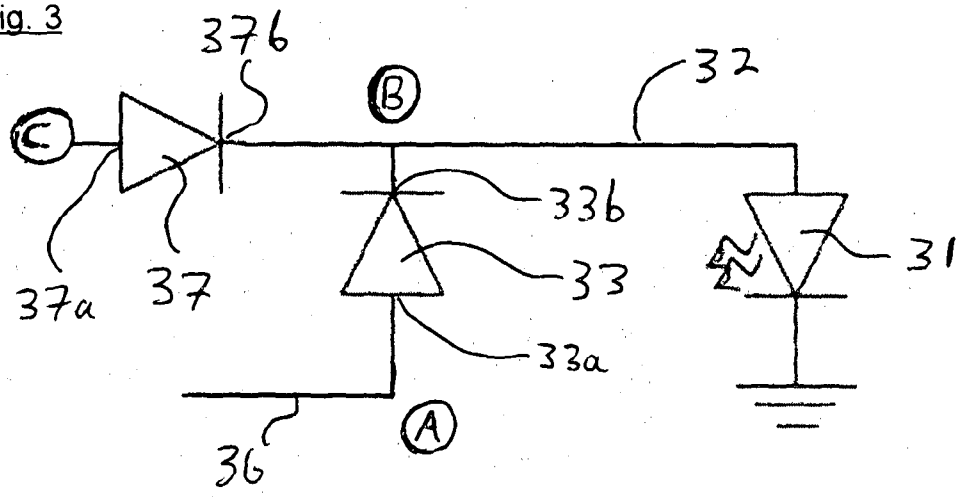
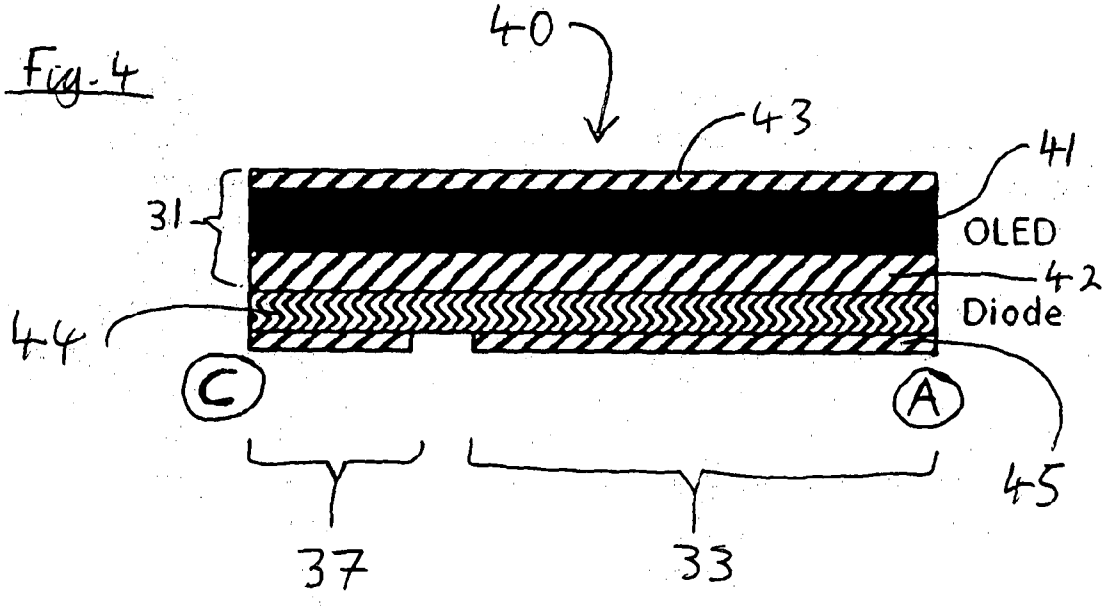

376
B
32
C
336
31
37a
37
33
33a
36
A

Fig. 4


40
43
41
31
OLED
42
Diode
44
C
A
45
37
33

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2012/000557

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/32 G09G3/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/263436 A1 (OKUDA YOSHIYUKI [JP]) 30 December 2004 (2004-12-30) paragraphs [0021] - [0039]; figure 2	1-17
X	US 2006/092148 A1 (OZAWA TOKURO [JP] ET AL) 4 May 2006 (2006-05-04) paragraphs [0045] - [0049], [0091], [0092]; figures 2,3	1-17
A	US 6 429 601 B1 (FRIEND RICHARD H [GB] ET AL) 6 August 2002 (2002-08-06) paragraph [0045]; figure 1	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 November 2012	12/11/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Bellatalla, Filippo

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2012/000557

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004263436 A1	30-12-2004	AU 2002328062 A1	01-04-2003
		CN 1555549 A	15-12-2004
		EP 1430468 A2	23-06-2004
		JP 2005503588 A	03-02-2005
		US 2004263436 A1	30-12-2004
		WO 03025894 A2	27-03-2003
US 2006092148 A1	04-05-2006	JP 4186961 B2	26-11-2008
		JP 2006154730 A	15-06-2006
		US 2006092148 A1	04-05-2006
US 6429601 B1	06-08-2002	AU 2529099 A	06-09-1999
		CN 1291321 A	11-04-2001
		EP 1057167 A1	06-12-2000
		JP 2002504717 A	12-02-2002
		US 6429601 B1	06-08-2002
		WO 9942983 A1	26-08-1999