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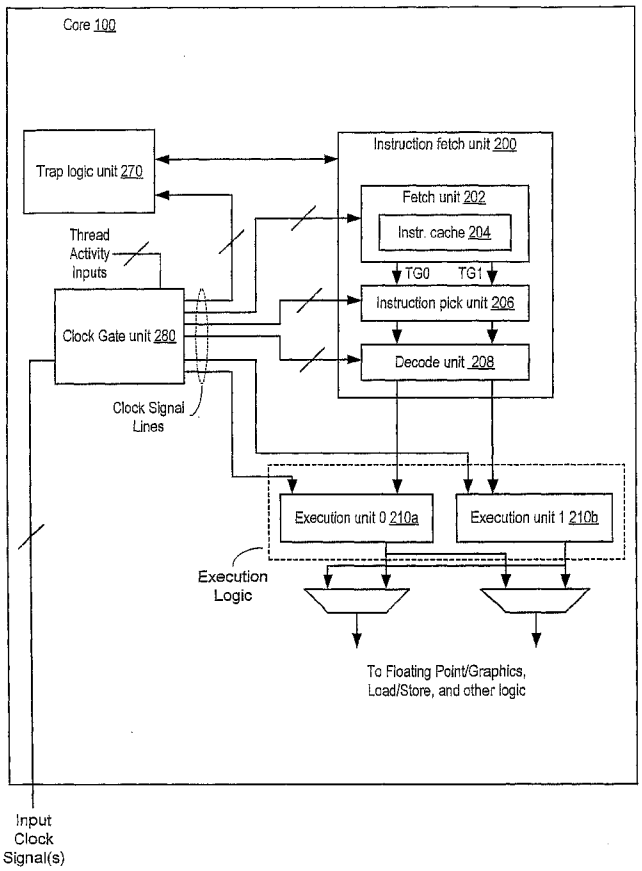
(54) Title: THREAD-BASED CLOCK ENABLING IN A MULTI-THREADED PROCESSOR



(57) Abstract: A method and apparatus for controlling power consumption in a multi-threaded processor. In one embodiment, the processor includes at least one logic unit for processing instructions. The logic unit includes a plurality of positions, wherein each of the plurality of positions corresponds to at least one instruction thread. Clock signals may be provided to the logic unit via a clock gating unit. The clock gating unit is configured to inhibit a clock signal from being provided to a corresponding one of the thread positions when no instruction thread is active for that position. The inhibiting of the clock signal for an inactive thread position may reduce power consumption by the processor.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 272 616 B1 (FERNANDO JOHN S ET AL) 7 August 2001 (2001-08-07) the whole document	1-3, 8-12,17, 18
X	US 2003/037226 A1 (TSURUTA TORU ET AL) 20 February 2003 (2003-02-20) the whole document	1-3, 8-12,17, 18
A	US 2002/095614 A1 (RODGERS DION ET AL) 18 July 2002 (2002-07-18) page 5, paragraph 60 - paragraph 62 page 11, paragraph 132 - paragraph 135 page 15, paragraph 170 - page 16, paragraph 183	1-18

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHANG A ET AL: "The effects of explicitly parallel mechanisms on the multi-ALU processor cluster pipeline" COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, 1998. ICCD '98. PROCEEDINGS. INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 5-7 OCT. 1998, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 5 October 1998 (1998-10-05), pages 474-481, XP010310318 ISBN: 0-8186-9099-2 the whole document	4-7, 13-16
A	US 5 742 782 A (ITO ET AL) 21 April 1998 (1998-04-21) the whole document	1-18

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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