(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 124 216 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
16.08.2001 Bulletin 2001/33

(51) Int Cl.[7]: **G09G 3/28**, G09G 3/20

(21) Application number: **00127839.9**

(22) Date of filing: **19.12.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **10.02.2000 JP 2000033496**

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(54) Method for driving display panel

(57) A method of driving a display panel that is capable of displaying pictures while suppressing the occurrence of pseudo contour without causing flicker even when the vertical synchronization frequency of the input video signal is low. When each of a plurality of light emitting elements that constitute a display screen of the display panel are caused to emit light only for a light emitting period corresponding to the luminance level of the input video signal within the unit display period, with the unit display period comprised of a first drive period of the first half and a second drive period of the second half, each of the light emitting elements is driven to emit light continuously for a first part of the light emitting period in the first drive period, and driven to emit light continuously for the remaining part of the light emitting period in the second drive period.

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a method for driving a display panel comprising light emitting elements, that have only two states, i.e. light emitting and non-light emitting states, being arranged therein.

2. Description of Related Art

[0002] Recently, as the increase in screen size of display apparatuses, demands for display devices of a smaller depth are growing. Plasma display panels of alternating current discharge type are regarded as a promising technology for thin display devices.

[0003] In such a plasma display panel, since each discharge cell that is an element of the display screen has only two states: the states of light emitting and non-light emitting, the sub-field method is employed for rendering intermediate tones of luminance that correspond to an input video signal.

[0004] The sub-field method divides the period of displaying one field into a plurality of sub-fields, and achieves a desired level of luminance by setting the discharge cells in each sub-field to light emitting state or an non-light emitting state. With the sub-field method, in the case where a light emitting state in successive sub-fields and a non light emitting state in successive sub-fields interchange with each other between light emission patterns of similar luminance levels, a so-called problem of pseudo contour occurs. Thus measures are taken to prevent the sustained light emitting state and the sustained non-light emitting state from interchanging with each other between light emission patterns of similar luminance levels.

[0005] However, in the case where the input video signal has a low vertical synchronization frequency as in the case of a PAL system television signal, for example, the frequency may happen to be identical with the frequency of switching between the sustained light emitting state and the sustained non-light emitting state. When such a television signal is supplied as the video signal, there has been a problem that flicker is generated.

OBJECTS AND SUMMARY OF THE INVENTION

[0006] The present invention has been made to solve such problems as described above, and an object of the invention is to provide a method of driving a display panel that is capable of displaying pictures while suppressing the occurrence of pseudo contours without causing flicker even when the vertical synchronization frequency of the input video signal is low.

[0007] According to the display panel driving method of the present invention, the display panel is driven to provide a toned display by causing each light emitting element to emit light only for a period corresponding to the luminance level of the input video signal, within the unit display period, in the display panel having a display screen constituted by a plurality of light emitting elements. The unit display period is made by a first drive period of a first half and a second drive period of a second half. In the first drive period, the light emitting element is driven to emit light continuously for the first part of the light emitting period and, in the second drive period, the light emitting element is driven to emit light continuously for the remaining part of the light emitting period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Fig. 1 is a diagram schematically showing the structure of a plasma display apparatus.

[0009] Fig. 2 shows an example of light emission drive format based on the sub-field method.

[0010] Fig. 3 shows an example of light emission drive pattern.

[0011] Fig. 4 shows the structure of a plasma display apparatus which drives a plasma display panel according to the driving method of the present invention.

[0012] Fig. 5 shows the inner structure of a data conversion circuit 30.

[0013] Fig. 6 shows the data conversion characteristic of a first data conversion circuit 32.

[0014] Fig. 7 shows an example of data conversion table based on the data conversion characteristic shown in Fig. 6.

[0015] Fig. 8 shows an example of data conversion table based on the data conversion characteristic shown in Fig. 6.

[0016] Fig. 9 shows the inner structure of a tone multiplication processing circuit 33.

[0017] Fig. 10 is a drawing for explaining the operation of an error diffusion processing circuit 330.

[0018] Fig. 11 shows the inner structure of a dither processing circuit 350.

[0019] Fig. 12 shows the operation of a dither processing circuit 350.

[0020] Fig. 13 shows a first data conversion table used in a second data conversion circuit 34 when the input video signal has a vertical synchronization frequency that is not lower than a predetermined frequency, and a light emission drive pattern thereof.

[0021] Fig. 14 shows a second data conversion table used in the second data conversion circuit 34 when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency, and a light emission drive pattern thereof.

[0022] Fig. 15 shows an example of light emission drive format (based on the selective erasure address method) employed when the input video signal has a vertical synchronization frequency that is not lower than the predetermined frequency.

[0023] Fig. 16 shows an example of light emission drive format (based on the selective erasure address method) employed when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency.

[0024] Fig. 17 shows the timing of applying various drive pulses to PDP 10.

[0025] Fig. 18 shows another example of second data conversion table used in the second data conversion circuit 34 when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency, and the light emission drive pattern thereof.

[0026] Fig. 19 shows another example of light emission drive format (based on the selective erasure address method) employed when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency.

[0027] Fig. 20 shows another example of second data conversion table used in the second data conversion circuit 34 when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency, and the light emission drive pattern thereof.

[0028] Fig. 21 shows an example of light emission drive format (based on the selective writing address method) employed when the input video signal has a vertical synchronization frequency that is not lower than the predetermined frequency.

[0029] Fig. 22 shows an example of light emission drive format (based on the selective writing address method) employed when the input video signal has a vertical synchronization frequency that is lower than the predetermined frequency.

[0030] Fig. 23 shows the first data conversion table used in the second data conversion circuit 34 when driving according to the light emission drive format shown in Fig. 21, and the light emission drive pattern thereof.

[0031] Fig. 24 shows the second data conversion table used in the second data conversion circuit 34 when driving according to the light emission drive format shown in Fig. 22, and the light emission drive pattern thereof.

[0032] Fig. 25 shows a variation of the light emission drive format shown in Fig. 16.

[0033] Fig. 26 shows the second data conversion table used in the second data conversion circuit 34 when driving according to the light emission drive format shown in Fig. 25, and the light emission drive pattern thereof.

[0034] Fig. 27 shows a variation of the light emission drive format shown in Fig. 22.

[0035] Fig. 28 shows the second data conversion table used in the second data conversion circuit 34 when driving according to the light emission drive format shown in Fig. 27, and the light emission drive pattern thereof.

[0036] Fig. 29 shows an example of light emission drive pattern employed when dividing one field into 13 sub-fields and driving a toned display based on the selective erasure address method.

[0037] Fig. 30 shows an example of light emission drive pattern employed when dividing one field into 13 sub-fields and driving a toned display based on the selective writing address technique.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] Prior to a description of a preferred embodiment of the present invention, a prior art method of driving a display panel will be described below with reference to the accompanying drawings.

[0039] Fig. 1 shows the schematic structure of a plasma display apparatus which displays pictures with such a plasma display panel.

[0040] In Fig. 1, PDP 10 which is the plasma display panel has m column electrodes D_1 through D_m that serve as data electrodes and n row electrodes X_1 through X_n and row electrodes Y_1 through Y_n that cross the column electrodes. A pair of X and Y electrodes constitute the row electrode corresponding to one line of the screen. The column electrode D and the row electrodes X, Y are formed on two glass substrates that are disposed to oppose each other interposing a discharge space which is filled with a discharge gas formed in between. Formed at the intersect of a row electrode and a column electrode is a discharge cell that serves as a display element for one pixel.

[0041] The discharge cell operates by making use of electric discharge, and therefore has only two states of light emitting and non-light emitting. That is, the discharge cell can provide luminance of only two tones, minimum luminance (non-light emitting) and maximum luminance (light emitting). Therefore a drive device 100 drives the PDP 10, comprising the discharge cells arranged in a matrix, by the sub-field method to drive toned display in order to render luminance of an intermediate tone that corresponds to input video signal.

[0042] The sub-field method divides the display period of one field into, for example, eight sub-fields SF1 through SF8 as shown in Fig. 2. The number of times light should be turned on in the sub-field is assigned to each of the sub-fields SF1 through SF8. As a consequence, light emission is carried out a number of times that corresponding to the luminance level of the input video signal in the display period of one field, by choosing a proper combination of sub-fields where light is to be emitted and sub-fields where light is not to be emitted according to the input video signal. This causes an intermediate level of luminance to be perceived according to the total number of times light is emitted in the display period of one field.

[0043] Fig. 3 shows an example of the combination of sub-fields where light is to be emitted and sub-fields where light is not to be emitted (hereinafter referred to

as a light emission drive pattern).

[0044] The drive device 100 selects one of nine different light emission drive patterns shown in Fig. 3, in accordance with the input video signal. Accordingly, various drive pulses are applied to the column electrodes D, and row electrodes X, Y of the PDP 10, to thereby emit light the number of times shown in Fig. 2 only in the sub-fields indicated by white circles in the light emission drive pattern that has been selected.

[0045] According to the nine light emission drive patterns shown in Fig. 3, pictures can be displayed with nine levels of intermediate luminance having the following proportions of luminance of light emitted.

{0, 1, 7, 23, 47, 82, 128, 185, 255}

[0046] At this time, in the light emission drive pattern shown in Fig. 3, once a discharge cell is turned to an non-light emitting state in one sub-field during the period of one field, subsequent sub-fields are controlled so that light is not emitted. That is, such a light emission drive pattern is rejected in which the state of sub-fields in which light is emitted occur successively (hereinafter referred to as the sustained light emitting state) as indicated by the white circles and the state of sub-fields in which light is not emitted occur successively (hereinafter referred to as the sustained non-light emitting state) interchange with each other between light emission patterns of similar luminance levels in the period of one field. This scheme suppresses the occurrence of pseudo contour that would take place in the boundary of two picture regions where the sustained light emitting state and the sustained non-light emitting state interchange with each other.

[0047] In the light emission drive pattern as shown in Fig. 3, the frequency of switching between the sustained light emitting state and the sustained non-light emitting state becomes equal to the vertical synchronization frequency that determines the period of displaying one field. As a result, there is a possibility of flicker occurring when the PAL system television signal wherein the vertical synchronization frequency is limited to 50Hz is supplied as the input video signal, as described previously.

[0048] Now a preferred embodiment of the present invention will be described below with reference to the accompanying drawings.

[0049] Fig. 4 schematically shows the structure of a plasma display apparatus which drives a plasma display panel according to the driving method of the present invention.

[0050] In Fig. 4, when the vertical synchronization frequency is detected from the input video signal, a sync detection circuit 1 generates and supplies a vertical synchronization detection signal V to a drive control circuit 2 and a vertical synchronization frequency detection circuit 3. When the horizontal synchronization signal is detected from the input video signal, the sync detection circuit 1 generates and supplies a horizontal synchronization detection signal H to the drive control circuit 2. The vertical synchronization frequency detection circuit 3 determines the vertical synchronization frequency of the input video signal by measuring the frequency of the vertical synchronization detection signal V, and supplies a vertical synchronization frequency signal VF that represents the frequency to the drive control circuit 2 and a data conversion circuit 30. An A/D converter 4 samples the input video signal thereby converting it into, for example, 8-bit pixel data D for each pixel in accordance with a clock signal supplied from the drive control circuit 2, and supplies the pixel data to the data conversion circuit 30.

[0051] Fig. 5 shows the inner structure of a data conversion circuit 30.

[0052] In Fig. 5, a first data conversion circuit 32 supplies a tone multiplication processing circuit 33 with converted pixel data D_{11} that is generated by multiplying the pixel data D by $(14 \times 16)/255$ according to the conversion characteristic shown in Fig. 6. In other words, the first data conversion circuit 32 converts the pixel data D that is capable of representing the levels of luminance for 256 tones, from 0 to 255, with eight bits, into the converted pixel data D_H that is capable of representing the levels of luminance for 255 tones, from 0 to 224, with eight bits. Specifically, the first data conversion circuit 32 converts the pixel data D into the converted pixel data D_H according to the conversion table shown in Fig. 7 and Fig. 8 based on the conversion characteristic shown in Fig. 6. The conversion characteristic is determined in accordance with the number of bits of the pixel data, the number of bits compressed in a tone multiplication process to be described later, and the number of displayed tones.

[0053] Thus the data are converted in the first data conversion circuit 32 in consideration of the number of displayed tones and the number of bits compressed in the tone multiplication, before carrying out the tone multiplication process that will be described later. With this data conversion, the input pixel data D is divided into a group of most significant bits (corresponding to multitoned pixel data) and a group of least significant bits (data to be discarded: error data), and the tone multiplication process is carried out according to this signal. This makes it possible to prevent saturation of luminance from occurring due to the tone multiplication process and flattening of the display characteristic (that is, distortion of tone) that occurs when the display tone is not on the bit boundary.

[0054] Fig. 9 shows the inner structure of the tone multiplication processing circuit 33 that carries out the tone multiplication process.

[0055] As shown in Fig. 9, the tone multiplication processing circuit 33 is composed of an error diffusion processing circuit 330 and a dither processing circuit 350.

[0056] A data separation circuit 331 of the error diffusion processing circuit 330 separates the 8-bit converted pixel data D_H supplied from the first data conversion circuit 32 into error data consisting of the least signifi-

cant two bits and display data consisting of the most significant six bits. An adder 332 adds the error data, delayed output of a delay circuit 334 and multiplied output of a coefficient multiplier 335, and supplies the sum to a delay circuit 336. The delay circuit 336 sends the sum supplied from the adder 332, with a delay time corresponding to the period of one clock cycle of the pixel data (hereinafter called the delay time D) being applied thereto, as delayed addition signal AD_1 to the coefficient multiplier 335 and the delay circuit 337. The coefficient multiplier 335 multiplies the delayed addition signal AD_1 by a predetermined coefficient K_1 (7/16, for example) and sends the product to the adder 332. The delay circuit 337 sends the delayed addition signal AD_1, with an additional delay time of (one horizontal scan period - delay time D $\times$ 4) applied thereto, as delayed addition signal AD_2 to a delay circuit 338. The delay circuit 338 sends the delayed addition signal AD_2, with further additional delay time of the delay time D applied thereto, as delayed addition signal AD_3 to a coefficient multiplier 339. The delay circuit 338 also sends the delayed addition signal AD_2, with a delay time of the delay time D $\times$ 2 applied thereto, as delayed addition signal AD_4 to a coefficient multiplier 340. The delay circuit 338 further sends the delayed addition signal AD_2, with a delay time equal to the delay time D $\times$ 3 applied thereto, as a delayed addition signal AD_5 to a coefficient multiplier 341. The coefficient multiplier 339 multiplies the delayed addition signal AD_3 by a predetermined coefficient K_2 (3/16, for example) and sends the product to the adder 342. The coefficient multiplier 340 multiplies the delayed addition signal AD_4 by a predetermined coefficient K_3 (5/16, for example) and sends the product to the adder 342. The coefficient multiplier 341 multiplies the delayed addition signal AD_5 by a predetermined coefficient K_4 (1/16, for example) and sends the product to the adder 342. The adder 342 adds up the products supplied from the coefficient multipliers 339, 340 and 341 and sends the sum to the delay circuit 334. The delay circuit 334 outputs the addition signal, with the delay time D applied thereto, to the adder 332. The adder 332 adds the error data, the delayed output from the delay circuit 334 and the multiplication output from the coefficient multiplier 335, and sends it to an adder 333 a carry-out signal C_o having a logical value of 0 when there is no carry over in the addition, or a logical value of 1 when there is carry over in the addition. The adder 333 adds the carry-out signal C_o to the display data comprising the most significant six bits of the converted pixel data D_H and outputs the sum as the 6-bit error diffusion processed pixel data ED.

[0057] Operation of the error diffusion processing circuit 330 having such a structure as described above will now be described below.

[0058] To determine the error diffusion processed pixel data ED for a pixel G(j, k) of the PDP 10 as shown in Fig. 10, for example, error data for each of a pixel G(j, k-1) located at the left of the pixel G(j, k), a pixel G(j-1, k-1) located at the upper left of the pixel G(j, k), a pixel G(j-1, k) located above the pixel G(j, k) and a pixel G(j-1, k+1) located at the upper right of the pixel G(j, k), are weighted by predetermined weighting factors K_1 through K_4 as follows.

Error data for the pixel G(j, k-1): Delayed addition signal AD_1
Error data for the pixel G(j-1, k+1): Delayed addition signal AD_3
Error data for the pixel G(j-1, k): Delayed addition signal AD_4
Error data for the pixel G(j-1, k-1): Delayed addition signal AD_5

[0059] Then the least significant two bits of the converted pixel data HD_P, namely the error data of the pixel G(j, k), is added to the sum obtained as described above. The carry-out signal C_o consisting of one bit thus obtained is added to the most significant six bits of the converted pixel data D_H, namely the display data of the pixel G(j, k), with the result of addition being taken as the error diffusion processed pixel data ED.

[0060] In the error diffusion processing circuit 330 having such a structure as described above, the most significant six bits and the least significant two bits of the converted pixel data D_H are used as the display data and the error data, respectively, and the error data weighted by the corresponding weighting factors for the peripheral pixels [G(j, k-1), G(j-1, k+1), G(j-1, k), G(j-1, k-1)] are added, with the result being reflected on the display data. This operation causes the luminance corresponding to the least significant two bits at the pixel G(j, k) to be represented alternatively by the peripheral pixels, thereby making it possible to provide a toned representation of luminance equivalent to 8-bit pixel data, by using 6-bit display data which is lower than 8-bit display data.

[0061] Simply adding the coefficient of error diffusion for each pixel may cause visual perception of noise caused by the error diffusion pattern, resulting in deteriorated picture quality. To counter this problem, the error diffusion coefficients K_1 through K_4 to be assigned to the four surrounding pixels may be changed from field to field.

[0062] The dither processing circuit 350 applies dither process to the error diffusion processed pixel data ED supplied from the error diffusion processing circuit 330. In the dither process, one intermediate display level is represented by a plurality of adjacent pixels. For example, to provide a toned display equivalent to that of eight bits by using the pixel data of the most significant six bits among the 8-bit pixel data, four vertically and horizontally adjacent pixels are grouped as a set, and four dither coefficients a through d of different values are added to the pixel data of corresponding pixels of the set. The dither process produces four different combinations of intermediate display levels from the four pix-

els. As a result, even when the pixel data comprises six bits, a number of tone levels four times larger, namely intermediate tones equivalent to those of eight bits, can be represented.

[0063] However, when the dither coefficients a through d of constant values are added to each pixel, visual perception of noise caused by the dither pattern may occur, resulting in deteriorated picture quality.

[0064] To counter this problem, in the dither processing circuit 350, the dither coefficients a though d to be assigned to the four pixels are changed from field to field.

[0065] Fig. 11 shows the inner structure of the dither processing circuit 350.

[0066] In Fig. 11, a dither coefficient generation circuit 352 generates four dither coefficients a, b, c and d for the four adjacent pixels [G(j, k), G(j, k+1), G(j+1, k), G (j+1, k+1)] as shown in Fig. 12 and sends the coefficients successively to the adder 351. The dither coefficient generation circuit 352 also changes the assignment of the dither coefficients a through d, that are generated in correspondence to the four pixels, from field to field as shown in Fig. 12.

[0067] Specifically, the dither coefficients a through d are generated cyclically and repetitively for the following assignments and are supplied to the adder 351.

In the first field:

Pixel G(j, k): Dither coefficient a
Pixel G(j, k+1): Dither coefficient b
Pixel G(j+1, k): Dither coefficient c
Pixel G(j+1, k+1): Dither coefficient d

In the second field:

Pixel G(j, k): Dither coefficient b
Pixel G(j, k+1): Dither coefficient a
Pixel G(j+1, k): Dither coefficient d
Pixel G(j+1, k+1): Dither coefficient c

In the third field:

Pixel G(j, k): Dither coefficient d
Pixel G(j, k+1): Dither coefficient c
Pixel G(j+1, k): Dither coefficient b
Pixel G(j+1, k+1): Dither coefficient a

In the fourth field:

Pixel G(j, k): Dither coefficient c
Pixel G(j, k+1): Dither coefficient d
Pixel G(j+1, k): Dither coefficient a
Pixel G(j+1, k+1): Dither coefficient b

[0068] The dither coefficient generation circuit 352 repetitively carries out the above operation for the first field through the fourth field. That is, when the operation of generating the dither coefficients for the fourth field is completed, the operation is repeated from the first field.

[0069] The adder 351 adds the dither coefficients a through d, that are assigned for each field as described above, to the error diffusion processed pixel data ED of the pixel G(j, k), pixel G(j, k+1), pixel G(j+1, k) and pixel G(j+1, k+1), respectively, that are supplied from the error diffusion processing circuit 330, and supplies the dither-added pixel data thus obtained to an upper bit extraction circuit 353.

[0070] In the first field shown in Fig. 12, for example, the following values are supplied successively to the upper bit extraction circuit 353 as the dither-added pixel data.

Error diffusion processed pixel data ED corresponding to pixel G(j, k) + dither coefficient a,
Error diffusion processed pixel data ED corresponding to pixel G(j, k+1) + dither coefficient b,
Error diffusion processed pixel data ED corresponding to pixel G(j+1, k) + dither coefficient c, and
Error diffusion processed pixel data ED corresponding to pixel G(j+1, k+1) + dither coefficient d.

[0071] The upper bit extraction circuit 353 extracts the four most significant bits of the dither-added pixel data, and supplies the extracted data as the multi-toned pixel data D_s to the second data conversion circuit 34 shown in Fig. 5.

[0072] The second data conversion circuit 34 converts the multi-toned pixel data D_s into 14-bit pixel drive data GD in accordance with a conversion table that corresponds to the vertical synchronization frequency of the input video signal indicated by the vertical synchronization frequency signal VF. For example, when NTSC system television signal having a vertical synchronization frequency of 60Hz or higher is supplied as the input video signal, the second data conversion circuit 34 converts the multi-toned pixel data D_s into pixel drive data GD in accordance with the first conversion table shown in Fig. 13. When PAL system television signal having vertical synchronization frequency lower than 60Hz is supplied as the input video signal, on the other hand, the multi-toned pixel data Ds is converted into pixel drive data GD in accordance with the second conversion table shown in Fig. 14.

[0073] A memory 5 shown in Fig. 4 stores the pixel drive data GD successively written therein according to the writing signal supplied from the drive control circuit 2. When the writing operation for the data of one picture frame (n rows, m columns) has been completed, the pixel drive data $GD_{11\text{-}nm}$ of one screen frame are read successively from the memory 5 at the same bit digit for one line, and are sent to an address driver 6. In other words, the pixel drive data bits $GD1_{11\text{-}nm}$ through $GD14_{11\text{-}nm}$ in the memory 5 are determined for each bit digit of the pixel drive data $GD_{11\text{-}nm}$ of one screen frame as follows.

$DB1_{11\text{-}nm}$: First bit of the pixel drive data $GD_{11\text{-}nm}$
$DB2_{11\text{-}nm}$: Second bit of the pixel drive data $GD_{11\text{-}nm}$
$DB3_{11\text{-}nm}$: Third bit of the pixel drive data $GD_{11\text{-}nm}$
$DB4_{11\text{-}nm}$: Fourth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB5_{11\text{-}nm}$: Fifth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB6_{11\text{-}nm}$: Sixth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB7_{11\text{-}nm}$: Seventh bit of the pixel drive data $GD_{11\text{-}nm}$
$DB8_{11\text{-}nm}$: Eighth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB9_{11\text{-}nm}$: Ninth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB10_{11\text{-}nm}$: Tenth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB11_{11\text{-}nm}$: Eleventh bit of the pixel drive data $GD_{11\text{-}nm}$
$DB12_{11\text{-}nm}$: Twelfth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB13_{11\text{-}nm}$: Thirteenth bit of the pixel drive data $GD_{11\text{-}nm}$
$DB14_{11\text{-}nm}$: Fourteenth bit of the pixel drive data $GD_{11\text{-}nm}$

[0074] Then $DB1_{11\text{-}nm}$ through $DB14_{11\text{-}nm}$ are read off successively line by line according to a read signal supplied from the drive control circuit 2 and supplied to the address driver 6.

[0075] The drive control circuit 2 employs a light emission drive format that corresponds to the vertical synchronization frequency of the input video signal indicated by the vertical synchronization frequency signal VF. According to the light emission drive format that is employed, the drive control circuit 2 generates various timing signals for the control of the address driver 6, a first sustain driver 7 and a second sustain driver 8.

[0076] For example, when NTSC system television signal having a vertical synchronization frequency of 60Hz or higher is supplied as the input video signal, the drive control circuit 2 employs the light emission drive format shown in Fig. 15. When a signal having vertical synchronization frequency lower than 60Hz, such as a PAL system television signal, is supplied as the input video signal, on the other hand, the drive control circuit 2 employs the light emission drive format shown in Fig. 16.

[0077] In the light emission drive format shown in Fig. 15 and Fig. 16, the display period for one field (this includes also one frame hereinafter) is divided into 14 sub-fields SF1 through SF 14. And in each sub-field, pixel data writing process Wc where the pixel data is written for each discharge cell of the PDP 10 thereby to set the light emitting cells and non-light emitting cells, and light emission sustaining process Ic where only the cells to be light emitting are turned on to emit light repetitively for the period shown in the drawing, are carried out.- Also a total reset process Rc, where the amounts of charges on the walls of all discharge cells of the PDP 10 are initialized, is carried out in the first sub-field SF1, and erasure process E where charges on the walls of all discharge cells are eliminated is carried out in the last sub-field SF14.

[0078] In the light emission drive format shown in Fig. 16, the sub-fields SF1, SF3, SF5, SF7, SF9, SF11 and SF13 in the light emission drive format of Fig. 15 are executed in the first half of one field, while SF2, SF4, SF6, SF8, SF10, SF12 and SF14 are executed in the second half of the field. At this time, the erasure process E is carried out in the last sub-field SF13 of the first half, and the total reset process Rc is carried out in the first sub-field SF2 of the second half.

[0079] The address driver 6, the first sustain driver 7 and the second sustain driver 8 apply various drive pulses for achieving the processes described above to the electrodes of the PDP 10 at the timing determined by a timing signal supplied from the drive control circuit 2.

[0080] Fig. 17 shows the timing of various drive pulses applied by the drivers to the column electrodes D and the row electrodes X, Y in the total reset process Rc, the pixel data writing process Wc, the light emission sustaining process Ic and the erasure process E.

[0081] First, in the total reset process Rc, the first sustain driver 7 and the second sustain driver 8 apply such reset pulses RP_X and RP_Y as shown in Fig. 17 to the row electrodes X_1 through X_n and Y_1 through Y_n. As the reset pulses RP_X and RP_Y are applied, all discharge cells of the PDP 10 discharge to be reset, so that a predetermined amount of charges deposit uniformly on the wall of every discharge cell. Thus all the discharge cells are reset to the light emitting cells.

[0082] In the pixel data writing process Wc, the address driver 6 generates pixel data pulse group DP (for one line), that has a voltage corresponding to the logical value of the pixel drive data bit DB which has been supplied from the memory 5, and applies the pulses to the column electrode $D_{1\text{-}m}$. In the pixel data writing process Wc of the sub-field SF1, for example, the pixel drive data bit $DB1_{11\text{-}1m}$ that corresponds to the first row is read from the memory 5. Accordingly the address driver 6 generates the pixel data pulse group DP consisting of the pixel data pulses of m pieces corresponding to the logical values of the $DB1_{11\text{-}1m}$ and applies the pixel data pulse group DP to the column electrodes $D_{1\text{-}m}$. Then as the pixel drive data bit $DB1_{21\text{-}2m}$ that corresponds to the second line is read from the memory 5, the address driver 6 generates the pixel data pulse group DP of m pieces corresponding to the logical values of the $DB1_{21\text{-}2m}$ and applies the pixel data pulse group DP to the column electrodes $D_{1\text{-}m}$. Similarly in the pixel data writing process Wc for the sub-field SF1, pixel data pulse group DP corresponding to the first through nth lines are applied successively to the column electrodes $D_{1\text{-}m}$ thereafter. The address driver 6 generates high voltage pixel data pulses when the logical value of the pixel drive data bit DB is "1", and generates low voltage pixel data pulses (0 volts) when the logical value is "0".

[0083] Also in the pixel data writing process Wc, the second sustaining driver 8 generates negative polarity scan pulse SP as shown in Fig. 17 at the same timing as the timing of applying the pixel data pulse group DP

described above. The scan pulses are applied to the row electrodes Y_1 through Y_n successively. At this time, electrical discharge (selective erasure discharge) occurs only in the discharge cell located at the intersection of the row to which the scan pulse SP is applied and the column to which the pixel data pulse of high voltage is applied, thereby selectively eliminating the charge remaining on the wall of the discharge cell. The discharge cell that was initialized to the state of an light emitting cell in the total reset process Rc is changed to the state of an non-light emitting cell by this selective erasure discharge. On the other hand, electrical discharge does not occur in the discharge cells located on the column to which the pixel data pulse of low voltage is applied, and the discharge cell remains in the present state. Thus the non-light emitting cells remain in the state of non-light emitting cell, and the light emitting cells remain in the state of light emitting cell.

[0084] In the light emission sustaining process Ic of each sub-field, the first sustain driver 7 and the second sustain driver 8 repetitively apply sustaining pulses IP_X and IP_Y of positive polarity to the row electrodes X_1 through X_n and Y_1 through Y_n alternately, as shown in Fig. 17. Proportions of the length of periods during which the sustaining pulse IP is kept being applied in the light emission sustaining process Ic for the sub-fields SF1 through SF14 are set as follows.

SF1: 1
SF2: 3
SF3: 5
SF4: 8
SF5: 10
SF6: 13
SF7: 16
SF8: 19
SF9: 22
SF10: 25
SF11: 28
SF12: 32
SF13: 35
SF14: 39

[0085] Sustained discharge is carried out in the discharge cell where charges are formed on the wall thereof, namely the light emitting cells, every time the sustaining pulses IP_X and IP_Y are applied only. That is, only the discharge cells that were set as light emitting cells in the pixel data writing process Wc repeat to emit light through the sustained discharge during the period determined by the weighting factor of the sub-field described above, thus sustaining the light emitting state. The longer the time in which the light emitting state is sustained, the brighter the display is perceived by the human eyes.

[0086] In the erasure process E, the second sustain driver 8 generates such an erasure pulse EP of negative polarity as shown in Fig. 17 and applies the pulse to the row electrodes Y_1 through Y_n. Application of the erasure pulse EP causes erasure discharge to occur in all discharge cells of the PDP 10, so that the charges remaining on the walls of all discharge cells disappear. That is, the erasure discharge forces all the discharge cells of the PDP 10 to turn into non-light emitting cells.

[0087] With the driving operation described above, only the discharge cells that were set as light emitting cells by the pixel data writing process Wc in each sub-field repeat to emit light in the light emission sustaining process Ic immediately after the process Wc during the period determined by the weighting factor of the sub-field as described above. Whether a discharge cell is set as an light emitting cell or non-light emitting cell is determined by the pixel drive data GD shown in Fig. 13 or Fig. 14.

[0088] The foregoing description can be summed as follows. When a bit of the pixel drive data GD consisting of first through fourteenth bits has logical value "1", selective erasure discharge occurs in the pixel data writing process Wc of the sub-field corresponding to the bit digit. This selective erasure discharge sets the discharge cell to the non-light emitting cell state. When a bit of the pixel drive data GD has logical value "0", on the other hand, selective erasure discharge does not occur in the pixel data writing process Wc of the sub-field corresponding to the bit digit. Thus discharge cells in the non-light emitting cell state remain in the non-light emitting cell state, and the discharge cells in the light emitting cells state remain in the light emitting cell state. A discharge cell can be changed from the non-light emitting cell state to the light emitting cell state only by the total reset process Rc.

[0089] The first through fourteenth bits of the pixel drive data GD shown in Fig. 13 correspond to the sub-fields SF1 through SF14 shown in Fig. 15, respectively.

[0090] Consequently, when driving according to the light emission drive format shown in Fig. 15 by using the pixel drive data GD shown in Fig. 13, all discharge cells are first initialized as the light emitting cells in the sub-field SF1. The light emitting cell state is maintained until the selective erasure discharge occurs in the sub-fields indicated by black circles in Fig. 13. In the light emission sustaining process Ic for each of the sub-fields (indicated by white circles) that are present while the light emitting cell state is maintained, light is emitted for a period determined by the weighting factor of the sub-field. In this driving operation, the number of times the state is switched from the sustained light emitting state where light is emitted in consecutive sub-fields to the sustained non-light emitting state where light is not emitted in consecutive sub-fields is one in the display period of one field. Here, sum of the periods of time during which light was emitted in the light emission sustaining process Ic of the sub-fields SF1 through SF14 relates to the luminance.

[0091] The first through fourteenth bits of the pixel drive data GD shown in Fig. 14 correspond to the sub-

fields SF1 through SF14 shown in Fig. 16 as follows, respectively.

1st bit of GD: SF1
2nd bit of GD: SF3
3rd bit of GD: SF5
4th bit of GD: SF7
5th bit of GD: SF9
6th bit of GD: SF11
7th bit of GD: SF13
8th bit of GD: SF2
9th bit of GD: SF4
10th bit of GD: SF6
11th bit of GD: SF8
12th bit of GD: SF10
13th bit of GD: SF12
14th bit of GD: SF14

[0092] In the light emission drive format shown in Fig. 16, total reset process Rc is executed not only,in the sub-field SF1 but also in the sub-field SF2.

[0093] Consequently, when driving according to the light emission drive format shown in Fig. 16 by using the pixel drive data GD shown in Fig. 14, the discharge cells are first initialized as the light emitting cells in the sub-field SF1. The light emitting cell state is maintained until the selective erasure discharge occurs in the sub-fields indicated by the black circles in Fig. 14. Then in the light emission sustaining process Ic of each of the sub-fields (indicated by white circles) that are present while the light emitting cell state is maintained, light is emitted for a period determined by the weighting factor of the sub-field. After the selective erasure discharge has occurred, the discharge cells turn to non-light emitting cells. Then the discharge cells are initialized to light emitting cells again in the sub-field SF2, and maintain the light emitting cell state until the selective erasure discharge occurs in the sub-fields indicated by the black circles. Then in the light emission sustaining process Ic for the sub-fields (indicated by the white circles) subsequent to the sub-field SF2 that are present while the light emitting cell state is maintained, light is emitted for a period determined by the weighting factor of the sub-field. In this driving operation, the number of times the state is switched, from the sustained light emitting state where light is emitted in consecutive sub-fields to the sustained non-light emitting state where light is not emitted in consecutive sub-fields, is two at maximum in the display period of one field. Here, sum of the periods of time during which light was emitted in the light emission sustaining process Ic of the sub-fields SF1 through SF14 relates to the luminance of light emission in one field.

[0094] As a result, when driving the toned display according to the light emission drive format shown in Fig. 15 or Fig. 16 by using the pixel drive data GD shown in Fig. 13 or Fig. 14 as described above, pictures can be displayed with intermediate tones of luminance of 15 levels as follows.

{0: 1: 4: 9: 17: 27: 40: 56: 75: 97: 122: 150: 182: 217: 256}

[0095] Combination of such a driving operation with 15 tone levels and the multi-tone processing in the tone multiplication processing circuit 33 described previously makes it possible to achieve a visual effect equivalent to 256 tone levels of luminance.

[0096] In the operation of toned display described above, the selective erasure discharge to change the state of the discharge cells is carried out only once in the period from the time of executing the total reset process Rc to the execution of the next total reset process Rc as indicated by the black circles in Fig. 13 and Fig. 14. With this operation, the sub-fields in which light is emitted continue (sustained light emitting state), while sub-fields in which light is not emitted continue (sustained non-light emitting state). There is no light emission drive pattern in which the sustained light emitting state and the sustained non-light emitting state are switched alternately. As a result, since no case occurs where two picture regions wherein the sustained light emitting state and the sustained non-light emitting state are switched alternately in the period of one field appear in one picture frame, occurrence of the pseudo contour that would take place in the boundary of two picture regions can be suppressed.

[0097] Also the present invention employs a toned display operation as the display period of one field is divided into the first drive period (SF1, SF3, SF5, SF7, SF9, SF11, SF13) of the first half and the second drive period (SF2, SF4, SF6, SF8, SF10, SF12, SF14) of the second half as shown in Fig. 14 and Fig. 16. Meanwhile, in the first drive period, light is emitted continuously for a period of time corresponding to the luminance level (first tone to fifteenth tone) of the input video signal, beginning at the start of the first drive period. In the second drive period, on the other hand, light is emitted continuously for a period of time corresponding to the luminance level (first tone to fifteenth tone) of the input video signal, beginning at the start of the second drive period. With this driving operation, therefore, the number of times the state is switched from the sustained light emitting state where light is emitted in consecutive sub-fields to the sustained non-light emitting state where light is not emitted in consecutive sub-fields is two at maximum in the display period of one field. Also the time interval between the start of light emission in the first drive period to the start of light emission in the second drive period is about one half the display period of one field. Therefore, since the frequency of switching between the sustained light emitting state and the sustained non-light emitting state is about twice the vertical synchronization frequency that determines the display period of one field, flicker does not occur even when the PAL system television signal of which vertical synchronization frequency is limited to 50Hz is supplied as the input video signal.

[0098] In the light emission drive pattern shown in Fig. 14, the selective erasure discharge is carried out only once in the period from the execution of the total reset process Rc to the next execution of the total reset process Rc. However, when the amount of charges remaining in the discharge cells is small, the selective erasure discharge may not occur normally even when the scan pulse SP and the high-voltage pixel data pulse are, for example, applied simultaneously.

[0099] For this reason, the second conversion table shown in Fig. 18 may be employed instead of that shown in Fig. 14 for use in the second data conversion table 34, to thereby reliably cause the selective erasure discharge. When the pixel drive data GD that are converted in accordance with the second conversion table are used, the selective erasure discharge occurs in two consecutive sub-fields as indicated by the black circles in Fig. 18. With this operation, even when the charges on the walls in the discharge cells cannot be eliminated normally by the first selective erasure discharge, the charges on the walls can be eliminated normally by the second selective erasure discharge.

[0100] In the light emission drive format shown in Fig. 16, the sub-fields SF1, SF3, SF5, SF7, SF9, SF11 and SF13 are executed in the first half of one field while SF2, SF4, SF6, SF8, SF10, SF12 and SF14 are executed in the second half thereof, although the present invention is not limited to this scheme.

[0101] Fig. 19 shows a variation of the light emission drive format shown in Fig. 16 devised in consideration of the facts described above.

[0102] In the light emission drive format shown in Fig. 19, sub-fields SF1, SF4, SF5, SF8, SF9, SF12 and SF13 are executed successively in the first half of one field while SF2, SF3, SF6, SF7, SF10, SF11 and SF14 are executed successively in the second half thereof.

[0103] Fig. 20 shows the second data conversion table used in the second data conversion circuit 34 when the light emission drive format shown in Fig. 19 is employed, and the light emission drive pattern thereof.

[0104] The embodiment described above is a case of employing the so-called selective erasure address method wherein all discharge cells are set to the light emitting cell state by forming charges on the walls of all discharge cells, and then the charges are eliminated selectively according to the pixel data for the purpose of writing the pixel data.

[0105] However, the present invention may also be applied to a case of employing the so-called selective writing address method wherein the charges are formed on the wall selectively according to the pixel data for the purpose of writing the pixel data.

[0106] Fig. 21 and Fig. 22 show the light emission drive format used when employing the selective writing address method. Fig. 23 shows the first data conversion table used in the second data conversion circuit 34 when the light emission drive format shown in Fig. 21 is employed, and the light emission drive pattern thereof. Fig. 24 shows the second data conversion table used in the second data conversion circuit 34 when the light emission drive format shown in Fig. 22 is employed, and the light emission drive pattern thereof.

[0107] According to the light emission drive format shown in Fig. 21, toned display is driven in the order of sub-fields from SF14 to SF1, contrary to the case of the light emission drive format shown in Fig. 15. In this case, the total reset process Rc', where charges remaining on walls of all the discharge cells are eliminated at the same time thereby initializing all discharge cells to the non-light emitting cell state, is carried out only in the first sub-field SF14. Then the pixel data writing process Wc and the light emission sustaining process Ic are carried out in each sub-field. At this time, selective writing discharge for forming charges on the wall occurs only in the pixel data writing process Wc' of the sub-fields (indicated by black circles) that correspond to digits having logical value of "1" in the pixel drive data GD shown in Fig. 23. The discharge cells where the selective writing discharge has occurred are set to light emitting cells. As a consequence, in the light emission sustaining process Ic of the sub-fields indicated by the black circles or white circles in Fig. 23, light is emitted for a period of time corresponding to the weighting factor of the sub-field.

[0108] In the light emission drive format shown in Fig. 22, sub-fields SF13, SF11, SF9, SF7, SF5, SF3 and SF1 are executed successively in the first half of one field while SF14, SF12, SF10, SF8, SF6, SF4 and SF2 are executed successively in the second half thereof. In this case, the total reset process Rc' described above is carried out similarly in the first sub-field SF13 of the first half and in the first sub-field SF14 of the second half. Then the pixel data writing process Wc' described above and the light emission sustaining process Ic are carried out in each sub-field. That is, only in the light emission sustaining process Ic of the sub-fields marked with the black circle and the white circle in Fig. 24, light is emitted for a period of time corresponding to the weighting factor of the sub-field. In this driving operation, switching from the sustained non-light emitting state to the sustained light emitting state is carried out twice in the display period of one field, similarly to the light emission drive pattern shown in Fig. 14.

[0109] In the case where there is no possibility of flicker occurring because of the vertical synchronization frequency of the input video signal being equal to or higher than the predetermined frequency (60Hz), the drive control circuit 2 controls the operation according to the light emission drive format shown in Fig. 21 by using the pixel drive data GD shown in Fig. 23. When there is a possibility of flicker occurring because of the vertical synchronization frequency of the input video signal being lower than the predetermined frequency (60Hz), the drive control circuit 2 controls the operation according to the light emission drive format shown in Fig. 22 by using the pixel drive data GD shown in Fig. 24. That is, when the vertical synchronization frequency of the input video signal is

lower than the predetermined frequency (60Hz), switching from the sustained non-light emitting state to the sustained light emitting state is carried out up to twice in the display period of one field as shown in Fig. 24.

[0110] In the light emission drive format shown in Fig. 16, the sub-fields having odd numbers are executed in the first half of one field and the sub-fields having even numbers are executed in the second half, although this order may be reverted.

[0111] Fig. 25 shows a variation of the light emission drive format (selective erasure address) shown in Fig. 16 devised in consideration of the facts described above.

[0112] In the light emission drive format shown in Fig. 25, the sub-fields SF2, SF4, SF6, SF8, SF10, SF12 and SF14 wherein light is to be emitted a number of times in proportions of [3: 8: 13: 19: 25: 32: 39] in the respective light emission sustaining process Ic are executed successively in the first half of one field. In the second half of the one field, the sub-fields SF1, SF3, SF5, SF7, SF9, SF11 and SF13 wherein light is to be emitted a number of times in proportions of [1: 5: 10: 16: 22: 28: 35] in the respective light emission sustaining process Ic are executed successively.

[0113] Fig. 26 shows the second data conversion table used in the second data conversion circuit 34 when the light emission drive format shown in Fig. 25 is employed, and the light emission drive pattern thereof.

[0114] Fig. 27 shows a variation of the light emission drive format (selective writing address) shown in Fig. 22.

[0115] In the light emission drive format shown in Fig. 27, the sub-fields SF14, SF12, SF10, SF8, SF6, SF4 and SF2 wherein light is to be emitted a number of times in proportions of [39: 32: 25: 16: 13: 5: 3] in the respective light emission sustaining process Ic are executed successively in the first half of one field. In the second half of the one field, the sub-fields SF13, SF11, SF9, SF7, SF5, SF3 and SF1 wherein light is to be emitted a number of times in proportions of [35: 28: 22: 19: 10: 8: 1] in the respective light emission sustaining process Ic are executed successively.

[0116] Fig. 28 shows the second data conversion table used in the second data conversion circuit 34 when the light emission drive format shown in Fig. 25 is employed, and the light emission drive pattern thereof.

[0117] While one field is divided into 14 sub-fields and the PDP 10 is driven to provide a toned display in the embodiment described above, the number of sub-fields is not limited to 14.

[0118] Fig. 29 and Fig. 30 show examples of light emission drive pattern employed in case one field is divided into 13 sub-fields and the PDP 10 is driven to provide toned display.

[0119] Fig. 29 shows the light emission drive pattern when the selective erasure address method is employed for writing the pixel data. In the light emission drive pattern shown in Fig. 29, the sub-fields SF1, SF3, SF5, SF7, SF9, SF11 and SF13 wherein light is to be emitted a number of times in proportions of [1: 5: 10: 16: 22: 28: 35] in the respective light emission sustaining process Ic are executed successively in the first half of one field. In the second half of the one field, the sub-fields SF2, SF4, SF6, SF8, SF10 and SF12 wherein light is to be emitted a number of times in proportions of [3: 8: 13: 19: 25: 32] in the respective light emission sustaining process Ic are executed successively.

[0120] Fig. 30 shows the light emission drive pattern when the selective writing address method is employed for writing the pixel data. In the light emission drive pattern shown in Fig. 30, the sub-fields SF13, SF11, SF9, SF7, SF5, SF3 and SF1 wherein light is to be emitted a number of times in proportions of [35: 28: 22: 16: 10: 5: 1] in the respective light emission sustaining process Ic are executed successively in the first half of one field. In the second half of the one field, the sub-fields SF12, SF10, SF8, SF6, SF4 and SF2 wherein light is to be emitted a number of times in proportions of [32: 25: 19: 13: 8: 3] in the respective light emission sustaining process Ic are executed successively.

[0121] According to the present invention, as described in detail above, the frequency of switching from the sustained non-light emitting state to the sustained light emitting state (or from the sustained light emitting state to the sustained non-light emitting state) in the display period of one field can be set higher than the vertical synchronization frequency. As a consequence, pictures in which pseudo contour is suppressed can be displayed without causing flicker even when the PAL system television signal wherein the vertical synchronization frequency is limited to 50Hz is supplied.

Claims

1. A display panel drive method for driving toned display of a display panel having a display screen formed from a plurality of light emitting elements by causing each of said light emitting elements to emit light for a light emission period that corresponds to the luminance level of the input video signal in the unit display period;

   wherein said unit display period comprises a first drive period of a first half and a second drive period of a second half, and wherein each of said light emitting elements is caused to emit light continuously during a first part of said light emission period in said first drive period, and caused to emit light continuously during a remaining part of said light emission period in said second drive period.

2. A display panel drive method as described in claim 1 wherein time interval between the start of emitting light in said first drive period and the start of emitting light in said second drive period is about one half of said unit display period.

3. A display panel drive method as described in claim 1 wherein said unit display period is divided into a plurality of divided display periods with all of said light emitting elements being initialized to either the light emitting cell state or an non-light emitting cell state, only during one of said divided display period that comes first in the first drive period;

a state of each of said light emitting elements is changed, in one of said divided display periods in said first drive period, from the non-light emitting cell state to an light emitting cell state or from the light emitting cell state to an non-light emitting cell state in accordance with said input video signal;
only those among said light emitting elements that are in the light emitting cell state are caused to emit light for a period of time determined by a weighting factor of said divided display period, in each of said divided display periods in said first drive period;
all of said light emitting elements are initialized to either the light emitting cell state or an non-light emitting cell state, only during the first divided display period in the second drive period;
a state of each of said light emitting elements is changed, in one of said divided display periods in said second drive period, from the non-light emitting cell state to an light emitting cell state or from the light emitting cell state to an non-light emitting cell state in accordance with said input video signal; and
only those among said light emitting elements that are in the light emitting cell state are caused to emit light for a period of time determined by the weighting factor of said divided display period, in each of said divided display periods in said second drive period.

4. A display panel drive method for driving toned display of a display panel, having a display screen formed from a plurality of light emitting elements, by causing each of said light emitting elements to emit light for a light emission period that corresponds to the luminance level of the input video signal in the unit display period; comprising

a first drive sequence for causing each of said light emitting elements to emit light continuously during said light emission period within said unit display period; and
a second drive sequence, in which said unit display period comprises a first drive period of a first half and a second drive period of a second half, for causing each of said light emitting elements to emit light continuously during a first part of said light emission period in said first drive period, and to emit light continuously during a remaining part of said light emission period in said second drive period;
wherein either said first drive sequence or said second drive sequence is selectively executed according to the vertical synchronization frequency of said input video signal.

5. A display panel drive method as described in claim 4 wherein the time interval between the start of emitting light in said first drive period and the start of emitting light in said second drive period is about one half of said unit display period.

6. A display panel drive method as described in claim 4 wherein said first drive sequence is executed when the vertical synchronization frequency of said input video signal is equal to or higher than a predetermined frequency, while said second drive sequence is executed when the vertical synchronization frequency of said input video signal is lower than said predetermined frequency.

7. A display panel drive method as described in claim 4 wherein said unit display period is divided into a plurality of divided display periods, with all of said light emitting elements being initialized to either a light emitting cell state or a non-light emitting cell state, only during the first divided display period in said first drive period;

a state of each of said light emitting elements is changed, in one of said divided display periods in said first drive period, from the non-light emitting cell state to the light emitting cell state or from the light emitting cell state to the non-light emitting cell state in accordance with said input video signal;
only those among said light emitting elements that are in the light emitting cell state are caused to emit light for a period of time determined by the weighting factor of said divided display period, in each of said divided display periods in said first drive period;
all of said light emitting elements are initialized to either the light emitting cell state or the non-light emitting cell state, only during the first divided display period in said second drive period;
the state of said light emitting elements is changed, in one of said divided display periods in said second drive period, from the non-light emitting cell state to the light emitting cell state or from the light emitting cell state to the non-light emitting cell state in accordance with said input video signal; and
only those among said light emitting elements that are in the light emitting cell state are caused to emit light for a period of time deter-

mined by the weighting factor of said divided display period, in each of said divided display periods in said second drive period.

8. A method for driving a display panel having a display screen formed from a plurality of light emitting elements; wherein

a display period of one field of input video signal comprises N sub-fields that are allocated to a first drive period of a first half of said display period of one field and a second drive period of a second half thereof, so as to provide display with N+1 intermediate levels of luminance from the first through (N+1)st tones;
in the case where said number N is an even number,
said light emitting elements are not caused to emit light in any of said sub-fields for said first tone; said light emitting elements are caused to emit light only in the first sub-field during either one of said first drive period and said second drive period for the second tone; said light emitting elements are caused to emit light only in the first sub-field during the other one of said first drive period and said second drive period, in addition to the sub-fields in which light is emitted for the second tone, for the third tone; said light emitting elements are caused to emit light only in the sub-field that is disposed at the second position during either one of said first drive period and said second drive period, in addition to the sub-fields in which light is emitted for the third tone, for the fourth tone; said light emitting elements are caused to emit light in the last sub-field during either one of said first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the (N-1)st tone, for the Nth tone; and said light emitting elements are caused to emit light in the last sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the Nth tone, for the (N+1)st tone; while
in the case where said number N is an odd number,
said light emitting elements are not caused to emit light in any of said sub-fields for said first tone; said light emitting elements are caused to emit light only in the first sub-field during either one of the first drive period and the second drive period for the second tone; said light emitting elements are caused to emit light only in the first sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the second tone, for the third tone; said light emitting elements are caused to emit light in the sub-field that is disposed at the second position during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the third tone, for the fourth tone; said light emitting elements are caused to emit light in the last sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the (N-1)st tone, for the Nth tone; and said light emitting elements are caused to emit light in the last sub-field during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the Nth tone, for the (N+1)st tone.

9. A method for driving a display panel having a display screen formed from a plurality of light emitting elements; wherein

with the display period of one field of input video signal being divided into N sub-fields that are allocated to a first drive period of the first half of said display period of one field and a second drive period of the second half, so as to provide display with N+1 intermediate levels of luminance from the first through (N+1)st tones;
in the case where said number N is an even number,
said light emitting elements are not caused to emit light in any of said sub-fields for said first tone; said light emitting elements are caused to emit light only in the last sub-field during either one of the first drive period and the second drive period for the second tone; said light emitting elements are caused to emit light only in the last sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the second tone, for the third tone; said light emitting elements are caused to emit light only in the sub-field that is disposed immediately before the last sub-field during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the third tone, for the fourth tone; said light emitting elements are caused to emit light in the first sub-field during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the (N-1)st tone, for the Nth tone; and said light emitting elements are caused to emit light in the first sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the Nth tone, for the (N+1)st tone; while

in the case where said number N is an odd number,
said light emitting elements are not caused to emit light in any of said sub-fields for said first tone; said light emitting elements are caused to emit light only in the last sub-field during either one of the first drive period and the second drive period for the second tone; said light emitting elements are caused to emit light only in the last sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the second tone, for the third tone; said light emitting elements are caused to emit light in the sub-field that is disposed immediately before the last sub-field during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the third tone, for the fourth tone; said light emitting elements are caused to emit light in the first sub-field during the other one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the (N-1)st tone, for the Nth tone; and said light emitting elements are caused to emit light in the first sub-field during either one of the first drive period and the second drive period, in addition to the sub-fields in which light is emitted for the Nth tone, for the (N+1)st tone.

10. A method for driving a display panel having a display screen formed from a plurality of light emitting elements; wherein

with the display period of one field of input video signal comprises N sub-fields so as to provide display with N+1 intermediate levels of luminance from the first tone through the (N+1)st tone;
said light emitting elements are caused to emit light in the other one of the sub-field in addition to the sub-fields in which light is emitted for the (n-1)st tone, for the nth tone ($1 \leq n \leq N+1$), while time interval between the start of emitting light in the sub-fields in which light is emitted for the (n-1)st tone or the sub-fields in which light is emitted for the (n+1)st tone and the start of emitting light in the sub-fields where light is emitted for the mth tone ($2 \leq m \leq N$) is about one half the length of the display period of one field.

FIG. 1

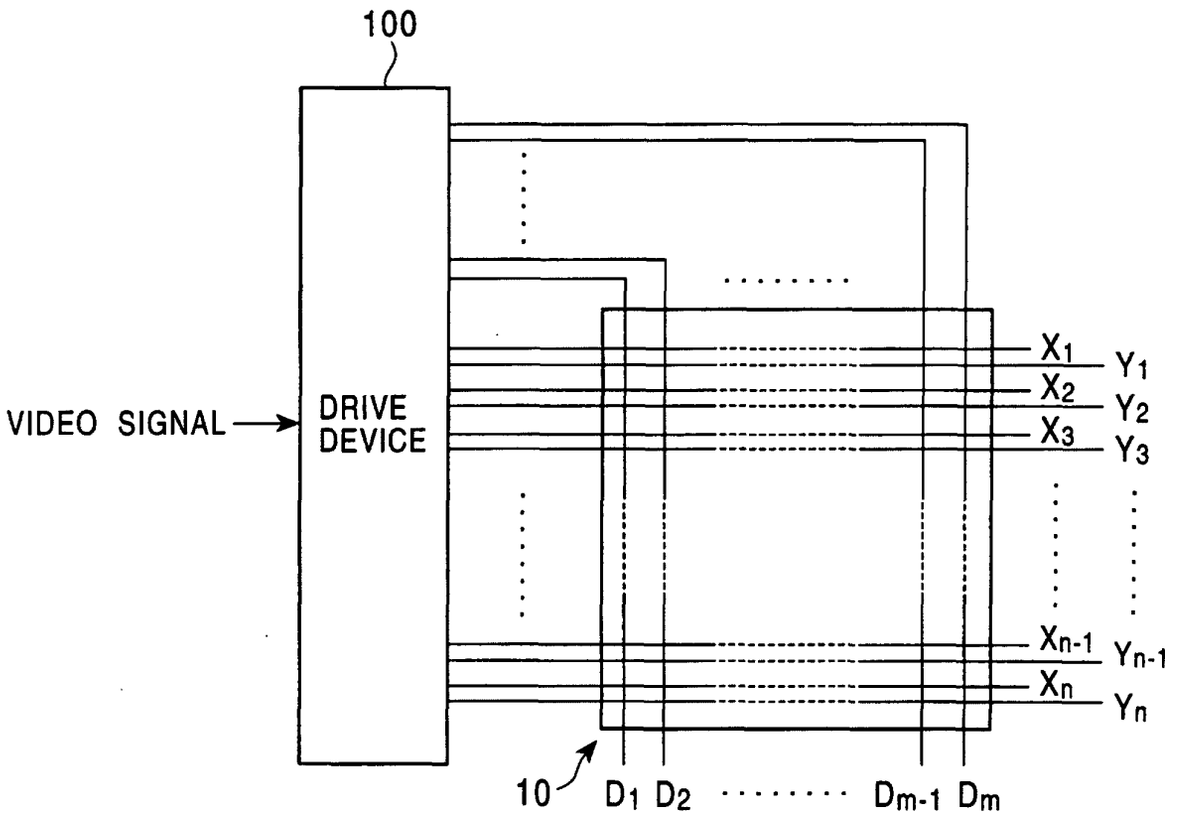

100
VIDEO SIGNAL
DRIVE DEVICE
X1
Y1
X2
Y2
X3
Y3
Xn-1
Yn-1
Xn
Yn
10
D1 D2
Dm-1 Dm

FIG. 2

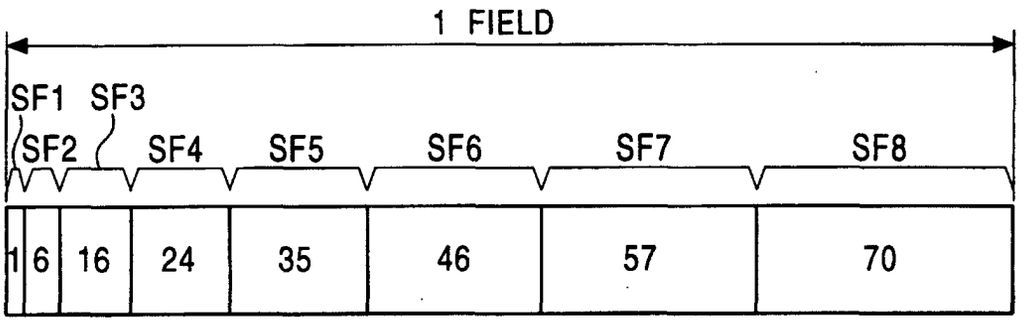


FIG. 3

TONE	LIGHT EMISSION DRIVE PATTERN IN 1 FIELD								LUMI-NANCE
	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	
1									0
2	○								1
3	○	○							7
4	○	○	○						23
5	○	○	○	○					47
6	○	○	○	○	○				82
7	○	○	○	○	○	○			128
8	○	○	○	○	○	○	○		185
9	○	○	○	○	○	○	○	○	255

○ : LIGHT EMISSION

FIG. 4

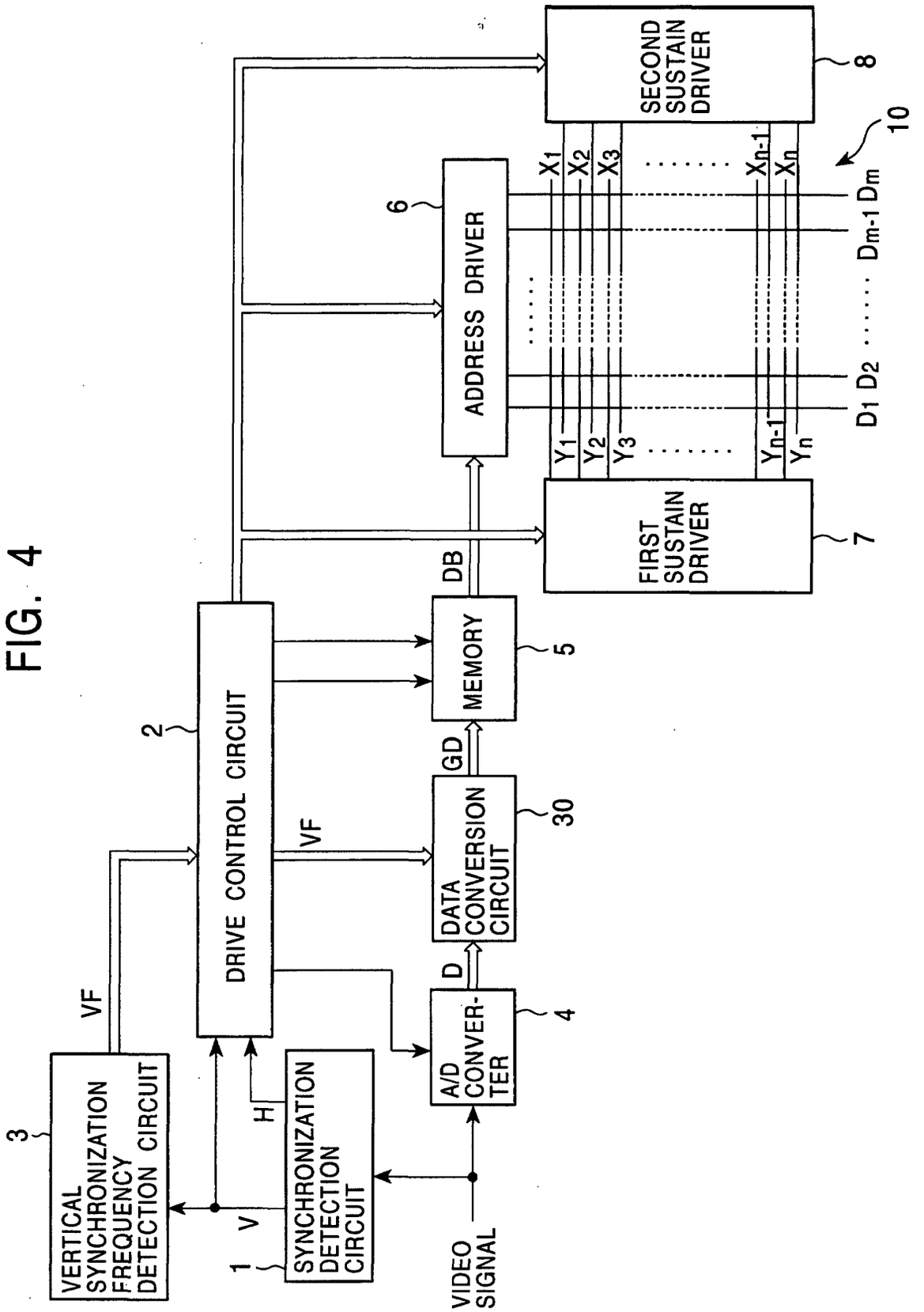

VERTICAL SYNCHRONIZATION FREQUENCY DETECTION CIRCUIT
3
VF
SYNCHRONIZATION DETECTION CIRCUIT
1
V
H
VIDEO SIGNAL
DRIVE CONTROL CIRCUIT
2
A/D CONVERTER
4
D
DATA CONVERSION CIRCUIT
30
GD
MEMORY
5
DB
ADDRESS DRIVER
6
FIRST SUSTAIN DRIVER
7
SECOND SUSTAIN DRIVER
8
10
X1 X2 X3 ..... Xn-1 Xn
Y1 Y2 Y3 ..... Yn-1 Yn
D1 D2 ..... Dm-1 Dm

FIG. 5

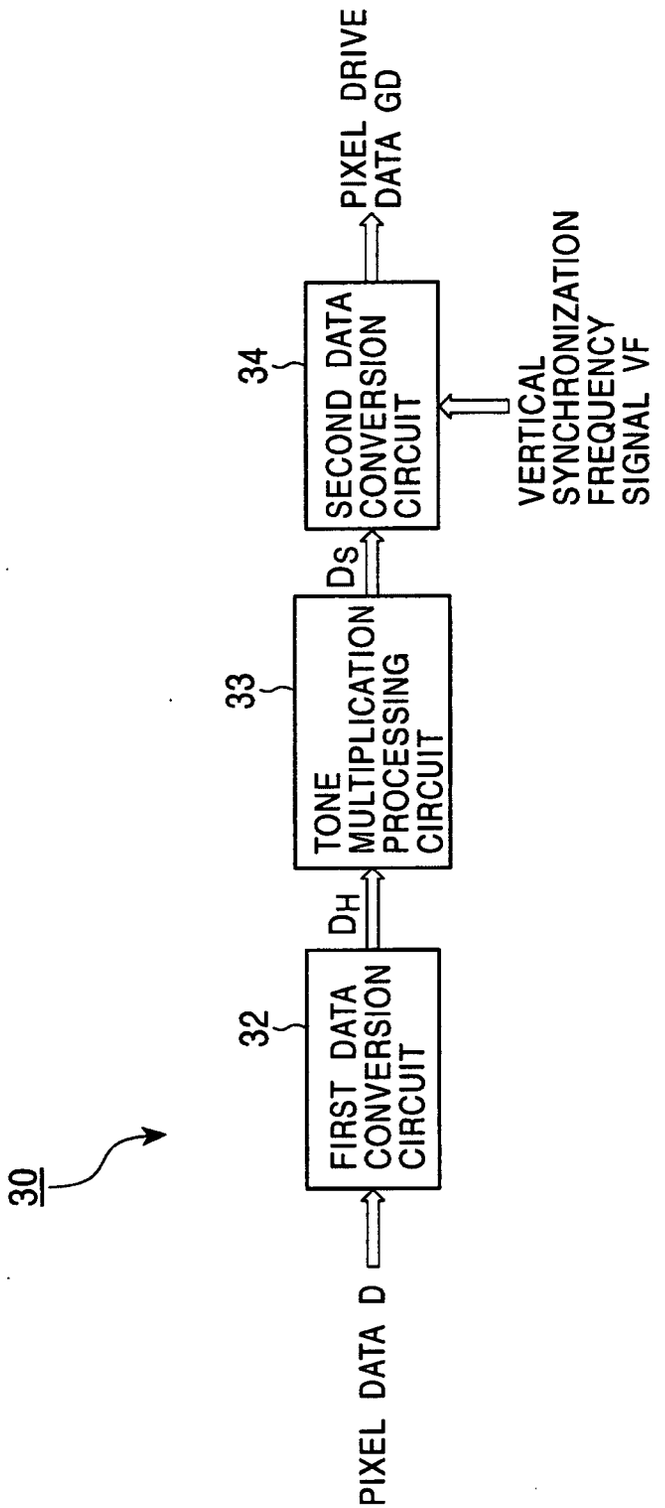

30
32
FIRST DATA CONVERSION CIRCUIT
DH
33
TONE MULTIPLICATION PROCESSING CIRCUIT
DS
34
SECOND DATA CONVERSION CIRCUIT
PIXEL DATA D
PIXEL DRIVE DATA GD
VERTICAL SYNCHRONIZATION FREQUENCY SIGNAL VF

FIG. 6

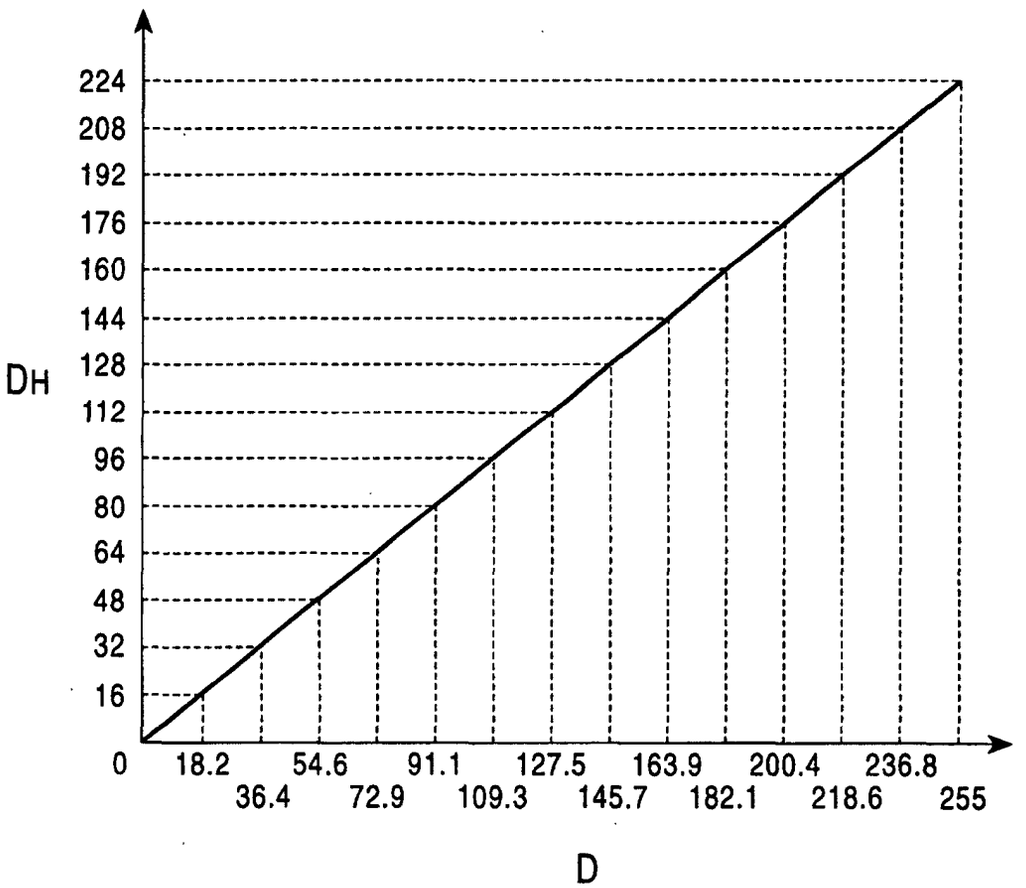

DH
224
208
192
176
160
144
128
112
96
80
64
48
32
16
0
18.2
36.4
54.6
72.9
91.1
109.3
127.5
145.7
163.9
182.1
200.4
218.6
236.8
255
D

FIG. 7

D		D_H		D		D_H	
LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7
0	00000000	0	00000000	64	01000000	56	00111000
1	00000001	0	00000000	65	01000001	57	00111001
2	00000010	1	00000001	66	01000010	57	00111001
3	00000011	2	00000010	67	01000011	58	00111010
4	00000100	3	00000011	68	01000100	59	00111011
5	00000101	4	00000100	69	01000101	60	00111100
6	00000110	5	00000101	70	01000110	61	00111101
7	00000111	6	00000110	71	01000111	62	00111110
8	00001000	7	00000111	72	01001000	63	00111111
9	00001001	7	00000111	73	01001001	64	01000000
10	00001010	8	00001000	74	01001010	65	01000001
11	00001011	9	00001001	75	01001011	65	01000001
12	00001100	10	00001010	76	01001100	66	01000010
13	00001101	11	00001011	77	01001101	67	01000011
14	00001110	12	00001100	78	01001110	68	01000100
15	00001111	13	00001101	79	01001111	69	01000101
16	00010000	14	00001110	80	01010000	70	01000110
17	00010001	14	00001110	81	01010001	71	01000111
18	00010010	15	00001111	82	01010010	72	01001000
19	00010011	16	00010000	83	01010011	72	01001000
20	00010100	17	00010001	84	01010100	73	01001001
21	00010101	18	00010010	85	01010101	74	01001010
22	00010110	19	00010011	86	01010110	75	01001011
23	00010111	20	00010100	87	01010111	76	01001100
24	00011000	21	00010101	88	01011000	77	01001101
25	00011001	21	00010101	89	01011001	77	01001101
26	00011010	22	00010110	90	01011010	78	01001110
27	00011011	23	00010111	91	01011011	79	01001111
28	00011100	24	00011000	92	01011100	80	01010000
29	00011101	25	00011001	93	01011101	81	01010001
30	00011110	26	00011010	94	01011110	82	01010010
31	00011111	27	00011011	95	01011111	83	01010011
32	00100000	28	00011100	96	01100000	84	01010100
33	00100001	28	00011100	97	01100001	85	01010101
34	00100010	29	00011101	98	01100010	86	01010110
35	00100011	30	00011110	99	01100011	86	01010110
36	00100100	31	00011111	100	01100100	87	01010111
37	00100101	32	00100000	101	01100101	88	01011000
38	00100110	33	00100001	102	01100110	89	01011001
39	00100111	34	00100010	103	01100111	90	01011010
40	00101000	35	00100011	104	01101000	91	01011011
41	00101001	36	00100100	105	01101001	92	01011100
42	00101010	36	00100100	106	01101010	93	01011101
43	00101011	37	00100101	107	01101011	93	01011101
44	00101100	38	00100110	108	01101100	94	01011110
45	00101101	39	00100111	109	01101101	95	01011111
46	00101110	40	00101000	110	01101110	96	01100000
47	00101111	41	00101001	111	01101111	97	01100001
48	00110000	42	00101010	112	01110000	98	01100010
49	00110001	43	00101011	113	01110001	99	01100011
50	00110010	43	00101011	114	01110010	100	01100100
51	00110011	44	00101100	115	01110011	101	01100101
52	00110100	45	00101101	116	01110100	101	01100101
53	00110101	46	00101110	117	01110101	102	01100110
54	00110110	47	00101111	118	01110110	103	01100111
55	00110111	48	00110000	119	01110111	104	01101000
56	00111000	49	00110001	120	01111000	105	01101001
57	00111001	50	00110010	121	01111001	106	01101010
58	00111010	50	00110010	122	01111010	107	01101011
59	00111011	51	00110011	123	01111011	108	01101100
60	00111100	52	00110100	124	01111100	108	01101100
61	00111101	53	00110101	125	01111101	109	01101101
62	00111110	54	00110110	126	01111110	110	01101110
63	00111111	55	00110111	127	01111111	111	01101111

FIG. 8

D		D_H		D		D_H	
LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7	LUMINANCE LEVEL	0 ~ 7
128	10000000	112	0111 0000	192	11000000	168	10101000
129	10000001	113	0111 0001	193	11000001	169	10101001
130	10000010	114	0111 0010	194	11000010	170	10101010
131	10000011	115	0111 0011	195	11000011	171	10101011
132	10000100	115	0111 0011	196	11000100	172	10101100
133	10000101	116	0111 0100	197	11000101	173	10101101
134	10000110	117	0111 0101	198	11000110	173	10101101
135	10000111	118	0111 0110	199	11000111	174	10101110
136	10001000	119	0111 0111	200	11001000	175	10101111
137	10001001	120	0111 1000	201	11001001	176	10110000
138	10001010	121	0111 1001	202	11001010	177	10110001
139	10001011	122	0111 1010	203	11001011	178	10110010
140	10001100	122	0111 1010	204	11001100	179	10110011
141	10001101	123	0111 1011	205	11001101	180	10110100
142	10001110	124	0111 1100	206	11001110	180	10110100
143	10001111	125	0111 1101	207	11001111	181	10110101
144	10010000	126	0111 1110	208	11010000	182	10110110
145	10010001	127	0111 1111	209	11010001	183	10110111
146	10010010	128	10000000	210	11010010	184	10111000
147	10010011	129	10000001	211	11010011	185	10111001
148	10010100	130	10000010	212	11010100	186	10111010
149	10010101	130	10000010	213	11010101	187	10111011
150	10010110	131	10000011	214	11010110	187	10111011
151	10010111	132	10000100	215	11010111	188	10111100
152	10011000	133	10000101	216	11011000	189	10111101
153	10011001	134	10000110	217	11011001	190	10111110
154	10011010	135	10000111	218	11011010	191	10111111
155	10011011	136	10001000	219	11011011	192	11000000
156	10011100	137	10001001	220	11011100	193	11000001
157	10011101	137	10001001	221	11011101	194	11000010
158	10011110	138	10001010	222	11011110	195	11000011
159	10011111	139	10001011	223	11011111	195	11000011
160	10100000	140	10001100	224	11100000	196	11000100
161	10100001	141	10001101	225	11100001	197	11000101
162	10100010	142	10001110	226	11100010	198	11000110
163	10100011	143	10001111	227	11100011	199	11000111
164	10100100	144	10010000	228	11100100	200	11001000
165	10100101	144	10010000	229	11100101	201	11001001
166	10100110	145	10010001	230	11100110	202	11001010
167	10100111	146	10010010	231	11100111	202	11001010
168	10101000	147	10010011	232	11101000	203	11001011
169	10101001	148	10010100	233	11101001	204	11001100
170	10101010	149	10010101	234	11101010	205	11001101
171	10101011	150	10010110	235	11101011	206	11001110
172	10101100	151	10010111	236	11101100	207	11001111
173	10101101	151	10010111	237	11101101	208	11010000
174	10101110	152	10011000	238	11101110	209	11010001
175	10101111	153	10011001	239	11101111	209	11010001
176	10110000	154	10011010	240	1111 0000	210	11010010
177	10110001	155	10011011	241	1111 0001	211	11010011
178	10110010	156	10011100	242	1111 0010	212	11010100
179	10110011	157	10011101	243	1111 0011	213	11010101
180	10110100	158	10011110	244	1111 0100	214	11010110
181	10110101	158	10011110	245	1111 0101	215	11010111
182	10110110	159	10011111	246	1111 0110	216	11011000
183	10110111	160	10010000	247	1111 0111	216	11011000
184	10111000	161	10100001	248	1111 1000	217	11011001
185	10111001	162	10100010	249	1111 1001	218	11011010
186	10111010	163	10100011	250	1111 1010	219	11011011
187	10111011	164	10100100	251	1111 1011	220	11011100
188	10111100	165	10100101	252	1111 1100	221	11011101
189	10111101	166	10100110	253	1111 1101	222	11011110
190	10111110	166	10100110	254	1111 1110	223	11011111
191	10111111	167	10100111	255	1111 1111	224	11100000

FIG. 9

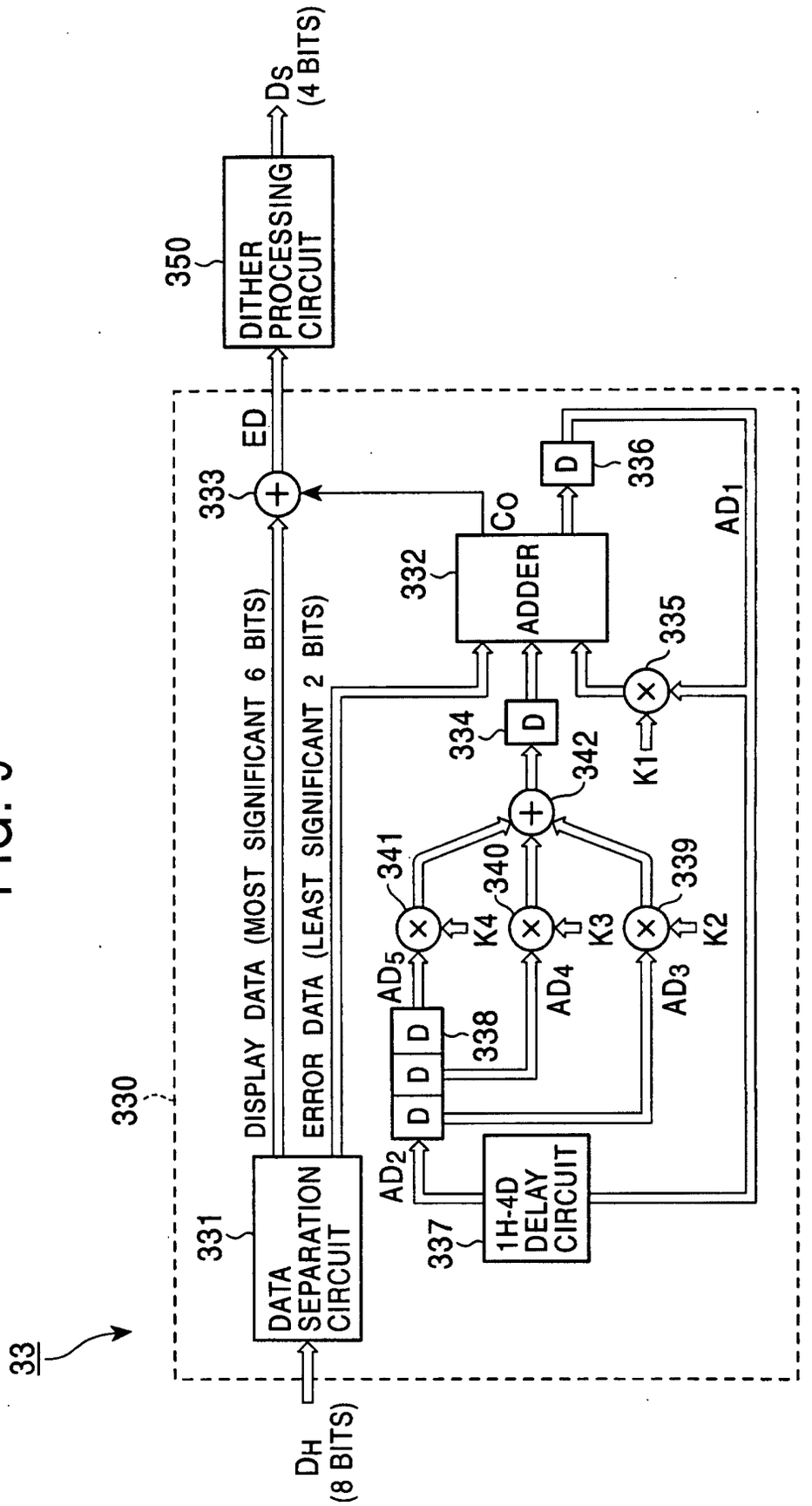

33
330
331
DATA SEPARATION CIRCUIT
DISPLAY DATA (MOST SIGNIFICANT 6 BITS)
ERROR DATA (LEAST SIGNIFICANT 2 BITS)
DH (8 BITS)
333
ED
350
DITHER PROCESSING CIRCUIT
DS (4 BITS)
332
ADDER
CO
336
D
AD1
335
K1
334
342
341
340
339
K4
K3
K2
AD5
AD4
AD3
338
AD2
337
1H-4D DELAY CIRCUIT

FIG. 10

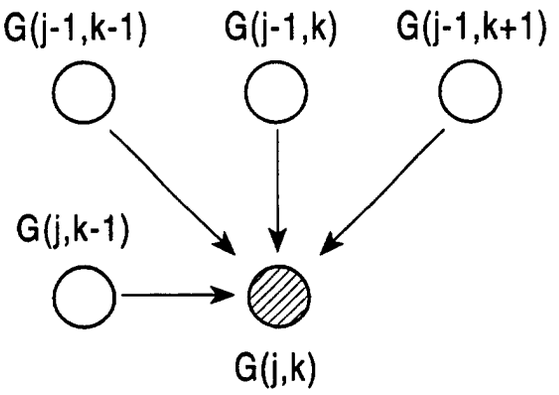

G(j-1,k-1)
G(j-1,k)
G(j-1,k+1)
G(j,k-1)
G(j,k)

FIG. 11

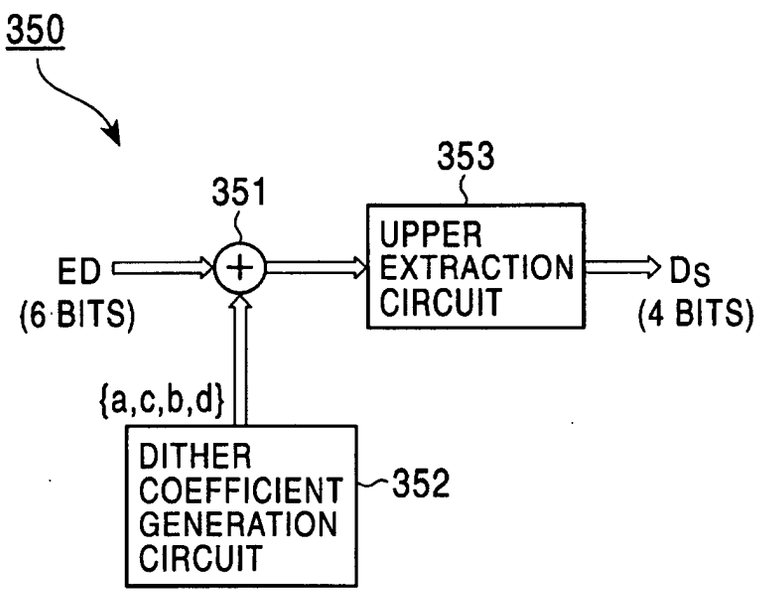

350
353
351
ED
(6 BITS)
UPPER
EXTRACTION
CIRCUIT
Ds
(4 BITS)
{a,c,b,d}
DITHER
COEFFICIENT
GENERATION
CIRCUIT
352

FIG. 12

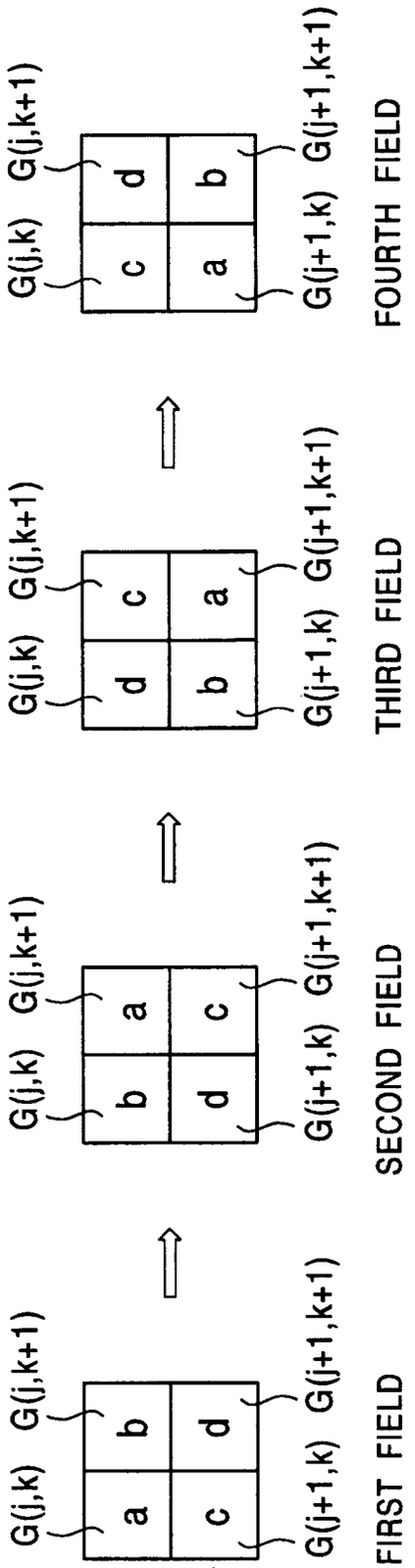

G(j,k)
G(j,k+1)
a
b
c
d
G(j+1,k)
G(j+1,k+1)
FIRST FIELD
SECOND FIELD
THIRD FIELD
FOURTH FIELD

FIG. 13

[SELECTIVE ERASURE]

TONE	FIRST DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD														LUMINANCE OF LIGHT EMITTED
	Ds	GD														SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
1	0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	●														0
2	0001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	○	●													1
3	0010	0	0	1	0	0	0	0	0	0	0	0	0	0	0	○	○	●												4
4	0011	0	0	0	1	0	0	0	0	0	0	0	0	0	0	○	○	○	●											9
5	0100	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●										17
6	0101	0	0	0	0	0	1	0	0	0	0	0	0	0	0	○	○	○	○	○	●									27
7	0110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●								40
8	0111	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	●							56
9	1000	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	●						75
10	1001	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	●					97
11	1010	0	0	0	0	0	0	0	0	0	0	1	0	0	0	○	○	○	○	○	○	○	○	○	○	●				122
12	1011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	●			150
13	1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	●		182
14	1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE

WHITE CIRCLE: LIGHT EMISSION

FIG. 14

[SELECTIVE ERASURE]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD														LUMINANCE OF LIGHT EMITTED
	Ds	GD														SF 1	SF 3	SF 5	SF 7	SF 9	SF 11	SF 13	SF 2	SF 4	SF 6	SF 8	SF 10	SF 12	SF 14	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14															
1	0000	1	0	0	0	0	0	0	1	0	0	0	0	0	0	●							●							0
2	0001	0	1	0	0	0	0	0	1	0	0	0	0	0	0	○	●						●							1
3	0010	0	1	0	0	0	0	0	0	1	0	0	0	0	0	○	●						○	●						4
4	0011	0	0	1	0	0	0	0	0	1	0	0	0	0	0	○	○	●					○	●						9
5	0100	0	0	1	0	0	0	0	0	0	1	0	0	0	0	○	○	●					○	○	●					17
6	0101	0	0	0	1	0	0	0	0	0	1	0	0	0	0	○	○	○	●				○	○	●					27
7	0110	0	0	0	1	0	0	0	0	0	0	1	0	0	0	○	○	○	●				○	○	○	●				40
8	0111	0	0	0	0	1	0	0	0	0	0	1	0	0	0	○	○	○	○	●			○	○	○	●				56
9	1000	0	0	0	0	1	0	0	0	0	0	0	1	0	0	○	○	○	○	●			○	○	○	○	●			75
10	1001	0	0	0	0	0	1	0	0	0	0	0	1	0	0	○	○	○	○	○	●		○	○	○	○	●			97
11	1010	0	0	0	0	0	1	0	0	0	0	0	0	1	0	○	○	○	○	○	●		○	○	○	○	○	●		122
12	1011	0	0	0	0	0	0	1	0	0	0	0	0	1	0	○	○	○	○	○	○	●	○	○	○	○	○	●		150
13	1100	0	0	0	0	0	0	1	0	0	0	0	0	0	1	○	○	○	○	○	○	●	○	○	○	○	○	○	●	182
14	1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE

WHITE CIRCLE: LIGHT EMISSION

FIG. 15

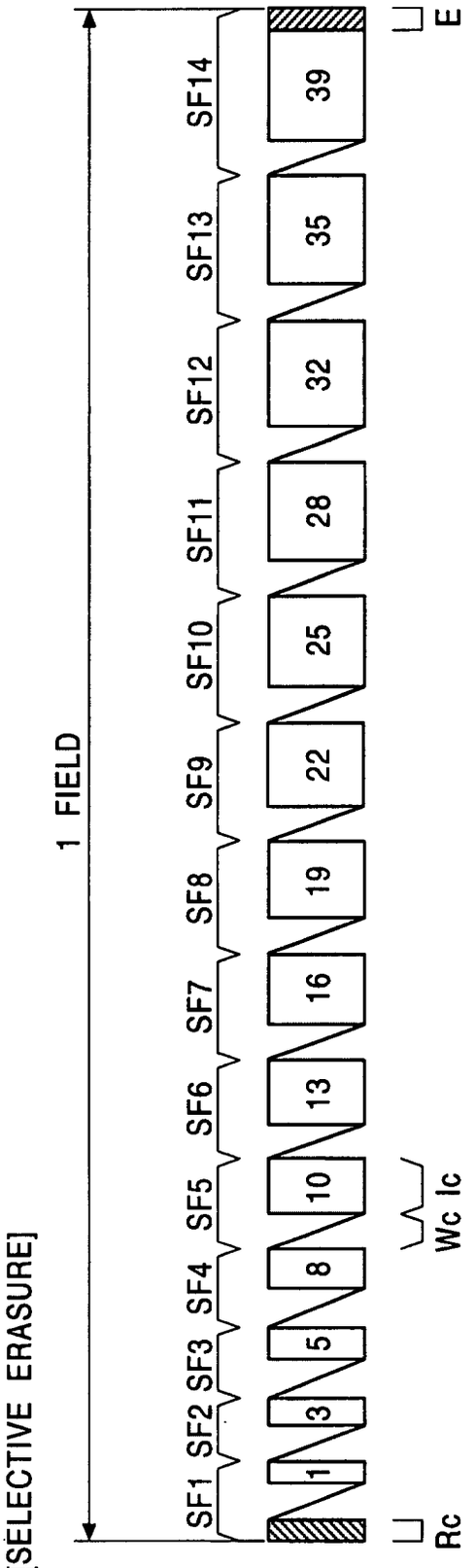

[SELECTIVE ERASURE]
1 FIELD
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
SF9
SF10
SF11
SF12
SF13
SF14
1
3
5
8
10
13
16
19
22
25
28
32
35
39
Rc
Wc
Ic
E

FIG. 16

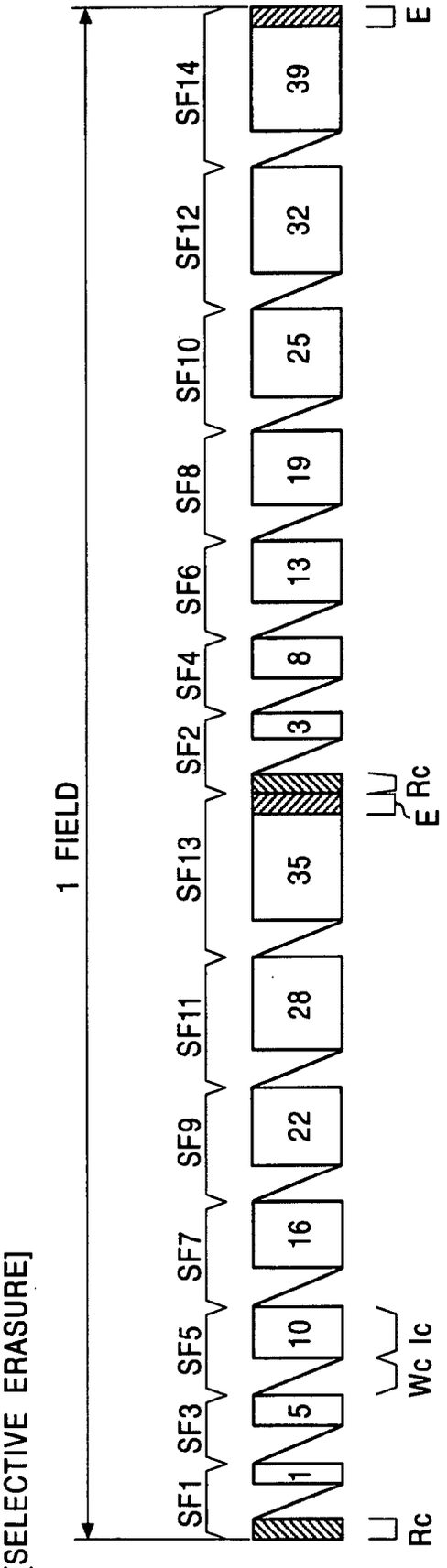

[SELECTIVE ERASURE]
1 FIELD
SF1
SF3
SF5
SF7
SF9
SF11
SF13
SF2
SF4
SF6
SF8
SF10
SF12
SF14
1
5
10
16
22
28
35
3
8
13
19
25
32
39
Rc
Wc Ic
E Rc
E

FIG. 17

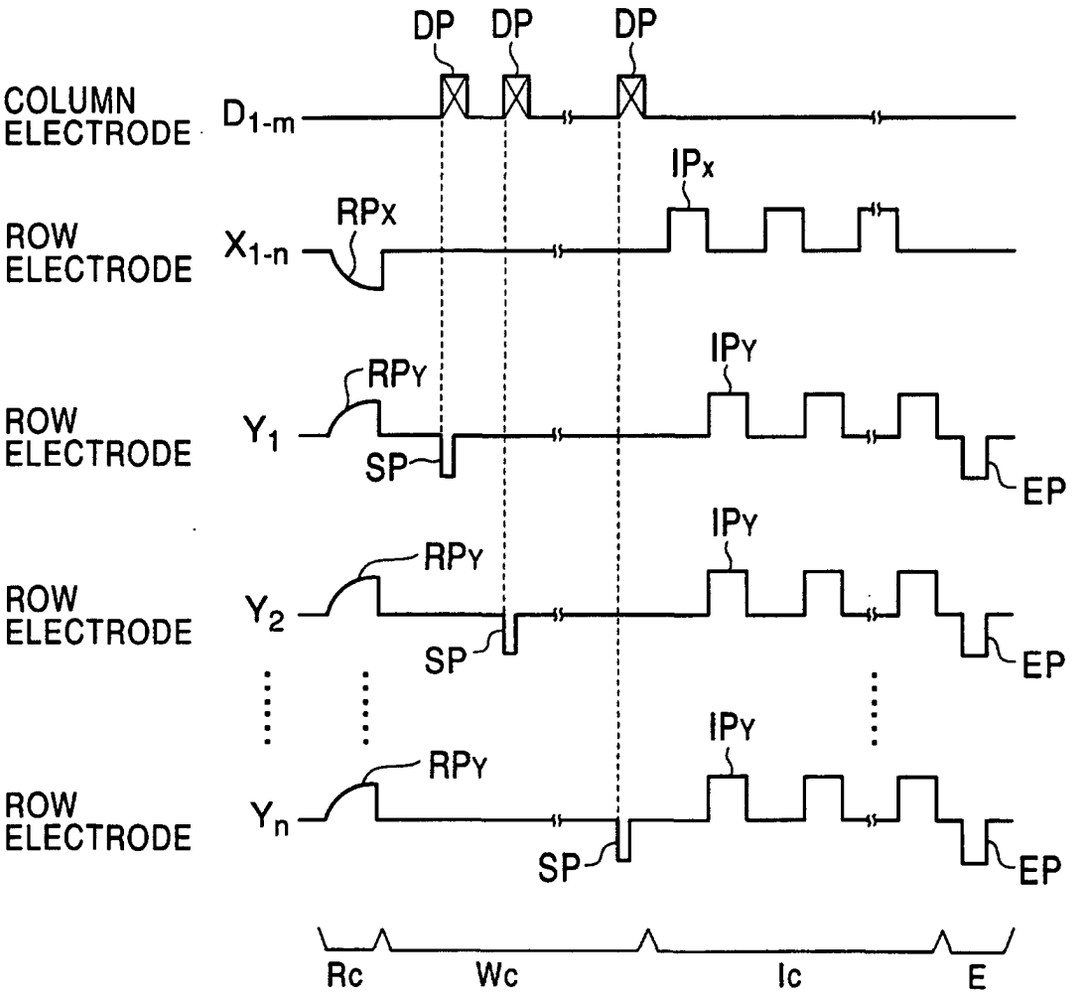

DP
DP
DP
COLUMN ELECTRODE
D1-m
IPx
RPx
ROW ELECTRODE
X1-n
IPY
RPY
ROW ELECTRODE
Y1
SP
EP
IPY
RPY
ROW ELECTRODE
Y2
SP
EP
IPY
RPY
ROW ELECTRODE
Yn
SP
EP
Rc
Wc
Ic
E

FIG. 18

[SELECTIVE ERASURE]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD													LUMINANCE OF LIGHT EMITTED
	Ds	GD														SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	3	5	7	9	11	13	2	4	6	8	10	12	14	
1	0000	1	1	0	0	0	0	0	1	1	0	0	0	0	0	●	●						●	●						0
2	0001	0	1	1	0	0	0	0	1	1	0	0	0	0	0	○	●						●	●						1
3	0010	0	1	1	0	0	0	0	0	1	1	0	0	0	0	○	●	●					○	●	●					4
4	0011	0	0	1	1	0	0	0	0	1	1	0	0	0	0	○	○	●					○	●	●					9
5	0100	0	0	1	1	0	0	0	0	0	1	1	0	0	0	○	○	●	●				○	○	●	●				17
6	0101	0	0	0	1	1	0	0	0	0	1	1	0	0	0	○	○	●	●				○	○	●	●				27
7	0110	0	0	0	1	1	0	0	0	0	0	1	1	0	0	○	○	○	●	●			○	○	○	●	●			40
8	0111	0	0	0	0	1	1	0	0	0	0	1	1	0	0	○	○	○	●	●			○	○	○	●	●			56
9	1000	0	0	0	0	1	1	0	0	0	0	0	1	1	0	○	○	○	○	●	●		○	○	○	○	●	●		75
10	1001	0	0	0	0	0	1	1	0	0	0	0	1	1	0	○	○	○	○	●	●	●	○	○	○	○	●	●		97
11	1010	0	0	0	0	0	1	1	0	0	0	0	0	1	1	○	○	○	○	○	●	●	○	○	○	○	○	●	●	122
12	1011	0	0	0	0	0	0	1	0	0	0	0	0	1	1	○	○	○	○	○	●	●	○	○	○	○	○	●	●	150
13	1100	0	0	0	0	0	0	1	0	0	0	0	0	0	1	○	○	○	○	○	○	●	○	○	○	○	○	○	●	182
14	1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE

WHITE CIRCLE: LIGHT EMISSION

FIG. 19

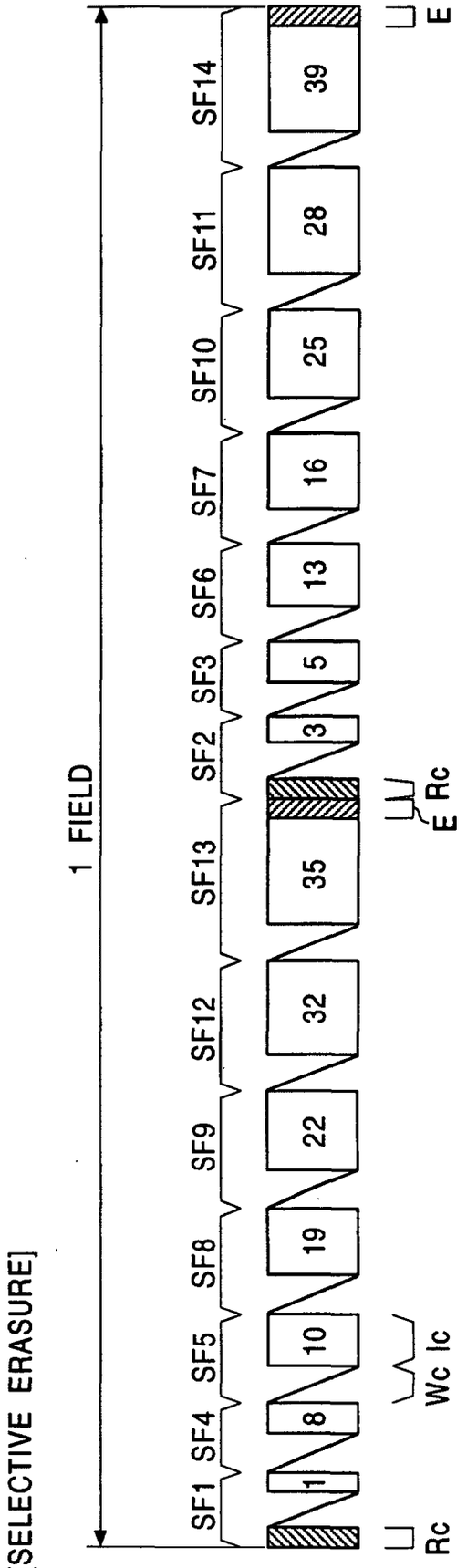

[SELECTIVE ERASURE]
1 FIELD
SF1
SF4
SF5
SF8
SF9
SF12
SF13
SF2
SF3
SF6
SF7
SF10
SF11
SF14
1
8
10
19
22
32
35
3
5
13
16
25
28
39
Rc
Wc
Ic
E
Rc
E

FIG. 20

[SELECTIVE ERASURE]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD														LUMINANCE OF LIGHT EMITTED
	Ds	GD														SF 1	SF 4	SF 5	SF 8	SF 9	SF 12	SF 13	SF 2	SF 3	SF 6	SF 7	SF 10	SF 11	SF 14	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14															
1	0000	1	0	0	0	0	0	0	1	0	0	0	0	0	0	●							●							0
2	0001	0	1	0	0	0	0	0	1	0	0	0	0	0	0	○	●						●							1
3	0010	0	1	0	0	0	0	0	0	1	0	0	0	0	0	○	●						○	●						4
4	0011	0	1	0	0	0	0	0	0	0	1	0	0	0	0	○	●						○	○	●					9
5	0100	0	0	1	0	0	0	0	0	0	1	0	0	0	0	○	○	●					○	○	●					17
6	0101	0	0	0	1	0	0	0	0	0	1	0	0	0	0	○	○	○	●				○	○	●					27
7	0110	0	0	0	1	0	0	0	0	0	0	1	0	0	0	○	○	○	●				○	○	○	●				40
8	0111	0	0	0	1	0	0	0	0	0	0	0	1	0	0	○	○	○	●				○	○	○	○	●			56
9	1000	0	0	0	0	1	0	0	0	0	0	0	1	0	0	○	○	○	○	●			○	○	○	○	●			75
10	1001	0	0	0	0	0	1	0	0	0	0	0	1	0	0	○	○	○	○	○	●		○	○	○	○	●			97
11	1010	0	0	0	0	0	1	0	0	0	0	0	0	1	0	○	○	○	○	○	●		○	○	○	○	○	●		122
12	1011	0	0	0	0	0	1	0	0	0	0	0	0	0	1	○	○	○	○	○	●		○	○	○	○	○	○	●	150
13	1100	0	0	0	0	0	0	1	0	0	0	0	0	0	1	○	○	○	○	○	○	●	○	○	○	○	○	○	●	182
14	1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE

WHITE CIRCLE: LIGHT EMISSION

FIG. 21

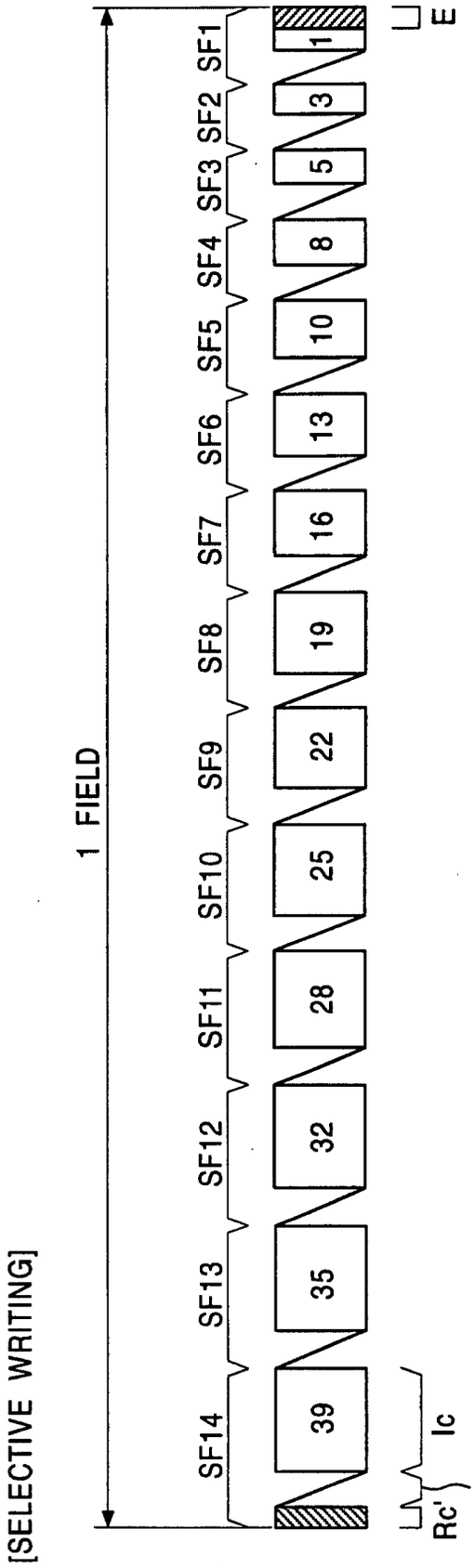

[SELECTIVE WRITING]
1 FIELD
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
SF9
SF10
SF11
SF12
SF13
SF14
1
3
5
8
10
13
16
19
22
25
28
32
35
39
E
Ic
Rc'
Wc'

FIG. 22

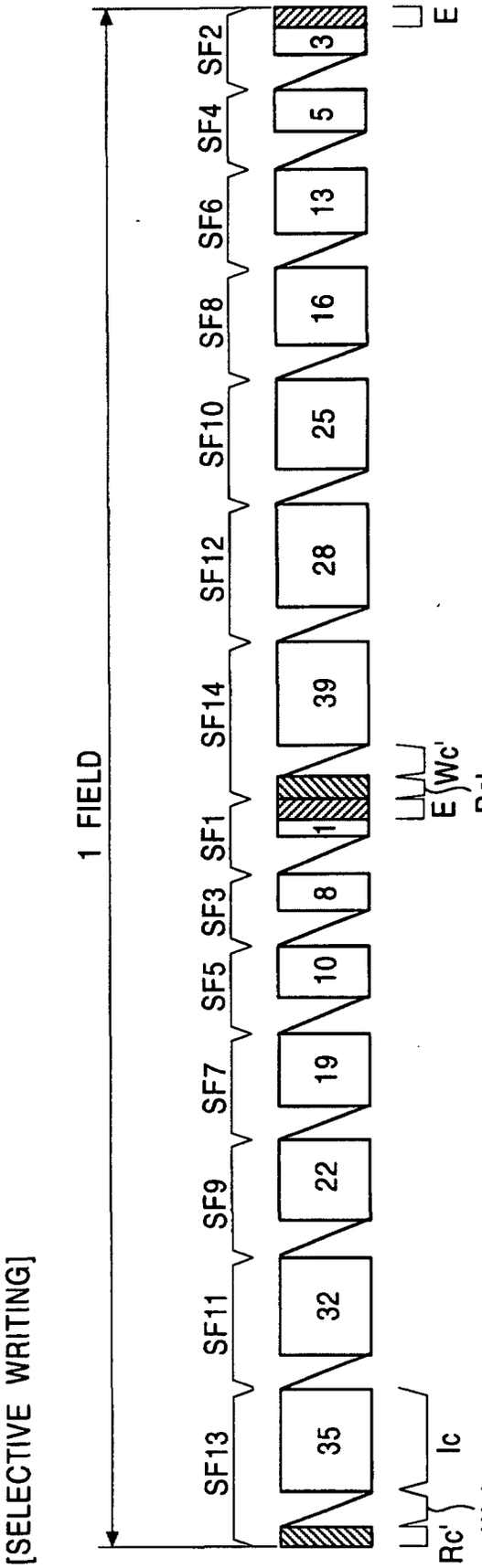

[SELECTIVE WRITING]
1 FIELD
SF13
SF11
SF9
SF7
SF5
SF3
SF1
SF14
SF12
SF10
SF8
SF6
SF4
SF2
35
32
22
19
10
8
1
39
28
25
16
13
5
3
Rc'
Wc'
Ic
E
Wc'
Rc'
E

FIG. 23

[SELECTIVE WRITING]

TONE	FIRST DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34														LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD												LUMINANCE OF LIGHT EMITTED
	Ds	GD													SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	SF	
		14	13	12	11	10	9	8	7	6	5	4	3	2	1	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
1	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0															0
2	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1														●	1
3	0010	0	0	0	0	0	0	0	0	0	0	0	0	1	0													●	○	4
4	0011	0	0	0	0	0	0	0	0	0	0	0	1	0	0												●	○	○	9
5	0100	0	0	0	0	0	0	0	0	0	0	1	0	0	0											●	○	○	○	17
6	0101	0	0	0	0	0	0	0	0	0	1	0	0	0	0										●	○	○	○	○	27
7	0110	0	0	0	0	0	0	0	0	1	0	0	0	0	0									●	○	○	○	○	○	40
8	0111	0	0	0	0	0	0	0	1	0	0	0	0	0	0								●	○	○	○	○	○	○	56
9	1000	0	0	0	0	0	0	1	0	0	0	0	0	0	0							●	○	○	○	○	○	○	○	75
10	1001	0	0	0	0	0	1	0	0	0	0	0	0	0	0						●	○	○	○	○	○	○	○	○	97
11	1010	0	0	0	0	1	0	0	0	0	0	0	0	0	0					●	○	○	○	○	○	○	○	○	○	122
12	1011	0	0	0	1	0	0	0	0	0	0	0	0	0	0				●	○	○	○	○	○	○	○	○	○	○	150
13	1100	0	0	1	0	0	0	0	0	0	0	0	0	0	0			●	○	○	○	○	○	○	○	○	○	○	○	182
14	1101	0	1	0	0	0	0	0	0	0	0	0	0	0	0		●	○	○	○	○	○	○	○	○	○	○	○	○	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	●	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE WRITING DISCHARGE + LIGHT EMISSION

WHITE CIRCLE: LIGHT EMISSION

FIG. 24

[SELECTIVE WRITING]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD													LUMINANCE OF LIGHT EMITTED
	Ds	GD 1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 13	SF 11	SF 9	SF 7	SF 5	SF 3	SF 1	SF 14	SF 12	SF 10	SF 8	SF 6	SF 4	SF 2	
1	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0															0
2	0001	0	0	0	0	0	0	1	0	0	0	0	0	0	0							●								1
3	0010	0	0	0	0	0	0	1	0	0	0	0	0	0	1							●							●	4
4	0011	0	0	0	0	0	1	0	0	0	0	0	0	0	1						●	○							●	9
5	0100	0	0	0	0	0	1	0	0	0	0	0	0	1	0						●	○						●	○	17
6	0101	0	0	0	0	1	0	0	0	0	0	0	0	1	0					●	○	○						●	○	27
7	0110	0	0	0	0	1	0	0	0	0	0	0	1	0	0					●	○	○					●	○	○	40
8	0111	0	0	0	1	0	0	0	0	0	0	0	1	0	0				●	○	○	○					●	○	○	56
9	1000	0	0	0	1	0	0	0	0	0	0	1	0	0	0				●	○	○	○				●	○	○	○	75
10	1001	0	0	1	0	0	0	0	0	0	0	1	0	0	0			●	○	○	○	○				●	○	○	○	97
11	1010	0	0	1	0	0	0	0	0	0	1	0	0	0	0			●	○	○	○	○			●	○	○	○	○	122
12	1011	0	1	0	0	0	0	0	0	0	1	0	0	0	0		●	○	○	○	○	○			●	○	○	○	○	150
13	1100	0	1	0	0	0	0	0	0	1	0	0	0	0	0		●	○	○	○	○	○		●	○	○	○	○	○	182
14	1101	1	0	0	0	0	0	0	0	1	0	0	0	0	0	●	○	○	○	○	○	○		●	○	○	○	○	○	217
15	1110	1	0	0	0	0	0	0	1	0	0	0	0	0	0	●	○	○	○	○	○	○	●	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE WRITING DISCHARGE + LIGHT EMISSION

WHITE CIRCLE: LIGHT EMISSION

FIG. 25

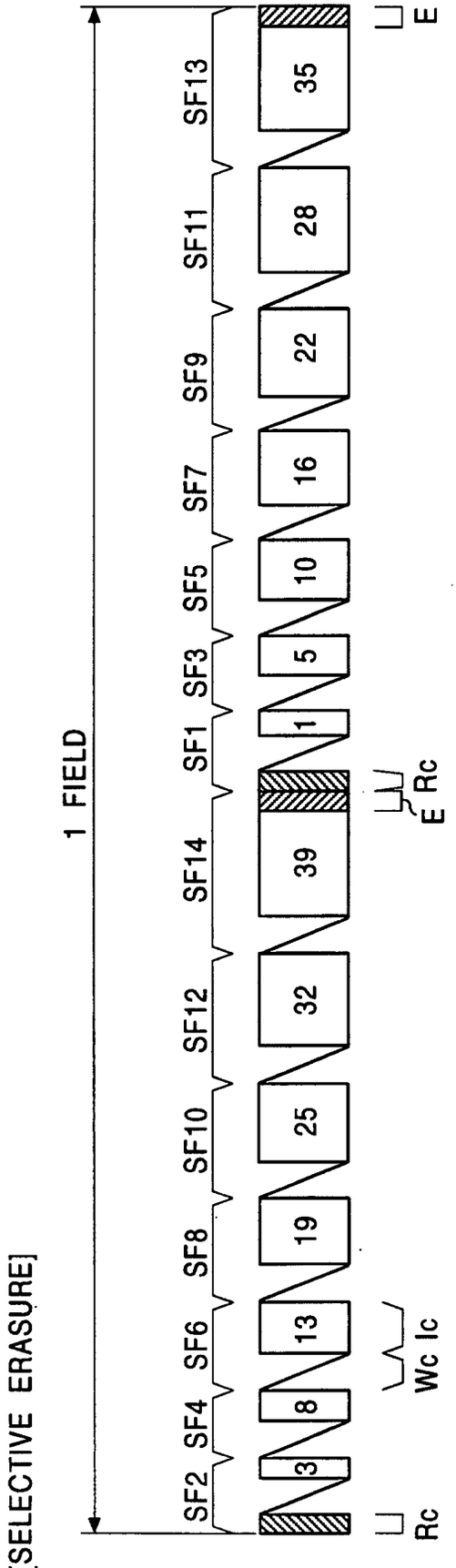

[SELECTIVE ERASURE]
1 FIELD
SF2
SF4
SF6
SF8
SF10
SF12
SF14
SF1
SF3
SF5
SF7
SF9
SF11
SF13
3
8
13
19
25
32
39
1
5
10
16
22
28
35
Rc
Wc
Ic
E
Rc
E

FIG. 26

[SELECTIVE ERASURE]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD													LUMINANCE OF LIGHT EMITTED
	Ds	GD 1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 2	SF 4	SF 6	SF 8	SF 10	SF 12	SF 14	SF 1	SF 3	SF 5	SF 7	SF 9	SF 11	SF 13	
1	0000	1	0	0	0	0	0	0	1	0	0	0	0	0	0	●							●							0
2	0001	1	0	0	0	0	0	0	0	1	0	0	0	0	0	●							○	●						1
3	0010	0	1	0	0	0	0	0	0	1	0	0	0	0	0	○	●						○	●						4
4	0011	0	1	0	0	0	0	0	0	0	1	0	0	0	0	○	●						○	○	●					9
5	0100	0	0	1	0	0	0	0	0	0	1	0	0	0	0	○	○	●					○	○	●					17
6	0101	0	0	1	0	0	0	0	0	0	0	1	0	0	0	○	○	●					○	○	○	●				27
7	0110	0	0	0	1	0	0	0	0	0	0	1	0	0	0	○	○	○	●				○	○	○	●				40
8	0111	0	0	0	1	0	0	0	0	0	0	0	1	0	0	○	○	○	●				○	○	○	○	●			56
9	1000	0	0	0	0	1	0	0	0	0	0	0	1	0	0	○	○	○	○	●			○	○	○	○	●			75
10	1001	0	0	0	0	1	0	0	0	0	0	0	0	1	0	○	○	○	○	●			○	○	○	○	○	●		97
11	1010	0	0	0	0	0	1	0	0	0	0	0	0	1	0	○	○	○	○	○	●		○	○	○	○	○	●		122
12	1011	0	0	0	0	0	1	0	0	0	0	0	0	0	1	○	○	○	○	○	●		○	○	○	○	○	○	●	150
13	1100	0	0	0	0	0	0	1	0	0	0	0	0	0	1	○	○	○	○	○	○	●	○	○	○	○	○	○	●	182
14	1101	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●	○	○	○	○	○	○	○	217
15	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE
WHITE CIRCLE: LIGHT EMISSION

FIG. 27

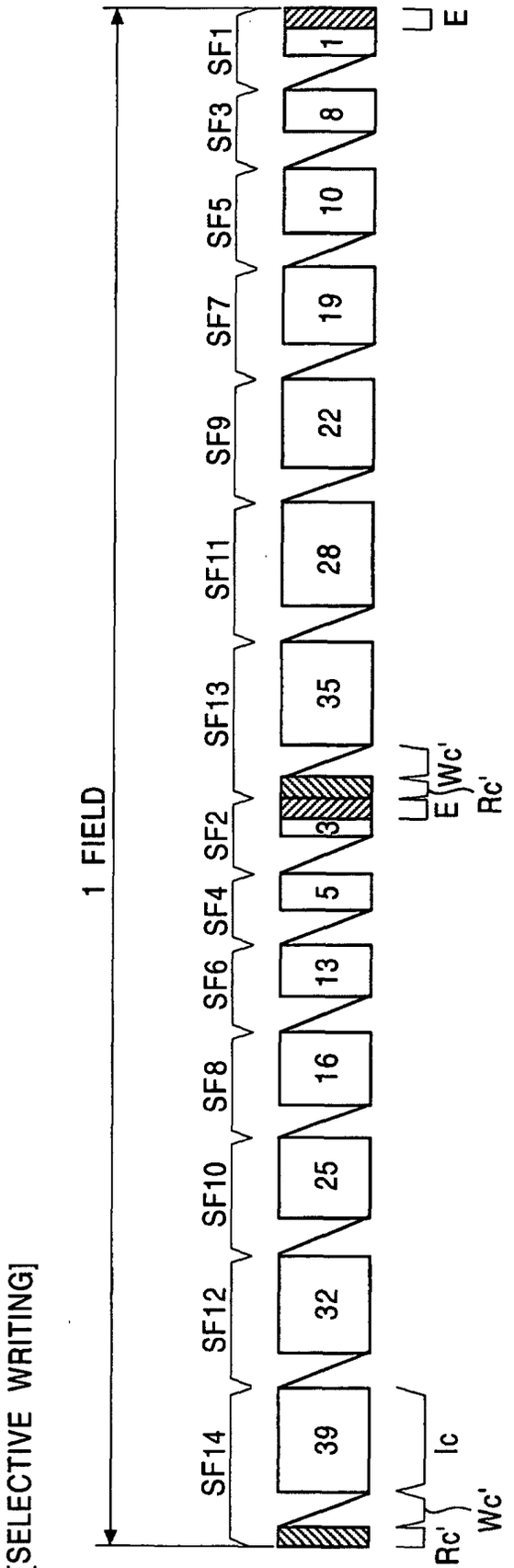

[SELECTIVE WRITING]
1 FIELD
SF14
SF12
SF10
SF8
SF6
SF4
SF2
SF13
SF11
SF9
SF7
SF5
SF3
SF1
39
32
25
16
13
5
3
35
28
22
19
10
8
1
Rc'
Wc'
Ic
E
E
Wc'
Rc'

FIG. 28

[SELECTIVE WRITING]

TONE	SECOND DATA CONVERSION TABLE OF SECOND DATA CONVERSION CIRCUIT 34															LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD														LUMINANCE OF LIGHT EMITTED
	Ds	GD														SF 14	SF 12	SF 10	SF 8	SF 6	SF 4	SF 2	SF 13	SF 11	SF 9	SF 7	SF 5	SF 3	SF 1	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14															
1	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0															0
2	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1														●	1
3	0010	0	0	0	0	0	0	1	0	0	0	0	0	0	1							●							●	4
4	0011	0	0	0	0	0	0	1	0	0	0	0	0	1	0							●						●	○	9
5	0100	0	0	0	0	0	1	0	0	0	0	0	0	1	0						●	○						●	○	17
6	0101	0	0	0	0	0	1	0	0	0	0	0	1	0	0						●	○					●	○	○	27
7	0110	0	0	0	0	1	0	0	0	0	0	0	1	0	0					●	○	○					●	○	○	40
8	0111	0	0	0	0	1	0	0	0	0	0	1	0	0	0					●	○	○				●	○	○	○	56
9	1000	0	0	0	1	0	0	0	0	0	0	1	0	0	0				●	○	○	○				●	○	○	○	75
10	1001	0	0	0	1	0	0	0	0	0	1	0	0	0	0				●	○	○	○			●	○	○	○	○	97
11	1010	0	0	1	0	0	0	0	0	0	1	0	0	0	0			●	○	○	○	○			●	○	○	○	○	122
12	1011	0	0	1	0	0	0	0	0	1	0	0	0	0	0			●	○	○	○	○		●	○	○	○	○	○	150
13	1100	0	1	0	0	0	0	0	0	1	0	0	0	0	0		●	○	○	○	○	○		●	○	○	○	○	○	182
14	1101	0	1	0	0	0	0	0	1	0	0	0	0	0	0		●	○	○	○	○	○	●	○	○	○	○	○	○	217
15	1110	1	0	0	0	0	0	0	1	0	0	0	0	0	0	●	○	○	○	○	○	○	●	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE WRITING DISCHARGE + LIGHT EMISSION

WHITE CIRCLE: LIGHT EMISSION

FIG. 29

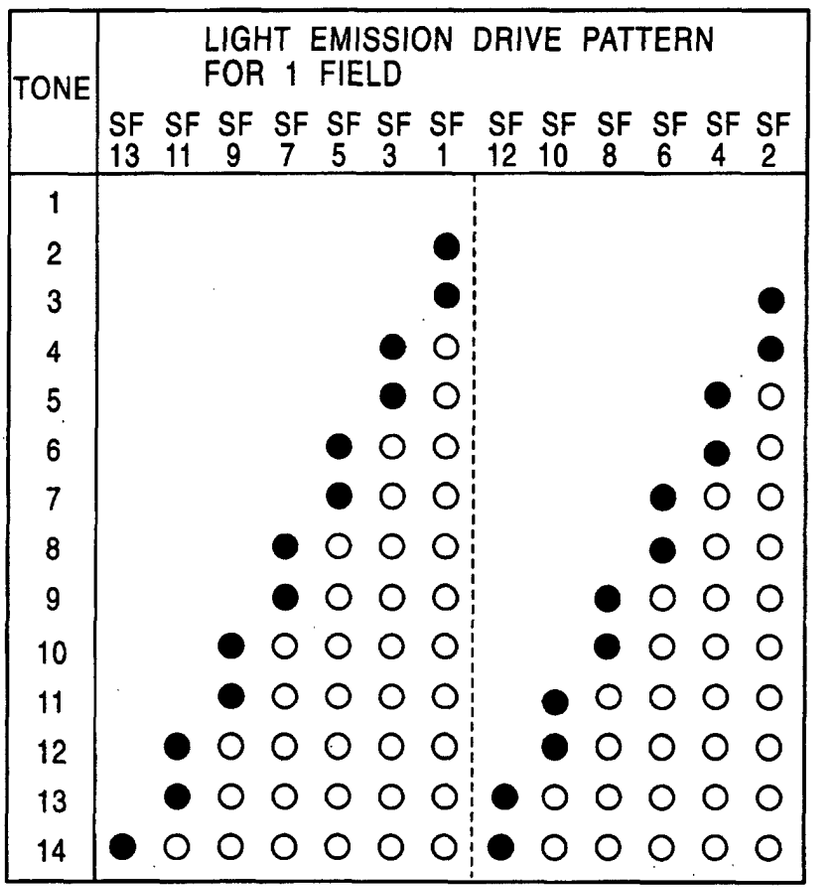
[SELECTIVE ERASURE]

TONE	LIGHT EMISSION DRIVE PATTERN FOR 1 FIELD												
	SF 1	SF 3	SF 5	SF 7	SF 9	SF 11	SF 13	SF 2	SF 4	SF 6	SF 8	SF 10	SF 12
1	●							●					
2	○	●						●					
3	○	●						○	●				
4	○	○	●					○	●				
5	○	○	●					○	○	●			
6	○	○	○	●				○	○	●			
7	○	○	○	●				○	○	○	●		
8	○	○	○	○	●			○	○	○	●		
9	○	○	○	○	●			○	○	○	○	●	
10	○	○	○	○	○	●		○	○	○	○	●	
11	○	○	○	○	○	●		○	○	○	○	○	●
12	○	○	○	○	○	○	●	○	○	○	○	○	●
13	○	○	○	○	○	○	●	○	○	○	○	○	○
14	○	○	○	○	○	○	○	○	○	○	○	○	○

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE
WHITE CIRCLE: LIGHT EMISSION

FIG. 30

[SELECTIVE WRITING]



BLACK CIRCLE: SELECTIVE WRITING DISCHARGE + LIGHT EMISSION

WHITE CIRCLE: LIGHT EMISSION