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(54) CONVERTER CIRCUITS

(71) We, DANFOSS A/S, a Danish Company of DK-6430 Nordborg, Denmark, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to converter circuits for operating asynchronous electric motors of adjustable rotary speed.

It is known to provide an converter circuit for an asynchronous motor, which circuit includes an inverter of which the output frequency is regulatable by a frequency regulator, and includes a D.C. supply having its voltage regulatable by a voltage regulator. It is known to provide a desired value input device for setting the output frequency, a voltage monitor and a current monitor, the three last-mentioned components each giving a respective output signal, namely a frequency input signal, a voltage measurement signal and a current measurement signal. It is known to provide a control circuit which processes these output signals to form input signals for the voltage regulator and the frequency regulator and which has a comparator which controls the voltage regulator.

In a known converter circuit of this kind, the operating point is set by means of a pctentiometer of which the tapped voltage is compared with a value approximately proportional to the D.C. supply voltage. The frequency is made to follow the supply voltage substantially proportionally. Since the slip and therefore the rotary speed varies with a change in the load of an asynchronous motor, provision is made for slip compensation which increases both the D.C. voltage supplied to the inverter and the inverter frequency with an increase in the current. In this way, the speed can be kept approximately constant in a certain operating range.

According to the invention, there is provided:

A converter circuit comprising an inverter settable to a desired output frequency for operating an asynchronous motor of which the rotary speed is adjustable, the inverter including a computation circuit arranged to calculate from the values of at least two of the parameters inverter current, inverter voltage and desired inverter frequency and at least one constant, a computed value for the inverter current or inverter voltage or inverter frequency which, together with the first-mentioned values, will operate an asynchronous motor supplied by the inverter at a substantially constant slip frequency, and means to adjust the inverter voltage either to make the actual value of the inverter current or inverter voltage substantially equal to its computed value or to make the computed inverter frequency substantially equal to the desired inverter frequency.

With this circuit a substantially constant slip frequency is obtained for the desired frequency value that is set. The inverter voltage is regulated so that this condition is maintained independently of the load. The result of this is that the nominal slip for a nominal load also occurs on partial load. This leads to the desired substantially constant speed. This slip frequency can be kept substantially constant even at low loads in that the air gap magnetisation is made substantially proportional to the rotor current, that is there is under-magnetisation. This has the further advantage that hunting is avoided of the kind occurring during slip compensation which corrects the frequency of the inverter whilst substantially maintaining the magnetisation level.

Even when switching off, no oscillation occurs between the motor and the inverter. The inverter can even be connected to the motor when the latter is already rotating, whereupon the motor changes its speed to that determined by the inverter without first having to come to a standstill.

It is further advantageous that for each load condition a minimum power is automatically set at which neither excessively high magnetic losses occur as a result of a high voltage nor excessively high copper losses occur as a result of an excessively high current. Instead, there will always be a state of equilibrium at which the current and voltage assume a virtually optimum value because they approach this state of equilibrium from opposite sides. If, for example, a motor is suddenly loaded more intensely, the current rises correspondingly because of the higher slip frequency. Consequently, the voltage is regulated to a higher value until the prescribed slip frequency is again reached. During this, however, the current drops, this setting a new state of equilibrium for the current and voltage.

It is also advantageous that no measurements need be undertaken at the motor itself; the measurement signals can be derived directly before and/or after the inverter.

The converter circuit can further comprise D.C. supply means including a voltage regulator, and a voltage sensor and a current sensor connected between the D.C. supply means and the inverter, the voltage and current sensors being connected to the computation circuit and the means to adjust the inverter voltage comprising the voltage regulator.

The D.C. supply means can comprise a rectifier circuit.

Preferably, the computation circuit comprises a computation element with which, in use, a value taking the slip frequency into account is introduced and is held constant below the nominal rotary speed at least over the major part of the motor operating range. Since the set slip frequency applies not only to a particular set frequency but also to the main operating range of the motor, one obtains a correspondingly simple lay-out for the computation circuit.

The computation circuit can calculate the computed value by using the equation

$$f = \frac{1}{k_1}\left(\frac{E}{I} - k_2\right)$$

where
f is the desired inverter frequency,
E is the inverter voltage,
I is the inverter current,
k_1 is a (or the) value taking the slip frequency into account, and
k_2 is the said at least one constant and corresponds to the winding resistance of the stator of the said motor.

Use of the above equation (or an adapted form thereof) allows a particularly simple computation circuit to be utilised.

The computation circuit can comprise a division circuit connected to receive the value of inverter voltage as the dividend and the value of inverter current as the divisor, and a subtraction circuit in which a fixed value is subtracted from the quotient. In this case, the computed value can be calculated substantially according to the equation

$$f' = \frac{1}{k_1}\left(\frac{E}{I} - k_2\right)$$

Alternatively, the computation circuit can comprise a subtraction circuit arranged to subtract a voltage-proportional value from the value of inverter voltage, and a division circuit connected to receive the output value of the subtraction circuit as the dividend and the value of inverter current as the divisor. In this case, the calculation of the computed value for inverter frequency f' can occur substantially according to the equation

$$f' = \frac{E - I \cdot k_2}{I \cdot k_1}$$

Alternatively, the computation circuit can comprise an addition circuit to add a value proportional to the value of desired inverter frequency to the said at least one constant, and a division circuit connected to receive the value of inverter voltage as the dividend and the output value of the addition circuit as the divisor. In this case, calculation of the computed value of inverter current I' can take place substantially according to the equation

$$I' = \frac{E}{f \cdot k_1 + k_2}$$

Alternatively, the computation circuit can comprise a subtraction circuit to subtract a current-proportional value from the value of inverter voltage, and a division circuit connected to receive the output value of the subtraction circuit as the dividend and the value of desired inverter frequency as the divisor. In this case, the calculation of the computed value of inverter current I' can take place substantially according to the equation

$$I' = \frac{E - I \cdot k_2}{f \cdot k_1}$$

If the division circuit is not itself adapted to introduce the factor $1/k_1$, a computation element introducing the factor $1/k_1$ can be connected before the dividend input or after the output of the division circuit.

Alternatively, the computation circuit can comprise a multiplication circuit arranged to receive the value of desired inverter frequency and the value of inverter current, one of which is multiplied by a (or the) value taking slip frequency into account, and an addition circuit in which the multiplication result is added to the value of inverter current multiplied by the said at least one constant. In this case, calculation of the computed value of inverter voltage E′ can be effected substantially according to the equation

$$E' = (f \cdot k_1 + k_2) \qquad \text{I}$$

Preferably the said at least one constant and/or the value taking the slip frequency into account can be adjustably set. For example to enable adaptation to a particular motor.

Where the computation circuit is arranged to make use of a value taking the slip frequency into account, that value can depend on at least one of the three parameters. For example in order also to enable the operating range to be extended to frequencies above the nominal motor frequency.

The inverter can include a frequency generator arranged to be controlled by the setting of desired inverter frequency. Alternatively, the inverter can include a frequency generator arranged to be controlled by the computed value of inverter frequency. This control by the computed value of inverter frequency is possible because the computed frequency is made to follow the desired inverter frequency during operation.

It is advisable to provide a minimum current generator to hold the value of inverter current supplied to the computation circuit at a predetermined minimum value for small values of actual inverter current. This ensures that the computation circuit will also operate reliably at zero torque or near zero torque without indefinite conditions occurring as a result, because an inverter voltage value near zero and an inverter current value near zero have to be divided by one another.

The means to adjust the inverter voltage can comprise a first comparator and it is also favourable if the output of the first comparator is connected to the output of a second comparator arranged to compare an adjustable maximum power value with the product of a factor corresponding approximately to the value of inverter current and a factor corresponding approximately to the value of inverter voltage and to override the first comparator when the product exceeds the maximum power value. Desirably, the maximum power value is set to the nominal power of the connected motor. If such a high load torque occurs at a prescribed frequency that the maximum power is exceeded, the second comparator ensures that the inverter frequency is reduced relative to the desired inverter frequency to such an extent that the load torque can be overcome with the nominal power. In the torque-frequency diagram, this gives a power hyperbola which limits the range in which the motor can be operated without overloading.

Further, it is favourable if the output of the first comparator is connected to the output of a further comparator arranged to compare an adjustable maximum torque value with a comparative value corresponding to inverter current and to override the first comparator when the comparative value exceeds the maximum torque value. The said further comparator ensures that a prescribed maximum current is not exceeded in the motor whereby the maximum torque is also determined because the torque is substantially proportional to the square of the motor current.

Further, the computation circuit can comprise a computation element arranged to introduce a factor proportional to slip frequency and hold it constant up to about nominal motor frequency, and a switch element arranged to increase this factor above the nominal frequency. In this way it is possible to extend the advantageous properties of the converter circuit to an operating range that extends beyond the nominal motor frequency even though the D.C. supply voltage is limited to a certain maximum value, generally the nominal motor voltage. If the slip frequency to be held constant increases with an increase in inverter frequency, it is possible to keep the motor speed substantially constant independently of the load torque without increasing the voltage that has to be applied.

The switch element can in particular be mechanically coupled to a setting device to set desired inverter frequency. This ensures that the slip frequency and the desired inverter frequency are changed simultaneously.

For example, the switch element can be arranged to control a division circuit in series with a computation element in the form of an amplifier, a signal dependent on the desired inverter frequency being fed, in use, as the divisor to the division circuit.

Another possibility is for the switch element to be arranged to adjust a feedback resistor of a computation element in the form of an amplifier with negative feedback, the feedback resistor being adjusted in dependence on desired inverter frequency.

In this case, the factor may double between the simple and double nominal frequency and substantially remain at this double value on a further rise in frequency.

The computation circuit can comprise a computation element arranged to introduce a factor proportional to the slip frequency and hold it constant in the operating range up to just below nominal voltage, and a switch element which increases this factor above this voltage limiting value. In this way, the manner of operation of the converter circuit remains unchanged in the entire operating range of the motor, even at frequencies exceeding the nominal frequency. Correction of the slip is undertaken only in the upper range of the available voltage.

In particular, the switch element can be controlled by a control signal which is equal to the value of inverter voltage reduced by a current-proportional value, and the voltage limiting value can correspond to about 90 to 95% of the nominal motor voltage. The limiting value of the voltage is thus determined by a prescribed percentage of the magnetising voltage.

A particularly simple embodiment for this is obtained if the computation element is an amplifier disposed between the subtraction circuit and division circuit and the switch element alters its degree of amplification and is controlled by the input signal of the amplifier.

It is advisable if the factor approximately doubles continuously between the limiting value and a value corresponding to the nominal voltage. In this way one ensures proper operation at which there is not yet a reduction below the pull-out point.

In some cases it is also desirable to bring other influences into play by correcting the input frequency signal.

For example, the output of an input device to set the desired inverter frequency can be connected to the output of a comparator arranged to compare an adjustable maximum current value with the value of inverter current and to reduce the desired inverter frequency value relative to the value set when the inverter current value exceeds the maximum current. By means of this feature one can likewise prevent the maximum motor current from being exceeded. The last-mentioned comparator therefore corresponds to the above-mentioned further comparator. In this way one also prevents the pull-out torque of the motor from being exceeded on overload because the frequency is necessarily reduced.

The output of an input device to set the desired inverter frequency can be connected to the output of a comparator which compares an adjustable maximum voltage with the inverter voltage value and increases the desired inverter frequency value relative to the value set when the inverter voltage exceeds the maximum voltage. This prevents a prescribed maximum voltage from being exceeded at the motor because the frequency is necessarily increased. This is advantageous for an intensive delay at full speed.

Preferably, the output of an input device to set the desired input frequency is connected to the output of a limiting value circuit arranged to change, when the difference between one of the parameter values and the associated computed value exceeds a predetermined limiting value, the desired inverter frequency value relative to the set value in the sense of a reduction of the difference. The limiting value circuit functions only during a dynamic operating situation when, on starting or changes in torque, strong accelerations or retardations occur. On excessively high acceleration, the motor slip can increase to such an extent that the pull-out torque is reached. On excessively high retardation, the motor can produce such high voltages that the inverter can be impaired. By correcting the desired inverter frequency value, the limiting value circuit ensures that these effects do not arise.

For example, where the means to adjust the inverter voltage comprises a first comparator the limiting value circuit can be preceded by a subtraction circuit fed with the two quantities to be compared in the first comparator. The subtraction result is a measure of the difference that could lead to disruptions. Another possibility is for a second computation circuit to be provided which computes a computed inverter frequency value from the value of inverter voltage and the value of inverter current, and for the limiting value circuit to be preceded by a subtraction circuit fed with the desired inverter frequency value and the computed inverter frequency value.

The limiting value circuit can simply comprise two diodes, particularly Zener diodes, connected in anti-parallel.

The desired inverter frequency value can be set by means of a simple potentiometer. However, it can also be introduced as a series of pulses and fed to the computation circuit by way of a digital/analogue converter. This is often desirable because the pulses can be used either directly or by simple division as control pulses for the inverter.

The desired inverter frequency value can also be fed to the division circuit as a series of pulses, the division circuit comprising an integrator which integrates the voltage measurement signal between two successive pulses, and a storage device can store each last integration result. Since the pulse spacing is inversely proportional to the frequency, the integration result corresponds to the desired quotient.

In many cases it is desirable that the inverter voltage value be obtained from the voltage on the output side of the inverter between two phases and the pulses correspond to the frequency of the inverter. Since halfwaves are supplied through the output side, each integration occurs during one half wave. In the meantime, until the next half-wave occurs, the integration result can be fed to the storage device and the contents of the integrator can be expunged.

It is also favourable if the inverter current value is obtained from an amplifier with adjustable degree of amplification and giving a current measurement signal. In this way, an adaptation to motors of different power can be readily effected.

Further, the inverter current value can be fed to the computation circuit by way of a timing network, particularly an RC network. This prevents a disruptive feedback effect on the computed value, particularly the frequency of the inverter, from occurring when there is a certain amount of waviness in the current fed to the inverter.

In order that there is no drop below the pull-out torque of the motor, it is desirable to provide a limiting circuit which limits the slip frequency to about twice the nominal slip frequency. This can, for example, be effected in that a limiting circuit is applied in the path of a signal relating to inverter frequency, particularly the desired inverter frequency value. If the frequency of the inverter and the permissible torque have an upper limit, the slip frequency is indirectly limited.

Advantageously, the inverter voltage value is fed by way of a band-pass filter of which the output signal is fed in the same sense as the inverter current value to the third comparator. This counteracts fluctuations in the inverter voltage that might lead to hunting during operation.

It is particularly advantageous to provide a slip-compensating signal generator which delivers a slip compensating signal which is zero up to about the nominal frequency of the inverter and above this has a value increasing with the frequency. In particular, the slip compensating signal generator can be controlled by the same input value as is a computation element determining a factor proportional to the slip frequency. Whenever this factor and thus the slip is changed, slip compensation will occur.

In particular, an addition circuit may be provided in which a first slip compensating signal is added to a signal relating to inverter frequency, for example, the desired inverter frequency value. In this way the effective frequency is increased with a rise in slip frequency so that the motor speed remains substantially constant.

Another possibility is an addition circuit in which a second slip compensating signal is added to the adjustable torque value fed to said further comparator. Whenever the slip frequency has to be increased at higher frequencies of the inverter, the effective torque will in this way also be increased, which permits the torque to be kept constant over a still larger range of speed.

In this connection it is desirable if the second slip compensating signal is fed by way of an amplifier of which the degree of amplification can assume at least two stages depending on the adjustable torque value, the higher stage being associated with a higher torque. This serves for adaptation to the non-linear curves in the operating diagram. In the extreme case, the degree of amplification can be changed continuously.

It is preferred that where the means to adjust the inverter voltage comprises a first comparator, the output of the first comparator is connected to another comparator arranged to compare an adjustable maximum current value with the value of inverter current and to override the first comparator when the inverter current exceeds the maximum current value. In this way one can avoid overloading of the inverter when the maximum torque fed to the said further comparator is increased by variable additive components relative to the set value.

Converter circuits constructed in accordance with the invention will now be described by way of example only with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a converter circuit according to the invention;

Figs. 2 to 4 are block diagrams of three alternative control circuits for use in the converter circuit of Fig. 1;

Figs. 5 to 10 are respective detailed representations of six exemplary control circuits;

Fig. 11 is the operating diagram of a switchable amplifier;

Fig. 12 is the operating diagram of a minimum current generator;

Fig. 13 is the torque-frequency diagram of the circuit according to Fig. 6, which also applies to Figs. 7 to 9;

Fig. 14 is the same diagram but for the circuit according to Figs. 5 or 10;

Fig. 15 is a circuit diagram corresponding to Fig. 6, which contains additional circuit components and is represented as functional blocks;

Fig. 16 is a diagram corresponding to Fig. 13.

A generalised description will be given before the drawings are referred to in detail.

The circuits shown in the accompanying drawings comprise converter circuits which permit motor speed to be kept constant over a larger operating range and with increased accuracy.

Each converter circuit comprises an inverter settable to a desired output frequency for operating an asynchronous motor of which the rotary speed is adjustable, the inverter including a computation circuit which, from the values at least two of the parameters inverter current, inverter voltage and desired inverter frequency and at least one constant calculates a computed value for the inverter current or inverter voltage or inverter frequency which, together with the first-mentioned values, will operate an asynchronous motor supplied by the inverter at a substantially constant slip frequency, and means to adjust the inverter voltage either to make the actual value of the inverter current or inverter voltage substantially equal to its computed value or to make the computed inverter frequency substantially equal to the desired inverter frequency.

In order that the slip or rotor frequency can be kept constant independently of the load at a set frequency, the formula

$$I_2/B = f_2 \,.\, \text{constant} \qquad (1)$$

applies, wherein I_2 is the active current in the rotor of the motor, B is the air gap induction and f_2 is the slip frequency. It is possible, with an adequate degree of accuracy, to replace the effective rotor current I_2 with the stator current I_1 which can, for example, be measured on the D.C. side in front of the inverter. The air gap induction can, with sufficiently high accuracy, be represented by

$$\frac{U_1 - I_1 \,.\, R_1}{f_1} \,.\, \text{constant} \qquad (2)$$

wherein U_1 is the voltage applied to the motor, I_1 is the active current supplied to the motor, R_1 is the ohmic resistance of the stator coil and f_1 is the frequency of the inverter. The voltage U_1 can be derived before or after the inverter. From (1) and (2), one obtains

$$\frac{I_1}{U_1 - I_1 \,.\, R_1} = \frac{f_2}{f_1} \,.\, \text{constant} \qquad (3)$$

which shows that, if the slip frequency f_2 is kept constant, a relatively simple relationship exists between the three values I_1, U_1 and f_1. If one introduces the primary active current I_1 as measured inverter current signal I, the primary voltage U_1 as measured inverter voltage E and the inverter frequency f_1 as the set desired inverter frequency f, then a computed value can be calculated in the computation circuit from at least two of the stated three parameter values E, I and f.

A particularly simple computation circuit is thus obtained if it calculates the computed value according to the equation

$$f = \frac{1}{k_1}\left(\frac{E}{I} - k_2\right) \qquad (4)$$

or an adaptation thereof.

In a first embodiment, the computed value is calculated substantially according to the equation

$$f' = \frac{1}{k_1}\left(\frac{E}{I} - k_2\right) \qquad (5)$$

In a second embodiment, the calculation of the computed value of inverter frequency f′ occurs substantially according to the equation

$$f' = \frac{E - I \,.\, k_2}{I \,.\, k_1} \qquad (6)$$

In a third embodiment, calculation of the computed value of inverter current I′ takes place substantially according to the equation

$$I' = \frac{E}{f \,.\, k_1 + k_2} \qquad (7)$$

In a fourth embodiment, the calculation of the computed value of inverter current I′ takes place substantially according to the equation

$$I' = \frac{E - I \,.\, k_2}{f \,.\, k_1} \qquad (8)$$

In a fifth embodiment, calculation of the computed value of inverter voltage E′ is effected substantially according to the equation

$$E' = (f \,.\, k_1 + k_2) \quad I \qquad (9)$$

Referring to Fig. 1, reference 1 represents the three-phase A.C. mains connected to a regulated-output rectifier circuit 2. The rectifier circuit 2 is connected by two D.C.

lines 3 and 4 to an inverter 5 having three output lines 6 are connected to an asynchronous motor 7. The output voltage U_1 of the rectifier 2 is regulatable with the aid of a voltage regulator 8 which, with the aid of a voltage regulating signal Su, controls for example a chopping circuit. The regulated D.C. voltage U_1 is measured by a voltage measuring device 9 that delivers a voltage measurement signal E. The direct current I_1 between rectifier circuit and inverter is measured by a current measurement device 10 which delivers a current measurement signal I.

The frequency of the inverter 5 is regulatable by means of a frequency regulator 11 which feeds a frequency regulating signal Sf to the inverter. In addition, there is a desired value setting device 12 which delivers a desired inverter frequency input signal f. In a control circuit 13, the three output values E, I and f are processed in such a way that the voltage regulating signal Su and the frequency regulating signal Sf operate the circuit so that the motor 7 has a constant slip or rotor frequency f_2.

Fig. 2 shows one form the control circuit 13 may take, namely a comparator 14 and a computation circuit 15. In the computation circuit 15, a computed value f′ of the frequency is calculated according to the equation (6) from the current measurement signal I and the voltage measurement signal E as well as two constants k_1 and k_2, the computed value being compared with the input frequency f in the comparator 14. The voltage regulating signal Su and thus the D.C. voltage U_1 are changed until the two values f and f′ are equal. Regardless of the load torque, this leads to a substantially constant slip or rotor frequency f_2 of the motor 7 and thus to a substantially constant speed. The constant k_1 is inversely proportional to the slip frequency f_2 and the constant k_2 is proportional to the winding resistance of the stator of the motor.

Fig. 3 shows a second form the control circuit 13 may take, namely a comparator 114 and a computation circuit 115. The latter calculates a computed value I′ of the current according to equation (7) from the voltage measurement value E and the frequency input value f, the computed value being compared with the current measurement value in the comparator 114. The voltage regulating signal Su is regulated until the values I and I′ are equal. This likewise leads to the desired substantially constant slip frequency.

Fig. 4 shows a third form the control circuit 13 may take, namely a comparator 214 and a computation circuit 215. The latter calculates a computed value E′ of the voltage according to equation (9) from the current measurement value I and the frequency input value f, the computed value being compared with the voltage measurement value E in the comparator 214. The voltage regulating signal Su is changed until the values E and E′ are equal. This likewise leads to the desired constant slip frequency.

Fig. 5 shows a practical realisation of the control circuit of Fig. 2. The desired value input device 12 comprises a potentiometer 16 of which the tapping 17 is connected by way of a first summating resistor 18 to the inverting input of an amplifier 19. In addition, the inverting input is fed with the computed value f′ by way of a summating resistor 20. The output of the amplifier 19 is connected to the voltage regulator 8 by way of a diode 21.

The computation circuit 15 comprises a subtraction circuit 22 to which the voltage measurement signal E is fed in the positive sense and the value k_2. I is fed in the negative sense by way of a multiplication element 23, for example and as shown, an amplifier. The subtraction result is fed to the dividend input 24 of a division circuit 25. The divisor input 26 is fed with the current measurement signal I by way of a diode 27. However, the input is additionally connected to the tapping of a potentiometer 29 by way of a second diode 28. The potentiometer forms a minimum current generator 30 which ensures that the divisor in the division circuit 25 does not become zero at low current measurement signals I. The quotient is fed by way of a resistor 31 to a computation element 32, for example and as shown, an amplifier, in which the quotient is multiplied by the factor $1/k_1$. This gives the computed value f′.

The factor $1/k_1$ is variable with the aid of a switch device 33. The latter consists of a special potentiometer 34 in a feedback circuit of the amplifier 32 formed by resistors 35 and 36. The tapping 37 of the potentiometer 34 is mechanically coupled to the tapping 17 of the desired value input device 12. On a change in the input frequency up to the value 1 (corresponding to the nominal frequency of the connected motor), the slip frequency will not alter. Between the single and double value of the nominal frequency, the slip frequency will change from the single to the double value and upon a further increase in the input frequency the slip frequency will remain at the double value.

Fig. 6 shows another practical realisation of the control circuit 13 and differs from that of Fig. 5 substantially in that instead of the computation element 32 for the factor $1/k_1$ there is connected in front of the dividend input 24 a computation element 38. The amplification factor of this computation element can be switched by a switch element 38′ depending on its input voltage, so that, on exceeding a limiting value of the magnetising voltage, the slip frequency f_2 will gradually increase from the single to a double value as will hereinafter be described in conjunction with Fig. 11. There is also a comparator 39. The latter comprises an amplifier 40 fed with a maximum power value N_{max} by way of a summating resistor 41 from an adjustable potentiometer 42 and with the instantaneous power by way of a summating resistor 43. The instantaneous power is obtained as the output of a multiplication circuit 44 fed with the voltage measurement value E and the current measurement value I. The output of the amplifier 40 is applied to the voltage regulator 8 by way of a diode 45. As soon as the set value N_{max} has been reached, this comparator takes over the voltage control of the inverter circuit.

A further comparator 46 comprises an amplifier 47 fed with a maximum torque value M_{max} by way of a summating resistor 48 from an adjustable potentiometer 49 and with the current measurement value I by way of a second summating resistor 50. The output of the amplifier 47 is connected to the voltage regulator 8 by way of a diode 51. As soon as the value M_{max} has been exceeded, voltage control of the inverter circuit takes place by way of this comparator 46.

Fig. 7 shows another practical realisation of the computation circuit 15. The rest of the circuit can be like that of Fig. 5 or Fig. 6 and a division circuit 25 and minimum current generator 30 are again employed. The division circuit 25 is, by way of a computation element 52, fed at the dividend input 24 with a voltage measurement value E which is related to the factor $1/k_1$. The current measurement value reaches the divisor input 26 and can be corrected by means of the minimum current generator 30. The quotient is fed to a subtraction circuit 53 in which a value k_2/k_1 is subtracted which is adjustable at a potentiometer 54. With this computer circuit, the computed value f′ is calculated according to equation (5).

Fig. 8 shows a practical realisation of the control circuit of Fig. 3. The desired value input device feeds the input frequency f′ in the form of a series of pulses. These pulses act directly on the frequency regulator 11. A digital/analogue converter 116 converts the signal to an analogue voltage. By way of a computation element 117 in which the product $k_1 . f$ is formed, the analogue voltage is fed to a summating circuit 118 in which the product has the constant k_2 added to it that is derivable from a potentiometer 119. The result of the addition is fed to the divisor input 120 of a division circuit 121 of which the dividend input 123 is supplied with the voltage measurement value E. One thereby obtains the computed value I′. The latter is fed by way of a summating resistor 124 to the inverting input of an amplifier 123 constituting the comparator 114. This input is additionally fed by way of a summating resistor 124′ with the current measurement signal I which can be corrected with the aid of a minimum current generator 30. This circuit gives a substantially constant slip frequency according to equation (7).

The two values I and I′ to be compared are additionally fed to a subtraction circuit 125. The difference influences a limiting value circuit which consists of two Zener diodes connected in anti-parallel and therefore gives no output signals at small differences but at large differences gives a comparatively large output signal to an addition circuit 128 by way of a resistor 127. In the addition circuit, the frequency input signal f is corrected in a manner such that on excessive acceleration or excessive retardation, the frequency signal fed to the computation circuit is corrected in the sense of a smaller departure from the frequency of the motor calculated from the measured values.

A comparator 129 comprises an amplifier 130 of which the inverting input is fed with a maximum current value I_{max} from a potentiometer 132 by way of a summating resistor 131 and the current measurement value I by way of a summating resistor 133. The amplifier output 130 is likewise connected to the input of the addition element 128 by way of a diode 134 and a resistor 135. When the set value I_{max} is exceeded, a correcting signal is obtained with which the frequency fed to the computer circuit is reduced relatively to the set desired value f.

A further comparator 136 comprises an amplifier 137 of which the inverting input is fed with a maximum voltage value U_{max} from an adjustable potentiometer 139 by way of a summating resistor 138 and with the voltage measurement value E by way of a second summating resistor 140. The amplifier output is likewise connected to the one input of the addition circuit 128 by way of a diode 141, which is oppositely poled to the diode 134, and a resistor 142. When a maximum voltage U_{max} is exceeded, the frequency input signal is corrected in a manner such that the frequency fed to the computation circuit is increased.

Fig. 9 illustrates a computation circuit 115 to implement equation (8). In it the current measurement signal I is provided with the factor k_2 in a computation element 143. This product is fed to the minus input of a subtraction circuit 144 of which the plus input is supplied with the voltage measurement signal E. The result of subtraction is fed to the dividend input 145 of a division circuit 146 of which the divisor input 147 is fed with the frequency input signal f. The quotient is related to the factor $1/k_1$ in a computation element 148. This gives the computed quantity I′ which is compared with the current measurement value I in the comparator 114.

Because of the supply of the frequency input signal f as a series of pulses, the division circuit 146 is designed so that an integrator 149 integrates the signal at the input 145 between two successive pulses that are fed by way of the input 147. The result of integration is in each case transmitted to a storage device 150 so that it is also available during the course of integration. Simultaneously, or immediately after transmission to the storage device, the integrator is returned to zero.

Fig. 10 shows a practical realisation of the circuit of Fig. 4 and implements equation (9).

The computation circuit 215 comprises a multiplication circuit 216 of which the one input 217 is fed with the frequency input value from a potentiometer 218 by way of a resistor 219 and the other input 220 is fed by way of a computation element 221, in which the current measurement value is related to the factor k_1, with the current measurement value I corrected by the minimum current generator 30. The product is fed to one input of an addition circuit 222 of which the other input is connected to the output of a computation element 223 supplied with the current measurement value I, so that this input is fed with the product $I \cdot k_2$. The summation result corresponds to the computed value E′ of the voltage. This is fed to the inverting input of an amplifier 225 of the comparator 214 by way of a summating resistor 224. The same input is fed with the voltage measurement signal E by way of a summating resistor 226. The output of the amplifier controls the voltage regulator 8 by way of a diode 227.

The computation element 221 is preceded by a division circuit 228 of which the dividend input 229 is fed with the current measurement value I. Normally the value 1 exists at the divisor input 230, this value being tapped from a voltage divider consisting of a fixed resistor 231 and a special potentiometer 232. The tappings 233 of the desired value setting device and 234 of the special potentiometer 232 are mechanically intercoupled in the following manner. When the frequency input value lies between zero and the nominal motor frequency, the divisor has the value 1. Between the single and double nominal frequency, the divisor increases from 1 to 2. Above double the nominal frequency, the divisor remains at the value 2. In function, this corresponds to the Fig. 5 arrangement.

In addition a second computation circuit 235 is provided. In a subtraction circuit 236, the product $I \cdot k_2$ is subtracted from the voltage measurement value E. The subtraction result is fed to the dividend input 237 of a division circuit 238 of which the divisor input 239 is fed with the product $I \cdot k_1$. One therefore obtains at the output a computed value f″ which is calculated according to the equation

$$f'' = \frac{E - I \cdot k_2}{I \cdot k_1} \qquad (10)$$

This equation corresponds to equation (6). This computed value f″ is compared with the frequency input value f in a subtraction circuit 240. The difference serves as the input signal for a limiting value circuit 241 corresponding to the limiting value circuit 126. Its output value is fed by way of a resistor 242 to an addition circuit 243 so that the frequency input value f can be corrected when the frequency f″ calculated from the measured values shows an excessively large difference from the frequency f that is actually introduced.

Fig. 11 shows the operating curve of the computation element 38 designed as an amplifier. Its input value $E - I \cdot k_2$ corresponds to the magnetising voltage. Since at higher motor frequencies and constant slip frequency this magnetising voltage goes beyond the maximum voltage available at the inverter input, this constant slip frequency is maintained only up to just below the nominal voltage (limiting value G) represented by 100% E_{max}. Thereafter, there is a correction such that the input value 100% E_{max} also corresponds to the output value 100% E_{max}, which causes a change in the slip frequency in this upper voltage range.

The operation of the minimum current generator 30 is shown in Fig. 12. When the current measurement value I and thus the active motor current I_1 approaches zero on the line A, the minimum current generator 30 takes over the generation of signals along the line B. The value I_{korr} that is effective in the computation circuit can therefore never drop below a predetermined value, for example 22%, which corresponds approximately to a minimum torque of 5%.

Fig. 13 is the torque-frequency operating diagram of an inverter circuit according to Fig. 6. The operating range extends over a frequency of 0 to 300% of the nominal motor voltage f_{1nenn}. The minimum current generator 30 is effective in the entire operating range. For this reason the range C is inoperative for the regulation. Between zero and about 100% of the nominal frequency, the torque is limited only by the horizontal M=100%. This takes place as a result of setting the potentiometer 49. For each operating point lying between the line M=100% and the region C, a constant motor speed is obtained for each desired torque that is determined by the input frequency f and the slip frequency selected by means of the factor $1/k_1$. In the frequency range between 100 and 200%, these conditions can be maintained up to the line f_2=100%. For a higher torque, there is a higher magnetising voltage which leads to switching over of the regulating element 38 corresponding to Fig. 11. The result of this is that at higher torques the slip frequency gradually increases to double the value. The upper limit that is here effective is the maximum power N_{max} which was set by the potentiometer 42 and which leads to a hyperbola N=100%. The motor can even be operated in the frequency range from about 200 to 300%, the same conditions as before being applicable. Only the upper limit is prescribed by the line f_2=200% because on a further increase in the slip frequency one would fall below the pull-out point. From all of this it will be evident that with the aid of the inverter circuit a motor can be operated independently of the torque at a constant rotary speed over an extraordinarily large frequency range and an extraordinarily large torque range and that even at higher frequencies operation will still be possible in the region E if one permits a twofold increase in the slip frequency.

In the diagram according to Fig. 14, which may for example correspond to the embodiment of Fig. 5, the upper limits are the same as in the Fig. 13 diagram. By reason of the potentiometer 34 mechanically coupled to the frequency input potentiometer 16, however, one obtains different conditions below the upper limiting curves. Up to the nominal frequency, there are no differences. In the frequency range from about 100 to 200%, the slip frequency increases in proportion to the frequency increase. Between 200 and 300%, the twofold slip frequency is constant. Since each frequency input signal f is associated with a substantially constant slip frequency f_2, no departures from the set speed occur for any of the permissible torques.

Extraordinarily high accuracies can be achieved at substantially constant rotary speed with the aid of the illustrated inverter circuits. With a conventional asynchronous motor, one can in this way keep every set speed substantially constant up to 10% of the maximum speed within a tolerance of ±0.5% within the entire load range from zero up to full load torque.

Still higher requirements can be met with the circuit according to Fig. 15 which is similar to Fig. 6 and in which the same reference numerals are used but which contains still further circuit components. For better illustration, some of the circuit components are shown as function blocks in each of which the input signal is entered on the abscissa and the output signal on the ordinate in a coordinate representation.

The path of the current measurement signal I contains an amplifier 55 with a variable amplification factor A. This permits motors of different size to be connected to the same inverter circuit even though the inverter circuit itself is designed for only one particular motor size.

If a motor is connected which has a lower nominal power than the nominal power of the inverter circuit, the full load current of the smaller motor would correspond to a partial load current of the larger motor. Consequently the smaller motor would be undermagnetised at full load and would also have insufficient magnetisation at every partial load. This would result in an undesirable higher slip frequency and make it possible for the pull-out torque of the motor to be exceeded. All these disadvantages can be avoided in a simple manner by increasing the amplification factor A in the amplifier 55. If, for example, a motor with half the nominal power is connected, the amplification factor A need merely be doubled. All the operations in the inverter circuit will then be performed at half the motor current.

The current measurement signal is fed to the computation circuit 15 by way of a time network 56, particularly an RC (resistance-capacitance) network. The time constant of this network, which may for example amount to 0.2 seconds ensures that a certain amount of ripple in the inverter current will not have any effects in the computation circuit 15. In particular, the frequency of the inverter will not change under the influence of this current ripple. This time constant also influences the speed with which the inverter circuit moves to a new operating point. However, the time constant can readily be selected so that the influence of the current ripple is suppressed but the approach to a new operating point proceeds sufficiently rapidly.

The voltage measurement value E is fed not only to the computation circuit 15 but also to a band-pass filter 57 which is impenetrable for D.C. voltage but allows an A.C. voltage component to pass to a larger or less extent depending on its frequency. This A.C. voltage component forms the output signal of the band-pass filter 57 and is fed in a combining stage 58 to the comparator 46 in the same sense as the current measurement signal I. The band-pass filter is desirably tuned to the resonant frequency of the filter circuit that is conventional for a regulatable rectifier 2. In this way one avoids hunting of the connected motor such as that occurring on a sudden load change with torque control. This hunting becomes noticeable because of the voltage changes. The A.C. voltage component acts as a feedback.

Since with this regulation the maximum motor current must not be exceeded, a further comparator 59 is provided of which the output is connected by way of a diode 60 to the outputs of the other comparators 14, 39 and 46. This comparator has a subtraction circuit 61 which is fed on the one hand with the current measurement signal I and on the other hand from a voltage divider 62 with a fixed reference signal as the highest permissible current value I_{max}. This comparator 59 therefore takes over the control of the voltage regulation signal Su as soon as the maximum current has been exceeded. The slip frequency of the motor must not, even under extreme conditions, become so large that one falls below the pull-out torque. This generally occurs when the actual slip frequency is larger than three times the nominal slip frequency. Since non-linear conditions obtain between the slip frequency and torque, which can be taken into account in the computer circuit with only very large expense, it is recommended that the slip frequency be limited to about twice the nominal slip frequency. This can for example be effected by a corresponding design of the switchable amplifier 38, 38′.

In the present circuit, however, there is indirect limiting by the limiting circuit 63 which prevents the frequency input signal f from exceeding a predetermined limiting value. If a maximum frequency has on the one hand been set by the circuit 63 and the maximum load has on the other hand been set by the comparator 59, then, conversely, the slip frequency can also not exceed a predetermined limiting value.

This also applies even if additional slip compensation is provided for. A slip compensation signal generator 64 is influenced by the same input quantity as the switchable amplifier 38, namely the value $E-I \cdot k_2$. With reference to Fig. 11, it will be recalled that at a limiting value G in the switchable amplifier 38 there is a change in the factor $1/k_1$. Up to this limiting value G, the slip compensation generator 64 gives a slip compensation signal Sk=0. On exceeding this limiting value G, the signal Sk increases continuously. The signal Sk is therefore effective only if the factor $1/k_1$ responsible for the slip frequency is increased, for example doubled. A first slip compensating signal Sk1 is tapped at a potentiometer 65 and superimposed on the frequency input signal f in a combining stage 66 of an addition circuit. The result of this is that the frequency of the inverter is continuously increased when the slip frequency is reduced by means of the amplifier 38. Consequently, one obtains a high speed constancy. A second slip compensating signal Sk2, which may be identical with the slip compensating signal Sk, is fed to an amplifier 67 which has two amplifier characteristic lines I and II. At low values of the maximum torque value M_{max} set at the potentiometer 49, the characteristic line I applies whereas at higher torque values the line II applies. The output value is added to the maximum torque value in an addition circuit 68. As a result, whenever a maximum torque value was set that was not equal to the highest permissible load, the set maximum torque can be kept substantially constant over a larger speed range, as will be explained in conjunction with Fig. 16.

As in Fig. 13, the torque M is applied by way of the inverter frequency fl in Fig. 16. Three different operating conditions are examined in which the maximum torque was set to 100, 75 and 50%. This corresponds to currents I of 100, 87 and 71%. Above the nominal frequency, the power hyperbolas N of 100, 87 and 71% correspond to these curves. It will be seen that at a torque setting below 100%, the torque above a predetermined frequency f1 drops even though there is torque in reserve. This reserve torque is utilised by the slip compensating signal Sk2 being superimposed on the set torque value M, this superimposition proceeding in the same sequence as the increase in the slip frequency f2. By means of this superimpositioning, one obtains the extended straight torque lines M′ and M″ from which it is seen that for example a set torque M of 50% can be maintained up to twice the nominal frequency. It should be noted that at higher torques which intersect the power hyperbola at steeper sections, larger additions of slip compensation are necessary than at smaller torques. This is taken into account by the two amplifier characteristic lines I and II of the amplifier 67. It will be clear that a higher accuracy can be achieved if the degree of amplification is changed continuously with the set torque M_{max}. The limit at an inverter frequency of 200% fl_{nenn} is the effect of the limiting circuit 63. The illustrated circuits are merely examples. The computation circuits can be realised in different ways. For example, instead of the division circuits one may use multiplication circuits at which the divisor is supplied as the reciprocal value. Instead of feeding the one output value direct to the comparator, one can also process it in the computer circuit and then compare two intermediate results with one another.

WHAT WE CLAIM IS:—

1. A converter circuit comprising an inverter settable to a desired output frequency for operating an asynchronous motor of which the rotary speed is adjustable, the inverter including a computation circuit arranged to calculate from the values of at least two of the parameters inverter current, inverter voltage and desired inverter frequency and at least one constant, a computed value for the inverter current or inverter voltage or inverter frequency which, together with the first-mentioned values, will operate an asynchronous motor supplied by the inverter at a substantially constant slip frequency, and means to adjust the inverter voltage either to make the actual value of the inverter current or inverter voltage substantially equal to its computed value or to make the computed inverter frequency substantially equal to the desired inverter frequency.

2. A converter circuit according to claim 1, further comprising D.C. supply means including a voltage regulator, and a voltage sensor and a current sensor connected between the D.C. supply means and the inverter, the voltage and current sensors being connected to the computation circuit and the means to adjust the inverter voltage comprising the voltage regulator.

3. A converter circuit according to claim 1 or 2, wherein the D.C. supply means comprises a rectifier circuit.

4. A converter circuit according to any preceding claim, wherein the computation circuit comprises a computation element with which, in use, a value taking the slip frequency into account is introduced and is held constant below the nominal rotary speed at least over the major part of the motor operating range.

5. A converter circuit according to any preceding claim, wherein the computation circuit calculates the computed value by using the equation

$$f = \frac{1}{k_1}\left(\frac{E}{I} - k_2\right)$$

where f is the desired inverter frequency, E is the inverter voltage, I is the inverter current, k_1 is a (or the) value taking the slip frequency into account, and k_2 is the said at least one constant and corresponds to the winding resistance of the stator of said motor.

6. A converter circuit according to any preceding claim wherein the computation circuit comprises a division circuit connected to receive the value of inverter voltage as the dividend and the value of inverter current as the divisor, and a subtraction circuit in which a fixed value is subtracted from the quotient.

7. A converter circuit according to any of claims 1 to 5, wherein the computation circuit comprises a subtraction circuit arranged to subtract a voltage-proportional value from the value of inverter voltage, and a division circuit connected to receive the output value of the subtraction circuit as the dividend and the value of inverter current as the divisor.

8. A converter circuit according to any of claims 1 to 5, wherein the computation circuit comprises an addition circuit to add a value proportional to the value of desired inverter frequency to the said at least one constant, and a division circuit connected to receive the value of inverter voltage as the dividend and the output value of the addition circuit as the divisor.

9. A converter circuit according to any of claims 1 to 5, wherein the computation circuit comprises a subtraction circuit to subtract a current-proportional value from the value of inverter voltage, and a division circuit connected to receive the output value of the subtraction circuit as the dividend and the value of desired inverter frequency as the divisor.

10. A converter circuit according to claim 7 or 8 when dependent on claim 5, wherein a computation element introducing a factor $1/k_1$ is connected before the dividend input or after the output of the division circuit.

11. A converter circuit according to any of claims 1 to 5, wherein the computation circuit comprises a multiplication circuit arranged to receive the value of desired inverter frequency and the value of inverter current, one of which is multiplied by a (or the) value taking slip frequency into account, and an addition circuit in which the multiplication result is added to the value of inverter current multiplied by the said at least one constant.

12. A converter circuit according to any preceding claim wherein the said at least one constant and/or the value taking the slip frequency into account can be adjustably set.

13. A converter circuit according to any of claims 1 to 11, wherein the computation circuit is arranged to make use of a value taking the slip frequency into account and that value depends on at least one of the three parameters.

14. A converter circuit according to any of claims 1 to 5, wherein the inverter includes a frequency generator arranged to be controlled by the setting of desired inverter frequency.

15. A converter circuit according to any of claims 1 to 5, wherein the inverter includes a frequency generator arranged to be controlled by the computed value of inverter frequency.

16. A converter circuit according to any preceding claim, wherein a minimum current generator is provided to hold the value of inverter current supplied to the computation circuit at a predetermined minimum value for small values of actual inverter current.

17. A converter circuit according to any preceding claim, wherein the means to adjust the inverter voltage comprises a first comparator and the output of the first comparator is connected to the output of a second comparator arranged to compare an adjustable maximum power value with the product of a factor corresponding approximately to the value of inverter current and a factor corresponding approximately to the value of inverter voltage and to override the first comparator when the product exceeds the maximum power value.

18. A converter circuit according to any preceding claim, wherein the means to adjust the inverter voltage comprises a first comparator and the output of the first comparator is connected to the output of a further comparator arranged to compare an adjustable maximum torque value with a comparative value corresponding to inverter current and to override the first comparator when the comparative value exceeds the maximum torque value.

19. A converter circuit according to any preceding claim, wherein the computation circuit comprises a computation element arranged to introduce a factor proportional to slip frequency and hold it constant in an operative range up to about nominal motor frequency, and a switch element arranged to increase this factor above the nominal frequency.

20. A converter circuit according to claim 19, wherein the switch element is mechanically coupled to a setting device operative to set desired inverter frequency.

21. A converter circuit according to claim 20, wherein the switch element is arranged to control a division circuit in series with a computation element in the form of an amplifier, a signal dependent on the desired inverter frequency being fed, in use, as the divisor to the division circuit.

22. A converter circuit according to claim 20, wherein the switch element is arranged to adjust a feedback resistor of a computation element in the form of an amplifier with negative feedback, the feedback resistor being adjusted in dependence on desired inverter frequency.

23. A converter circuit according to any of claims 19 to 22, wherein the factor proportional to slip frequency, in use, doubles between the simple and double nominal frequency and substantially remains at this double value on a further rise in frequency.

24. A converter circuit according to one of claims 1 to 20, wherein the computation circuit comprises a computation element arranged to introduce a factor proportional to the slip frequency and hold it constant in the operating range up to just below nominal voltage, and a switch element which increases this factor above this voltage limiting value.

25. A converter circuit according to claim 24, wherein the switch element is arranged to be controlled by a control signal which is equal to the value of inverter voltage reduced by a current-proportional value, and the voltage limiting value corresponds to about 90 to 95% of nominal motor voltage.

26. A converter circuit according to claims 18 and 25, wherein the computation element is an amplifier disposed between the subtraction circuit and division circuit, and the switch element is arranged to alter the degree of amplification of the amplifier and be controlled by the input signal of the amplifier.

27. A converter circuit according to one of claims 22 to 24, wherein the factor proportional to slip frequency is arranged to approximately double continuously between the voltage limiting value and a value corresponding to the nominal voltage.

28. A converter circuit according to any preceding claim, wherein the output of an input device to set the desired inverter frequency is connected to the output of a comparator arranged to compare an adjustable maximum current value with the value of inverter current and to reduce the desired inverter frequency value relative to the value set when the inverter current value exceeds the maximum current.

29. A converter circuit according to any preceding claim, wherein the output of an input device to set the desired inverter frequency is connected to the output of a comparator arranged to compare an adjustable maximum voltage with the inverter voltage value and to increase the desired inverter frequency value relative to the value set when the inverter voltage measurement signal exceeds the maximum voltage.

30. A converter circuit according to any preceding claim, wherein the output of an

input device to set the desired inverter frequency is connected to the output of a limiting value circuit arranged to change, when the difference between one of the parameter values and the associated computed value exceeds a predetermined limiting value, the desired inverter frequency value relative to the set value in the sense of a reduction of the difference.

31. A converter circuit according to claim 30, wherein the means to adjust the inverter voltage comprises a first comparator and the limiting value circuit is preceded by a subtraction circuit fed with two quantities to be compared in the first comparator.

32. A converter circuit according to claim 30, wherein a second computation circuit is provided to compute a computed inverter frequency value from the value of inverter voltage and the value of inverter current and the limiting value circuit is preceded by a subtraction circuit arranged to receive the desired inverter frequency value and the computed inverter frequency value.

33. A converter circuit according to one of claims 30 to 32, wherein the limiting value circuit comprises two diodes, for example Zener diodes, connected in anti-parallel.

34. A converter circuit according to any preceding claim, wherein the desired inverter frequency value is introduced, in use, as a series of pulses and fed to the computation circuit by way of a digital/analogue converter.

35. A converter circuit according to claim 9, wherein the desired inverter frequency value is fed, in use, to the division circuit as a series of pulses, the division circuit comprises an integrator arranged to integrate a voltage measurement signal between two successive pulses, and a storage device is provided to store each last integration result.

36. A converter circuit according to claim 35 and claim 9 as dependent on any of claims 1 to 5 other than claim 2 wherein the inverter voltage value is obtained, in use, from the voltage on the output side of the inverter between two phases, and the pulses correspond, in use, to the output frequency of the inverter.

37. A converter circuit according to any preceding claim wherein the inverter current value is obtained, in use, from an amplifier with adjustable degree of amplification arranged to give a current measurement signal.

38. A converter circuit according to any preceding claim, wherein the inverter current value is fed, in use, to the computation circuit by way of a timing network, for example an RC network.

39. A converter circuit according to any preceding claim, wherein a limiting circuit is provided to limit slip frequency to about twice nominal slip frequency.

40. A converter circuit according to claim 39, wherein a limiting circuit is provided in the path of a signal relating to inverter frequency, for example the desired inverter frequency value.

41. A converter circuit according to any preceding claim, and including the features of claim 18, wherein the inverter voltage value is fed, in use, by way of a band pass filter of which the output signal is fed, in use, in the same sense as the inverter current value to the said further comparator.

42. A converter circuit according to any preceding claim, wherein a slip compensating signal generator is provided to deliver a slip compensating signal which is zero up to about the nominal frequency of the inverter and above this has a value increasing with the frequency.

43. A converter circuit according to claim 42, wherein the slip compensating signal generator is arranged to be controlled by the same input value as is a computation element determining a factor proportional to the slip frequency.

44. A converter circuit according to claim 42 or claim 43, wherein an addition circuit is provided to add a first slip computing signal to a signal relating to inverter frequency, for example, the desired inverter frequency value.

45. A converter circuit according to one of claims 42 to 44, and including the features of claim 18, wherein an addition circuit is provided to add a second slip compensating signal to an adjustable torque value fed to the said further comparator.

46. A converter circuit according to claim 45, wherein the second slip compensating signal is fed, in use, by way of an amplifier of which the degree of amplification can assume at least two settings depending on an adjustable torque value, the higher setting being associated with a higher torque.

47. A converter circuit according to one of claims 41 to 46, wherein the means to adjust the inverter voltage comprises a first comparator and the output of the first comparator is connected to the output of another comparator arranged to compare an adjustable maximum current value with the value of inverter current and to override the first comparator when the inverter current exceeds the maximum current value.

48. A converter circuit substantially as herein described with reference to, and as illustrated by the accompanying drawings.

49. A converter circuit substantially as described with reference to, and as illustrated by, Figures 1 and 2 of the accompanying drawings.

50. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1 and 3 of the accompanying drawings.

51. A converter circuit substantially as herein described with reference to, and as illustrated by Figures 1 and 4 of the accompanying drawings.

52. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 2 and 5 of the accompanying drawings.

53. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 2 and 6 of the accompanying drawings.

54. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 2, 5 and 7 of the accompanying drawings.

55. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 2, 6 and 7 of the accompanying drawings.

56. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 3 and 8 of the accompanying drawings.

57. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1 and 9 of the accompanying drawings.

58. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 4 and 10 of the accompanying drawings.

59. A converter circuit substantially as herein described with reference to, and as illustrated by, Figures 1, 2, 6 and 15 of the accompanying drawings.

60. An asynchronous electric motor connected for supply by a converter circuit as claimed in any preceding claim.

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1594460 COMPLETE SPECIFICATION

6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

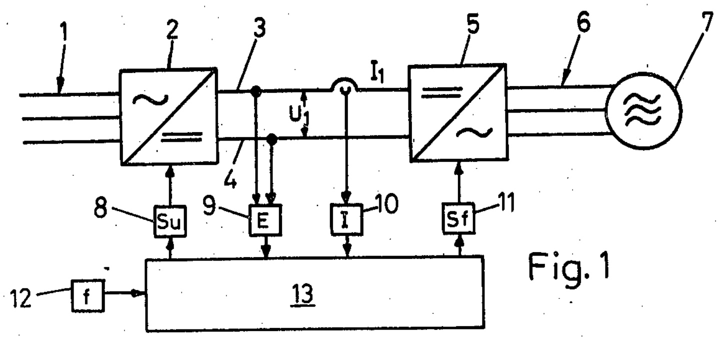


Fig. 1

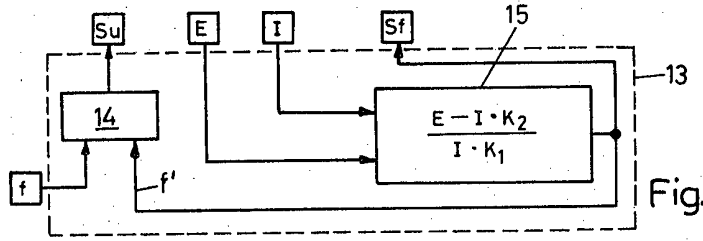


Fig. 2

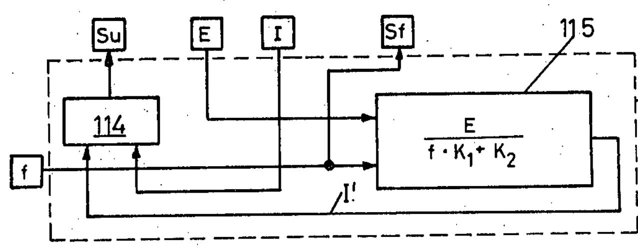


Fig. 3

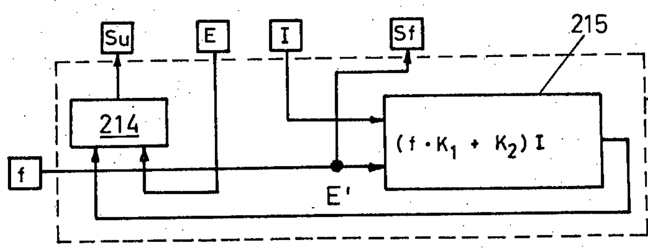
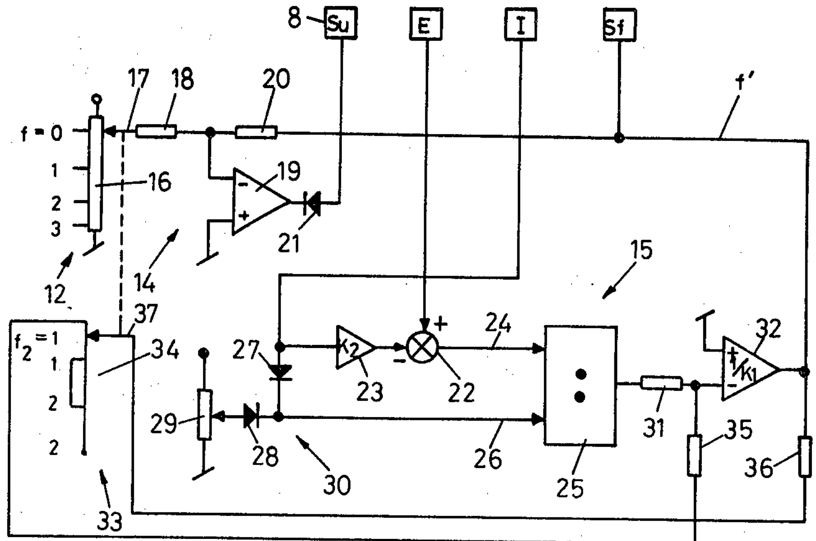


Fig. 4


Su
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18
20
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f = 0
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16
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12
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37
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27
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23
22
24
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26
28
29
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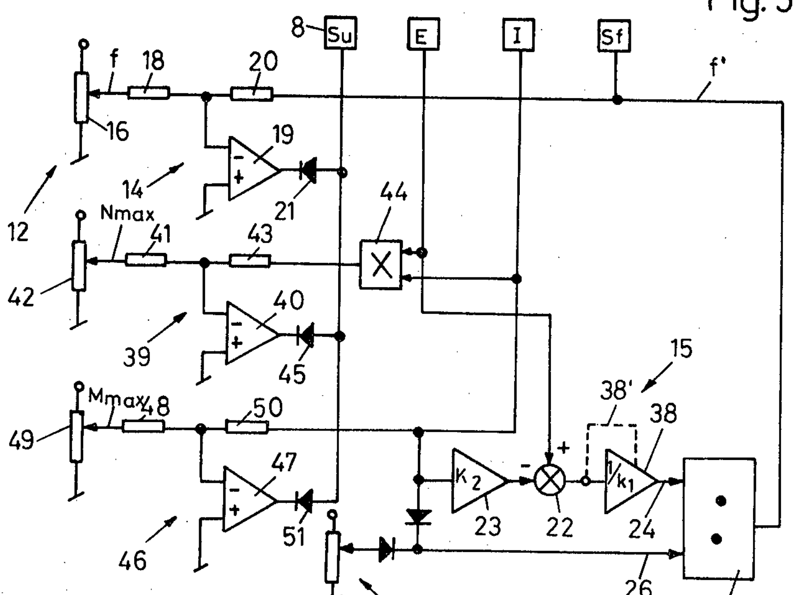
Fig. 5


Su
E
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8
f
18
20
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16
19
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12
Nmax
41
43
44
42
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Fig. 6

1594460 COMPLETE SPECIFICATION

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Sheet 3

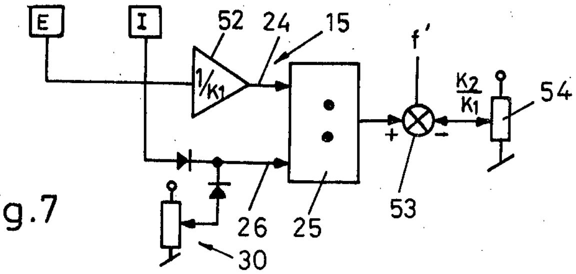

Fig.7

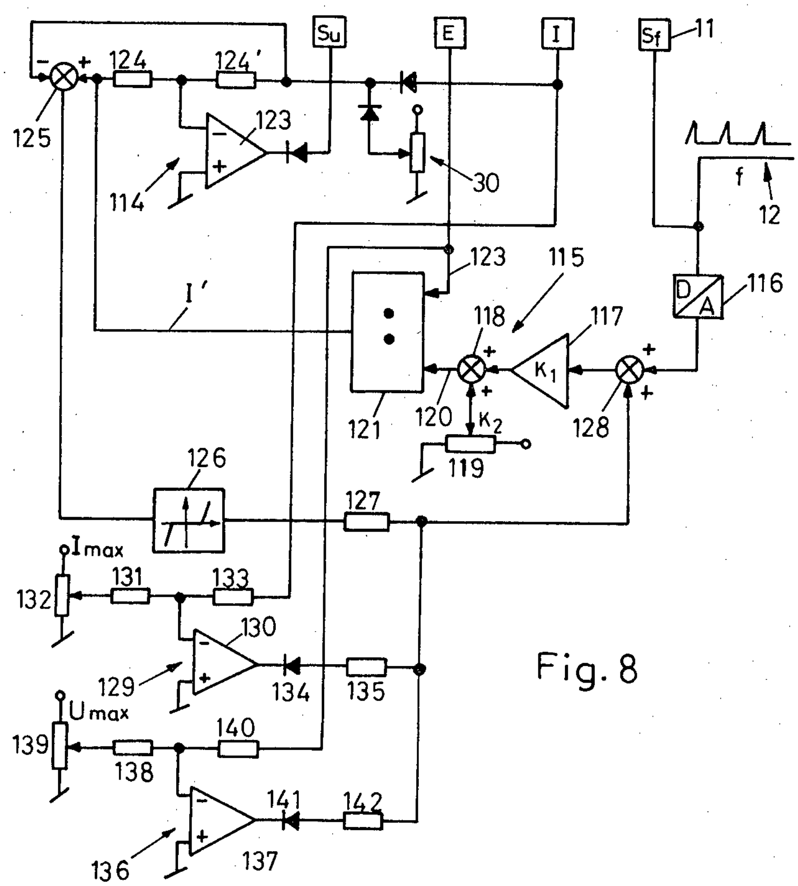

Fig. 8

1594460 COMPLETE SPECIFICATION

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Sheet 4

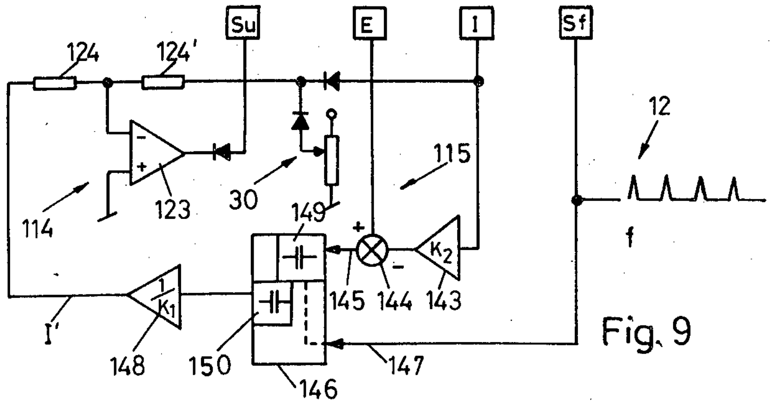


Fig. 9

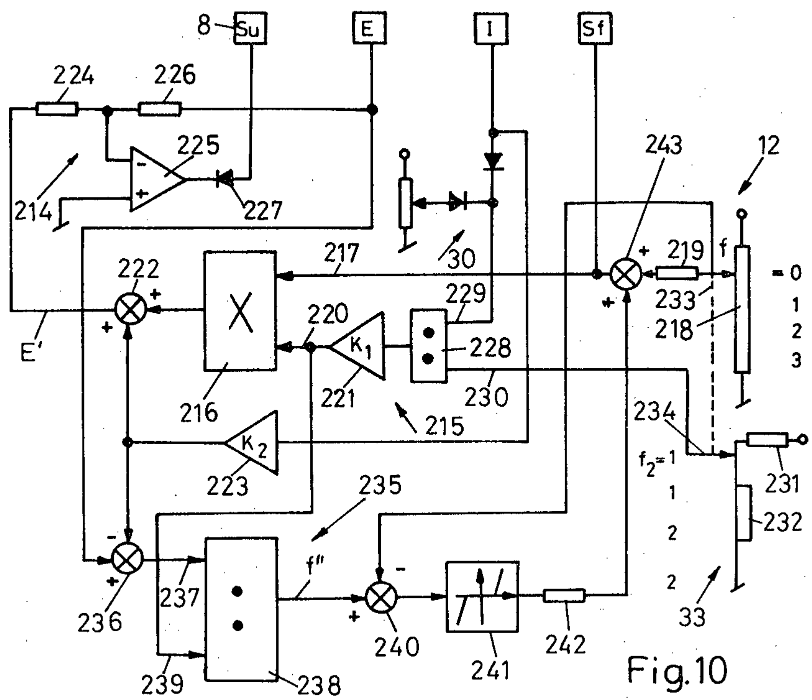


Fig. 10

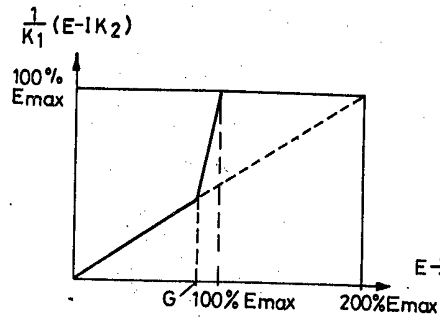


Fig. 11

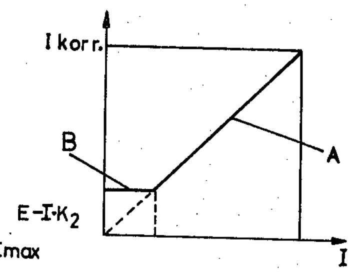


Fig. 12

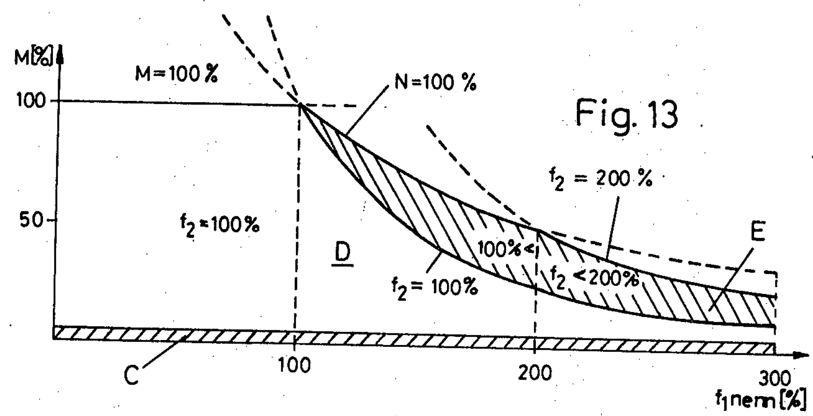


Fig. 13

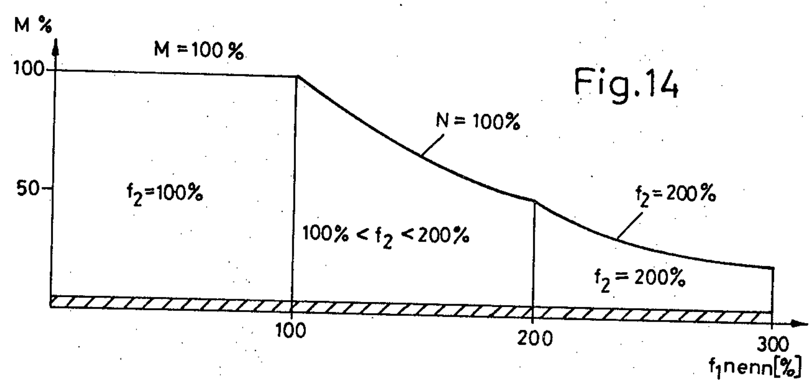
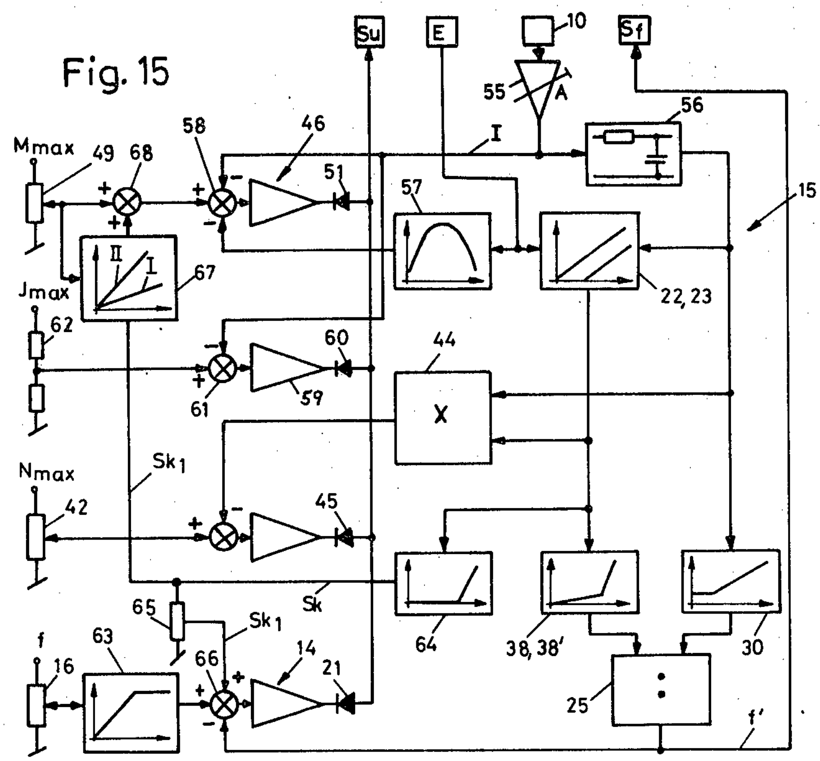


Fig.14

Fig. 15


Su
E
10
Sf
55
A
56
58
46
Mmax
49
68
I
51
57
15
II
I
67
22, 23
Jmax
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X
Nmax
Sk1
42
45
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65
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38, 38'
30
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66
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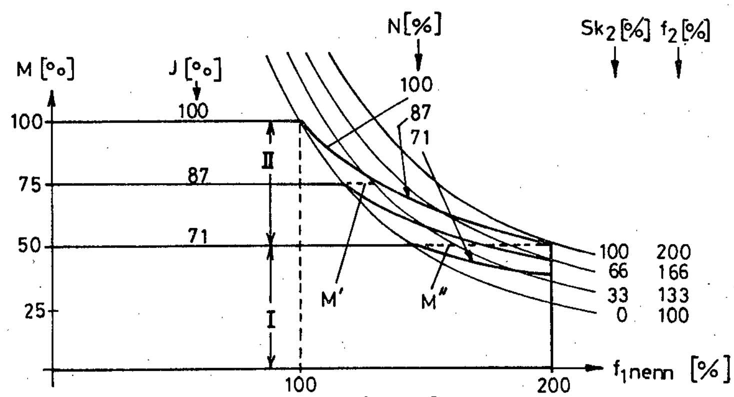
N[%]
Sk2 [%] f2 [%]
M [°o]
J [°o]
100
87
71
100
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75
87
50
71
25
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66 166
33 133
0 100
100
200
f1nenn [%]

Fig.16