



(51) International Patent Classification:

G02F 1/1368 (2006.01) G06F 3/044 (2006.01)
G02F 1/1333 (2006.01) G09F 9/00 (2006.01)
G02F 1/1343 (2006.01) G09F 9/30 (2006.01)
G06F 3/041 (2006.01) H01L 29/786 (2006.01)

(21) International Application Number:

PCT/IB2016/052927

(22) International Filing Date:

19 May 2016 (19.05.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2015-110612 29 May 2015 (29.05.2015) JP

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

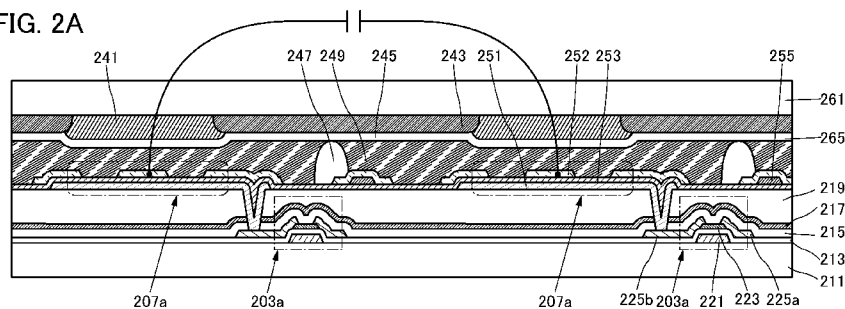
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: INPUT/OUTPUT DEVICE AND ELECTRONIC DEVICE

FIG. 2A



(57) Abstract: An input/output device is provided. The input/output device includes a first pixel electrode, a second pixel electrode, a first common electrode, a second common electrode, a liquid crystal, a first insulating film, a second insulating film, and a transistor. The first common electrode can serve as one electrode of a sensor element. The second common electrode can serve as the other electrode of the sensor element. The transistor includes a first gate, a second gate, and a semiconductor layer. The pixel electrode, the common electrodes, and the second gate are positioned on different planes. The second gate contains one or more kinds of metal elements included in the semiconductor layer. The second gate, the pixel electrode, and the common electrodes preferably contain one or more kinds of metal elements included in the semiconductor layer.



DESCRIPTION

INPUT/OUTPUT DEVICE AND ELECTRONIC DEVICE

5 TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to an input/output device and an electronic device.

[0002]

10 Note that one embodiment of the present invention is not limited to the above technical field. Specifically, examples of the technical field of one embodiment of the present invention disclosed in this specification and the like include a semiconductor device, a display device, a light-emitting device, a power storage device, a memory device, an electronic device, a lighting device, an input device (e.g., a touch sensor), an output device, an input/output device (e.g., a
15 touch panel), a method for driving any of them, and a method for manufacturing any of them.

BACKGROUND ART

[0003]

Transistors used for most flat panel displays typified by a liquid crystal display device
20 and a light-emitting display device are formed using silicon semiconductors such as amorphous silicon, single crystal silicon, and polycrystalline silicon provided over glass substrates. Furthermore, such a transistor employing such a silicon semiconductor is used in integrated circuits (ICs) and the like.

[0004]

25 In recent years, attention has been drawn to a technique in which, instead of a silicon semiconductor, a metal oxide exhibiting semiconductor characteristics is used in transistors. Note that in this specification, a metal oxide exhibiting semiconductor characteristics is referred to as an oxide semiconductor. For example, in Patent Documents 1 and 2, a technique is disclosed in which a transistor is manufactured using zinc oxide or an In-Ga-Zn-based oxide as
30 an oxide semiconductor and the transistor is used as a switching element or the like of a pixel of a display device.

[0005]

What is desirable is a touch panel in which a display device is provided with a function of inputting data with a finger or the like touching a screen as a user interface.

35 [0006]

A display device provided with a touch sensor or a display module provided with a touch sensor is called a touch panel, a touch screen, or the like. Furthermore, a device that has a touch sensor and does not have a display element is called a touch panel in some cases. Thus, a display device provided with a touch sensor or a display module provided with a touch sensor is called a display device having a touch sensor, a display device having a touch panel, a touch sensor having a display device, or a touch panel having a display device in some cases. Note that a display device provided with a touch sensor is referred to as a touch panel.

[0007]

For example, Patent Documents 3 to 6 each disclose a touch panel using a liquid crystal element as a display element.

[Reference]

[Patent Document]

[0008]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

[Patent Document 3] Japanese Published Patent Application No. 2011-197685

[Patent Document 4] Japanese Published Patent Application No. 2014-44537

[Patent Document 5] Japanese Published Patent Application No. 2014-178847

[Patent Document 6] United States Patent Application Publication No. 2008/0158183

DISCLOSURE OF INVENTION

[0009]

An object of one embodiment of the present invention is to provide a thin input/output device. Another object of one embodiment of the present invention is to provide a lightweight input/output device. Another object of one embodiment of the present invention is to provide an input/output device with a small number of components.

[0010]

Another object of one embodiment of the present invention is to provide a highly reliable input/output device. Another object of one embodiment of the present invention is to provide an input/output device with high detection sensitivity. Another object of one embodiment of the present invention is to provide a novel input/output device.

[0011]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects can be derived from the description of the specification, the drawings, the claims, and the

like.

[0012]

One embodiment of the present invention is an input/output device including a first pixel electrode, a second pixel electrode, a first common electrode, a second common electrode, a liquid crystal, a first insulating film, a second insulating film, and a transistor. The first common electrode can serve as one electrode of a sensor element. The second common electrode can serve as the other electrode of the sensor element. The transistor includes a first gate, a second gate, and a semiconductor layer. The semiconductor layer includes an oxide semiconductor in a channel formation region. The second gate includes an oxide conductor. The oxide conductor contains one or more kinds of metal elements included in the oxide semiconductor. The semiconductor layer is over the first gate. The second gate is over the semiconductor layer. The first insulating film is over the second gate. The first pixel electrode, the second pixel electrode, the first common electrode, and the second common electrode are over the first insulating film. The first pixel electrode partly overlaps with the first common electrode with the second insulating film interposed therebetween. The second pixel electrode partly overlaps with the second common electrode with the second insulating film interposed therebetween. The liquid crystal is over the first pixel electrode, the second pixel electrode, the first common electrode, and the second common electrode. The first pixel electrode is apart from the second pixel electrode on one plane. The first common electrode is apart from the second common electrode on one plane.

[0013]

The transistor is included in at least one of a display portion or a driver circuit portion. For example, an input/output device of one embodiment of the present invention includes two transistors that are each the above transistor. A source or a drain of one of the two transistors may be electrically connected to the first pixel electrode. A source or a drain of the other of the two transistors may be electrically connected to the second pixel electrode. Alternatively, the transistor may be positioned in the driver circuit portion.

[0014]

In each of the above structures, the second gate may be electrically connected to the first gate.

[0015]

In each of the above structures, the second insulating film may be over the first pixel electrode and the second pixel electrode, and the first common electrode and the second common electrode may be over the second insulating film. In each of the above structures, the second insulating film may be over the first common electrode and the second common electrode, and

the first pixel electrode and the second pixel electrode may be over the second insulating film.

[0016]

In each of the above structures, the first pixel electrode and the second pixel electrode may each include at least one metal element contained in the oxide semiconductor.

5 Furthermore, the first common electrode and the second common electrode may each include at least one metal element contained in the oxide semiconductor.

[0017]

In each of the above structures, the oxide semiconductor and the oxide conductor may each include an oxide containing indium. Furthermore, the first pixel electrode and the second
10 pixel electrode may each include an oxide containing indium. Furthermore, the first common electrode and the second common electrode may each include an oxide containing indium.

[0018]

In each of the above structures, the oxide semiconductor and the oxide conductor may each include an In- M_1 -Zn oxide (M_1 is Al, Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). Furthermore,
15 the first pixel electrode and the second pixel electrode may each include the In- M_1 -Zn oxide. Furthermore, the first common electrode and the second common electrode may each include the In- M_1 -Zn oxide.

[0019]

In each of the above structures, the first pixel electrode, the second pixel electrode, the
20 first common electrode, and the second common electrode may each have a function of transmitting visible light.

[0020]

In each of the above structures, a first conductive film may be positioned between the first insulating film and the first common electrode. The first conductive film may have a lower
25 resistivity than the first common electrode and may be electrically connected to the first common electrode. Furthermore, a second conductive film may be positioned between the first insulating film and the second common electrode. The second conductive film may have a lower resistivity than the second common electrode and may be electrically connected to the second common electrode. The first conductive film may be apart from the second conductive
30 film on one plane.

[0021]

In each of the above structures, a light-blocking film may be provided. The light-blocking film may include a region overlapping with at least one of the first conductive film and the second conductive film with the liquid crystal positioned therebetween.

35 [0022]

Another embodiment of the present invention is a module such as a module in which a connector such as a flexible printed circuit (FPC) or a tape carrier package (TCP) is attached to the input/output device or a module in which an IC is mounted on the input/output device by a chip on glass (COG) method, a chip on film (COF) method, or the like.

5 [0023]

Another embodiment of the present invention is an electronic device including the module and at least one of an antenna, a battery, a housing, a speaker, a microphone, an operation switch, and an operation button.

[0024]

10 According to one embodiment of the present invention, a thin input/output device can be provided. According to another embodiment of the present invention, a lightweight input/output device can be provided. According to another embodiment of the present invention, an input/output device with a small number of components can be provided.

[0025]

15 According to one embodiment of the present invention, a highly reliable input/output device can be provided. According to another embodiment of the present invention, an input/output device with high detection sensitivity can be provided. According to another embodiment of the present invention, a novel input/output device or the like can be provided.

[0026]

20 Note that the description of these effects does not disturb the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above. Other effects can be derived from the description of the specification, the drawings, the claims, and the like.

25 BRIEF DESCRIPTION OF DRAWINGS

[0027]

FIGS. 1A and 1B are a top view and a cross-sectional view illustrating an example of an input/output device.

FIGS. 2A and 2B are cross-sectional views illustrating examples of an input/output
30 device.

FIGS. 3A to 3F are cross-sectional views illustrating examples of an input/output device.

FIG. 4 is a cross-sectional view illustrating an example of an input/output device.

FIG. 5 is a cross-sectional view illustrating an example of an input/output device.

35 FIG. 6 is a cross-sectional view illustrating an example of an input/output device.

FIGS. 7A and 7B illustrate examples of a sensor element and a pixel.

FIGS. 8A to 8E illustrate examples of operation of a sensor element and a pixel.

FIGS. 9A and 9B are top views illustrating examples of a sensor element and a pixel.

FIG. 10 is a top view illustrating an example of a sensor element.

5 FIGS. 11A and 11B are top views illustrating an example of a sensor element.

FIG. 12 is a top view illustrating an example of an input/output device.

FIG. 13 is a top view illustrating an example of an input/output device.

FIGS. 14A and 14B are top views illustrating examples of an input/output device.

FIG. 15 is a block diagram illustrating an example of a touch panel module.

10 FIGS. 16A to 16C illustrate examples of a touch panel module.

FIGS. 17A to 17D are cross-sectional views illustrating an example of a method for manufacturing a transistor and the like.

FIGS. 18A to 18C are cross-sectional views illustrating an example of a method for manufacturing a transistor and the like.

15 FIGS. 19A to 19C are cross-sectional views illustrating an example of a method for manufacturing a transistor and the like.

FIG. 20 is a cross-sectional view of an example illustrating a method for manufacturing a transistor and the like.

FIG. 21 is a cross-sectional view illustrating an example of a transistor.

20 FIGS. 22A to 22C are a top view and cross-sectional views illustrating an example of a transistor.

FIGS. 23A to 23D are cross-sectional views illustrating examples of a transistor.

FIGS. 24A and 24B show band structures.

FIGS. 25A to 25D are cross-sectional views illustrating examples of a transistor.

25 FIGS. 26A to 26E show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD and selected-area electron diffraction patterns of a CAAC-OS.

FIGS. 27A to 27E show a cross-sectional TEM image and plan-view TEM images of a CAAC-OS and images obtained through analysis thereof.

30 FIGS. 28A to 28D show electron diffraction patterns and a cross-sectional TEM image of an nc-OS.

FIGS. 29A and 29B show cross-sectional TEM images of an a-like OS.

FIG. 30 shows a change in crystal part of an In-Ga-Zn oxide induced by electron irradiation.

FIG. 31 shows an example of a touch panel module.

35 FIGS. 32A to 32H illustrate examples of electronic devices.

FIGS. 33A and 33B illustrate examples of electronic devices.

FIG. 34 is a cross-sectional view illustrating an example of an input/output device.

FIG. 35 is a photograph of an input/output device of an example.

FIG. 36 shows measured XRD spectra of samples.

5 FIGS. 37A and 37B are TEM images of samples and FIGS. 37C to 37L are electron diffraction patterns thereof.

FIGS. 38A to 38C show EDX mapping images of a sample.

BEST MODE FOR CARRYING OUT THE INVENTION

10 [0028]

Embodiments are described in detail with reference to drawings. Note that the present invention is not limited to the description below, and it is easily understood by those skilled in the art that various changes and modifications can be made without departing from the spirit and scope of the present invention. Accordingly, the present invention should not be interpreted as
15 being limited to the content of the embodiments below.

[0029]

Note that in the structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and description of such portions is not repeated. Furthermore, the same hatching
20 pattern is applied to portions having similar functions, and the portions are not especially denoted by reference numerals in some cases.

[0030]

In addition, the position, size, range, or the like of each structure illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the
25 disclosed invention is not necessarily limited to the position, the size, the range, or the like disclosed in the drawings and the like.

[0031]

Note that the terms "film" and "layer" can be interchanged with each other depending on the case or circumstances. For example, the term "conductive film" can be changed into the
30 term "conductive layer" in some cases. Also, the term "insulating layer" can be changed into the term "insulating film" in some cases.

[0032]

In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to -10° and less than or equal to 10° , and accordingly also
35 includes the case where the angle is greater than or equal to -5° and less than or equal to 5° . In

addition, the term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to -30° and less than or equal to 30° . In addition, the term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100° , and accordingly also includes the case where the angle is greater than or equal to 85° and less than or equal to 95° . A term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120° .

[0033]

In this specification, trigonal and rhombohedral crystal systems are included in a hexagonal crystal system.

[0034]

(Embodiment 1)

In this embodiment, an input/output device of one embodiment of the present invention is described with reference to FIGS. 1A and 1B, FIGS. 2A and 2B, FIGS. 3A to 3F, FIG. 4, FIG. 5, FIG. 6, FIGS. 7A and 7B, FIGS. 8A to 8E, FIGS. 9A and 9B, FIG. 10, FIGS. 11A and 11B, FIG. 12, FIG. 13, FIGS. 14A and 14B, FIG. 15, and FIGS. 16A to 16C.

[0035]

The input/output device of one embodiment of the present invention is an in-cell touch panel that has a function of displaying an image and serves as a touch sensor.

[0036]

There is no particular limitation on a display element included in the input/output device of one embodiment of the present invention. As the display element, a variety of display elements including a liquid crystal element, an optical element that utilizes micro electro mechanical systems (MEMS), a light-emitting element such as an organic electroluminescent (EL) element or a light-emitting diode (LED), and an electrophoretic element can be used.

[0037]

In this embodiment, a transmissive liquid crystal display device using a liquid crystal element in a horizontal electric field mode is described as an example.

[0038]

There is no particular limitation on a sensor element included in the input/output device of one embodiment of the present invention. Note that a variety of sensors that can sense proximity or touch of a sensing target such as a finger or a stylus can be used as the sensor element.

[0039]

For example, a variety of types such as a capacitive type, a resistive type, a surface

acoustic wave type, an infrared type, an optical type, and a pressure-sensitive type can be used for the sensor.

[0040]

In this embodiment, an input/output device including a capacitive sensor element is described as an example.

[0041]

Examples of the capacitive sensor element are a surface capacitive sensor element and a projected capacitive sensor element. Examples of the projected capacitive sensor element include a self-capacitive sensor element and a mutual capacitive sensor element. The use of a mutual capacitive sensor element is preferable because multiple points can be sensed simultaneously.

[0042]

In the input/output device of one embodiment of the present invention, an electrode or the like included in a sensor element is provided only on a substrate supporting a display element. The input/output device of one embodiment of the present invention is a full-in-cell touch panel. As an example of a structure of an in-cell touch panel, a structure in which an electrode and the like included in a sensor element are provided on both a substrate supporting a display element and a counter substrate or on only the counter substrate is given. As compared with the structure, the full-in-cell touch panel is preferable because the structure of the counter substrate can be simplified.

[0043]

The input/output device of one embodiment of the present invention is preferable because an electrode included in the display element also serves as an electrode included in the sensor element and thus the manufacturing process can be simplified and the manufacturing cost can be reduced.

[0044]

One embodiment of the present invention can reduce the thickness or weight of the input/output device or the number of components of the input/output device as compared with a structure in which a display panel and a sensor element separately formed are attached to each other or a structure in which a sensor element is formed on a counter substrate side.

[0045]

In the input/output device of one embodiment of the present invention, both an FPC for supplying a signal for driving a pixel and an FPC for supplying a signal for driving a sensor element are on one substrate side. With this structure, the touch panel can be easily incorporated into an electronic device, and the number of components can be reduced. Note

that the signal for driving a pixel and the signal for driving a sensor element may be supplied by one FPC.

[0046]

The structure of the input/output device of one embodiment of the present invention is described below.

[0047]

[Cross-sectional structure example 1 of input/output device]

FIG. 1A is a top view of an input/output device 300. FIG. 1B is a cross-sectional view taken along dashed-dotted lines A-B and C-D in FIG. 1A.

[0048]

As illustrated in FIG. 1A, the input/output device 300 includes a display portion 301 and scan line driver circuits 302. The display portion 301 includes a plurality of pixels 303, a plurality of signal lines, and a plurality of scan lines, and has a function of displaying an image. Moreover, the display portion 301 also serves as an input portion. That is, the display portion 301 includes a plurality of sensor elements that can sense touch or proximity of a sensing target to the input/output device 300 and thus serves as a touch sensor. The scan line driver circuit 302 has a function of outputting a scan signal to the scan lines included in the display portion 301. The pixel 303 includes a plurality of subpixels. Although FIG. 1A illustrates an example in which the pixel 303 includes three subpixels, one embodiment of the present invention is not limited to this example.

[0049]

Although FIG. 1A illustrates an example in which the input/output device 300 includes the scan line driver circuits, one embodiment of the present invention is not limited to this example. The input/output device 300 that does not include any of a scan line driver circuit, a signal line driver circuit, and a sensor driver circuit may be employed, or the input/output device 300 that includes any one or more of a scan line driver circuit, a signal line driver circuit, and a sensor driver circuit may be employed.

[0050]

In the input/output device 300, an IC 268 is mounted on a substrate 211 by a COG method or the like. The IC 268 includes, for example, any one or more of a signal line driver circuit, a scan line driver circuit, and a sensor driver circuit.

[0051]

An FPC 269 is electrically connected to the input/output device 300. The IC 268 and a scan line driver circuit are supplied with a signal from the outside via the FPC 269. Furthermore, a signal can be output from the IC 268 to the outside via the FPC 269.

[0052]

An IC may be mounted on the FPC 269. For example, an IC including any one or more of a signal line driver circuit, a scan line driver circuit, and a sensor driver circuit may be mounted on the FPC 269. For example, the IC may be mounted on the FPC 269 by a COF method or a tape automated bonding (TAB) method.

[0053]

For example, the IC 268 may include a signal line driver circuit and a sensor driver circuit. Alternatively, for example, the IC 268 may include a signal line driver circuit and the IC mounted on the FPC 269 may include a sensor driver circuit.

[0054]

As illustrated in FIG. 1B, the input/output device 300 includes a transistor 201a, a transistor 203a, a connection portion 205a, a liquid crystal element 207a, and the like over the substrate 211.

[0055]

FIG. 1B illustrates the cross section of one subpixel as an example of the display portion 301. For example, a subpixel exhibiting a red color, a subpixel exhibiting a green color, and a subpixel exhibiting a blue color form one pixel, and thus full-color display can be achieved in the display portion 301. Note that the color exhibited by subpixels is not limited to red, green, and blue. For example, a subpixel exhibiting white, yellow, magenta, cyan, or the like may be used for a pixel.

[0056]

The transistors 201a and 203a include a gate electrode 221, an insulating film 213, an oxide semiconductor film 223, a source electrode 225a, and a drain electrode 225b. The transistor 201a further includes a conductive film 226, an insulating film 215, and an oxide conductor film 227. Note that the insulating film 215 can also be regarded as a component of the transistor 203a.

[0057]

The gate electrode 221 and the oxide conductor film 227 can each serve as a gate. The transistor 201a has a structure in which an oxide semiconductor film where a channel is formed is sandwiched between two gates. The gate electrode 221 is electrically connected to the oxide conductor film 227 through the conductive film 226. Transistors having such a structure in which two gates are electrically connected to each other can have a higher field-effect mobility and thus have higher on-state current than other transistors. Consequently, a circuit capable of high-speed operation can be obtained. Furthermore, the area occupied by a circuit portion can be reduced. The use of a transistor having high on-state current can reduce signal delay in

wirings and can suppress display unevenness even in an input/output device in which the number of wirings is increased in accordance with the increase in size or resolution. Moreover, with such a structure, a highly reliable transistor can be formed.

[0058]

5 The transistors 201a and 203a may have the same structure or different structures. That is, a transistor included in a driver circuit portion and a transistor included in a display portion may have the same structure or different structures. The driver circuit portion may include transistors having a plurality of structures. The display portion may include transistors having a plurality of structures. For example, a transistor having a structure in which two gates
10 are electrically connected to each other is preferably used for one or more of a shift register circuit, a buffer circuit, and a protection circuit included in a scan line driver circuit.

[0059]

 The transistors 201a and 203a are covered with an insulating film 217 and an insulating film 219. Note that the insulating films 217 and 219 can be regarded as the components of the
15 transistors 201a and 203a. The insulating film 217 preferably has an effect of suppressing diffusion of impurities into a semiconductor included in a transistor. For example, for the insulating film 217, a material through which impurities such as water and hydrogen are hardly diffused is preferably used. As the insulating film 219, an insulating film having a planarization function is preferably selected in order to reduce surface unevenness due to the
20 transistor.

[0060]

 In the transistor 201a, the oxide semiconductor film 223 is used as a semiconductor layer, and the oxide conductor film 227 is used as a gate. In that case, it is preferable that the oxide semiconductor film 223 and the oxide conductor film 227 be formed using an oxide
25 semiconductor.

[0061]

 The resistivity of an oxide semiconductor can be easily controlled in a manufacturing process of the input/output device; thus, an oxide semiconductor can be favorably used as a material of a semiconductor film and a conductive film. When two or more layers included in
30 the input/output device are formed using oxide semiconductors containing the same metal element, the same manufacturing apparatus (e.g., deposition apparatus or processing apparatus) can be used in two or more steps and manufacturing cost can thus be reduced.

[0062]

 An oxide semiconductor is a material that transmits visible light and can therefore be
35 favorably used for an element that transmits visible light.

[0063]

Forming the oxide semiconductor film 223 and the oxide conductor film 227 using the same metal element can reduce the manufacturing cost. For example, when metal oxide targets with the same metal composition are used, the manufacturing cost can be reduced and the same etching gas or the same etchant can be used in processing the oxide semiconductor films. Even when the oxide semiconductor film 223 and the oxide conductor film 227 contain the same metal element, they have different compositions in some cases. For example, a metal element in a film is released during the manufacturing process of the input/output device, which might result in different metal compositions.

[0064]

The transistors 201a and 203a preferably include the oxide semiconductor film 223 that is highly purified to reduce the formation of oxygen vacancies. Accordingly, the current in an off state (off-state current) of the transistors can be made small. Thus, an electrical signal such as an image signal can be held for a longer period, and a writing interval can be set longer in an on state. Accordingly, frequency of refresh operation can be reduced, which leads to an effect of reducing power consumption.

[0065]

In the transistors 201a and 203a, relatively high field-effect mobility can be obtained, whereby high-speed operation is possible. When such a transistor that can operate at high speed is used for the input/output device, a transistor in a display portion and a transistor in a driver circuit portion can be formed over one substrate. That is, since a semiconductor device formed of a silicon wafer or the like is not additionally needed as a driver circuit, the number of components of the input/output device can be reduced. In addition, the transistor that can operate at high speed can be used also in the display portion, whereby a high-quality image can be provided.

[0066]

The liquid crystal element 207a is a liquid crystal element having a fringe field switching (FFS) mode. The liquid crystal element 207a includes a conductive film 251, a conductive film 252, and a liquid crystal 249. Orientation of the liquid crystal 249 can be controlled with an electric field generated between the conductive films 251 and 252. The conductive film 251 can serve as a pixel electrode. The conductive film 252 can serve as a common electrode.

[0067]

When a conductive material that transmits visible light is used for the conductive films 251 and 252, the input/output device 300 can serve as a transmissive liquid crystal display device.

When a conductive material that reflects visible light is used for the conductive film 251 and a conductive material that transmits visible light is used for the conductive film 252, the input/output device 300 can serve as a reflective liquid crystal display device.

[0068]

5 For example, a material containing one of indium (In), zinc (Zn), and tin (Sn) is preferably used for the conductive material that transmits visible light. Specifically, indium oxide, indium tin oxide (ITO), indium zinc oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide to which silicon oxide is added, zinc oxide,
10 and zinc oxide to which gallium is added are given, for example. Note that a film including graphene can be used as well. The film including graphene can be formed, for example, by reducing a film containing graphene oxide.

[0069]

An oxide conductor film is preferably used as the conductive film 251. Furthermore,
15 an oxide conductor film is preferably used as the conductive film 252. The oxide conductor film preferably contains one or more kinds of metal elements included in the oxide semiconductor film 223. For example, the conductor film 251 preferably contains indium and is further preferably an In-*M*-Zn oxide (*M* is Al, Ti, Ga, Ge, Y, Zr, La, Ce, Sn, Mg, Nd, or Hf) film. Similarly, the conductive film 252 preferably contains indium and is further preferably
20 the In-*M*-Zn oxide film.

[0070]

Note that at least one of the conductive films 251 and 252 may be formed using an oxide semiconductor. As described above, when two or more layers included in the input/output device are formed using oxide semiconductors containing the same metal element,
25 the same manufacturing apparatus (e.g., deposition apparatus or processing apparatus) can be used in two or more steps and manufacturing cost can thus be reduced.

[0071]

For example, when a silicon nitride film containing hydrogen is used as an insulating film 253 and an oxide semiconductor is used for the conductive film 251, the conductivity of the
30 oxide semiconductor can be increased owing to hydrogen supplied from the insulating film 253.

[0072]

Examples of a conductive material that reflects visible light include aluminum, silver, and an alloy including any of these metal elements.

[0073]

35 The conductive film 251 serving as a pixel electrode is electrically connected to a

source or a drain of the transistor 203a. Here, the conductive film 251 is electrically connected to the drain electrode 225b.

[0074]

The conductive film 252 has a comb-like top surface shape or a top surface shape provided with a slit (a top surface shape is also referred to as a planar surface shape). The insulating film 253 is provided between the conductive films 251 and 252. The conductive film 251 partly overlaps with the conductive film 252 with the insulating film 253 interposed therebetween. In a region where a coloring film 241 overlaps with the conductive film 251, there is a portion where the conductive film 252 is not provided over the conductive film 251.

[0075]

A conductive film 255 is provided over the insulating film 253. The conductive film 255 is electrically connected to the conductive film 252 and can serve as an auxiliary wiring of the conductive film 252. With the auxiliary wiring electrically connected to the common electrode, voltage drop due to the resistance of the common electrode can be suppressed. In that case, a stacked structure of a conductive film including a metal oxide and a conductive film including a metal is preferably used because these conductive films can be formed by a patterning technique using a half tone mask and thus the process can be simplified.

[0076]

The conductive film 255 has a lower resistivity than the conductive film 252. For example, the conductive film 255 can be formed to have a single-layer structure or a stacked-layer structure using any of metal materials such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, silver, neodymium, and scandium, and an alloy material containing any of these elements.

[0077]

To prevent the conductive film 255 from being perceived by the user of the input/output device, the conductive film 255 is preferably provided in a position overlapping with a light-blocking film 243 and the like.

[0078]

The connection portion 205a is electrically connected to an external input terminal through which a signal (e.g., a video signal, a clock signal, a start signal, and a reset signal) or a potential from the outside is transmitted to the scan line driver circuit 302. An example in which the FPC 269 is provided as an external input terminal is shown here.

[0079]

The connection portion 205a includes a conductive film 231 over the insulating film 213, a conductive film 233 over the conductive film 231, and a conductive film 235 over the

conductive film 233. The conductive film 231 is electrically connected to the conductive film 235 via the conductive film 233. The conductive film 235 is electrically connected to the FPC 269 via a connector 267.

[0080]

5 The conductive film 231 can be formed using the same material and the same step as those of the source electrode 225a and the drain electrode 225b included in the transistors 201a and 203a. The conductive film 233 can be formed using the same material and the same step as those of the conductive film 251 included in the liquid crystal element 207a. The conductive film 235 can be formed using the same material and the same step as those of the conductive film 252 included in the liquid crystal element 207a. It is preferable to form the conductive films included in the connection portion 205a using the same materials and the same steps as an electrode or a wiring used for a display portion or a driver circuit portion in such a manner because an increase in number of steps can be prevented.

[0081]

15 A substrate 261 is provided with the coloring film 241, the light-blocking film 243, and an insulating film 245. FIG. 1B illustrates an example in which the substrate 261 has a smaller thickness than the substrate 211; however, one embodiment of the present invention is not limited to this example. One of the substrates 261 and 211 may be thinner than the other, or the substrates 261 and 211 may have the same thickness. It is preferable to make the substrate on the display surface side (the side near a sensing target) thin because the detection sensitivity of a sensor element can be increased.

[0082]

The coloring film 241 partly overlaps with the liquid crystal element 207a. The light-blocking film 243 partly overlaps with at least one of the transistors 201a and 203a.

25 [0083]

The insulating film 245 preferably has a function of an overcoat preventing impurities contained in the coloring film 241, the light-blocking film 243, and the like from diffusing into the liquid crystal 249. The insulating film 245 is not necessarily provided.

[0084]

30 Note that an alignment film in contact with the liquid crystal 249 may be provided. The alignment film can control the alignment of the liquid crystal 249. For example, in FIG. 1B, an alignment film may be formed to cover the conductive film 252 or may be formed between the insulating film 245 and the liquid crystal 249. The insulating film 245 may serve as an alignment film and an overcoat.

35 [0085]

The input/output device 300 includes a spacer 247. The spacer 247 has a function of preventing the distance between the substrate 211 and the substrate 261 from being shorter than or equal to a certain distance.

[0086]

FIG. 1B illustrates an example in which the spacer 247 is provided over the insulating film 253 and the conductive film 252; however, one embodiment of the present invention is not limited thereto. The spacer 247 may be provided on the substrate 211 side or on the substrate 261 side. For example, the spacer 247 may be formed on the insulating film 245. Moreover, although FIG. 1B illustrates an example in which the spacer 247 is in contact with the insulating films 253 and 245, the spacer 247 is not necessarily in contact with a component provided on the substrate 211 side or on the substrate 261 side.

[0087]

A particulate spacer may be used as the spacer 247. Although a material such as silica can be used for the particulate spacer, an elastic material such as a resin or rubber is preferably used. In that case, the particulate spacer may be vertically crushed.

[0088]

The substrates 211 and 261 are attached to each other with a bonding layer 265. A region surrounded by the substrate 211, the substrate 261, and the bonding layer 265 is filled with the liquid crystal 249.

[0089]

Note that when the input/output device 300 serves as a transmissive liquid crystal display device, two polarizing plates are provided so that a display portion is sandwiched between the two polarizing plates. Light from a backlight provided outside the polarizing plate enters through the polarizing plate. At this time, the alignment of the liquid crystal 249 is controlled with a voltage applied between the conductive films 251 and 252, whereby optical modulation of light can be controlled. In other words, the intensity of light emitted through the polarizing plate can be controlled. Light excluding light in a particular wavelength range is absorbed by the coloring film 241, so that red, blue, or green light is emitted.

[0090]

In addition to the polarizing plate, a circularly polarizing plate can be used, for example. As the circularly polarizing plate, for example, a stack including a linear polarizing plate and a quarter-wave retardation plate can be used. With the circularly polarizing plate, the viewing angle dependence of display of the input/output device can be reduced.

[0091]

Note that the liquid crystal element 207a is an element using an FFS mode here;

however, one embodiment of the present invention is not limited thereto, and a liquid crystal element using any of a variety of modes can be used. For example, a liquid crystal element using a vertical alignment (VA) mode, a twisted nematic (TN) mode, an in-plane switching (IPS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optically compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

[0092]

Furthermore, a normally black liquid crystal display device, for example, a transmissive liquid crystal display device using a vertical alignment (VA) mode, may be used as the input/output device 300. As a vertical alignment mode, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, or an ASV mode can be employed, for example.

[0093]

Note that the liquid crystal element is an element that controls transmission or non-transmission of light by utilizing an optical modulation action of liquid crystal. Note that optical modulation action of a liquid crystal is controlled by an electric field applied to the liquid crystal (including a horizontal electric field, a vertical electric field, and an oblique electric field). As the liquid crystal used for the liquid crystal element, thermotropic liquid crystal, low-molecular liquid crystal, high-molecular liquid crystal, polymer dispersed liquid crystal (PDLC), ferroelectric liquid crystal, anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

[0094]

As the liquid crystal material, a positive liquid crystal or a negative liquid crystal may be used, and an appropriate liquid crystal material can be used depending on the mode and design to be used.

[0095]

Alternatively, in the case of employing a horizontal electric field mode, a liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which 5 weight% or more of a chiral material is mixed is used for the liquid crystal 249 in order to increase the temperature range. The liquid crystal composition that includes liquid crystal exhibiting a blue phase and a chiral material has a short response time and has optical isotropy.

In addition, the liquid crystal composition that includes liquid crystal exhibiting a blue phase and a chiral material does not need alignment treatment and has a small viewing angle dependence. In addition, since an alignment film does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects or damage of the liquid crystal display device in the manufacturing process can be reduced.

[0096]

A substrate with which a sensing target, such as a finger or a stylus, is to be in contact may be provided above the substrate 261. In that case, a polarizing plate or a circularly polarizing plate is preferably provided between the substrate 261 and the above substrate. In that case, a protective layer (such as a ceramic coat) is preferably provided over the above substrate. The protective layer can be formed using an inorganic insulating material such as silicon oxide, aluminum oxide, yttrium oxide, or yttria-stabilized zirconia (YSZ). Alternatively, tempered glass may be used for the substrate. Physical or chemical processing by an ion exchange method, a wind tempering method, or the like is performed on the tempered glass, so that compressive stress is applied on the surface.

[0097]

FIG. 2A is a cross-sectional view of two adjacent pixels. Two subpixels illustrated in FIG. 2A are included in respective pixels.

[0098]

In the input/output device of FIG. 2A, capacitance formed between the conductive film 252 in the left subpixel and the conductive film 252 in the right subpixel is utilized to sense proximity, touch, or the like of a sensing target. That is, in the input/output device of one embodiment of the present invention, the conductive film 252 serves as a common electrode of the liquid crystal element and an electrode of the sensor element.

[0099]

As described above, an electrode included in the liquid crystal element also serves as an electrode included in the sensor element in the input/output device of one embodiment of the present invention; thus, the manufacturing process can be simplified and the manufacturing cost can be reduced. In addition, the thickness and weight of the input/output device can be reduced.

[0100]

The conductive film 252 is electrically connected to the conductive film 255 serving as an auxiliary wiring. With the conductive film 255, the resistance of the electrode of the sensor element can be lowered. With the lowered resistance of the electrode of the sensor element, the

time constant of the electrode of the sensor element can be small. The smaller the time constant of the electrode of the sensor element is, the higher the detection sensitivity and the detection accuracy are.

[0101]

When the capacitance between the electrode of the sensor element and a signal line is too large, the time constant of the electrode of the sensor element becomes too large in some cases. Thus, an insulating film having a planarizing function is preferably provided between the electrode of the sensor element and the transistors to reduce the capacitance between the electrode of the sensor element and the signal line. For example, in FIG. 2A, as the insulating film having a planarizing function, the insulating film 219 is provided. With the insulating film 219, the capacitance between the conductive film 252 and the signal line can be small. Accordingly, the time constant of the electrode of the sensor element can be small. As described above, the smaller the time constant of the electrode of the sensor element is, the higher the detection sensitivity and the detection accuracy are.

[0102]

For example, the time constant of the electrode of the sensor element is greater than 0 seconds and smaller than or equal to 1×10^{-4} seconds, preferably greater than 0 seconds and smaller than or equal to 5×10^{-5} seconds, more preferably greater than 0 seconds and smaller than or equal to 5×10^{-6} seconds, more preferably greater than 0 seconds and smaller than or equal to 5×10^{-7} seconds, more preferably greater than 0 seconds and smaller than or equal to 2×10^{-7} seconds. In particular, when the time constant is smaller than or equal to 1×10^{-6} seconds, high detection sensitivity can be achieved while the influence of noise is reduced.

[0103]

[Cross-sectional structure example 2 of input/output device]

FIG. 2B is a cross-sectional view of two adjacent pixels that are different from those in FIG. 2A. Two subpixels illustrated in FIG. 2B are included in respective pixels. FIG. 3A is a cross-sectional view of this case taken along dashed-dotted lines A-B and C-D in FIG. 1A.

[0104]

Structure example 2 illustrated in FIG. 2B and FIG. 3A differs from Structure example 1 illustrated in FIGS. 1B and 2A in the stacking order of the conductive film 251, the conductive film 252, the insulating film 253, and the conductive film 255. Note that in Structure example 2, the above description can be referred to for portions similar to Structure example 1.

[0105]

Specifically, in Structure example 2, the conductive film 255 is over the insulating film 219, the conductive film 252 is over the conductive film 255, the insulating film 253 is over the

conductive film 252, and the conductive film 251 is over the insulating film 253.

[0106]

As illustrated in a liquid crystal element 207b of FIG. 2B, the conductive film 251 which is provided on the upper side and whose top surface shape is a comb-like shape or has a slit may serve as a pixel electrode, and the conductive film 252 provided on the lower side may serve as a common electrode. The conductive film 251 is electrically connected to the source or the drain of the transistor 203a.

[0107]

In FIG. 2B, capacitance formed between the conductive film 252 in the left subpixel and the conductive film 252 in the right subpixel is utilized to sense proximity, touch, or the like of a sensing target. That is, in the input/output device of one embodiment of the present invention, the conductive film 252 serves as the common electrode of the liquid crystal element and the electrode of the sensor element.

[0108]

Note that in Structure example 1 (FIGS. 1B and 2A), the conductive film 252 serving as the electrode of the sensor element and the common electrode is closer to the display surface side (the side near a sensing target) than the conductive film 251 serving as the pixel electrode is. Thus, in some cases, the detection sensitivity of Structure example 1 is higher than that of Structure example 2 in which the conductive film 251 is closer to the display surface side than the conductive film 252 is.

[0109]

Moreover, the connection portion of Structure example 2 also differs from that of Structure example 1 because the stacking order of the conductive film 251, the conductive film 252, the insulating film 253, and the conductive film 255 of Structure example 2 is different from that of Structure example 1.

[0110]

A connection portion 205b illustrated in FIG. 3A includes the conductive film 231 over the insulating film 213, the conductive film 233 over the conductive film 231, and the conductive film 235 over the conductive film 233. The conductive film 233 can be formed using the same material and the same step as those of the conductive film 252 included in the liquid crystal element 207b. The conductive film 235 can be formed using the same material and the same step as those of the conductive film 251 included in the liquid crystal element 207b.

[0111]

FIGS. 3B and 3C illustrate other structure examples of the transistor included in the input/output device of one embodiment of the present invention. As illustrated in a transistor

having two gates of FIG. 3B, the two gates are not necessarily electrically connected to each other. As illustrated in FIG. 3C, a top-gate transistor may be included in at least one of the driver circuit portion and the display portion.

[0112]

5 FIGS. 3D to 3F illustrate other structure examples of the liquid crystal element included in the input/output device of one embodiment of the present invention. Both of the conductive films 251 and 252 may have a comb-like top surface shape or a top surface shape provided with a slit (a top surface shape is also referred to as a planar surface shape).

[0113]

10 For example, when seen from the top, an end portion of a slit of one conductive film may overlap with an end portion of a slit of the other conductive film. A cross-sectional view of this case is illustrated in FIG. 3D.

[0114]

15 Alternatively, when seen from the top, a portion where the conductive films 251 and 252 are not provided may exist. A cross-sectional view of this case is illustrated in FIG. 3E.

[0115]

 Further alternatively, when seen from the top, the conductive films 251 and 252 may overlap with each other partly. A cross-sectional view of this case is illustrated in FIG. 3F.

[0116]

20 [Cross-sectional structure example 3 of input/output device]

 FIG. 4 is a cross-sectional view taken along dashed-dotted lines A-B and C-D in FIG. 1A that is different from the cross-sectional views of FIG. 1B and FIG. 3A.

[0117]

25 The structures of the transistors included in the display portion 301 and in the scan line driver circuit 302 of Structure example 3 in FIG. 4 differ from those of Structure example 1 in FIGS. 1B and 2A. Note that in Structure example 3, the above description can be referred to for portions similar to Structure example 1.

[0118]

30 A transistor 201b has a structure in which an oxide semiconductor film where a channel is formed is sandwiched between two gates. The transistor 201b differs from the transistor 201a in that the gate electrode 221 is directly in contact with the oxide conductor film 227. Like this, two gates may be electrically connected to each other with no layer interposed therebetween.

[0119]

35 Like the transistor 201b, a transistor 203b has a structure in which the oxide

semiconductor film 223 where a channel is formed is sandwiched between two gates. Like this, a transistor having two gates may be applied not only in the driver circuit portion but also in the display portion. Note that although not illustrated, also in the transistor 203b, the gate electrode 221 is preferably electrically connected to the oxide conductor film 227.

5 [0120]

Note that the shorter the distance between the oxide conductor film 227 and the electrode of the sensor element is, the more a problem of changing the potential of the electrode of the sensor element due to an influence of the oxide conductor film 227 is caused. In one embodiment of the present invention, the oxide conductor film 227 and the electrode of the sensor element are formed in different layers. This is preferable because the electrode of the sensor element is not easily affected by the oxide conductor film 227.

[0121]

[Cross-sectional structure example 4 of input/output device]

FIG. 5 is a cross-sectional view taken along dashed-dotted lines A-B and C-D in FIG. 1A that is different from the cross-sectional views of FIG. 1B, FIG. 3A, and FIG. 4.

[0122]

Structure example 4 in FIG. 5 differs from Structure example 1 in FIGS. 1B and 2A in the structure of the transistor in the scan line driver circuit 302 and in the substrate provided with the spacer 247. Note that in Structure example 4, the above description can be referred to for portions similar to Structure example 1.

[0123]

A transistor 201c has a structure in which an oxide semiconductor film where a channel is formed is sandwiched between two gates. The transistor 201c differs from the transistor 201a in the formation position of the oxide conductor film 227. Specifically, the insulating film 217 is over the insulating film 215, an insulating film 218 having a planarizing function is over the insulating film 217, and the oxide conductor film 227 is over the insulating film 218. As described above, the oxide conductor film 227 may be formed over an insulating film having a planarizing function. The transistor 201c is covered with the insulating film 219 having a planarizing function. Note that FIG. 5 illustrates an example in which the oxide conductor film 227 is electrically connected to the gate electrode 221 via the conductive film 226; however, as illustrated in FIG. 4, the oxide conductor film 227 may be directly in contact with the gate electrode 221.

[0124]

Furthermore, FIG. 5 illustrates an example in which the spacer 247 is provided on the insulating film 245. Like this, the spacer 247 may be arranged on the substrate 261 side.

[0125]

[Cross-sectional structure example 5 of input/output device]

FIG. 6 is a cross-sectional view taken along dashed-dotted lines A-B and C-D in FIG. 1A that is different from the cross-sectional views of FIG. 1B, FIG. 3A, FIG. 4, and FIG. 5.

[0126]

Structure example 5 in FIG. 6 differs from Structure example 1 in FIGS. 1B and 2A in the position of the coloring film 241. Note that in Structure example 5, the above description can be referred to for portions similar to Structure example 1.

[0127]

The coloring film 241 is not necessarily formed on the counter substrate (the substrate 261) side. As illustrated in FIG. 6, the coloring film 241 may be formed over the substrate 211 provided with the transistors and the like. Accordingly, a decrease in yield and display quality caused by a decrease in alignment accuracy of the substrates 211 and 261 due to an increase in resolution of the display of the input/output device can be suppressed.

[0128]

[Cross-sectional structure example 6 of input/output device]

FIG. 34 is a cross-sectional view of an input/output device that is different from the input/output devices in the above-described structure examples. The input/output device of one embodiment of the present invention is not limited to a full-in-cell touch panel in which an electrode and the like included in a sensor element are provided only over a substrate supporting a display element. As illustrated in the input/output device of FIG. 34, an electrode included in a sensor element may be provided on a counter substrate side.

[0129]

FIG. 34 illustrates an example in which a conductive film 254 is formed over a surface of the substrate 261 that is opposite to a surface on which the coloring film 241 and the like are formed. The conductive film 254 is electrically connected to an FPC 259 via a connector 257. In the input/output device 300 of FIG. 34, capacitance formed between the conductive film 252 and the conductive film 254 is utilized to sense proximity, touch, or the like of a sensing target. That is, in the input/output device of one embodiment of the present invention, the conductive film 252 serves as the common electrode of the liquid crystal element and one electrode of the sensor element. In this manner, the common electrode of the liquid crystal element may serve as the one electrode or a pair of electrodes of the sensor element.

[0130]

Furthermore, FIG. 34 illustrates an example in which the conductive film 255 is formed over the conductive film 252. The electrode of the liquid crystal element may be over or under

a conductive film that can serve as an auxiliary wiring of the electrode.

[0131]

Next, the details of the materials and the like that can be used for components of the input/output device of this embodiment are described. Note that description on the components already described is omitted in some cases. The materials described below can be used for the input/output device described in a later embodiment and its components.

[0132]

<<Substrate>>

There is no particular limitation on a material and the like of the substrates included in the input/output device 300 as long as the material has heat resistance high enough to withstand at least heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like may be used as the substrates. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon or silicon carbide, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like may be used. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate. Furthermore, any of these substrates further provided with a semiconductor element may be used as the substrate. In the case where a glass substrate is used as the substrate, a glass substrate having any of the following sizes can be used: the 6th generation (1500 mm × 1850 mm), the 7th generation (1870 mm × 2200 mm), the 8th generation (2200 mm × 2400 mm), the 9th generation (2400 mm × 2800 mm), and the 10th generation (2950 mm × 3400 mm). Thus, a large-sized display device can be manufactured. Alternatively, a flexible substrate may be used as the substrate 211, and the transistor, the capacitor, and the like may be formed directly on the flexible substrate.

[0133]

The weight and thickness of the input/output device can be reduced by using a thin substrate. Furthermore, a flexible input/output device can be obtained by using a substrate that is thin enough to have flexibility.

[0134]

Other than the above, a transistor can be formed using various substrates as the substrates 211 and 261. The type of a substrate is not limited to a certain type. Examples of the substrate include a plastic substrate, a metal substrate, a stainless steel substrate, a substrate including stainless steel foil, a tungsten substrate, a substrate including tungsten foil, a flexible substrate, an attachment film, paper including a fibrous material, and a base film. As an example of a glass substrate, a barium borosilicate glass substrate, an aluminoborosilicate glass substrate, a soda lime glass substrate, or the like can be given. Examples of a flexible substrate

include a flexible synthetic resin such as plastics typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyether sulfone (PES), and acrylic. Examples of an attachment film are attachment films formed using polypropylene, polyester, polyvinyl fluoride, polyvinyl chloride, and the like. Examples of the material for the base film include polyester, polyamide, polyimide, inorganic vapor deposition film, and paper. Specifically, the use of semiconductor substrates, single crystal substrates, SOI substrates, or the like enables the manufacture of small-sized transistors with a small variation in characteristics, size, shape, or the like and with high current capability. A circuit using such transistors achieves lower power consumption of the circuit or higher integration of the circuit.

[0135]

Note that a transistor may be formed using one substrate, and then the transistor may be transferred to another substrate. Examples of a substrate to which a transistor is transferred include, in addition to the above substrate over which the transistor can be formed, a paper substrate, a cellophane substrate, a stone substrate, a wood substrate, a cloth substrate (including a natural fiber (e.g., silk, cotton, or hemp), a synthetic fiber (e.g., nylon, polyurethane, or polyester), a regenerated fiber (e.g., acetate, cupra, rayon, or regenerated polyester), and the like), a leather substrate, and a rubber substrate. When such a substrate is used, a transistor with excellent properties or a transistor with low power consumption can be formed, a device with high durability or high heat resistance can be provided, or reduction in weight or thickness can be achieved.

[0136]

<<Transistor>>

The structure of the transistors in the input/output device of one embodiment of the present invention is not particularly limited. For example, a planar transistor, a staggered transistor, or an inverted staggered transistor may be used. A top-gate transistor or a bottom-gate transistor may be used. Gate electrodes may be provided above and below a channel. A semiconductor material used for the transistor is not particularly limited, and for example, an oxide semiconductor, silicon, or germanium can be used.

[0137]

There is no particular limitation on the crystallinity of a semiconductor material used for the transistor either, and an amorphous semiconductor or a semiconductor having crystallinity (a microcrystalline semiconductor, a polycrystalline semiconductor, a single-crystal semiconductor, or a semiconductor partly including crystal regions) may be used. It is preferable that a semiconductor having crystallinity be used, in which case deterioration of the transistor characteristics can be suppressed.

[0138]

As a semiconductor material for the semiconductor layer of the transistor, an element of Group 14, a compound semiconductor, or an oxide semiconductor can be used, for example. Typically, a semiconductor containing silicon, a semiconductor containing gallium arsenide, an oxide semiconductor containing indium, or the like can be used.

[0139]

An oxide semiconductor is preferably used as a semiconductor in which a channel of the transistor is formed. In particular, an oxide semiconductor having a wider band gap than silicon is preferably used. A semiconductor material having a wider band gap and a lower carrier density than silicon is preferably used because the off-state current of the transistor can be reduced.

[0140]

For example, it is preferable that the oxide semiconductor contain at least indium (In) or zinc (Zn). It is further preferable that the oxide semiconductor contains an oxide represented by an In-*M*-Zn oxide (*M* is a metal such as Al, Ti, Ga, Ge, Y, Zr, La, Ce, Sn, Mg, Nd, or Hf).

[0141]

As the semiconductor layer, it is particularly preferable to use an oxide semiconductor film including a plurality of crystal parts whose c-axes are aligned substantially perpendicular to a surface on which the semiconductor layer is formed or the top surface of the semiconductor layer and having no grain boundary between adjacent crystal parts.

[0142]

There is no grain boundary in such an oxide semiconductor; therefore, generation of a crack in an oxide semiconductor film that is caused by stress when a display panel is bent is prevented. Therefore, such an oxide semiconductor can be preferably used for a flexible input/output device that is used in a bent state, or the like.

[0143]

Moreover, the use of such an oxide semiconductor for the semiconductor layer makes it possible to provide a highly reliable transistor in which a variation in electrical characteristics is suppressed.

[0144]

Charge accumulated in a capacitor through a transistor can be held for a long time because of the low off-state current of the transistor. When such a transistor is used for a pixel, operation of a driver circuit can be stopped while a gray scale of an image displayed in each display region is maintained. As a result, a display device with an extremely low power consumption can be obtained.

[0145]

<<Oxide semiconductor film>>

It is preferable that the oxide semiconductor film 223 includes a film represented by an In-*M*-Zn oxide that contains, for example, at least indium (In), zinc (Zn), and *M* (a metal such as Al, Ti, Ga, Ge, Y, Zr, La, Ce, Sn, Mg, Nd, or Hf). In order to reduce variations in electrical characteristics of the transistor including the oxide semiconductor, the oxide semiconductor preferably contains a stabilizer in addition to the above elements.

[0146]

Examples of the stabilizer, including metals that can be used as *M*, are gallium (Ga), tin (Sn), hafnium (Hf), aluminum (Al), and zirconium (Zr). Other examples of the stabilizer are lanthanoid such as lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), and lutetium (Lu).

[0147]

As an oxide semiconductor included in the oxide semiconductor film 223, any of the following oxides can be used, for example: an In-Ga-Zn-based oxide, an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, an In-Hf-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, an In-Lu-Zn-based oxide, an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, and an In-Hf-Al-Zn-based oxide.

[0148]

Note that here, an "In-Ga-Zn-based oxide" means an oxide containing In, Ga, and Zn as its main components, and there is no limitation on the ratio of In:Ga:Zn. The In-Ga-Zn-based oxide may contain another metal element in addition to In, Ga, and Zn.

[0149]

Note that in the case where the oxide semiconductor film 223 includes an In-*M*-Zn oxide, when the summation of In and *M* is assumed to be 100 atomic%, the atomic proportions of In and *M* are preferably higher than 25 atomic% and lower than 75 atomic%, respectively, more preferably higher than 34 atomic% and lower than 66 atomic%, respectively.

[0150]

The energy gap of the oxide semiconductor film 223 is 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more. In this manner, the off-state current of the transistor

can be reduced by using an oxide semiconductor having a wide energy gap.

[0151]

The thickness of the oxide semiconductor film 223 is greater than or equal to 3 nm and less than or equal to 200 nm, preferably greater than or equal to 3 nm and less than or equal to 100 nm, more preferably greater than or equal to 3 nm and less than or equal to 50 nm.

[0152]

In the case where the oxide semiconductor film 223 includes an In-*M*-Zn oxide (*M* is Al, Ti, Ga, Ge, Y, Zr, La, Ce, Sn, Mg, Nd, or Hf), it is preferable that the atomic ratio of metal elements of a sputtering target used for forming a film of the In-*M*-Zn oxide satisfy $\text{In} \geq M$ and $\text{Zn} \geq M$. As the atomic ratio of the metal elements of such a sputtering target, In:M:Zn = 1:1:1, In:M:Zn = 1:1:1.2, In:M:Zn = 3:1:2, In:M:Zn = 1:3:4, In:M:Zn = 1:3:6, and the like are given. Note that the atomic ratio of metal elements in the formed oxide semiconductor film 223 varies from the above atomic ratio of metal elements of the sputtering target within a range of $\pm 40\%$ as an error.

[0153]

An oxide semiconductor film with a low carrier density is used as the oxide semiconductor film 223. For example, an oxide semiconductor film whose carrier density is lower than or equal to $1 \times 10^{17} / \text{cm}^3$, preferably lower than or equal to $1 \times 10^{15} / \text{cm}^3$, more preferably lower than or equal to $1 \times 10^{13} / \text{cm}^3$, more preferably lower than or equal to $1 \times 10^{11} / \text{cm}^3$ is used as the oxide semiconductor film 223.

[0154]

Note that, without limitation to those described above, a material with an appropriate composition can be used depending on required semiconductor characteristics and electrical characteristics (e.g., field-effect mobility and threshold voltage) of the transistor. Furthermore, to obtain required semiconductor characteristics of the transistor, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like of the oxide semiconductor film 223 be set to be appropriate.

[0155]

When silicon or carbon that is one of elements belonging to Group 14 is contained in the oxide semiconductor film 223, oxygen vacancies are increased, and the oxide semiconductor film 223 has n-type conductivity. Thus, the concentration of silicon or carbon (measured by secondary ion mass spectrometry (SIMS)) of the oxide semiconductor film 223 is lower than or equal to $2 \times 10^{18} \text{ atoms/cm}^3$, preferably lower than or equal to $2 \times 10^{17} \text{ atoms/cm}^3$.

[0156]

Furthermore, the concentration of alkali metal or alkaline earth metal in the oxide semiconductor film 223, which is measured by SIMS, is lower than or equal to 1×10^{18} atoms/cm³, preferably lower than or equal to 2×10^{16} atoms/cm³. Alkali metal and alkaline earth metal might generate carriers when bonded to an oxide semiconductor, in which case the off-state current of the transistor might be increased. Therefore, it is preferable to reduce the concentration of alkali metal or alkaline earth metal in the oxide semiconductor film 223.

[0157]

When nitrogen is contained in the oxide semiconductor film 223, electrons serving as carriers are generated to increase the carrier density, so that the oxide semiconductor film 223 easily has n-type conductivity. Thus, a transistor including an oxide semiconductor that contains nitrogen is likely to be normally on. For this reason, nitrogen in the oxide semiconductor film is preferably reduced as much as possible; the concentration of nitrogen that is measured by SIMS is preferably set to, for example, lower than or equal to 5×10^{18} atoms/cm³.

[0158]

The oxide semiconductor film 223 may have a non-single-crystal structure, for example. The non-single-crystal structure includes a c-axis aligned crystalline oxide semiconductor (CAAC-OS) that is described later, a polycrystalline structure, a microcrystalline structure that is described later, or an amorphous structure, for example. Among the non-single-crystal structures, an amorphous structure has the highest density of defect states, whereas CAAC-OS has the lowest density of defect states.

[0159]

The oxide semiconductor film 223 may have an amorphous structure, for example. An oxide semiconductor film having an amorphous structure has disordered atomic arrangement and no crystalline component, for example. Alternatively, an oxide film having an amorphous structure has, for example, an absolutely amorphous structure and no crystal part.

[0160]

Note that the oxide semiconductor film 223 may be a mixed film including two or more of the following: a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a region of CAAC-OS, and a region having a single-crystal structure. The mixed film has a single-layer structure including, for example, two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure in some cases. Furthermore, the mixed film has a stacked-layer structure of two or more of the following in some cases: the region having an amorphous

structure, the region having a microcrystalline structure, the region having a polycrystalline structure, the region of CAAC-OS, and the region having a single-crystal structure.

[0161]

Alternatively, silicon is preferably used as a semiconductor in which a channel of the transistor is formed. Although amorphous silicon may be used as silicon, silicon having crystallinity is particularly preferable. For example, microcrystalline silicon, polycrystalline silicon, single crystal silicon, or the like is preferably used. In particular, polycrystalline silicon can be formed at a lower temperature than single crystal silicon and has a higher field-effect mobility and a higher reliability than amorphous silicon. When such a polycrystalline semiconductor is used for a pixel, the aperture ratio of the pixel can be improved. Even in the case where an extremely high resolution input/output device is manufactured, a gate driver circuit and a source driver circuit can be formed over a substrate over which the pixels are formed, and the number of components of an electronic device can be reduced.

[0162]

<<Method for controlling resistivity of oxide semiconductor>>

An oxide semiconductor is a semiconductor material whose resistance can be controlled by oxygen vacancies in the film and/or the concentration of impurities such as hydrogen or water in the film. Thus, the resistivity of the oxide conductor film can be controlled by selecting treatment for increasing oxygen vacancies and/or impurity concentration on the oxide semiconductor film or treatment for reducing oxygen vacancies and/or impurity concentration on the oxide semiconductor film.

[0163]

Note that such an oxide conductor film formed using an oxide semiconductor film can be referred to as an oxide semiconductor film having a high carrier density and a low resistance, an oxide semiconductor film having conductivity, or an oxide semiconductor film having high conductivity.

[0164]

Specifically, plasma treatment is performed on an oxide semiconductor film to be the oxide conductor film 227 serving as a gate to increase oxygen vacancies and/or impurities such as hydrogen or water in the oxide semiconductor film; accordingly, the oxide semiconductor film can have a high carrier density and a low resistance. Alternatively, the insulating film 217 containing hydrogen is formed in contact with the oxide semiconductor film to diffuse hydrogen from the insulating film 217 containing hydrogen to the oxide semiconductor film, so that the oxide semiconductor film can have a high carrier density and a low resistance.

[0165]

The insulating film 215 is formed over the oxide semiconductor film 223 so that the oxide semiconductor film 223 is not subjected to the above plasma treatment. Since the insulating film 215 is provided, the oxide semiconductor film 223 is not in contact with the insulating film 217 containing hydrogen. The insulating film 215 can be formed using an insulating film capable of releasing oxygen, in which case oxygen can be supplied to the oxide semiconductor film 223. The oxide semiconductor film 223 to which oxygen is supplied is an oxide semiconductor in which oxygen vacancies in the film or at the interface are reduced and which has a high resistance. Note that as the insulating film capable of releasing oxygen, a silicon oxide film or a silicon oxynitride film can be used, for example.

[0166]

To obtain an oxide semiconductor film having a low resistivity, hydrogen, boron, phosphorus, or nitrogen may be introduced into the oxide semiconductor film by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like.

[0167]

As the plasma treatment to be performed on the oxide conductor film 227, plasma treatment using a gas containing one of a rare gas (He, Ne, Ar, Kr, or Xe), phosphorus, boron, hydrogen, and nitrogen is typical. Specifically, plasma treatment in an Ar atmosphere, plasma treatment in a mixed gas atmosphere of Ar and hydrogen, plasma treatment in an ammonia atmosphere, plasma treatment in a mixed gas atmosphere of Ar and ammonia, plasma treatment in a nitrogen atmosphere, or the like can be employed.

[0168]

By the plasma treatment, an oxygen vacancy is formed in a lattice from which oxygen is released (or in a portion from which oxygen is released) in the oxide conductor film 227. This oxygen vacancy can cause carrier generation. Furthermore, when hydrogen is supplied from an insulating film that is in the vicinity of the oxide conductor film 227, specifically, that is in contact with the lower surface or the upper surface of the oxide conductor film 227, and hydrogen enters the oxygen vacancy, an electron serving as a carrier might be generated. Accordingly, the oxide conductor film 227 whose oxygen vacancies are increased by the plasma treatment has a higher carrier density than the oxide semiconductor film 223.

[0169]

The oxide semiconductor film 223 in which oxygen vacancies are reduced and the hydrogen concentration is reduced can be referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film. The term "substantially intrinsic" refers to the state where an oxide semiconductor has a carrier density lower than $1 \times$

$10^{17} / \text{cm}^3$, preferably lower than $1 \times 10^{15} / \text{cm}^3$, further preferably lower than $1 \times 10^{13} / \text{cm}^3$. Furthermore, the state in which an impurity concentration is low and the density of defect states is low (the amount of oxygen vacancies is small) is referred to as "highly purified intrinsic" or "substantially highly purified intrinsic". A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier generation sources, and thus has a low carrier density in some cases. Thus, a transistor including the oxide semiconductor film in which a channel region is formed is likely to have positive threshold voltage (normally-off characteristics). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film 223 has a low density of defect states and accordingly can have a low density of trap states.

[0170]

Furthermore, the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film 223 has an extremely low off-state current; even when an element has a channel width of $1 \times 10^6 \mu\text{m}$ and a channel length of $10 \mu\text{m}$, the off-state current can be less than or equal to the measurement limit of a semiconductor parameter analyzer, i.e., less than or equal to $1 \times 10^{-13} \text{ A}$, at a voltage (drain voltage) between a source electrode and a drain electrode of from 1 V to 10 V. Thus, the transistor whose channel region is formed in the oxide semiconductor film 223 has a small variation in electrical characteristics and high reliability.

[0171]

For example, an insulating film containing hydrogen, that is, an insulating film capable of releasing hydrogen, typically, a silicon nitride film, is used as the insulating film 217, whereby hydrogen can be supplied to the oxide conductor film 227. The insulating film capable of releasing hydrogen preferably has a hydrogen concentration of $1 \times 10^{22} \text{ atoms/cm}^3$ or higher. Such an insulating film is formed in contact with the oxide conductor film 227, whereby hydrogen can be effectively contained in the oxide conductor film 227. In this manner, the above-described plasma treatment is performed and the structure of the insulating film in contact with the oxide semiconductor film (or the oxide conductor film) is changed, whereby the resistance of the oxide semiconductor film (or the oxide conductor film) can be appropriately adjusted.

[0172]

Hydrogen contained in the oxide conductor film 227 reacts with oxygen bonded to a metal atom to be water, and in addition, an oxygen vacancy is formed in a lattice from which oxygen is released (or a portion from which oxygen is released). Due to entry of hydrogen into the oxygen vacancy, an electron serving as a carrier is generated in some cases. Furthermore, in some cases, bonding of part of hydrogen to oxygen bonded to a metal atom causes generation of

an electron serving as a carrier. Thus, the oxide conductor film 227 containing hydrogen has a higher carrier density than the oxide semiconductor film 223.

[0173]

Hydrogen in the oxide semiconductor film 223 of the transistor in which a channel region is formed is preferably reduced as much as possible. Specifically, in the oxide semiconductor film 223, the concentration of hydrogen that is measured by SIMS is set to 2×10^{20} atoms/cm³ or lower, preferably 5×10^{19} atoms/cm³ or lower, more preferably 1×10^{19} atoms/cm³ or lower, more preferably 5×10^{18} atoms/cm³ or lower, preferably 1×10^{18} atoms/cm³ or lower, more preferably 5×10^{17} atoms/cm³ or lower, still more preferably 1×10^{16} atoms/cm³ or lower.

[0174]

On the other hand, the oxide conductor film 227 serving as a gate is a low-resistance oxide conductor film having a high hydrogen concentration and/or a large amount of oxygen vacancies as compared to the oxide semiconductor film 223.

[0175]

A material that can be used for the oxide semiconductor film 223 and a method for forming the oxide semiconductor film 223 can be applied to those for the oxide conductor film 227. Note that the oxide semiconductor film 223 and the oxide conductor film 227 have a light-transmitting property.

[0176]

Note that a material that can be used for the oxide conductor film 227 and a method for forming the oxide conductor film 227 can be applied to those for the conductive films 251 and 252.

[0177]

<<Insulating film>>

An organic insulating material or an inorganic insulating material can be used as an insulating material that can be used for the insulating film, the overcoat, the spacer, or the like included in the input/output device. Examples of a resin include an acrylic resin, an epoxy resin, a polyimide resin, a polyamide resin, a polyamide-imide resin, a siloxane resin, a benzocyclobutene-based resin, and a phenol resin. Examples of an inorganic insulating film include a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film.

[0178]

<<Conductive film>>

For the conductive film such as the gate, the source, and the drain of a transistor and the wiring, the electrode, and the like of the input/output device, a single-layer structure or a stacked structure using any of metals such as aluminum, titanium, chromium, nickel, copper, yttrium, zirconium, molybdenum, silver, tantalum, and tungsten, or an alloy containing any of these metals as its main component can be used. For example, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a tungsten film, a two-layer structure in which a copper film is stacked over a molybdenum film, a two-layer structure in which a copper film is stacked over an alloy film containing molybdenum and tungsten, a two-layer structure in which a copper film is stacked over a copper-magnesium-aluminum alloy film, a three-layer structure in which a titanium film or a titanium nitride film, an aluminum film or a copper film, and a titanium film or a titanium nitride film are stacked in this order, a three-layer structure in which a molybdenum film or a molybdenum nitride film, an aluminum film or a copper film, and a molybdenum film or a molybdenum nitride film are stacked in this order, and the like can be given. For example, in the case where the source electrode 225a and the drain electrode 225b have a three-layer structure, it is preferable that each of the first and third layers be a film formed of titanium, titanium nitride, molybdenum, tungsten, an alloy containing molybdenum and tungsten, an alloy containing molybdenum and zirconium, or molybdenum nitride, and that the second layer be a film formed of a low-resistance material such as copper, aluminum, gold, silver, or an alloy containing copper and manganese. A light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added may be used.

[0179]

Note that the conductive film may be formed using the above-described method for controlling the resistivity of an oxide semiconductor.

[0180]

<<Bonding layer>>

A curable resin such as a thermosetting resin, a photocurable resin, or a two-liquid mixing type curable resin can be used for the bonding layer 265. For example, an acrylic resin, a urethane resin, an epoxy resin, or a resin having a siloxane bond can be used.

[0181]

<<Connector>>

As the connector, anisotropic conductive films (ACF), anisotropic conductive pastes

(ACP), and the like can be used for example.

[0182]

<<Coloring film>>

The coloring film is a colored layer that transmits light in a specific wavelength range.

- 5 Examples of a material that can be used for the coloring film include a metal material, a resin material, and a resin material containing a pigment or dye.

[0183]

<<Light-blocking film>>

- 10 The light-blocking film is provided between adjacent coloring films. For the light-blocking film, for example, a black matrix can be formed using a metal material or a resin material containing pigment or dye. Note that it is preferable to provide the light-blocking film also in a region other than the display portion, such as a driver circuit portion, in which case undesired leakage of guided light or the like can be inhibited.

[0184]

- 15 [Operation example of input/output device]

Next, an operation example and the like of the input/output device of one embodiment of the present invention are described.

[0185]

- 20 FIG. 7A is an equivalent circuit diagram of a pixel circuit provided in the display portion of the input/output device of one embodiment of the present invention.

[0186]

Each pixel includes at least a transistor 3503 and a liquid crystal element 3504. A gate of the transistor 3503 is electrically connected to a wiring 3501. One of a source and a drain of the transistor 3503 is electrically connected to a wiring 3502.

- 25 [0187]

The pixel circuit includes a plurality of wirings extending in the X direction (e.g., a wiring 3510_1 and a wiring 3510_2) and a plurality of wirings extending in the Y direction (e.g., a wiring 3511_1). They are provided to intersect with each other, and capacitance is formed therebetween.

- 30 [0188]

- Among the pixels provided in the pixel circuit, electrodes on one side of the liquid crystal elements of some pixels adjacent to each other are electrically connected to each other to form one block. The block is classified into two types: an island-shaped block (e.g., a block 3515_1 or a block 3515_2) and a linear block extending in the X direction or the Y direction (e.g., a block 3516 extending in the Y direction). Note that only part of the pixel circuit is illustrated
- 35

in FIG. 7A, and actually, these two kinds of blocks are repeatedly arranged in the X direction and the Y direction. An electrode on one side of the liquid crystal element is, for example, a common electrode. An electrode on the other side of the liquid crystal element is, for example, a pixel electrode.

5 [0189]

The wiring 3510_1 (or 3510_2) extending in the X direction is electrically connected to the island-shaped block 3515_1 (or the block 3515_2). Although not illustrated, the wiring 3510_1 extending in the X direction is electrically connected to a plurality of island-shaped blocks 3515_1 that are provided discontinuously along the X direction with the linear blocks
10 therebetween. Furthermore, the wiring 3511_1 extending in the Y direction is electrically connected to the linear block 3516.

[0190]

FIG. 7B is an equivalent circuit diagram illustrating the connection relation between a plurality of wirings extending in the X direction (the wirings 3510_1 to 3510_6 are collectively
15 called a wiring 3510 in some cases) and a plurality of wirings extending in the Y direction (wirings 3511_1 to 3511_6 are collectively called a wiring 3511 in some cases). A common potential can be input to each of the wirings 3510 extending in the X direction and each of the wirings 3511 extending in the Y direction. A pulse voltage can be input to each of the wirings 3510 extending in the X direction from a pulse voltage output circuit. Furthermore, each of the
20 wirings 3511 extending in the Y direction can be electrically connected to the detection circuit. Note that the wiring 3510 and the wiring 3511 can be replaced with each other.

[0191]

An operation example of the input/output device of one embodiment of the present invention is described with reference to FIGS. 8A and 8B.

25 [0192]

Here, one frame period is divided into a writing period and a sensing period. The writing period is a period in which image data is written to a pixel, and the wirings 3501 (also referred to as gate lines or scan lines) are sequentially selected. The sensing period is a period during which sensing is performed by the sensor element.

30 [0193]

FIG. 8A is an equivalent circuit diagram in the writing period. In the wiring period, a common potential is input to both the wiring 3510 extending in the X direction and the wiring 3511 extending in the Y direction.

[0194]

35 FIG. 8B is an equivalent circuit diagram in the sensing period. In the sensing period,

each of the wirings 3511 extending in the Y direction is electrically connected to the detection circuit. Furthermore, a pulse voltage is input to the wirings 3510 extending in the X direction from a pulse voltage output circuit.

[0195]

5 FIG. 8C illustrates an example of a timing chart of the input and output waveforms of a mutual capacitive sensor element.

[0196]

 In FIG. 8C, sensing of a sensing target is performed in all rows and columns in one frame period. FIG. 8C shows two cases in the sensing period: a case in which a sensing target
10 is not sensed (not touched) and a case in which a sensing target is sensed (touched).

[0197]

 A pulse voltage is supplied to the wirings 3510_1 to 3510_6 from the pulse voltage output circuit. When the pulse voltage is applied to the wirings 3510_1 to 3510_6, an electric field is generated between a pair of electrodes forming a capacitor, and current flows in the
15 capacitor. The electric field generated between the electrodes is changed by being blocked by the touch of a finger or a stylus. That is, the capacitance value of the capacitor is changed by touch or the like. By utilizing this, proximity or touch of a sensing target can be sensed.

[0198]

 The wirings 3511_1 to 3511_6 are connected to the detection circuit for detecting the
20 change in current in the wirings 3511_1 to 3511_6 caused by the change in capacitance value of the capacitor. The current value detected in the wirings 3511_1 to 3511_6 is not changed when there is no proximity or touch of a sensing target, and is decreased when the capacitance value is decreased because of the proximity or touch of a sensing target. In order to detect a change in current, the total amount of current may be detected. In that case, an integrator circuit or the
25 like may be used to detect the total amount of current. Alternatively, the peak value of current may be detected. In that case, current may be converted into voltage, and the peak value of voltage may be detected.

[0199]

 Note that the waveforms of the wirings 3511_1 to 3511_6 in FIG. 8C show voltage
30 values corresponding to the detected current values. As shown in FIG. 8C, the timing of the display operation is preferably in synchronization with the timing of the sensing operation.

[0200]

 The waveforms of the wirings 3511_1 to 3511_6 change in accordance with pulse voltages applied to the wirings 3510_1 to 3510_6. When there is no proximity or touch of a

sensing target, the waveforms of the wirings 3511_1 to 3511_6 uniformly change in accordance with changes in the voltages of the wirings 3510_1 to 3510_6. The current value is decreased at the point of proximity or touch of a sensing target and accordingly the waveform of the voltage value also changes.

5 [0201]

By detecting a change in capacitance in this manner, proximity or touch of a sensing target can be sensed. Even when a sensing target such as a finger or a stylus does not touch but only approaches the input/output device, a signal may be detected in some cases.

[0202]

10 Note that FIG. 8C shows an example in which a common potential supplied in the writing period is equal to a low potential supplied in the sensing period in the wiring 3510; however, one embodiment of the present invention is not limited thereto. The common potential may be different from the low potential.

[0203]

15 It is preferable that, as an example, the pulse voltage output circuit and the detection circuit be formed in one IC. For example, the IC is preferably mounted on input/output device or a substrate in a housing of an electronic device. In the case where the input/output device has flexibility, parasitic capacitance might be increased in a bent portion of the input/output device, and the influence of noise might be increased. In view of this, it is preferable to use an
20 IC to which a driving method less influenced by noise is applied. For example, it is preferable to use an IC to which a driving method capable of increasing a signal-noise ratio (S/N ratio) is applied.

[0204]

It is preferable that a period in which an image is written and a period in which sensing
25 is performed by a sensor element be separately provided as described above. Thus, a decrease in sensitivity of the sensor element caused by noise generated when data is written to a pixel can be suppressed.

[0205]

In one embodiment of the present invention, as shown in FIG. 8D, one frame period
30 includes one writing period and one sensing period. Alternatively, as shown in FIG. 8E, two sensing periods may be included in one frame period. When a plurality of sensing periods are included in one frame period, the detection sensitivity can be further increased. For example, two to four sensing periods may be included in one frame period.

[0206]

35 [Top structure example of sensor element]

Next, top structure examples of the sensor element of the input/output device of one embodiment of the present invention are described with reference to FIGS. 9A and 9B, FIG. 10, and FIGS. 11A and 11B.

[0207]

FIG. 9A illustrates a top view of the sensor element. The sensor element includes a conductive film 56a and a conductive film 56b. The conductive film 56a serves as one electrode of the sensor element. The conductive film 56b serves as the other electrode of the sensor element. The sensor element can sense proximity, touch, or the like of a sensing target by utilizing capacitance formed between the conductive films 56a and 56b. Although not illustrated, the conductive films 56a and 56b have a comb-like top surface shape or a top surface shape provided with a slit in some cases.

[0208]

In one embodiment of the present invention, the conductive films 56a and 56b also serve as the common electrode of the liquid crystal element.

[0209]

A plurality of conductive films 56a are provided in the Y direction and extend in the X direction. A plurality of conductive films 56b provided in the Y direction are electrically connected to each other via a conductive film 58 extending in the Y direction. FIG. 9A illustrates an example in which m conductive films 56a and n conductive films 58 are provided.

[0210]

Note that the plurality of conductive films 56a may be provided in the X direction and in that case, may extend in the Y direction. The plurality of conductive films 56b provided in the X direction may be electrically connected to each other via the conductive film 58 extending in the X direction.

[0211]

As illustrated in FIG. 9B, a conductive film 56 serving as an electrode of the sensor element is provided over a plurality of pixels 60. The conductive film 56 corresponds to each of the conductive films 56a and 56b in FIG. 9A. The pixel 60 is formed of a plurality of subpixels exhibiting different colors. FIG. 9B shows an example in which the pixel 60 is formed of three subpixels, subpixels 60a, 60b, and 60c.

[0212]

A pair of electrodes of the sensor element is preferably electrically connected to respective auxiliary wirings. FIG. 10 illustrates an example in which the conductive films 56a and 56b are electrically connected to auxiliary wirings 57a and 57b, respectively. Note that FIG. 10 illustrates an example in which the auxiliary wirings are stacked over the conductive films;

however, the conductive films may be stacked over the auxiliary wirings.

[0213]

The resistivity of the conductive film that transmits visible light is relatively high in some cases. Thus, the resistance of the pair of electrodes of the sensor element is preferably lowered by electrically connecting the pair of electrodes of the sensor element to the auxiliary wiring.

[0214]

When the resistance of the pair of electrodes of the sensor element is lowered, the time constant of the pair of electrodes can be small. Accordingly, the detection sensitivity of the sensor element can be increased; furthermore, the detection accuracy of the sensor element can be increased.

[0215]

In the writing period, as illustrated in FIG. 11A, a common potential VCOM is input to the conductive films 56a extending in the X direction and the conductive films 58 extending in the Y direction (and the conductive films 56b electrically connected to the conductive film 58). In contrast, in the sensing period, as illustrated in FIG. 11B, each of the conductive films 58 extending in the Y direction (and each of the conductive films 56b electrically connected to the conductive films 58) is electrically connected to a detection circuit. Furthermore, the conductive films 56a extending in the X direction are electrically connected to pulse voltage output circuits and supplied with a pulse voltage.

[0216]

[Top structure example of pixel]

Next, top structure examples of the pixel of the input/output device of one embodiment of the present invention are described with reference to FIG. 12, FIG. 13, and FIGS. 14A and 14B.

[0217]

FIG. 12 is a top view of the pixel. FIG. 13 is a view that differs from FIG. 12 in that the conductive film 252 is indicated by a dotted line. Note that Cross-sectional structure example 1 (FIG. 1A and FIG. 2A) can also be referred to for the stacking order of the layers.

[0218]

A plurality of the conductive films 251 each have an island-shaped top surface shape and are arranged in a matrix. The conductive film 251 is electrically connected to the source or the drain of the transistor 203a.

[0219]

The conductive film 252 is provided to overlap with a plurality of the conductive films

251. The conductive film 252 is provided with a slit. Furthermore, the conductive film 252 has an opening in a position overlapping with the transistor 203a.

[0220]

Here, the conductive film 251 serves as the pixel electrode of the liquid crystal element.

5 The conductive film 252 serves as the common electrode of the liquid crystal element. Note that FIG. 12 and FIG. 13 illustrate examples in which the conductive film 252 on the upper side is a common electrode and the conductive film 251 on the lower side is a pixel electrode; however, a conductive film on the upper side may be a pixel electrode and a conductive film on the lower side may be a common electrode.

10 [0221]

The conductive film 252 serves as an electrode of the sensor element.

[0222]

A conductive film 275 is electrically connected to the conductive film 255 in a region 277 indicated by a dashed line. The conductive film 255 serves as an auxiliary wiring of the 15 conductive film 252 and is electrically connected to the conductive film 252. The conductive film 275 can be formed using the same material and the same step as those of the source and the drain of the transistor 203a.

[0223]

A plurality of conductive films 252 provided in the Y direction corresponds to the 20 conductive film 56b in FIG. 9A and the like. The conductive film 275 extending in the Y direction corresponds to the conductive film 58 in FIG. 9A and the like. The plurality of conductive films 252 provided in the Y direction are electrically connected to the conductive film 275 via the conductive film 255 extending in the Y direction. At this time, when an oxide conductor film is used as the conductive film 252, it is preferable to connect the conductive film 25 255 formed using a metal, an alloy, or the like to the conductive film 275 and electrically connect the conductive film 252 to the conductive film 275 via the conductive film 255, in which case the contact resistance can be lower than that in the case where the conductive film 252 is directly in contact with the conductive film 275.

[0224]

30 Although FIG. 12 and FIG. 13 illustrate examples in which a pixel 273 includes three subpixels, one embodiment of the present invention is not limited thereto.

[0225]

FIGS. 14A and 14B illustrate examples of electrodes of a liquid crystal element.

[0226]

35 A pixel electrode and a common electrode included in a liquid crystal element 207 do

not necessarily have a flat-plate like shape and may have a variety of opening patterns (also referred to as a slit) or a comb-like shape including a bending portion or a branching portion.

[0227]

The liquid crystal element 207 in FIGS. 14A and 14B includes the conductive film 251 that can serve as a pixel electrode and the conductive film 252 that can serve as a common electrode.

[0228]

The transistor 203 in FIGS. 14A and 14B includes the gate electrode 221, the oxide semiconductor film 223, the source electrode 225a, and the drain electrode 225b. The conductive film 251 is electrically connected to the drain electrode 225b.

[0229]

FIG. 14A illustrates an example in which the conductive film 251 has a slit. FIG. 14B illustrates an example in which the conductive film 251 has a comb-like shape. Note that FIGS. 14A and 14B illustrate examples in which the conductive film 251 is over the conductive film 252; however, the conductive film 252 may be over the conductive film 251.

[0230]

[Touch panel module]

Next, a touch panel module including the input/output device of one embodiment of the present invention and an IC are described with reference to FIG. 15 and FIGS. 16A to 16C.

[0231]

FIG. 15 shows a block diagram of a touch panel module 6500. The touch panel module 6500 includes a touch panel 6510 and an IC 6520. The input/output device of one embodiment of the present invention can be applied to the touch panel 6510.

[0232]

The touch panel 6510 includes a display portion 6511, an input portion 6512, and a scan line driver circuit 6513. The display portion 6511 includes a plurality of pixels, a plurality of signal lines, and a plurality of scan lines, and has a function of displaying an image. The input portion 6512 serves as a touch sensor by including a plurality of sensor elements that can sense touch or proximity of a sensing target to the touch panel 6510. A scan line driver circuit 6513 has a function of outputting a scan signal to the scan lines included in the display portion 6511.

[0233]

Here, the display portion 6511 and the input portion 6512 are separately illustrated as the components of the touch panel 6510 for simplicity; however, what is called an in-cell touch panel having a function of displaying an image and serving as a touch sensor is preferable. The input/output device of one embodiment of the present invention is an in-cell touch panel and is

thus favorable.

[0234]

The resolution of the display portion 6511 is preferably as high as HD (number of pixels: 1280×720), FHD (number of pixels: 1920×1080), WQHD (number of pixels: 2560×1440), WQXGA (number of pixels: 2560×1600), 4K (number of pixels: 3840×2160), or 8K (number of pixels: 7680×4320). In particular, resolution of 4K, 8K, or higher is preferable. The pixel density (definition) of the pixels in the display portion 6511 is higher than or equal to 300 ppi, preferably higher than or equal to 500 ppi, more preferably higher than or equal to 800 ppi, more preferably higher than or equal to 1000 ppi, more preferably higher than or equal to 1200 ppi. The display portion 6511 with such high resolution and high definition enables an increase in a realistic sensation, sense of depth, and the like in personal use such as portable use and home use.

[0235]

The IC 6520 includes a circuit unit 6501, a signal line driver circuit 6502, a sensor driver circuit 6503, and a detection circuit 6504. The circuit unit 6501 includes a timing controller 6505, an image processing circuit 6506, or the like.

[0236]

The signal line driver circuit 6502 has a function of outputting a video signal that is an analog signal to a signal line included in the display portion 6511. For example, the signal line driver circuit 6502 can include a shift register circuit and a buffer circuit in combination. The touch panel 6510 may include a demultiplexer circuit connected to a signal line.

[0237]

The sensor driver circuit 6503 has a function of outputting a signal for driving a sensor element included in the input portion 6512. As the sensor driver circuit 6503, a shift register circuit and a buffer circuit can be used in combination, for example.

[0238]

The detection circuit 6504 has a function of outputting, to the circuit unit 6501, an output signal from the sensor element included in the input portion 6512. The detection circuit 6504 can include an amplifier circuit and an analog-digital converter (ADC), for example. In that case, the detection circuit 6504 converts an analog signal output from the input portion 6512 into a digital signal to be output to the circuit unit 6501.

[0239]

The image processing circuit 6506 included in the circuit unit 6501 has a function of generating and outputting a signal for driving the display portion 6511 of the touch panel 6510, a function of generating and outputting a signal for driving the input portion 6512, and a function

of analyzing a signal output from the input portion 6512 and outputting the signal to a CPU 6540.

[0240]

As specific examples, the image processing circuit 6506 has the following functions: a function of generating a video signal in accordance with an instruction from the CPU 6540; a function of performing signal processing on a video signal in accordance with the specification of the display portion 6511, converting the signal into an analog video signal, and supplying the converted signal to the signal line driver circuit 6502; a function of generating a driving signal output to the sensor driver circuit 6503 in accordance with an instruction from the CPU 6540; and a function of analyzing a signal input from the detection circuit 6504 and outputting the analyzed signal to the CPU 6540 as positional information.

[0241]

The timing controller 6505 may have a function of generating a signal (e.g., a clock signal or a start pulse signal) on the basis of a synchronization signal included in a video signal or the like on which the image processing circuit 6506 performs processing and outputting the signal to the scan line driver circuit 6513 and the sensor driver circuit 6503. Furthermore, the timing controller 6505 may have a function of generating and outputting a signal for determining timing when the detection circuit 6504 outputs a signal. Here, the timing controller 6505 preferably outputs a signal synchronized with the signal output to the scan line driver circuit 6513 and a signal synchronized with the signal output to the sensor driver circuit 6503. In particular, it is preferable that a period in which data in a pixel in the display portion 6511 is rewritten and a period in which sensing is performed with the input portion 6512 be separately provided. For example, the touch panel 6510 can be driven by dividing one frame period into a period in which data in a pixel is rewritten and a period in which sensing is performed. Furthermore, detection sensitivity and detection accuracy can be increased, for example, by providing two or more sensing periods in one frame period.

[0242]

The image processing circuit 6506 can include a processor, for example. A microprocessor such as a digital signal processor (DSP) or a graphics processing unit (GPU) can be used, for example. Furthermore, such a microprocessor may be obtained with a programmable logic device (PLD) such as a field programmable gate array (FPGA) or a field programmable analog array (FPAA). The image processing circuit 6506 interprets and executes instructions from various programs with the processor to process various kinds of data and control programs. The programs executed by the processor may be stored in a memory region included in the processor or a memory device that is additionally provided.

[0243]

A transistor that includes an oxide semiconductor in a channel formation region and has an extremely low off-state current can be used in the display portion 6511 or the scan line driver circuit 6513 included in the touch panel 6510, the circuit unit 6501, the signal line driver circuit 6502, the sensor driver circuit 6503, or the detection circuit 6504 included in the IC 6520, the CPU 6540 provided outside, or the like. With the use of the transistor having an extremely low off-state current as a switch for holding electric charge (data) that flows into a capacitor serving as a memory element, a long data retention period can be ensured. For example, by utilizing the characteristic for at least one of a register and a cache memory of the image processing circuit 6506, normally off computing is achieved where the image processing circuit 6506 operates only when needed and data on the previous processing is stored in the memory element in the rest of time; thus, power consumption of the touch panel module 6500 and an electronic device on which the touch panel module 6500 is mounted can be reduced.

[0244]

Although the structure where the circuit unit 6501 includes the timing controller 6505 and the image processing circuit 6506 is used here, the image processing circuit 6506 itself or a circuit having a function of part of the image processing circuit 6506 may be provided outside. Alternatively, the CPU 6540 may have a function of the image processing circuit 6506 or part thereof. For example, the circuit unit 6501 can include the signal line driver circuit 6502, the sensor driver circuit 6503, the detection circuit 6504, and the timing controller 6505.

[0245]

Although the example where the IC 6520 includes the circuit unit 6501 is shown here, the structure where the circuit unit 6501 is not included in the IC 6520 may be employed. In that case, the IC 6520 can include the signal line driver circuit 6502, the sensor driver circuit 6503, and the detection circuit 6504. For example, in the case where the touch panel module 6500 includes a plurality of ICs, the circuit unit 6501 may be provided outside the touch panel module 6500 and a plurality of ICs 6520 without the circuit unit 6501 may be provided, and alternatively, the IC 6520 and an IC including only the signal line driver circuit 6502 can be provided in combination.

[0246]

When an IC has a function of driving the display portion 6511 of the touch panel 6510 and a function of driving the input portion 6512 as described above, the number of ICs mounted on the touch panel module 6500 can be reduced; accordingly, cost can be reduced.

[0247]

FIGS. 16A to 16C each are a schematic diagram of the touch panel module 6500 on

which the IC 6520 is mounted.

[0248]

In FIG. 16A, the touch panel module 6500 includes a substrate 6531, a counter substrate 6532, a plurality of FPCs 6533, the IC 6520, ICs 6530, and the like. The display portion 6511, the input portion 6512, and the scan line driver circuits 6513 are provided between the substrate 6531 and the counter substrate 6532. The IC 6520 and the ICs 6530 are mounted on the substrate 6531 by a COG method.

[0249]

The IC 6530 is an IC in which only the signal line driver circuit 6502 is provided in the above-described IC 6520 or an IC in which the signal line driver circuit 6502 and the circuit unit 6501 are provided in the above-described IC 6520. The ICs 6520 and 6530 are supplied with a signal from the outside through the FPCs 6533. Furthermore, a signal can be output to the outside from at least one of the ICs 6520 and 6530 through the FPC 6533.

[0250]

FIG. 16A illustrates an example where the display portion 6511 is positioned between two scan line driver circuits 6513. The ICs 6530 are provided in addition to the IC 6520. Such a structure is preferable in the case where the display portion 6511 has extremely high resolution.

[0251]

FIG. 16B illustrates an example where one IC 6520 and one FPC 6533 are provided. It is preferable to bring functions into one IC 6520 in this manner because the number of components can be reduced. In the example in FIG. 16B, the scan line driver circuit 6513 is provided along a side close to the FPC 6533 among two short sides of the display portion 6511.

[0252]

FIG. 16C illustrates an example where a printed circuit board (PCB) 6534 on which the image processing circuit 6506 and the like are mounted is provided. The ICs 6520 and 6530 over the substrate 6531 are electrically connected to the PCB 6534 through the FPCs 6533. Here, the above-described structure without the image processing circuit 6506 can be applied to the IC 6520.

[0253]

In each of FIGS. 16A to 16C, the ICs 6520 and 6530 may be mounted on the FPC 6533, not on the substrate 6531. For example, the ICs 6520 and 6530 can be mounted on the FPC 6533 by a COF method, a tape automated bonding (TAB) method, or the like.

[0254]

A structure where the FPC 6533, the IC 6520 (and the IC 6530), or the like is provided

on a short side of the display portion 6511 as illustrated in FIGS. 16A and 16B enables the frame of the display device to be narrowed; thus, the structure is preferably used for electronic devices such as smartphones, mobile phones, and tablet terminals, for example. The structure with the PCB 6534 illustrated in FIG. 16C can be preferably used for television devices, monitors, tablet terminals, or notebook personal computers, for example.

[0255]

This embodiment can be combined with any of the other embodiments as appropriate.

[0256]

(Embodiment 2)

In this embodiment, a manufacturing method of an input/output device of one embodiment of the present invention is described with reference to FIGS. 17A to 17D, FIGS. 18A to 18C, FIGS. 19A to 19C, FIG. 20, and FIG. 21. In this embodiment, a manufacturing method of a transistor is mainly described. Note that the description in Embodiment 1 can be referred to for the material of each layer.

[0257]

First, the gate electrode 221 is formed over the substrate 211. After that, the insulating film 213 including insulating films 106 and 107 is formed over the substrate 211 and the gate electrode 221 (see FIG. 17A).

[0258]

In this embodiment, a glass substrate is used as the substrate 211; a tungsten film is used as the gate electrode 221; a silicon nitride film capable of releasing hydrogen is used as the insulating film 106; and a silicon oxide film capable of releasing oxygen is used as the insulating film 107.

[0259]

The insulating film 106 serves as a blocking film that inhibits penetration of oxygen. For example, in the case where excess oxygen is supplied to at least one of the insulating film 107, the insulating film 215, the insulating film 217, and the oxide semiconductor film 223, the insulating film 106 can inhibit penetration of oxygen.

[0260]

Note that the insulating film 107 that is in contact with the oxide semiconductor film 223 serving as a channel region of the transistor is preferably an oxide insulating film and preferably includes a region including oxygen in excess of the stoichiometric composition (oxygen-excess region). In other words, the insulating film 107 is an insulating film that is capable of releasing oxygen. In order to provide the oxygen-excess region in the insulating film 107, the insulating film 107 can be formed in an oxygen atmosphere, for example.

Alternatively, the oxygen excess region may be formed by introduction of oxygen into the insulating film 107 after the deposition. As a method for introducing oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like may be employed.

5 [0261]

In the case where hafnium oxide is used for one or both of the insulating films 106 and 107, the following effect is attained. Hafnium oxide has a higher dielectric constant than silicon oxide and silicon oxynitride. Therefore, by using hafnium oxide, the thickness of one or both of the insulating films 106 and 107 can be made large as compared with the case where
10 silicon oxide is used; thus, leakage current due to tunnel current can be low. That is, it is possible to provide a transistor with a low off-state current. Moreover, hafnium oxide with a crystalline structure has higher dielectric constant than hafnium oxide with an amorphous structure. Therefore, it is preferable to use hafnium oxide with a crystalline structure in order to provide a transistor with a low off-state current. Examples of the crystalline structure include a
15 monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited to the above examples.

[0262]

In this embodiment, a silicon nitride film is formed as the insulating film 106, and a silicon oxide film is formed as the insulating film 107. A silicon nitride film has a higher
20 dielectric constant than a silicon oxide film and needs a larger thickness for a capacitance equivalent to that of the silicon oxide film. When a silicon nitride film is included as the insulating film 213 serving as a gate insulating film of the transistor, the physical thickness of the insulating film can be increased. This makes it possible to reduce a decrease in withstand voltage of the transistor and furthermore increase the withstand voltage, thereby reducing
25 electrostatic discharge damage to the transistor.

[0263]

To form the gate electrode 221, a conductive film is formed over the substrate 211, the conductive film is patterned so that a desired region thereof remains, and unnecessary regions are etched.

30 [0264]

Next, the oxide semiconductor film 223 is formed in a region overlapping with the gate electrode 221 over the insulating film 213 (FIG. 17B).

[0265]

In this embodiment, as the oxide semiconductor film 223, an In-Ga-Zn oxide film,
35 which is formed using a metal oxide target with In:Ga:Zn = 1:1:1.2 [atomic ratio], is used.

[0266]

The oxide semiconductor film 223 can be formed in such a manner that an oxide semiconductor film is formed over the insulating film 213, the oxide semiconductor film is patterned so that a desired region thereof remains, and then unnecessary regions are etched.

[0267]

After formation of the oxide semiconductor film 223, heat treatment is preferably performed. The heat treatment is preferably performed at a temperature of higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 300 °C and lower than or equal to 500 °C, more preferably higher than or equal to 350 °C and lower than or equal to 450 °C, in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, or a reduced pressure atmosphere. Alternatively, the heat treatment may be performed first in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more in order to compensate oxygen released from the oxide semiconductor film 223. By this heat treatment, impurities such as hydrogen and water can be removed from at least one of the insulating film 106, the insulating film 107, and the oxide semiconductor film 223. Note that the above-described heat treatment may be performed before the oxide semiconductor film 223 is processed into an island shape.

[0268]

Note that stable electrical characteristics can be effectively imparted to the transistor in which the oxide semiconductor film 223 serves as a channel region by reducing the concentration of impurities in the oxide semiconductor film 223 to make the oxide semiconductor film 223 intrinsic or substantially intrinsic.

[0269]

Next, a conductive film is formed over the insulating film 213 and the oxide semiconductor film 223 and is patterned so that a desired region thereof remains and unnecessary regions are etched, whereby the source electrode 225a and the drain electrode 225b are formed over the insulating film 213 and the oxide semiconductor film 223 (see FIG. 17C).

[0270]

In this embodiment, a three-layered structure including a tungsten film, an aluminum film, and a titanium film can be used for the source electrode 225a and the drain electrode 225b.

[0271]

After the source electrode 225a and the drain electrode 225b are formed, a surface of the oxide semiconductor film 223 may be cleaned. The cleaning may be performed, for example, using a chemical solution such as phosphoric acid. The cleaning using a chemical solution such as a phosphoric acid can remove impurities (e.g., elements contained in the source electrode

225a and the drain electrode 225b) attached to the surface of the oxide semiconductor film 223. Note that the cleaning is not necessarily performed, and thus the cleaning may be unnecessary.
[0272]

In addition, in the step of forming the source electrode 225a and the drain electrode 225b and/or the cleaning step, the thickness of a region of the oxide semiconductor film 223 that is not covered by the source electrode 225a and the drain electrode 225b might be reduced.
[0273]

Next, the insulating film 215 including insulating films 114 and 116 is formed over the insulating film 213, the oxide semiconductor film 223, the source electrode 225a, and the drain electrode 225b. Then, the insulating film 215 is patterned so that a desired region thereof remains and unnecessary regions are etched, whereby an opening 141 is formed (see FIG. 17D).
[0274]

Note that after the insulating film 114 is formed, the insulating film 116 is preferably formed in succession without exposure to the air. After the insulating film 114 is formed, the insulating film 116 is formed in succession by adjusting at least one of the flow rate of a source gas, pressure, a high-frequency power, and a substrate temperature without exposure to the air, whereby the concentration of impurities attributed to the atmospheric component at the interface between the insulating film 114 and the insulating film 116 can be reduced, and oxygen in the insulating films 114 and 116 can be moved to the oxide semiconductor film 223; accordingly, the number of oxygen vacancies in the oxide semiconductor film 223 can be reduced.
[0275]

Note that the insulating film 114 serves as a protective film for the oxide semiconductor film 223 in the step of forming the insulating film 116. Consequently, the insulating film 116 can be formed using the high-frequency power having a high power density while damage to the oxide semiconductor film 223 is reduced.
[0276]

In this embodiment, a silicon oxynitride film capable of releasing oxygen is used as the insulating films 114 and 116.
[0277]

Note that the insulating film 114 that is in contact with the oxide semiconductor film 223 serving as a channel region of the transistor is preferably an oxide insulating film capable of releasing oxygen. In other words, the insulating film capable of releasing oxygen is an insulating film that includes a region containing oxygen in excess of that in the stoichiometric composition (oxygen-excess region). In order to provide the oxygen-excess region in the insulating film 114, the insulating film 114 can be formed in an oxygen atmosphere, for example.

Alternatively, the oxygen-excess region may be formed by supplying oxygen to the formed insulating film 114. As a method for supplying oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like can be employed.

5 [0278]

The use of the insulating film capable of releasing oxygen as the insulating film 114 can reduce the number of oxygen vacancies in the oxide semiconductor film 223 by transferring oxygen to the oxide semiconductor film 223 serving as the channel region of the transistor. For example, the number of oxygen vacancies in the oxide semiconductor film 223 can be reduced
10 by using an insulating film having the following feature: the number of oxygen molecules released from the insulating film by heat treatment at a temperature higher than or equal to 100 °C and lower than or equal to 700 °C, or higher than or equal to 100 °C and lower than or equal to 500 °C is greater than or equal to 1.0×10^{18} molecules/cm³ when measured by thermal desorption spectroscopy (TDS) analysis.

15 [0279]

It is preferable that the number of defects in the insulating film 114 be small, typically the spin density corresponding to a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than or equal to 3×10^{17} spins/cm³ by ESR measurement. This is because if the density of defects in the insulating film 114 is high, oxygen is bonded to the defects and the
20 amount of oxygen that permeates the insulating film 114 is decreased. Furthermore, it is preferable that the amount of defects at the interface between the insulating film 114 and the oxide semiconductor film 223 be small and typically, the spin density of a signal that appears at $g = 1.89$ or more and 1.96 or less due to the defect in the oxide semiconductor film 223 be lower than or equal to 1×10^{17} spins/cm³, more preferably lower than or equal to the lower limit of
25 detection by ESR measurement.

[0280]

Note that all oxygen entering the insulating film 114 from the outside moves to the outside of the insulating film 114 in some cases. Alternatively, some oxygen entering the insulating film 114 from the outside remains in the insulating film 114 in some cases.
30 Furthermore, movement of oxygen occurs in the insulating film 114 in some cases in such a manner that oxygen enters the insulating film 114 from the outside and oxygen contained in the insulating film 114 moves to the outside of the insulating film 114. When an oxide insulating film that is permeable to oxygen is formed as the insulating film 114, oxygen released from the insulating film 116 provided over the insulating film 114 can be moved to the oxide
35 semiconductor film 223 through the insulating film 114.

[0281]

The insulating film 114 can be formed using an oxide insulating film having a low density of states due to nitrogen oxide. Note that the density of states due to nitrogen oxide can be formed between the energy of the valence band maximum (E_{v_os}) and the energy of the conduction band minimum (E_{c_os}) of the oxide semiconductor film. A silicon oxynitride film that releases less nitrogen oxide, an aluminum oxynitride film that releases less nitrogen oxide, or the like can be used as the oxide insulating film.

[0282]

Note that a silicon oxynitride film that releases a small amount of nitrogen oxide is a film of which the amount of released ammonia is larger than the amount of released nitrogen oxide in TDS analysis; the amount of released ammonia is typically greater than or equal to 1×10^{18} molecules/cm³ and less than or equal to 5×10^{19} molecules/cm³. The amount of released ammonia corresponds to the released amount caused by heat treatment at a film surface temperature higher than or equal to 50 °C and lower than or equal to 650 °C, preferably higher than or equal to 50 °C and lower than or equal to 550 °C.

[0283]

Nitrogen oxide (NO_x ; x is greater than 0 and less than or equal to 2, preferably greater than or equal to 1 and less than or equal to 2), typically NO_2 or NO , forms levels in the insulating film 114, for example. The levels are positioned in the energy gap of the oxide semiconductor film 223. Therefore, when nitrogen oxide is diffused to the interface between the insulating film 114 and the oxide semiconductor film 223, an electron is trapped by the level on the insulating film 114 side. As a result, the trapped electron remains in the vicinity of the interface between the insulating film 114 and the oxide semiconductor film 223; thus, the threshold voltage of the transistor is shifted in the positive direction.

[0284]

Nitrogen oxide reacts with ammonia and oxygen in heat treatment. Since nitrogen oxide contained in the insulating film 114 reacts with ammonia contained in the insulating film 116 in heat treatment, nitrogen oxide contained in the insulating film 114 is reduced. Therefore, an electron is hardly trapped at the interface between the insulating film 114 and the oxide semiconductor film 223.

[0285]

In a transistor using the oxide insulating film as the insulating film 114, the shift in threshold voltage can be reduced, which leads to a smaller change in electrical characteristics of the transistor.

[0286]

Note that in an ESR spectrum obtained at 100 K or lower of the insulating film 114, by heat treatment in a manufacturing process of the transistor, typically heat treatment at a temperature lower than 400 °C or lower than 375 °C (preferably higher than or equal to 340 °C and lower than or equal to 360 °C), a first signal that appears at a *g*-factor of greater than or equal to 2.037 and less than or equal to 2.039, a second signal that appears at a *g*-factor of greater than or equal to 2.001 and less than or equal to 2.003, and a third signal that appears at a *g*-factor of greater than or equal to 1.964 and less than or equal to 1.966 are observed. The split width of the first and second signals and the split width of the second and third signals, which are obtained by ESR measurement using an X-band, are each approximately 5 mT. The sum of the spin densities of the first signal that appears at a *g*-factor of greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a *g*-factor of greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a *g*-factor of greater than or equal to 1.964 and less than or equal to 1.966 is less than 1×10^{18} spins/cm³, typically greater than or equal to 1×10^{17} spins/cm³ and less than 1×10^{18} spins/cm³.

[0287]

In the ESR spectrum at 100 K or lower, the first signal that appears at a *g*-factor of greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a *g*-factor of greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a *g*-factor of greater than or equal to 1.964 and less than or equal to 1.966 correspond to signals attributed to nitrogen oxide (NO_x; *x* is greater than 0 and less than or equal to 2, preferably greater than or equal to 1 and less than or equal to 2). Typical examples of nitrogen oxide include nitrogen monoxide and nitrogen dioxide. In other words, the smaller the sum of the spin densities of the first signal that appears at a *g*-factor greater than or equal to 2.037 and less than or equal to 2.039, the second signal that appears at a *g*-factor greater than or equal to 2.001 and less than or equal to 2.003, and the third signal that appears at a *g*-factor greater than or equal to 1.964 and less than or equal to 1.966 is, the lower the content of nitrogen oxide in the oxide insulating film is.

[0288]

The nitrogen concentration of the oxide insulating film measured by SIMS is lower than or equal to 6×10^{20} atoms/cm³.

[0289]

The oxide insulating film is formed by a PECVD method at a substrate temperature higher than or equal to 220 °C and lower than or equal to 350 °C using silane and dinitrogen monoxide, whereby a dense and hard film can be formed.

[0290]

The insulating film 116 in contact with the insulating film 114 is formed using an oxide insulating film whose oxygen content is in excess of that in the stoichiometric composition. Part of oxygen is released from the oxide insulating film whose oxygen content is in excess of that in the stoichiometric composition by heating. The oxide insulating film whose oxygen content is in excess of that in the stoichiometric composition is an oxide insulating film of which the amount of released oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{19} atoms/cm³, preferably greater than or equal to 3.0×10^{20} atoms/cm³ in TDS analysis. Note that the temperature of the film surface in the TDS analysis is preferably higher than or equal to 100 °C and lower than or equal to 700 °C, or higher than or equal to 100 °C and lower than or equal to 500 °C.

[0291]

Furthermore, it is preferable that the amount of defects in the insulating film 116 be small, typically the spin density of a signal that appears at $g = 2.001$ due to a dangling bond of silicon be less than 1.5×10^{18} spins/cm³, preferably less than or equal to 1×10^{18} spins/cm³ by ESR measurement. Note that the insulating film 116 is provided more apart from the oxide semiconductor film 223 than the insulating film 114 is; thus, the insulating film 116 may have higher defect density than the insulating film 114.

[0292]

The thickness of the insulating film 114 can be greater than or equal to 5 nm and less than or equal to 150 nm, preferably greater than or equal to 5 nm and less than or equal to 50 nm, more preferably greater than or equal to 10 nm and less than or equal to 30 nm. The thickness of the insulating film 116 can be greater than or equal to 30 nm and less than or equal to 500 nm, preferably greater than or equal to 150 nm and less than or equal to 400 nm.

[0293]

The insulating films 114 and 116 can be formed using insulating films formed of the same kinds of materials; thus, a boundary between the insulating films 114 and 116 cannot be clearly observed in some cases. Thus, in this embodiment, the boundary between the insulating films 114 and 116 is shown by a dashed line. Although a two-layer structure of the insulating films 114 and 116 is described in this embodiment, the present invention is not limited to this. For example, a single-layer structure of the insulating film 114, a single-layer structure of the insulating film 116, or a stacked-layer structure of three or more layers may be used.

[0294]

Heat treatment (hereinafter referred to as first heat treatment) is preferably performed after the insulating films 114 and 116 are formed. The first heat treatment can reduce nitrogen oxide included in the insulating films 114 and 116. By the first heat treatment, part of oxygen

included in the insulating films 114 and 116 can be moved to the oxide semiconductor film 223, so that the number of oxygen vacancies included in the oxide semiconductor film 223 can be reduced.

[0295]

5 The temperature of the first heat treatment is typically lower than 400 °C, preferably lower than 375 °C, further preferably higher than or equal to 150 °C and lower than or equal to 350 °C. The first heat treatment may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air with a water content of 20 ppm or less, preferably 1 ppm or less, more preferably 10 ppb or less), or a rare gas (argon, helium, or the like). The atmosphere of
10 nitrogen, oxygen, ultra-dry air, or a rare gas preferably does not contain hydrogen, water, and the like. An electric furnace, a rapid thermal annealing (RTA) apparatus, or the like can be used for the heat treatment.

[0296]

The opening 141 is formed to expose part of the drain electrode 225b. The opening
15 141 can be formed by a dry etching method, for example. Alternatively, a wet etching method or a combination of dry etching and wet etching can be employed for formation of the opening 141. Note that the etching step of forming the opening 141 can reduce the thickness of the drain electrode 225b in some cases.

[0297]

20 Next, an oxide semiconductor film to be the oxide conductor film 227 is formed over the insulating film 116 to cover the opening 141 (FIGS. 18A and 18B).

[0298]

Note that FIG. 18A is a schematic cross-sectional view of the inside of a deposition apparatus when the oxide semiconductor film is formed over the insulating film 116. In FIG.
25 18A, a sputtering apparatus is used as the deposition apparatus, and a target 193 placed inside the sputtering apparatus and plasma 194 formed under the target 193 are schematically shown.

[0299]

When the oxide semiconductor film is formed, plasma discharge is performed in an atmosphere containing a third oxygen gas. At this time, oxygen is added to the insulating film
30 116 over which the oxide semiconductor film is to be formed. When the oxide semiconductor film is formed, an inert gas (e.g., a helium gas, an argon gas, or a xenon gas) and the third oxygen gas may be mixed. For example, it is preferable to use the argon gas and the third oxygen gas with the flow rate of the third oxygen gas higher than the flow rate of the argon gas. When the flow rate of the third oxygen gas is set higher, oxygen can be favorably added to the
35 insulating film 116. As an example of the formation conditions of the oxide semiconductor

film, the proportion of the third oxygen gas in a whole deposition gas can be higher than or equal to 50 % and lower than or equal to 100 %, preferably higher than or equal to 80 % and lower than or equal to 100 %.

[0300]

5 In FIG. 18A, oxygen or excess oxygen added to the insulating film 116 is schematically shown by arrows of broken lines.

[0301]

The oxide semiconductor film is formed at a substrate temperature higher than or equal to room temperature and lower than 340 °C, preferably higher than or equal to room temperature and lower than or equal to 300 °C, further preferably higher than or equal to 100 °C and lower than or equal to 250 °C, still further preferably higher than or equal to 100 °C and lower than or equal to 200 °C. The oxide semiconductor film is formed while being heated, so that the crystallinity of the oxide semiconductor film can be increased. On the other hand, in the case where a large-sized glass substrate (e.g., the 6th generation to the 10th generation) is used as the substrate 211 and the oxide semiconductor film is formed at a substrate temperature higher than or equal to 150 °C and lower than 340 °C, the substrate 211 might be changed in shape (distorted or warped). In the case where a large-sized glass substrate is used, the change in the shape of the glass substrate can be suppressed by forming the oxide semiconductor film at a substrate temperature higher than or equal to 100 °C and lower than 150 °C.

20 [0302]

In this embodiment, the oxide semiconductor film is formed by a sputtering method using an In-Ga-Zn metal oxide target (with In:Ga:Zn = 1:3:6 [atomic ratio]).

[0303]

25 Next, the oxide semiconductor film is processed into a desired shape to form an island-shaped oxide semiconductor film 227a (see FIG. 18C).

[0304]

The oxide semiconductor film 227a can be formed in such a manner that an oxide semiconductor film is formed over the insulating film 116, the oxide semiconductor film is patterned so that a desired region thereof remains, and then unnecessary regions are etched.

30 [0305]

Next, the insulating film 217 is formed over the insulating film 116 and the oxide semiconductor film 227a (see FIG. 19A).

[0306]

The insulating film 217 has a function of blocking oxygen, hydrogen, water, alkali metal,

alkaline earth metal, or the like. With the insulating film 217, diffusion of oxygen from the oxide semiconductor film 223 to the outside, diffusion of oxygen contained in the insulating film 215 to the outside, and entry of hydrogen, water, alkali metal, alkaline earth metal, or the like from the outside into the oxide semiconductor film 223 can be prevented.

5 [0307]

The insulating film 217 preferably contains one or both of hydrogen and nitrogen. As the insulating film 217, a silicon nitride film is preferably used, for example. The insulating film 217 can be formed by a sputtering method or a PECVD method, for example. In the case where the insulating film 217 is formed by a PECVD method, for example, the substrate
10 temperature is lower than 400 °C, preferably lower than 375 °C, further preferably higher than or equal to 180 °C and lower than or equal to 350 °C. The substrate temperature at which the insulating film 217 is formed is preferably within the above range because a dense film can be formed. Furthermore, when the substrate temperature at which the insulating film 217 is formed is within the above range, oxygen or excess oxygen in the insulating films 114 and 116
15 can be moved to the oxide semiconductor film 223.

[0308]

Note that instead of the nitride insulating film having a blocking effect against oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. As the oxide
20 insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given.

[0309]

25 After the insulating film 217 is formed, heat treatment similar to the first heat treatment (hereinafter referred to as second heat treatment) may be performed. Through such heat treatment at lower than 400 °C, preferably lower than 375 °C, further preferably higher than or equal to 180 °C and lower than or equal to 350 °C after the addition of oxygen to the insulating film 116 when the oxide semiconductor film to be the oxide conductor film 227 is formed,
30 oxygen or excess oxygen in the insulating film 116 can be moved into the oxide semiconductor film 223 and compensate oxygen vacancies in the oxide semiconductor film 223.

[0310]

Oxygen moved to the oxide semiconductor film 223 is described with reference to FIG.
20. FIG. 20 are model diagrams illustrating oxygen moved to the oxide semiconductor film 223 due to the substrate temperature at the time of forming the insulating film 217 (typically,
35

lower than 375 °C) or the second heat treatment after the formation of the insulating film 217 (typically, lower than 375 °C). In FIG. 20, oxygen (oxygen radicals, oxygen atoms, or oxygen molecules) moved to the oxide semiconductor film 223 is shown by arrows of broken lines. Note that FIG. 20 is a cross-sectional view of the transistor after the insulating film 217 is formed and its periphery.

[0311]

In the oxide semiconductor film 223 in FIG. 20, oxygen vacancies are compensated with oxygen moved from films in contact with the oxide semiconductor film 223 (here, the insulating film 107 and the insulating film 114). Specifically, in the input/output device of one embodiment of the present invention, the insulating film 107 includes an excess oxygen region because an oxygen gas is used at the time of forming the oxide semiconductor film to be the oxide semiconductor film 223 by sputtering and oxygen is added to the insulating film 107. Furthermore, the insulating film 116 includes an excess oxygen region because an oxygen gas is used at the time of forming the oxide semiconductor film to be the oxide conductor film 227 by sputtering and oxygen is added to the insulating film 116. In the oxide semiconductor film 223 between the insulating films including the excess oxygen regions, oxygen vacancies can be favorably compensated.

[0312]

Furthermore, the insulating film 106 is provided under the insulating film 107, and the insulating film 217 is provided over the insulating films 114 and 116. When the insulating films 106 and 217 are formed using a material having low oxygen permeability, e.g., silicon nitride, oxygen contained in the insulating films 107, 114, and 116 can be confined to the oxide semiconductor film 223 side; thus, oxygen can be favorably moved to the oxide semiconductor film 223.

[0313]

The insulating film 217 preferably has a function of lowering the resistivity of the oxide conductor film 227.

[0314]

With the insulating film 217 containing one or both of hydrogen and nitrogen, one or both of hydrogen and nitrogen is added to the oxide semiconductor film 227a in contact with the insulating film 217. Accordingly, the carrier density of the oxide semiconductor film 227a is increased, and the oxide semiconductor film 227a can serve as an oxide conductor film.

[0315]

Note that the oxide semiconductor film 227a with decreased resistivity is illustrated as the oxide conductor film 227 after FIG. 19A.

[0316]

The resistivity of the oxide conductor film 227 is lower than at least the resistivity of the oxide semiconductor film 223 and is preferably higher than or equal to $1 \times 10^{-3} \Omega\text{cm}$ and lower than $1 \times 10^4 \Omega\text{cm}$, further preferably higher than or equal to $1 \times 10^{-3} \Omega\text{cm}$ and lower than $1 \times 10^{-1} \Omega\text{cm}$.

[0317]

Then, an opening 142 is formed as follows: the insulating film 219 is formed over the insulating film 217, the insulating films 217 and 219 are patterned so that a desired region thereof remains, and unnecessary regions are etched (see FIG. 19B).

[0318]

In this embodiment, an acrylic resin is used for the insulating film 219.

[0319]

The opening 142 is formed to expose the drain electrode 225b. The opening 142 can be formed by a dry etching method, for example. Alternatively, a wet etching method or a combination of dry etching and wet etching can be employed for formation of the opening 142. Note that the etching step of forming the opening 142 can reduce the thickness of the drain electrode 225b in some cases.

[0320]

Note that the opening may be formed in the insulating films 114, 116, 217, and 219 at one time in the step of forming the opening 142 without performing the step of forming the opening 141. In this case, the number of steps of manufacturing the input/output device of one embodiment of the present invention is reduced, resulting in a reduction of the manufacturing cost.

[0321]

Then, a conductive film is formed over the insulating film 219 to cover the opening 142 and is patterned so that a desired region thereof remains, and unnecessary regions are etched; thus, the conductive film 251 is formed. The insulating film 253 is formed over the conductive film 251. Then, a conductive film is formed over the insulating film 253 and is patterned so that a desired region of the conductive film remains, and an unnecessary region is etched; thus, the conductive film 255 is formed. After that, a conductive film is formed over the insulating film 253 and the conductive film 255 and is patterned so that a desired region of the conductive film remains, and then, an unnecessary region is etched to form the conductive film 252 (see FIG. 19C).

[0322]

In this embodiment, ITO films are used as the conductive films 251 and 252, a silicon

nitride film is used as the insulating film 253, an alloy film of silver, palladium, and copper (also referred to as Ag-Pd-Cu or APC) is used as the conductive film 255.

[0323]

The formation order of the conductive films 252 and 255 is not limited; however, the conductive film 255 is preferably formed before the conductive film 252. In such a case, damage to the conductive film 252 caused by etching of the conductive film 255 can be reduced, for example.

[0324]

Note that the conductive film 251 may be formed using an oxide semiconductor film by a method similar to that of the oxide conductor film 227. In this case, the insulating film 253 over the conductive film 251 can be formed using a material that can be used for the insulating film 217. The conductive film 252 may be formed by forming an oxide semiconductor film and performing treatment for lowering the resistivity of the oxide semiconductor film.

[0325]

Through the above steps, the transistor 203b and the pair of electrodes of the liquid crystal element illustrated in FIG. 4 can be formed.

[0326]

Note that although the structure with the insulating film 219 is shown in FIG. 19C, a structure without the insulating film 219 may be employed (see FIG. 21).

[0327]

This embodiment can be combined with any of the other embodiments as appropriate.

[0328]

(Embodiment 3)

In this embodiment, a transistor that can be used for the input/output device of one embodiment of the present invention is described with reference to FIGS. 22A to 22C, FIGS. 23A to 23D, FIGS. 24A and 24B, and FIGS. 25A to 25D. Note that the description in Embodiment 1 can be referred to for the material of each layer.

[0329]

<Structure example 1 of transistor>

FIG. 22A is a top view of a transistor 270. FIG. 22B is a cross-sectional view taken along the dashed-dotted line A1-A2 in FIG. 22A, and FIG. 22C is a cross-sectional view taken along the dashed-dotted line B1-B2 in FIG. 22A. Note that the direction of the dashed dotted line A1-A2 may be called the channel length direction, and the direction of the dashed dotted line B1-B2 may be called the channel width direction.

[0330]

The transistor 270 includes a conductive film 504 serving as a first gate electrode over a substrate 502, an insulating film 506 over the substrate 502 and the conductive film 504, an insulating film 507 over the insulating film 506, an oxide semiconductor film 508 over the insulating film 507, a conductive film 512a serving as a source electrode electrically connected to the oxide semiconductor film 508, a conductive film 512b serving as a drain electrode electrically connected to the oxide semiconductor film 508, insulating films 514 and 516 over the oxide semiconductor film 508 and the conductive films 512a and 512b, and an oxide conductor film 511b over the insulating film 516. In addition, an insulating film 518 is provided over the oxide conductor film 511b.

[0331]

In the transistor 270, the insulating films 514 and 516 serve as a second gate insulating film of the transistor 270. An oxide semiconductor film 511a is connected to the conductive film 512b through an opening 552c provided in the insulating films 514 and 516. The oxide semiconductor film 511a serves as, for example, a pixel electrode of a display element. The oxide conductor film 511b in the transistor 270 serves as a second gate electrode (also referred to as a back gate electrode).

[0332]

As illustrated in FIG. 22C, the oxide conductor film 511b is connected to the conductive film 504 serving as a first gate electrode through openings 552a and 552b provided in the insulating films 506, 507, 514, and 516. Accordingly, the oxide conductor film 504 and the oxide conductor film 511b are supplied with the same potential.

[0333]

Note that although the structure in which the openings 552a and 552b are provided so that the oxide conductor film 511b and the conductive film 504 are connected to each other is described in this embodiment, one embodiment of the present invention is not limited thereto. For example, a structure in which only one of the openings 552a and 552b is provided so that the oxide conductor film 511b and the conductive film 504 are connected to each other, or a structure in which the openings 552a and 552b are not provided and the oxide conductor film 511b and the conductive film 504 are not connected to each other may be employed. Note that in the case where the oxide conductor film 511b and the conductive film 504 are not connected to each other, it is possible to apply different potentials to the oxide conductor film 511b and the conductive film 504.

[0334]

As illustrated in FIG. 22B, the oxide semiconductor film 508 is positioned to face each of the conductive film 504 serving as a first gate electrode and the oxide conductor film 511b

serving as a second gate electrode, and is sandwiched between the two conductive films serving as gate electrodes. The length in the channel length direction and the length in the channel width direction of the oxide conductor film 511b serving as a second gate electrode are longer than that in the channel length direction and that in the channel width direction of the oxide semiconductor film 508, respectively. The whole oxide semiconductor film 508 is covered with the oxide conductor film 511b with the insulating films 514 and 516 positioned therebetween. Since the oxide conductor film 511b serving as a second gate electrode is connected to the conductive film 504 serving as a first gate electrode through the openings 552a and 552b provided in the insulating films 506 and 507 and the insulating films 514 and 516, a side surface of the oxide semiconductor film 508 in the channel width direction faces the oxide conductor film 511b serving as a second gate electrode with the insulating films 514 and 516 positioned therebetween.

[0335]

In other words, in the channel width direction of the transistor 270, the conductive film 504 serving as a first gate electrode and the oxide conductor film 511b serving as a second gate electrode are connected to each other through the openings provided in the insulating films 506 and 507 serving as gate insulating films and the insulating films 514 and 516 serving as second gate insulating films; and the conductive film 504 and the oxide conductor film 511b surround the oxide semiconductor film 508 with the insulating films 506 and 507 serving as the gate insulating films and the insulating films 514 and 516 serving as the second gate insulating films positioned therebetween.

[0336]

Such a structure enables the oxide semiconductor film 508 included in the transistor 270 to be electrically surrounded by electric fields of the conductive film 504 serving as a first gate electrode and the oxide conductor film 511b serving as a second gate electrode. A device structure of a transistor, like that of the transistor 270, in which electric fields of a first gate electrode and a second gate electrode electrically surround an oxide semiconductor film where a channel region is formed, can be referred to as a surrounded channel (s-channel) structure.

[0337]

Since the transistor 270 has the s-channel structure, an electric field for inducing a channel can be effectively applied to the oxide semiconductor film 508 by the conductive film 504 serving as a first gate electrode; therefore, the current drive capability of the transistor 270 can be improved and high on-state current characteristics can be obtained. Since the on-state current can be increased, it is possible to reduce the size of the transistor 270. In addition, since the transistor 270 is surrounded by the conductive film 504 serving as a first gate electrode and

the oxide conductor film 511b serving as a second gate electrode, the mechanical strength of the transistor 270 can be increased.

[0338]

<Structure example 2 of transistor>

FIGS. 23A and 23B illustrate a cross-sectional view illustrating a modification example of the transistor 270 in FIGS. 22B and 22C. FIGS. 23C and 23D illustrate a cross-sectional view illustrating another modification example of the transistor 270 in FIGS. 22B and 22C.

[0339]

A transistor 270A in FIGS. 23A and 23B is different from the transistor 270 in FIGS. 22B and 22C in that the oxide semiconductor film 508 has a three-layer structure. Specifically, the oxide semiconductor film 508 of the transistor 270A includes an oxide semiconductor film 508a, an oxide semiconductor film 508b, and an oxide semiconductor film 508c.

[0340]

A transistor 270B in FIGS. 23C and 23D is different from the transistor 270 in FIGS. 22B and 22C in that the oxide semiconductor film 508 has a two-layer structure. Specifically, the oxide semiconductor film 508 of the transistor 270B includes the oxide semiconductor films 508b and 508c.

[0341]

Here, a band structure including the oxide semiconductor film 508 and insulating films in contact with the oxide semiconductor film 508 is described with reference to FIGS. 24A and 24B.

[0342]

FIG. 24A shows an example of a band structure in the thickness direction of a layered structure including the insulating film 507, the oxide semiconductor films 508a, 508b, and 508c, and the insulating film 514. FIG. 24B shows an example of a band structure in the thickness direction of a layered structure including the insulating film 507, the oxide semiconductor films 508b and 508c, and the insulating film 514. For easy understanding, the energy level of the conduction band minimum (E_c) of each of the insulating film 507, the oxide semiconductor films 508a, 508b, and 508c, and the insulating film 514 is shown in the band structures.

[0343]

In the band structure of FIG. 24A, a silicon oxide film is used as each of the insulating film 507 and the insulating film 514, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 1:1:1.2, is used as the oxide semiconductor film 508a, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 4:2:4.1, is used as the oxide semiconductor film

508b, and an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 1:1:1.2, is used as the oxide semiconductor film 508c.

[0344]

In the band structure of FIG. 24B, a silicon oxide film is used as each of the insulating film 507 and the insulating film 514, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 4:2:4.1, is used as the oxide semiconductor film 508b, and an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 1:1:1.2, is used as the oxide semiconductor film 508c.

[0345]

As illustrated in FIGS. 24A and 24B, the energy level of the conduction band minimum gradually changes between the oxide semiconductor films 508a and 508b and between the oxide semiconductor films 508b and 508c. In other words, the energy level of the conduction band minimum is continuously changed or continuously connected. To obtain such a band structure, there exists no impurity, which forms a defect state such as a trap center or a recombination center, at the interface between the oxide semiconductor films 508a and 508b or at the interface between the oxide semiconductor films 508b and 508c.

[0346]

To form a continuous junction between the oxide semiconductor films 508a and 508b and between the oxide semiconductor films 508b and 508c, it is necessary to form the films successively without exposure to the air by using a multi-chamber deposition apparatus (sputtering apparatus) provided with a load lock chamber.

[0347]

With the band structures of FIGS. 24A and 24B, the oxide semiconductor film 508b serves as a well, and a channel region is formed in the oxide semiconductor film 508b in the transistor with the layered structure.

[0348]

By providing the oxide semiconductor films 508a and 508c, the oxide semiconductor film 508b can be distanced away from trap states.

[0349]

In addition, the trap states might be more distant from the vacuum level than the energy level of the conduction band minimum (E_c) of the oxide semiconductor film 508b serving as a channel region, so that electrons are likely to be accumulated in the trap states. When the electrons are accumulated in the trap states, the electrons become negative fixed electric charge, so that the threshold voltage of the transistor is shifted in the positive direction. Therefore, it is

preferable that the trap states be closer to the vacuum level than the energy level of the conduction band minimum (E_c) of the oxide semiconductor film 508b. Such a structure inhibits accumulation of electrons in the trap states. As a result, the on-state current and the field-effect mobility of the transistor can be increased.

5 [0350]

The energy level of the conduction band minimum of each of the oxide semiconductor films 508a and 508c is closer to the vacuum level than that of the oxide semiconductor film 508b. Typically, a difference in energy level between the conduction band minimum of the oxide semiconductor film 508b and the conduction band minimum of each of the oxide semiconductor
10 films 508a and 508c is 0.15 eV or more or 0.5 eV or more and 2 eV or less or 1 eV or less. That is, the difference between the electron affinity of each of the oxide semiconductor films 508a and 508c and the electron affinity of the oxide semiconductor film 508b is 0.15 eV or more or 0.5 eV or more and 2 eV or less or 1 eV or less.

[0351]

15 In such a structure, the oxide semiconductor film 508b serves as a main path of a current. In other words, the oxide semiconductor film 508b serves as a channel region, and the oxide semiconductor films 508a and 508c serve as oxide insulating films. In addition, since the oxide semiconductor films 508a and 508c each include one or more metal elements included in the oxide semiconductor film 508b in which a channel region is formed, interface scattering is less
20 likely to occur at the interface between the oxide semiconductor films 508a and 508b or at the interface between the oxide semiconductor films 508b and 508c. Thus, the transistor can have high field-effect mobility because the movement of carriers is not hindered at the interface.

[0352]

To prevent each of the oxide semiconductor films 508a and 508c from serving as part of
25 a channel region, a material having sufficiently low conductivity is used for the oxide semiconductor films 508a and 508c. Thus, the oxide semiconductor films 508a and 508c can be referred to as oxide insulating films for such properties and/or functions. Alternatively, a material that has a smaller electron affinity (a difference in energy level between the vacuum level and the conduction band minimum) than the oxide semiconductor film 508b and has a
30 difference in energy level in the conduction band minimum from the oxide semiconductor film 508b (band offset) is used for the oxide semiconductor films 508a and 508c. Furthermore, to inhibit generation of a difference in threshold voltage due to the value of the drain voltage, the energy level of the conduction band minimum of each of the oxide semiconductor films 508a and 508c is preferably closer to the vacuum level than the energy level of the conduction band
35 minimum of the oxide semiconductor film 508b is. For example, a difference between the

energy level of the conduction band minimum of the oxide semiconductor film 508b and the energy level of the conduction band minimum of each of the oxide semiconductor films 508a and 508c is preferably greater than or equal to 0.2 eV, more preferably greater than or equal to 0.5 eV.

5 [0353]

It is preferable that the oxide semiconductor films 508a and 508c not have a spinel crystal structure. This is because if the oxide semiconductor films 508a and 508c have a spinel crystal structure, constituent elements of the conductive films 512a and 512b might be diffused to the oxide semiconductor film 508b at the interface between the spinel crystal structure and another region. Note that each of the oxide semiconductor films 508a and 508c is preferably a CAAC-OS film, in which case a higher blocking property against constituent elements of the conductive films 512a and 512b, for example, copper elements, can be obtained.

[0354]

The thickness of each of the oxide semiconductor films 508a and 508c is greater than or equal to a thickness that is capable of inhibiting diffusion of the constituent elements of the conductive films 512a and 512b to the oxide semiconductor film 508b, and less than a thickness that inhibits supply of oxygen from the insulating film 514 to the oxide semiconductor film 508b. For example, when the thickness of each of the oxide semiconductor films 508a and 508c is greater than or equal to 10 nm, diffusion of the constituent elements of the conductive films 512a and 512b to the oxide semiconductor film 508b can be inhibited. When the thickness of each of the oxide semiconductor films 508a and 508c is less than or equal to 100 nm, oxygen can be effectively supplied from the insulating film 514 to the oxide semiconductor film 508b.

[0355]

Although the example where an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements, In:Ga:Zn = 1:1:1.2, is used as each of the oxide semiconductor films 508a and 508c is described in this embodiment, one embodiment of the present invention is not limited thereto. For example, an oxide semiconductor film formed using a metal oxide target having an atomic ratio of In:Ga:Zn = 1:1:1, In:Ga:Zn = 1:3:2, In:Ga:Zn = 1:3:4, or In:Ga:Zn = 1:3:6, may be used as each of the oxide semiconductor films 508a and 508c.

[0356]

When the oxide semiconductor films 508a and 508c are formed using a metal oxide target having an atomic ratio of In:Ga:Zn = 1:1:1, the oxide semiconductor films 508a and 508c have an atomic ratio of In:Ga:Zn = 1:β₁ (0 < β₁ ≤ 2):β₂ (0 < β₂ ≤ 3) in some cases. When the oxide semiconductor films 508a and 508c are formed using a metal oxide target having an

atomic ratio of In:Ga:Zn = 1:3:4, the oxide semiconductor films 508a and 508c have an atomic ratio of In:Ga:Zn = 1: β_3 ($1 \leq \beta_3 \leq 5$): β_4 ($2 \leq \beta_4 \leq 6$) in some cases. When the oxide semiconductor films 508a and 508c are formed using a metal oxide target having an atomic ratio of In:Ga:Zn = 1:3:6, the oxide semiconductor films 508a and 508c have an atomic ratio of In:Ga:Zn = 1: β_5 ($1 \leq \beta_5 \leq 5$): β_6 ($4 \leq \beta_6 \leq 8$) in some cases.

[0357]

The drawings illustrate an example where the oxide semiconductor film 508 in the transistor 270 and the oxide semiconductor film 508c in the transistors 270A and 270B have a small thickness in a region that does not overlap with the conductive films 512a and 512b, that is, an example where part of the oxide semiconductor film has a depressed portion. However, one embodiment of the present invention is not limited thereto, and the oxide semiconductor film does not necessarily have a depressed region in a region that does not overlap with the conductive films 512a and 512b. FIGS. 25A and 25B illustrate examples in this case. FIGS. 25A and 25B are cross-sectional views illustrating an example of the transistor. FIGS. 25A and 25B illustrate a structure where the oxide semiconductor film 508 in the transistor 270B does not have a depressed portion.

[0358]

As illustrated in FIGS. 25C and 25D, the oxide semiconductor film 508c may be formed thinner than the oxide semiconductor film 508b in advance, and an insulating film 519 may further be formed over the oxide semiconductor film 508c and the insulating film 507. In that case, openings for connecting the oxide semiconductor film 508c and the conductive films 512a and 512b are formed in the insulating film 519. The insulating film 519 can be formed with the same material and the same forming method as the insulating film 514.

[0359]

The structures of the transistors of this embodiment can be freely combined with each other.

[0360]

This embodiment can be combined with any of the other embodiments as appropriate.

[0361]

(Embodiment 4)

In this embodiment, an oxide semiconductor is described with reference to FIGS. 26A to 26E, FIGS. 27A to 27E, FIGS. 28A to 28D, FIGS. 29A and 29B, and FIG. 30.

[0362]

<Structure of oxide semiconductor>

The structure of an oxide semiconductor is described below.

[0363]

An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis-aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

[0364]

From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. Examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline oxide semiconductor, and an nc-OS.

[0365]

An amorphous structure is generally thought to be isotropic and have no non-uniform structure, to be metastable and not have fixed positions of atoms, to have a flexible bond angle, and to have a short-range order but have no long-range order, for example.

[0366]

This means that a stable oxide semiconductor cannot be regarded as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. In contrast, an a-like OS, which is not isotropic, has an unstable structure that contains a void. Because of its instability, an a-like OS is close to an amorphous oxide semiconductor in terms of physical properties.

[0367]

<CAAC-OS>

First, a CAAC-OS is described.

[0368]

A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

[0369]

Analysis of a CAAC-OS by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an InGaZnO₄ crystal that is classified into the space group R-3m is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. 26A. This peak is derived from the (009) plane of the InGaZnO₄ crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to a surface over which the CAAC-OS film is

formed (also referred to as a formation surface) or the top surface of the CAAC-OS film. Note that a peak sometimes appears at a 2θ of around 36° in addition to the peak at a 2θ of around 31° . The peak at a 2θ of around 36° is derived from a crystal structure that is classified into the space group Fd-3m; thus, it is preferable that this peak not appear in a CAAC-OS.

5 [0370]

On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray is incident on the CAAC-OS in a direction parallel to the formation surface, a peak appears at a 2θ of around 56° . This peak is attributed to the (110) plane of the InGaZnO₄ crystal. When analysis (ϕ scan) is performed with 2θ fixed at around 56° and with the sample
10 rotated using a normal vector to the sample surface as an axis (ϕ axis), as shown in FIG. 26B, a peak is not clearly observed. In contrast, in the case where single crystal InGaZnO₄ is subjected to ϕ scan with 2θ fixed at around 56° , as shown in FIG. 26C, six peaks that are derived from crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of a-axes and b-axes are irregularly oriented in the
15 CAAC-OS.

[0371]

Next, a CAAC-OS analyzed by electron diffraction is described. For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an InGaZnO₄ crystal in a direction parallel to the formation surface of the CAAC-OS, a diffraction
20 pattern (also referred to as a selected-area electron diffraction pattern) shown in FIG. 26D can be obtained. In this diffraction pattern, spots derived from the (009) plane of an InGaZnO₄ crystal are included. Thus, the electron diffraction also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, FIG. 26E shows a
25 diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. 26E, a ring-like diffraction pattern is observed. Thus, the electron diffraction using an electron beam with a probe diameter of 300 nm also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS do not have regular orientation. The first ring in FIG.
30 26E is considered to be derived from the (010) plane, the (100) plane, and the like of the InGaZnO₄ crystal. The second ring in FIG. 26E is considered to be derived from the (110) plane and the like.

[0372]

In a combined analysis image (also referred to as a high-resolution TEM image) of a
35 bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a

transmission electron microscope (TEM), a plurality of pellets can be observed. However, even in the high-resolution TEM image, a boundary between pellets, that is, a grain boundary is not clearly observed in some cases. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

5 [0373]

FIG. 27A shows a high-resolution TEM image of a cross section of the CAAC-OS that is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly referred to as a
10 Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be observed with, for example, an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd.

[0374]

FIG. 27A shows pellets in which metal atoms are arranged in a layered manner. FIG.
15 27A proves that the size of a pellet is greater than or equal to 1 nm or greater than or equal to 3 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc). Furthermore, the CAAC-OS can also be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC). A pellet reflects unevenness of a formation surface or a top surface of the CAAC-OS, and is parallel to the formation surface or the top surface of the CAAC-OS.

20 [0375]

FIGS. 27B and 27C show Cs-corrected high-resolution TEM images of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. 27D and 27E are images obtained through image processing of FIGS. 27B and 27C. The method of image processing is as follows. The image in FIG. 27B is subjected to fast Fourier
25 transform (FFT), so that an FFT image is obtained. Then, mask processing is performed such that a range of from 2.8 nm^{-1} to 5.0 nm^{-1} from the origin in the obtained FFT image remains. After the mask processing, the FFT image is processed by inverse fast Fourier transform (IFFT) to obtain a processed image. The image obtained in this manner is called an FFT filtering image. The FFT filtering image is a Cs-corrected high-resolution TEM image from which a
30 periodic component is extracted, and shows a lattice arrangement.

[0376]

In FIG. 27D, a portion where a lattice arrangement is broken is denoted with a dashed line. A region surrounded by a dashed line is one pellet. The portion denoted with the dashed line is a junction of pellets. The dashed line draws a hexagon, which means that the pellet has a
35 hexagonal shape. Note that the shape of the pellet is not always a regular hexagon but is a

non-regular hexagon in many cases.

[0377]

In FIG. 27E, a dotted line denotes a portion between a region where a lattice arrangement is well aligned and another region where a lattice arrangement is well aligned. A clear crystal grain boundary cannot be observed even in the vicinity of the dotted line. When a lattice point in the vicinity of the dotted line is regarded as a center and surrounding lattice points are joined, a distorted hexagon, pentagon, and/or heptagon can be formed, for example. That is, a lattice arrangement is distorted so that formation of a crystal grain boundary is inhibited. This is probably because the CAAC-OS can tolerate distortion owing to a low density of the atomic arrangement in an a-b plane direction, the interatomic bond distance changed by substitution of a metal element, and the like.

[0378]

As described above, the CAAC-OS has c-axis alignment, its pellets (nanocrystals) are connected in an a-b plane direction, and the crystal structure has distortion. For this reason, the CAAC-OS can also be referred to as an oxide semiconductor including a c-axis-aligned a-b-plane-anchored (CAA) crystal.

[0379]

The CAAC-OS is an oxide semiconductor with high crystallinity. Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancies).

[0380]

Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity.

[0381]

The characteristics of an oxide semiconductor having impurities or defects might be changed by light, heat, or the like. Impurities included in the oxide semiconductor might serve as carrier traps or carrier generation sources, for example. For example, an oxygen vacancy in the oxide semiconductor might serve as a carrier trap or serve as a carrier generation source

when hydrogen is captured therein.

[0382]

The CAAC-OS having small amounts of impurities and oxygen vacancies is an oxide semiconductor film with a low carrier density (specifically, lower than $8 \times 10^{11}/\text{cm}^3$, preferably lower than $1 \times 10^{11}/\text{cm}^3$, and further preferably lower than $1 \times 10^{10}/\text{cm}^3$ and higher than or equal to $1 \times 10^{-9}/\text{cm}^3$). Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states. Thus, the CAAC-OS can be referred to as an oxide semiconductor having stable characteristics.

[0383]

<nc-OS>

Next, an nc-OS is described.

[0384]

Analysis of an nc-OS by XRD is described. For example, when the structure of an nc-OS is analyzed by an out-of-plane method, a peak indicating orientation does not appear. That is, a crystal of an nc-OS does not have orientation.

[0385]

For example, when an electron beam with a probe diameter of 50 nm is incident on a 34-nm-thick region of thinned nc-OS including an InGaZnO₄ crystal in a direction parallel to the formation surface, a ring-shaped diffraction pattern (nanobeam electron diffraction pattern) shown in FIG. 28A is observed. FIG. 28B shows a diffraction pattern (nanobeam electron diffraction pattern) obtained when an electron beam with a probe diameter of 1 nm is incident on the same sample. As shown in FIG. 28B, a plurality of spots are observed in a ring-like region. In other words, ordering in an nc-OS is not observed with an electron beam with a probe diameter of 50 nm but is observed with an electron beam with a probe diameter of 1 nm.

[0386]

Furthermore, an electron diffraction pattern in which spots are arranged in an approximately hexagonal shape is observed in some cases as shown in FIG. 28C when an electron beam having a probe diameter of 1 nm is incident on a region with a thickness of less than 10 nm. This means that an nc-OS has a well-ordered region, i.e., a crystal, in the range of less than 10 nm in thickness. Note that an electron diffraction pattern having regularity is not observed in some regions because crystals are aligned in various directions.

[0387]

FIG. 28D shows a Cs-corrected high-resolution TEM image of a cross section of an nc-OS observed from the direction substantially parallel to the formation surface. In a

high-resolution TEM image, an nc-OS has a region in which a crystal part is observed, such as the part indicated by additional lines in FIG. 28D, and a region in which a crystal part is not clearly observed. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or specifically, greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to 100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

[0388]

As described above, in the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not ordered. Accordingly, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor, depending on an analysis method.

[0389]

Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

[0390]

The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an a-like OS and an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

[0391]

<a-like OS>

An a-like OS has a structure between those of the nc-OS and the amorphous oxide semiconductor.

[0392]

FIGS. 29A and 29B are high-resolution cross-sectional TEM images of an a-like OS.

FIG. 29A is the high-resolution cross-sectional TEM image of the a-like OS at the start of the electron irradiation. FIG. 29B is the high-resolution cross-sectional TEM image of a-like OS after the electron (e^-) irradiation at $4.3 \times 10^8 \text{ e}^-/\text{nm}^2$. FIGS. 29A and 29B show that stripe-like bright regions extending vertically are observed in the a-like OS from the start of the electron irradiation. It can be also found that the shape of the bright region changes after the electron irradiation. Note that the bright region is presumably a void or a low-density region.

[0393]

The a-like OS has an unstable structure because it contains a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

[0394]

An a-like OS, an nc-OS, and a CAAC-OS are prepared as samples. Each of the samples is an In-Ga-Zn oxide.

[0395]

First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

[0396]

It is known that a unit cell of an InGaZnO_4 crystal has a structure in which nine layers including three In-O layers and six Ga-Zn-O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the spacing between lattice fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of InGaZnO_4 in the following description. Each of lattice fringes corresponds to the a-b plane of the InGaZnO_4 crystal.

[0397]

FIG. 30 shows the average size of crystal parts (at 22 points to 30 points) in each sample. Note that the crystal part size corresponds to the length of a lattice fringe. FIG. 30 indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose in obtaining TEM images, for example. As shown in FIG. 30, a crystal part of approximately 1.2 nm (also referred to as an initial nucleus) at the start of TEM observation grows to a size of approximately 1.9 nm at a cumulative electron (e^-) dose of $4.2 \times 10^8 \text{ e}^-/\text{nm}^2$. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of $4.2 \times 10^8 \text{ e}^-/\text{nm}^2$. As shown in FIG. 30, the crystal part sizes in an nc-OS and a CAAC-OS are approximately 1.3 nm and approximately 1.8 nm, respectively, regardless of the cumulative electron dose. For the

electron beam irradiation and TEM observation, a Hitachi H-9000NAR transmission electron microscope was used. The conditions of electron beam irradiation were as follows: the accelerating voltage was 300 kV; the current density was $6.7 \times 10^5 \text{ e}^-/(\text{nm}^2 \cdot \text{s})$; and the diameter of irradiation region was 230 nm.

5 [0398]

In this manner, growth of the crystal part in the a-like OS is sometimes induced by electron irradiation. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

10 [0399]

The a-like OS has a lower density than the nc-OS and the CAAC-OS because it contains a void. Specifically, the density of the a-like OS is higher than or equal to 78.6 % and lower than 92.3 % of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3 % and lower than 100 % of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78 % of the density of the single crystal oxide semiconductor.

[0400]

For example, in the case of an oxide semiconductor having an atomic ratio of In: Ga: Zn = 1:1:1, the density of single crystal InGaZnO_4 with a rhombohedral crystal structure is 6.357 g/cm^3 . Accordingly, in the case of the oxide semiconductor having an atomic ratio of In: Ga: Zn = 1:1:1, the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3 . For example, in the case of the oxide semiconductor having an atomic ratio of In: Ga: Zn = 1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3 .

[0401]

Note that in the case where an oxide semiconductor having a certain composition does not exist in a single crystal structure, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide semiconductor having the desired composition can be calculated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to calculate the density.

35 [0402]

As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a stacked layer including two or more films of an amorphous oxide semiconductor, an a-like OS, an nc-OS, and a CAAC-OS, for example.

5 [0403]

This embodiment can be combined with any of the other embodiments as appropriate.

[Embodiment 5]

[0404]

<CAC composition>

10 Described below is the composition of a cloud aligned complementary oxide semiconductor (CAC-OS) applicable to the present invention.

[0405]

The CAC refers to, for example, a composition of a material in which elements included in an oxide semiconductor are unevenly distributed. The material including unevenly distributed elements has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, preferably greater than or equal to 1 nm and less than or equal to 2 nm, or a similar size. Note that in the following description of an oxide semiconductor, a state in which one or more metal elements are unevenly distributed and regions including the metal element(s) are mixed is referred to as a mosaic pattern or a patch-like pattern. The region has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, preferably greater than or equal to 1 nm and less than or equal to 2 nm, or a similar size.

20 [0406]

For example, of an In-Ga-Zn oxide (hereinafter also referred to as IGZO), CAC-IGZO has a composition in which materials are separated into indium oxide (InO_{X1} , where $X1$ is a real number greater than 0) or indium zinc oxide ($\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$, where $X2$, $Y2$, and $Z2$ are real numbers greater than 0), and gallium oxide (GaO_{X3} , where $X3$ is a real number greater than 0), gallium zinc oxide ($\text{Ga}_{X4}\text{Zn}_{Y4}\text{O}_{Z4}$, where $X4$, $Y4$, and $Z4$ are real numbers greater than 0), or the like, and a mosaic pattern is formed. Then, InO_{X1} and $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ forming the mosaic pattern are evenly distributed in the film. This composition is also referred to as a cloud-like composition.

30 [0407]

That is, the CAC-IGZO is a composite oxide semiconductor with a composition in which a region including GaO_{X3} as a main component and a region including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ or InO_{X1} as a main component are mixed. Note that in this specification, for example, when the atomic ratio of In to an element M in a first region is greater than the atomic ratio of In to an

35

element M in a second region, the first region has higher In concentration than the second region.
[0408]

Note that a compound including In, Ga, Zn, and O is also known as IGZO. Typical examples of IGZO include a crystalline compound represented by $\text{InGaO}_3(\text{ZnO})_{m1}$ ($m1$ is a natural number) and a crystalline compound represented by $\text{In}_{(1+x0)}\text{Ga}_{(1-x0)}\text{O}_3(\text{ZnO})_{m0}$ ($-1 \leq x0 \leq 1$; $m0$ is a given number).
[0409]

The above crystalline compounds have a single crystal structure, a polycrystalline structure, or a CAAC structure. Note that the CAAC structure is a crystal structure in which a plurality of IGZO nanocrystals have c-axis alignment and are connected in the a-b plane direction without alignment.
[0410]

On the other hand, the CAC relates to the material composition. In a CAC material including In, Ga, Zn, and O, regions where nanoparticles including Ga as a main component are partly observed and regions where nanoparticles including In as a main component are partly observed are randomly dispersed to form a mosaic pattern. Therefore, the crystal structure is a secondary element for the CAC composition.
[0411]

Note that in the CAC composition, a stacked-layer structure including two or more films with different atomic ratios is not included. For example, a two-layer structure of a film including In as a main component and a film including Ga as a main component is not included.
[0412]

A boundary between the region including GaO_{x3} as a main component and the region including $\text{In}_{x2}\text{Zn}_{y2}\text{O}_{z2}$ or InO_{x1} as a main component is not clearly observed in some cases.
[0413]

<Analysis of CAC-IGZO>

Next, measurement results of an oxide semiconductor over a substrate by a variety of methods are described.
[0414]

<<Structure of samples and formation method thereof>>

Nine samples of one embodiment of the present invention are described below. The samples are formed at different substrate temperatures and with different ratios of an oxygen gas flow rate in formation of the oxide semiconductor. Note that each sample includes a substrate and an oxide semiconductor over the substrate.
[0415]

A method for forming the samples is described.

[0416]

A glass substrate is used as the substrate. Over the glass substrate, a 100-nm-thick In-Ga-Zn oxide is formed as an oxide semiconductor with a sputtering apparatus. The formation conditions are as follows: the pressure in a chamber is 0.6 Pa, and an oxide target (with an atomic ratio of In:Ga:Zn = 4:2:4.1) is used as a target. The oxide target provided in the sputtering apparatus is supplied with an AC power of 2500 W.

[0417]

As for the conditions in the formation of the oxide of the nine samples, the substrate temperature is set to a temperature that is not increased by intentional heating (hereinafter such a temperature is also referred to as R.T.), to 130 °C, and to 170 °C. The ratio of a flow rate of an oxygen gas to a flow rate of a mixed gas of Ar and oxygen (also referred to as an oxygen gas flow rate ratio) is set to 10 %, 30 %, and 100 %.

[0418]

<<Analysis by X-ray diffraction>>

In this section, results of X-ray diffraction (XRD) measurement performed on the nine samples are described. As an XRD apparatus, D8 ADVANCE manufactured by Bruker AXS is used. The conditions are as follows: scanning is performed by an out-of-plane method at $\theta/2\theta$, the scanning range is 15 deg. to 50 deg., the step width is 0.02 deg., and the scanning speed is 3.0 deg./min.

[0419]

FIG. 36 shows XRD spectra measured by an out-of-plane method. In FIG. 36, the top row shows the measurement results of the samples formed at a substrate temperature of 170 °C; the middle row shows the measurement results of the samples formed at a substrate temperature of 130 °C; the bottom row shows the measurement results of the samples formed at a substrate temperature of R.T. The left column shows the measurement results of the samples formed with an oxygen gas flow rate ratio of 10 %; the middle column shows the measurement results of the samples formed with an oxygen gas flow rate ratio of 30 %; the right column shows the measurement results of the samples formed with an oxygen gas flow rate ratio of 100 %.

[0420]

In the XRD spectra shown in FIG. 36, the higher the substrate temperature at the time of formation is or the higher the oxygen gas flow rate ratio at the time of formation is, the higher the intensity of the peak at around $2\theta = 31^\circ$ is. Note that it is found that the peak at around $2\theta = 31^\circ$ is derived from a crystalline IGZO compound whose c-axes are aligned in a direction

substantially perpendicular to a formation surface or a top surface of the crystalline IGZO compound (such a compound is also referred to as c-axis aligned crystalline (CAAC) IGZO).

[0421]

As shown in the XRD spectra in FIG. 36, as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, a peak becomes less clear. Accordingly, it is found that there are no alignment in the a-b plane direction and c-axis alignment in the measured areas of the samples that are formed at a lower substrate temperature or with a lower oxygen gas flow rate ratio.

[0422]

<<Analysis with electron microscope>>

This section describes the observation and analysis results of the samples formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 % with a high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM). An image obtained with an HAADF-STEM is also referred to as a TEM image.

[0423]

Described are the results of image analysis of plan-view images and cross-sectional images obtained with an HAADF-STEM (also referred to as plan-view TEM images and cross-sectional TEM images, respectively). The TEM images are observed with a spherical aberration corrector function. The HAADF-STEM images are obtained using an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd. under the following conditions: the acceleration voltage is 200 kV, and irradiation with an electron beam with a diameter of approximately 0.1 nm is performed.

[0424]

FIG. 37A is a plan-view TEM image of the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 %. FIG. 37B is a cross-sectional TEM image of the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 %.

[0425]

<<Analysis of electron diffraction patterns>>

This section describes electron diffraction patterns obtained by irradiation of the sample formed at a substrate temperature of R.T. and an oxygen gas flow rate ratio of 10 % with an electron beam with a probe diameter of 1 nm (also referred to as a nanobeam).

[0426]

Electron diffraction patterns of points indicated by black dots a1, a2, a3, a4, and a5 in the plan-view TEM image in FIG. 37A of the sample formed at a substrate temperature of R.T.

and an oxygen gas flow rate ratio of 10 % are observed. Note that the electron diffraction patterns are observed while electron beam irradiation is performed at a constant rate for 35 seconds. FIGS. 37C, 37D, 37E, 37F, and 37G show the results of the points indicated by the black dots a1, a2, a3, a4, and a5, respectively.

5 [0427]

In FIGS. 37C, 37D, 37E, 37F, and 37G, regions with high luminance in a circular (ring) pattern can be shown. Furthermore, a plurality of spots can be shown in a ring-like shape.

[0428]

10 Electron diffraction patterns of points indicated by black dots b1, b2, b3, b4, and b5 in the cross-sectional TEM image in FIG. 37B of the sample formed at a substrate temperature of R.T. and an oxygen gas flow rate ratio of 10 % are observed. FIGS. 37H, 37I, 37J, 37K, and 37L show the results of the points indicated by the black dots b1, b2, b3, b4, and b5, respectively.

[0429]

15 In FIGS. 37H, 37I, 37J, 37K, and 37L, regions with high luminance in a ring pattern can be shown. Furthermore, a plurality of spots can be shown in a ring-like shape.

[0430]

For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an InGaZnO₄ crystal in a direction parallel to the sample surface, a diffraction pattern including a spot derived from the (009) plane of the InGaZnO₄ crystal is
20 obtained. That is, the CAAC-OS has c-axis alignment and the c-axes are aligned in the direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, a ring-like diffraction pattern is shown when an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. That is, it is found that the CAAC-OS has neither a-axis alignment nor b-axis alignment.

25 [0431]

Furthermore, a diffraction pattern like a halo pattern is observed when an oxide semiconductor including a nanocrystal (a nanocrystalline oxide semiconductor (nc-OS)) is subjected to electron diffraction using an electron beam with a large probe diameter (e.g., 50 nm or larger). Meanwhile, bright spots are shown in a nanobeam electron diffraction pattern of the
30 nc-OS obtained using an electron beam with a small probe diameter (e.g., smaller than 50 nm). Furthermore, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of bright spots are shown in a ring-like shape in some cases.

35 [0432]

The electron diffraction pattern of the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 % has regions with high luminance in a ring pattern and a plurality of bright spots appears in the ring-like pattern. Accordingly, the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 % exhibits an electron diffraction pattern similar to that of the nc-OS and does not show alignment in the plane direction and the cross-sectional direction.

[0433]

According to what is described above, an oxide semiconductor formed at a low substrate temperature or with a low oxygen gas flow rate ratio is likely to have characteristics distinctly different from those of an oxide semiconductor film having an amorphous structure and an oxide semiconductor film having a single crystal structure.

[0434]

<<Elementary analysis>>

This section describes the analysis results of elements included in the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 %. For the analysis, by energy dispersive X-ray spectroscopy (EDX), EDX mapping images are obtained. An energy dispersive X-ray spectrometer AnalysisStation JED-2300T manufactured by JEOL Ltd. is used as an elementary analysis apparatus in the EDX measurement. A Si drift detector is used to detect an X-ray emitted from the sample.

[0435]

In the EDX measurement, an EDX spectrum of a point is obtained in such a manner that electron beam irradiation is performed on the point in a detection target region of a sample, and the energy of characteristic X-ray of the sample generated by the irradiation and its frequency are measured. In this embodiment, peaks of an EDX spectrum of the point are attributed to electron transition to the L shell in an In atom, electron transition to the K shell in a Ga atom, and electron transition to the K shell in a Zn atom and the K shell in an O atom, and the proportions of the atoms in the point are calculated. An EDX mapping image indicating distributions of proportions of atoms can be obtained through the process in an analysis target region of a sample.

[0436]

FIGS. 38A to 38C show EDX mapping images in a cross section of the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 %. FIG. 38A shows an EDX mapping image of Ga atoms. The proportion of the Ga atoms in all the atoms is 1.18 atomic% to 18.64 atomic%. FIG. 38B shows an EDX mapping image of In atoms. The proportion of the In atoms in all the atoms is 9.28 atomic% to 33.74 atomic%. FIG. 38C shows

an EDX mapping image of Zn atoms. The proportion of the Zn atoms in all the atoms is 6.69 atomic% to 24.99 atomic%. FIGS. 38A to 38C show the same region in the cross section of the sample formed at a substrate temperature of R.T. and with an oxygen flow rate ratio of 10 %. In the EDX mapping images, the proportion of an element is indicated by grayscale: the more measured atoms exist in a region, the brighter the region is; the less measured atoms exist in a region, the darker the region is. The magnification of the EDX mapping images in FIGS. 38A to 38C is 7200000 times.

[0437]

The EDX mapping images in FIGS. 38A to 38C show relative distribution of brightness indicating that each element has a distribution in the sample formed at a substrate temperature of R.T. and with an oxygen gas flow rate ratio of 10 %. Areas surrounded by solid lines and areas surrounded by dashed lines in FIGS. 38A to 38C are examined.

[0438]

In FIG. 38A, a relatively dark region occupies a large area in the area surrounded by the solid line, while a relatively bright region occupies a large area in the area surrounded by the dashed line. In FIG. 38B, a relatively bright region occupies a large area in the area surrounded by the solid line while a relatively dark region occupies a large area in the area surrounded by the dashed line.

[0439]

That is, the areas surrounded by the solid lines are regions including a relatively large number of In atoms and the areas surrounded by the dashed lines are regions including a relatively small number of In atoms. In FIG. 38C, the right portion of the area surrounded by the solid line is relatively bright and the left portion thereof is relatively dark. Thus, the area surrounded by the solid line is a region including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$, InO_{X1} , and the like as main components.

[0440]

The area surrounded by the solid line is a region including a relatively small number of Ga atoms and the area surrounded by the dashed line is a region including a relatively large number of Ga atoms. In FIG. 38C, the upper left portion of the area surrounded by the dashed line is relatively bright and the lower right portion thereof is relatively dark. Thus, the area surrounded by the dashed line is a region including GaO_{X3} , $\text{Ga}_{X4}\text{Zn}_{Y4}\text{O}_{Z4}$, and the like as main components.

[0441]

Furthermore, as shown in FIGS. 38A to 38C, the In atoms are relatively more uniformly distributed than the Ga atoms, and regions including InO_{X1} as a main component is seemingly

joined to each other through a region including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ as a main component. Thus, the regions including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ and InO_{X1} as a main component extend like a cloud.

[0442]

An In-Ga-Zn oxide having a composition in which the regions including GaO_{X3} as a main component and the regions including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ or InO_{X1} as a main component are unevenly distributed and mixed can be referred to as CAC-IGZO.

[0443]

The crystal structure of CAC-IGZO includes an nc structure. In an electron diffraction pattern of the CAC-IGZO with the nc structure, several or more bright spots appear in addition to bright spots derived from IGZO including a single crystal, a polycrystal, or a CAAC. Alternatively, in addition to the several or more bright spots, the crystal structure is defined as having high luminance regions appearing in a ring pattern.

[0444]

As shown in FIGS. 38A to 38C, each of the regions including GaO_{X3} as a main component and the regions including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ or InO_{X1} as a main component has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm. Note that it is preferable that a diameter of a region including each metal element as a main component be greater than or equal to 1 nm and less than or equal to 2 nm in the EDX mapping images.

[0445]

As described above, CAC-IGZO has a structure different from that of an IGZO compound in which metal elements are evenly distributed, and has characteristics different from those of the IGZO compound. That is, in CAC-IGZO, regions including GaO_{X3} or the like as a main component and regions including $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ or InO_{X1} as a main component are separated to form a mosaic pattern. Accordingly, when CAC-IGZO is used for a semiconductor element, the property derived from GaO_{X3} or the like and the property derived from $\text{In}_{X2}\text{Zn}_{Y2}\text{O}_{Z2}$ or InO_{X1} complement each other, whereby high on-state current (I_{on}) and high field-effect mobility (μ) can be achieved.

[0446]

A semiconductor element including CAC-IGZO has high reliability. Thus, CAC-IGZO is suitably used in a variety of semiconductor devices typified by a display.

[0447]

At least part of this embodiment can be implemented in combination with any of the other embodiments described in this specification as appropriate.

[0448]

(Embodiment 6)

In this embodiment, a touch panel module and electronic devices that include the input/output device of one embodiment of the present invention are described with reference to FIG. 31, FIGS. 32A to 32H, and FIGS. 33A and 33B.

5 [0449]

In a touch panel module 8000 illustrated in FIG. 31, a touch panel 8004 connected to an FPC 8003, a frame 8009, a printed board 8010, and a battery 8011 are provided between an upper cover 8001 and a lower cover 8002.

[0450]

10 The input/output device of one embodiment of the present invention can be used for the touch panel 8004, for example.

[0451]

The shapes and sizes of the upper cover 8001 and the lower cover 8002 can be changed as appropriate in accordance with the size of the touch panel 8004.

15 [0452]

In the case of a transmissive liquid crystal element, a backlight 8007 may be provided as illustrated in FIG. 31. The backlight 8007 includes a light source 8008. Note that although a structure in which the light source 8008 is provided over the backlight 8007 is illustrated in FIG. 31, one embodiment of the present invention is not limited to this structure. For example, a structure in which the light source 8008 is provided at an end portion of the backlight 8007 and a light diffusion plate is further provided may be employed. Note that the backlight 8007 needs not be provided in the case where a self-luminous light-emitting element such as an organic EL element is used or in the case where a reflective panel or the like is employed.

[0453]

25 The frame 8009 protects the touch panel 8004 and serves as an electromagnetic shield for blocking electromagnetic waves generated by the operation of the printed board 8010. The frame 8009 can also serve as a radiator plate.

[0454]

30 The printed board 8010 is provided with a power supply circuit and a signal processing circuit for outputting a video signal and a clock signal. As a power source for supplying electric power to the power supply circuit, an external commercial power source or a power source using the battery 8011 provided separately may be used. The battery 8011 can be omitted in the case of using a commercial power source.

[0455]

35 The touch panel 8004 can be additionally provided with a component such as a

polarizing plate, a retardation plate, or a prism sheet.

[0456]

FIGS. 32A to 32H and FIGS. 33A and 33B illustrate electronic devices. These electronic devices can each include a housing 5000, a display portion 5001, a speaker 5003, an LED lamp 5004, operation keys 5005 (including a power switch or an operation switch), a connection terminal 5006, a sensor 5007 (a sensor having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, odor, or infrared rays), a microphone 5008, and the like.

[0457]

FIG. 32A illustrates a mobile computer, which can include a switch 5009, an infrared port 5010, and the like in addition to the above components. FIG. 32B illustrates a portable image reproducing device provided with a recording medium (e.g., a DVD reproducing device), which can include a second display portion 5002, a recording medium reading portion 5011, and the like in addition to the above components. FIG. 32C illustrates a television device, which can include a stand 5012 and the like in addition to the above components. The television device can be operated by an operation switch of the housing 5000 or a separate remote controller 5013. With operation keys of the remote controller 5013, channels and volume can be controlled, and images displayed on the display portion 5001 can be controlled. The remote controller 5013 may be provided with a display portion for displaying data output from the remote controller 5013. FIG. 32D illustrates a portable game machine, which can include the recording medium reading portion 5011 and the like in addition to the above components. FIG. 32E illustrates a digital camera that has a television reception function and can include an antenna 5014, a shutter button 5015, an image receiving portion 5016, and the like in addition to the above components. FIG. 32F illustrates a portable game machine, which can include the second display portion 5002, the recording medium reading portion 5011, and the like in addition to the above components. FIG. 32G illustrates a portable television receiver, which can include a charger 5017 capable of transmitting and receiving signals, and the like in addition to the above components. FIG. 32H illustrates a wrist-watch-type information terminal, which can include a band 5018, a clasp 5019, and the like in addition to the above components. The display portion 5001 mounted in the housing 5000 also serving as a bezel includes a non-rectangular display region. The display portion 5001 can display an icon 5020 indicating time, another icon 5021, and the like. FIG. 33A illustrates a digital signage. FIG. 33B illustrates a digital signage mounted on a cylindrical pillar.

[0458]

The electronic devices illustrated in FIGS. 32A to 32H and FIGS. 33A and 33B can have a variety of functions, for example, a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on a display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of controlling processing with a variety of software (programs), a wireless communication function, a function of being connected to a variety of computer networks with a wireless communication function, a function of transmitting and receiving a variety of data with a wireless communication function, and a function of reading a program or data stored in a recording medium and displaying the program or data on a display portion. Furthermore, the electronic device including a plurality of display portions can have a function of displaying image information mainly on one display portion while displaying text information mainly on another display portion, a function of displaying a three-dimensional image by displaying images where parallax is considered on a plurality of display portions, or the like. Furthermore, the electronic device including an image receiving portion can have a function of photographing a still image, a function of photographing a moving image, a function of automatically or manually correcting a photographed image, a function of storing a photographed image in a recording medium (an external recording medium or a recording medium incorporated in the camera), a function of displaying a photographed image on a display portion, or the like. Note that the functions of the electronic devices illustrated in FIGS. 32A to 32H and FIGS. 33A and 33B are not limited thereto, and the electronic devices can have a variety of functions.

[0459]

The electronic devices in this embodiment each include a display portion for displaying some kind of information. The input/output device of one embodiment of the present invention can be used for the display portion.

[0460]

This embodiment can be combined with any of the other embodiments as appropriate.

[Example]

[0461]

In this example, an input/output device of one embodiment of the present invention is described.

[0462]

First, the specifications of the input/output device of this example are described. The size was 4.3 inch (diagonal). The number of effective pixels was 1080 (H) × 1920 (V) corresponding to full high definition (FAHD). The pixel size was 49.5 μm (H) × 49.5 μm (V).

The external panel size was 69.76mm (H) × 141.4mm (V). The size of each of the display region and the sensor region was 53.46 mm (H) × 95.04 mm (V). The resolution was 513 ppi. A channel-etched (CE) transistor including an oxide semiconductor in a channel formation region was used.

5 [0463]

The input/output device of this example can serve as a transmissive liquid crystal display device. A liquid crystal element using an FFS mode was used as the display element. A color filter (CF) method was used as the coloring method. The aperture ratio was 48.0 %. The drive frequency was 60 Hz. An analog line sequential video signal format was used as the video signal format.

10

[0464]

The gate driver was incorporated. A COF was used for the source driver.

[0465]

A projected capacitive (mutual capacitive) sensor element was used as the sensor element. A common electrode of the liquid crystal element also serves as an electrode of the sensor element. The number of sensor units was 18 (H) × 32 (V). Specifically, 32 conductive films 56a in FIG. 9A and 18 conductive films 58 in FIG. 9A were prepared. The size of one sensor unit was 2.970 mm × 2.970 mm. The size of one conductive film 56b in FIG. 9A corresponded to 30 × 60 pixels. The size of one conductive film 56a in FIG. 9A corresponded to 30 × 1080 pixels.

15

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[0466]

The one frame period shown in FIG. 8E was 16.667 ms, the writing period was 8.333 ms, and the two sensing periods were each 4.167 ms.

[0467]

A schematic cross-sectional view of the input/output device of this embodiment corresponds to FIG. 1B, and Embodiment 1 can be referred to for the detail.

25

[0468]

As the substrate 211, an approximately 0.7-mm-thick glass substrate was used. As the substrate 261, a glass substrate with a thickness of approximately 0.1 mm, approximately 0.2 mm, or approximately 0.3 mm was used. As the gate electrode 221, a stacked-layer structure of a tungsten nitride film and a copper film was used. As the insulating film 213, a stacked-layer structure of a silicon nitride film and a silicon oxynitride was used. For the oxide semiconductor film 223, a CAAC-IGZO that was one of CAAC-OSs was used. The oxide semiconductor film 223 had a two-layer structure in which two layers were formed using sputtering targets having different atomic ratios of metal elements. The total thickness of the

30

35

two layers was approximately 25 nm. The oxide semiconductor film 223 and the oxide conductor film 227 were formed using an In-Ga-Zn oxide. The oxide conductor film 227 had a single-layer structure and had a thickness of approximately 100 nm. The source electrode 225a and the drain electrode 225b had a stacked-layer structure of a tungsten film, an aluminum film, and a titanium film. As the insulating film 215, a silicon oxynitride film was used. As the insulating film 217, a silicon nitride film was used. As the insulating film 219, an acrylic film was used. As each of the conductive films 251 and 252, an approximately 100-nm-thick indium tin oxide film containing silicon was used. As the insulating film 253, a silicon nitride film was used. As the liquid crystal 249, a negative liquid crystal was used. An approximately 200- μ m-thick polarizing film was attached to a surface of the substrate 261. In this example, two input/output devices were fabricated: an input/output device in which an approximately 100-nm-thick APC film was used as the conductive film 255 and an input/output device in which an approximately 200-nm-thick Ti film was used as the conductive film 255.

[0469]

FIG. 35 is a photograph showing the display state of the input/output device in this example. In FIG. 35, FPCs were connected to a right side and a top side (not shown) of the display region. For the input/output device in FIG. 35, an approximately 0.3-mm-thick glass substrate was used as the substrate 261. As the conductive film 255, an approximately 100-nm-thick APC film was used. As shown in FIG. 35, with one embodiment of the present invention, an input/output device capable of favorable display was able to be fabricated. Furthermore, the input/output device in FIG. 35 had a touch sensor having a favorable detection sensitivity and was able to sense multiple points simultaneously.

[0470]

Stripe-like display unevenness was observed in some images. The width of the stripe was almost the same as the width of the conductive film 56a (a length in the Y direction in FIG. 9A). Thus, to make the parasitic capacitance of the conductive films 56a and 56b even, the widths of the conductive films 56a and 56b were changed. The size of one conductive film 56b after the change corresponded to 21×60 pixels. The size of one conductive film 56a after the change corresponded to 39×1080 pixels. Accordingly, the resistivity of the conductive film 56b was changed from 1.66 k Ω to 1.19 k Ω , and the capacitance of the conductive film 56b was changed from 534 pF to 674 pF. The resistivity of the conductive film 56a was changed from 0.86 k Ω to 1.35 k Ω , and the capacitance of the conductive film 56b was changed from 930pF to 684pF. By making the parasitic capacitance of the conductive films 56a and 56b even, the display unevenness was reduced, so that a favorable display was able to be performed. As compared to the case where a signal for touch sensing is input to the conductive film 56b, the

display unevenness was reduced and thus a favorable display was able to be performed in the case where a signal for touch sensing is input to the conductive film 56a and the conductive film 56b alternately.

5 REFERENCE NUMERALS

[0471]

56: conductive film, 56a: conductive film, 56b: conductive film, 57a: auxiliary wiring, 57b: auxiliary wiring, 58: conductive film, 60: pixel, 60a: subpixel, 60b: subpixel, 60c: subpixel, 106: insulating film, 107: insulating film, 114: insulating film, 116: insulating film, 141: opening, 142: opening, 193: target, 194: plasma, 201a: transistor, 201b: transistor, 201c: transistor, 203: transistor, 203a: transistor, 203b: transistor, 205a: connection portion, 205b: connection portion, 207: liquid crystal element., 207a: liquid crystal element., 207b: liquid crystal element., 211: substrate, 213: insulating film, 215: insulating film, 217: insulating film, 218: insulating film, 219: insulating film, 221: gate electrode, 223: oxide semiconductor film, 225a: source electrode, 225b: drain electrode, 226: conductive film, 227: oxide conductive film, 227a: oxide semiconductor film, 231: conductive film, 233: conductive film, 235: conductive film, 241: coloring film, 243: light-blocking film, 245: insulating film, 247: spacer, 249: liquid crystal., 251: conductive film, 252: conductive film, 253: insulating film, 254: conductive film, 255: conductive film, 257: connector, 259: FPC, 261: substrate, 265: bonding layer, 267: connector, 268: IC, 269: FPC, 270: transistor, 270A: transistor, 270B: transistor, 273: pixel, 275: conductive film, 277: region, 300: input/output device, 301: display portion, 302: scan line driver circuit, 303: pixel, 502: substrate, 504: conductive film, 506: insulating film, 507: insulating film, 508: oxide semiconductor film, 508a: oxide semiconductor film, 508b: oxide semiconductor film, 508c: oxide semiconductor film, 511a: oxide semiconductor film, 511b: oxide conductive film, 512a: conductive film, 512b: conductive film, 514: insulating film, 516: insulating film, 518: insulating film, 519: insulating film, 552a: opening, 552b: opening, 552c: opening, 3501: wiring, 3502: wiring, 3503: transistor, 3504: liquid crystal element., 3510: wiring, 3510_1: wiring, 3510_2: wiring, 3511: wiring, 3515_1: block, 3515_2: block, 3516: block, 5000: housing, 5001: display portion, 5002: display portion, 5003: speaker, 5004: LED lamp, 5005: operation keys, 5006: connection terminal, 5007: sensor, 5008: microphone, 5009: switch, 5010: infrared port, 5011: recording medium reading portion, 5012: stand, 5013: remote controller, 5014: antenna, 5015: shutter button, 5016: image receiving portion, 5017: charger, 5018: band, 5019: clasp, 5020: icon, 5021: icon, 6500: touch panel module, 6501: circuit unit, 6502: signal line driver circuit, 6503: sensor driver circuit., 6504: detection circuit, 6505: timing controller, 6506: image processing circuit, 6510: touch panel, 6511: display portion, 6512: input portion, 6513: scan line

driver circuit, 6520: IC, 6530: IC, 6531: substrate, 6532: counter substrate, 6533: FPC, 6534: PCB, 6540: CPU, 8000: touch panel module, 8001: upper cover, 8002: lower cover, 8003: FPC, 8004: touch panel, 8007: backlight, 8008: light source, 8009: frame, 8010: printed board, 8011: battery

5

This application is based on Japanese Patent Application serial no. 2015-110612 filed with Japan Patent Office on May 29, 2015, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. An input/output device comprising:
a first pixel electrode;
5 a second pixel electrode;
a first common electrode;
a second common electrode;
a liquid crystal;
a first insulating film;
10 a second insulating film; and
a transistor,
wherein the first common electrode serves as one electrode of a sensor element,
wherein the second common electrode serves as the other electrode of the sensor
element,
15 wherein the transistor comprises a first gate, a semiconductor layer over the first gate,
and a second gate over the semiconductor layer,
wherein the semiconductor layer comprises a channel formation region that comprises
an oxide semiconductor,
wherein the second gate comprises an oxide conductor,
20 wherein the oxide conductor comprises one or more kinds of metal elements comprised
in the oxide semiconductor,
wherein the first insulating film is positioned over the second gate,
wherein the first pixel electrode, the second pixel electrode, the first common electrode,
and the second common electrode are positioned over the first insulating film,
25 wherein the first pixel electrode overlaps with the first common electrode with the
second insulating film positioned between the first pixel electrode and the first common
electrode,
wherein the second pixel electrode overlaps with the second common electrode with the
second insulating film positioned between the second pixel electrode and the second common
30 electrode,
wherein the liquid crystal is positioned over the first pixel electrode, the second pixel
electrode, the first common electrode, and the second common electrode,
wherein the first pixel electrode and the second pixel electrode are apart from each other
and are positioned on a same plane, and
35 wherein the first common electrode and the second common electrode are apart from

each other and are positioned on a same plane.

2. The input/output device according to claim 1,

further comprising a second transistor,

wherein a source or a drain of one of the transistor and the second transistor is electrically connected to the first pixel electrode, and

wherein a source or a drain of the other of the transistor and the second transistor is electrically connected to the second pixel electrode.

3. The input/output device according to claim 1, wherein the transistor is positioned in a driver circuit portion.

4. The input/output device according to claim 1, wherein the second gate is electrically connected to the first gate.

5. The input/output device according to claim 1,

wherein the second insulating film is positioned over the first pixel electrode and the second pixel electrode, and

wherein the first common electrode and the second common electrode are positioned over the second insulating film.

6. The input/output device according to claim 1, wherein the first pixel electrode, the second pixel electrode, the first common electrode, and the second common electrode each comprise one or more kinds of metal elements comprised in the oxide semiconductor.

7. The input/output device according to claim 1, wherein the oxide semiconductor, the oxide conductor, the first pixel electrode, the second pixel electrode, the first common electrode, and the second common electrode each comprise an oxide comprising indium.

8. The input/output device according to claim 1, wherein the first pixel electrode, the second pixel electrode, the first common electrode, and the second common electrode each have a function of transmitting visible light.

9. The input/output device according to claim 1,

wherein the oxide semiconductor and the oxide conductor each comprise an In- M_1 -Zn

oxide, and

wherein the M_1 is Al, Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf.

10. The input/output device according to claim 1,

5 further comprising a first conductive film between the first insulating film and the first common electrode,

wherein the first conductive film has a lower resistivity than the first common electrode, and

wherein the first conductive film is electrically connected to the first common electrode.

11. The input/output device according to claim 10,

further comprising a second conductive film between the first insulating film and the second common electrode,

15 wherein the second conductive film has a lower resistivity than the second common electrode,

wherein the second conductive film is electrically connected to the second common electrode, and

wherein the first conductive film and the second conductive film are apart from each other and are positioned on a same plane.

12. The input/output device according to claim 11,

further comprising a light-blocking film,

25 wherein the light-blocking film overlaps with one of the first conductive film and the second conductive film with the liquid crystal positioned between the light-blocking film and the one of the first conductive film and the second conductive film.

13. An electronic device comprising:

the input/output device according to claim 1; and

30 an antenna, a battery, a housing, a speaker, a microphone, an operation switch, or an operation button.

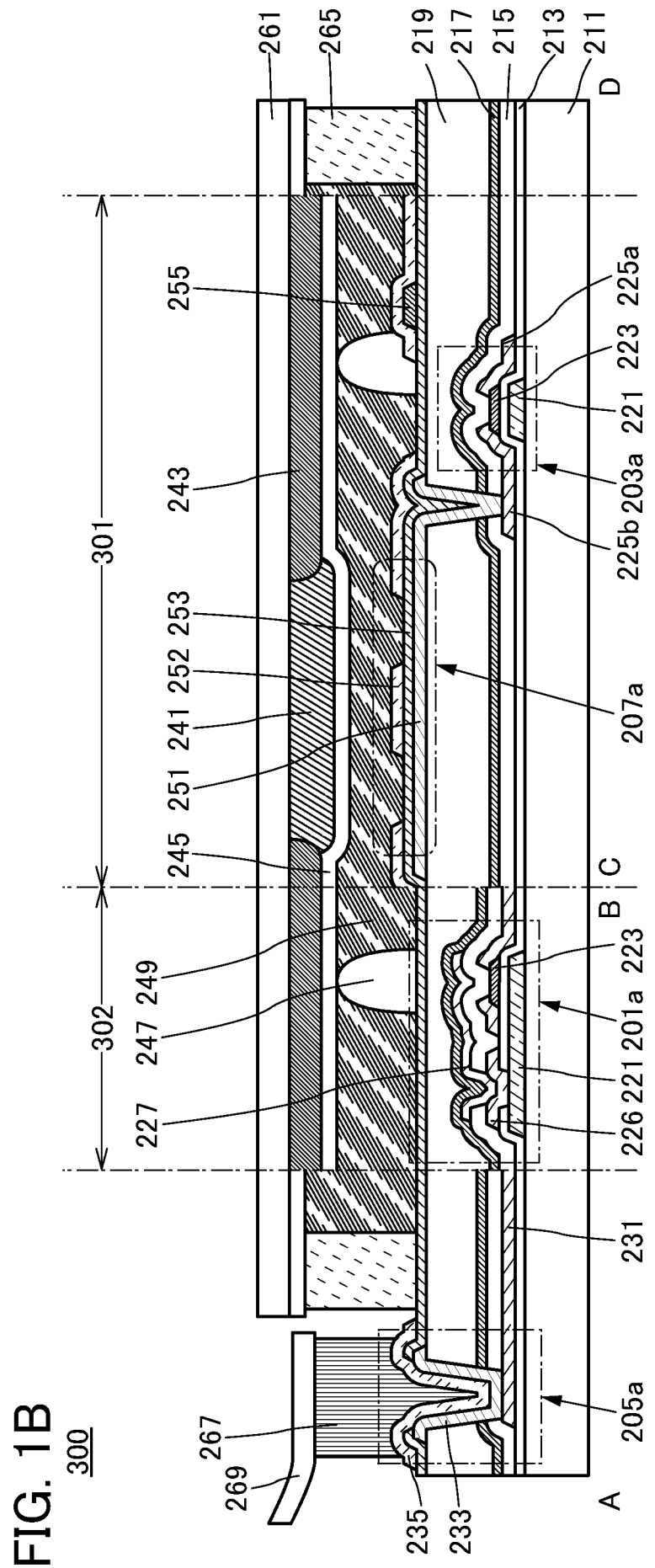
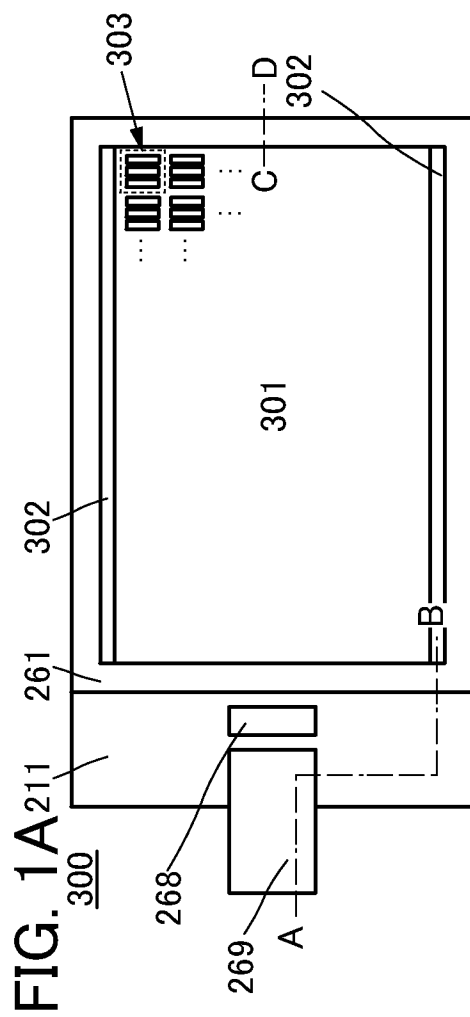


FIG. 2A

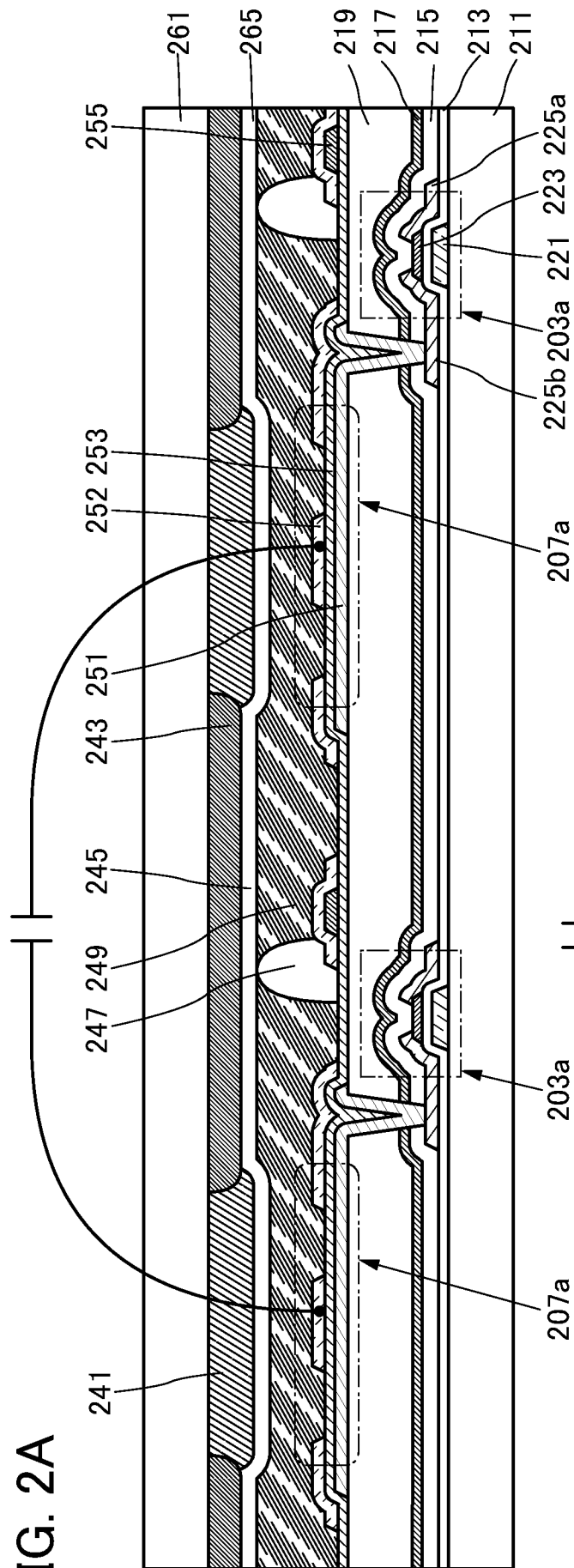


FIG. 2B

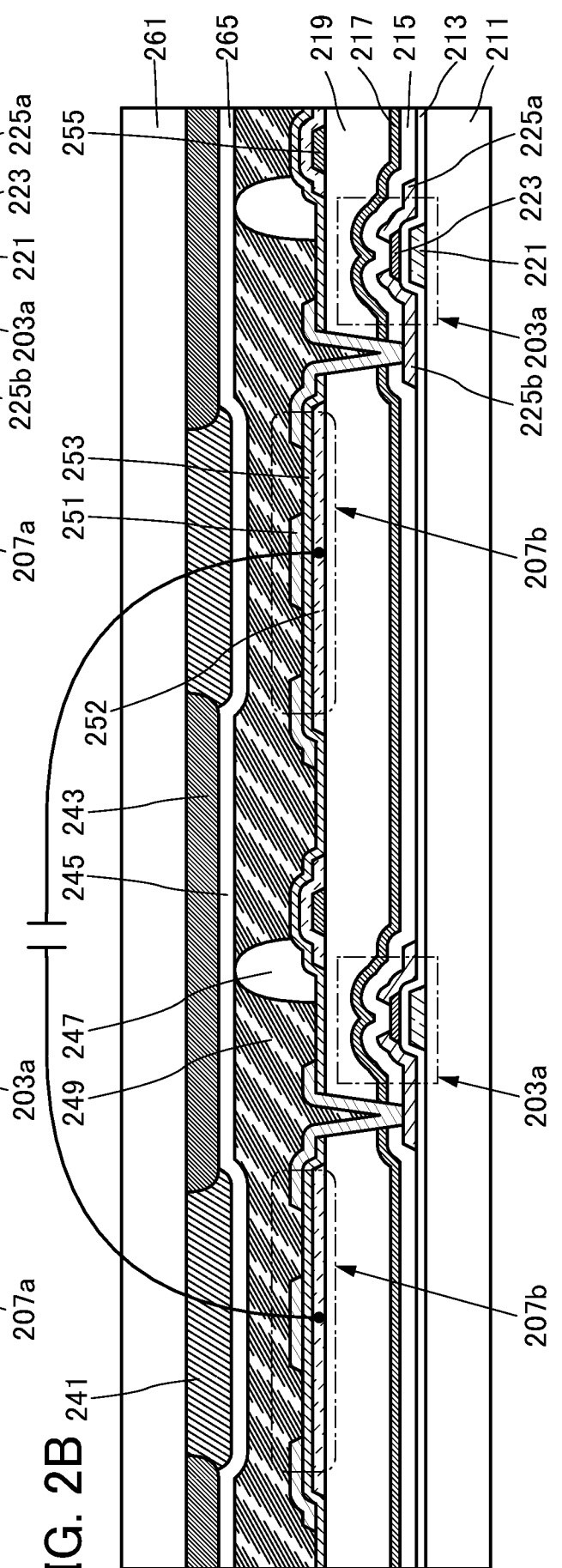


FIG. 3A

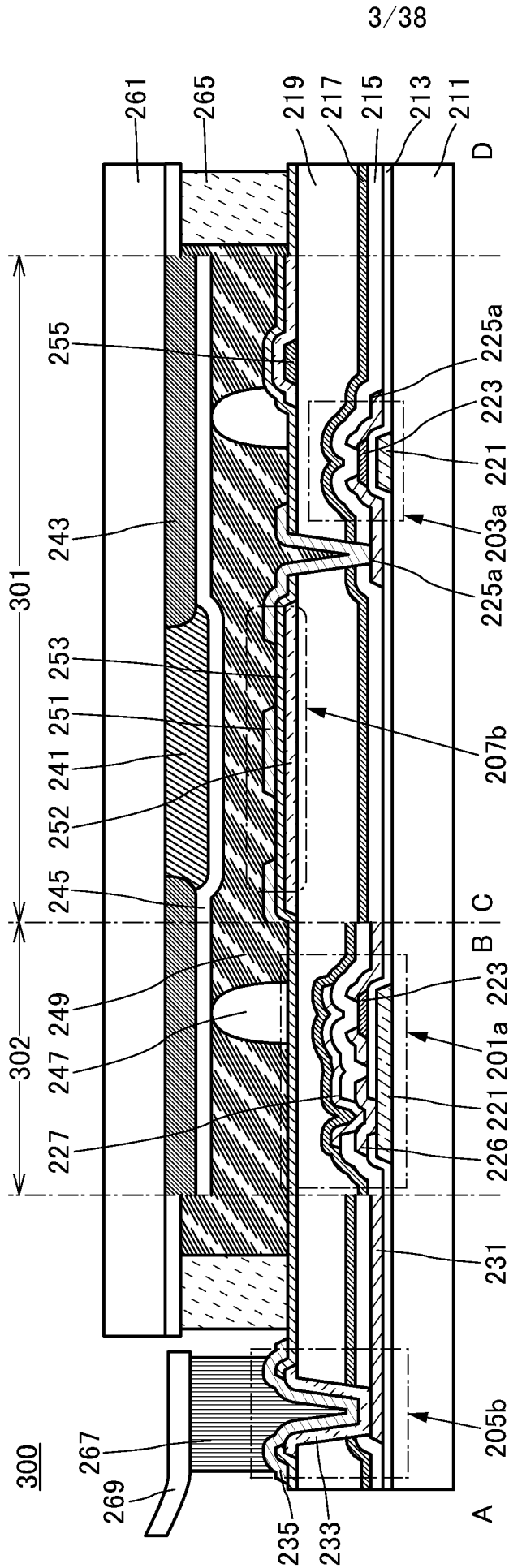


FIG. 3B

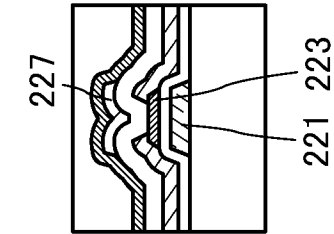


FIG. 3C

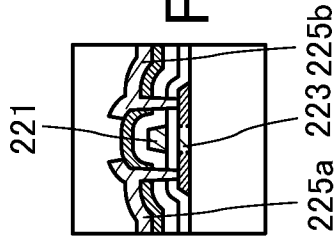


FIG. 3D

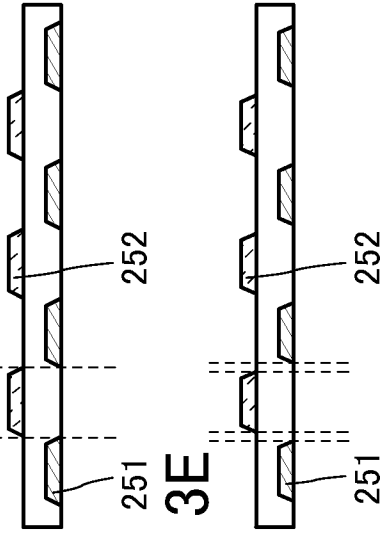


FIG. 3E

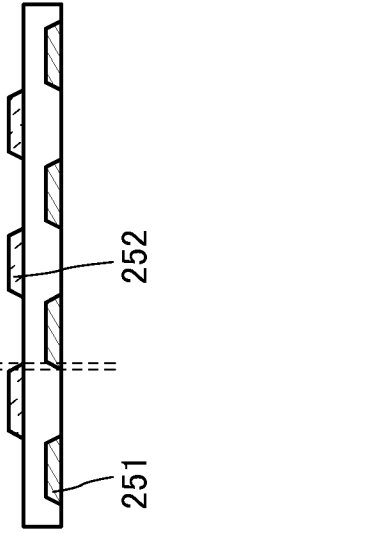


FIG. 3F

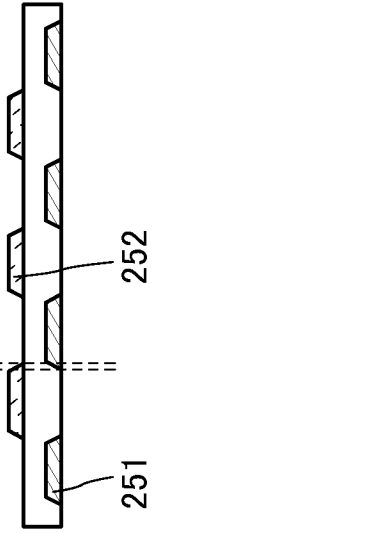


FIG. 4

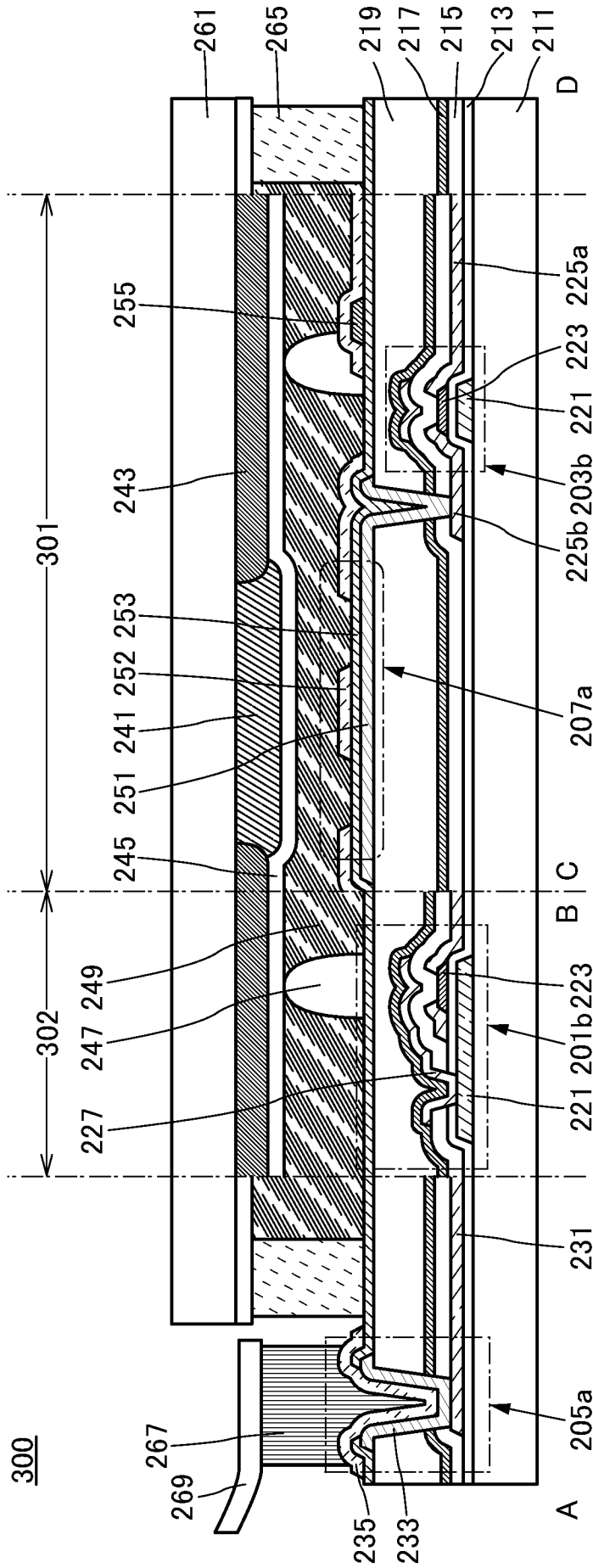


FIG. 5

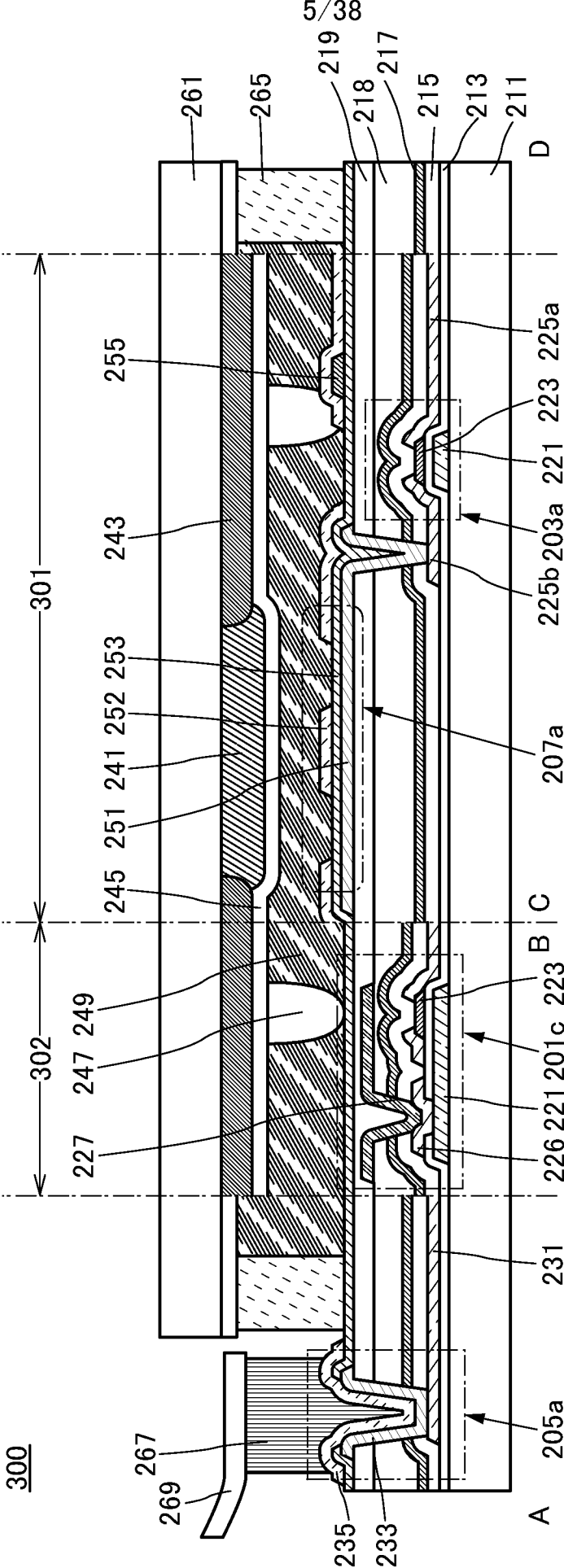


FIG. 6

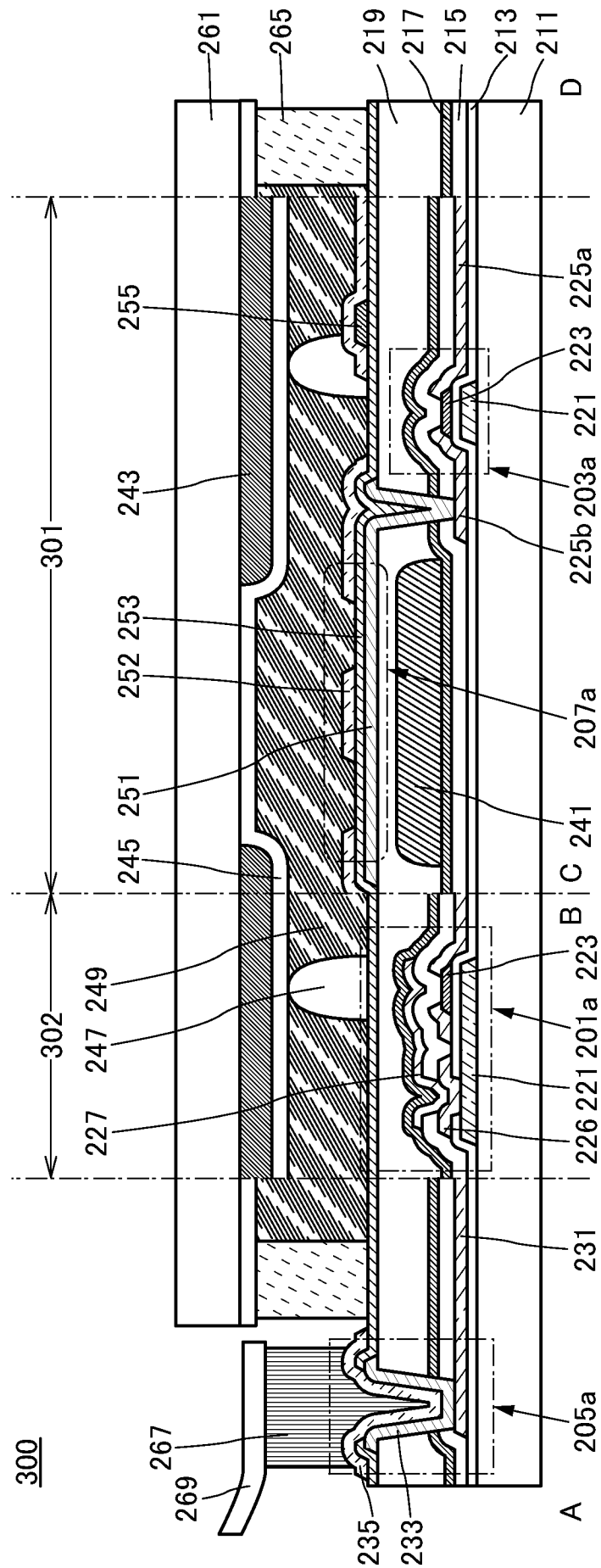


FIG. 7A

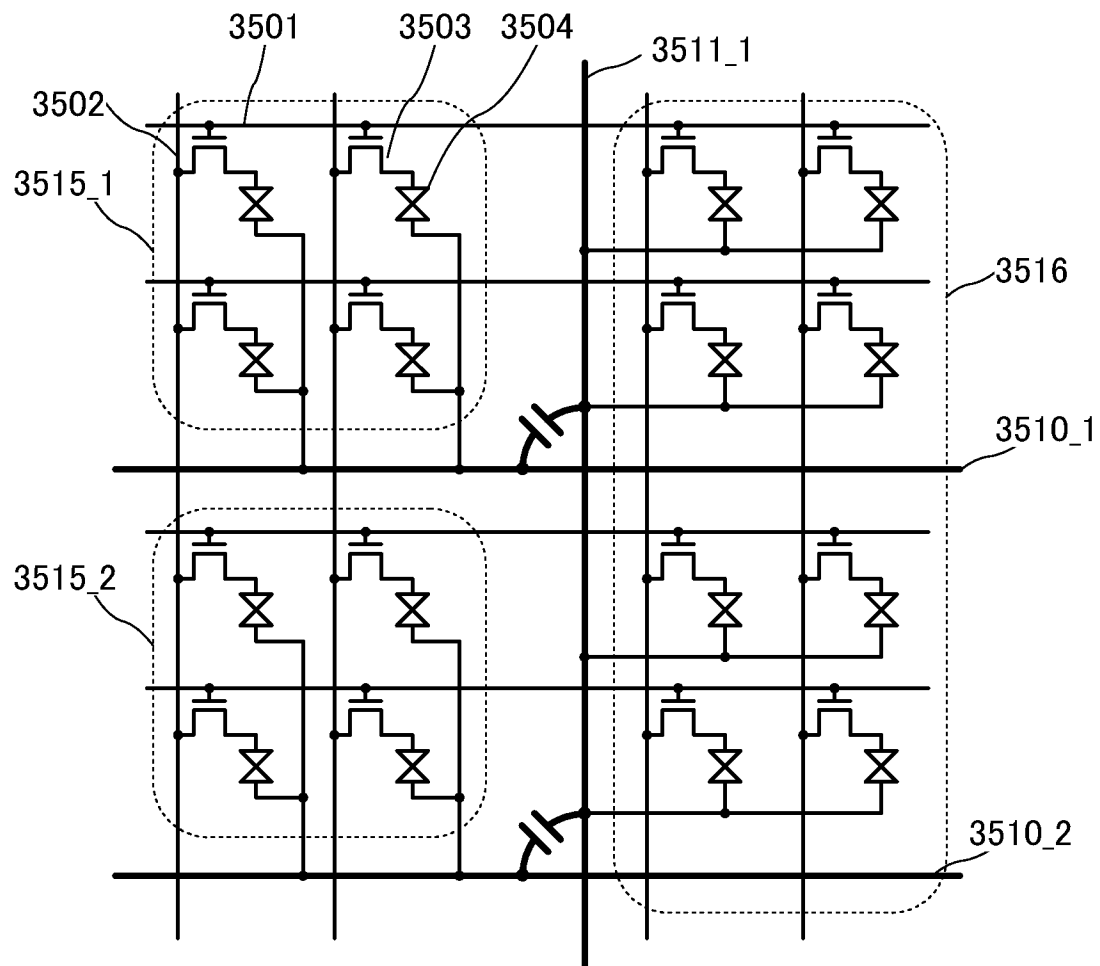
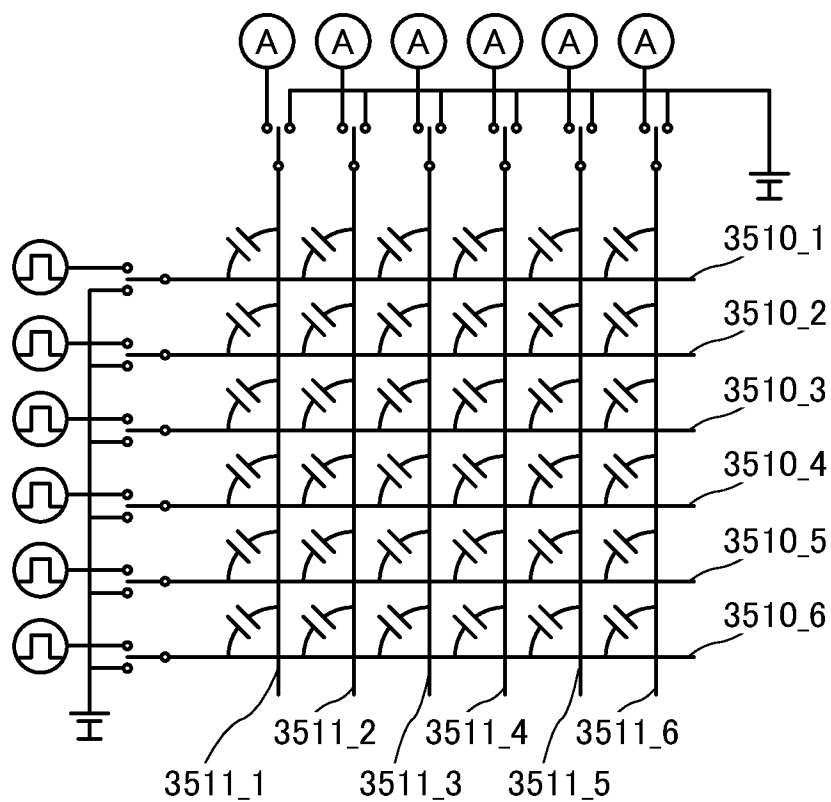


FIG. 7B



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FIG. 8A

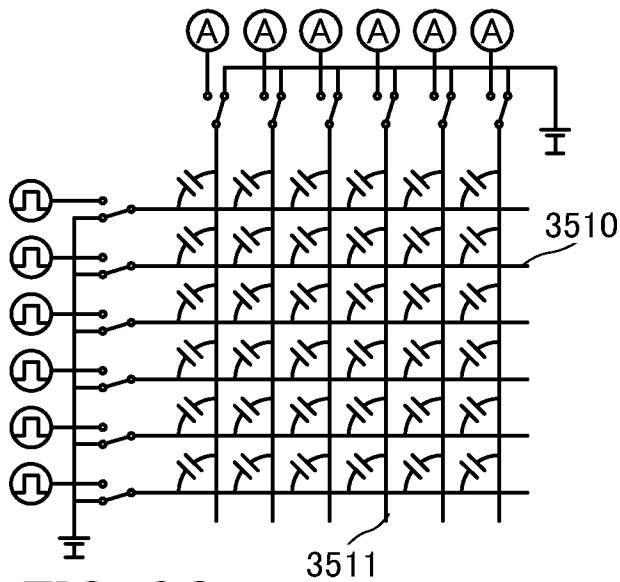


FIG. 8B

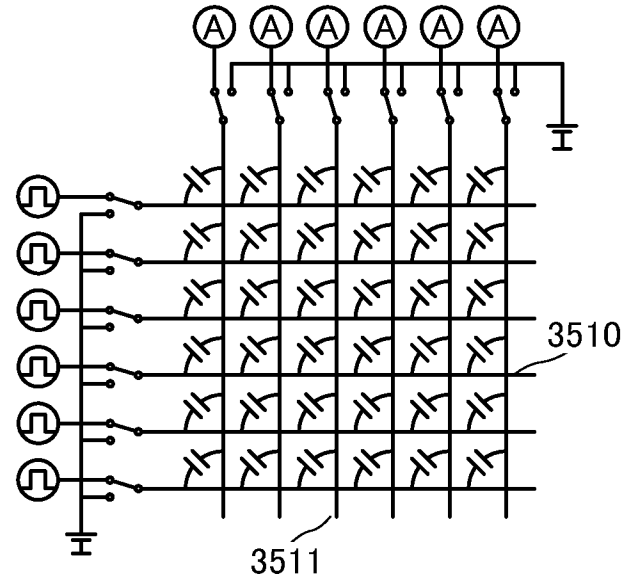


FIG. 8C

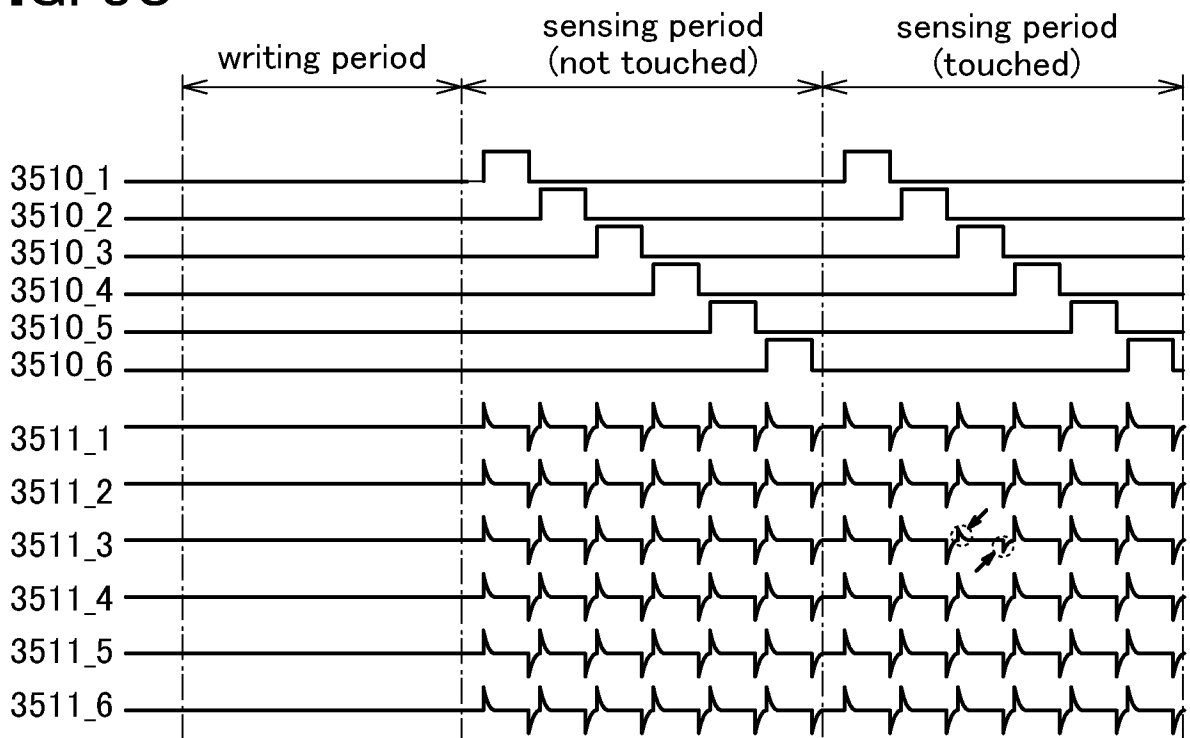
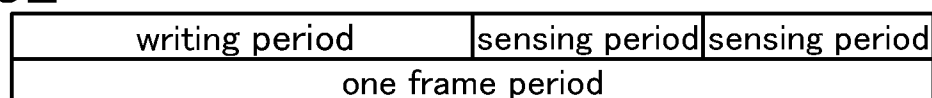


FIG. 8D



FIG. 8E



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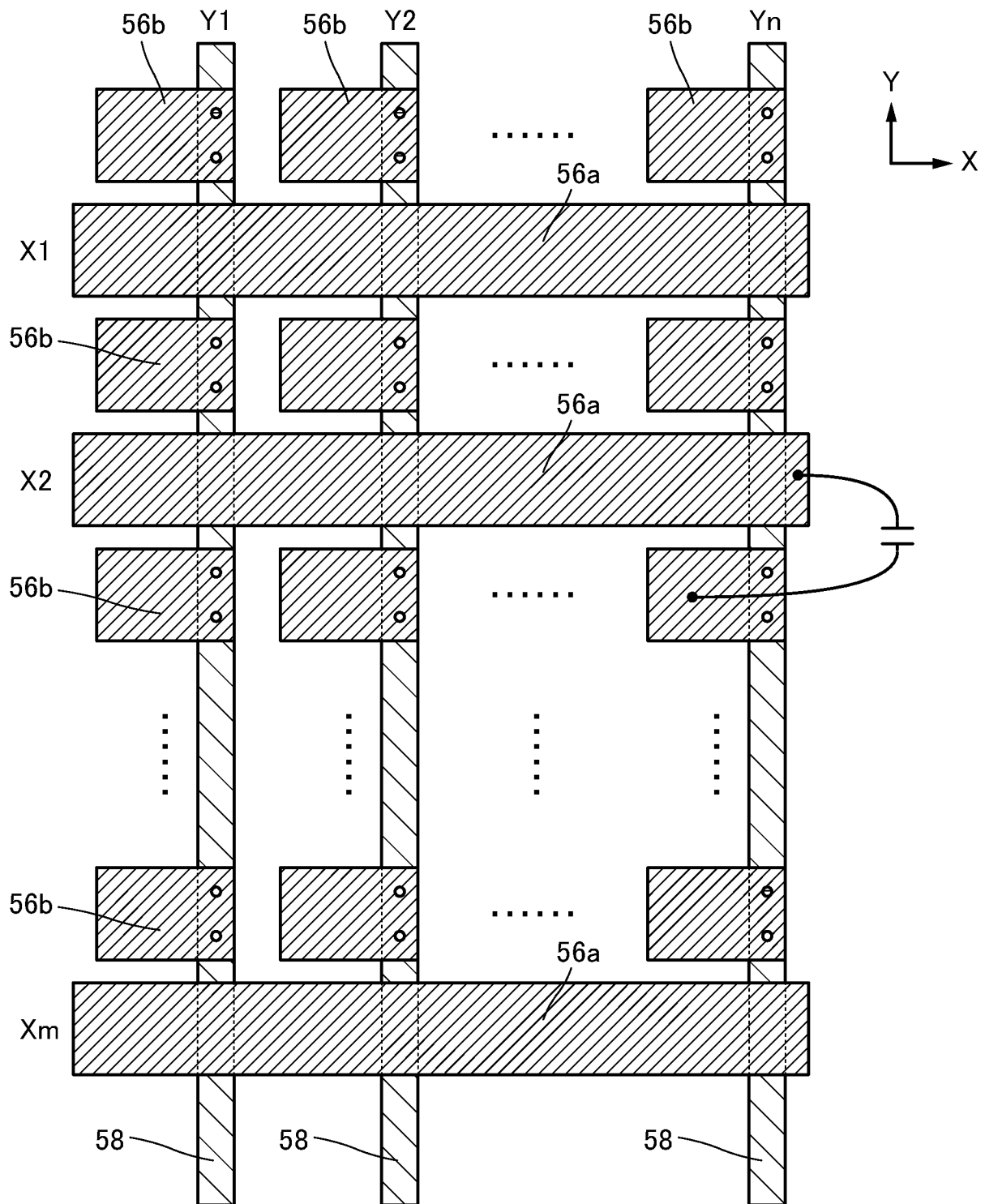


FIG. 9A

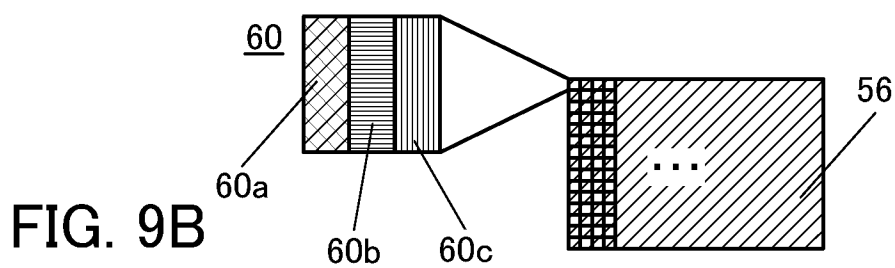


FIG. 9B

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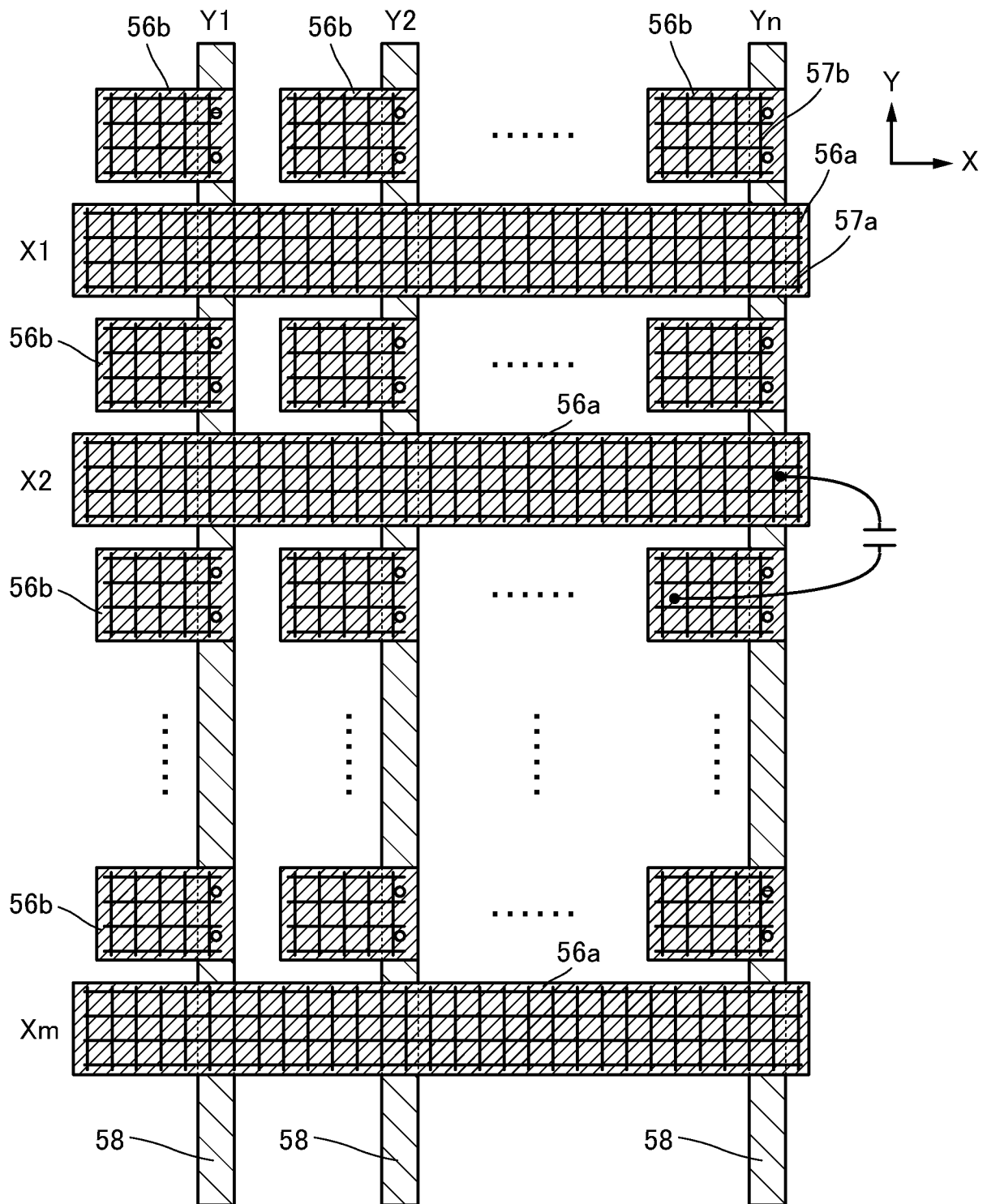


FIG. 10

FIG. 11A

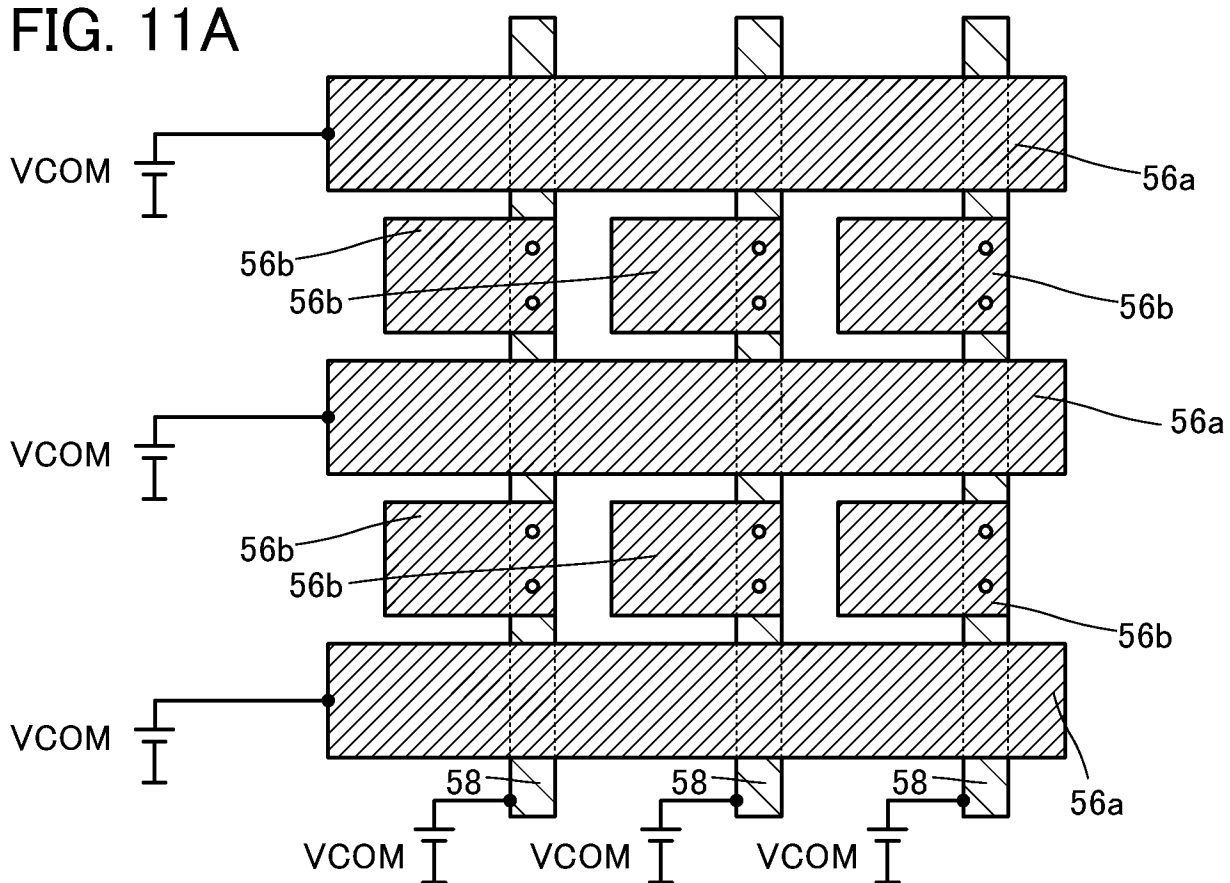
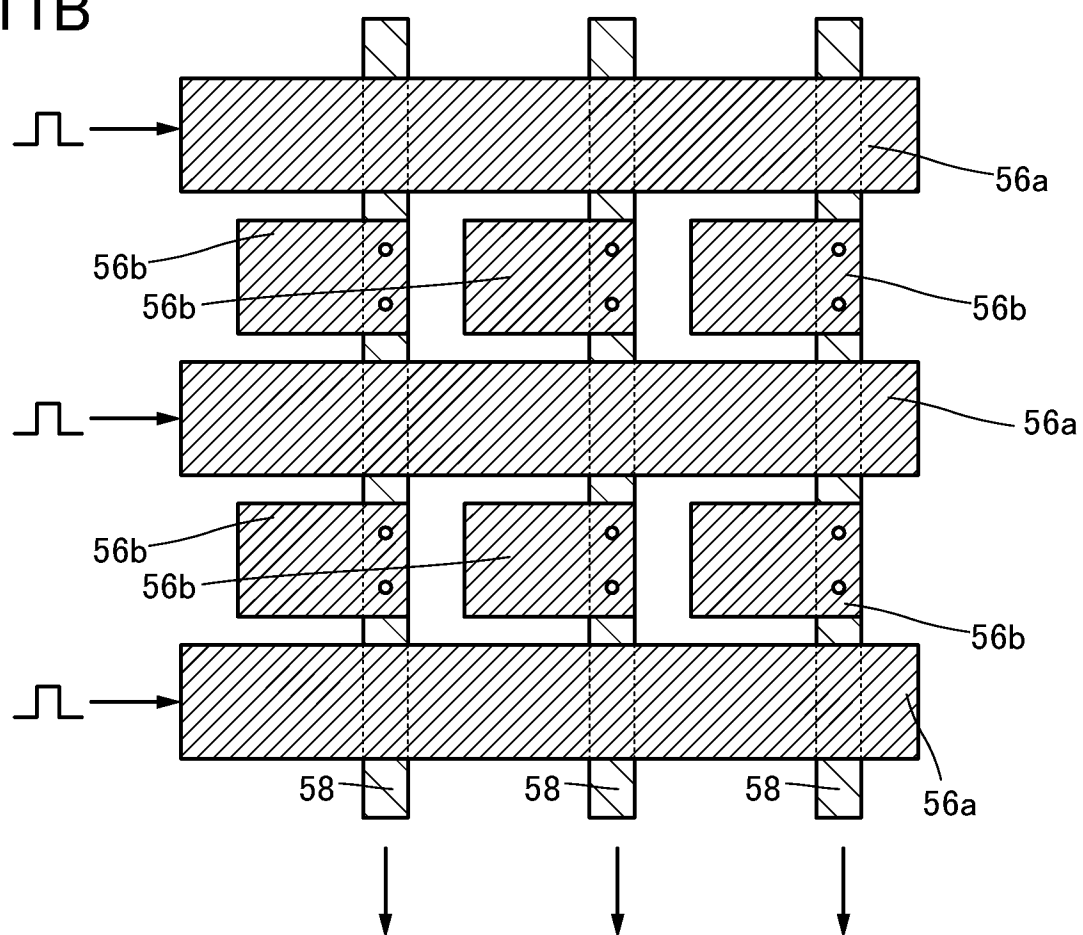
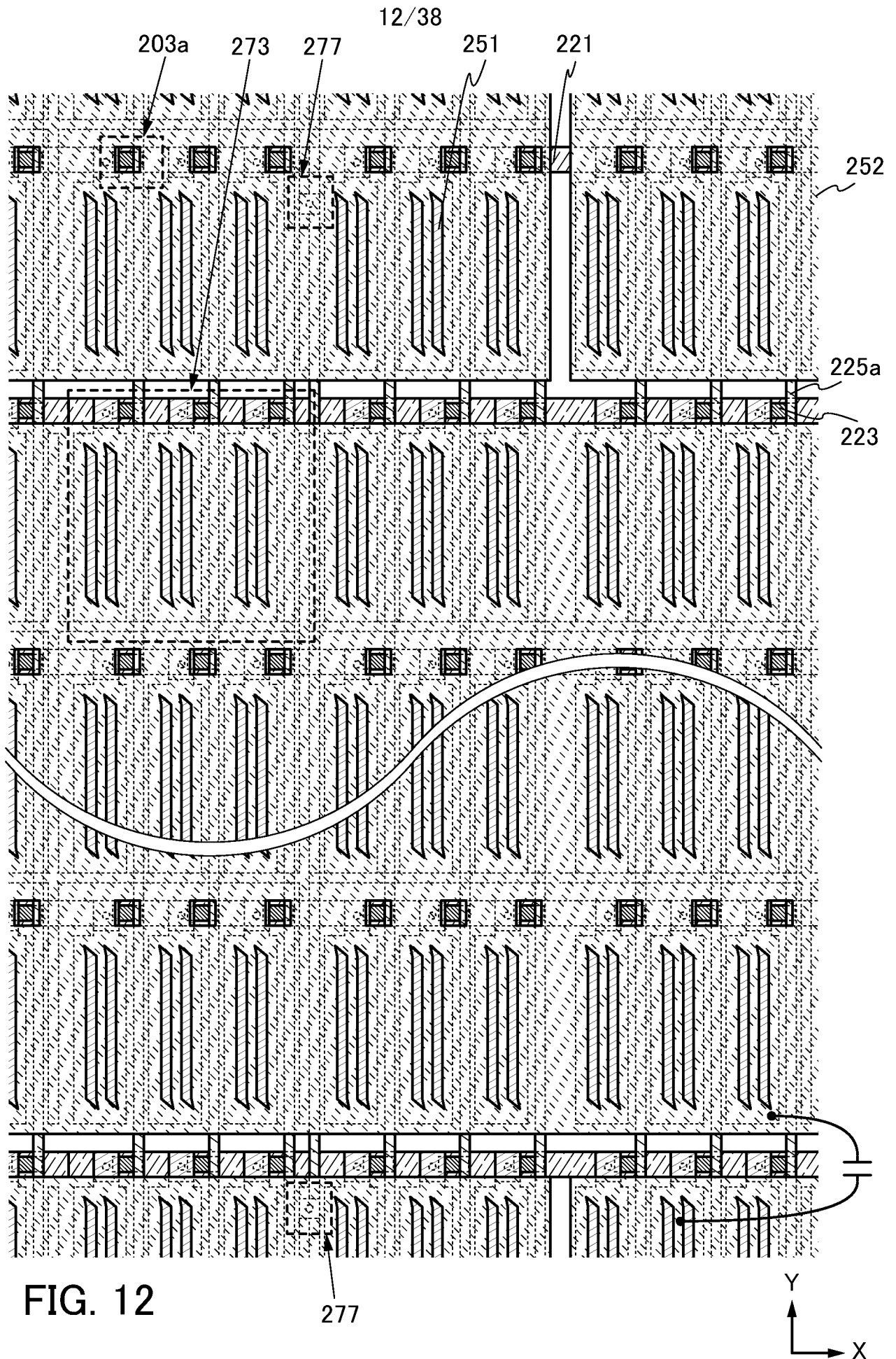


FIG. 11B





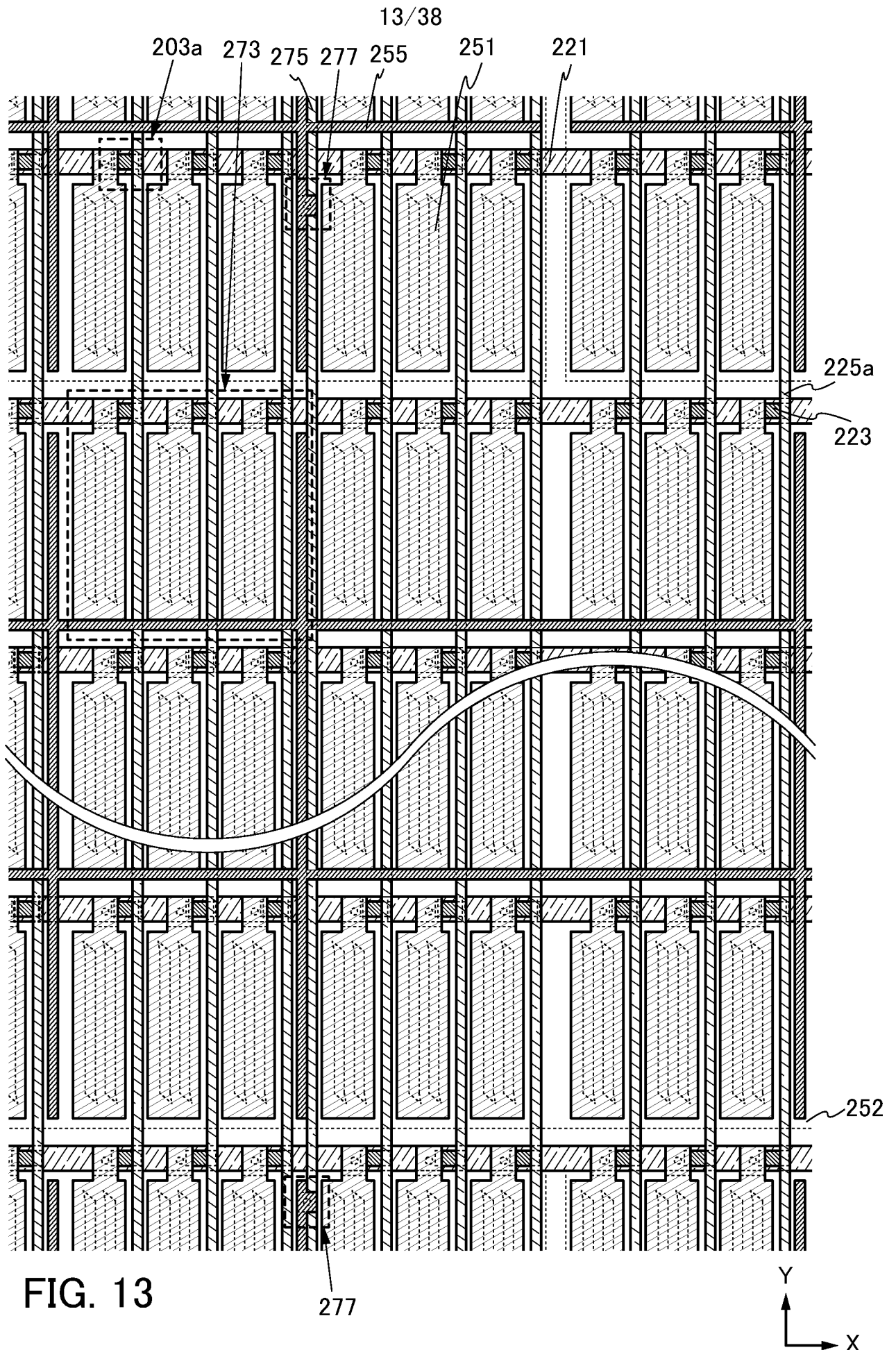


FIG. 14A

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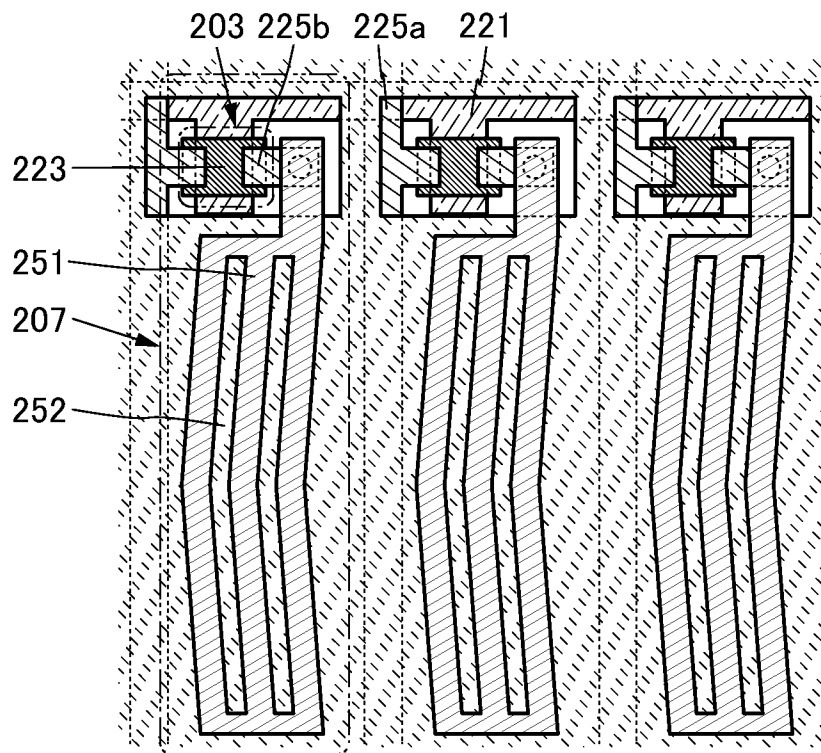


FIG. 14B

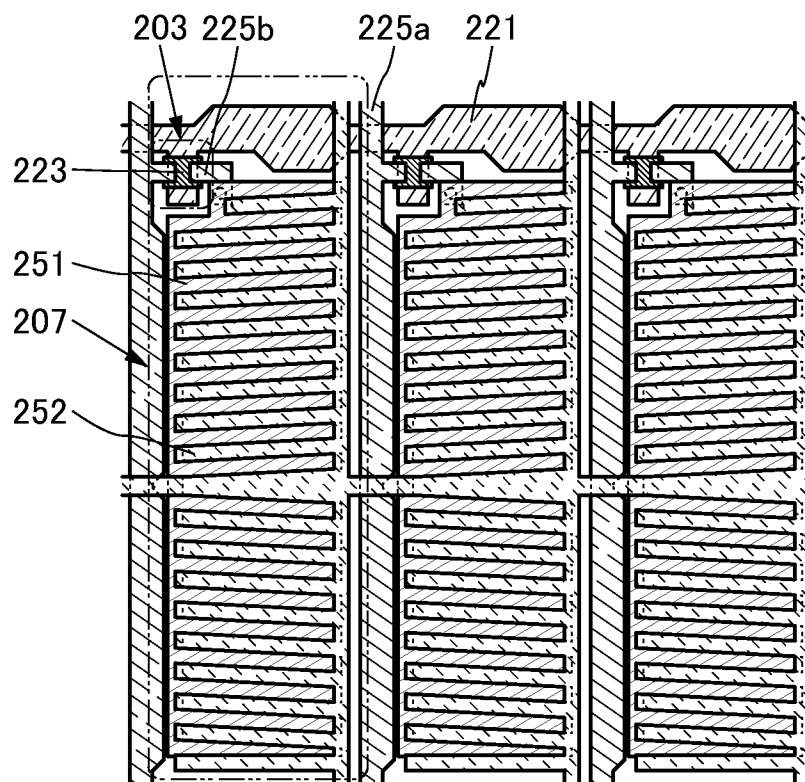
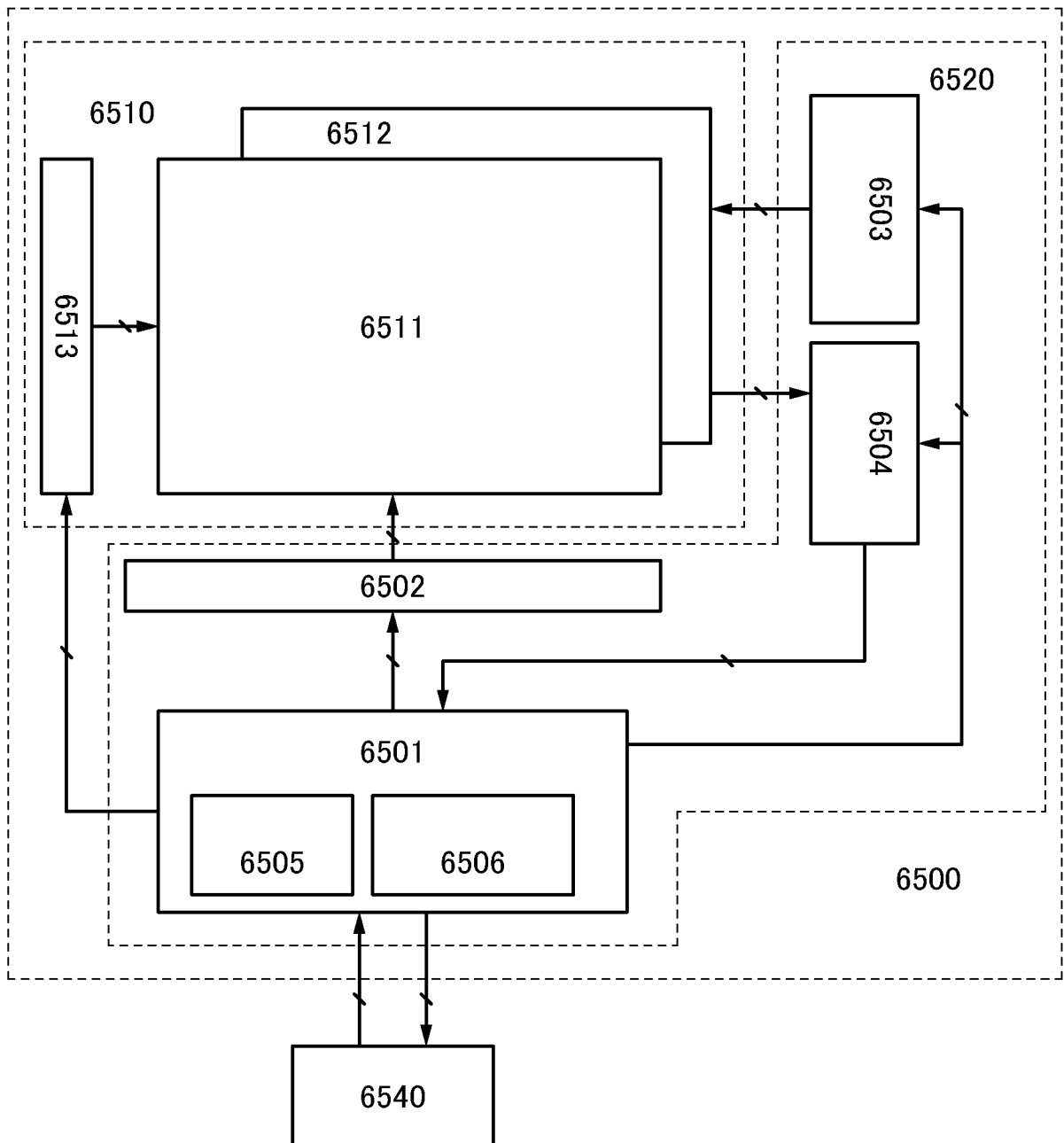


FIG. 15



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FIG. 16A

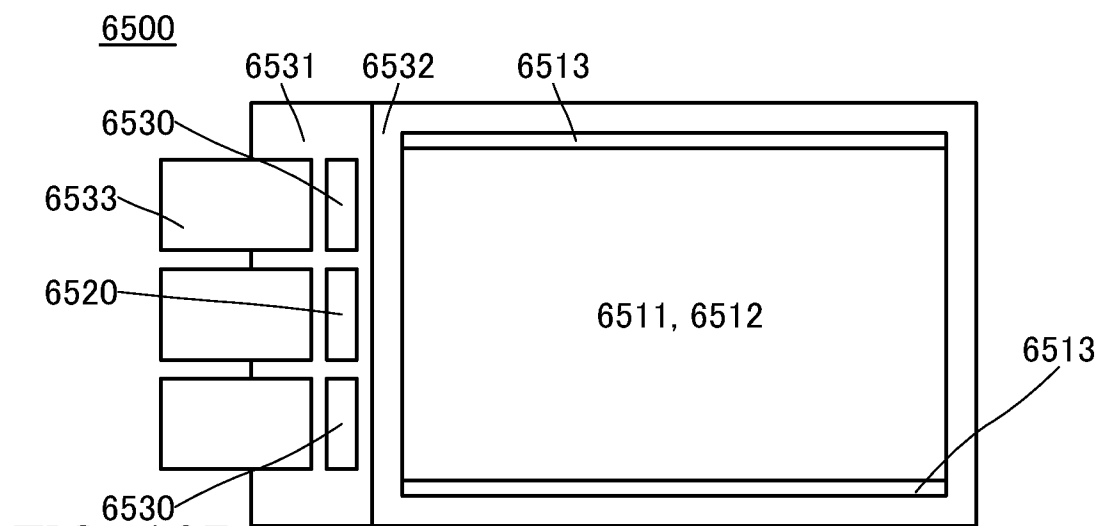


FIG. 16B

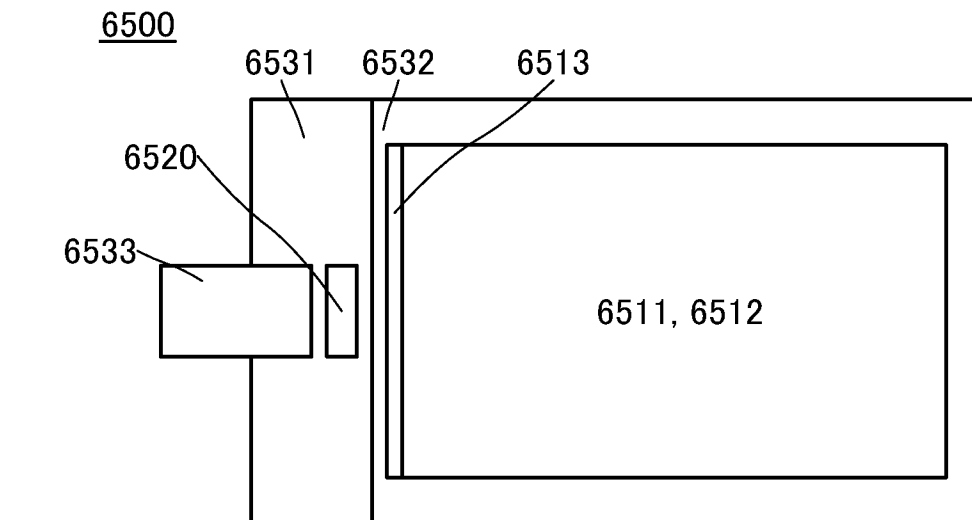
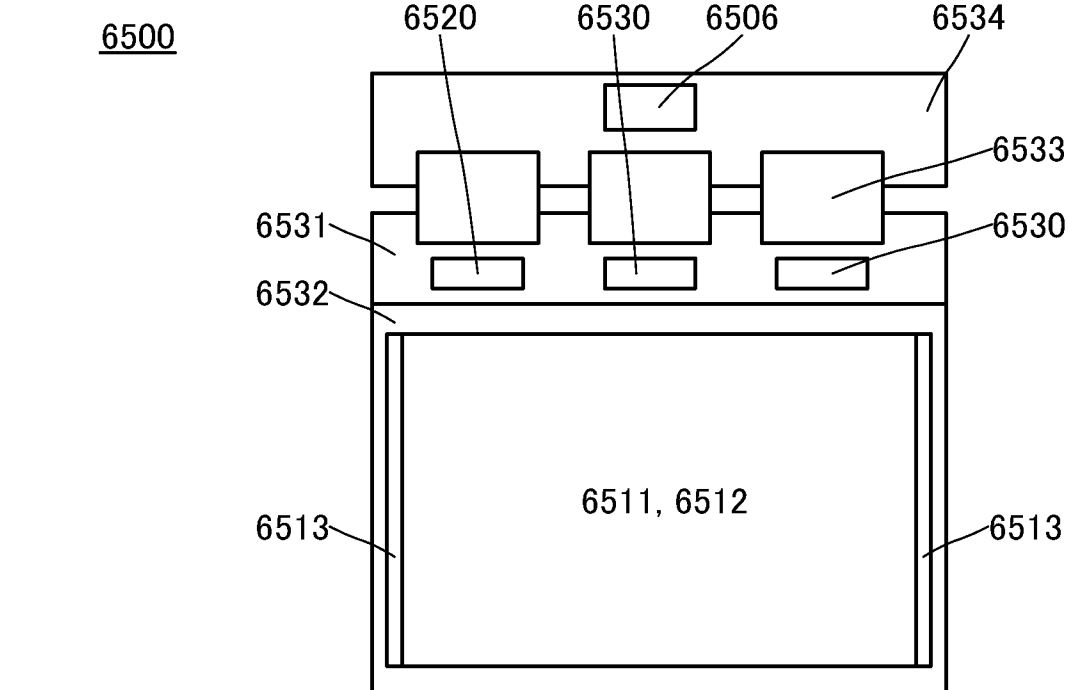


FIG. 16C



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FIG. 17A

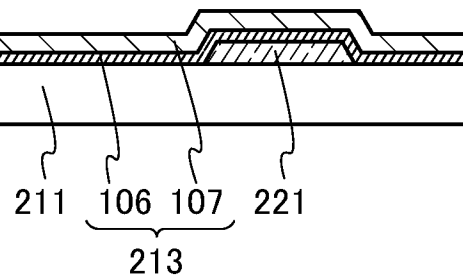


FIG. 17B

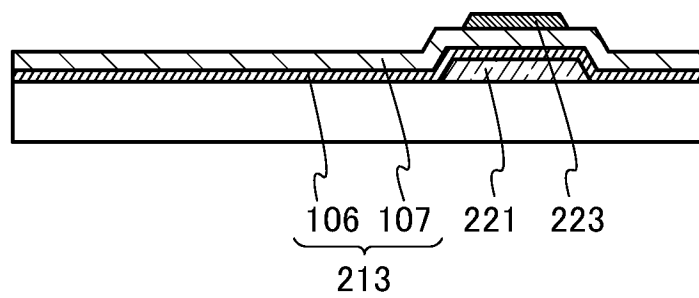


FIG. 17C

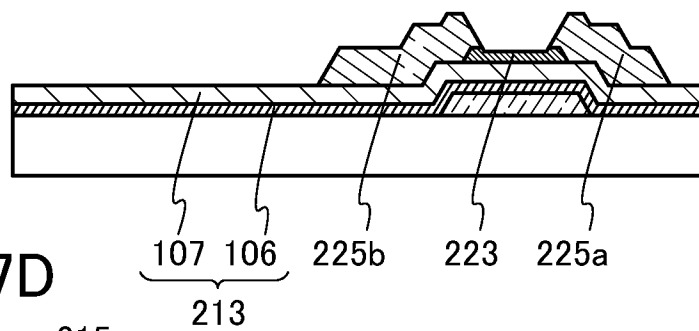
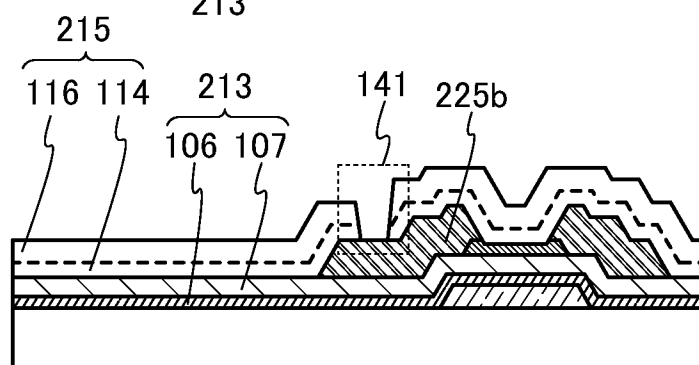


FIG. 17D



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FIG. 18A

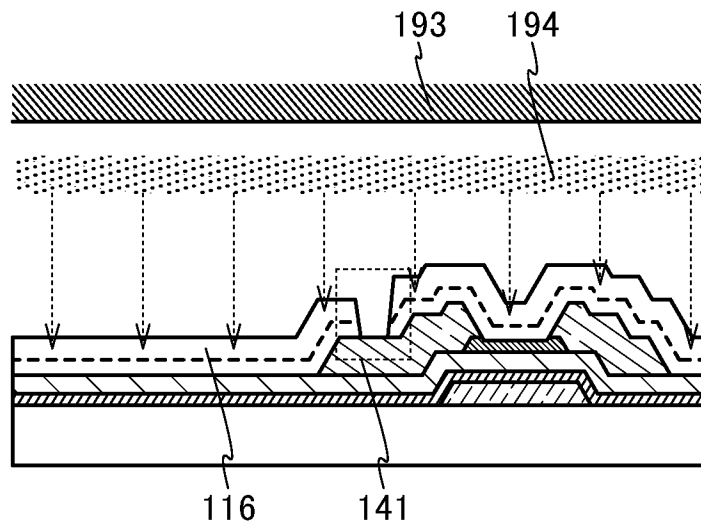


FIG. 18B

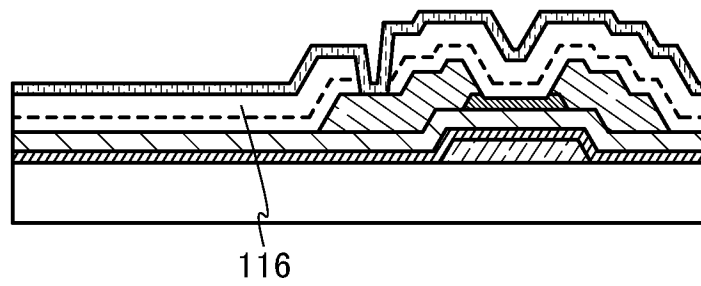


FIG. 18C

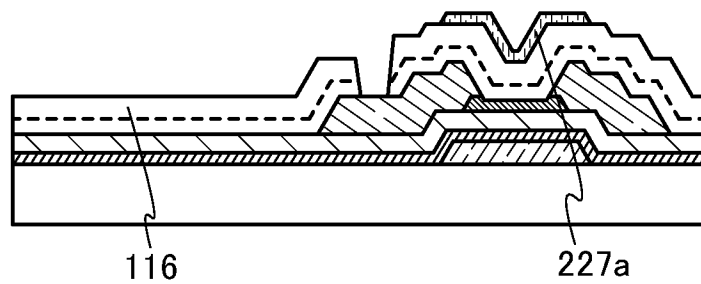


FIG. 19A

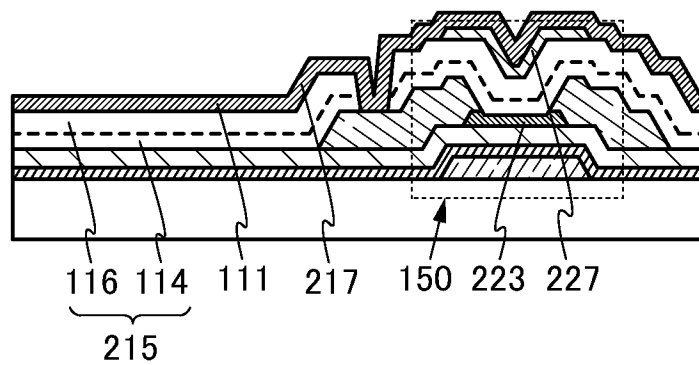


FIG. 19B

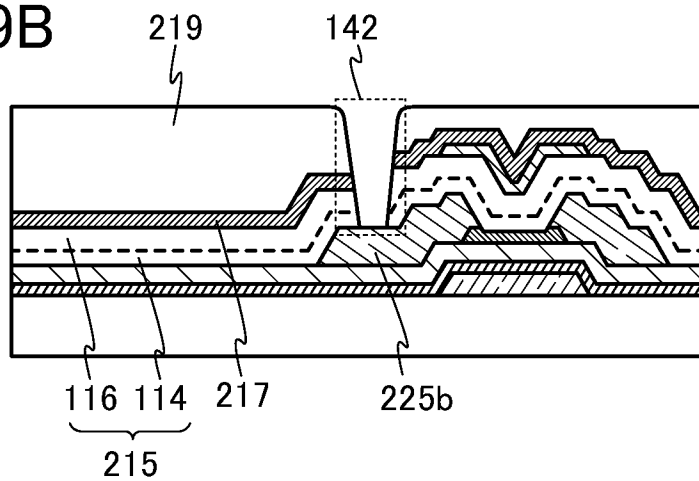
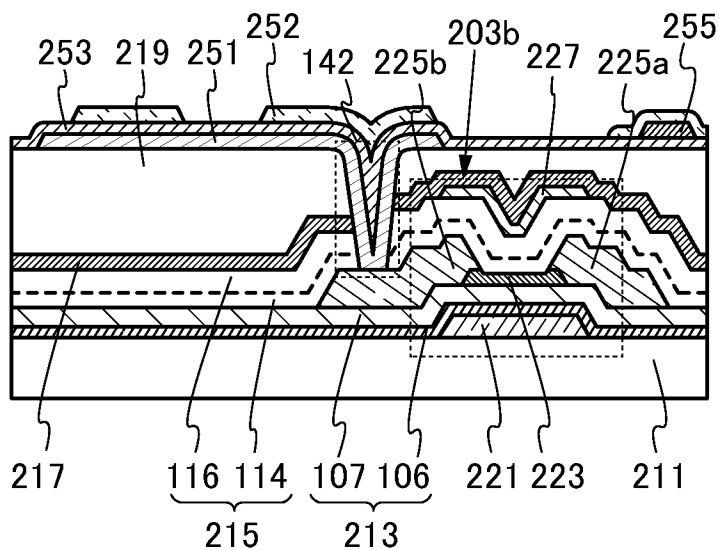


FIG. 19C



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FIG. 20

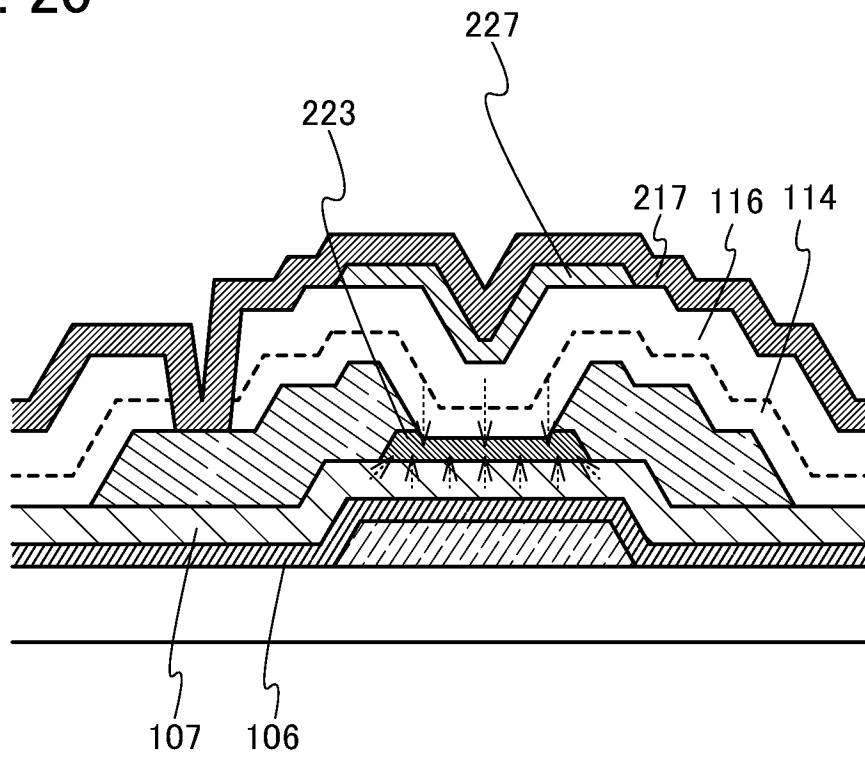


FIG. 21

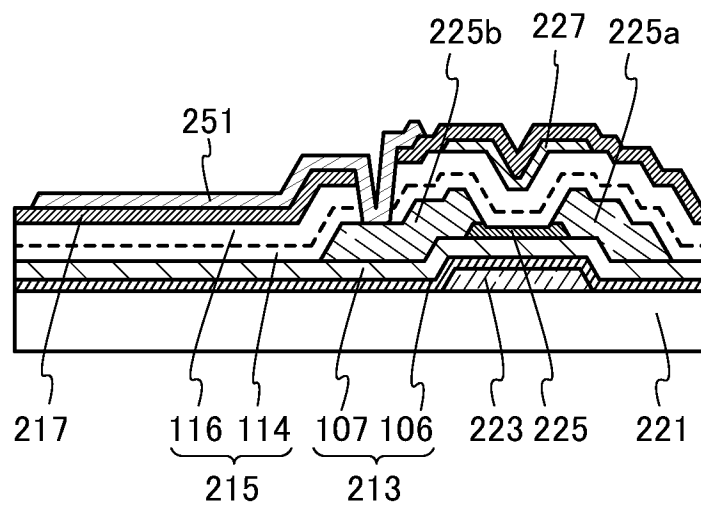


FIG. 22A

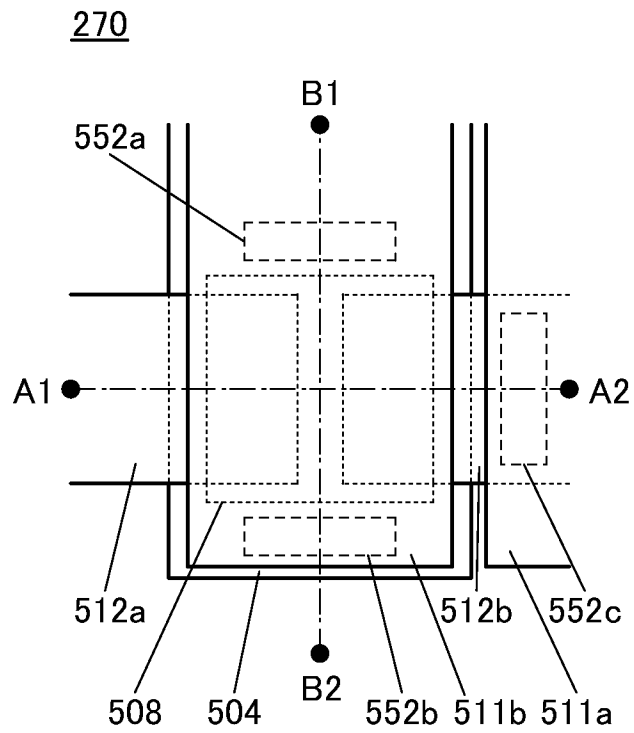


FIG. 22B

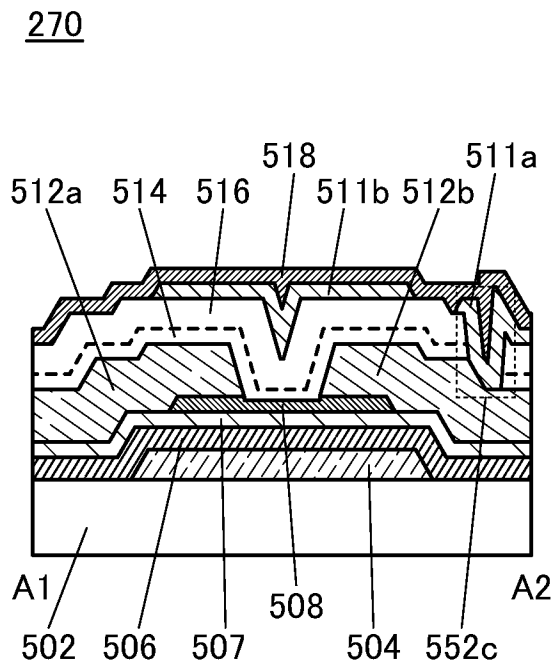


FIG. 22C

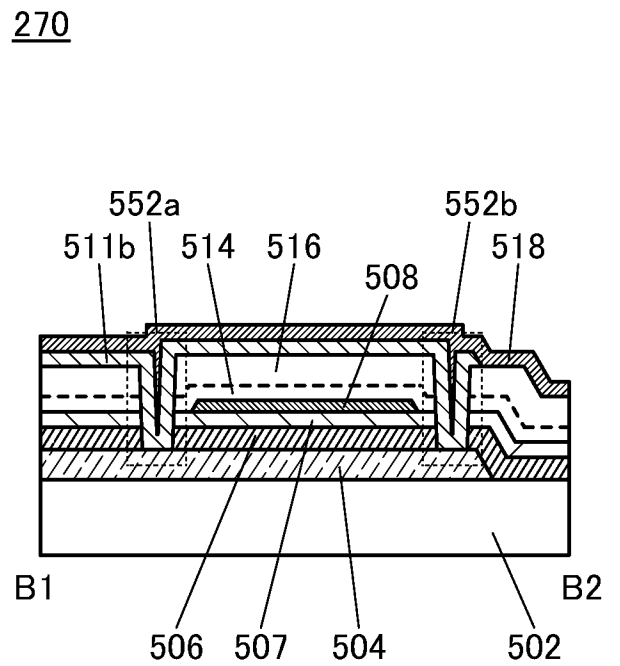


FIG. 23A

270A

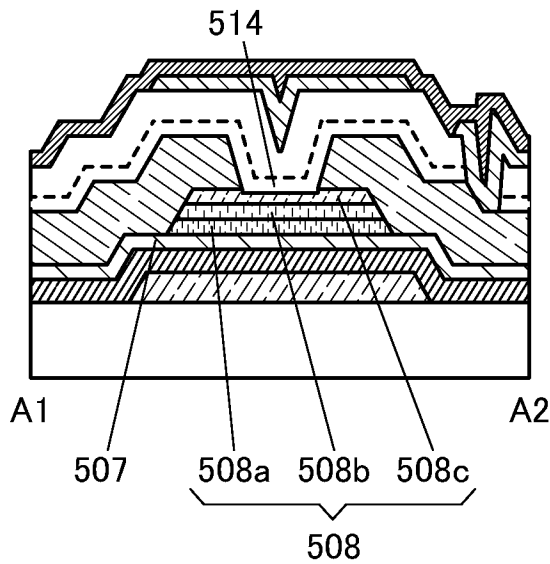


FIG. 23B

270A

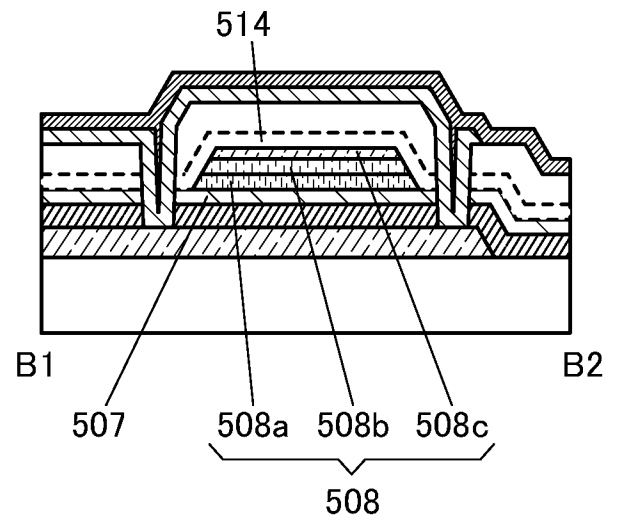


FIG. 23C

270B

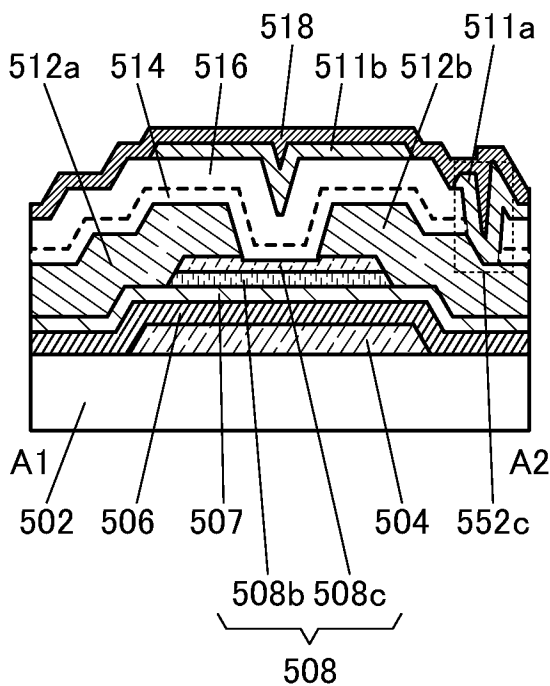


FIG. 23D

270B

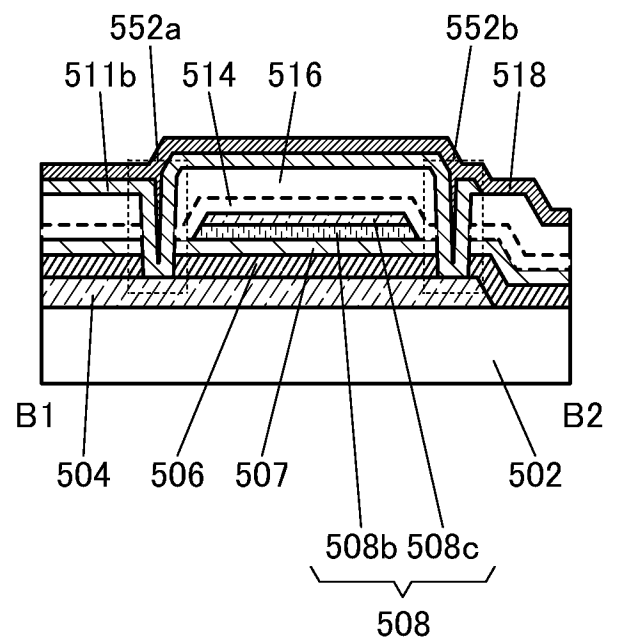


FIG. 24A

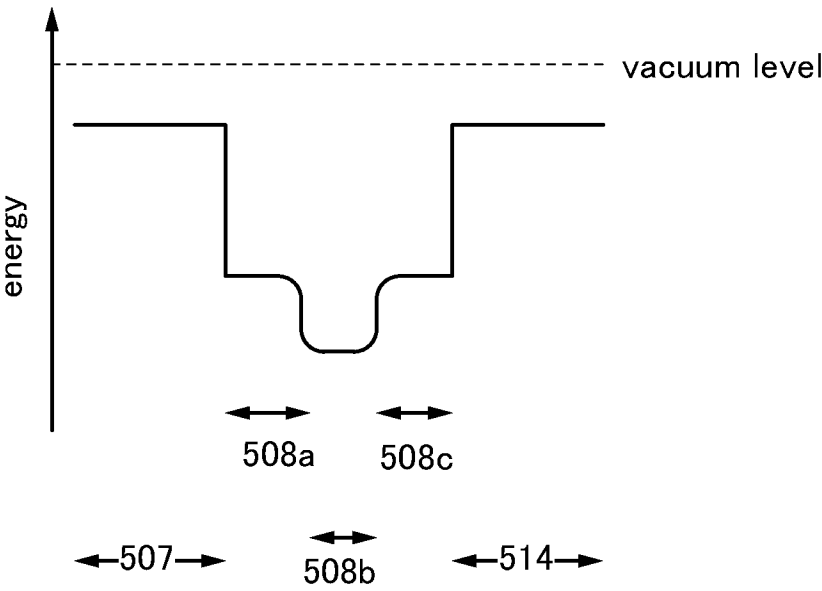


FIG. 24B

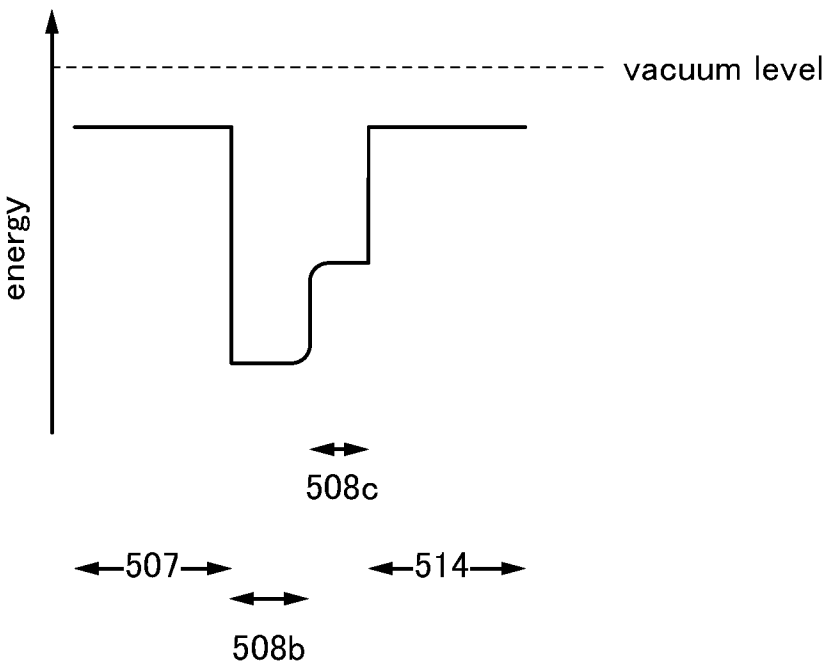


FIG. 25A

FIG. 25B

270B

270B

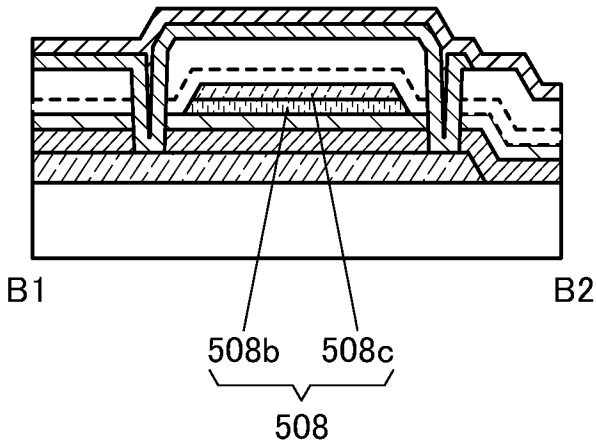
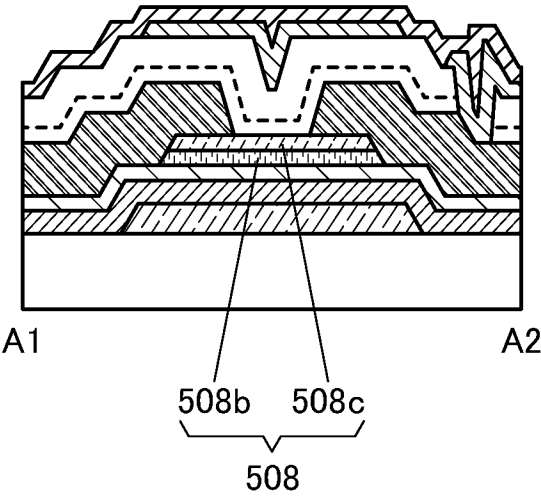
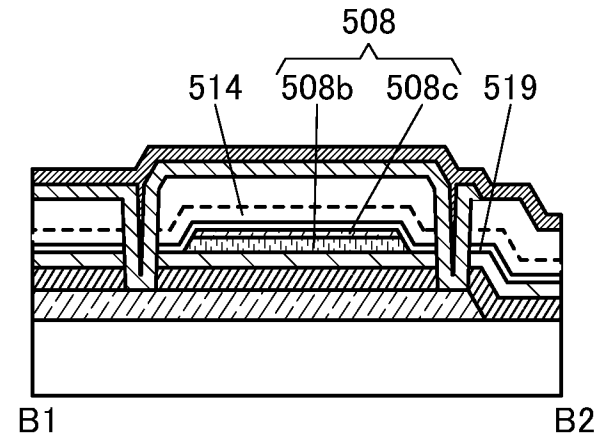
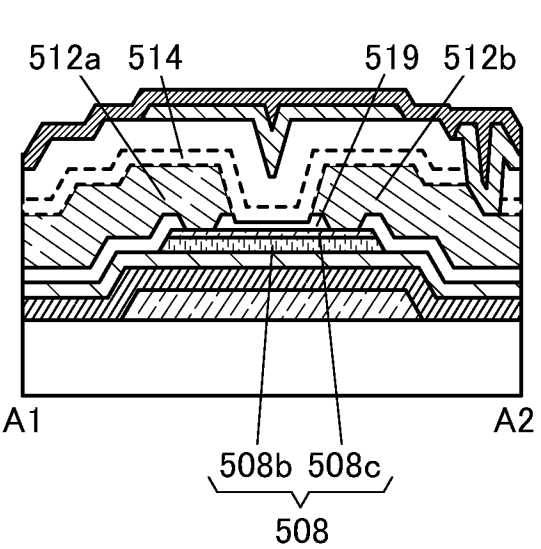


FIG. 25C

FIG. 25D



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FIG. 26A

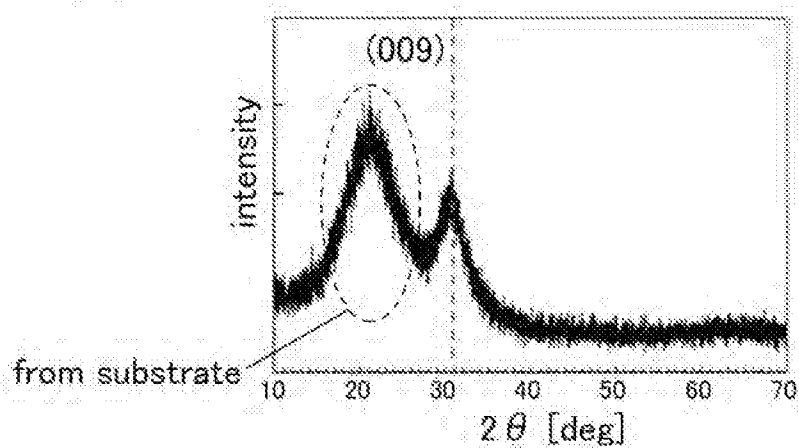


FIG. 26B

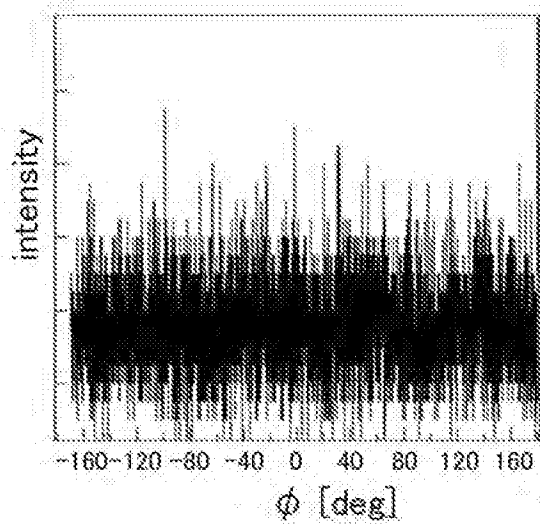


FIG. 26C

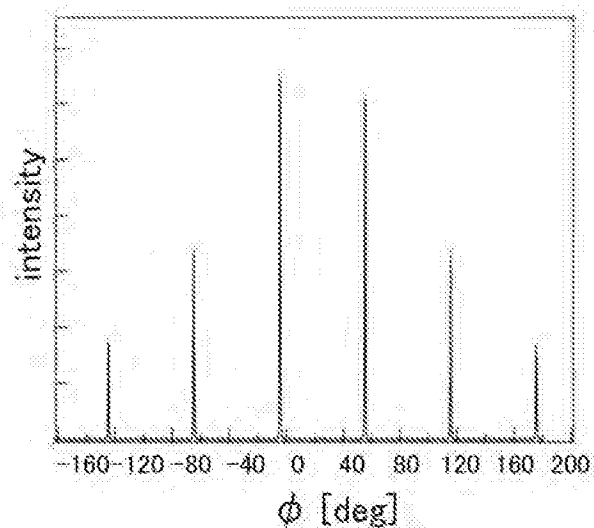


FIG. 26D

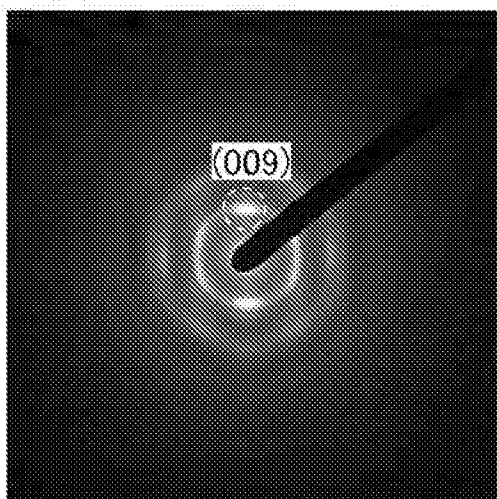
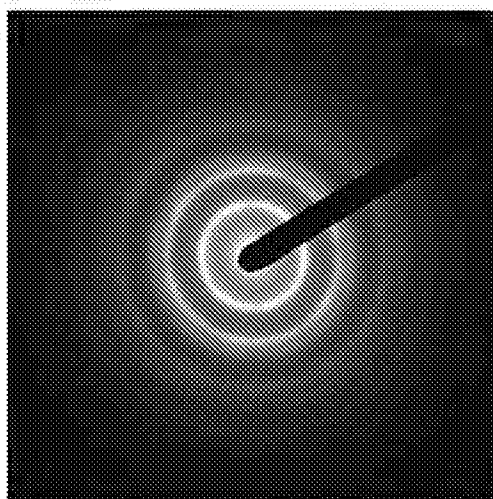


FIG. 26E



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FIG. 27A

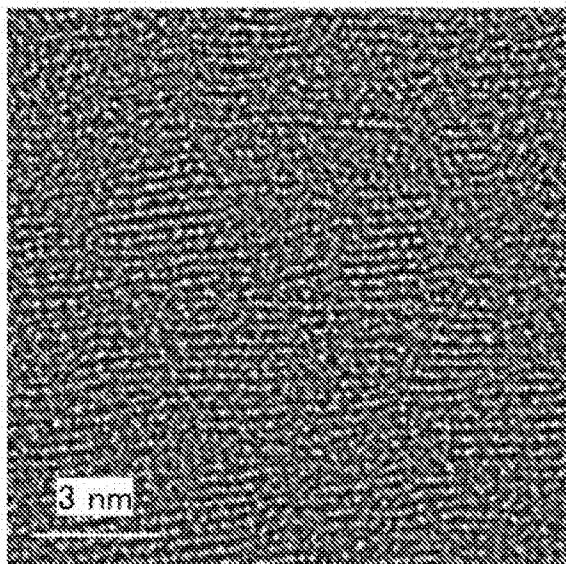


FIG. 27B

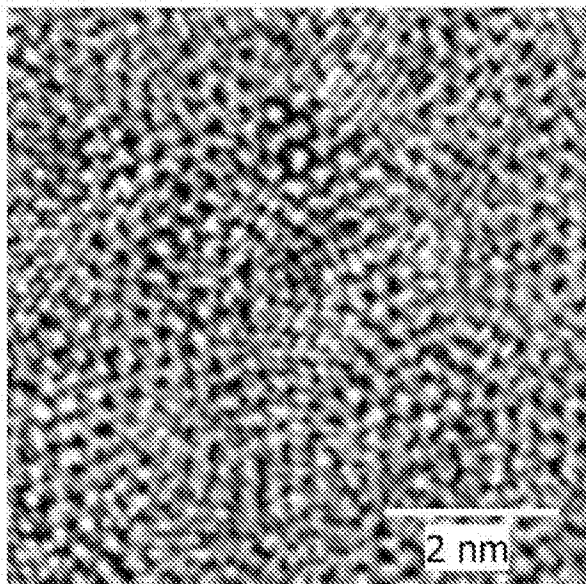


FIG. 27C

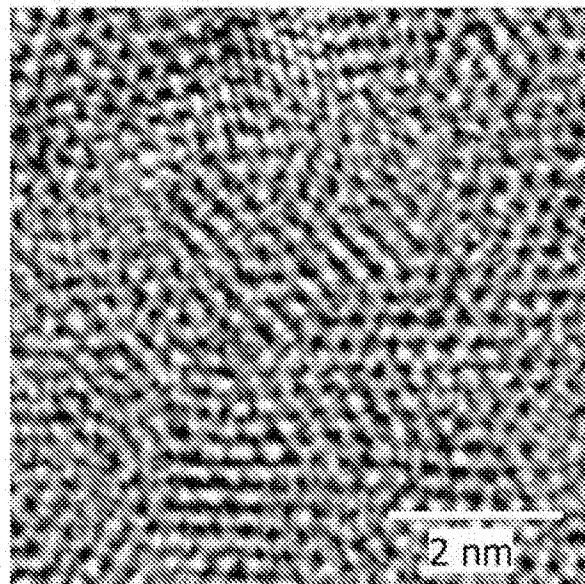


FIG. 27D

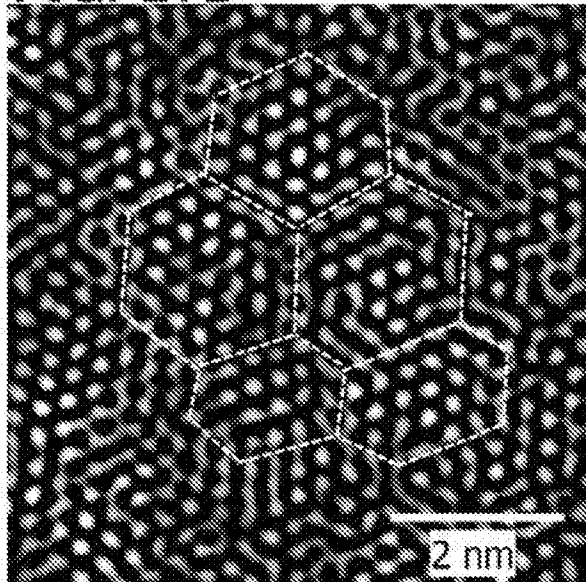
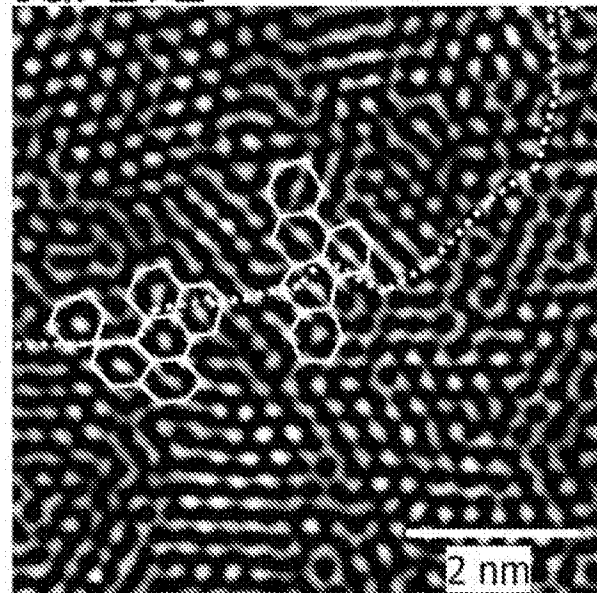


FIG. 27E



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FIG. 28A

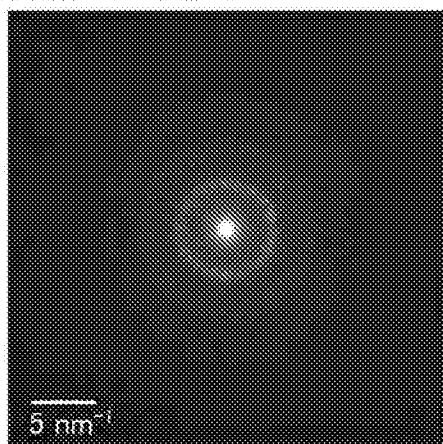


FIG. 28B

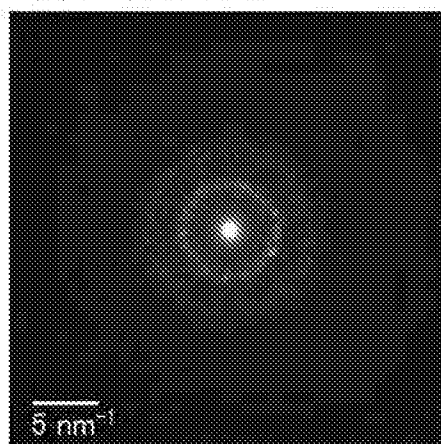


FIG. 28C

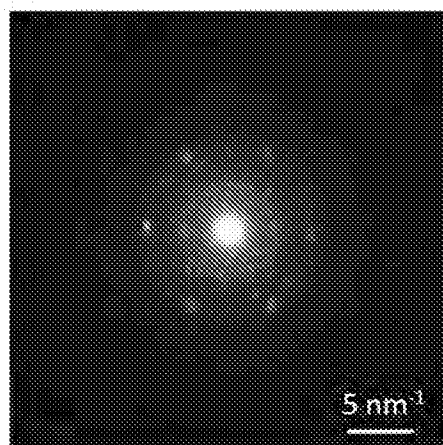


FIG. 28D

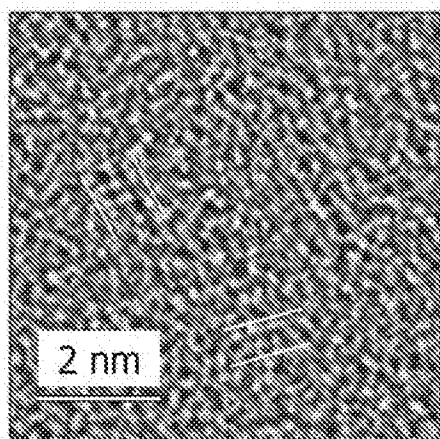
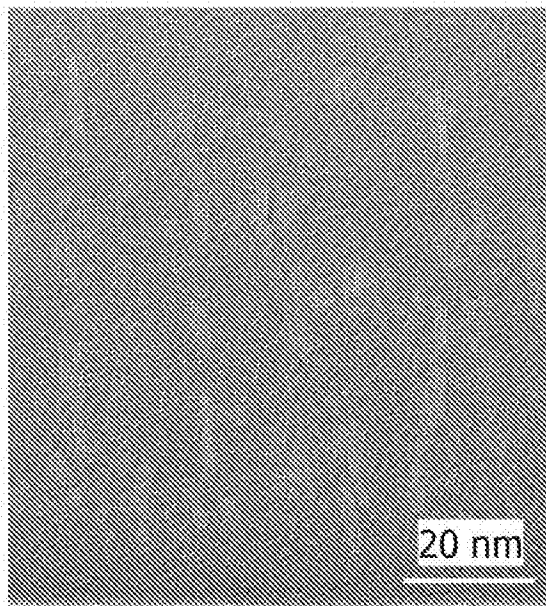
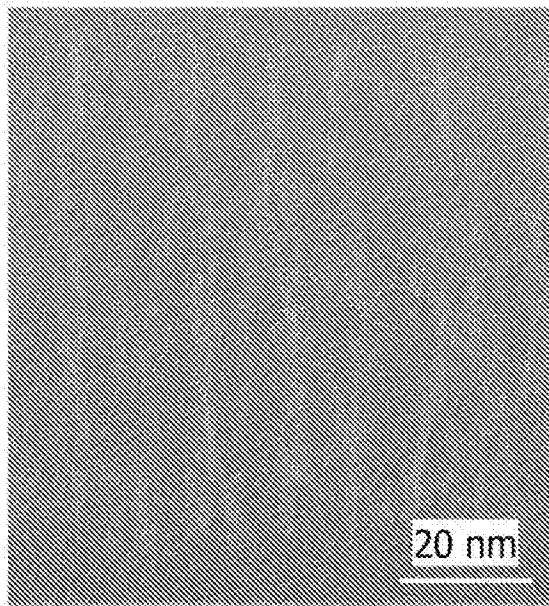


FIG. 29A

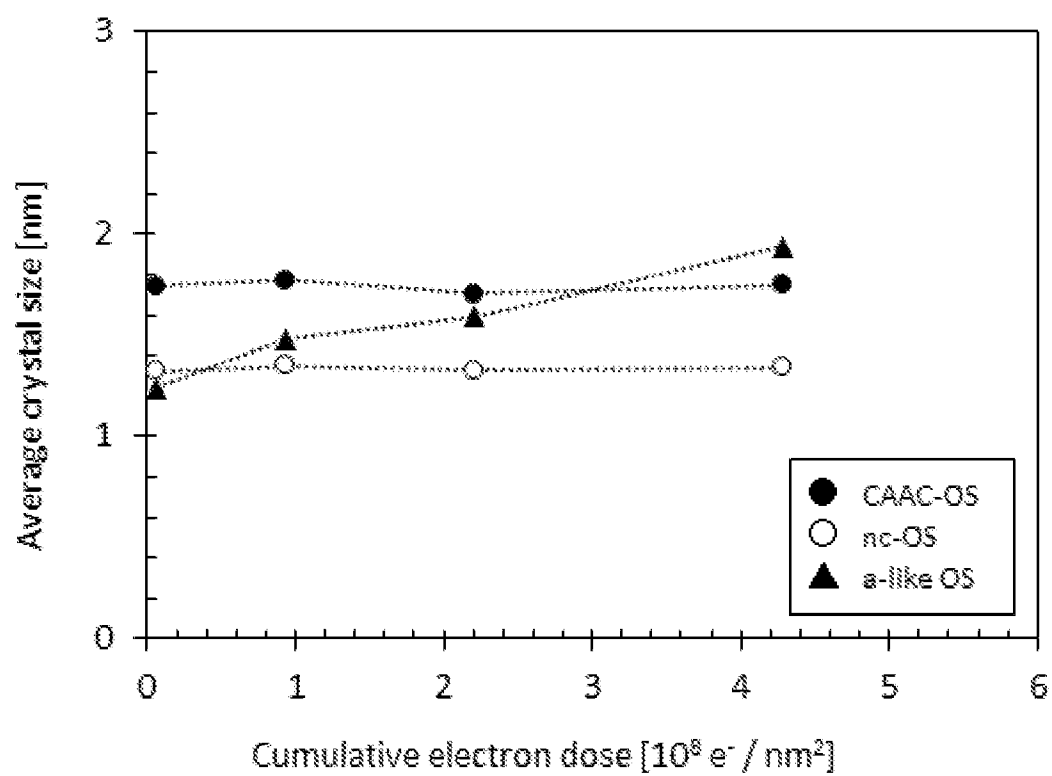
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FIG. 29B



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FIG. 30



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FIG. 31

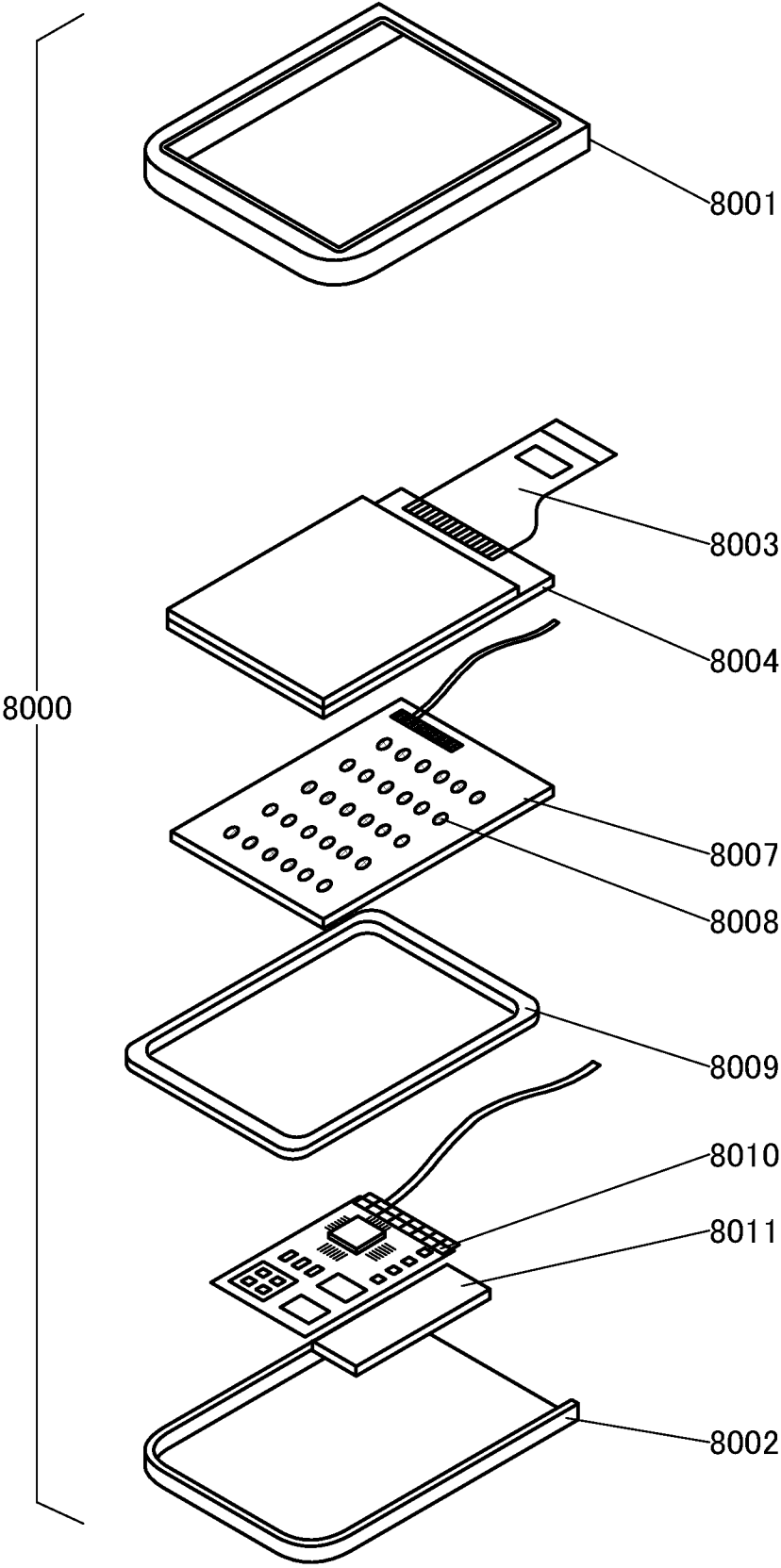


FIG. 32A

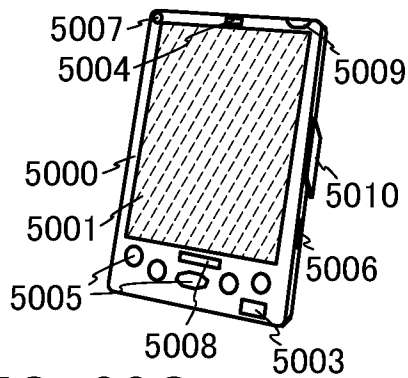


FIG. 32B

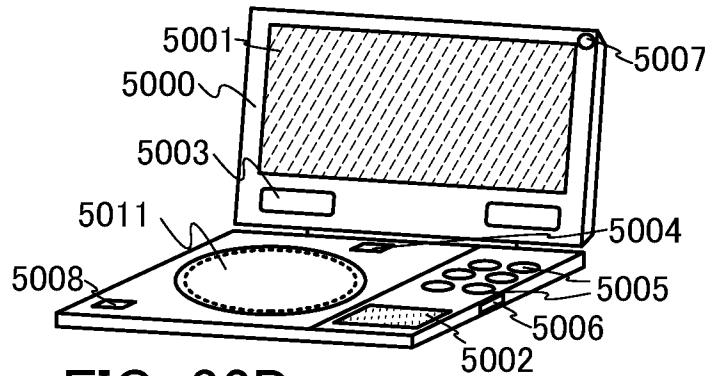


FIG. 32C

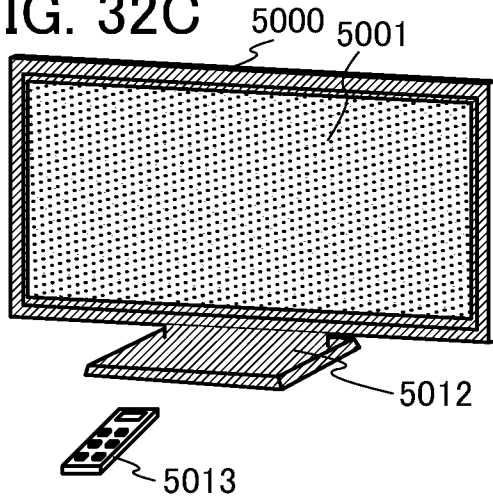


FIG. 32D

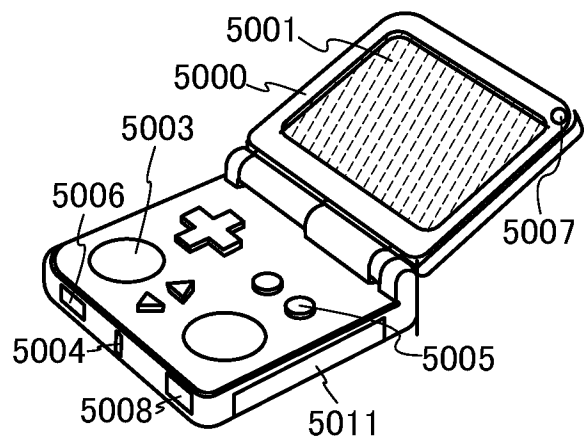


FIG. 32E

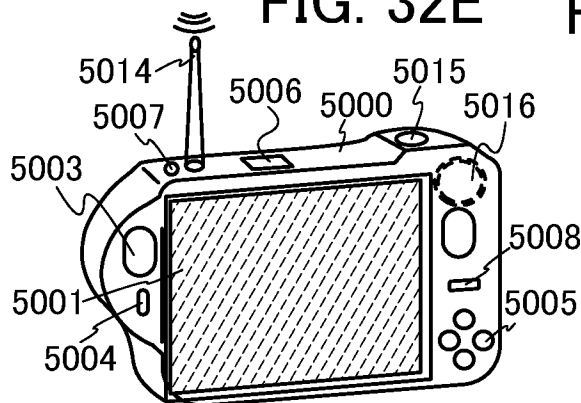


FIG. 32F

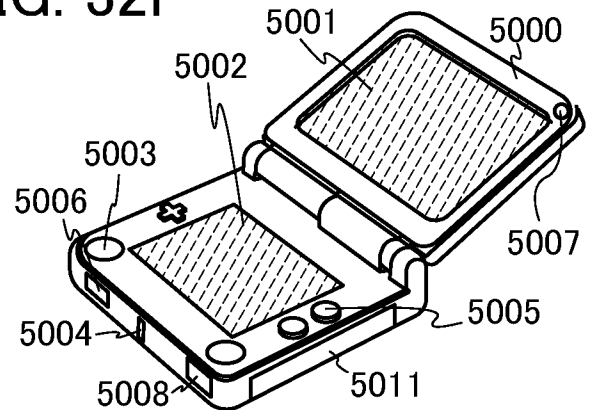


FIG. 32G

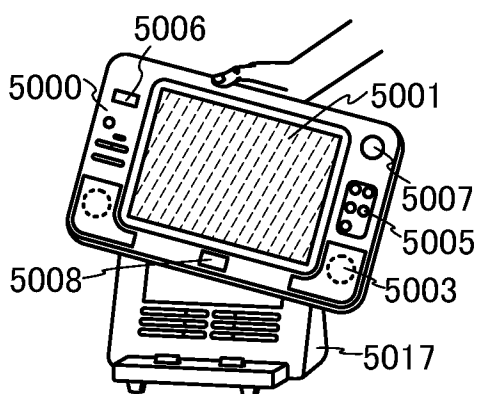


FIG. 32H

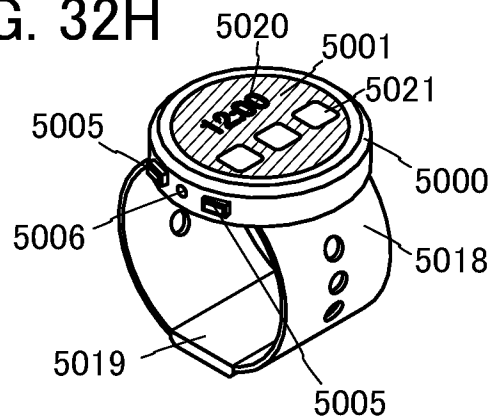


FIG. 33A

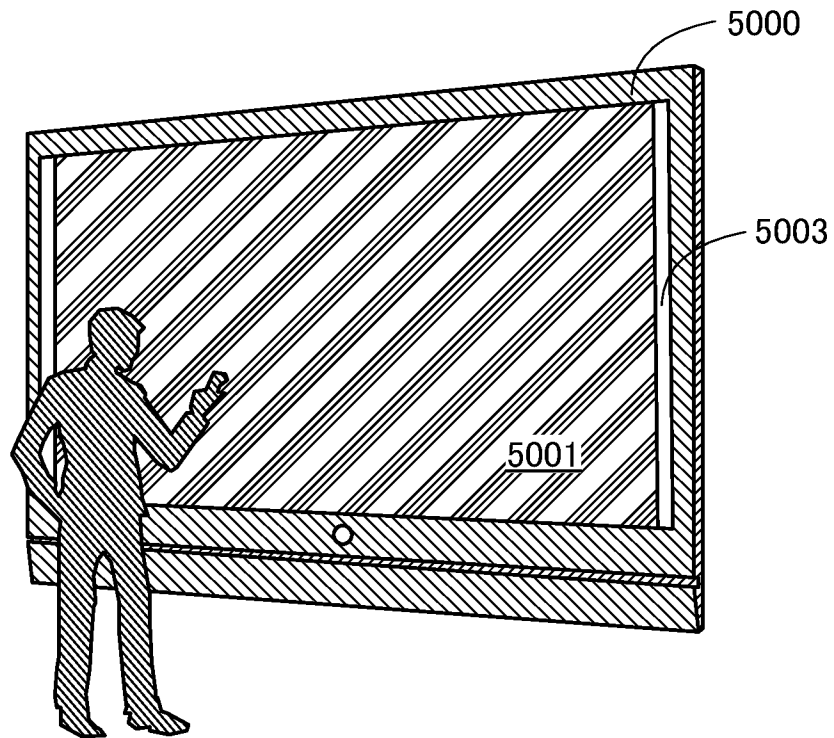


FIG. 33B

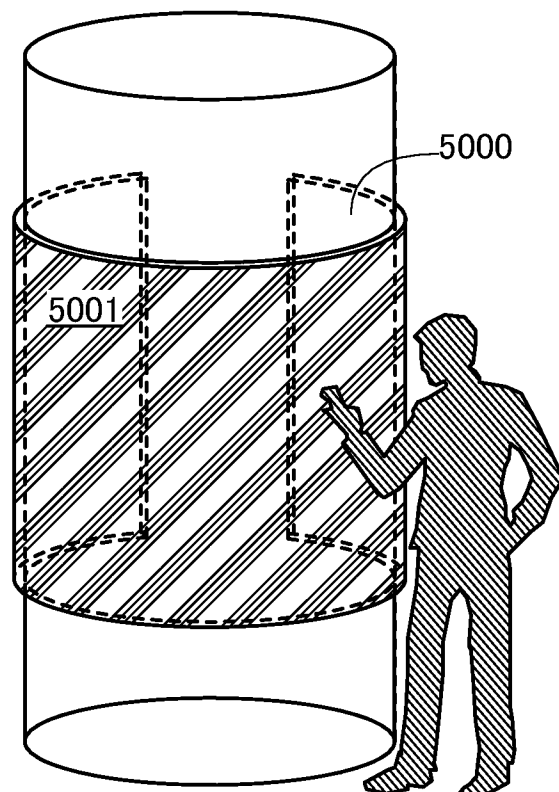


FIG. 34

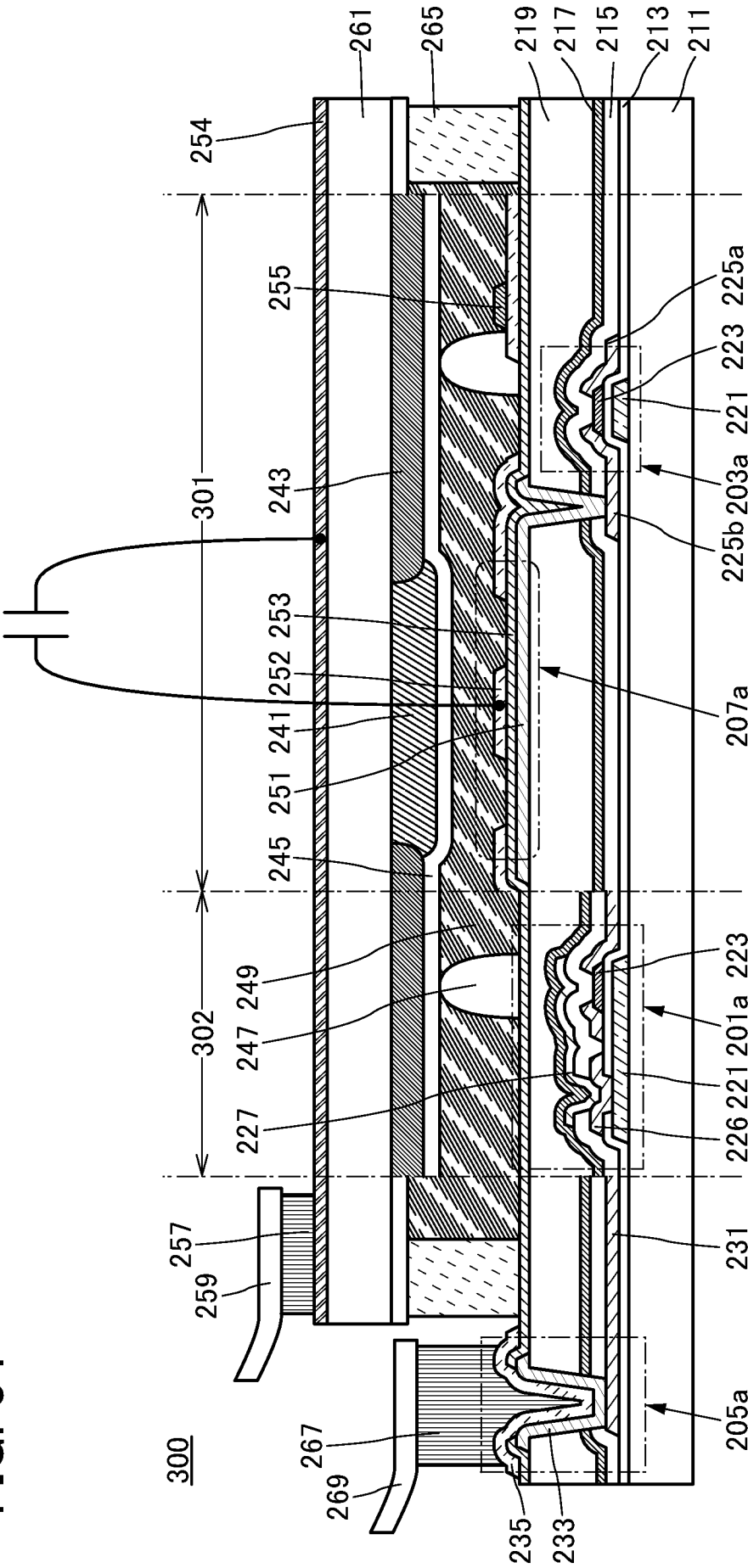


FIG. 35

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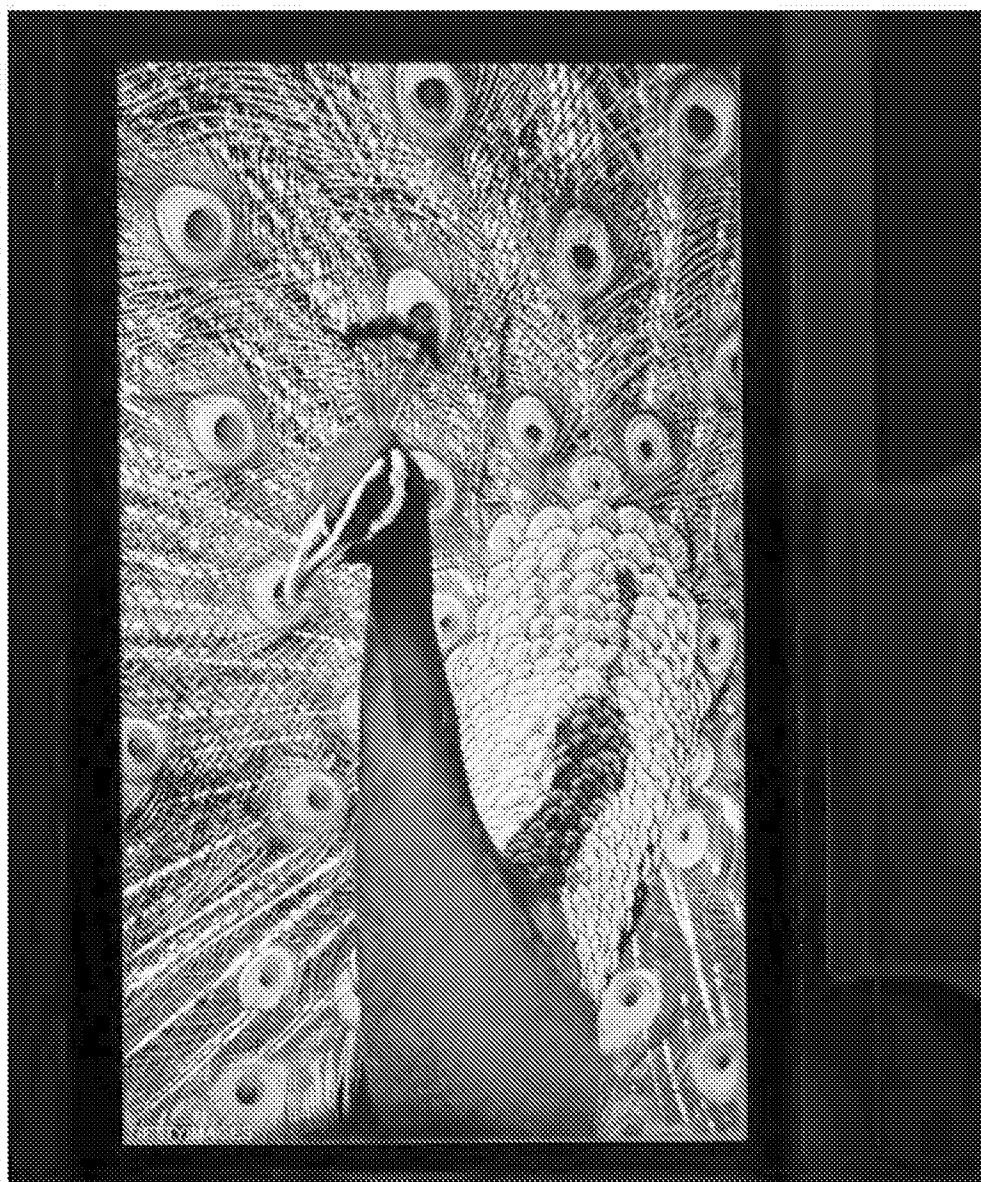


FIG. 36

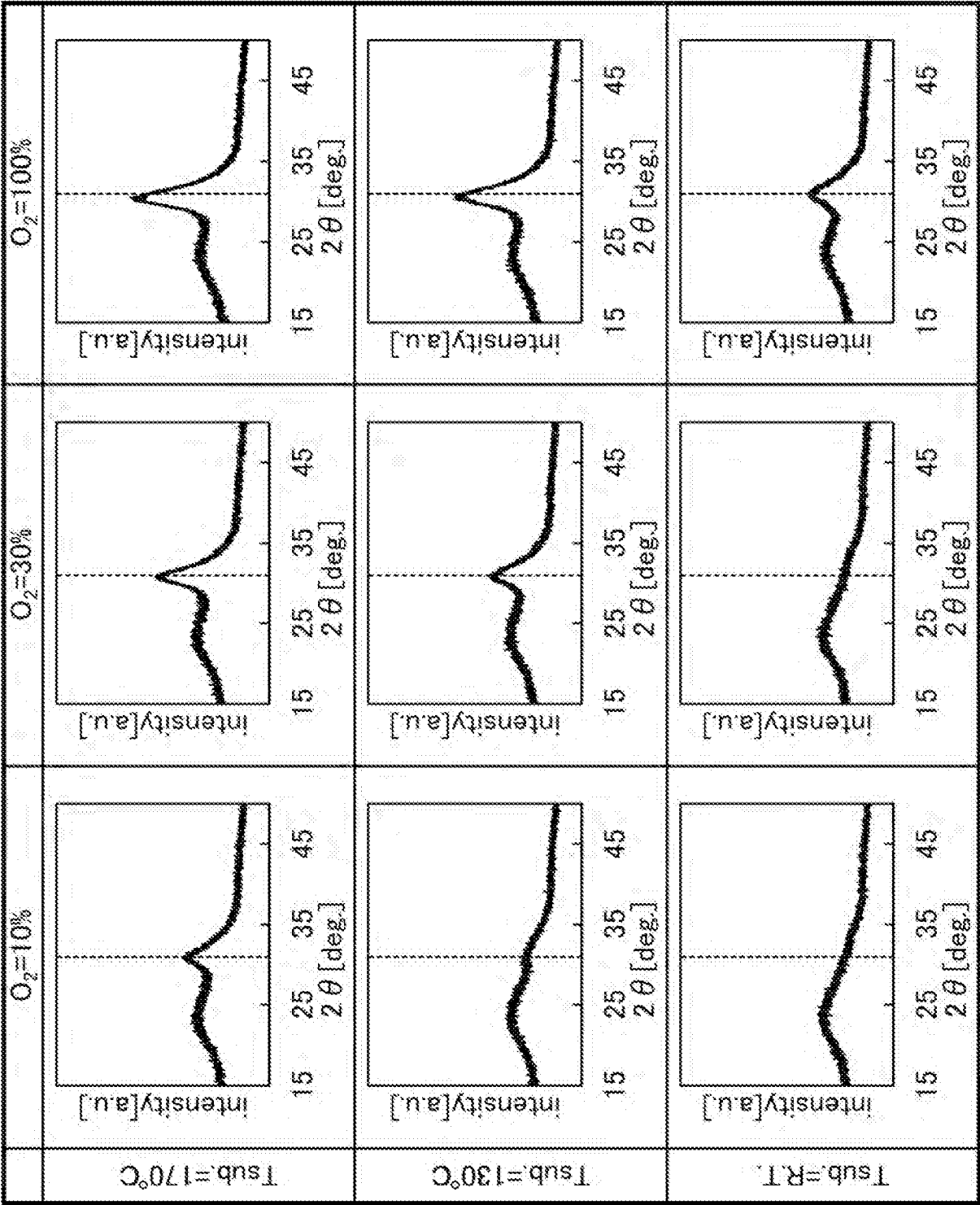


FIG. 37A

plan-view TEM image

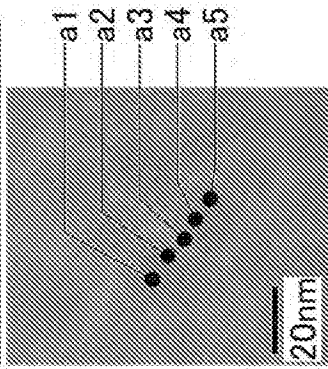


FIG. 37B

cross-sectional TEM image

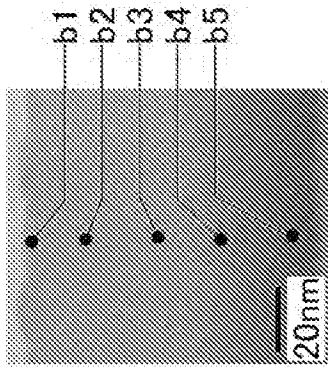


FIG. 37C

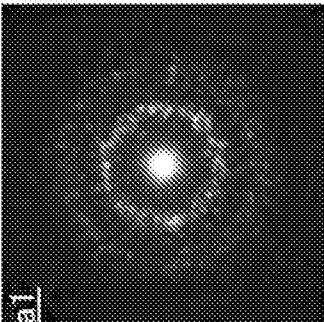


FIG. 37D

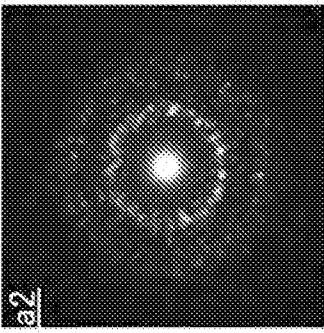


FIG. 37E

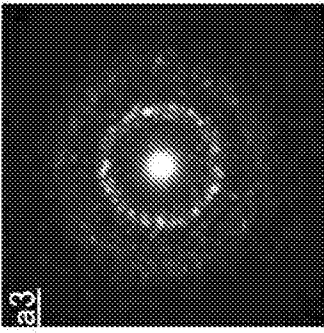


FIG. 37F

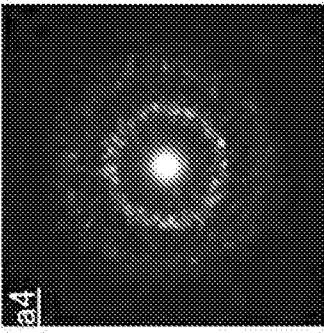


FIG. 37G

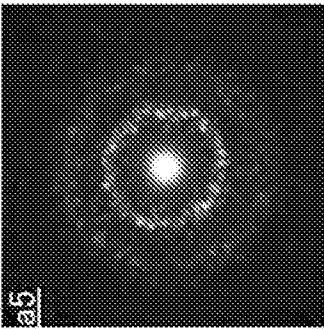


FIG. 37H

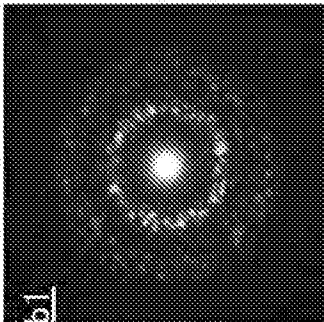


FIG. 37I

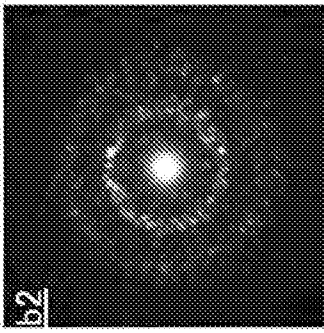


FIG. 37J

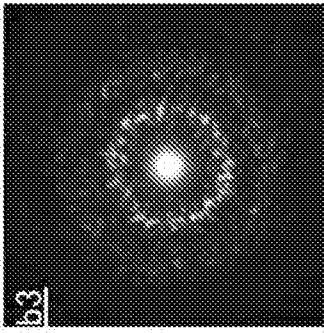


FIG. 37K

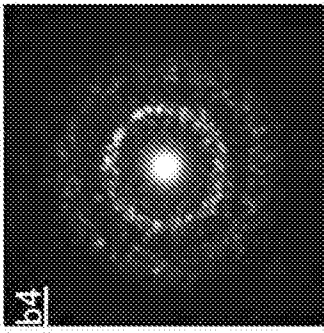


FIG. 37L

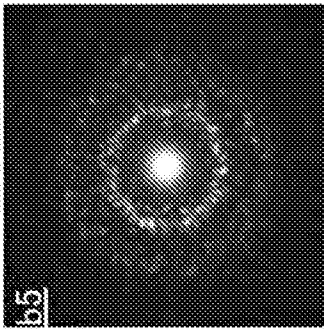


FIG. 38A

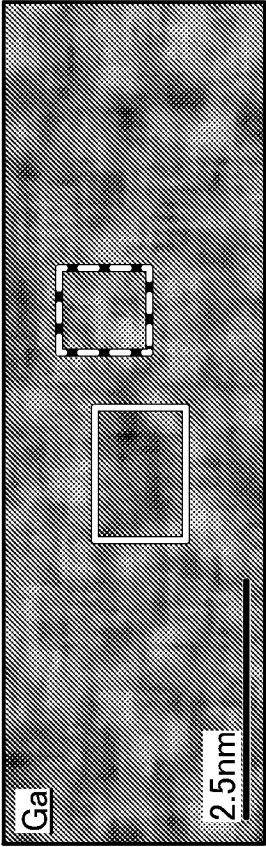


FIG. 38B

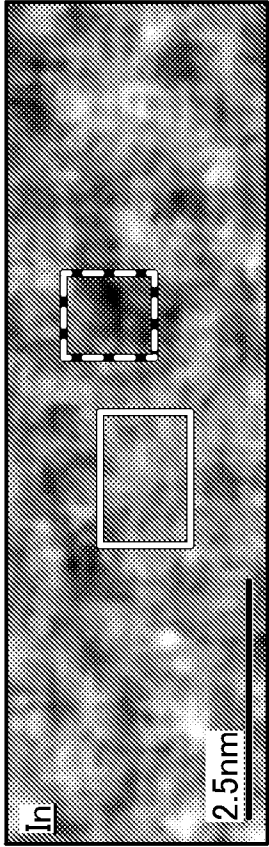
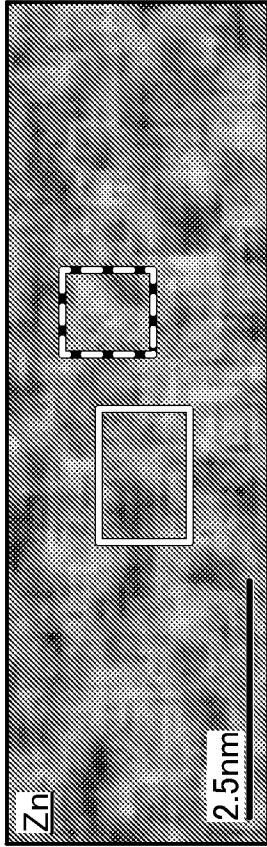


FIG. 38C



INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2016/052927

A. CLASSIFICATION OF SUBJECT MATTER		
Int.Cl. See extra sheet		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int.Cl. G02F1/1368, G02F1/1333, G02F1/1343, G06F3/041, G06F3/044, G09F9/00, G09F9/30, H01L29/786		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2016 Registered utility model specifications of Japan 1996-2016 Published registered utility model applications of Japan 1994-2016		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014/0209901 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2014.07.31, paragraphs [0067] to [0140], [0358] to [0395], [FIG.1C] [FIG.24B] & JP 2014-64011 A & CN 101944506 A & KR 10-2011-0003265 A & TW 201110243 A	1-13
Y	US 2013/0342801 A1 (SHARP KABUSHIKI KAISHA) 2013.12.26, paragraphs [0010] to [0019], [FIG.2], [0043] to [009 0], [FIG. 1] to [FIG. 6] & WO 2012/118038 A1 & CN 103403612 A	1-13
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
05.08.2016		16.08.2016
Name and mailing address of the ISA/JP		Authorized officer
Japan Patent Office		HIROTA, Kaori
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan		2L 3812
		Telephone No. +81-3-3581-1101 Ext. 3295

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2016/052927

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/0194697 A1 (APPLE INC.) 2010.08.05, paragraphs [0039]to[0079], [Fig. 4] to [Fig.11B] & EP 2214084 A1 & CN 101825966 A & TW 201031961 A & KR 10-2011-0122727 A & JP 2010-231773 A	1-13
Y A	US 2005/0030461 A1 (JAPAN DISPLAY INC., PANASONIC LIQUID CRYSTAL DISPLAY CO., LTD.) 2005.02.10, paragraphs [0178]to[0188], [Fig. 21] & JP 2015-28666 A & KR 10-2007-0046986 A & TW 285780 B	10-12 1-9, 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2016/052927

CLASSIFICATION OF SUBJECT MATTER

G02F1/1368(2006.01) i, G02F1/1333(2006.01) i, G02F1/1343(2006.01) i,
G06F3/041(2006.01) i, G06F3/044(2006.01) i, G09F9/00(2006.01) i,
G09F9/30(2006.01) i, H01L29/786(2006.01) i