METHOD OF AND APPARATUS FOR FORMING THREE-DIMENSIONAL STRUCTURES INTEGRAL WITH SEMICONDUCTOR BASED CIRCUITRY

Abstract: Enhanced Electrochemical fabrication processes are provided that can form three-dimensional multi-layer structures using semiconductor based circuitry as a substrate. Electrically functional portions of the structure are formed from structural material (e.g. nickel) that adheres to contact pads of the circuit. Aluminum contact pads and silicon structures are protected from copper diffusion damage by application of appropriate barrier layers.
Related Applications

This application claims benefit of U.S. Provisional Patent Application No. 60/379,183, filed on May 7, 2002 which is hereby incorporated herein by reference as if set forth in full.

Government Support

This invention was made with Government support under Grant Numbers DABT63-97-C-0051 and DABT63-99-C0042 awarded by DARPA. The Government has certain rights.

Field of the Invention

This invention relates to the field of electrochemical deposition and more particularly to the field of electrochemical fabrication which includes electrochemical deposition of one or more materials according to desired cross-sectional configurations so as to build up three-dimensional structures from a plurality of at least partially adhered layers of deposited material. More particularly the invention relates to the integration of multilayer electrochemically fabricated structures with semiconductor circuitry and in particular to the formation of such structures on integrated circuits.

Background

A technique for forming three-dimensional structures (e.g. parts, components, devices, and the like) from a plurality of adhered layers was invented by Adam L. Cohen and is known as Electrochemical Fabrication. It is being commercially pursued by MEMGen\textsuperscript{\textregistered} Corporation of Burbank, California under the name EFAB\textsuperscript{TM}. This technique was described in US Patent No. 6,027,830, issued on February 22, 2000. This electrochemical deposition technique allows the selective deposition of a material using a unique masking technique that involves the use of a mask that includes patterned conformable material on a support structure that is independent of the substrate onto which plating will occur. When desiring to perform an electrodeposition using the mask, the conformable portion of the mask is brought into contact with a substrate while in the presence of a plating solution such that the contact of the conformable portion of the mask to the substrate inhibits deposition at selected locations. For convenience, these masks might be generically called conformable contact masks; the masking technique may be generically called a conformable contact mask plating process. More specifically, in the terminology of MEMGen\textsuperscript{\textregistered} Corporation of Burbank, California such masks have come to be
known as INSTANT MASKS™ and the process known as INSTANT MASKING™ or INSTANT MASK™ plating. Selective depositions using conformable contact mask plating may be used to form single layers of material or may be used to form multi-layer structures. The teachings of the '630 patent are hereby incorporated herein by reference as if set forth in full herein. Since the filing of the patent application that led to the above noted patent, various papers about conformable contact mask plating (i.e. INSTANT MASKING) and electrochemical fabrication have been published:


The disclosures of these nine publications are hereby incorporated herein by reference as if set forth in full herein.

The electrochemical deposition process may be carried out in a number of different ways as set forth in the above patent and publications. In one form, this process involves the execution of three separate operations during the formation of each layer of the structure that is to be formed:

1. Selectively depositing at least one material by electrodeposition upon one or more desired regions of a substrate.

2. Then, blanket depositing at least one additional material by electrodeposition so that the additional deposit covers both the regions that were previously selectively deposited onto, and the regions of the substrate that did not receive any previously applied selective depositions.

3. Finally, planarizing the materials deposited during the first and second operations to produce a smoothed surface of a first layer of desired thickness having at least one region containing the at least one material and at least one region containing at least the one additional material.

After formation of the first layer, one or more additional layers may be formed adjacent to the immediately preceding layer and adhered to the smoothed surface of that preceding layer. These additional layers are formed by repeating the first through third operations one or more times wherein the formation of each subsequent layer treats the previously formed layers and the initial substrate as a new and thickening substrate.

Once the formation of all layers has been completed, at least a portion of at least one of the materials deposited is generally removed by an etching process to expose or release the three-dimensional structure that was intended to be formed.

The preferred method of performing the selective electrodeposition involved in the first operation is by conformable contact mask plating. In this type of plating, one or more conformable contact (CC) masks are first formed. The CC masks include a support structure onto which a patterned conformable dielectric material is adhered or formed. The conformable material for each mask is shaped in accordance with a particular cross-section of material to be plated. At least one CC mask is needed for each unique cross-sectional pattern that is to be plated.
The support for a CC mask is typically a plate-like structure formed of a metal that is to be selectively electroplated and from which material to be plated will be dissolved. In this typical approach, the support will act as an anode in an electroplating process. In an alternative approach, the support may instead be a porous or otherwise perforated material through which deposition material will pass during an electroplating operation on its way from a distal anode to a deposition surface. In either approach, it is possible for CC masks to share a common support, i.e. the patterns of conformable dielectric material for plating multiple layers of material may be located in different areas of a single support structure. When a single support structure contains multiple plating patterns, the entire structure is referred to as the CC mask while the individual plating masks may be referred to as “submasks”. In the present application such a distinction will be made only when relevant to a specific point being made.

In preparation for performing the selective deposition of the first operation, the conformable portion of the CC mask is placed in registration with and pressed against a selected portion of the substrate (or onto a previously formed layer or onto a previously deposited portion of a layer) on which deposition is to occur. The pressing together of the CC mask and substrate occur in such a way that all openings, in the conformable portions of the CC mask contain plating solution. The conformable material of the CC mask that contacts the substrate acts as a barrier to electrodeposition while the openings in the CC mask that are filled with electroplating solution act as pathways for transferring material from an anode (e.g. the CC mask support) to the non-contacted portions of the substrate (which act as a cathode during the plating operation) when an appropriate potential and/or current are supplied.

An example of a CC mask and CC mask plating are shown in Figures 1(a) - 1(c).

Figure 1(a) shows a side view of a CC mask 8 consisting of a conformable or deformable (e.g. elastomeric) insulator 10 patterned on an anode 12. The anode has two functions. Figure 1(a) also depicts a substrate 6 separated from mask 8. One is as a supporting material for the patterned insulator 10 to maintain its integrity and alignment since the pattern may be topologically complex (e.g., involving isolated “islands” of insulator material). The other function is as an anode for the electroplating operation. CC mask plating selectively deposits material 22 onto a substrate 6 by simply pressing the insulator against the substrate then electrodepositing material through apertures 26a and 26b in the insulator as shown in Figure 1(b). After deposition, the CC mask is separated, preferably non-destructively, from the substrate 6 as shown in Figure 1(c). The CC mask plating
process is distinct from a “through-mask” plating process in that in a through-mask plating process the separation of the masking material from the substrate would occur destructively. As with through-mask plating, CC mask plating deposits material selectively and simultaneously over the entire layer. The plated region may consist of one or more isolated plating regions where these isolated plating regions may belong to a single structure that is being formed or may belong to multiple structures that are being formed simultaneously. In CC mask plating as individual masks are not intentionally destroyed in the removal process, they may be usable in multiple plating operations.

Another example of a CC mask and CC mask plating is shown in Figures 1(d) - 1(f). Figure 1(d) shows an anode 12' separated from a mask 8' that comprises a patterned conformable material 10' and a support structure 20. Figure 1(d) also depicts substrate 6 separated from the mask 8'. Figure 1(e) illustrates the mask 8' being brought into contact with the substrate 6. Figure 1(f) illustrates the deposit 22' that results from conducting a current from the anode 12' to the substrate 6. Figure 1(g) illustrates the deposit 22' on substrate 6 after separation from mask 8'. In this example, an appropriate electrolyte is located between the substrate 6 and the anode 12' and a current of ions coming from one or both of the solution and the anode are conducted through the opening in the mask to the substrate where material is deposited. This type of mask may be referred to as an anodeless INSTANT MASK™ (AIM) or as an anodeless conformable contact (ACC) mask.

Unlike through-mask plating, CC mask plating allows CC masks to be formed completely separate from the fabrication of the substrate on which plating is to occur (e.g. separate from a three-dimensional (3D) structure that is being formed). CC masks may be formed in a variety of ways, for example, a photolithographic process may be used. All masks can be generated simultaneously, prior to structure fabrication rather than during it.

This separation makes possible a simple, low-cost, automated, self-contained, and internally-clean “desktop factory” that can be installed almost anywhere to fabricate 3D structures, leaving any required clean room processes, such as photolithography to be performed by service bureaus or the like.

An example of the electrochemical fabrication process discussed above is illustrated in Figures 2(a) - 2(f). These figures show that the process involves deposition of a first material 2 which is a sacrificial material and a second material 4 which is a structural material. The CC mask 8, in this example, includes a patterned conformable material (e.g. an elastomeric dielectric material) 10 and a support 12 which is made from deposition material 2. The conformal portion of the CC mask is pressed against substrate
6 with a plating solution 14 located within the openings 16 in the conformable material 10. An electric current, from power supply 18, is then passed through the plating solution 14 via (a) support 12 which doubles as an anode and (b) substrate 6 which doubles as a cathode. Figure 2(a), illustrates that the passing of current causes material 2 within the plating solution and material 2 from the anode 12 to be selectively transferred to and plated on the cathode 6. After electroplating the first deposition material 2 onto the substrate 6 using CC mask 8, the CC mask 8 is removed as shown in Figure 2(b). Figure 2(c) depicts the second deposition material 4 as having been blanket-deposited (i.e. non-selectively deposited) over the previously deposited first deposition material 2 as well as over the other portions of the substrate 6. The blanket deposition occurs by electroplating from an anode (not shown), composed of the second material, through an appropriate plating solution (not shown), and to the cathode/substrate 6. The entire two-material layer is then planarized to achieve precise thickness and flatness as shown in Figure 2(d). After repetition of this process for all layers, the multi-layer structure 20 formed of the second material 4 (i.e. structural material) is embedded in first material 2 (i.e. sacrificial material) as shown in Figure 2(e). The embedded structure is etched to yield the desired device, i.e. structure 20, as shown in Figure 2(f).

Various components of an exemplary manual electrochemical fabrication system 32 are shown in Figures 3(a) - 3(c). The system 32 consists of several subsystems 34, 36, 38, and 40. The substrate holding subsystem 34 is depicted in the upper portions of each of Figures 3(a) to 3(c) and includes several components: (1) a carrier 48, (2) a metal substrate 6 onto which the layers are deposited, and (3) a linear slide 42 capable of moving the substrate 6 up and down relative to the carrier 48 in response to drive force from actuator 44. Subsystem 34 also includes an indicator 46 for measuring differences in vertical position of the substrate which may be used in setting or determining layer thicknesses and/or deposition thicknesses. The subsystem 34 further includes feet 68 for carrier 48 which can be precisely mounted on subsystem 36.

The CC mask subsystem 36 shown in the lower portion of Figure 3(a) includes several components: (1) a CC mask 8 that is actually made up of a number of CC masks (i.e. submasks) that share a common support/anode 12, (2) precision X-stage 54, (3) precision Y-stage 56, (4) frame 72 on which the feet 68 of subsystem 34 can mount, and (5) a tank 58 for containing the electrolyte 16. Subsystems 34 and 36 also include appropriate electrical connections (not shown) for connecting to an appropriate power source for driving the CC masking process.
The blanket deposition subsystem 38 is shown in the lower portion of Figure 3(b) and includes several components: (1) an anode 62, (2) an electrolyte tank 64 for holding plating solution 66, and (3) frame 74 on which the feet 68 of subsystem 34 may sit. Subsystem 38 also includes appropriate electrical connections (not shown) for connecting the anode to an appropriate power supply for driving the blanket deposition process.

The planarization subsystem 40 is shown in the lower portion of Figure 3(c) and includes a lapping plate 52 and associated motion and control systems (not shown) for planarizing the depositions.

In addition to the above teachings, the ‘630 patent sets forth a process for integrating EFAB production with integrated circuits. In this process the structural EFAB material is plated onto and in electrical contact with aluminum contact pads on the integrated circuit. These contact pads may be considered primary contact pads and the locations to which contact with the EFAB structural material will be made. In the described process the integrated circuit design is modified to include secondary contact pads (i.e. one or more pads) that are electrically connected to the primary pads but are spaced therefrom by a distance. The secondary contact pads provide connection points for feeding current to the primary contact pads so that the primary pads may function as cathodes during electroplating operations. The process is illustrated in Figures 13a - 13i of that patent and is outlined as follows:

1. The process starts with
   a. An integrated circuit that includes a silicon wafer 38, a primary contact pad 40, and a secondary contact pad 41 connected to the primary pad by conductor 42. With the exception of the contact pads 40 and 41 the integrated circuit is covered by passivation layer 44 (Figure 13a & 13b); and
   b. A polyimide 34 coated copper disk 36. The polyimide may be coated onto the disk by spin coating.

2. The copper disk 36 is adhered to the bottom surface of the silicon wafer 38 with the polyimide 34 coated surface of the copper disk located between the copper and the silicon.

3. The silicon wafer is partially sawed through which assists in separation of the die after processing.

4. A photosensitive polyimide 35 is spin coated onto the top surface of wafer 38. This coating provides an additional passivation layer and potentially protects aluminum pads 40 and 41 during subsequent etching operations and it fills saw line 46.
5. The polyimide 35 is patterned by selective exposure to light and subsequent
development to expose contact pads 40 and 41.

6. The wafer is degreased and immersed in zincate plating solution which
provides a thin coating over the exposed aluminum contact pads to increase adhesion of
subsequently deposited material.

7. A photoresist is applied and patterned leaving a valley into which copper
may be deposited to form a bus 48 that connects contact pads 41 (Fig. 13d). Copper is
deposited, for example by sputtering and the photoresist is removed leaving behind
copper bus 48.

8. A photoresist is applied and patterned to cover most of bus 48 to prevent
nickel from depositing thereon.

9. Electrical contact is made with the portion of the bus 48 that is not covered
by photoresist and then plating enough nickel 50 (Fig. 13e) on aluminum pad 40 to allow
subsequent planarization.

10. The photoresist is removed thereby exposing the entire copper bus 48.

11. A thin plating base of copper 51 is deposited, e.g. by sputtering, over the
entire surface of the integrated circuit.

12. Electrical contact is made with the copper and a sufficient amount of copper
52 is then electroplated over the entire wafer surface to allow planarization (FIG. 13F).

13. The surface is planarized to expose the nickel 50 (Fig. 13g).

14. Layers of the microstructure are electroplated (Fig. 13h).

15. The copper deposited by electroplating and sputtering is removed by
etching.

16. The polyimide 35 is stripped thereby exposing the resulting microstructure
device 54 attached to wafer 38 (Fig. 13i).

Another method for forming microstructures from electroplated metals (i.e. using
electrochemical fabrication techniques) is taught in US Patent No. 5,190,637 to Henry
Guckel, entitled “Formation of Microstructures by Multiple Level Deep X-ray Lithography
with Sacrificial Metal layers. This patent teaches the formation of metal structure utilizing
mask exposures. A first layer of a primary metal is electroplated onto an exposed plating
base to fill a void in a photoresist, the photoresist is then removed and a secondary metal
is electroplated over the first layer and over the plating base. The exposed surface of the
secondary metal is then machined down to a height which exposes the first metal to
produce a flat uniform surface extending across the both the primary and secondary
metals. Formation of a second layer may then begin by applying a photoresist layer over the first layer and then repeating the process used to produce the first layer. The process is then repeated until the entire structure is formed and the secondary metal is removed by etching. The photoresist is formed over the plating base or previous layer by casting and the voids in the photoresist are formed by exposure of the photoresist through a patterned mask via X-rays or UV radiation.

Even in view of these teachings a need remains in the electrochemical fabrication arts for alternative processes and simpler processes for integrating electrochemically fabricated structures with integrated circuits and particularly for processes that allow formation of multilayer electrochemically fabricated structures on and in electrical contact with semiconductor produced circuitry.

**Summary of the Invention**

It is an object of various aspects of the present invention to provide alternative processes for integrating electrochemically fabricated multilayer structures with integrated circuits.

It is an object of various aspects of the present invention to provide simpler processes for integrating electrochemically fabricated multilayer structures with integrated circuits.

It is an object of various aspects of the present invention to provide simpler processes that allow formation of multilayer electrochemically fabricated structure on and in electrical contact with semiconductor produced circuitry.

Other objects and advantages of various aspects of the invention will be apparent to those of skill in the art upon review of the teachings herein. The various aspects of the invention, set forth explicitly herein or otherwise ascertained from the teachings herein, may address any one of the above objects alone or in combination, or alternatively may not address any of the objects set forth above but instead address some other object ascertained from the teachings herein. It is not intended that all of these objects be addressed by any single aspect of the invention even though that may be the case with regard to some aspects.

A first aspect of the invention provides an electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process including: (A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may include previously deposited material; (B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited
layers, wherein said forming includes repeating operation (A) a plurality of times; wherein at least a plurality of the selective depositing operations include: (1) locating a mask on or in proximity to a substrate; (2) in presence of a plating solution, conducting an electric current between an anode and the substrate through the at least one opening in the mask, such that a selected deposition material is deposited onto the substrate to form at least a portion of a layer; and (3) separating the selected preformed mask from the substrate; wherein the substrate includes a semiconductor wafer or single die containing electrical circuitry and having contact pads to which structural material is to connect; and wherein the process of contacting the contact pads with structural material includes in order: (a) placing a protective coating over the contact pads; (b) applying a layer of sacrificial material to a surface of the wafer, (c) removing the protective coating from the contact pads; and (d) applying a coating of structural material to the contact pads.

A second aspect of the invention provides an electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process including: (A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may include previously deposited material; (B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited layers, wherein said forming includes repeating operation (A) a plurality of times; wherein at least a plurality of the selective depositing operations include: (1) locating a mask on or in proximity to a substrate; (2) in presence of a plating solution, conducting an electric current between an anode and the substrate through the at least one opening in the mask, such that a selected deposition material is deposited onto the substrate to form at least a portion of a layer; and (3) separating the selected preformed mask from the substrate; wherein the substrate includes a semiconductor wafer or single die containing electrical circuitry and having contact pads to which structural material is to connect; and wherein the process of contacting the contact pads with structural material includes, in order: (a) depositing sacrificial material onto a surface of the wafer or die in regions excluding contact pad regions; and (b) depositing structural material to at least selected contact pad regions.

A third aspect of the invention provides an electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process including: (A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may include previously deposited material; (B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited
layers, wherein said forming includes repeating operation (A) a plurality of times; wherein 
at least a plurality of the selective depositing operations include: (1) locating a mask on or 
in proximity to a substrate; (2) in presence of a plating solution, conducting an electric 
current between an anode and the substrate through the at least one opening in the mask, 
such that a selected deposition material is deposited onto the substrate to form at least a 
portion of a layer; and (3) separating the selected preformed mask from the substrate; 
wherein the substrate includes a semiconductor wafer or single die containing electrical 
circuitry and having contact pads to which structural material is to connect and having a 
passivation layer; and wherein the process of contacting the contact pads with structural 
material includes in order: (a) locating an electroless plating catalyst for a sacrificial 
material on at least a portion of the surface of the passivation layer; (b) electroless plating 
the sacrificial material on to the passivation layer; (c) applying a structural material over 
the contact pads.

Further aspects of the invention will be understood by those of skill in the art upon 
reviewing the teachings herein. Other aspects of the invention may involve combinations 
of the above noted aspects of the invention and/or addition of various feat.3ures of one or 
more embodiments. Other aspects of the invention may involve apparatus that can be 
used in implementing one or more of the above method aspects of the invention. These 
other aspects of the invention may provide various combinations of the aspects presented 
above as well as provide other configurations, structures, functional relationships, and 
processes that have not been specifically set forth above.

**Brief Description of the Drawings**

Figures 1(a) - 1(c) schematically depict side views of various stages of a CC mask 
plating process, while Figures 1(d) - (g) schematically depict a side views of various 
stages of a CC mask plating process using a different type of CC mask.

Figures 2(a) - 2(f) schematically depict side views of various stages of an 
electrochemical fabrication process as applied to the formation of a particular structure 
where a sacrificial material is selectively deposited while a structural material is blanket 
deposited.

Figures 3(a) - 3(c) schematically depict side views of various example 
subassemblies that may be used in manually implementing the electrochemical fabrication 
method depicted in Figures 2(a) - 2(f).

Figures 4(a) – 4(j) schematically depict the formation of a first layer of a structure 
using adhered mask plating where the blanket deposition of a second material overlays
both the openings between deposition locations of a first material and the first material itself.

Figures 5(a) - 5(l) schematically depict side views of various stages of a process according to a first embodiment for forming electrochemically fabricated structures on integrated circuits.

Figures 6(a) – 6(f) schematically depict side views of various stages of a process according to one variation of a second embodiment for forming electrochemically fabricated structures on integrated circuits.

**Detailed Description**

Figures 1(a) - 1(g), 2(a) - 2(f), and 3(a) - 3(c) illustrate various features of one form of electrochemical fabrication that are known. Other electrochemical fabrication techniques are set forth in the '630 patent referenced above, in the various previously incorporated publications, in various other patents and patent applications incorporated herein by reference, still others may be derived from combinations of various approaches described in these publications, patents, and applications, or are otherwise known or ascertainable by those of skill in the art from the teachings set forth herein. All of these techniques may be combined with those of the various embodiments of various aspects of the invention to yield enhanced embodiments. Still other embodiments may be derived from combinations of the various embodiments explicitly set forth herein.

Figures 4(a)-4(i) illustrate various stages in the formation of a single layer of a multilayer fabrication process where a second metal is deposited on a first metal as well as in openings in the first metal where its deposition forms part of the layer. In Figure 4(a), a side view of a substrate 82 is shown, onto which patternable photoresist 84 is cast as shown in Figure 4(b). In Figure 4(c), a pattern of resist is shown that results from the curing, exposing, and developing of the resist. The patterning of the photoresist 84 results in openings or apertures 92(a) - 92(c) extending from a surface 86 of the photoresist through the thickness of the photoresist to surface 88 of the substrate 82. In Figure 4(d), a metal 94 (e.g., nickel) is shown as having been electroplated into the openings 92(a) - 92(c). In Figure 4(e), the photoresist has been removed (i.e., chemically stripped) from the substrate to expose regions of the substrate 82 which are not covered with the first metal 94. In Figure 4(f), a second metal 96 (e.g., silver) is shown as having been blanket electroplated over the entire exposed portions of the substrate 82 (which is conductive) and over the first metal 94 (which is also conductive). Figure 4(g) depicts the completed first layer of the structure which has resulted from the planarization of the first and second
metals down to a height that exposes the first metal and sets a thickness for the first layer. In Figure 4(h) the result of repeating the process steps shown in Figures 4(b) - 4(g) several times to form a multi-layer structure are shown where each layer consists of two materials. For most applications, one of these materials is removed as shown in Figure 4(i) to yield a desired 3-D structure 98 (e.g. component or device).

The various electrochemical fabrication processes used in various embodiments, alternatives, and techniques disclosed herein may have application to conformable contact masks and masking operations, proximity masks and masking operations (i.e. operations that use masks that at least partially selectively shield a substrate by their proximity to the substrate even if contact is not made), non-conformable masks and masking operations (i.e. masks and operations based on masks whose contact surfaces are not significantly conformable), and adhered masks and masking operations (masks and operations that use masks that are adhered to a substrate onto which selective deposition or etching is to occur as opposed to only being contacted to it).

Various embodiments are directed to techniques for interfacing or integrating the electrochemical fabrication of multi-layer three dimensional structures with semiconductor devices (e.g. integrated circuits) or devices produced by semiconductor manufacturing techniques. In the various embodiments presented hereafter, the semiconductor devices are provided in wafer form or die form and are used as substrates for the electrochemical fabrication build up process. These devices may be supplied with a passivation layer of adequate thickness already applied or such layers may be thickened prior to beginning the integration process.

An integration process of a first preferred embodiment is depicted in Figures 5(a) - 5(l). A wafer 102 (or single die) is received from a standard IC fabrication process as shown in Figure 5(a). The wafer includes electronic circuitry (not shown) with interface contact pads 104 and connected bus contact pads 106 exposed. The pads are connected by runners 108 which travel under a passivation layer 112 which covers the surface of the wafer 102. Pads 104 and runners 108 may have been specifically designed with the intent of integrating a device made by electrochemical fabrication, or alternatively pre-designed pads and interconnects that can serve as runners may be used. Other pads (not shown) may be located on wafer 102 for purposes of wire bonding, flip chip packaging, etc.

A photoresist layer 122 is applied to the upper surface of the wafer as shown in Figure 5(b). The photoresist is patterned so that the interface pads 104 remain covered.
with hardened photoresist 124 as shown in Figure 5(c). These covered pads are the ones to which the multilayer electrochemically fabricated structure will be interfaced.

A thin layer of copper 126 is deposited over the entire surface as shown in Figure 5(d). The deposition of the copper may for example occur via a physical vapor deposition process (e.g. evaporated or sputtered), via electroless copper plating, or via direct metallization (i.e. direct plating). As the adhesion between the copper and the exposed aluminum bus contact pads is not critical it may be unnecessary to apply a coating of zincate to the surface prior to copper deposition. But a zincate coating can be applied if desired or found necessary. Furthermore, as the bus contact pads 106 are located some distance from the interface contact pads, some damage by the copper to the bus contact pads may be acceptable. If such damage is a concern or found to be a problem a barrier layer can be applied prior to the copper deposition. The barrier layer can then be removed toward the end of the process after removal of the copper.

Next, electrical contact is made to the thin copper coating 126 and thick copper 128 is plated as shown in Figure 5(e) with a sufficient depth to allow planarization to occur.

Next the applied coatings of copper are planarized to expose the resist 124 overlaying the interface contact pads 104 as shown in Figure 5(f). The resist 124 is then removed as shown in Figure 5(g).

Next, a transition/barrier layer 132 is deposited onto the wafer as shown in Figure 5(h). The transition/barrier layer may include one or both of a coating of an adhesion promoter (such as zincate) and a diffusion barrier such as titanium nitride (TiN), tantalum (Ta), and/or tantalum Nitride (TaN).

Next, electrical contact is made to the barrier layer and an electrochemical fabrication structural material 134 (e.g., Ni) is plated thickly as shown in Figure 5(i).

The deposits are again planarized as shown Figure 5(j) exposing the thickly plated copper 128, and removing the barrier layer 132 except near where it bounds the remaining nickel deposit 134 near the interface contact pads 104.

After again making electrical contact with the deposited metal, the electrochemical fabrication process is performed to build up the multiple layers of the three dimensional structure. The multilayer deposition process is shown as completed in Figure 5(k). The electrochemical fabrication process may be performed in a variety of manners and may include a variety of operations, such as, for example, selective depositions, selective etchings, blanket depositions, blanket etchings, planarization operations, and the like. It may also include various cleaning, activation, passivation, and other treatment operations.
The selection of operations and the ordering of the operations may vary from build process to build process or even from layer-to-layer within a single build process. Any selective deposition operations, selective etching operations, or selective treatment operations may make use of contact masks (e.g. of the conformable or non-conformable type), proximity masks, and/or adhered masks.

Next, all of the deposited copper is removed by etching as indicated in Figure 5(l). Only the structural material from the electrochemical fabrication process is left behind along with the transition/barrier layer and the wafer or (single die) material deposited between the nickel and interface contact pads 104 and covering a portion of the sides of the nickel around the interface contact pads. In this way the structure produced by electrochemical fabrication is mechanically and electrically interfaced to the metallization of the wafer.

Various alternatives to this first embodiment are possible. For example, a diffusion barrier layer could be deposited prior to the thin copper deposit 126 but after formation of the patterned resist 124, it could be removed by controlled etching as its surface area would be largely exposed compared to the amount of exposure that a coating between the interface contact pads 104 and the electrochemically fabricated structure would have. Due to this differential in exposure, it is believed that controlled etching may be performed, after layer formation is complete and the sacrificial material has been removed, to remove the barrier/transition layer from non-contact regions of the electrochemically fabricated structure without excessive damage to the contact regions after layer formation.

In another alternative embodiment, a barrier layer could be applied prior to the application of the photoresist thereby obviating the need for a potential barrier layer prior to thin copper deposition of Figure 5(d) and prior to the structural material deposition of Figure 5(l). In this alternative the uncovered portion of the barrier layer would be removed after the removal of the copper.

In other alternative embodiments an adhesion transition layer may also be formed at different stages of the process.

In another alternative embodiment the runner and bus pad would not be needed.

In this alternative, the interface pad is made larger than the area intended for deposition of the structural material (e.g. Ni). In this alternative, the portion of the interface contact pad 104 that is not covered by the structural material serves as the contact pad (rather than having a remote contact pad). However, since Al metallization used in the integrated circuit device may be attacked by the Cu stripper, etching of the Cu surrounding the
structural material may damage the pad near the structural material. Using the runner and remote contact pad avoids this problem. Also this alternative embodiment could benefit from the previous alternative embodiment where the pre-photoresist application of a barrier layer would inhibit the attack.

A second group of embodiments may take an alternative approach to interfacing the wafer 102 to the initial conductive deposits onto which the multiple layers of the structure will be formed. Figures 6(a) - 6(f) show one variation of the second group of embodiments. Figure 6(a) shows wafer 102 which may be prepared for the interfacing process by, for example, coating pads 140 with a material that facilitates electrodeposition or enhances adhesion (e.g., zincate treatment for aluminum pads) or adding additional passivation or barrier layers to protect wafer 102 from materials (e.g., sodium) which may be present in plating or etching baths. In Figure 6(b), a catalyst 142 for an electroless plating bath that is suitable for depositing the sacrificial material has been applied to the surface of the IC passivation layer 112. Catalyst 142 may be selectively located on the passivation layer away from contact pads 140 so that sacrificial material will not be inadvertently deposited onto the contact pads. However, if catalyst 142 coats only the perimeter of pads 140 this is acceptable and may be desirable in some embodiments. Catalyst 142 may be selectively applied, for example, by contacting the protruding surface of passivation 112 with a plate or stamp coated with a thin film of catalyst 142, or by selectively dispensing catalyst 142 (e.g. via an ink jet or an extrusion head).

In Figure 6(c), sacrificial material 144 has been deposited onto the catalyzed surface, which is assumed to be confined to the top surface of passivation 112. In Figure 6(d) the deposit has been continued until material 144 'mushrooms' out and makes contact with the perimeter of pads 140. Once such contact is made, pads 140 are in electrical contact with one another and with material 144 and can be electrodeposited with another material. In Figure 6(e), structural material has been electrodeposited onto pads 140. Finally, in Figure 6(f), sacrificial and structural materials have been planarized so as to create a relatively flat and smooth substrate—as in Figure 5(j)—suitable as a starting layer for further electrochemical fabrication operations where the starting layer includes regions of sacrificial material (e.g., copper) and regions of structural material (e.g., nickel). In other words, the starting layer includes a structural material in regions that contact the pads and are intended to be electrically active, while a temporary presence of copper is located in all other regions.
An integration process of a first preferred embodiment is depicted in Figures 5(a) - 5(l). A wafer 102 (or single die) is received from a standard IC fabrication process as shown in Figure 5(a). The wafer includes electronic circuitry (not shown) with interface contact pads 104 and connected bus contact pads 106 exposed. The pads are connected by runners 108 which travel under a passivation layer 112 which covers the surface of the wafer 102.

A photoresist layer 122 is applied to the upper surface of the wafer as shown in Figure 5(b). The photoresist is patterned so that the interface pads 104 remained covered with hardened photoresist 124 as shown in Figure 5(c). These covered pads are the ones to which the multilayer electrochemically fabricated structure will be interfaced.

A thin layer of copper 126 is deposited over the entire surface as shown in Figure 5(d). The deposition of the copper may for example occur via a physical vapor deposition process (e.g. evaporated or sputtered) or electroless copper plating. As the adhesion between the copper and the exposed aluminum bus contact pads is not critical it may be unnecessary to apply a coating of zincate to the surface prior to copper deposition. But a Zincate coating can be applied is desired or found necessary. Furthermore, as the bus contact pads 106 are located some distance from the interface contact pads, some damage by the copper to the bus contact pads may be acceptable. If such damage is a concern or found to be a problem a barrier layer can be applied prior to the copper deposition. The barrier layer can then be removed toward the end of the process after removal of the copper.

Next, electrical contact is made to the thin copper coating 126 and thick copper 128 is plated as shown in Figure 5(e) with a sufficient depth to allow planarization to occur.

Next the applied coatings of copper are planarized to expose the resist overlaying the interface contact pads 104 as shown in Figure 5(f). The resist is then removed as shown in Figure 5(g).

Next, a transition/barrier layer 132 is deposited onto the wafer as shown in Figure 5(h). The transition/barrier layer may include one or both of a coating of an adhesion promoter (such as zincate) amid a diffusion barrier such as titanium nitride (TiN), tantalum (Ta), and/or tantalum Nitride (TaN).

Next, electrical contact is made to the barrier layer and an electrochemical fabrication structural material 134 (e.g., Ni) is plated thickly as shown in Figure 5(i).

Though the present embodiments have focused on electrochemically fabricated structures containing a structural material of nickel and a sacrificial material of copper,
other embodiments are possible where different structural and/or sacrificial materials are used. Furthermore, interfacing between a wafer or die and electrochemically produced structures utilizing different structural and/or sacrificial materials may occur via the nickel and copper materials exemplified herein or may occur via the different materials according to the generalized applicability of the processes set forth herein to those materials. Still other embodiments will be apparent to those of skill in the art upon reviewing the teaching herein, such as processes that involves various combinations of the operations used in the different embodiments disclosed herein.

Various alternatives to and variations of the above noted embodiments exist. In some alternative embodiments, the structural material of choice is nickel and the sacrificial material of choice is copper, and in other embodiments other or additional structural materials may be chosen and other or additional sacrificial materials may be chosen.

Various other embodiments exist. Some of these embodiments may be based on a combination of the teachings herein with various teachings incorporated herein by reference. Some embodiments may not use any blanket deposition process and/or they may not use a planarization process. Some embodiments may involve the selective deposition of a plurality of different materials on a single layer or on different layers. Some embodiments may use blanket depositions processes that are not electrodeposition processes. Some embodiments may use selective deposition processes on some layers that are not conformable contact masking processes and are not even electrodeposition processes. Some embodiments may use nickel as a structural material while other embodiments may use different materials such as gold, silver, or any other electrodepositable materials that can be separated from the copper and/or some other sacrificial material. Some embodiments may use copper as the structural material with or without a sacrificial material. Some embodiments may remove a sacrificial material while other embodiments may not. In some embodiments the anode may be different from the conformable contact mask support and the support may be a porous structure or other perforated structure. Some embodiments may use multiple conformable contact masks with different patterns so as to deposit different selective patterns of material on different layers and/or on different portions of a single layer. In some embodiments, the depth of deposition will be enhanced by pulling the conformable contact mask away from the substrate as deposition is occurring in a manner that allows the seal between the conformable portion of the CC mask and the substrate to shift from the face of the conformal material to the inside edges of the conformable material.
In view of the teachings herein, many further embodiments, alternatives in design and uses of the invention will be apparent to those of skill in the art. As such, it is not intended that the invention be limited to the particular illustrative embodiments, alternatives, and uses described above but instead that it be solely limited by the claims presented hereafter.
I claim:

1. An electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process comprising:
   (A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may comprise previously deposited material;
   (B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited layers, wherein said forming comprises repeating operation (A) a plurality of times;
   wherein at least a plurality of the selective depositing operations comprise:
      (1) locating a mask on or in proximity to a substrate;
      (2) in presence of a plating solution, conducting an electric current between an anode and the substrate through the at least one opening in the mask, such that a selected deposition material is deposited onto the substrate to form at least a portion of a layer; and
      (3) separating the selected preformed mask from the substrate;
   wherein the substrate comprises a semiconductor wafer or single die containing electrical circuitry and having contact pads to which structural material is to connect; and
   wherein the process of contacting the contact pads with structural material comprises in order:
      (a) placing a protective coating over the contact pads;
      (b) applying a layer of sacrificial material to a surface of the wafer,
      (c) removing the protective coating from the contact pads; and
      (d) applying a coating of structural material to the contact pads.

2. The process of claim 1 wherein a plurality of layers comprise at least one structural material and at least one sacrificial material.

3. The process of claim 1 wherein the applied layer of sacrificial material is thin compared to a desired coating thickness, and wherein after operation (b) and before operation (c), the process additional comprises:
   (b2) thickening the thin layer to many times its original thickness via electroplating.
4. The process of claim 3, wherein after performance of operation (b2) and before operation (c), the process additionally comprises:
   (b3) planarizing the sacrificial material and the protective coating.

5. The process of claim 4, wherein after performance of operation (d), the process additionally comprises:
   (e) planarizing the structural and sacrificial materials.

6. The process of claim 5, wherein after performance of operation (e), the process additionally comprises:
   (e) forming a plurality of layers comprising at least one structural material and at least one sacrificial material.

7. The process of claim 1 additionally comprising:
   (A) supplying a plurality of preformed masks, wherein each mask comprises a patterned dielectric material that includes at least one opening through which deposition can take place during the formation of at least a portion of a layer, and wherein each mask comprises a support structure that supports the patterned dielectric material; and wherein the locating of a mask on or in proximity to a substrate comprises contacting the substrate and the dielectric material of a selected preformed mask.

8. The process of claim 1 wherein the locating of a mask on or in proximity to a substrate comprises forming and adhering a patterned mask to the substrate.

9. The process of claim 1 wherein prior to operation (d), the process further comprises applying a transition treatment to the contact pads.

10. The process of claim 9 wherein transition treatment comprises application of an adhesion promoter.

11. The process of claim 9 wherein transition treatment comprises application of a diffusion barrier.
12. An electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process comprising:

(A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may comprise previously deposited material;

(B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited layers, wherein said forming comprises repeating operation (A) a plurality of times;

wherein at least a plurality of the selective depositing operations comprise:

1. locating a mask on or in proximity to a substrate;

2. in presence of a plating solution, conducting an electric current between an anode and the substrate through the at least one opening in the mask, such that a selected deposition material is deposited onto the substrate to form at least a portion of a layer; and

3. separating the selected preformed mask from the substrate;

wherein the substrate comprises a semiconductor wafer or single die containing electrical circuitry and having contact pads to which structural material is to connect; and

wherein the process of contacting the contact pads with structural material comprises, in order:

(a) depositing sacrificial material onto a surface of the wafer or die in regions excluding contact pad regions; and

(b) depositing structural material to at least selected contact pad regions.

13. The process of claim 12 wherein a plurality of layers comprise at least one structural material and at least one sacrificial material.

14. The process of claim 12 wherein prior to performance of operation (a), the process additionally comprises placing a protective coating over the contact pads.

15. The process of claim 14 wherein after performance of operation (a), the process additionally comprises:

(a3) removing the protective coating from at least selected contact pads.
16. The process of claim 14 wherein operation (a) comprises depositing sacrificial material to a thickness less than a desired thickness using a first deposition operation and then increasing the thickness of the deposited sacrificial material using a different deposition operation.

17. The process of claim 16 wherein first deposition operation comprises something other than an electroplating operation and wherein the second deposition operation comprises at least an electroplating operation.

18. The process of claim 12 wherein after depositing the sacrificial material and depositing the structural material, planarizing the deposited materials to yield a substrate comprising selective regions of sacrificial and structural material on to which additional layers of a structural material and a sacrificial material will be deposited.

19. The process of claim 12 wherein the process further comprises applying a transition treatment to the contact pads.

20. The process of claim 19 wherein transition treatment comprises application of an adhesion promoter.

21. The process of claim 19 wherein transition treatment comprises application of a diffusion barrier.

22. The process of claim 12 wherein the structural material comprises nickel.

23. The process of claim 12 wherein the sacrificial material comprise copper.

24. The process of claim 12 additionally comprising:
   (A) supplying a plurality of preformed masks, wherein each mask comprises a patterned dielectric material that includes at least one opening through which deposition can take place during the formation of at least a portion of a layer, and wherein each mask comprises a support structure that supports the patterned dielectric material; and wherein the locating of a mask on or in proximity to a substrate comprises contacting the substrate and the dielectric material of a selected preformed mask.
25. The process of claim 12 wherein the locating of a mask on or in proximity to a substrate comprises forming and adhering a patterned mask to the substrate.

26. An electrochemical fabrication process for producing a three-dimensional structure from a plurality of adhered layers, the process comprising:

(A) selectively depositing at least a portion of a layer onto the substrate, wherein the substrate may comprise previously deposited material;

(B) forming a plurality of layers such that successive layers are formed adjacent to and adhered to previously deposited layers, wherein said forming comprises repeating operation (A) a plurality of times;

wherein at least a plurality of the selective depositing operations comprise:

(1) locating a mask on or in proximity to a substrate;

(2) in presence of a plating solution, conducting an electric current between an anode and the substrate through the at least one opening in the mask, such that a selected deposition material is deposited onto the substrate to form at least a portion of a layer; and

(3) separating the selected preformed mask from the substrate;

wherein the substrate comprises a semiconductor wafer or single die containing electrical circuitry and having contact pads to which structural material is to connect and having a passivation layer; and

wherein the process of contacting the contact pads with structural material comprises in order:

(a) locating an electroless plating catalyst for a sacrificial material on at least a portion of the surface of the passivation layer;

(b) electroless plating the sacrificial material on to the passivation layer;

(c) applying a structural material over the contact pads.

27. The process of claim 26 wherein the sacrificial material comprises copper.

28. The process of claim 26 wherein the structural material comprises nickel.

29. The process of claim 26 wherein the applying of the structural material comprises electroplating the structural material.
30. The process of claim 26 wherein after operation (b), the process additionally comprises:
   (b2) increasing the thickness of the sacrificial material by electroplating additional sacrificial material onto the electroless plated sacrificial material.

31. The process of claim 26 wherein after operation (c), the process additionally comprises:
   (d) planarizing the deposited materials.

32. The process of claim 26 wherein a plurality of layers comprise at least one structural material and at least one sacrificial material.

33. The process of claim 26 additionally comprising:
   (A) supplying a plurality of preformed masks, wherein each mask comprises a patterned dielectric material that includes at least one opening through which deposition can take place during the formation of at least a portion of a layer, and wherein each mask comprises a support structure that supports the patterned dielectric material; and wherein the locating of a mask on or in proximity to a substrate comprises contacting the substrate and the dielectric material of a selected preformed mask.

34. The process of claim 26 wherein the locating of a mask on or in proximity to a substrate comprises forming and adhering a patterned mask to the substrate.