(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 January 2016 (14.01.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/007316 A1

(51) International Patent Classification:
H03F 1/30 (2006.01)

(21) International Application Number:
PCT/US2015/038126

(22) International Filing Date:
26 June 2015 (26.06.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/329,615 11 July 2014 (11.07.2014) US

(71) Applicant: **QUALCOMM INCORPORATED** [US/US]; ATTN: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(72) Inventor: **PELUSO, Vincenzo F.**; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(74) Agent: **YEE, George B. F.**; Fountainhead Law Group P.C., 900 Lafayette St., Suite 301, Santa Clara, California 95050 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: CURRENT SENSE CIRCUIT USING A SINGLE OPAMP HAVING DC OFFSET AUTO-ZEROING

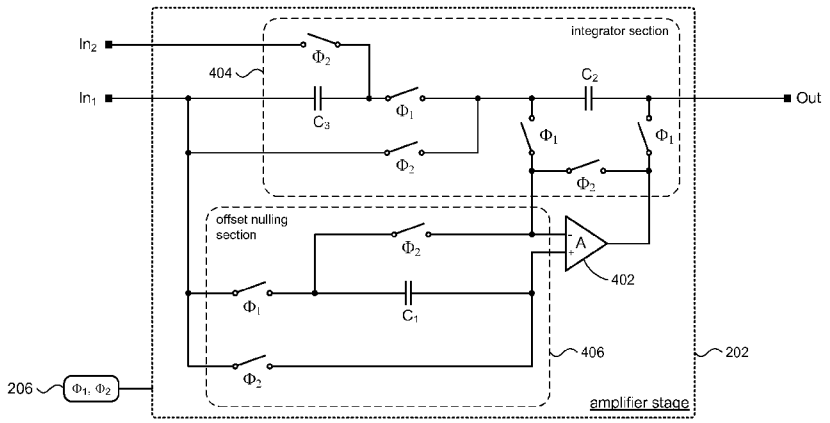

Fig. 4

(57) Abstract: A current sense circuit having a single opamp DC offset auto-zero capability that allows for continuous current sensing operation while at the same time providing for DC offset sensing and compensation. The single opamp design can operate in a first phase to sense and store a DC offset, while providing an output to drive an output stage of the current sense circuit. The single opamp design can operate in a second phase, using the sensed DC offset to generate an accurate output that can drive the output stage and which can be used in the first phase.

WO 2016/007316 A1

CURRENT SENSE CIRCUIT USING A SINGLE OPAMP HAVING DC OFFSET AUTO-ZEROING

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Application No. 14/329,615 filed July 11, 2014, the content of which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

[0002] Unless otherwise indicated, the foregoing is not admitted to be prior art to the claims recited herein and should not be construed as such.

[0003] Knowing the amount of current being delivered to a load can be useful in a wide variety of applications. For example, in low-power electronic devices (e.g., smart phone, computer tablets, and other consumer electronics) the supply current can be monitored to understand the system's impact on battery life. The load current also can be used to make safety-critical decisions in over-current protection circuits. Generally, a current sensor is a circuit that can detect a current (e.g., current through a load) and produce an output current that is representative of the detected current. In some circuit applications, the output current can be converted to an easily measured output voltage that is proportional to the detected current.

[0004] In typical current sensing circuit designs, it is important to be able to produce a sense current that accurately represents (replicates) the current flowing (the current being sensed) through the pass device that supplies current to the load. Analysis of accuracy limitations of producing a sense current of a current flowing through a pass device has shown that the replica device voltage drop across the channel must match the voltage drop across the channel of the pass device very accurately. Typically, an active high gain feedback loop is used, which employs one or more amplifiers. The offset in each amplifier should be reduced to very low values in order to produce an accurate sense current.

[0005] A technique called "auto-zeroing" can automatically drive the DC offset of an amplifier to zero. Auto zeroing uses a switched capacitor technique. The conventional

switched capacitor auto zero technique is one that prevents the amplifier from being used during part of a repeating cycle during which a capacitor samples its offset. Fig. 1, for example, shows a basic switched capacitor auto zero design. At time Φ1, switches S1 and S2 are closed and switch S3 is open, allowing the capacitor C to sense and store the DC offset Vos of amplifier A. At time Φ2, switches S1 and S2 are open and switch S3 is closed, allowing the amplifier A to operate on signal x(t), using the voltage stored in capacitor C to cancel the DC offset of amplifier A. However, during time Φ1, when the DC offset is being sensed by capacitor C, the amplifier A cannot be used to process signal x(t). This intermittency can degrade the performance of a circuit that uses amplifier A. Alternatives that do not exhibit this drawback use two opamps, each with two inputs. Such designs are therefore large, requiring more die area and consuming more power.

SUMMARY

[0006] In embodiments, a circuit includes an amplifier section that has an integrator section, an amplifier section, and an offset nulling section. The amplifier section can be connected to or disconnected from an output of the circuit. The amplifier section can be disconnected from the output of the circuit when the offset nulling section is storing an offset of the amplifier section. The integrator section can drive the output of the circuit when the amplifier section is disconnected from the output, and sense an error signal at the inputs of the circuit. The amplifier section can be connected to the output of the circuit to generate an control signal when the integrator section is connected to the amplifier section. The offset nulling section can compensate for the DC offset of the amplifier section.

[0007] In some embodiments, the amplifier section contains a single opamp. In some embodiments, the amplifier is a differential mode amplifier.

[0008] In some embodiments, the circuit may be connected in a current sense circuit.

[0009] In some embodiments, the circuit may include switches to configure the connections among the amplifier section, the integrator section, and the offset nulling section.

[0010] The following detailed description and accompanying drawings provide a better understanding of the nature and advantages of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] With respect to the discussion to follow and in particular to the drawings, it is stressed that the particulars shown represent examples for purposes of illustrative discussion, and are presented in the cause of providing a description of principles and conceptual aspects of the present disclosure. In this regard, no attempt is made to show implementation details beyond what is needed for a fundamental understanding of the present disclosure. The discussion to follow, in conjunction with the drawings, make apparent to those of skill in the art how embodiments in accordance with the present disclosure may be practiced. In the accompanying drawings:

[0012] Fig. 1 shows a conventional switched capacitor design for DC offset compensation.

[0013] Figs. 2 and 3 illustrate examples of current sensing circuits in accordance with the present disclosure.

[0014] Fig. 4 illustrates an embodiment of an amplifier stage in accordance with the present disclosure.

[0015] Fig. 4A illustrates phase Φ1 operation of the amplifier stage shown in Fig. 4.

[0016] Fig. 4B illustrates phase Φ2 operation of the amplifier stage shown in Fig. 4.

[0017] Figs. 5, 6, and 6A illustrate additional embodiments of an amplifier stage in accordance with the present disclosure.

[0018] Fig. 7 shows an example of a low dropout regulator.

[0019] Fig. 8 is a block diagram showing a current sensing device incorporated in an electronic device.

[0020] Figs. 9A and 9B illustrate timing diagrams of Φ1 and Φ2 clocks.

[0021] Fig. 10A illustrates phase Φ2 operation of the current sensing circuit of Fig. 3 in accordance with the present disclosure.

[0022] Fig. 10B illustrates phase Φ1 operation of the current sensing circuit of Fig. 3 in accordance with the present disclosure.

[0023] Fig. 11A illustrates phase Φ2 operation of the current sensing circuit of Fig. 2 in accordance with the present disclosure.

[0024] Fig. 11B illustrates phase Φ1 operation of the current sensing circuit of Fig. 2 in accordance with the present disclosure.

[0025] Fig. 12 illustrates an amplifier stage in accordance with another embodiment of the present disclosure.

DETAILED DESCRIPTION

[0026] In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present disclosure as expressed in the claims may include some or all of the features in these examples, alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0027] Fig. 2 shows a current sensing circuit 200 for sensing current flow in an electronic circuit (not shown) in accordance with the present disclosure. The current sensing circuit 200 may sense the current flow I_{load} flowing through a pass device M_{pass} into load 12 that is controlled by a control device 14. In some embodiments, for example, the pass device M_{pass} and control device 14 may constitute a low dropout (LDO) regulator. The control device 14 may be the error amplifier of the LDO (see Fig. 7, for example). It will be appreciated, however, that in other embodiments, the pass device M_{pass} and control device 14 may be components of any applicable electronic circuitry for driving load 12.

[0028] In some embodiments, the current sensing circuit 200 may comprise a sense device M_{sense} that is configured with pass device M_{pass} as a current mirror. The control inputs (e.g., gate terminals in the case of a field-effect transistor, FET) of M_{pass} and M_{sense} may be connected to the control device 14, and the outputs (e.g., source terminals) of M_{pass} and M_{sense} may be connected to the load.

[0029] In order to accurately mirror the current through M_{pass}, the voltage drop V_{DS} across the channel of M_{pass} and the channel of M_{sense} should match. Accordingly, the current sensing circuit 200 may utilize a high gain feedback loop that includes an amplifier stage (amplifier circuit) 202 to drive an output stage 204 to regulate the voltage level at input node 208b (e.g., drain terminals) of M_{sense} to match the voltage

level at input node 208a. As will be explained below, in some embodiments, the amplifier stage 202 may operate based on timing signals from timing circuitry 206.

[0030] The output stage 204 may comprise FET M_{mir1} that operates as a current source. The output (Out) of amplifier stage 202 may control the amount of current that flows through M_{mir1}. The output stage 204 may further comprise FET M_{mir2} that is configured with M_{mir1} as a current mirror. The current flow (sense current) I_{meas} through M_{mir2} is representative of the load current I_{load}. In some embodiments, the size of M_{mir2} may be dimensioned (gate width, gate length) with respect to M_{mir1} so that the current amplification ratio produces a suitable signal for I_{meas}. In some embodiments, the current mirror M_{mir1}, M_{mir2} may be biased using an internal voltage level V_{dd} that can be generated in an electronic device (e.g., Fig. 8) that incorporates the current sensing circuit 200. For example, in a battery operated device as illustrated in Fig. 8 (e.g., cellular phone, computer tablet, etc.) the internal voltage V_{dd} may come from the battery. In some embodiments, the current sensing circuit 200 may be used in sub-regulating the output (e.g., < battery voltage) of a switching power converter, e.g., as in a buck converter (not shown).

[0031] In operation, the amplifier stage 202 may regulate M_{mir1} in a feedback loop to drive the voltage difference (error) at nodes 208a, 208b sensed between inputs In_1, In_2 to zero. As the load current I_{load} varies, so will the voltage at In_1. Current through M_{mir1} can be regulated to provide the same voltage at In_2. FET M_{mir2} mirrors the current through M_{mir1}, and thus provides a sense current I_{meas} that is representative of the load current I_{load}. In accordance with the present disclosure, the DC offset in amplifier stage 202 can be significantly reduced to maintain an accurate match between the voltage drop V_{DS} across the channel of M_{sense} and the channel of M_{pass}. Additional details of the amplifier stage 202 will be provided below.

[0032] The current sense circuit 200 in Fig. 2 is suitable for a design where the pass device M_{pass} is an NMOS device. Referring to Fig. 3, a current sense circuit 300 is shown that can be used in a design where the pass device M_{pass} is a PMOS device. The output stage 304 may comprise FET M_{casc} that is configured with M_{sense} as a cascode. In this embodiment, the output of M_{casc} produces the sense current I_{meas}. The inputs In_1, In_2 of amplifier stage 202 may be connected to nodes 308a, 308b (e.g., drain terminals) of M_{pass} and M_{sense}, respectively. In operation, the amplifier stage 202 regulates M_{casc} in a

feedback loop to reduce the difference in voltage between nodes 208a, 208b sensed at inputs In_1, In_2 to zero. As the load current I_{load} varies, so will the voltage at In_1. Current through M_{casc} will be regulated so that the same voltage at node 308b appears at In_2. The current output from M_{casc} thus provides an output sense current I_{meas} that is representative of the load current I_{load}.

[0033] Referring to Fig. 4, additional details of amplifier stage 202 in accordance with the present disclosure will now be described. In some embodiments, the amplifier stage 202 may comprise two inputs In_1, In_2, and an output Out. Components in the amplifier stage 202 may include an amplifier section (amplifier) 402, an integrator section 404, and an offset nulling section 406. The amplifier 402 may be a conventional two-input operational amplifier (opamp), having an inverting (-) input and a non-inverting (+) input. In accordance with the present disclosure, the amplifier 402 comprises a single opamp.

[0034] The amplifier stage 202 may further include switches Φ1 and Φ2 that can alternate between two different configurations of OPEN and CLOSE. In some embodiments, the timing circuitry 206 (e.g., a clock circuit) may generate control signals Φ1, Φ2 to operate the switches to the OPEN state or the CLOSE state. For example, the switches identified by Φ1 can OPEN and CLOSE in accordance with a control signal Φ1, while the switches identified by Φ2 can OPEN and CLOSE in accordance with a control signal Φ2. While, in some embodiments, the timing circuitry 206 uses two control signals Φ1, Φ2 to alternate between the two switch configurations, it will be appreciated from the description to follow that in other embodiments the timing circuitry may use additional signals to control the switches between configurations.

[0035] Referring to Fig. 9A for a moment, in some embodiments, control signals Φ1 and Φ2 may be clock pulses. Each Φ1 clock and Φ2 clock may have a 50% duty cycle and be 180° out of phase with respect to each other. In practice, it is preferable that the Φ1 switches and the Φ2 switches do not CLOSE at the same time, since doing so can create shorts in the circuitry and other undesirable circuit conditions. Accordingly, in some embodiments, the duty cycle of one or both the Φ1 and the Φ2 clocks can be adjusted so that a slight delay can be introduced between the falling and rising edges of the clocks to ensure break-before-make operation between the Φ1 switches and the Φ2

switches. Fig. 9B, for example, shows clock pulses Φ1, Φ2 where a delay δ is introduce between the falling edges of Φ1 and rising edges of Φ2, and between the rising edges of Φ1 and falling edges of Φ2.

[0036] Continuing with Fig. 4, in some embodiments, the integrator section 404 may comprise a capacitor (output capacitor) C2 and a capacitor (error capacitor) C3. One side of capacitor C2 is connected to the output (Out) of amplifier stage 202. One side of capacitor C3 is connected to the In_1 input of the amplifier stage 202. In one configuration of the switches, the capacitors C2, C3 can be connected in series, and connected to the amplifier 402 in a feedback loop. In another configuration of the switches, the capacitors C2, C3, and amplifier 402 only share the In_1 input as a common reference ("virtual ground"), but are otherwise disconnected from each other.

[0037] In some embodiments, the offset nulling section 406 may comprise a capacitor (offset capacitor) C1. In one configuration of the switches, the capacitor C1 can be connected to sense and store a DC offset voltage of the amplifier 402. In another configuration of the switches, the capacitor C1 can be connected to apply the stored voltage to the amplifier 402 to compensate the amplifier's DC offset.

[0038] Referring now to Fig. 4A, operation of the amplifier stage 202 in phase Φ1 will be described. The electrical path set up by this configuration of the switches is shown in heavy lines. In phase Φ1, the capacitor C3 is connected to the amplifier 402. The output of amplifier 402 will drive the output (Out) of the amplifier stage 202 based on the charge stored in C3.

[0039] Since capacitor C2 is connected in a negative feedback loop, one of ordinary skill will understand that the amplifier 402 will effectively add the charge that is stored in C3 to the charge that is already stored in C2. The negative feedback loop will limit the amount of charge stored in C2 to the amount of charge in C3. The DC offset in amplifier 402, which would cause too much charge or too little charge to accumulate in C2, can be compensated for by capacitor C1; this will become more apparent from the description of operation of the amplifier stage 202 during phase Φ2.

[0040] Referring now to Fig. 4B, operation of the amplifier stage 202 in phase Φ2 will be described. The electrical path set up by this configuration of the switches is shown in heavy lines. In phase Φ2, the integrator section 404 is disconnected from the amplifier 402, and the output of amplifier 402 is disconnected from the output (Out) of

amplifier stage 202. Note in Fig. 4A, during phase Φ1, capacitor C2 is referenced to the In_1 input of the amplifier stage 202 through capacitor C3. In phase Φ2, since C2 is still being referenced to In_1, the charge stored on capacitor C2 can drive the output (Out) of amplifier stage 202. Thus, although the amplifier 402 is disconnected from the output Out in phase Φ2, the output Out can still be driven by C2. In phase Φ2, C3 is disconnected from C2 and is connected across the In_1 and In_2 inputs of the amplifier stage 202 to sense and store the voltage potential between the In_1 and In_2 inputs.

[0041] In phase Φ2, the amplifier 402 is configured with unity gain feedback. Capacitor C1 is connected across the inputs of amplifier 402, and referenced to the In_1 input of the amplifier stage 202. The charge that is stored in C1 by amplifier 402 represents the DC offset of the amplifier. Capacitor C1, therefore, samples and stores the DC offset of amplifier 402 in phase Φ2, which is then used in phase Φ1 to compensate for the DC offset as explained above.

[0042] Referring to Fig. 5, in some embodiments, an additional capacitor C4 may be provided to operate with capacitor C1. Capacitor C4 may provide a filtering function in usage cases where the DC offset that is sampled by C1 may vary from sample to sample, to provide for a more robust storage of the DC offset. In operation, when C1 is sampling the DC offset in phase Φ2, C4 is disconnected from the rest of the circuitry and any charge accumulated on C4 remains on C4. In phase Φ1, C1 and C4 are connected in parallel and charge sharing between C1 and C4 occurs. Over the course of a number of cycles between phase Φ1 and phase Φ2, the voltage across C1 and C4 will gradually build up to the DC offset of amplifier 402. Fluctuations in the DC offset sensed by C1 in phase Φ2 can be "smoothed" out by C4 in phase Φ1. It can be appreciated that, in other embodiments, additional such filtering capacitors may be provided.

[0043] Referring to Fig. 6, in some embodiments, the non-inverting input of amplifier 402 may be referenced to a reference voltage V_{ref} instead of the In_1 input. This configuration may be suitable in certain usage cases where the voltage difference between In_1 and the supply to the amplifier 402 (e.g., V_{IN}) is too small. An example of such a usage case is illustrated in Fig. 10A. There is a headroom requirement for the amplifier 402 to operate properly. For example, placing the amplifier 402 in unity gain feedback is problematic if the supply of the amplifier is not sufficiently greater than In_1.

In that case, the amplifier feedback loop cannot operate correctly. Fig. 6A illustrates an embodiment in which a selector 602 can be used to select between the In_1 input or a reference voltage V_{ref}, to serve as a reference for the non-inverting input of amplifier 402. Figs. 6 and 6A show the additional filtering capacitor C4 discussed above. It will be appreciated, of course, that in some embodiments, the filtering capacitor C4 can be omitted.

[0044] Referring for a moment to Fig. 2, basic operations for current sensing in accordance with the present disclosure may be summarized as follows:

- Measuring a potential difference (error) between node being monitored (e.g., 208a) and a control node (e.g., 208b) with a capacitor.
- Integrate the charge on the capacitor onto a second capacitor using an integrator.
- Using the integrator in a negative feedback loop to drive the error to zero.

[0045] Specific operations in accordance with the present disclosure may be summarized as follows:

- In one phase (e.g., Φ2)
  - sample a DC offset of an amplifier onto an offset capacitor (e.g., C1).
  - Sample an error onto an error capacitor (e.g., C3),
  - Use an output capacitor (e.g., C2) to reduce the error.
- In another phase (e.g., Φ1)
  - using the amplifier to integrate the sampled error onto the output capacitor,
  - using the amplifier to reduce the error,
  - using the offset capacitor to compensate the DC offset

[0046] Referring to Figs. 10A and 10B, a description of operation of the amplifier stage 202 in the context of the current sensing circuit 300 shown in Fig. 3 will now be described. Fig. 10A shows an embodiment of the amplifier stage 202 having filtering capacitor C4 and voltage reference V_{ref}. As explained above in connection with Fig. 3, the amplifier stage 202 senses the voltage difference between nodes 308a and 308b and regulates M_{casc} to maintain the voltage at node 308b equal to the voltage a node 308a. In the configuration of Figs. 10A and 10B, since In_1 is connected to V_{OUT}, if the circuit headroom (difference between V_{IN} and V_{OUT}) is too small, then there may be insufficient

headroom for amplifier 402 when In_1 is used as the reference ("virtual ground") and V_{IN} supplies the amplifier. Accordingly, a separate reference voltage (V_{ref}), as shown in Figs. 10A and 10B, can be provided to ensure sufficient headroom for amplifier 402.

[0047] Referring to Fig. 10A, the switches are shown in a configuration for phase Φ2. In this configuration of the switches, capacitor C3 is connected across In_1 and In_2, and to sense the voltage difference across nodes 308a and 308b. C3 therefore senses and stores the error between V_{DS} of the M_{pass} and M_{sense} devices. The amplifier stage 202 will "hold" the gate voltage of M_{casc} using capacitor C2, which is connected to the output Out, to maintain current flow through M_{casc}. Thus, even though amplifier 402 is disconnected from the output Out, M_{casc} can still operate adequately during phase Φ2 by virtue of the charge on C2. The current I_{meas} through M_{casc} is representative of the load current I_{load}. Amplifier 402, being disconnected from the output Out, can be connected in a unity gain loop with capacitor C1 in order to store the DC offset voltage of the amplifier in C1.

[0048] Referring Fig. 10B, the switches are in a configuration for phase Φ1. In this phase, the voltage on capacitor C3 stores the voltage difference between nodes 308a and 308b sensed during Φ2. This voltage difference represents the error between the nodes 308a, 308b that needs to be corrected. Since the output (Out) of amplifier 402 is connected to capacitor C2 and M_{casc}, the amplifier can integrate the charge in C3 onto C2 and at the same time regulate M_{casc} according to the error between the nodes 308a, 308b. The charge that is stored in C2 allows C2 to continue to hold the gate voltage of M_{casc} in Φ2, when the amplifier 402 is disconnected from M_{casc} to do DC offset sensing. Compensation of the DC offset of amplifier 402 during Φ1 occurs by virtue of capacitors C1 (and, in some embodiments, C4) being connected in series with C3. This arrangement allows for continuous ON operation of the load current sensing circuit 300, while allowing for DC offset correction to occur for accurate sensing of the load current.

[0049] Referring to Figs 11A and 11B, a description of operation of the amplifier stage 202 in the context of the current sensing circuit 200 shown in Fig. 2 will now be described. Fig. 11A shows an embodiment of the amplifier stage 202 having filtering capacitor C4. As explained above in connection with Fig. 2, the amplifier stage 202 senses the voltage difference (error) between nodes 208a and 208b and regulates M_{mir1} to maintain the voltage at node 208b to be equal to the voltage a node 208a. FET M_{mir2}

mirrors the current flow through M_{mir1} to produce an output current I_{meas} that represents the load current I_{load}.

[0050] In Fig. 11A, the switches are in a configuration for phase Φ2. Although amplifier 402 is disconnected from, and hence does not regulate M_{mir1}, the gate voltage of FET M_{mir1} continues to operated by virtue of the charge on capacitor C2. Capacitor C1 senses and stores the DC offset of amplifier 402. Capacitor C3 senses and stores the voltage (error) across nodes 208a, 208b.

[0051] In Fig. 11B, the switches are in a configuration for phase Φ1. The error sensed by C3 during phase Φ2 is used by the amplifier 402 to generate a signal to regulate M_{mir1} and to charge C2 so that C2 can continue to hold the gate voltage of M_{mir1} during phase Φ2. The DC offset of the amplifier 402 is compensated for by C1 (and, in some embodiments, C4).

[0052] Charge injection from operation of the switches Φ1 and Φ2 can affect the charge stored on the capacitors, thus affecting the voltage on the capacitors and impacting the accuracy of the DC offset function. By using a differential circuit (which suppresses common mode effects) charge injection can be largely made to be a common mode effect, and will hence be largely rejected by the differential circuit.

[0053] Referring now to Fig. 12, an amplifier stage 1202 in accordance with another embodiment of the present disclosure may employ a differential integrator design. Using a differential integrator offers the benefit of improving common mode rejection by virtue of the nature of a differential design. Fig. 12 shows an NMOS LDO. It will be appreciated by those of ordinary skill, however, that the differential configuration can be incorporated in a PMOS LDO.

[0054] Operation in phase Φ1 and phase Φ2 is similar to the foregoing embodiments, but in a differential context. The differential inputs of differential amplifier A1 have corresponding capacitors C1a/C1b and C2a/C2b. A2 may be a differential to single-ended amplifier/converter that can convert the differential output from A1 into a control signal at the output OUT.

[0055] Capacitors C1a and C1b sense and store the DC offsets in the differential inputs of differential amplifier A1 during phase Φ2 and serve as nulling capacitors during phase Φ1. The capacitor C3 stores the voltage difference between nodes 308a

and 308b sensed during Φ2. The charge stored on capacitor C3 can be integrated onto capacitors C2a and C2b during phase Φ1, which in turn can serve as holding capacitors during phase Φ2 to maintain the input to A2 and hence maintain the output at OUT.

Advantages and Technical Effect

[0056] Embodiments in accordance with the present disclosure can provide more accurate current sensing. In particular embodiments, accuracy in current sensing can be achieved by more accurate replication of the voltage drop of a pass transistor onto a sense transistor. Embodiments in accordance with the present disclosure can reduce DC offset in an amplifier using a single opamp auto-zeroing design that can provide continuous-on operation.

[0057] The above description illustrates various embodiments of the present disclosure along with examples of how aspects of the particular embodiments may be implemented. The above examples should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the particular embodiments as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the present disclosure as defined by the claims.

[0058] I claim the following:

1. A circuit comprising:

first and second circuit inputs;

a circuit output;

a first capacitor;

a second capacitor connected to the circuit output;

an amplifier having first and second amplifier inputs and an amplifier output; and

a plurality of switches operable to be in a first configuration and operable to be in a second configuration,

wherein, in the first configuration of the switches:

the amplifier output is disconnected from the circuit output;

the first capacitor is connected across the amplifier inputs to sense a DC offset of the amplifier; and

the second capacitor is connected only between the circuit output and one of the circuit inputs,

wherein, in the second configuration of the switches:

the amplifier output is connected to the circuit output;

the first capacitor is connected to one of the amplifier inputs to compensate for the DC offset of the amplifier; and

the second capacitor is connected to the amplifier in a feedback loop.

2. The circuit of claim 1 further comprising a third capacitor, wherein, in the first configuration of the switches, the third capacitor is connected only between the circuit inputs, wherein in the second configuration of the switches, the third capacitor is connected to both the second capacitor and the amplifier to integrate a charge of the third capacitor onto the second capacitor using the amplifier.

3. The circuit of claim 1 wherein, in both the first configuration of the switches and the second configuration of the switches, one of the circuit inputs is connected to provide a voltage reference point that is common to the first capacitor, the second capacitor, and the amplifier.

4. The circuit of claim 1 wherein, in the first configuration of the switches, the first capacitor is connected between one of the amplifier inputs and one of the circuit inputs.

5. The circuit of claim 1 wherein the first circuit input is connected to a first transistor and the second circuit input is connected to a second transistor.

6. The circuit of claim 5 wherein the first transistor and the second transistor are connected in a current mirror configuration.

7. The circuit of claim 1 wherein the circuit output is connected to an output stage comprising a first transistor.

8. The circuit of claim 7 wherein the first transistor is connected with a second transistor as a cascode.

9. The circuit of claim 7 wherein the first transistor is connected with a second transistor as a current mirror.

10. A circuit comprising:

first and second circuit inputs;

a circuit output;

an amplifier having an output, the output having a first configuration that is not connected to the circuit output and a second configuration that is connected to the circuit output;

an output capacitor that is connected to the circuit output, the output capacitor having a first configuration that is connected to the amplifier in a feedback loop and a second configuration that is not connected to the amplifier;

an input capacitor that is connected to the first circuit input, the input capacitor having a first configuration that is connected to the amplifier in a feedback loop with the output capacitor and a second configuration that is connected to only the second circuit input; and

a first offset capacitor having a first configuration that is connected to first and second inputs of the amplifier and having a second configuration that is connected in series with the input capacitor at a time when the input capacitor is connected to the amplifier in the feedback loop with the output capacitor.

11. The circuit of claim 10 further comprising a plurality of switches that are connected to the amplifier, the output capacitor, the input capacitor, and the offset capacitor, each switch being selectively operable to an open position and to a closed position.

12. The circuit of claim 11 further comprising one or more control inputs to receive control signals to operate the switches.

13. The circuit of claim 10 further comprising a plurality of switches that are operable to configure the amplifier in the first configuration, the output capacitor in the first configuration, the input capacitor in the first configuration, and the offset capacitor in the first configuration, and to configure the amplifier in the second configuration, the output capacitor in the second configuration, the input capacitor in the second configuration, and the offset capacitor in the second configuration.

14. The circuit of claim 10 further comprising a second offset capacitor that is configurable to be disconnected from the first offset capacitor at a time when the first offset capacitor is in the first configuration, and to be connected in parallel with the first offset capacitor at a time when the first offset capacitor is in the second configuration.

15. The circuit of claim 10 wherein at a time when the amplifier is in the first configuration, the output capacitor is in the first configuration, the input capacitor is in the first configuration, and the offset capacitor is in the first configuration.

16. The circuit of claim 15 wherein at a time when the amplifier is in the second configuration, the output capacitor is in the second configuration, the input capacitor is in the second configuration, and the offset capacitor is in the second configuration.

17. The circuit of claim 10 wherein the amplifier comprises a single opamp.

18. A circuit comprising:

a pass transistor having an output terminal connectable to a load;

a sense transistor connected to the pass transistor to mirror a current flow through the pass transistor;

an output stage connected to the sense transistor; and

an amplifier circuit having a first circuit input connected to the pass transistor, a second circuit input connected to the sense transistor, and a circuit output connected to the output stage, the amplifier circuit comprising:

an amplifier section having an output that is selectively connectable to and disconnectable from the circuit output;

an integrator section connected to the circuit output and selectively connectable to and disconnectable from the amplifier section; and

an offset nulling section connected to the amplifier section,

wherein the amplifier section is disconnected from the circuit output at a time when the offset nulling section is sampling an offset of the amplifier,

wherein the integrator section provides an output to the circuit output to drive the output stage at a time when the amplifier section is disconnected from the circuit output.

19. The circuit of claim 18 wherein the integrator section further stores a voltage difference between the first and second circuit inputs of the amplifier circuit at a time when the amplifier section is disconnected from the circuit output.

20. The circuit of claim 18 wherein the amplifier section is connected to the circuit output to drive the output stage at a time when the integrator section is connected to the amplifier section in a feedback loop configuration.

21. The circuit of claim 20 wherein the offset nulling section compensates a DC offset of the amplifier section using a sampled DC offset when the integrator section is connected to the amplifier section.

22. The circuit of claim 18 the output stage comprises a transistor connected to the sense transistor as a cascode.

23. The circuit of claim 18 the output stage comprises a current mirror.

24. The circuit of claim 18 the pass transistor further having a control input connectable to a control source.

25. The circuit of claim 24 the control source is an error amplifier of a low dropout regulator.

26. A circuit comprising:

first and second circuit inputs;

a circuit output;

first capacitors;

second capacitors;

a differential amplifier having first and second amplifier inputs and a differential output; and

an output amplifier connected to the circuit output, the second capacitors connected to the output amplifier;

a plurality of switches operable to be in a first configuration and operable to be in a second configuration,

wherein, in the first configuration of the switches:

the differential output is disconnected from the output amplifier;

the first capacitors are connected across the amplifier inputs to sense a DC offset of the differential amplifier; and

the second capacitors are connected only between the output amplifier and the amplifier inputs,

wherein, in the second configuration of the switches:

the differential output is connected to the output amplifier;

the first capacitors are connected to the amplifier inputs to compensate for the DC offset of the amplifier; and

the second capacitors are connected to the differential amplifier in feedback loops.

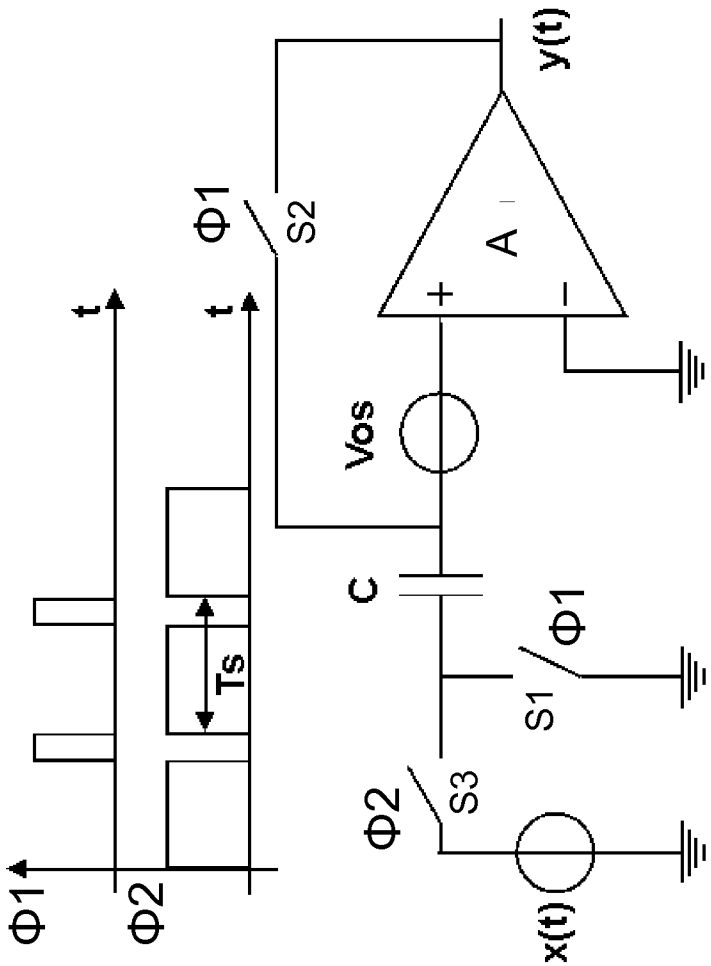

Fig. 1
(prior art)

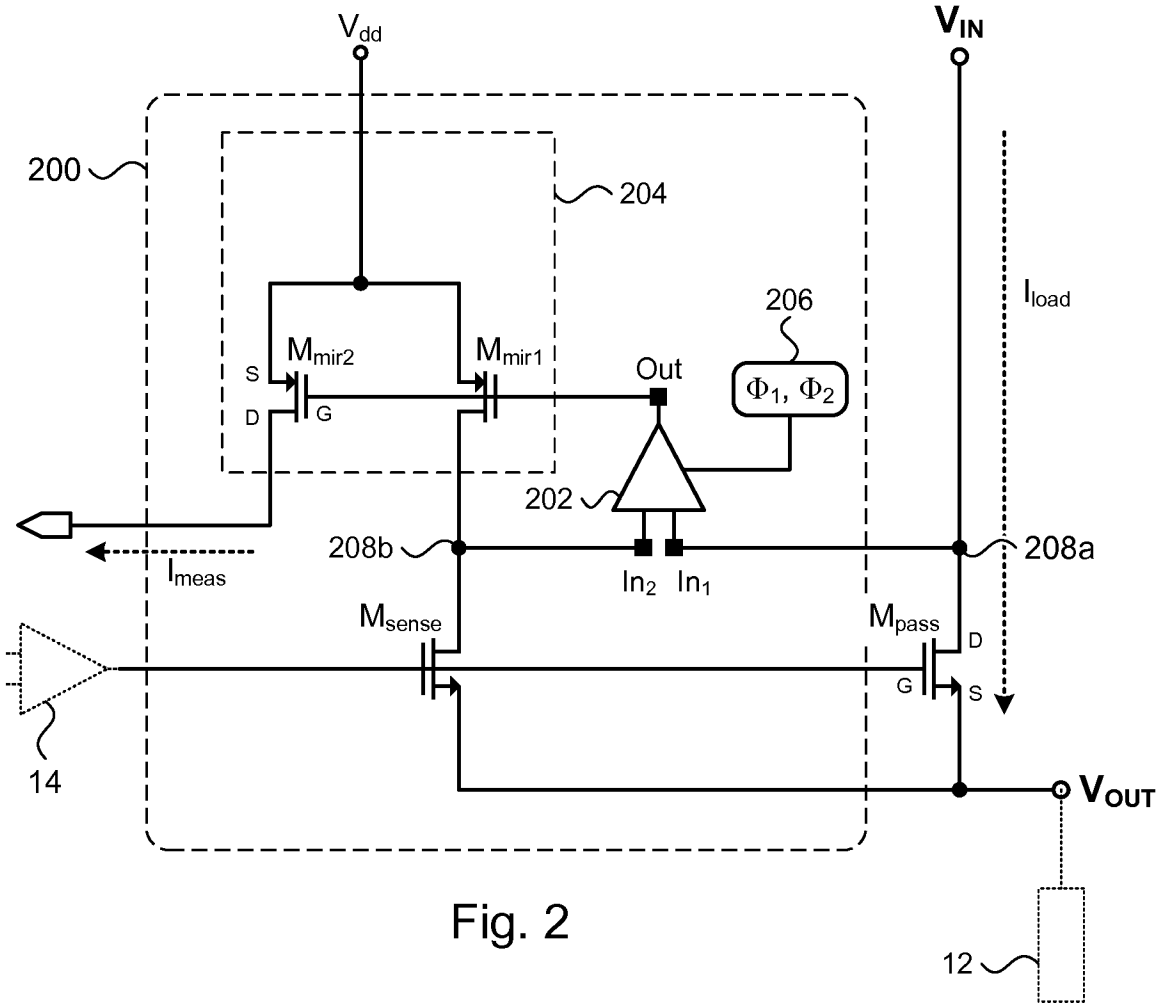
V_{dd}
V_{IN}
200
204
206
I_{load}
M_{mir2}
M_{mir1}
S
D
G
Out
Φ_1, Φ_2
202
208b
208a
I_{meas}
In_2 In_1
M_{sense}
M_{pass}
D
G
S
14
V_{OUT}
12

Fig. 2

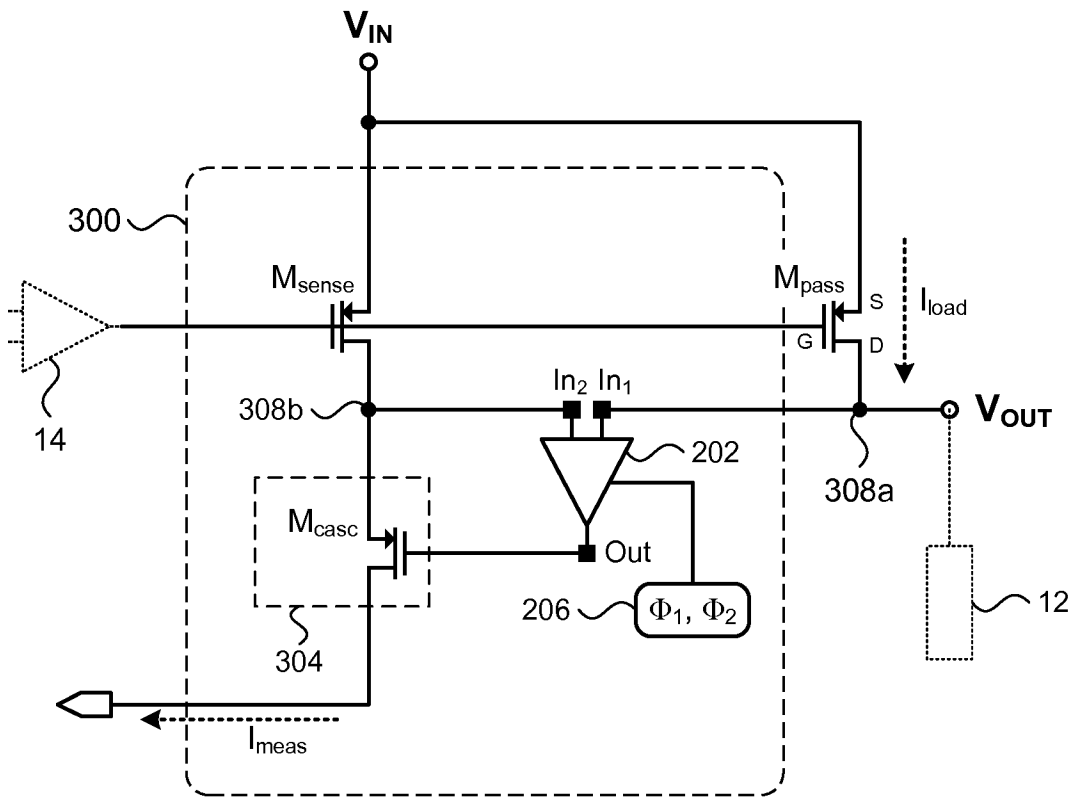
V_{IN}
300
M_{sense}
M_{pass}
S
G
D
I_{load}
14
308b
In_2 In_1
V_{OUT}
202
308a
M_{casc}
Out
206
Φ_1, Φ_2
12
304
I_{meas}

Fig. 3

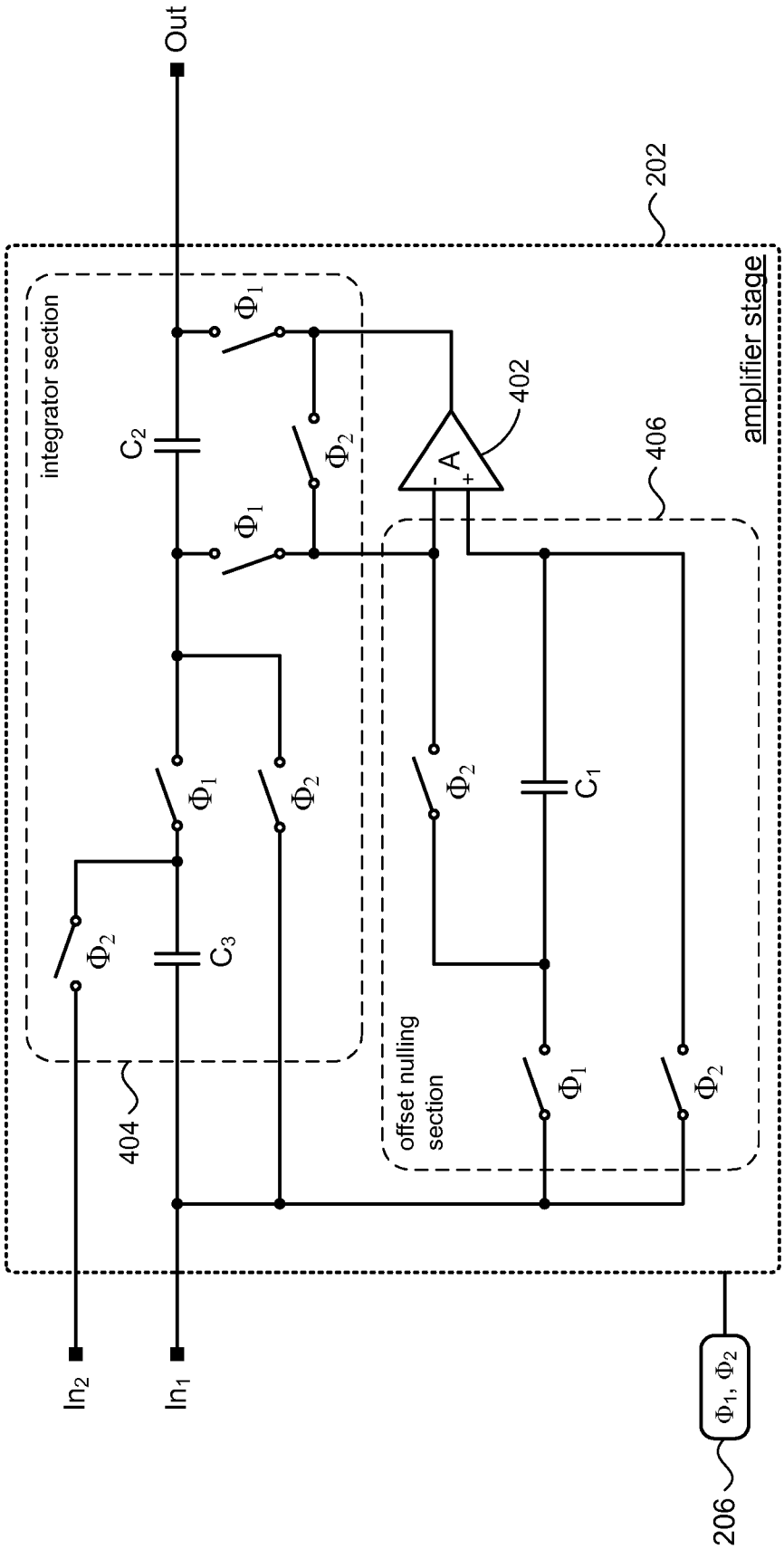
Out
202
integrator section
amplifier stage
Φ_1
Φ_2
C_2
402
A
406
C_3
C_1
404
offset nulling section
In_2
In_1
Φ_1, Φ_2
206

Fig. 4

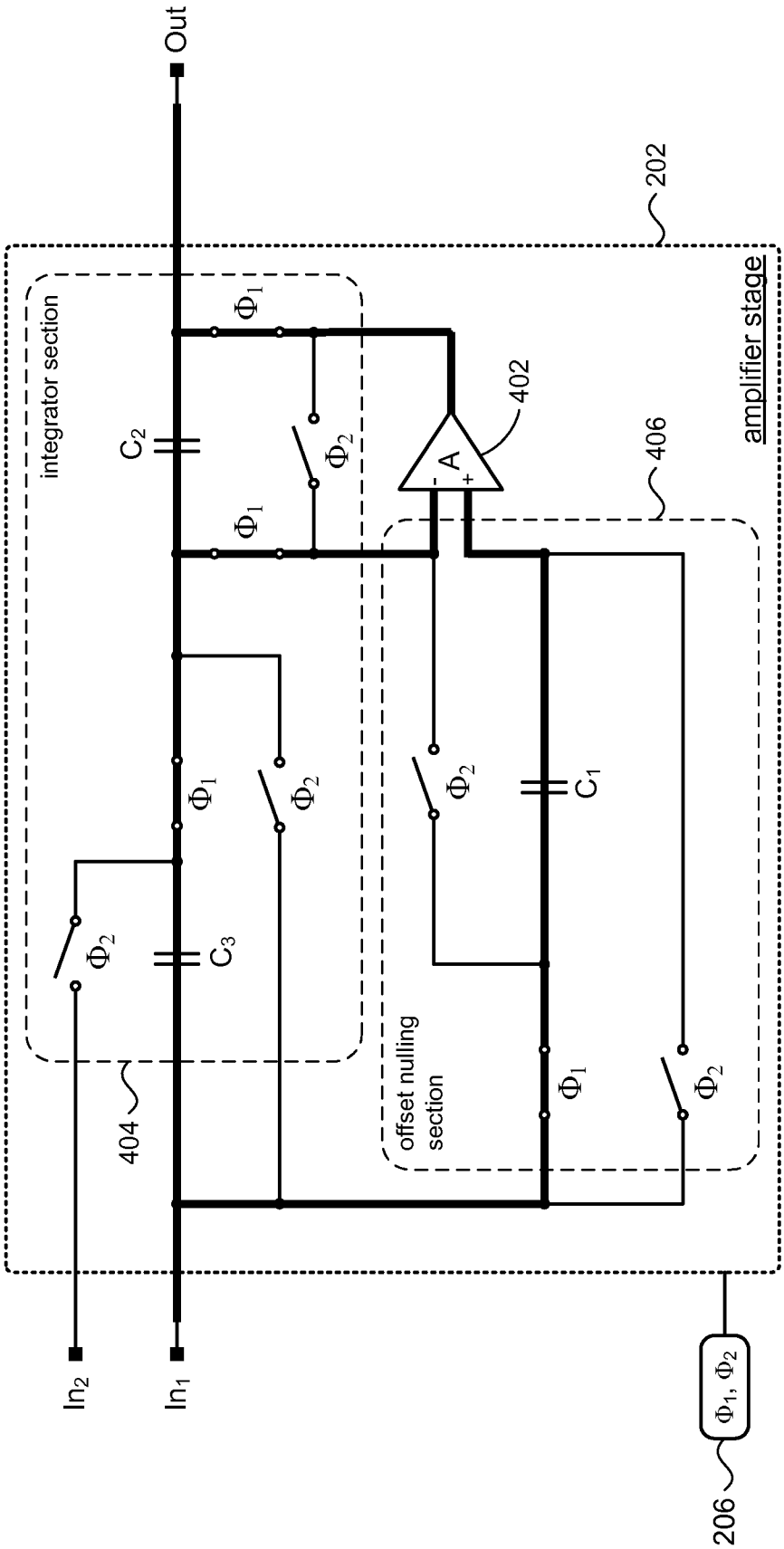
Out
202
amplifier stage
integrator section
Φ_1
Φ_2
C_2
402
A
406
C_1
C_3
offset nulling section
404
In_2
In_1
Φ_1, Φ_2
206

Fig. 4A

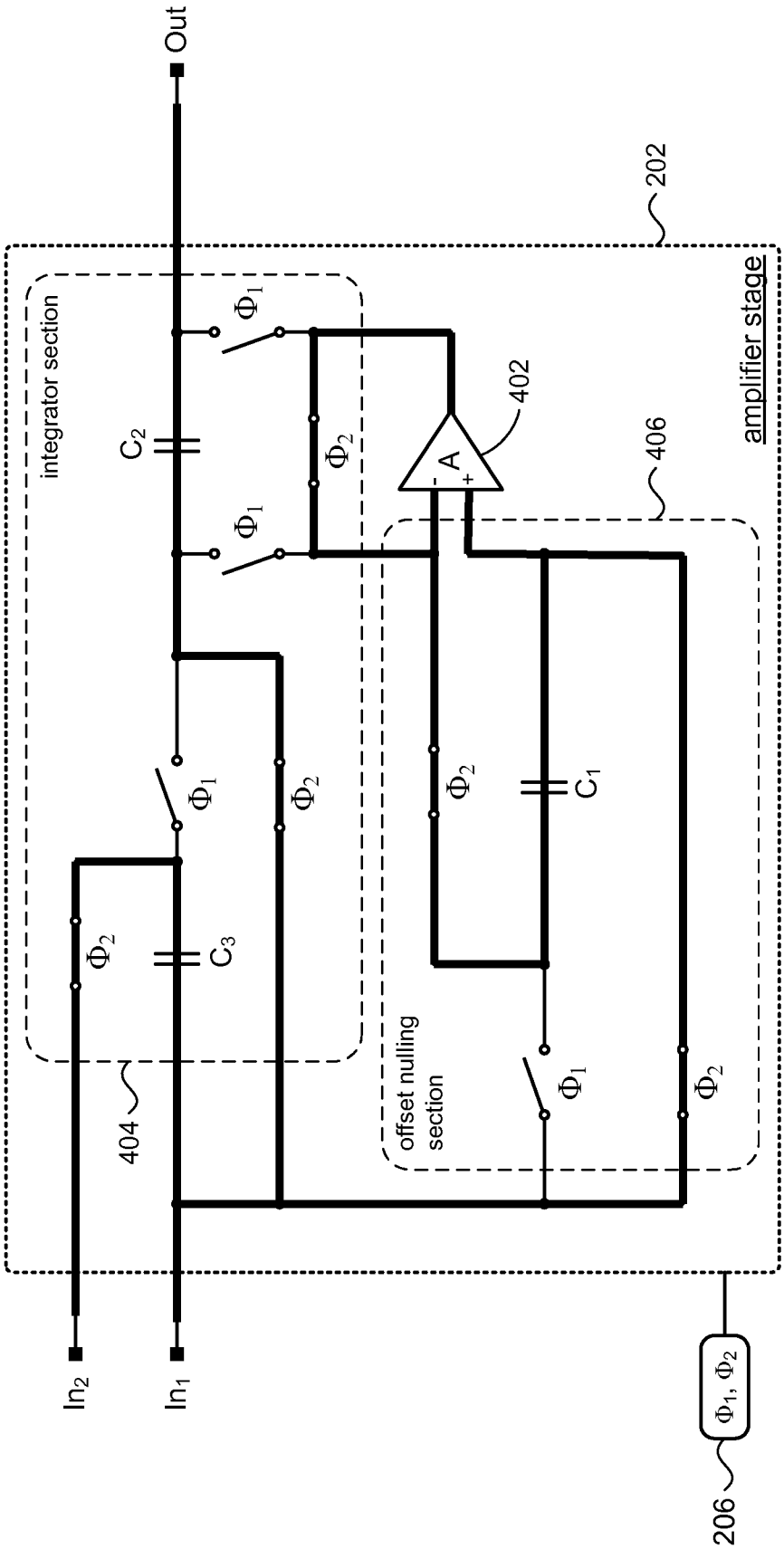
Out
202
amplifier stage
integrator section
Φ_1
C_2
Φ_2
402
A
406
offset nulling section
C_1
C_3
404
In_2
In_1
Φ_1, Φ_2
206

Fig. 4B

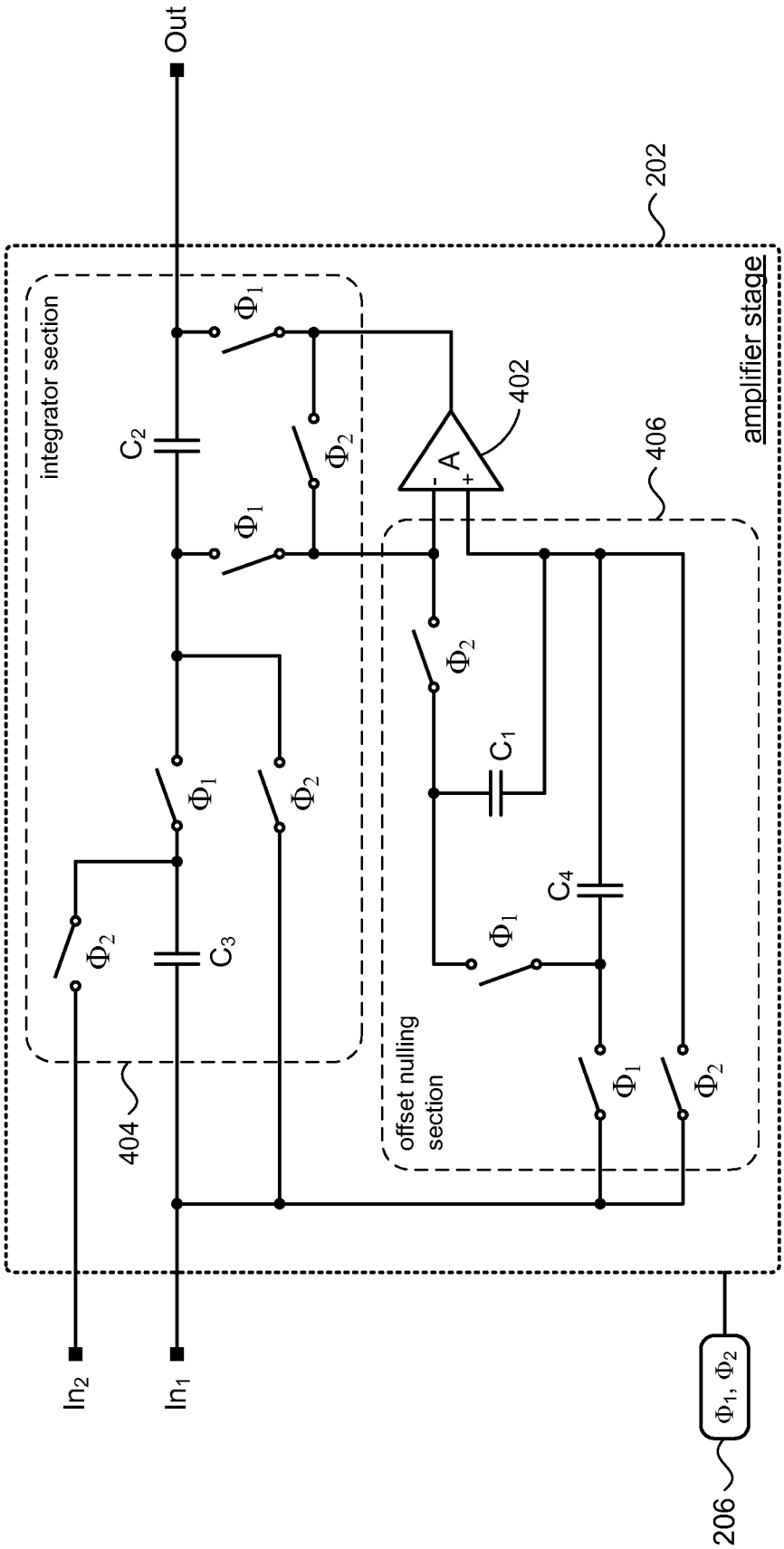
Out
202
amplifier stage
integrator section
Φ_1
Φ_2
C_2
402
A
406
C_1
C_3
C_4
offset nulling section
404
In_2
In_1
Φ_1, Φ_2
206

Fig. 5

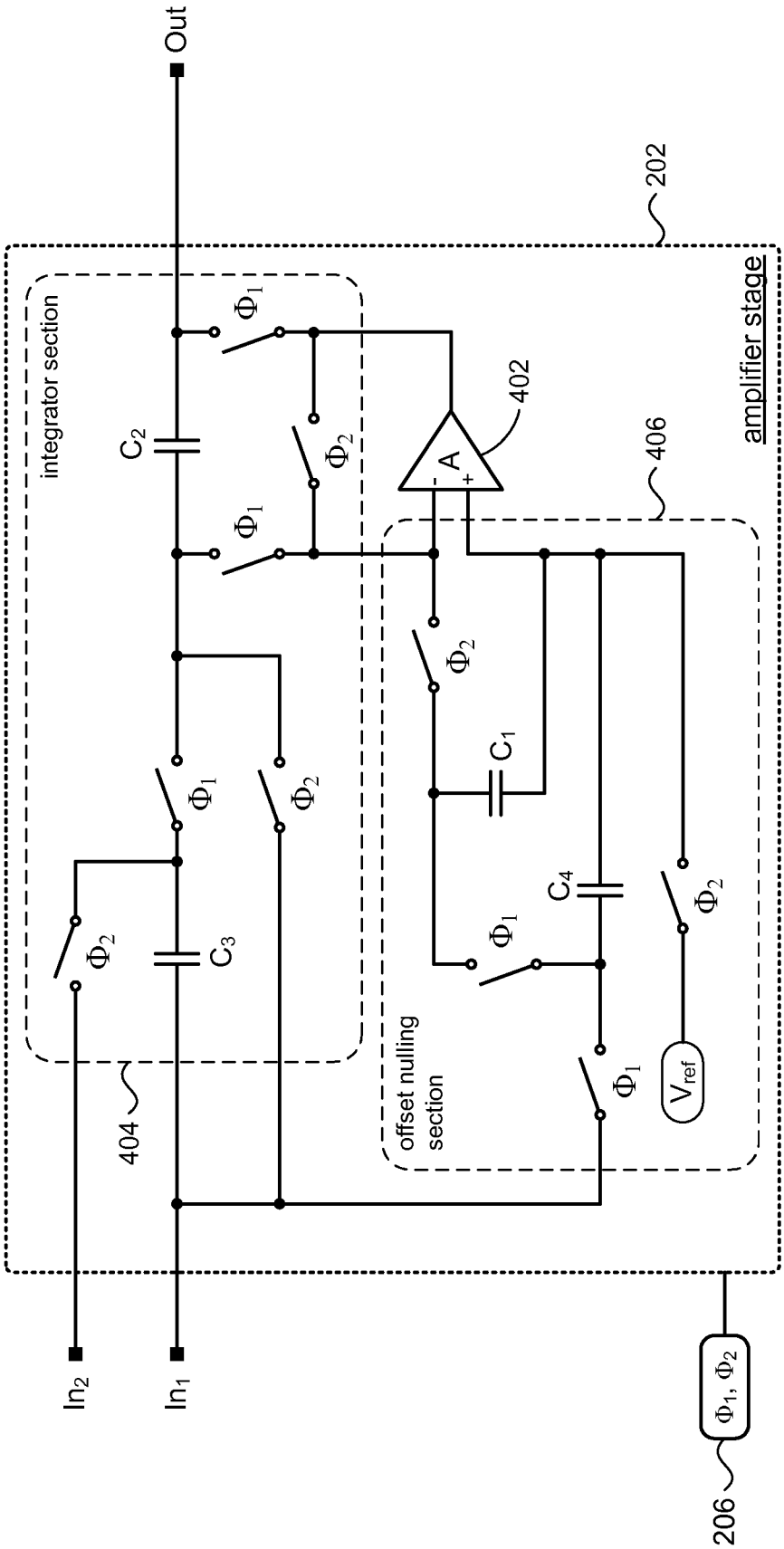
Out
202
amplifier stage
integrator section
Φ_1
Φ_2
C_2
402
A
406
C_1
C_3
C_4
V_{ref}
offset nulling section
404
In_2
In_1
Φ_1, Φ_2
206

Fig. 6

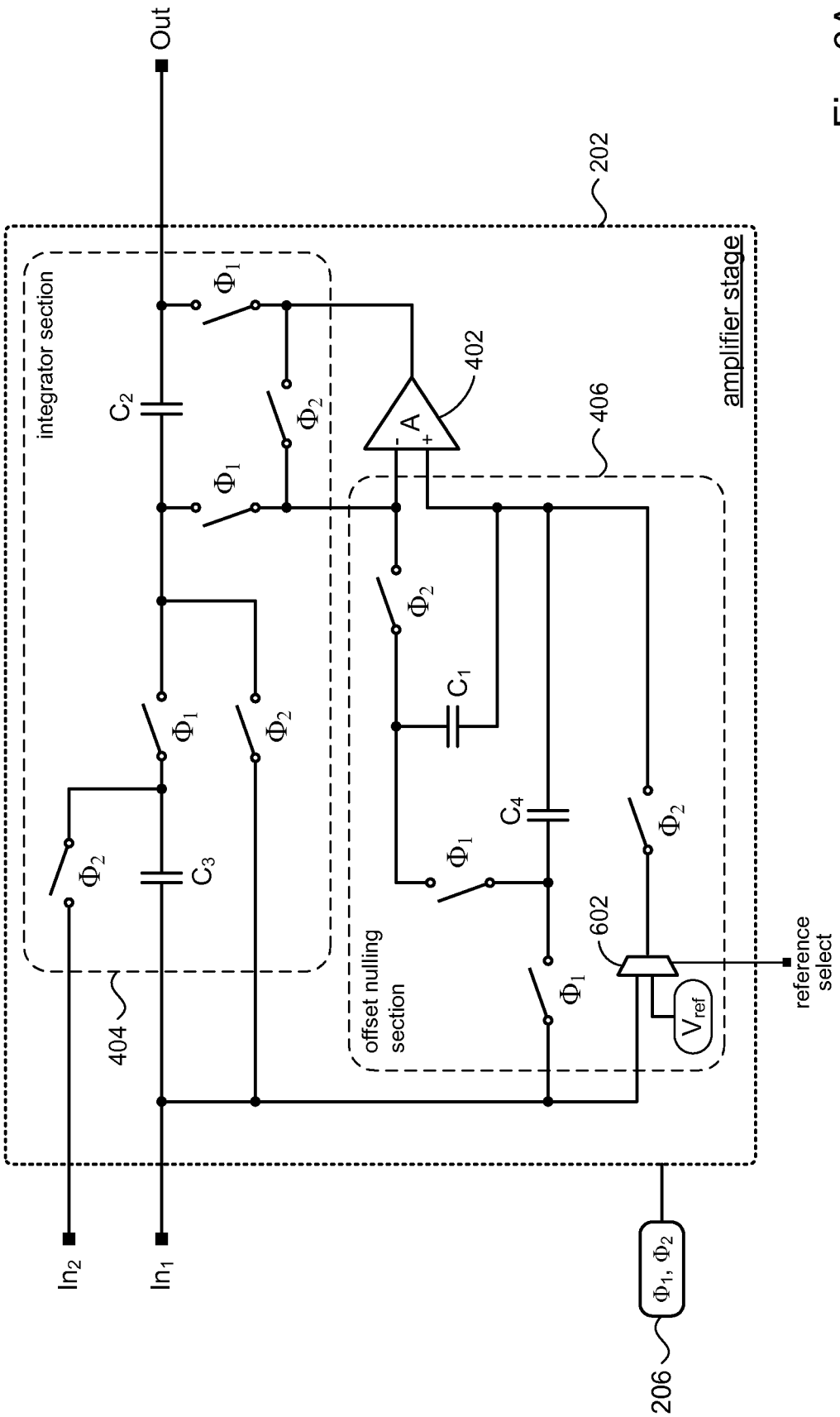
Out
202
amplifier stage
integrator section
offset nulling section
402
406
404
602
reference select
V_{ref}
C_1
C_2
C_3
C_4
Φ_1
Φ_2
Φ_1, Φ_2
206
In_1
In_2

Fig. 6A

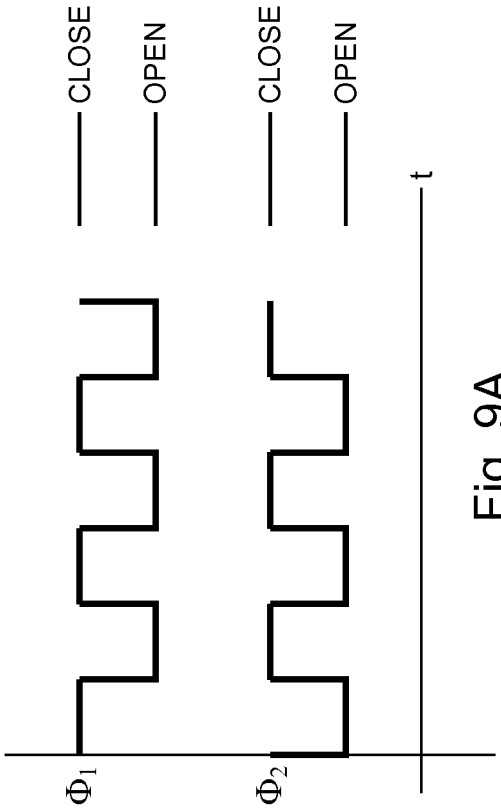

Fig. 9A

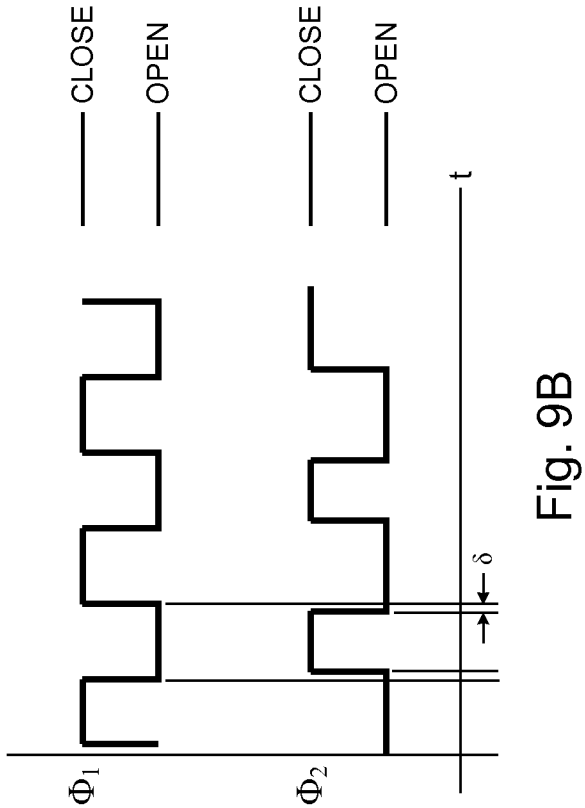

Fig. 9B

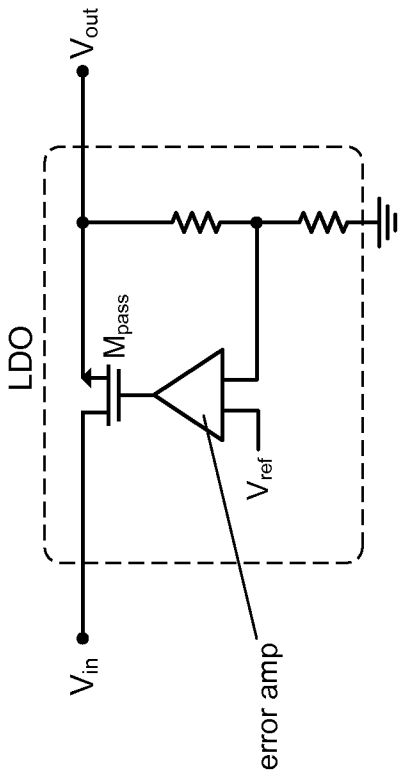

Fig. 7

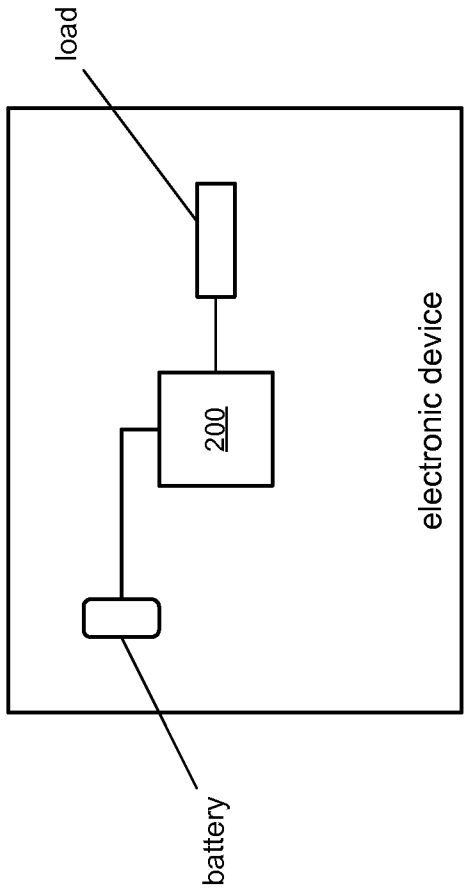

Fig. 8

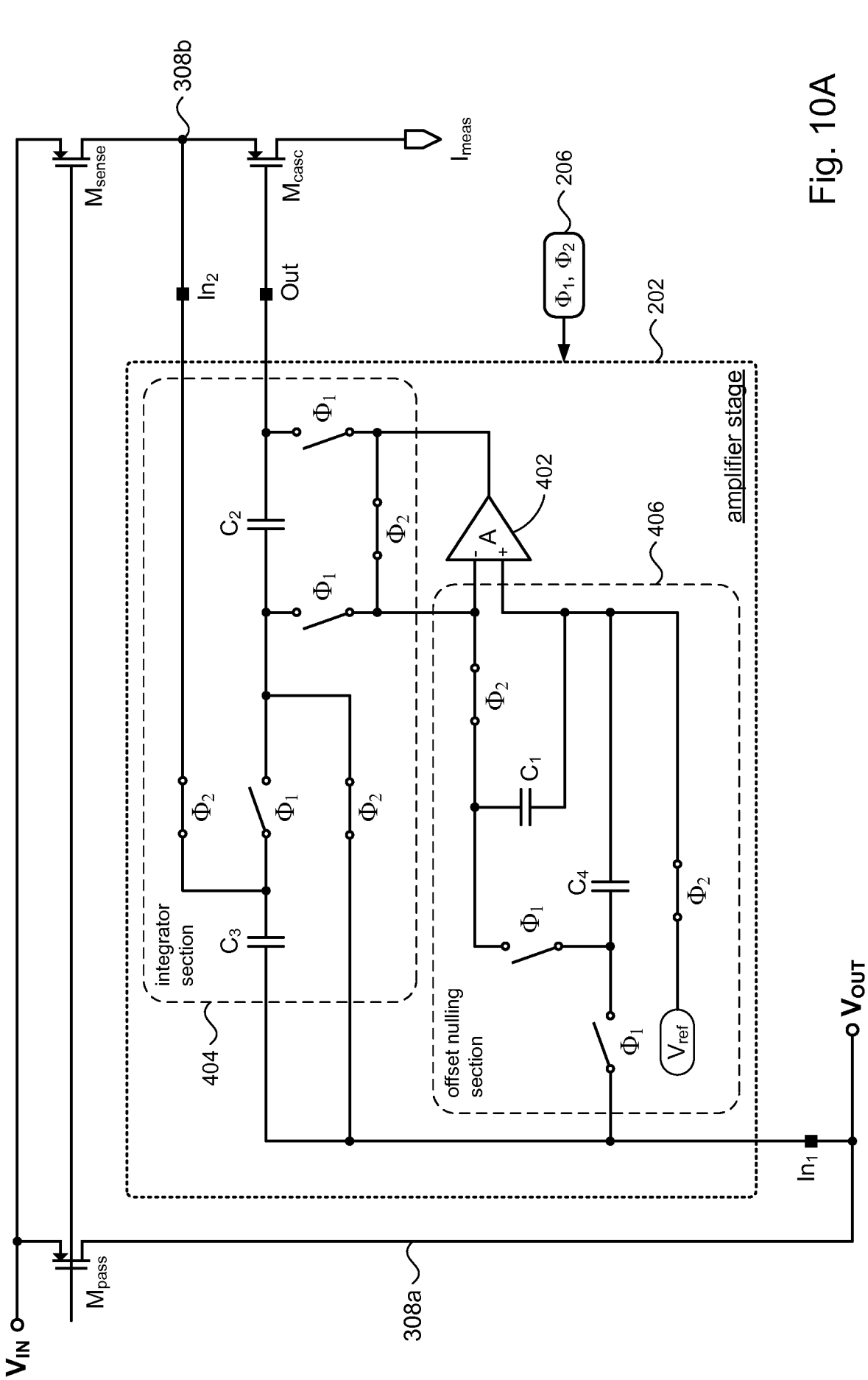
300
308b
M_{sense}
M_{casc}
I_{meas}
206
Φ_1, Φ_2
202
In_2
Out
amplifier stage
Φ_1
C_2
Φ_2
402
A
406
integrator section
C_3
404
offset nulling section
C_1
C_4
V_{ref}
In_1
V_{OUT}
V_{IN}
M_{pass}
308a

Fig. 10A

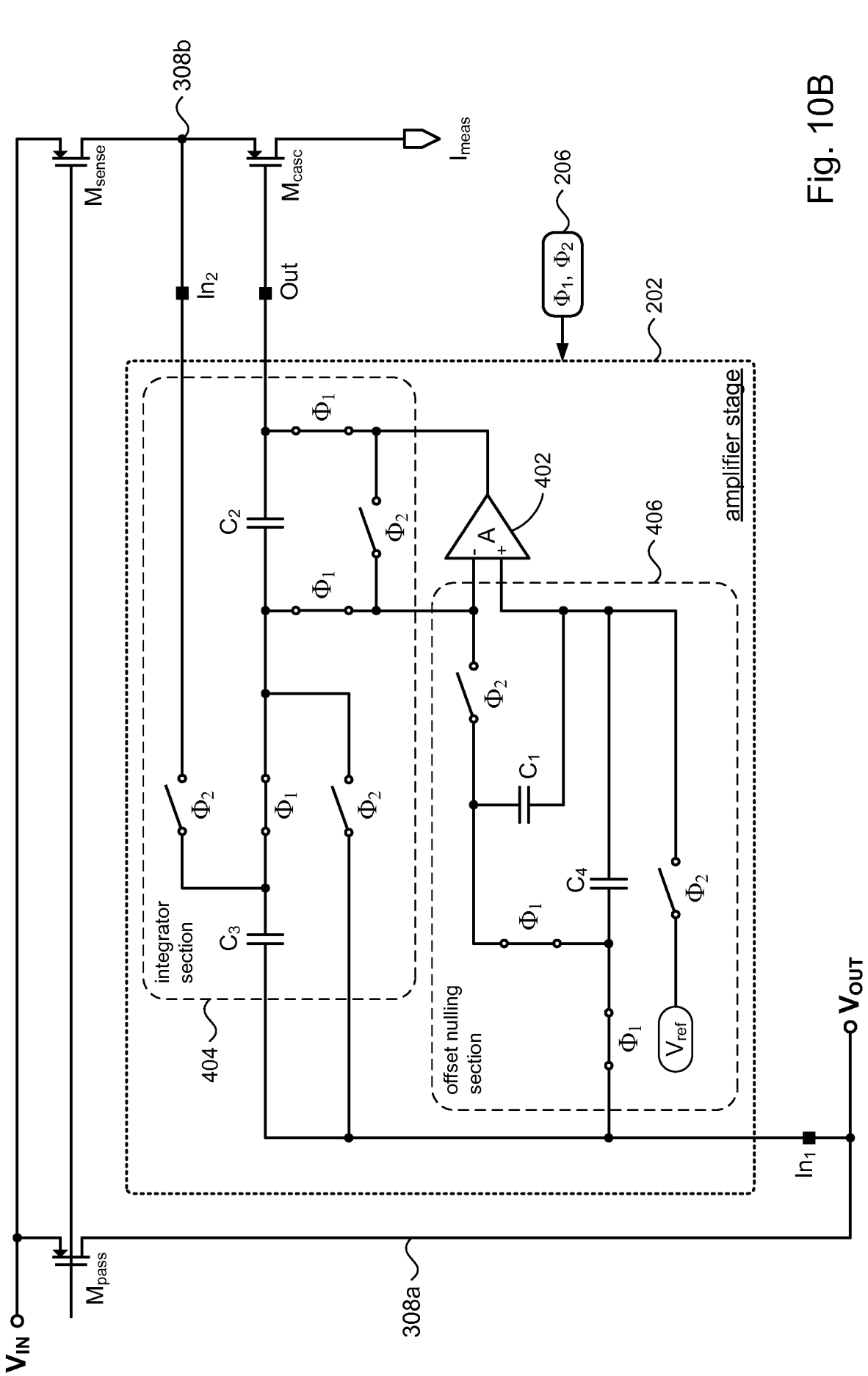
300
308b
M_{sense}
M_{casc}
I_{meas}
206
Φ_1, Φ_2
202
In_2
Out
amplifier stage
Φ_1
C_2
Φ_2
402
A
406
integrator section
C_3
404
offset nulling section
C_1
C_4
V_{ref}
In_1
V_{OUT}
V_{IN}
M_{pass}
308a

Fig. 10B

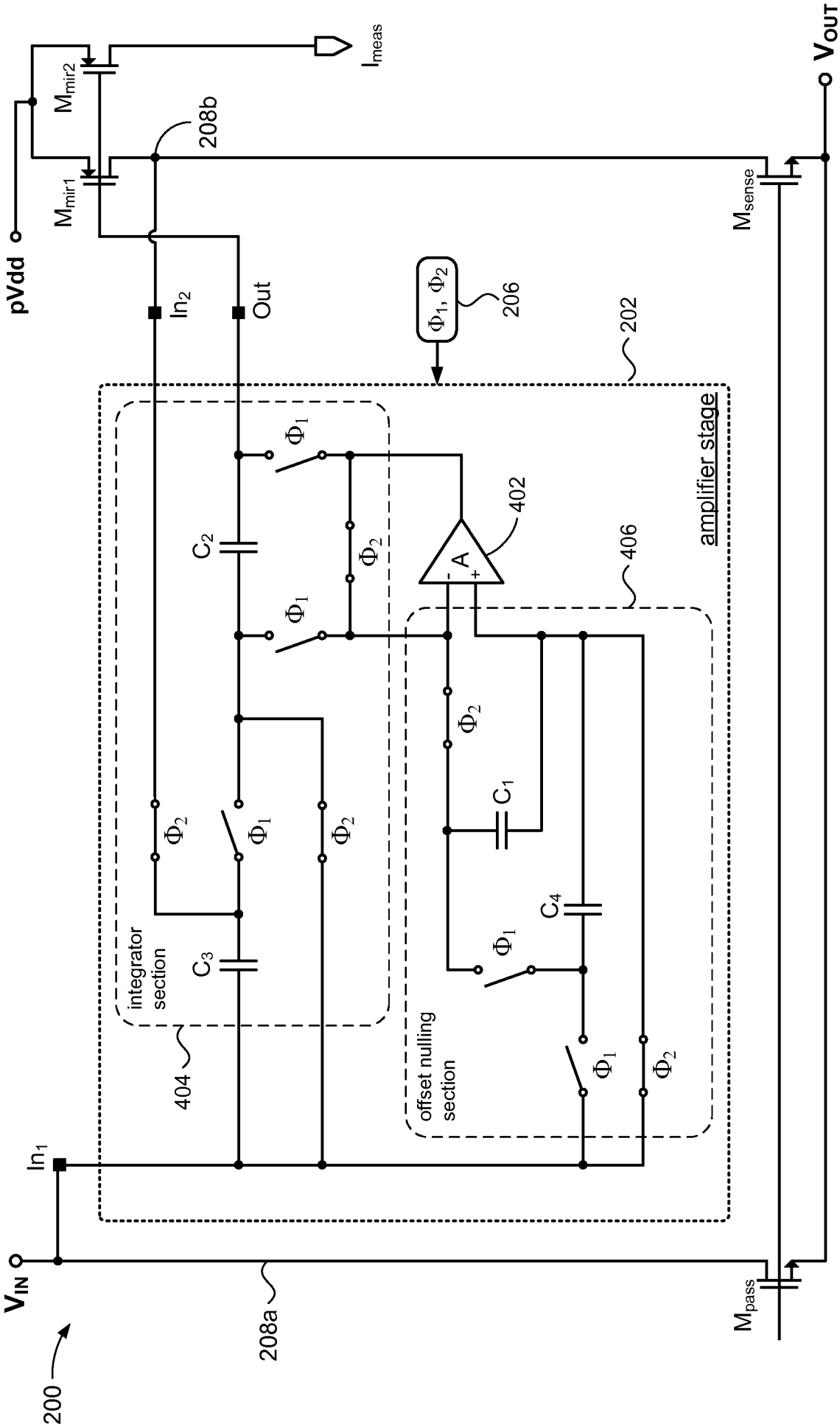
pVdd
M_{mir2}
M_{mir1}
I_{meas}
208b
V_{OUT}
M_{sense}
In_2
Out
Φ_1, Φ_2
206
202
amplifier stage
Φ_1
C_2
Φ_2
Φ_1
402
A
406
Φ_2
C_1
C_4
Φ_1
Φ_2
Φ_1
Φ_2
C_3
integrator section
404
offset nulling section
Φ_1
Φ_2
In_1
V_{IN}
208a
M_{pass}
200

Fig. 11A

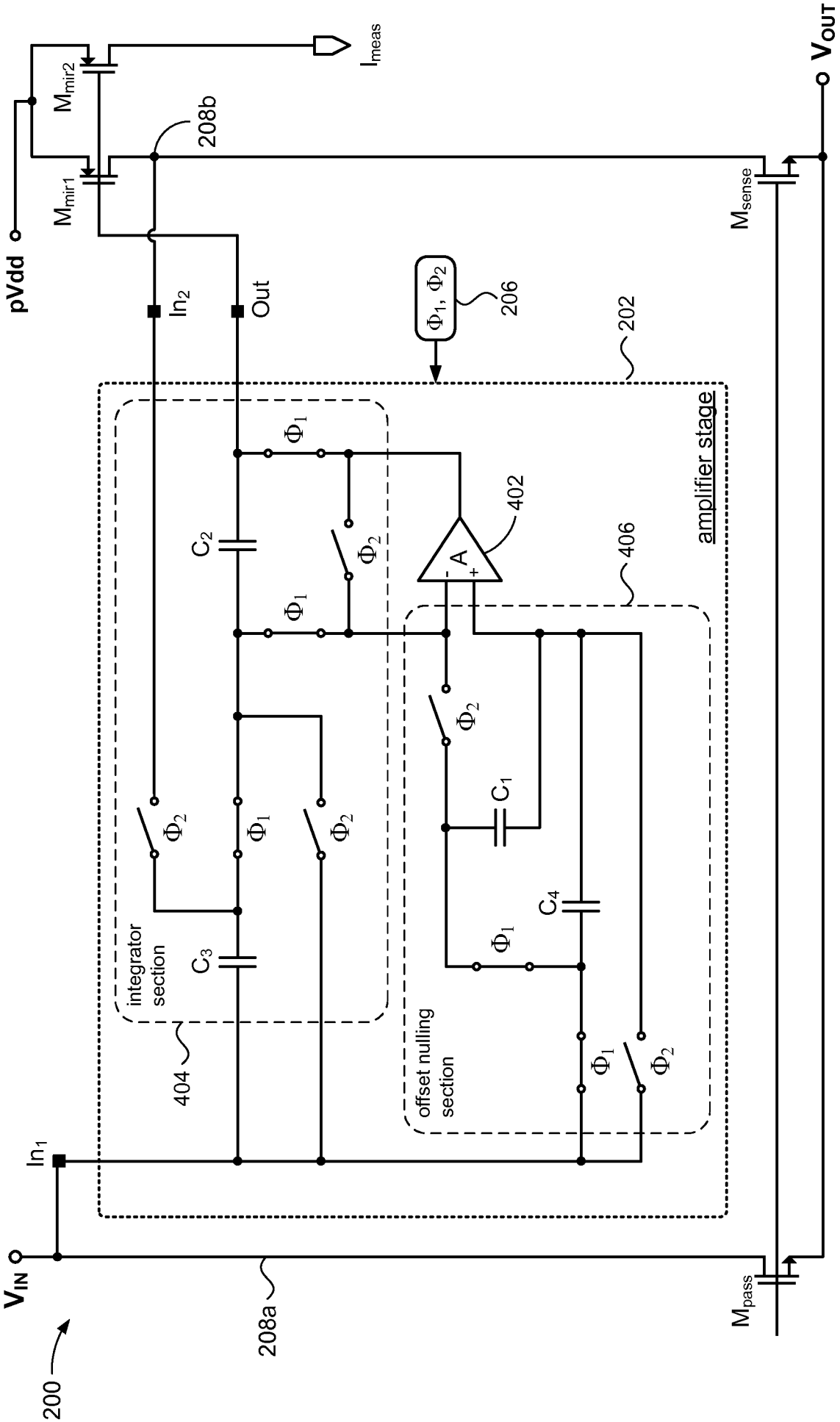
pVdd
M_{mir2}
M_{mir1}
I_{meas}
208b
V_{OUT}
M_{sense}
In_2
Out
Φ_1, Φ_2
206
202
amplifier stage
Φ_1
C_2
Φ_2
402
A
406
integrator section
C_3
404
offset nulling section
C_1
C_4
In_1
V_{IN}
208a
200
M_{pass}

Fig. 11B

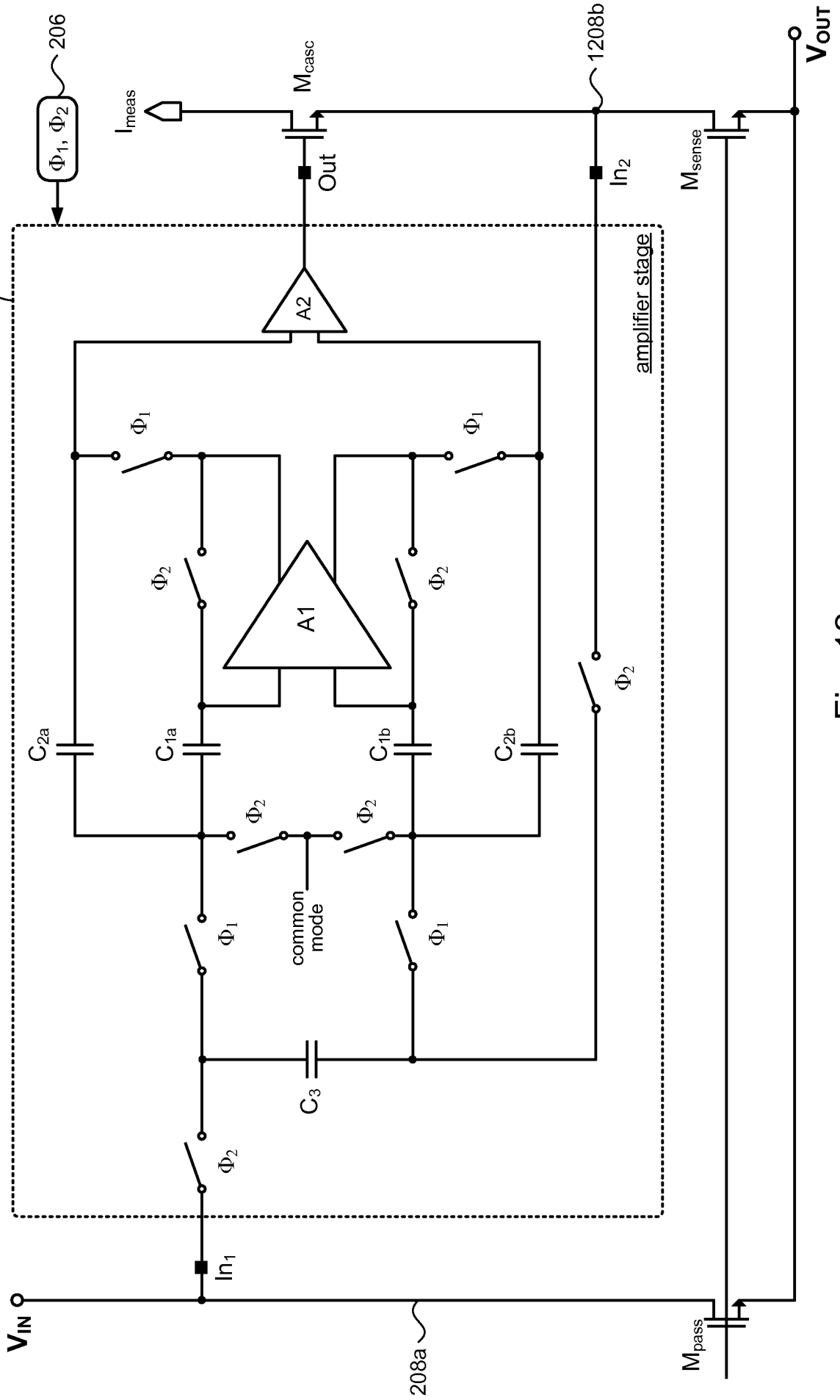
206
Φ1, Φ2
Imeas
Mcasc
1208b
VOUT
1202
Out
In2
Msense
amplifier stage
A2
Φ1
Φ2
A1
C2a
C1a
C1b
C2b
common mode
C3
In1
VIN
1208a
Mpass

Fig. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/038126

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LIN J ET AL: "Offset-compensated area-efficient switched-capacitor sum-gain amplifier", PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCS). CHICAGO, MAY 3 - 6, 1993; [PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCS)], NEW YORK, IEEE, US, vol. -, 3 May 1993 (1993-05-03), pages 1026-1029, XP010115276, DOI: 10.1109/ISCAS.1993.393899 ISBN: 978-0-7803-1281-4 figure 2 ----- -/--	1-17,26

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 September 2015	21/10/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kurzbauer, Werner

1

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	XIAOJING SHI ET AL: "Gain- and offset-compensated non-inverting SC circuits", CIRCUITS AND SYSTEMS, 2000. PROCEEDINGS. ISCAS 2000 GENEVA. THE 2000 I EEE INTERNATIONAL SYMPOSIUM ON MAY 28-31, 2000, PISCATAWAY, NJ, USA,IEEE, vol. 2, 28 May 2000 (2000-05-28), pages 425-428, XP010502751, ISBN: 978-0-7803-5482-1 figure 3	1-26
A	RADEV N A ET AL: "Comparative analysis of two gain- and offset compensated very large time constant switched-capacitor integrators", MICROELECTRONICS, 2000. ICM 2000. PROCEEDINGS OF THE 12TH INTERNATIONA L CONFERENCE ON OCT. 31 - NOV. 2, 2000, PISCATAWAY, NJ, USA,IEEE, 31 October 2000 (2000-10-31), pages 51-54, XP010538939, ISBN: 978-964-360-057-0 the whole document	1-26
A	HIROKAZU YOSHIZAWA ET AL: "Switched-Capacitor Track-and-Hold Amplifiers With Low Sensitivity to Op-Amp Imperfections", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I: REGULAR PAPERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 54, no. 1, 1 January 2007 (2007-01-01), pages 193-199, XP011155732, ISSN: 1057-7122, DOI: 10.1109/TCSI.2006.887454 the whole document	1-26
A	JP 2005 020291 A (TOYOTA MOTOR CORP) 20 January 2005 (2005-01-20) abstract	1-26
A	US 7 321 260 B2 (LARSON MARK R [US]) 22 January 2008 (2008-01-22) figure 1A	1-26

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/038126

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-26

A circuit comprising first and second circuit inputs; a circuit output; an amplifier having an output, the output having a first and second configuration

1.1. claims: 1-9, 26

A circuit comprising first and second circuit inputs; a circuit output; a first capacitor; a second capacitor connected to the circuit output; an amplifier having first and second amplifier inputs and an amplifier output; and a plurality of switches operable to be in a first configuration and operable to be in a second configuration, wherein, in the first configuration of the switches the amplifier output is disconnected from the circuit output; the first capacitor is connected across the amplifier inputs to sense a DC offset of the amplifier; and the second capacitor is connected only between the circuit output and one of the circuit inputs, wherein, in the second configuration of the switches the amplifier output is connected to the circuit output; the first capacitor is connected to one of the amplifier inputs to compensate for the DC offset of the amplifier; and the second capacitor is connected to the amplifier in a feedback loop.

1.2. claims: 10-17

A circuit comprising first and second circuit inputs; a circuit output; an amplifier having an output, the output having a first configuration that is not connected to the circuit output and a second configuration that is connected to the circuit output; an output capacitor that is connected to the circuit output, the output capacitor having a first configuration that is connected to the amplifier in a feedback loop and a second configuration that is not connected to the amplifier; an input capacitor that is connected to the first circuit input, the input capacitor having a first configuration that is connected to the amplifier in a feedback loop with the output capacitor and a second configuration that is connected to only the second circuit input; and a first offset capacitor having a first configuration that is connected to first and second inputs of the amplifier and having a second configuration that is connected in series with the input capacitor at a time when the input capacitor is connected to the amplifier in the feedback loop with the output capacitor.

1.3. claims: 18-25

A circuit comprising:a pass transistor having an output terminal connectable to a load; a sense transistor connected

to the pass transistor to mirror a current flow through the pass transistor; an output stage connected to the sense transistor; and an amplifier circuit having a first circuit input connected to the pass transistor, a second circuit input connected to the sense transistor, and a circuit output connected to the output stage, the amplifier circuit comprising:an amplifier section having an output that is selectively connectable to and disconnectable from the circuit output; an integrator section connected to the circuit output and selectively connectable to and disconnectable from the amplifier section; and an offset nulling section connected to the amplifier section, wherein the amplifier section is disconnected from the circuit output at a time when the offset nulling section is sampling an offset of the amplifier, wherein the integrator section provides an output to the circuit output to drive the output stage at a time when the amplifier section is disconnected from the circuit output.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/038126

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2005020291 A	20-01-2005	NONE	
US 7321260 B2	22-01-2008	EP 1992067 A1	19-11-2008
		JP 2009529288 A	13-08-2009
		US 2007222505 A1	27-09-2007
		WO 2007102863 A1	13-09-2007