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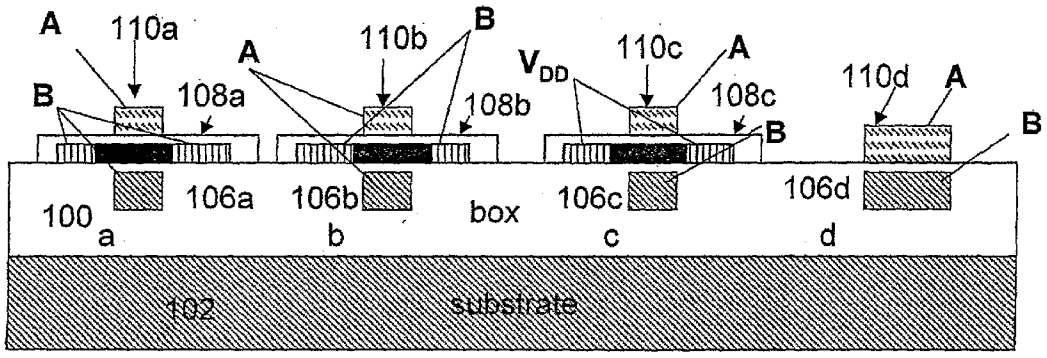
(54) **Title:** HIGH PERFORMANCE CAPACITORS IN PLANAR BACK GATES CMOS



(57) **Abstract:** A method of manufacture and device for a dual-gate CMOS structure. The structure includes a first plate (106a-d) in an insulating layer (100) and a second plate (110a-d) above the insulating layer electrically corresponding to the first plate. An isolation structure (108a-d) is between the first plate and the second plate.

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HIGH PERFORMANCE CAPACITORS IN PLANAR BACK GATES CMOS

TECHNICAL FIELD

The invention relates to semiconductor devices, and more particularly to ultra-thin SOI based dual-gate CMOS capacitors and method of manufacture.

BACKGROUND ART

A conventional MOS (metal-oxide semiconductor) capacitor can be modeled as a parallel plate capacitor. In this type of structure, one plate may be made from a metal or a heavily-doped polycrystalline silicon ("poly") and one plate may be made from a semiconductor (e.g., the inversion layer formed when the MOS capacitor is under high forward bias). An insulator such as SiO_2 or "oxide", for example, may be used to separate the two plates. In deeply scaled ultra-thin SOI (silicon on insulator) devices, the insulation layer, e.g., oxide, beneath the source and drain regions, is made thinner to improve MOS transistor performance. Although this results in a faster transistor, the thinner channel region and dopant solid solubility limits the amount of active dopants that can be placed in the channel. This results in the effective series resistance becoming quite large in the capacitor. This may pose many problems from a circuit standpoint.

More specifically, in ultra-thin SOI MOS devices, the n-channel FET of the nMOS transistor is made of p-type silicon, and the p-channel FET of the pMOS transistor is made of n-type silicon. Heavily-doped source and drain regions provide electrodes to contact the previously mentioned channel region. In an SOI MOS device, an oxide region is created beneath the channel. The oxide region electrically isolates the source, drain, and channel regions of device from the substrate. The MOS threshold voltage of the channel, i.e., the gate potential when charge carriers can flow through the channel from the source to the drain in significant quantities, is determined by factors such as the work function of the gate, any channel dopants, and the dimensions of the transistor structure. However, low mobile channel charge in a SOI MOS device can under certain conditions have large effective resistance (equivalent serial resistance (ESR)). This large ESR has a great influence on the performance of the capacitor. For example, an increase in the effective resistance of the capacitor will result in worsening frequency characteristics of the capacitor.

A more detailed model of the MOS structure decomposes the vertical gate-dielectric-substrate gate "stack" into two capacitors in series, e.g., a linear oxide capacitance and a nonlinear channel capacitance. By way of example, if the voltage on the gate is strongly negative on an N-type MOS structure, holes are attracted to the dielectric-substrate interface and accumulate there. In the accumulation regime, MOS capacitors act approximately as linear capacitors. On the other hand, if the gate voltage is made positive on

an N-type MOS structure, the surface is depleted of mobile holes, creating a depleted region with exposed dopant ions. The depletion capacitance is nonlinear due to the approximately square root dependence of the depletion charge on potential under the gate dielectric. But, as the gate voltage is raised further, the potential barrier between the source terminal and the channel is lower electrostatically and the channel is flooded with mobile electrons from the source. It is the presence of electrons in channel that indicates the inversion of the silicon near the surface, e.g., an NFET channel becomes n-type and analogously a PFET channel becomes p-type.

In the ultra-thin SOI devices, the depth of the silicon region beneath the gate stack is made very thin due to transistor scaling rules, where the bottom of the silicon region beneath the gate is bounded by the buried oxide. Even at channel doping levels near the solid solubility limit, the depletion region induced by the gate can extend from the gate to the back oxide creating a region that is depleted of mobile carriers, (i.e., "fully depleted").

Weak inversion results when the number of mobile electrons (the inversion charge) is much lower than the number of exposed dopant ions in the depletion region (the depletion charge). On the other hand, strong inversion results when the inversion charge greatly exceeds the depletion charge. Also, the transition between strong inversion to moderate inversion can be defined as the condition when the inversion charge and the depletion charge are comparable. When the channel area under the gate is strongly inverted, the gate

charge is balanced out primarily by the inversion layer charge. The voltage at which inversion layer charge dominates is called the threshold voltage Vt and Vt_0 indicates the threshold voltage when the source voltage equals zero.

In SOI MOS technologies, there are several modes of operation depending on the application of an external bias to the SOI channel region (also referred to as the silicon body). The silicon body is isolated from the substrate by the buried back oxide. This case, the floating body case, the potential in the body is controlled by many physical factors including diode junction currents from the source and drain, impact ionization near the drain, gate leakage, bipolar effects, and capacitive coupling to the device's electrical terminals the gate, source, drain, and body. An SOI body potential can be defined relative to the source potential and the body potential can be significantly forward-biased with respect to the source potential during normal operation. If an external potential is applied to the SOI body (called a body contact), the body potential is constrained by the external potential and the resistance between the external body contact and the SOI body. Note however that in the case of an ultra-thin SOI device with a silicon body that has been scaled to the point where it is fully-depleted, the external resistance can be so high that the body contact is ineffective.

An extension of the ultra-thin SOI MOS device described above is the dual-gate SOI MOS transistor. In this structure, the back oxide have been thinned to the point that the region below the back

oxide can exert non-negligible electrical field on the body and possibly form for an inversion layer or accumulation layer adjacent to the back oxide. When a second gate electrode is placed in or beneath the back oxide, a dual-gate device SOI MOS transistor is formed. Furthermore the second gate electrode (the back gate) is typically isolated from other electrically conductive elements such as the substrate, source, drain, and top gate (front gate).

In conventional MOS process technologies such as SOI or bulk (non-SOI) intentional capacitor circuit elements can be created without significant extra process steps by using a regular MOS transistor that is biased in the inversion or accumulation regime. This gives a relative constant high value capacitor due to the usage of the regular MOS gate oxide. These capacitors can function as decoupling capacitors or as reactive elements in analog applications. However in dual gate ultra-thin SOI the intentional capacitive element formed in this manner can contain parasitic resistance that is dominated by the fully-depleted body in some ranges of operation, reducing it usefulness as a circuit design element. However, traditional and leading-edge circuit design techniques still have a need for intentional capacitive elements, since dual-gate SOI has certain performance advantages over ultra-thin single gate SOI technologies Therefore it is desirable to introduce intentional capacitive circuit elements into dual-gate technologies that are low in parasitic resistance, have high capacitance, and are easy to fabricate.

DISCLOSURE OF INVENTION

In a first aspect of the invention, a method of manufacturing a dual-gate CMOS structure includes forming a first plate in an insulating layer and forming a second plate above the insulating layer electrically corresponding to the first plate. The method further includes providing an isolation structure between the first plate and the second plate.

In another aspect of the invention, the method of manufacturing a dual-gate CMOS structure includes forming at least one back plate in an insulating layer and forming at least one front plate above the insulating layer corresponding to the at least one back plate. The method further includes providing a dielectric between the at least one back plate and the front plate.

In yet another aspect of the invention, a capacitor formed on a substrate having a buried insulator layer and a device layer on the insulator layer comprises a lower plate formed in a buried insulator layer. A portion of the buried insulator layer is formed on the lower plate to provide a first capacitor dielectric. A portion of a device layer is formed on the first capacitor dielectric and a second capacitor dielectric is formed on the portion of the device layer. An upper plate is formed on the second capacitor dielectric.

In another aspect, the invention includes a dual-gate capacitor having at least one back gate formed in a buried insulator layer and at least one front gate formed above the buried insulator layer. A dielectric layer is formed between the at least one front gate

and back gate. Diffusion regions are doped adjacent to the at least one back gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates steps in manufacturing a device in accordance with the invention;

Figure 2 illustrates additional steps in manufacturing the device in accordance with the invention;

Figure 3 illustrates additional steps in manufacturing the device in accordance with the invention;

Figure 4 illustrates additional steps in manufacturing the device in accordance with the invention;

Figure 5 illustrates additional steps in manufacturing the device in accordance with the invention;

Figures 6a-6d show top views or wiring schematics of the different structures of the invention, manufactured in accordance with the steps of the invention; and

Figure 7 shows a side view of the respective structures of Figures 6a-6d.

BEST MODE FOR CARRYING OUT THE INVENTION

The invention is directed to CMOS structures and more particularly to low resistance, high value capacitors in scaled dual-gate SOI and a method of manufacture. By using the dual-gate device and method of fabrication of the invention, ultra-thin SOI capacitors with enhanced functionality are achieved. By way of example, in one

application series resistance can be lowered for high frequency operations; whereas, in other applications, high capacitance can be achieved per unit area.

In accordance with the invention, four distinct CMOS capacitor structures may be manufactured simultaneously, if desired, based on scaled dual-gate SOI technology; namely, the initial structures may be formed with substantially the same processes, with different wiring structures to obtain desired results. In one application, two structures are designed to provide high capacitance directly between front and back gates with negligible reduction in series resistance. In another structure, for example, higher capacitance is provided with reduced series resistance by using both front and back gates electrically tied together, with the active silicon neither inverted or accumulated, thus providing a capacitive element vertically between the two plates and through the fully-depleted channel region.

Figure 1 shows a beginning structure in accordance with the invention. In this structure, an oxide or dielectric layer 100 may be formed on a substrate 102, using any conventional methods. One such conventional method may include wafer bonding, where another wafer (not shown) with the oxide layer 100 is bonded to the substrate by van der Waals forces. The substrate wafer 102 may be comprised of silicon, germanium, or other readily known materials, and is preferably approximately 500 microns in thickness for purposes of manufacturing processes. A thin layer of silicon 104 is provided on

the surface of the oxide layer 100. The silicon layer 104, in one embodiment, is approximately 50 Å to 400 Å thick, with other dimensions contemplated by the invention. Figure 1 displays all embodiments in close proximity however this is not a requirement for application and one or more embodiments can be placed in arbitrary locations around the chip area.

Prior to the bonding the layers 100, 102, one or more back gates 106a-106d (also known as plates) are formed in the oxide layer. It should be understood that each back gate 106a-106d may be used to form a similar or different capacitor, depending on the wiring structure desired for a particular application. For example, in the embodiment shown in Figure 1, the four back gates 106a-106d form structures in regions, a-d, respectively. Additionally, more or less than four back gates may also be formed, again depending on the desired application. Accordingly, it should be understood that the discussion of back gates 106a-106d are exemplary and should not be considered a limiting feature of the invention.

In forming the back gates 106a-106d, process steps including conventional standard lithographic and etching processes may be utilized, all known to those of skill in the art. For example, the process may include block masks used in combination with Reactive Ion Etching (RIE), in certain applications. In implementation, the back gates 106a-106d may be polysilicon and conventionally doped, for example, using phosphorous, boron or arsenic. Also, in embodiments, the cross-section of the back gates 106a-106d are of

such dimensions so as to minimize any significant gate resistance. For example, the height of the back gates 106a-106d may be approximately 1000 Å to 2000 Å, although other critical dimensions are also contemplated by the invention. A space of approximately 10Å to 100Å is provided between the top surface of the oxide layer 100 and the back gates 106a-106d. This distance demarcates a region that can be referred to as the back gate oxide or dielectric layer, which can be sized to minimize any potential parasitic effects such as direct tunneling currents.

Figure 2 represents further processing steps in accordance with the invention. In Figure 2, the silicon layer 104 is etched away, using conventional processes. For example, Figure 2 is illustrative of an active area mask that is used to define each isolated capacitor element, which may include channel, drain, and source regions. In one application, the active area mask is placed over regions represented as "a", "b" and "c". The structure is then etched in a silicon isolation process, resulting in silicon bodies or islands 104a, 104b and 104c. The silicon layer 104 may be completely etched in the region "d".

Gate oxide or dielectric layers 108a, 108b, 108c are then thermally grown or deposited on the silicon bodies 104a, 104b, and 104c, respectively. In one embodiment, the gate oxide layers 108a, 108b, 108c are formed to a thickness of approximately 10 Å to 100 Å, similar to the spacing of the oxide layer 100 between the back gates 106a-106d and the silicon layer 104. This oxide layer may be used to form the actual capacitor(s) of the invention.

Figure 3 is representative of a gate material 110 (e.g., polysilicon) being deposited on the structure of Figure 2. This material 110 is used to form the front gates, using subsequent steps described below. The gate material 110 may be heavily doped (e.g., 10^{20} cm^{-3}) however not necessarily the same dopant species as was used with the back gates 106a-106b. High dopant levels of species such as phosphorous, boron or arsenic are used to minimize polysilicon depletion effects. The considerations for the dimensions of the polysilicon material 110 are also substantially the same as that of the back gates 106a-106c. For example, the cross section of the poly material 110 is of such dimensions so as to minimize any significant gate resistance, e.g., approximately 1000 Å to 2000 Å, although other critical dimensions are also contemplated by the invention.

Figure 4 is illustrative of an exemplary patterning and etching process in order to form the front gates 110a-110d. In one process, the formation of the front gate 110d of section "d" may be formed separately from that of the remaining front gates 110a-110c. This is due to the front gate 110d being etched more deeply since the silicon layer 104 and subsequent oxide layer is not provided over this region. In one example, a protecting mask may be placed over region "d" during the processes forming the front gates 110a-110c. Likewise, a protecting mask may be placed over regions "a", "b" and "c", during the formation of the front gate 110d. These processes are well known in the art to those of skill such that further discussion is not required herein for a complete understanding of the invention.

Figure 5 illustrates several processing steps including the formation of spacers, source and drain regions and silicide. In the illustration of Figure 5, only the CMOS structure for region "a" is shown; however, it should be understood that the processes discussed with reference to section "a" are equally applicable for the formation of the structures in regions "b", "c" and "d". Accordingly, the exemplary illustration of Figure 5 can be used for the formation of the source, drain, sidewalls and silicide formations on any of the structures shown in Figures 6a-7.

By way of example, referring to region "a", the source and drain regions 112_1 and 112_2, are formed in the silicon body in any conventional manner. An isolation region 105 is adjacent the source and drain regions 112_1 and 112_2. Spacers 114 are formed on the sidewalls of the front gate 110a and the front oxide layer 108a, extending to the doped source and drain regions 112_1 and 112_2, respectively. These regions can be doped using phosphorous, boron or arsenic, preferably resulting in the range of $1x\ 10^{20}$ particles/cm^3 for the source and drain, but typically lower levels for other doped regions such as halo or extension implants that may be part of the conventional transistor process into which the dual-gate MOS capacitor is being included. A silicide layer 116 is formed on the exposed silicon layer at the doped source and drain regions 112_1 and 112_2, respectively, in addition to a top surface of the front gate 110a. The formation of the silicide and spacers are well known in the art by those of skill in the art.

Figures 6a-6d show top views of wiring schematics of the different structures "a" through "d" described with reference to Figures 1-5. In Figure 6a, a dual-gate FET capacitor is shown, corresponding to the manufacturing processes described for section "a". In the FET capacitor of Figure 6a, a first wire "A" contacts the front gate 110a and forms a first terminal of the capacitor. A second wire "B" contacts the back gate106a, in addition to both opposing sides of the silicon layer, and forms the second terminal of the capacitor. Thus, in this structure, the capacitor is formed from the "A" electrode, through the structure to the "B" electrode, which results in the source and drain shorted together. Alternatively, the roles of the back gate and the front gate can be reversed, with the "B" electrode consisting of the back gate and the "A" terminal consisting to the diffusion regions tied to the front gate.

Figure 6b is a dual-gate capacitor using the structure formed in region "b" of Figures 1-5, with the wiring schematic shown herein. In the high-density capacitor of Figure 6b, a first wire "A" contacts both sides of the silicon layer diffusion regions and forms a first terminal of the capacitor. A second wire "B" contacts the front gate 110b and the back gate 106b and forms the second terminal of the capacitor. Thus, in this structure, the wire "A" ties together the two sides of the silicon , while the wire "B" ties together the front gate 110b and the back gate 106b . The device of Figure 6b provides increased capacitance as the device of Figure 6a due to the front and back channel charge regions functioning electrically together.

In the capacitor structure of Figures 6a and 6b, high capacitance is possible because of the thin dielectric layer (a process step that is potentially shared with the conventional MOS transistor process that includes these dual-gate capacitors) directly between the front and back gates 106a and 110a, respectively. Also, since the outer edges (diffusions) of the silicon are connected together by wire "B", the top portion of the structure looks similar to a conventional MOSFET. And, in this case, an inversion layer can be formed beneath the top oxide layer 108a. That is, the dual-gate structure also allows both devices to have an inversion channel forms under the oxide layer 108a.

Also, accumulation or diffusion effects can occur since the front gate is formed over the silicon and there are two diffusions wired out at an electrically different potential from the front gate. Thus, as should be understood by this wiring schematic, if the potential of the "B" wire goes above the front or back gate threshold voltage with respect to the diffusion, an inversion layer will form; whereas, if the potential of the wire "B" has low enough bias with respect to the diffusion potential, an accumulation layer will occur under one or both of the capacitor oxides. It is recognized that opposite biasing results occur in p-type and n-type devices.

Figure 6c is a dual-gate capacitor using the structure formed in region "c" of Figures 1-5, with the wiring schematic shown herein. In the wiring structure of Figure 6c, a first wire "A" contacts the front gate 110c and forms a first terminal of the capacitor. A

second wire "B" contacts the back gate106c and forms the second terminal of the capacitor. A high potential (for example Vdd) contacts both sides (diffusions) of the silicon layer. From an electrical standpoint, the thin-body structure of Figure 6c is fully-depleted and has field lines substantially penetrating the structure from "A" to "B", e.g., the front gate 110c to the back gate 106c. The dual-gate capacitor of Figure 6c offers low series resistance for high-frequency operation (similar to that of Figure 6d).

In the device of Figure 6c, an inversion layer cannot form because the potential on the gate does not exceed the potential of the diffusion. An inversion layer may form when the gate potential, relative to one of the outside diffusion potentials, is above a MOS FET threshold and there is a source of carriers around, which is the source and drain. But, this is not desirable due to resistance issues. This phenomenon is eliminated in the device of Figure 6c since the potential on the diffusions is high and the potentials on "A" and "B" are operated below that potential. Also, an accumulation can occur if the gate terminal goes too low; however, the assumption is that the device of Figure 6c is operated so that this does not occur since there is roughly 1.2 volts (or the bandgap potential) between the high diffusion potential and the bias where accumulation would occur.

Figure 6d is a gate capacitor using the structure formed in region "c" of Figures 1-5, with the wiring schematic shown herein. In the capacitor of Figure 6d, a first wire "A" contacts the front gate 110d and forms a first terminal of the capacitor. A second wire "B" contacts

the back gate106d and forms the second terminal of the capacitor. The device of Figure 6d offers low series resistance for high-frequency operations and high capacitance per unit area based on scaling of the back oxide thickness.

Figure 7 shows a side view of the respective structures of Figures 6a-6d. The first wire "A" and the second wire "B" are representative of the respective terminals of the devices shown in Figures 6a-6d. Figure 7 also clearly illustrates the regions "a", "b", "c" and "d" representative of the devices shown and described in Figures 6a-6d, respectively. In this illustration, two dielectric or oxide layers separate the front gates 110a-110c and the back gates 106a-106c. A contribution to parasitic resistance, direct tunneling through either the front or back gate is controlled by selecting the appropriate oxide thickness such that leakage current is minimized.

While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.

What is claimed is:

1. A method of manufacturing a dual-gate CMOS structure, comprising:

forming a first plate buried in an insulating layer;

forming a second plate above the insulating layer electrically corresponding to the first plate; and

providing an isolation structure between the first plate and the second plate.

2. The method of claim 1, wherein the isolation structure forms a first dielectric layer above the first plate.

3. The method of claim 1, further comprising doping the isolation structure to form diffusion regions between the first plate and the second plate.

4. The method of claim 1, wherein the isolation structure is approximately 50 Å to 400 Å thick.

5. The method of claim 3, wherein a height of either of the first plate and the second plate is approximately 1000 Å to 2000 Å.

6. The method of claim 3, wherein the isolation structure includes a dielectric layer and a silicon island and the

insulating layer forms a back plate insulating structure between the first plate and the silicon island.

7. The method of claim 6, wherein the dielectric layer is thermally grown on the silicon island.

8. The method of claim 6, wherein the dielectric layer and the back plate insulating structure are each approximately 10 Å to 100 Å thick.

9. The method of claim 6, further comprising:

forming a first terminal connected to the first plate and to opposing sides of the silicon island using diffusion regions formed on the silicon island; and

forming a second terminal connected to the second plate.

10. The method of claim 6, further comprising:

forming a first terminal connected to opposing sides of the silicon island at diffusions regions; and

forming a second terminal connected to the first plate and the second plate.

11. The method of claim 6, further comprising:

forming a first terminal connected to the silicon island;

forming a second terminal connected to the first plate; and

forming a third terminal connected to the second plate; and

providing a higher potential to the first terminal than the second terminal or the third terminal.

12. The method of claim 6, wherein the isolation structure is formed from a silicon layer which is entirely etched away between the first plate and the second plate such that the second plate is formed directly on the insulating layer and further comprising:

forming a first terminal connected to the first plate; and

forming a second terminal connected to the second plate.

13. The method of claim 1, further comprising

providing capacitance directly between the first plate and the second when the silicon body between the plates is fully-depleted.

14. The method of claim 1, further comprising:

forming an inversion layer beneath a top portion of the insulating layers when a potential of a wire shorting between diffusion regions formed on the isolation structure with respect to one diffusion region of the diffusion regions causes channel inversion; and

forming an accumulation layer beneath the top portion of the insulating layers when the potential of the wire is high with respect to the one diffusion region.

15. The method of claim 1, further comprising:

forming at least another plate in the insulating layer;

forming at least another plate above the insulating layer corresponding to the at least another plate in the insulating layer; and providing an isolation island and dielectric structure between the at least another plate in the insulating layer and above the insulating layer.

16. A method of manufacturing a dual-gate CMOS structure, comprising:

forming at least one back plate in an insulating layer;

forming at least one front plate above the insulating layer corresponding to the at least one back plate; and

providing a dielectric structure between the at least one back plate and the front plate.

17. The method of claim 16, wherein the dielectric structure is a back gate dielectric layer and a front gate dielectric layer, the front gate dielectric formed between a silicon based island and the at least one front plate.

18. The method of claim 17, further comprising doping an isolation island formed in the dielectric structure to form diffusion regions.

19. The method of claim 16, further comprising:

forming a silicon layer in the dielectric structure between the at least one back plate and the front plate;

etching portions of the silicon layer to form isolated islands corresponding to the at least one back plate and the at least one front plate; and

doping portions of the isolated islands to form diffusion regions,

wherein the dielectric structure is a back gate dielectric layer provided between the back plate and the isolated islands, and a front gate dielectric formed between the isolated islands and the front plate.

20. The method of claim 16, further comprising doping diffusion regions associated with the at least one back plate and front plate.

21. The method of claim 20, wherein the dielectric structure is a front plate dielectric and a back plate dielectric separated by diffusion regions.

22. The method of claim 21, further comprising:

forming a first terminal connected to the back plate and opposing sides of the diffusion regions to short the diffusion regions; and

forming a second terminal connected to the front plate.

23. The method of claim 21, further comprising:

forming a first terminal connected to the diffusions regions; and

forming a second terminal connected to the front plate and the back plate.

24. The method of claim 21, further comprising:

forming a first terminal connected to the one diffusion region of the diffusion regions;

forming a second terminal connected to the front plate; and

forming a third terminal connected to the back plate; and

providing a higher potential to the first terminal than the second terminal or the third terminal.

25. The method of claim 16, wherein:

the dielectric is a first dielectric and a second dielectric both approximately 10 Å to 100 Å thick; and

the front plate and the back gate have a critical dimension of approximately 1000 Å to 2000 Å.

26. The method of claim 16, wherein:

the at least one back plate is at least two back plates;

the at least one front plate is at least two front plates;

the dielectric structure contains a first dielectric and a second dielectric.

27. The method of claim 26, wherein the two front gates are at least a first front gate and a second front gate, the

first and second front gate being formed simultaneously in a same process.

28. The method of claim 26, wherein the two or more front gates are a first front gate and a second front gate, the first and second front gate being formed separately.

29. A capacitor formed on a substrate having a buried insulator layer and a device layer on the insulator layer, said capacitor comprising:

a lower plate formed in a buried insulator layer;

a portion of said buried insulator layer formed on said lower plate to provide a first capacitor dielectric;

a portion of a device layer formed on said first capacitor dielectric;

a second capacitor dielectric formed on said portion of said device layer; and

an upper plate formed on said second capacitor dielectric.

30. The capacitor of claim 29, wherein said portion of said device layer has at least one terminal electrically coupled to a first voltage level.

31. The capacitor of claim 29, wherein said upper plate is electrically coupled to a second voltage level.

32. The capacitor of claim 31, wherein said lower plate is electrically coupled to said first voltage level.

33. The capacitor of claim 31, wherein said lower plate is electrically coupled to said second voltage level.

34. The capacitor of claim 31, wherein said lower plate is electrically coupled to a third voltage level.

35. The capacitor of claim 34, wherein said first voltage level comprises a voltage source high enough to prevent MOS channel inversion.

36. A dual-gate capacitor, comprising:

at least one back gate formed in a buried insulator layer;

at least one front gate formed above the buried insulator layer;

a dielectric layer formed between the at least one front gate and back gate; and

diffusion regions doped adjacent to the at least one back gate.

37. The dual-gate capacitor of claim 36, wherein a portion of the buried insulator layer is a first capacitor dielectric and the dielectric is a second capacitor dielectric.

38. The dual-gate capacitor of claim 36, further comprising:

a first terminal connected to the at least back plate and the diffusion regions to short the diffusion regions; and

a second terminal connected to the at least front plate.

39. The dual-gate capacitor of claim 36, further comprising:

a first terminal connected to the diffusions regions; and

a second terminal connected to the at least one front plate and back plate.

40. The dual-gate capacitor of claim 36, further comprising:

a first terminal connected to the one diffusion region of the diffusion regions;

a second terminal connected to the at least front plate; and

a third terminal connected to the at least back plate.

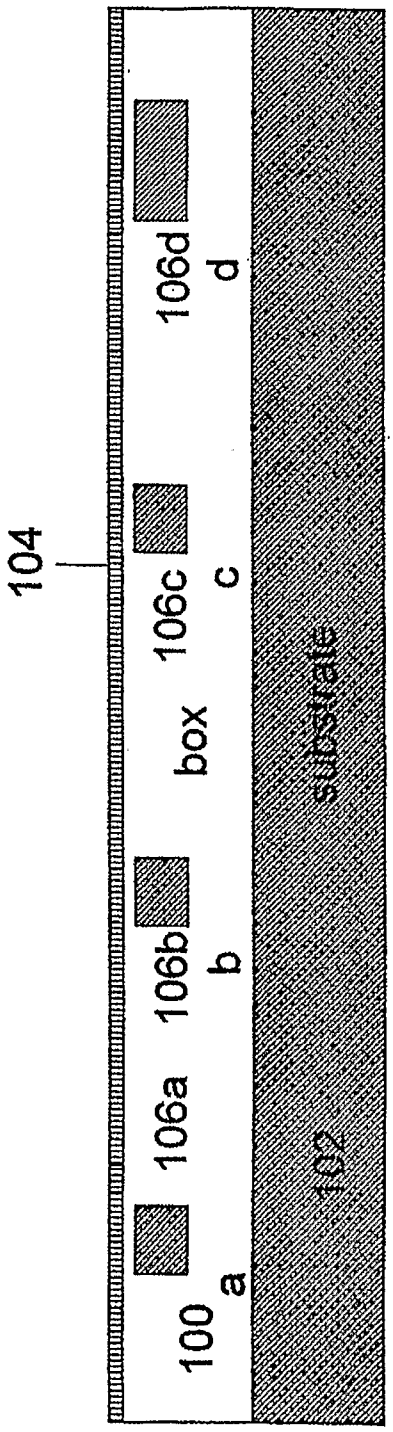


Figure 1

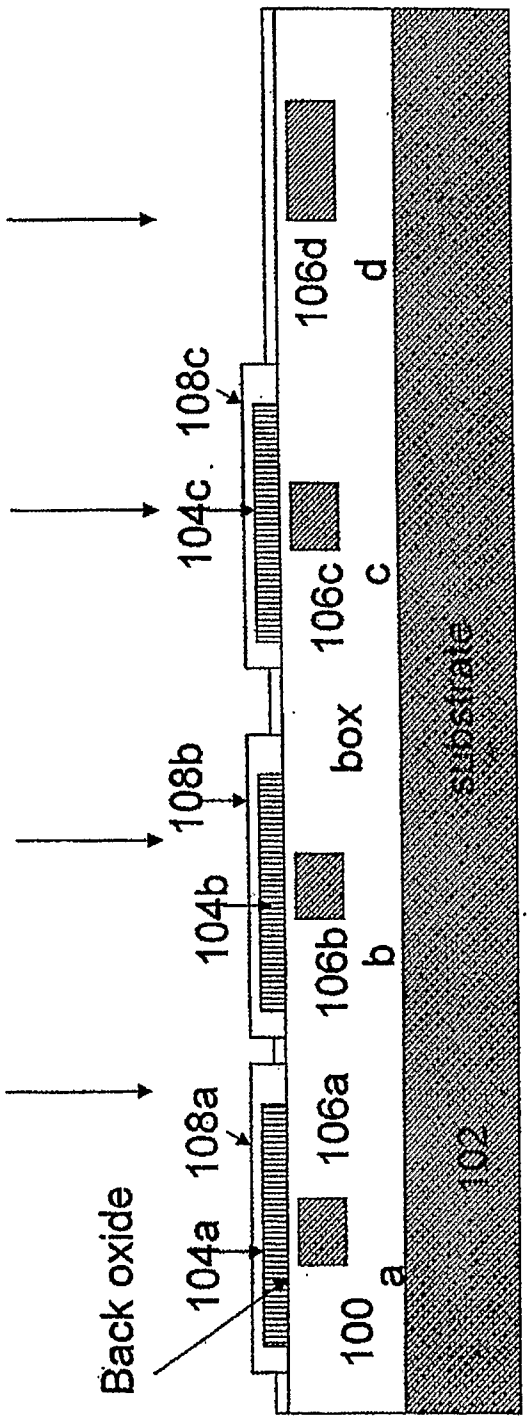

Back oxide
104a
108a
106a
a
100
104b
108b
106b
b
box
104c
108c
106c
c
106d
d
substrate
102

Figure 2

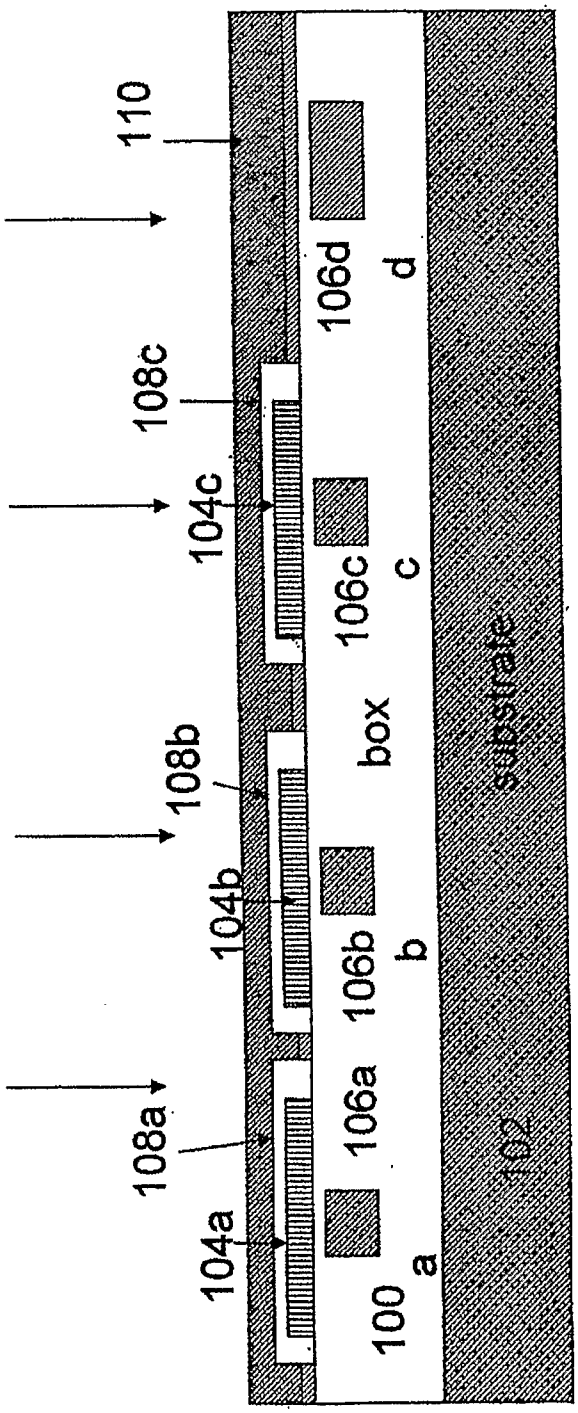

110
108c
104c
108b
104b
108a
104a
106a
106b
106c
106d
a
b
c
d
box
substrate
102
100

Figure 3

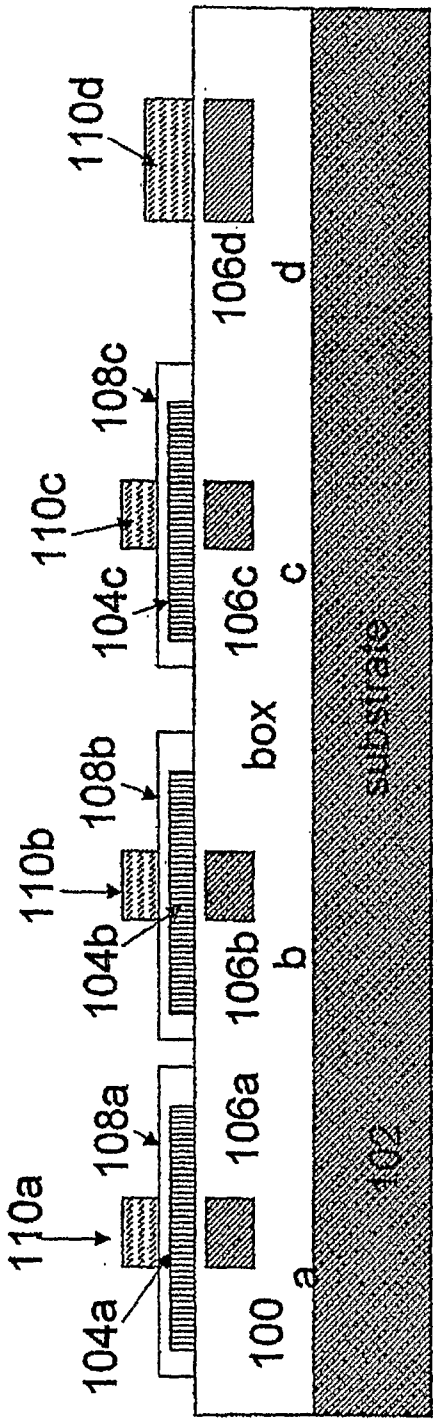

110d
106d
d
108c
110c
104c
106c
c
box
108b
110b
104b
106b
b
108a
106a
110a
104a
100
a
substrate

Figure 4

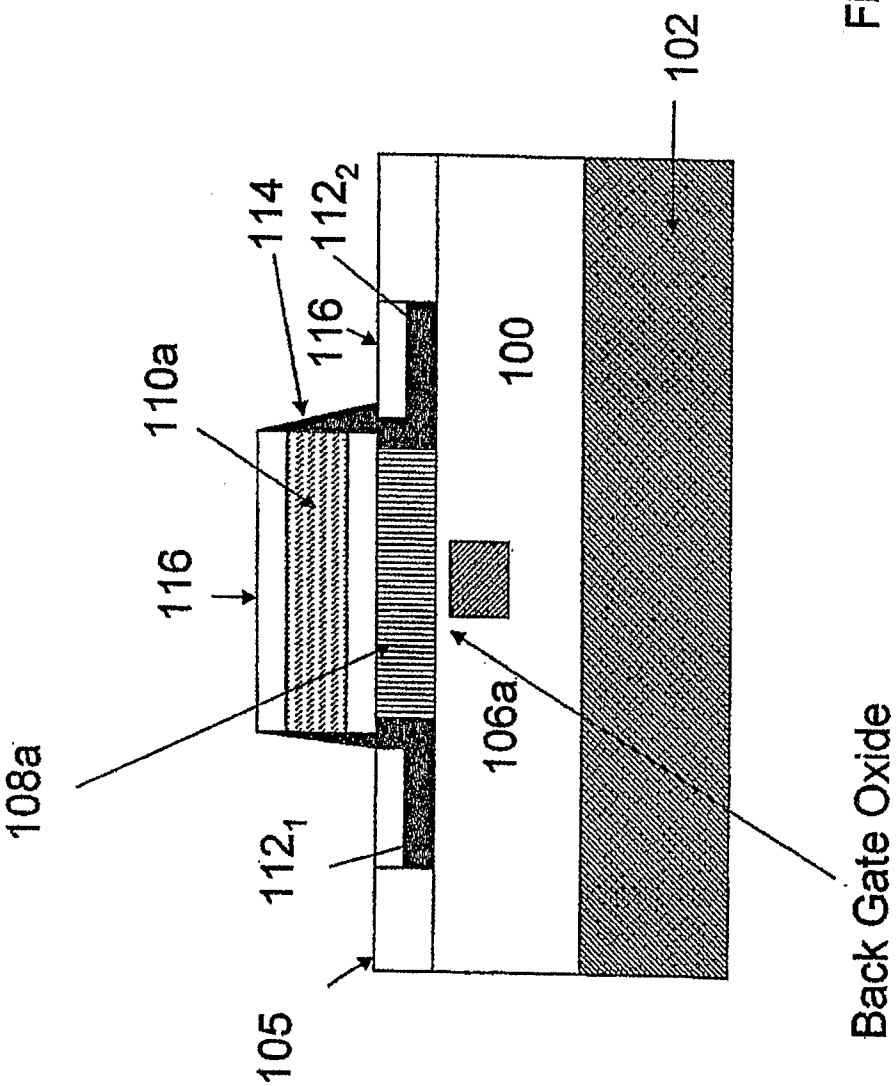
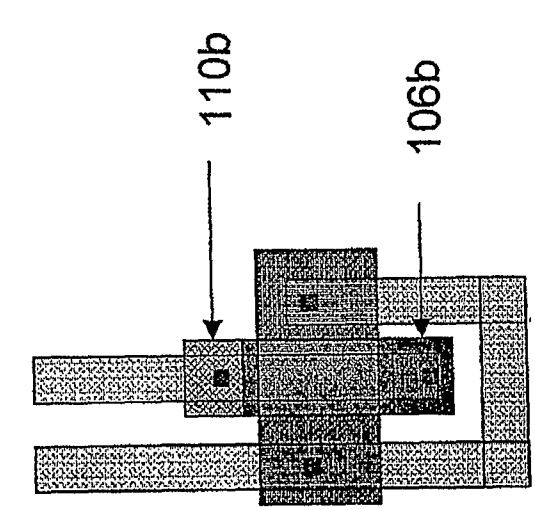

102
114
112$_2$
116
110a
100
116
108a
106a
112$_1$
105
Back Gate Oxide

Figure 5



B: High Density Capacitor

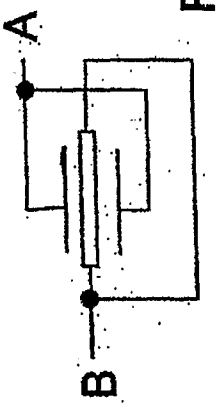
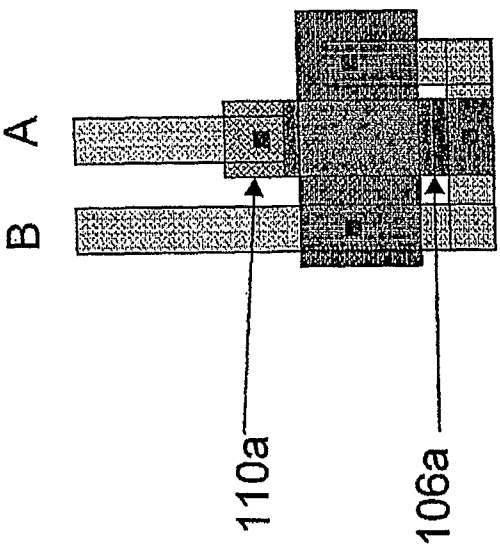


Figure 6b



A: FET Capacitor

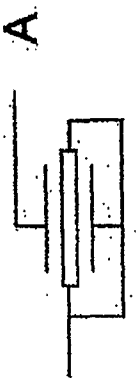
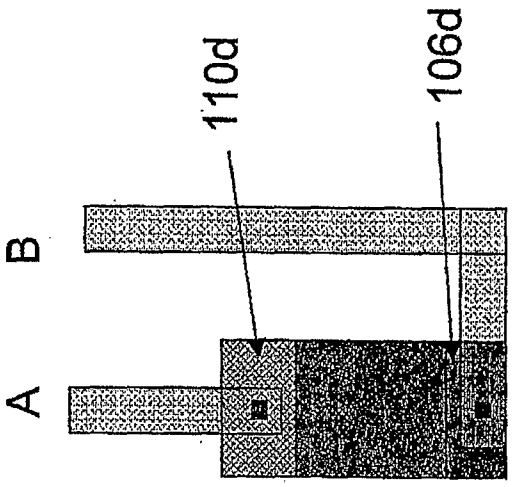
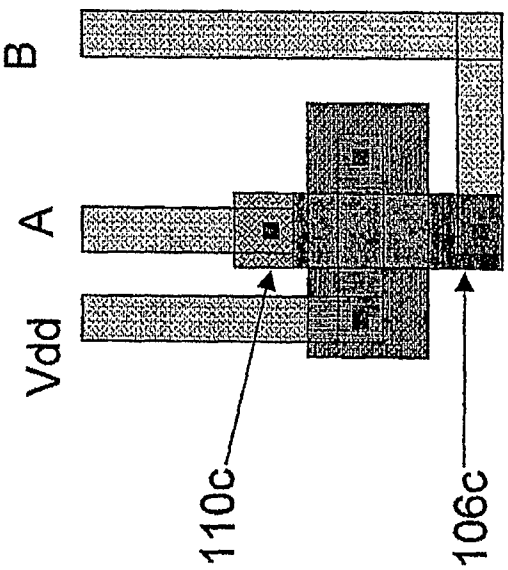


Figure 6a



D: Dual gate capacitor

Figure 6d



C: FD Capacitor

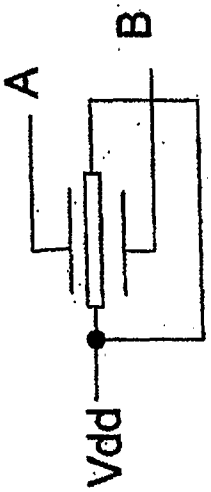


Figure 6c

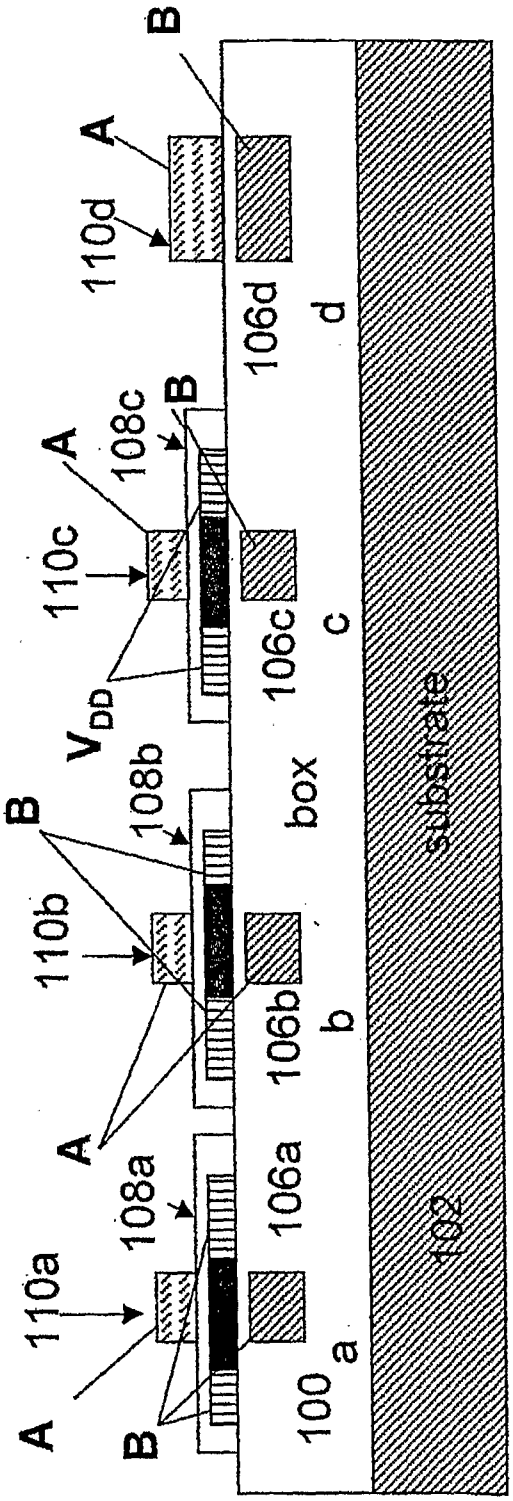

A
B
110a
108a
106a
a
100
B
A
110b
108b
106b
b
box
B
A
110c
108c
106c
c
V_{DD}
B
A
110d
106d
d
substrate
102

Figure 7