

[54] **METHOD FOR COMPRESSING AND SYNTHESIZING A CYCLIC ANALOG SIGNAL BASED UPON HALF CYCLES**

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[51] Int. Cl. **H04b 1/66**

[58] Field of Search.....179/1 SA, 1 VS, 15.55 T, 179/15.55 R, 15 BW, 15 BT; 325/62, 328, 329; 333/14

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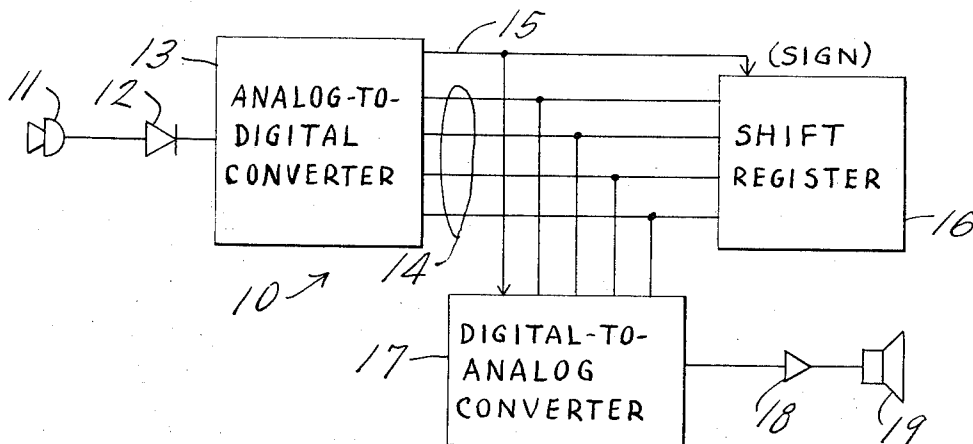
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[57] **ABSTRACT**

An improved method for compressing a cyclic analog signal in which adjacent positive and negative half cycles are similar, such as an audio signal, and for reconstructing or synthesizing a new analog signal from the compressed signal. The original signal is compressed by removing one of the positive or the negative half cycles and, in a preferred embodiment, digitizing the remaining half cycles. The new analog signal is generated by sequentially applying each half cycle to an output and simultaneously storing such applied half cycle in a memory. After a half cycle is applied to the output and prior to applying the next half cycle in the sequence, the stored half cycle is applied to the output at a reversed polarity to simulate the portion which was originally removed.

12 Claims, 8 Drawing Figures



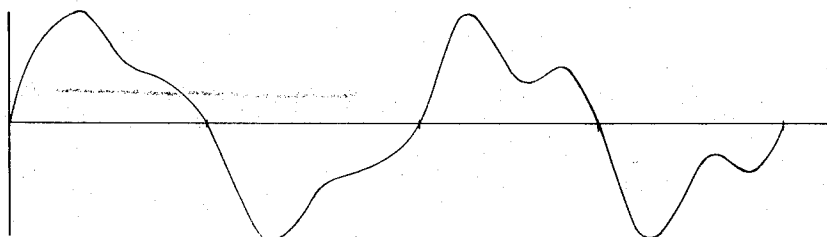


FIG-1A-

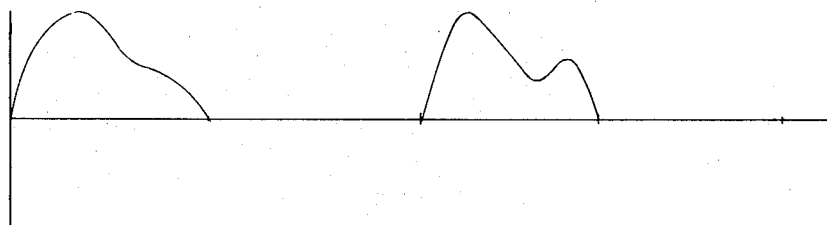


FIG-1B-

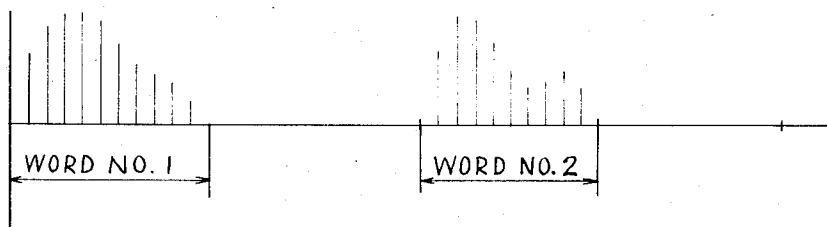


FIG-1C-

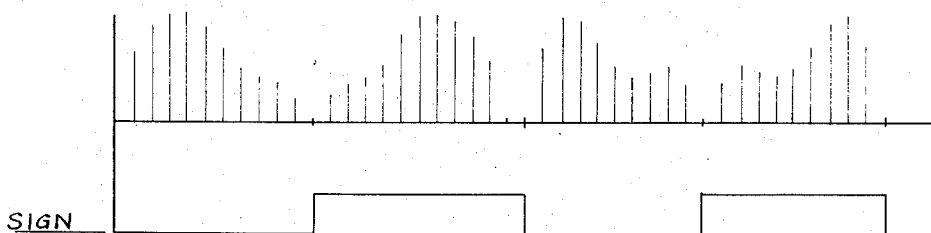


FIG-1D-

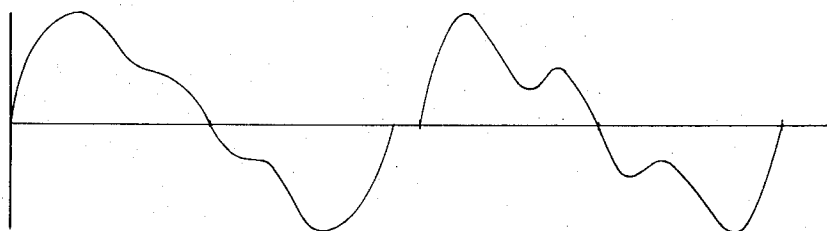
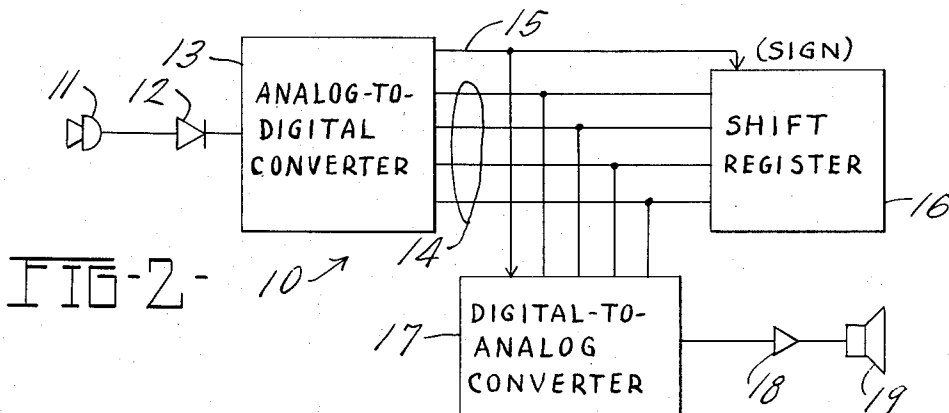
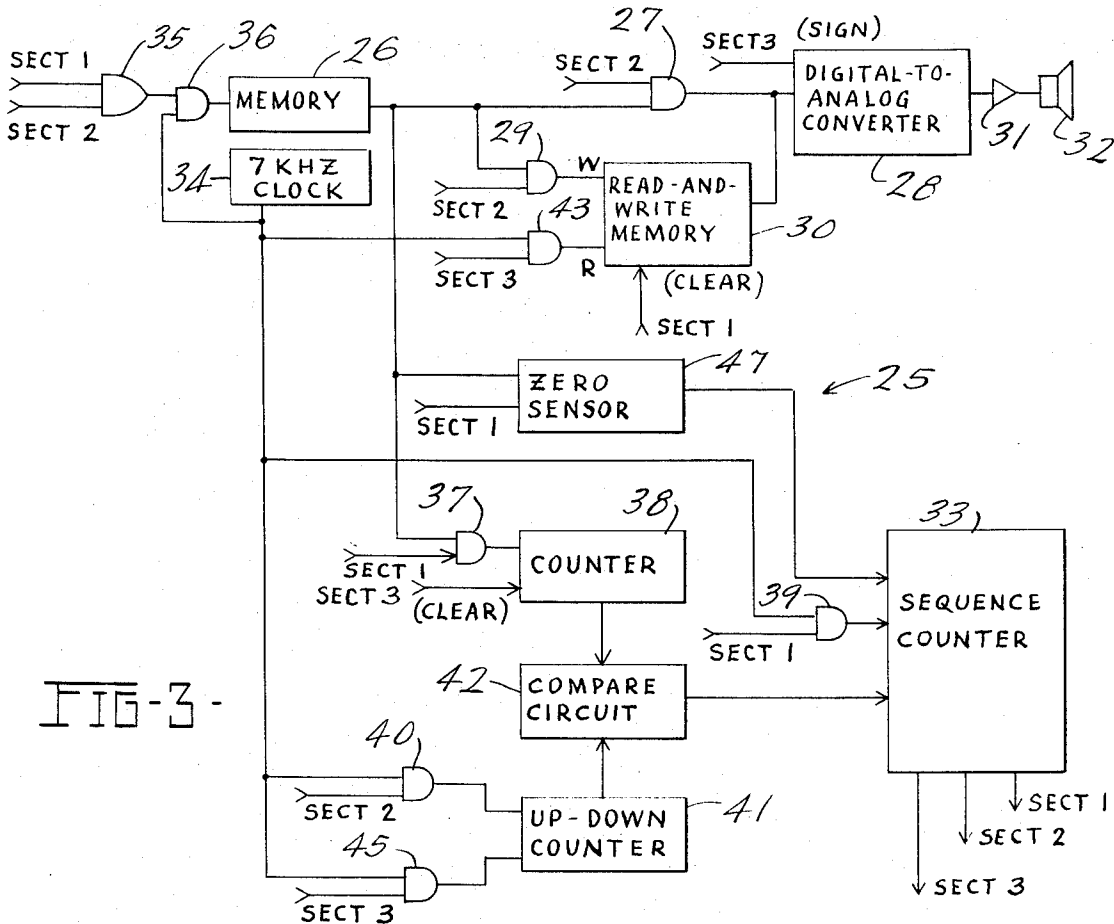


FIG-1E-

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NUMBER OF DATA FRAMES	4-BIT DATA FRAMES
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FIG-4-

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METHOD FOR COMPRESSING AND SYNTHESIZING A CYCLIC ANALOG SIGNAL BASED UPON HALF CYCLES

BACKGROUND OF THE INVENTION

This invention relates to speech compression and more particularly to an improved method for compressing speech and similar analog signals and for generating a new analog signal from the compressed signal.

Each year federal, state and local governments and various businesses expand their use of radio communications in day to day business operations. However, the available bands for radio communications are fixed and quite limited. The ever increasing demands placed on communications facilities have therefore created a demand for methods for compressing speech.

In addition, it has sometimes been advantageous to give general purpose and special purpose digital computers an output having the capability of audibly reproducing spoken words. Typically, a limited dictionary of words is stored in the computer memory and spoken messages are formed by programing the computer to sequentially address the individual message words in the memory and to deliver the addressed words to, for example, a loudspeaker. It is also desirable to compress the spoken words which are stored in the computer memory. If the spoken words are not compressed prior to storage in the memory, large segments of the computer's memory may be required for storing the dictionary of words. However, it is undesirable to tie up large segments of the computer's memory since this limits the capabilities of the computer for solving complicated problems which require a large amount of memory space. It is therefore apparent that any techniques which will reduce the memory size necessary to store words in a computer memory is valuable to the computer industry.

SUMMARY OF THE INVENTION

According to the present invention, an improved method is provided for compressing speech, or other cyclic analog signals in which adjacent positive and negative half cycles are similar, and for reconstructing or synthesizing a new analog signal from the compressed signal. The analog signals are compressed by removing one of the positive or the negative half cycles and, preferably, also digitizing the remaining half cycles. The compressed signal may then be transmitted to a receiving station or stored in a computer memory.

The analog signal is generated from the compressed signal by sequentially applying each half cycle of the compressed signal to an output and simultaneously storing each applied half cycle in a memory. After a half cycle is applied to the output and prior to applying the next half cycle in the sequence, the stored half cycle is applied to the output at a reversed polarity to simulate the portion of the signal which was removed. When the compressed signal is in a digitized format, the signal appearing at the output is converted to an analog format by means of a conventional digital-to-analog converter. Approximately a 40 percent reduction in information can be accomplished through the use of this technique for compressing analog signals. This information reduction is less than 50 percent since information must be also stored or transmitted to indicate when to change the sign of the signal appearing at the output.

Accordingly, it is a preferred embodiment of the invention to provide an improved method for compressing analog signals and for or synthesizing a new analog signal from the compressed signal.

Another object of the invention is to provide an improved method for reducing the amount of space required for storing spoken words in a memory and for reconstructing the spoken words from signals stored in the memory.

Other objects and advantages of the invention will become apparent from the following detailed description with reference being made to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1, comprising FIGS. 1a - 1e, comprises a series of diagrams of waveforms generated while compressing and reconstructing an analog waveform in accordance with the present invention;

FIG. 2 is a schematic block diagram of apparatus according to one embodiment of the present invention for compressing, transmitting and reconstructing spoken messages;

FIG. 3 is a block diagram of apparatus according to a second embodiment of the present invention for reconstructing spoken messages from compressed speech stored in a computer memory; and

FIG. 4 is a diagram showing the format of a word stored in a computer memory for use by the apparatus of FIG. 3 in reconstructing spoken messages.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the present invention, an improved method is provided for compressing speech and similar cyclic analog signals and for generating from the compressed waveforms a new analog signal which simulates the original waveform. A typical portion of an analog waveform which may be compressed is shown in FIG. 1a. This waveform has the properties of being cyclic, alternating between positive and negative half cycles. Two adjacent half cycles which form a single cycle may vary in length and form as the analog signal varies. However, variations in adjacent half cycles are typically minimum. Since adjacent half cycles are similar, the analog signal may be compressed by half wave rectification to remove one of the positive or the negative half cycles. As shown in FIG. 1b, the analog signal of FIG. 1a has been compressed by removing the negative half cycles, thereby reducing the information by 50 percent. The signal may be further compressed by digitizing, resulting in the waveform of FIG. 1c. This waveform comprises a series of pulses having amplitudes corresponding to the amplitude of the signal of FIG. 1b at periodic sampling points. The sampling must take place at a rate higher than the highest frequency component in the original analog signal of FIG. 1a. For speech, it has been found that a 7 kHz. sampling rate is satisfactory.

The compressed signal of FIG. 1c is suitable for transmission over transmission lines or by radio or it may be stored in a digital memory in, for example, a computer. When the signal of FIG. 1c is transmitted to a receiving station, an additional signal must also be simultaneously transmitted to indicate the beginning and ending of each half cycle. When the signal is stored in a memory, additional information must also be stored in

the memory to indicate the length or number of samples in each half cycle. This additional signal or information reduces the effective compression from 50 to perhaps only 40 percent.

After a signal is compressed into the format shown in FIG. 1c and is either transmitted to a receiver or read from a memory, a new signal such as that shown in FIG. 1d is generated and applied to a digital-to-analog converter for reconstructing or synthesizing a new analog signal as shown in FIG. 1e. The signal of FIG. 1d comprises each remaining half cycle from FIG. 1c sequentially followed by either the reflection of such half cycle or a repetition of such half cycle. The sign or polarity of the reflection or repetition of the half cycle is changed from that of the transmitted half cycle for simulating the portion of the original waveform which was removed during compression. The new analog signal of FIG. 1e is then obtained by applying the digital signal of FIG. 1d to a conventional digital-to-analog converter.

It will be noted that a short break appears between the first and second cycles in the reconstructed or synthesizing analog signal of FIG. 1e. This occurs because the second half cycle of the original signal in FIG. 1a, the portion of the signal which was removed during compression, is slightly longer than the first half cycle. If, on the other hand, the second half cycle was shorter than the first half cycle, the reflected half cycle would be cut short to maintain the timing occurring in the original signal of FIG. 1a. Although the reconstructed half cycles shown in FIG. 1e are reversed from the original, removed half cycles from FIG. 1a, reproduction of the audio signal is intelligible since frequency components are maintained from cycle to cycle in both positive and negative half cycles.

Referring now to FIG. 2, apparatus 10 is shown according to one embodiment of this invention for compressing an audio signal, and for reconstructing a new audio signal to correspond to the original signal. An audio signal generated by conventional means, for example, by a microphone 11, is compressed by serially applying the signal through a rectifier 12 and an analog-to-digital converter 13. The converter 13 has a binary output which appears on a plurality of lines 14 and corresponds to the amplitude of samples of the original audio signal. A sign bit also appears on an output line 15 from the converter 13 for indicating changes in polarity of the original signal. The lines 14 and 15 may comprise transmission lines or a radio link in the event that the compressed signal is to be transmitted over a long distance. The lines 14 and 15 are terminated at a receiving station which includes a memory, such as a shift register 16, and a digital-to-analog converter 17. Compressed half cycles of the type shown in FIG. 1c are simultaneously applied to the converter 17 and stored in the shift register 16. The end of each transmitted half cycle is indicated by a change in the sign bit appearing on the line 15. A change in the sign bit appearing on the line 15 at the end of a half cycle causes the contents of the register 16 to be shifted to the converter 17. The converter 17 will then have an input as shown in FIG. 1d and an output as shown in FIG. 1e. The output may be amplified by means of an amplifier 18 and reproduced by, for example, a loudspeaker 19.

Turning now to FIG. 3, apparatus 25 is shown for reconstructing analog speech signals of the type shown in FIG. 1e from a compressed signal of the type shown in

FIG. 1c stored in a memory 26. The memory 26 may comprise any conventional memory or it may comprise an integrated circuit read only memory. The format of signals stored in the memory 26 is shown in FIG. 4. A word is stored in the memory 26 for each of the digitized half cycles remaining after the signal is compressed as shown in FIG. 1c. For the sake of description, it will be assumed that data is stored in and read from the memory 26 as a series of 4-bit frames. A single 4-bit frame appears at the beginning of each word stored in the memory 26 for indicating the number of samples occurring in the half cycle associated with such stored word. The remaining portion of the stored word comprises a series of 4-bit data frames, one for each sample in the associated half cycle. The maximum number of samples appearing in a half cycle is determined by the lowest possible frequency component in the original analog waveform and the sampling rate. If, for example, a 7 kHz. sampling rate is used, a low frequency cutoff of 250 Hz. will result in a maximum of 15 samples in a half cycle. This permits the use of four bits for indicating the number of samples or data frames in a half cycle.

Referring again to FIG. 3, the output of the memory 26 is applied through an AND gate 27 to a digital-to-analog converter 28 and through an AND gate 29 to a read and write memory 30. The output of the converter 28, which will be similar to the waveform shown in FIG. 1e, is delivered through an amplifier 31 to a transducer, such as a loudspeaker 32. The process of reading the memory 26 and reconstructing a new analog waveform is controlled by a sequence counter 33 and a 7 kHz. control clock 34. The clock 34 must, of course, operate at the same frequency as the original signal was sampled when it was digitized. While a new analog signal is being reconstructed, the sequence counter 33 will have one of three possible outputs, SECT 1, SECT 2 and SECT 3. At the termination of reconstructing the new analog signal, the three outputs of the sequence counter 33 will all go to zero or ground potential. For simplicity, connections to the outputs of the sequence counter 33 have been omitted from FIG. 3.

When an analog signal is to be reconstructed or generated, the sequence counter 33 is counted to SECT 1. The SECT 1 output of the counter 33 is applied through an OR gate 35 to enable a clock pulse to pass from the clock 34 through an AND gate 36 to read the first 4-bit frame from the memory 26. As stated above, this first frame consists of a binary number corresponding to the number of 4-bit data frames to be read from the memory 26. At the same time, the SECT 1 output of the counter 33 enables an AND gate 37 for applying the output of the memory 26 to a 4-bit counter 38, clears the memory 30 and enables a gate 39 to pass a clock pulse from the clock 34 to the sequence counter 33 to count to SECT 2.

The SECT 2 output of the sequence counter 33, like the SECT 1 output, passes through the OR gate 35 for enabling the AND gate 36 to apply a series of pulses from the clock 34 to the memory 26. At the same time, the SECT 2 output enables the gate 27 for applying the output of the memory 26 to the digital-to-analog converter 28 and enables the gate 29 for writing the output of the memory 26 into the read and write memory 30. The series of pulses from the clock 34 are also applied through an AND gate 40, which is enabled by SECT 2, to count up an up-down counter 41 by one for each

pulse. A conventional compare circuit 42 continuously compares the counts stored in the counters 38 and 41. When a complete half cycle has been read from the memory 26, the contents of the counter 41 will equal the contents previously stored in the counter 38 and the compare circuit 42 will cause the sequence counter 33 to step to SECT 3. The memory 26 is not read during SECT 3.

The sequence count of SECT 3 enables a gate 43 for applying pulses from the clock 34 to the read and write memory 30. Each clock pulse applied from the gate 43 to the memory 30 causes a 4-bit data frame to be read from the memory 30 and applied to the digital-to-analog converter 28. If the memory 30 is of the first-in-first-out type, the data read from the memory 30 will correspond directly to the data read from the memory 26. If, however, the memory 30 is of the last-in-first-out type, the output of the memory 30 will be a reflection of the output from the memory 26. SECT 3 is also applied to the converter 28 to cause the converter 28 to change the polarity of the analog output generated from the data read from the memory 30. In addition, the sequence count SECT 3 is used to clear the counter 38 to zero and to enable an AND gate 45 to apply clock pulses to a count down input of the up-down counter 41.

Each time a 4-bit data frame is read from the read and write memory 30, the counter 41 is counted down by one. When the counter 41 is counted down to zero, the compare circuit 42 will cause the sequence counter 33 to return to SECT 1. This in turn causes the next half cycle to be read from the memory 26 in a manner similar to that described above. If the sequence counter 33 returns to SECT 1 and the final word has been read from the memory 26, a sensor 47 will sense a zero output on all four bits from the memory 26 and cause all three outputs of the sequence counter 33 to go to ground. This terminates generating the new analog signal.

It has been found that in some instances distortion occurs in the reconstructed analog signal, particularly at low signal levels. Such distortion has been traced to a mismatched phase relationship between the original half cycle read from the memory 26 and the half cycle read from the memory 30. The noise has been reduced or eliminated by advancing the signal read from the memory 30 to achieve a proper phase relationship. A similar advance may be used when reading the shift register 16 of FIG. 2. The advance may be accomplished by shifting the clock pulse which reads the shift register 16 in FIG. 2 or the memory 30 in FIG. 3 by one-half cycle. This can be accomplished, for example, by using a 14 kHz. clock source and eliminating every other clock pulse to obtain a 7 kHz. clock signal for reading the memory. Each time the sign of the reconstructed analog signal changes, an extra pulse is allowed to pass from the 14 kHz. source to advance the phase of the 7 kHz. clock signal by one-half cycle. The phase shift may, of course, be accomplished by other obvious techniques.

It will be appreciated that various changes and modifications may be made to the above described embodiments and that this invention may be used for compressing and reconstructing various types of analog signals without departing from the spirit and the scope of the claimed invention.

What I claim is:

1. For a cyclic analog signal in which adjacent positive and negative half cycles are similar, an improved method for compressing said signal during transmission and synthesizing a similar signal at an output comprising the steps of: removing one of said positive and negative half cycles; transmitting the remaining other of said positive and negative half cycles to said output; and repeating at said output each transmitted half cycle prior to reception of the next half cycle, each of said transmitted half cycles being repeated at a polarity opposite from the polarity of said transmitted half cycles.

2. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 1, including the step of storing said transmitted half cycles in a memory and wherein said transmitted half cycles are repeated by reading each stored half cycle from said memory prior to storing the next transmitted half cycle.

3. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 2, wherein each stored half cycle is read from said memory in an order reversed from the order in which it was transmitted and stored.

4. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 2, wherein each stored half cycle is read from said memory in the same order in which it was transmitted and stored.

5. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 2, and including the step of modifying the phase relationship between said transmitted half cycles and said repeated half cycles more nearly to simulate the cyclic analog signal.

6. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 2, including the steps of digitizing said transmitted half cycles prior to transmission and converting said received half cycles and said repeated half cycles from a digital to an analog format at said output.

7. An improved method for compressing a cyclic analog signal during transmission and synthesizing a similar signal at an output, as set forth in claim 1, and including the steps of digitizing said transmitted half cycles prior to transmission and converting said received half cycles and said repeated half cycles from a digital to an analog format at said output.

8. A method for synthesizing a cyclic analog signal from a sequence of half cycles to one polarity comprising the steps of: sequentially applying said half cycles to an output, simultaneously storing each half cycle applied to said output, and applying each stored half cycle to said output prior to applying the next half cycle in the sequence to said output, each stored half cycle being applied at a polarity opposite from the polarity of said sequence of half cycles.

9. A method for synthesizing a cyclic analog signal from a sequence of half cycles of one polarity, as set forth in claim 8, wherein each stored half cycle is applied to said output in a format reversed from the format in which the original half cycle is applied to said output.

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10. A method for synthesizing a cyclic analog signal from a sequence of half cycles of one polarity, as set forth in claim 8, wherein each stored half cycle is applied to said output in the same format as the original half cycle is applied to said output.

11. A method for synthesizing a cyclic analog signal from a sequence of half cycles of one polarity, as set forth in claim 8, and including the step of modifying the phase relationship between the applied half cycles and

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the applied stored half cycles more nearly to simulate the original cyclic analog signal.

12. A method for synthesizing a cyclic analog signal from a sequence of half cycles of one polarity, as set forth in claim 8, wherein said sequence of half cycles are in a digitized format and further including the step of converting to an analog format said applied sequence of half cycles and said applied stored half cycles.

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