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(54) **Title**: A COMPONENT OF A SUBSTRATE SUPPORT ASSEMBLY PRODUCING LOCALIZED MAGNETIC FIELDS

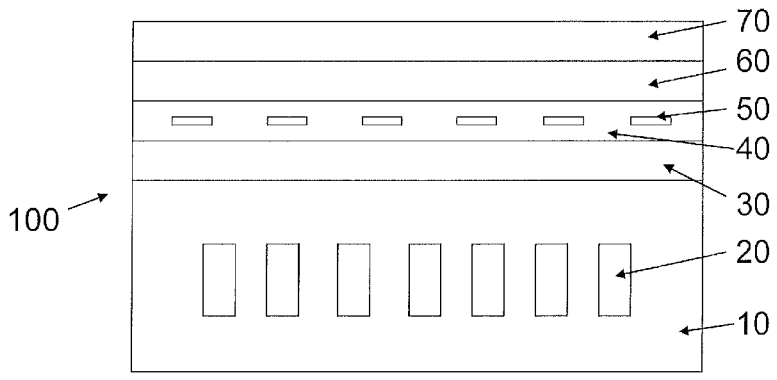

Figure 1

(57) **Abstract**: A component of a substrate support assembly such as a substrate support or edge ring includes a plurality of current loops incorporated in the substrate support and/or the edge ring. The current loops are laterally spaced apart and extend less than halfway around the substrate support or edge ring with each of the current loops being operable to induce a localized DC magnetic field of field strength less than 20 Gauss above a substrate supported on the substrate support during plasma processing of the substrate. When supplied with DC power, the current loops generate localized DC magnetic fields over the semiconductor substrate so as to locally affect the plasma and compensate for non-uniformity in plasma processing across the substrate.

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A COMPONENT OF A SUBSTRATE SUPPORT ASSEMBLY PRODUCING LOCALIZED MAGNETIC FIELDS

FIELD OF THE INVENTION

[0001] Disclosed herein is a component of a substrate support assembly having a plurality of current loops adapted to generate small magnetic fields and compensate for variations during plasma processing of a semiconductor substrate supported on the substrate support assembly. The component can be an edge ring or substrate support such as a tunable electrostatic chuck (ESC) that allows for improved control of critical dimension (CD) uniformity, as well as methods and uses thereof.

BACKGROUND

[0002] In this specification where a document, act or item of knowledge is referred to or discussed, this reference or discussion is not an admission that the document, act or item of knowledge or any combination thereof was at the priority date, publicly available, known to the public, part of common general knowledge, or otherwise constitutes prior art under the applicable statutory provisions; or is known to be relevant to an attempt to solve any problem with which this specification is concerned.

[0003] Commonly-owned U.S. Patent No. 6,921,724 discloses an etch processor for etching a wafer that includes an ESC for holding a wafer and a temperature sensor reporting a temperature of the wafer. The chuck includes a heater controlled by a temperature control system and a temperature sensor is operatively coupled to the temperature control system to maintain the temperature of the ESC at a selectable set-point temperature. A first set-point temperature and a second set-point temperature are selected. The wafer is placed on the chuck and set to the first set-point temperature. The wafer is then processed for a first period of time at the first set-point temperature and for a second period of time at the second set-point temperature.

[0004] Commonly-owned U.S. Patent No. 6,847,014 discloses a ESC for a plasma processor comprising a temperature-controlled base, a thermal insulator, a flat support, and a heater. The temperature-controlled base has a temperature below the

desired temperature of a substrate. The thermal insulator is disposed over the temperature-controlled base. The flat support holds a substrate and is disposed over the thermal insulator. A heater is embedded within the flat support and/or disposed on an underside of the flat support and includes a plurality of heating elements that heat a plurality of corresponding heating zones. The power supplied and/or temperature of each heating element is controlled independently.

[0005] Commonly-owned U.S. Patent Publication No. 2011/0092072 discloses a heating plate for a substrate support assembly in a semiconductor plasma processing apparatus comprising multiple independently controllable planar heater zones arranged in a scalable multiplexing layout, and electronics to independently control and power the planar heater zones.

[0006] Thus, there is a need for a component of a substrate support assembly, such as a substrate support assembly comprising an ESC or edge ring, which is capable of making spatial corrections and/or adjustments to the azimuthal plasma processing rate non-uniformity to correct for film thickness variation, etch chamber induced etch rate non-uniformity and large magnetic field (from plasma generation) induced non-uniformity.

[0007] While certain aspects of conventional technologies have been discussed to facilitate disclosure of the invention, Applicant in no way disclaims these technical aspects, and it is contemplated that the claimed invention may encompass or include one or more of the conventional technical aspects discussed herein.

SUMMARY

[0008] Disclosed herein is a component of a substrate support assembly comprising an edge ring or substrate support incorporating a plurality of current loops which generate small magnetic fields in a plasma during plasma processing of at least one semiconductor substrate. The component creates a localized magnetic field without the need for a permanent magnet or iron core. The magnetic fields are small enough to avoid damage to circuits undergoing processing on the semiconductor substrate but strong enough to affect the plasma so as to increase or decrease localized plasma processing such as etch rates during plasma etching. The spatial adjustments to the localized plasma processing rates can compensate for film

thickness variation, chamber non-uniformity and/or magnetic field induced non-uniformity.

[0009] During plasma processing such as etching, the current loops can be powered to manipulate the plasma and effect spatial adjustments to an azimuthal plasma to correct for film thickness variation, chamber non-uniformity and/or magnetic field induced non-uniformity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure **1** shows a cross-sectional view of a substrate support assembly comprising an ESC.

[0011] Figure **2** shows a top view (FIG. **2A**) of a component of a substrate support assembly in accordance with an embodiment and a cross-sectional view (FIG. **2B**) of the associated perpendicular applied magnetic field.

[0012] Figure **3** shows a perspective view of a component of a substrate support assembly in accordance with an embodiment.

[0013] Figure **4** shows a top view of a component of a substrate support assembly in accordance with another embodiment.

[0014] Figure **5** shows a top view of a component of a substrate support assembly in accordance with yet another embodiment.

[0015] Figure **6** shows a top view of a component of a substrate support assembly in accordance with a further embodiment.

[0016] Figure **7** shows a top view of a component in accordance with an embodiment that surrounds a substrate support.

[0017] Figure **8** shows a perspective view of a component in accordance with an embodiment that surrounds a substrate support.

[0018] Figure **9** shows a top view of a component in accordance with another embodiment that surrounds a substrate support.

[0019] Figure **10** shows a top view of a component of a substrate support in accordance with an embodiment and a component surrounding the substrate support in accordance with an embodiment.

[0020] Figure **11** shows a top view of a component of a substrate support in accordance with another embodiment and a component surrounding the substrate support in accordance with another embodiment.

[0021] Figure **12** shows a top view of a component of a substrate support in accordance with yet another embodiment and a component surrounding the substrate support in accordance with yet another embodiment.

[0022] Figure **13** shows a top view of an etch rate pattern after partial etching of a substrate.

[0023] Figure **14** shows a top view of an etch rate pattern after final etching of a substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] Precise azimuthal CD control on a substrate by small (e.g., <5°C) corrections azimuthally to the substrate temperature can address CD uniformity which is sensitive to substrate temperature (e.g., as high as 1 nm/°C). For example, even with an azimuthally symmetric etch chamber design, film thickness non-uniformity can result in azimuthal etch rate non-uniformity, as regions of substrate with thinner films undergo film clearing faster than other regions on the substrate. Small variabilities in hardware also contribute to azimuthal etch rate non-uniformity (e.g., <1%). Large applied DC magnetic fields (e.g., >20 Gauss), such as those used for plasma generation, can be a source of etch rate non-uniformity in plasma etching. Such a magnetic field induces a force, F, defined by F = ExB (where E is the electric field in the plasma and B is the magnetic field) on electrons in the plasma which results in azimuthal non-uniformity in the plasma during plasma etching, such non-uniformity in the plasma can lead to non-uniformity in the etch rate.

[0025] Figure **1** shows a cross-sectional perspective of a substrate **70** and substrate support assembly **100** comprising a tunable ESC. The tunable ESC comprises a baseplate **10** with coolant fluid channels **20** disposed therethrough. A thermal insulating layer **30** is disposed on baseplate **10**. A heating plate **40** is disposed on insulating layer **30** and comprises an array of discrete heating zones **50** distributed laterally across the substrate support and is operable to tune a spatial temperature profile for CD control. A ceramic plate **60** is disposed on heating plate **40**. A

substrate **70** is disposed over the ceramic plate **60** and is electrostatically clamped to the ESC by an electrostatic chucking electrode (not shown) embedded in the ceramic plate. It is noted that a substrate support **100** may comprise a standard, or non-tunable, ESC, instead of a tunable ESC. The substrate support assembly is adapted to support substrates of at least about 200mm in diameter, or at least about 300mm in diameter or at least about 450mm in diameter. The materials of the components are not particularly limited. Baseplate **10** is preferably made from a suitable thermal conductor, such as aluminum or stainless steel. Ceramic plate **60** is preferably made from a suitable ceramic material, such as aluminum oxide (Al_2O_3) or aluminum nitride (AlN). Thermal insulating layer **30** preferably comprises a silicone material, which adheres baseplate **10** to heating plate **40**. An epoxy, silicone or metallurgical bond is preferably used to adhere heating plate **40** to ceramic plate **60**.

[0026] Under operational conditions (e.g., plasma etching), DC magnetic fields used for plasma generation are a known source of etch rate non-uniformity. For example, a magnetic field parallel to the plane of substrate undergoing processing in the plasma volume is expected to induce non-uniformity in the azimuthal etch rate pattern with about 5% etch rate non-uniformity induced per Gauss of applied magnetic field. Thin film thickness variation and etch chamber hardware variation are also known to contribute to azimuthal etch rate non-uniformity.

[0027] The induced non-uniformity can be used to make adjustments to the azimuthal etch rate pattern using applied DC magnetic fields. These applied magnetic fields are relatively small (e.g., <20 Gauss or <10 Gauss, preferably $\leq$ 1 Gauss or $\leq$ 1/2 Gauss) and allow for localized corrections to the plasma processing such as etch rate to be made without significantly affecting other etch parameters (e.g. CD uniformity, substrate temperature). For example, the relatively small applied magnetic field also minimizes potential damage to circuits on a substrate being etched. Thus, when an azimuthal etch rate non-uniformity is detected in an etching process, such as those induced by film thickness variation, etch chamber hardware and the magnetic field of the plasma, a localized magnetic field above a substrate and generated from the substrate support can be used to make adjustments to an azimuthal etch rate pattern. Similar results can be obtained in other plasma processing such as plasma assisted deposition.

[0028] To apply such a localized magnetic field, at least one current carrying conductor (current loop) may be powered. Figure **2** illustrates a current carrying conductor **150** embedded in a component of a substrate support assembly **100** (FIG. **2A**). When DC current flows through the current carrying conductor **150**, a magnetic field is generated predominantly in a direction perpendicular (FIG. **2B**) to substrate support assembly **100** and substrate **70**. Under operational conditions (e.g., plasma etching), the conductor **150** is operated independently of the other components of substrate support assembly **100**, such as RF to the baseplate **10** and power to the heating plate **40** and voltage to the ESC. The conductor **150** is adapted to generate a DC magnetic field when DC power is supplied thereto by electrical leads running through the body of the component.

[0029] In order to generate small magnetic fields, a plurality of conductors **150** are laterally spaced across the substrate support and/or edge ring at locations suitable to generate applied magnetic fields effective to make corrections and/or adjustments to plasma processing such as an etch rate pattern. The conductors **150** may be located in a component such as an ESC ceramic, such as ceramic plate **60**. The conductors **150** may be located in another component, such as baseplate **10**. The conductors **150** may also be located in hardware adjacent the substrate support, such as an edge ring. Preferably, the current carrying conductors **150** are placed inside baseplate **10**, such that any heat generated due to electrical current flow inside the conductors does not substantially alter the substrate temperature. If incorporated in baseplate **10**, the conductors **150** are preferably wires with an electrically insulating sheath.

[0030] The current carrying conductor **150** may preferably comprise a wire, cable or conductive trace that is electrically isolated from its surroundings to ensure that the applied DC current only flows inside the conductor and not within the substrate support component in which it is embedded. Electrical isolation may be realized by providing a thin electrically insulating layer, or layers, surrounding current carrying conductor **150**. For example, if current carrying conductor **150** is disposed in a component that is electrically conductive, a thin layer, or layers, of electrically insulating material or sheath is disposed around the conductor for electrical isolation. The electrically insulating material may comprise a Kapton film, an epoxy film, a silicone film and combinations thereof. If current carrying conductor **150** is

disposed in a component that is electrically non-conductive, a thin layer, or layers, of electrically insulating material or sheath is not required for electrical isolation. The material of conductor **150** preferably comprises copper, but may be comprised of other materials with a suitable electrical conductivity.

[0031] The conductor **150** may be disposed within a component of a substrate support such that it forms a current loop **150**. The current loop **150** may be formed into any desirable shape within the component and with reference to the plane of the upper surface of the substrate **70** and is preferably circular or semi-circular. Other shapes may be oval, semi-oval, square, rectangular, trapezoidal, triangular or other polygonal shape. If a wire is chosen for conductor **150** to be incorporated in ceramic plate **60**, a wire may be placed at a desired location in a mold containing powder starting materials of the component. The molded component is then fired to form the component. If a conductive trace is chosen for conductor **150**, a powder starting material of the trace may be formed into a pattern in a powder molding, with subsequent firing of the molding to form the component. If a conductive trace is chosen for conductor **150** and is to be placed on an outer surface of a component, a metal or other material may be plated on the component, with subsequent etching of the metal or other material to form the current loop on the component. If an individual wire is chosen as the conductor **150** and is to be formed on an upper surface of a component, a groove may be machined into the surface with dimensions suitable for receiving the wire and the insulated wire can be mounted in the groove with a suitable adhesive.

[0032] The current loop **150** can be supplied DC power by electrical leads connected thereto. Figure **3** shows a perspective view of a substrate support assembly **100** comprising current loop **150** with leads **130** for power supply (up arrow) and power return (down arrow). The current loop **150** is disposed in or on baseplate **10**. The leads are spaced a few mm apart such that the magnetic fields generated on the leads, and particularly those proximate the current loop **150**, cancel each other out and do not interfere in the magnetic field over the substrate **70** being etched (Fig. **2A**).

[0033] A current loop, or loops, may comprise a single turn. However, a current loop, or loops, comprising a plurality of turns to form a coil, or coil-like, structure

are also contemplated. The coil, or coil-like, structure may reduce the DC current required for generating the applied magnetic field during an etching process. The embodiments of the current loop, or loops, are preferably disposed in planes parallel to the substrate. However, the current loop, or loops, may be disposed in planes that are not parallel to the substrate if such a disposition is desired.

[0034] The dimensions of current carrying conductor **150** are not particularly limited so long as the dimensions render its applied magnetic field effective to make corrections and/or adjustments to the plasma to achieve uniform processing such as an azimuthal etch rate pattern. The length of current carrying conductor **150** may be chosen such that the corresponding current loop **150** may be shaped into a desired form. For example, if a 300mm diameter wafer is to be etched, each localized magnetic field can be generated by a single circular shaped current loop formed with a loop diameter between about 1-150mm and preferably between about 1-75mm. Depending on the shape of the current loop and the desired number of currently loops in the substrate support, the length of an individual current loop may be 5-1000mm, e.g., 5-50mm or 50-1000mm, such as in the case of a component comprising up to two hundred current loops. The diameter of current carrying conductor **150** itself is also not particularly limited and may be any diameter or dimension that forms a suitable applied localized magnetic field. For example, if a 300mm diameter wafer is to be etched, the current loop may be a wire with a diameter of between about 0.5mm-10mm and preferably between about 0.5mm-5mm. If a conductive trace is to be the current loop **150**, the trace may be formed in a rectangular shape with a thickness of between about 0.5mm-10mm, preferably between about 0.5mm-5mm, and a width of between about 0.5mm-10mm, preferably between about 0.5mm-5mm. The direction of current flowing in the current loop is not particularly limited and may be either clockwise or counter-clockwise. Preferably, the current flowing in current loop **150** is adapted to be reversible to switch the direction of the current flow, and thus, switching the direction of the applied DC magnetic field, if desired.

[0035] For purposes of explanation, Figure **2** shows an embodiment of a component of a substrate support assembly **100** comprising a single current loop **150**. However, to provide localized magnetic fields it is desirable to have a plurality

of current loops **150** in the substrate support. A plurality of current loops **150** allows for reduction of DC current required for a localized magnetic field strength over a substrate. An advantage of a plurality of current loops **150** is that each loop can be operated independently of one another such that each current loop may be supplied varying power levels and processing non-uniformity can be corrected and/or adjusted more efficiently. If each of the current loops **150** in the plurality of current loops is independently operable, further fine tuning capabilities are imparted to the applied magnetic field over the substrate. Preferably, the plurality of current loops **150** are connected to one or more DC power sources controlled by a controller such that the loops can be supplied power at the same or different times with the same or different power levels. Preferably, the DC power source, or sources, comprise a multiplexed powering scheme and can supply power to each current loop 150 such that each loop can be individually tuned by time-domain multiplexing. Preferably, the periphery of each current loop **150** in a plurality of current loops is laterally offset from the periphery of an adjacent current loop such that no overlap occurs. Preferably, the plurality of current loops **150** are disposed in a laterally symmetric or equidistant manner such that a plane that vertically intersects the center of the component where the loops are disposed produces substantial mirror images of each half of the component. The current loops 150 in the component are preferably arranged in a defined pattern, for example, a rectangular grid, a hexagonal grid, a polar array or any desired pattern.

[0036] Figure **4** shows a preferred embodiment of a component of a substrate support assembly **100** wherein substrate support **100** comprises a plurality of current loops **150**. Figure **4** shows a preferred embodiment having two separate current loops **150** which are D-shaped and having their straight legs facing each other. The current loops **150** may be of the same size or may be of different sizes. Preferably, each of the current loops **150** extends less than about halfway around the support or edge ring. The current loops **150** are shown as being disposed towards a peripheral area of the substrate support component, but may also be disposed at any radial position desired. When the currents of these two loops are applied in the same direction (e.g., both clockwise or both counter-clockwise), a magnetic field similar to that shown in Figure **2A** is generated. When the currents of the two loops are

applied in opposite directions (e.g., one clockwise and one counter-clockwise), certain portions of the applied magnetic field are cancelled over the center of the substrate.

[0037] Figure **5** shows a preferred embodiment of a component of a substrate support assembly **100** wherein a substrate support **100** comprises multiple current loops **150**. Figure **5** shows a preferred embodiment with four separate current loops **150** which are each D-shaped and having their straight legs facing inward. Similar to those shown in Figure **4**, the current loops **150** are shown as being disposed towards a peripheral area of the substrate support component, but may also be disposed at any radial position desired. The four current loops **150** are capable of generating applied magnetic fields in various directions over the substrate depending on the direction of the current in each of the four loops **150**, similar to the applied magnetic field generated by the two separate loops in Figure **4**.

[0038] Figure **6** shows an embodiment of a component of a substrate support assembly **100** having circular current loops wherein controlling the direction of current in various current loops **150**, more complex magnetic field patterns can be generated over the substrate. The embodiment of Figure **6** comprises nine separate current loops **150**, with eight outer current loops surrounding a center current loop. If desired, the total number of current loops **150** may be significantly more than nine, and can be as high as about two hundred. The more current loops **150**, the more fine tuning capability imparted to the applied magnetic field over the substrate.

[0039] Figure **7** shows an embodiment of a substrate support assembly **100** wherein a component adapted to surround a substrate support **100** comprises at least one current loop **150**, and wherein substrate support **100** does not comprise a current loop. The generation of the magnetic field from the component compensates for non-uniformity at the outermost edge of substrate **70**. Figure **7** shows an embodiment wherein an edge ring **110** comprises two current loops **150** disposed in a plane substantially parallel to an upper surface of substrate **70**. The current loops **150** are formed into a block semi-circular shape that substantially surround substrate support **100** and are disposed on opposite sides of edge ring **110**. The loops are independently operated with respect to each other such that two magnetic fields can be generated. The major legs of the current loops can be on the same or different

planes. Figure **8** shows a perspective view of current loop **150** disposed in edge ring **110**. The loop includes major legs which are vertically offset with electrical leads **130** for power supply (up arrow) and power return (down arrow). The leads are spaced a few mm apart such that the magnetic fields generated on the leads, and particularly those proximate the current loop **150**, cancel each other out and do not interfere in the magnetic field over the substrate **70** being etched (Fig. **2A**). If desired, edge ring **110** may comprise more than two current loops **150**. Figure **9** shows an embodiment wherein edge ring **110** comprises four current loops **150** and wherein substrate support **100** does not comprise any current loops. Each of the four current loops **150** are arranged diametrically opposite to another one of the loops **150**.

[0040] Figure **10** shows an embodiment of a component of a substrate support assembly **100** wherein both substrate support **100** and a component **110** surrounding the substrate support comprise at least one current loop **150**. Adding at least one current loop **150** to such hardware, such as edge ring **110** surrounding the substrate support **100**, extends the influence of the applied magnetic field over the substrate to the outermost edge of substrate **70**. In the embodiment of Figure **10**, the substrate support **100** and edge ring **110** each comprise two current loops **150**. The current loops incorporated in the substrate support are D-shaped with the straight legs facing each other. The current loops incorporated in the edge ring are offset 90° with respect to the current loops of the substrate support. The current loops **150** in the substrate support **100** and edge ring **110** may or may not be planar with respect to each other or with respect to a substrate surface. The current loops **150** in the edge ring **110** preferably extend around a substantial portion of its circumference.

[0041] The number of current loops **150** that the substrate support assembly **100** comprise may be greater than two, such as that shown in Figure **11,** wherein both substrate support **100** and edge ring **110** each comprise four current loops **150**. Figure **12** shows an embodiment of a substrate support assembly 100 wherein the support comprises nine current loops **150** and edge ring **110** comprises twelve current loops **150**. The current loops **150** comprised in the substrate support or edge ring are laterally distributed in a symmetric manner.

[0042] The current loops can be incorporated in any type of substrate support which may or may not include an electrostatic clamping arrangement, heating arrangement and/or temperature controlled baseplate. In a preferred method of controlling and/or adjusting an etch rate pattern using a substrate support incorporating current loops, a substrate is supported on a substrate support comprising a baseplate, a thermal insulating layer disposed over the baseplate, a heating plate disposed over the thermal insulating layer, a ceramic plate disposed over the a thermal insulating layer; and current loops; etching a substrate disposed on the substrate support; detecting an etch rate non-uniformity, such as an azimuthal etch rate non-uniformity, after etching has been initiated; and providing one or more of the current loops with DC power to generate localized DC magnetic fields that correct and/or adjust the etch rate non-uniformity.

[0043] An azimuthal etch rate non-uniformity may be detected as follows. A substrate comprising a thin film, such as a polysilicon thin film in the case of semiconductor substrate, to be processed is inspected to determine the thickness of the thin film at various locations across the substrate using standard interferometry techniques. The substrate is then plasma etched, or partially etched. After etching, or partial etching, the thickness of the thin film is measured again using standard interferometry techniques. The difference between the two thin film thickness measurements is determined by an appropriate algorithm, which also is able to generate an etch pattern on the substrate surface. From an etch rate pattern, a mean depth of the film thickness left on the substrate is determined, along with other parameters, such as the standard deviation and global maximum and minimum depths. These parameters are used to determine where selective application of a magnetic field can be applied to correct and/or adjust an azimuthal etch rate non-uniformity during subsequent etching of a batch of wafers undergoing the same etch process.

[0044] Alternatively, incoming wafer thickness of a substrate can be measured, the B-field pattern to provide uniform etching can be determined, and etching of a batch of substrates can be carried out. In another method, a substrate can be etched, an azimuthal pattern for etching can be determined, the magnetic field compensation is determined and further substrates are etched while applying the magnetic field

compensation. The etch rate or other parameters could be monitored during plasma etching and the current loops could be powered to compensate for local etch rate variation during the plasma etch process.

EXAMPLE 1

[0045] A silicon wafer with a 1μm thick silicon oxide film on its surface to be etched to a depth of about 400nm is surrounded by an edge ring with two current loops, similar to the configuration of Figure **7**, wherein the supply trace and return trace are non-planar. Etching can be carried out using a fluorocarbon etching gas. The substrate is loaded into a plasma etch vacuum chamber and is partially etched to a depth of about 200nm and then removed from the chamber. Interferometric techniques are used to determine the etch rate non-uniformity by measuring the film thickness profile over the substrate before and after partial etching. From these measurements, an algorithm is used to generate the etch rate pattern. After analysis of the pattern, parameters used to determine corrections and/or adjustments to be carried out to the azimuthal etch rate non-uniformity are determined. The partial etch is determined to result in average depth in the film of 192.4nm, with a three-sigma standard deviation of 19.2nm (10%). The difference between a global maximum and minimum is 31.9nm (16.6%). Analysis of the etch rate pattern is shown in Figure **13**. Areas **190** (in black) on substrate **70** are shown to be etched with a faster etch rate than areas **180** (in gray).

[0046] Etching the remaining portions of the film on substrate **70** is then carried out. During the subsequent etching, DC power is supplied to the current loops **150** disposed in edge ring **110**. DC power is supplied such that an 3 Gauss magnetic field is generated by the loops **150**. After completion of etching, the etch rate pattern is determined, as described above. This etch results in an average of 189.5nm of film thickness removed, with a three-sigma standard deviation of 13.9nm (7.3%). The difference between a global maximum and minimum is 25.2nm (13.3%). Analysis of the etch rate pattern is shown in Figure **14**. Areas **190** (in gray) on substrate **70** are shown to be etched with a slower etch rate than areas **180** (in black).

[0047] Thus, etching a substrate in the presence of an applied DC magnetic field can compensate for etch rate non-uniformity and thus provide a more uniform etch rate. With an applied magnetic field of about 3 Guass generated from current loops in an edge ring, azimuthal etch rate non-uniformity can be decreased by about 3.3% (range after partial etch - range after final etch), with a decrease in the three-sigma standard deviation of about 2.7% (deviation after partial etch - deviation after final etch). Furthermore, application of an 3 Gauss magnetic field shows that areas etched at a faster etch rate in the partial etch can be etched at a slower etch rate in the final etch step, thus, correcting for an azimuthal etch rate non-uniformity. Similarly, application of an 3 Gauss magnetic field shows that the areas that are etched at a slower etch rate in the partial etch can be etched at a faster etch rate in the final etch step, thus, correcting for an azimuthal etch rate non-uniformity.

EXAMPLE 2

[0048] In a process scheme to compensate for etch rate variation:

a. a wafer is partially etched and the etch rate non-uniformity is measured;

b. apply a magnetic field pattern to the plasma above a wafer (based on historical knowledge);

c. etch another wafer, determine etch pattern sensitivity to the applied magnetic field pattern since the applied field is known; and

d. optionally repeat steps a-c to determine an optimal magnetic field pattern.

EXAMPLE 3

[0049] In a process scheme to compensate for incoming wafer thickness variation:

a. measure incoming wafer thickness variation;

b. apply a magnetic field pattern (based on historical knowledge);

c. etch a wafer, determine etch pattern sensitivity to the applied magnetic field pattern since the applied field is known; and

d. optionally repeat steps a-c and adjust the applied magnetic field pattern if necessary.

[0050] All of the above-mentioned references are herein incorporated by reference in their entirety to the same extent as if each individual reference was specifically and individually indicated to be incorporated herein by reference in its entirety.

[0051] While the invention has been described with reference to preferred embodiments, it is to be understood that variations and modifications may be resorted to as will be apparent to those skilled in the art. Such variations and modifications are to be considered within the purview and scope of the invention as defined by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A component of a substrate support assembly useful for supporting individual semiconductor substrates undergoing plasma processing, the component comprising:

a substrate support on which the semiconductor substrate can be supported during plasma processing thereof and/or an edge ring which surrounds the semiconductor substrate;

a plurality of current loops incorporated in the substrate support and/or the edge ring, the current loops being laterally spaced apart and extending less than halfway around the substrate support or edge ring, each of the current loops being operable to induce a localized DC magnetic field of field strength less than 20 Gauss above a substrate supported on the substrate support during plasma processing of the substrate.

2. The component of Claim 1, wherein the substrate support includes a baseplate, a thermal insulating layer above the baseplate, and a ceramic plate with embedded electrostatic chucking electrode above the thermal insulating layer; and the current loops are embedded in the baseplate or the ceramic plate such that the current loops lie substantially in a plane parallel to an upper surface of the semiconductor substrate.

3. The component of Claim 1, wherein the current loops are embedded in the edge ring such that the current loops lie substantially in a plane parallel to an upper surface of the semiconductor substrate.

4. The component of Claim 1, wherein up to 200 current loops of the same size and having a circular shape are embedded in the substrate support or the edge ring.

5. The component of Claim 1, wherein each of the current loops has a circular, semi-circular, oval, semi-oval, square, rectangular, trapezoidal, triangular or polygonal shape.

6. The component of Claim 1, wherein each current loop in the plurality of current loops is a wire formed into a loop having a diameter of between about 0.5-10mm.

7. The component of Claim 1, wherein a periphery of each current loop in the plurality of current loops is laterally offset from a periphery of an adjacent current loop.

8. A plasma processing chamber incorporating the component of Claim 1, wherein the substrate support includes a heater layer having a plurality of heaters laterally distributed across the substrate support and operable to tune a spatial temperature profile for critical dimension (CD) control, the substrate support including at least 9 current loops distributed laterally across the substrate support and operable to compensate for local non-uniformity in processing on the semiconductor substrate.

9. The plasma processing chamber of Claim 8, wherein the plasma processing chamber is a plasma etching chamber.

10. The plasma processing chamber of Claim 8, wherein the current loops are connected to one or more DC power sources controlled by a controller such that the current loops can be supplied DC power at the same time or different times with the same or different power levels and the current flow in the current loops is in the same direction or different directions.

11. A method of controlling and/or adjusting a magnetic field pattern during plasma processing of a semiconductor substrate undergoing processing in the plasma processing chamber of Claim 8, comprising:

a) supporting a semiconductor substrate on the substrate support;

b) plasma processing the semiconductor substrate; and

c) supplying at least one of the current loops with DC power to generate a localized DC magnetic field in a region above the semiconductor substrate so as to compensate for local non-uniformity in processing.

12. The method of Claim 11, wherein the current loops are supplied different amounts of DC power with current travelling in a clockwise direction in each of the current loops.

13. The method of Claim 11, wherein the current loops are supplied different amounts of DC power with current travelling in different directions in some of the current loops.

14. The method of Claim 11, wherein each of the current loops generates a localized magnetic field above the semiconductor substrate with a field strength of less than 1 Gauss.

15. The method of Claim 14, wherein the field strength is less than 0.5 Gauss.

16. The method of Claim 11, wherein the substrate support is surrounded by an edge ring having at least two current loops with each of the current loops arranged on an opposite side of the edge ring.

17. The method of Claim 16, wherein the edge ring has at least four current loops with each of the current loops arranged diametrically opposite to another one of the current loops and each of the current loops has a circular, semi-circular, oval, semi-oval, square, rectangular, trapezoidal, triangular or polygonal shape.

18. The method of Claim 11, wherein the plasma processing is plasma etching and further comprising, after steps a) and b) and prior to step c):

removing the semiconductor substrate from the chamber;

detecting an etch-rate non-uniformity in an etch-rate pattern on the semiconductor substrate; and

modifying step c) so as to compensate for film thickness induced etch-rate non-uniformity, etch chamber induced etch-rate non-uniformity or plasma induced etch-rate non-uniformity.

19. The method of Claim 11, wherein the DC power is supplied from at least one DC power source comprising a multiplexed power scheme.

20. The method of Claim 11, wherein the substrate support is adapted to support a substrate having a diameter of at least about 200mm, at least about 300mm or at least about 450mm.

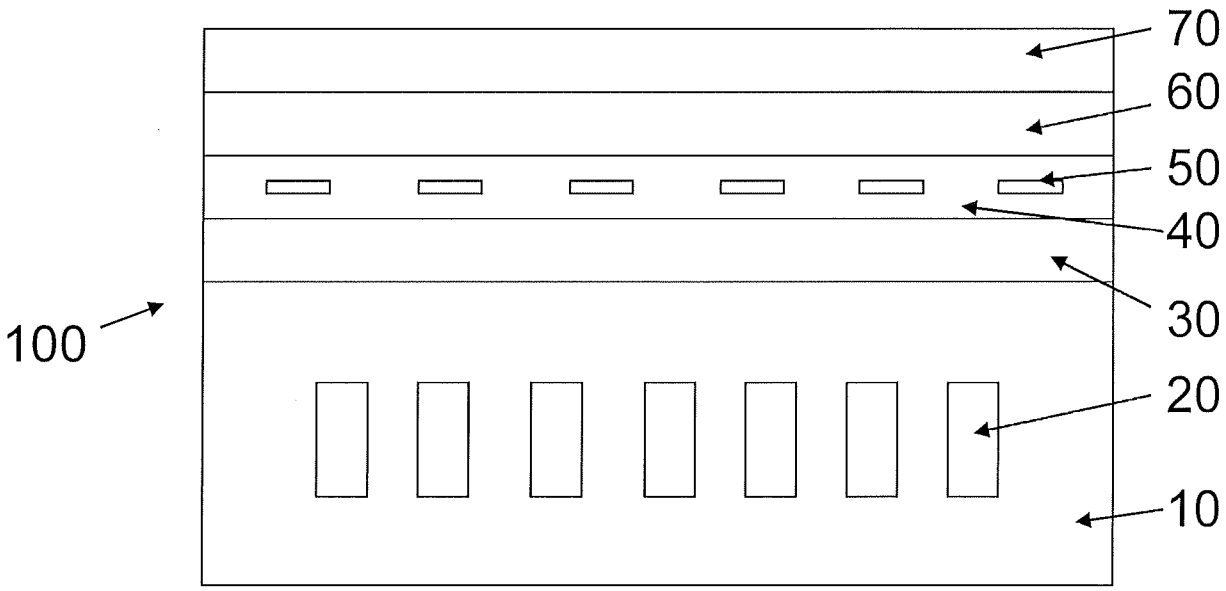

Figure 1

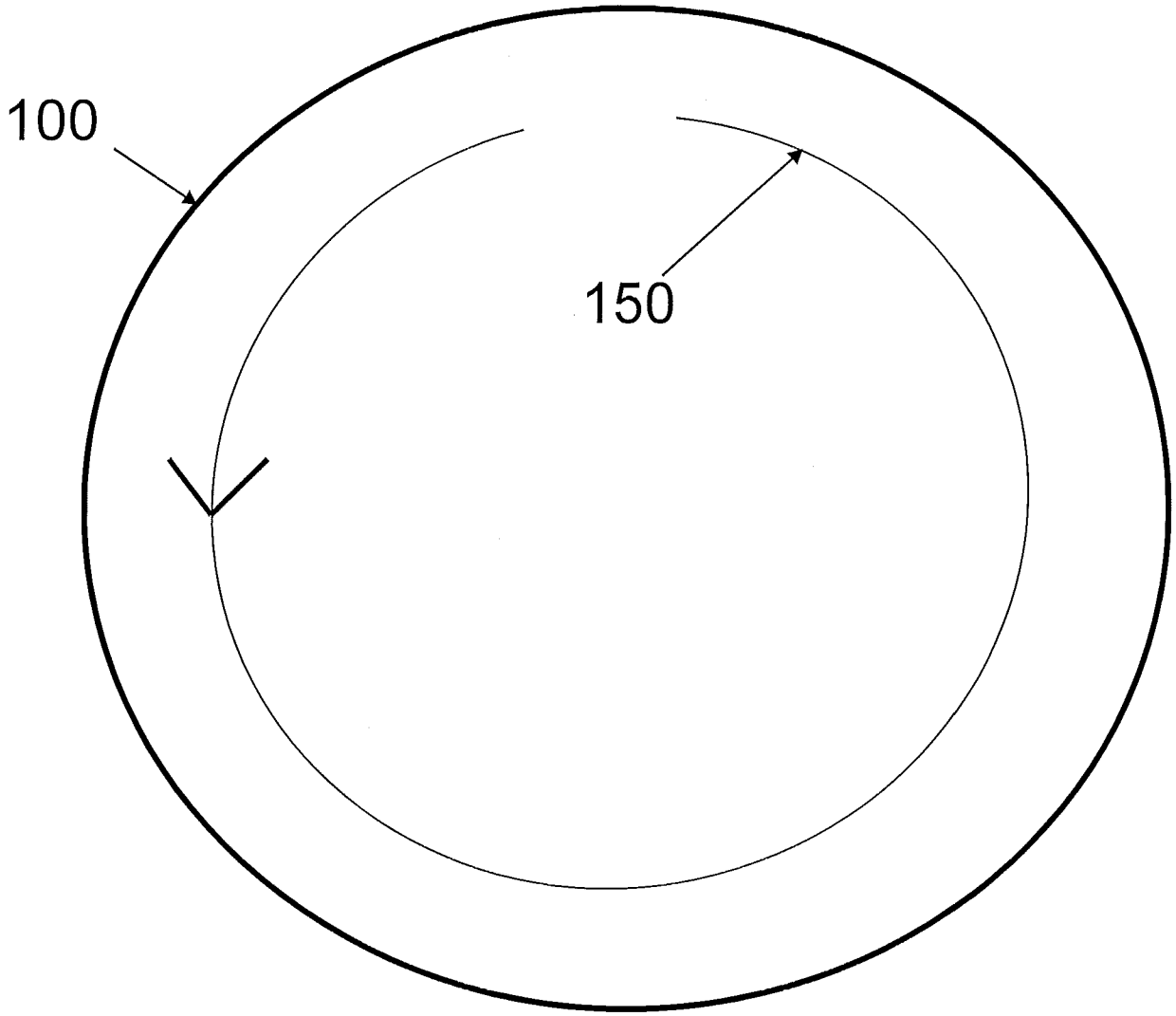

Figure 2A

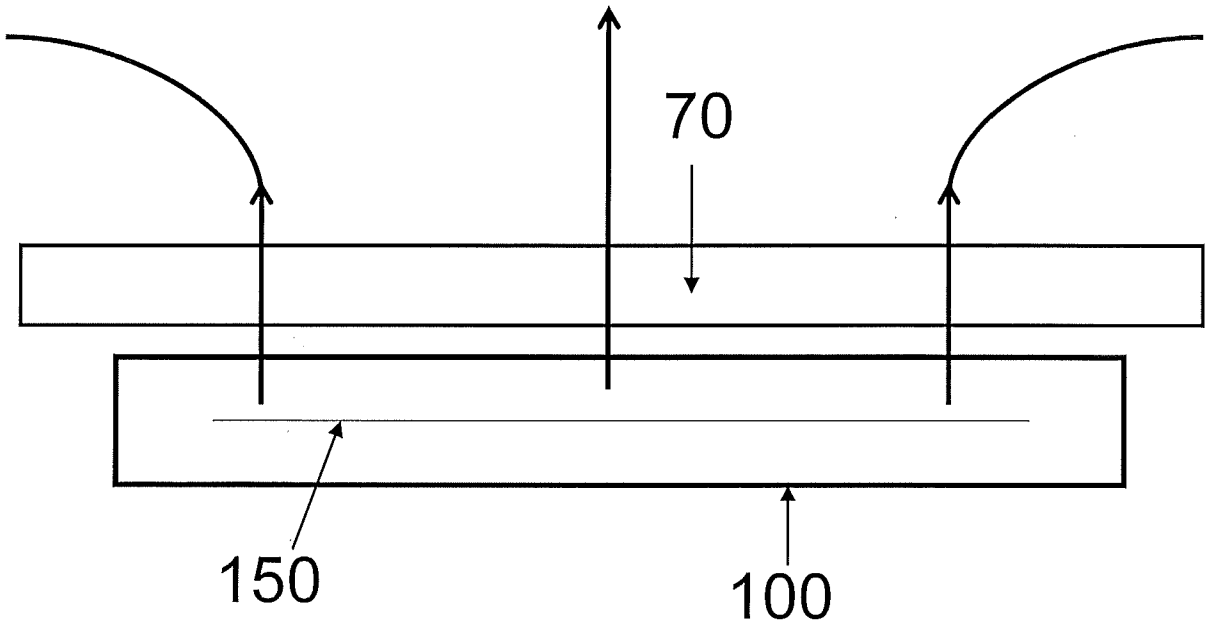

Figure 2B

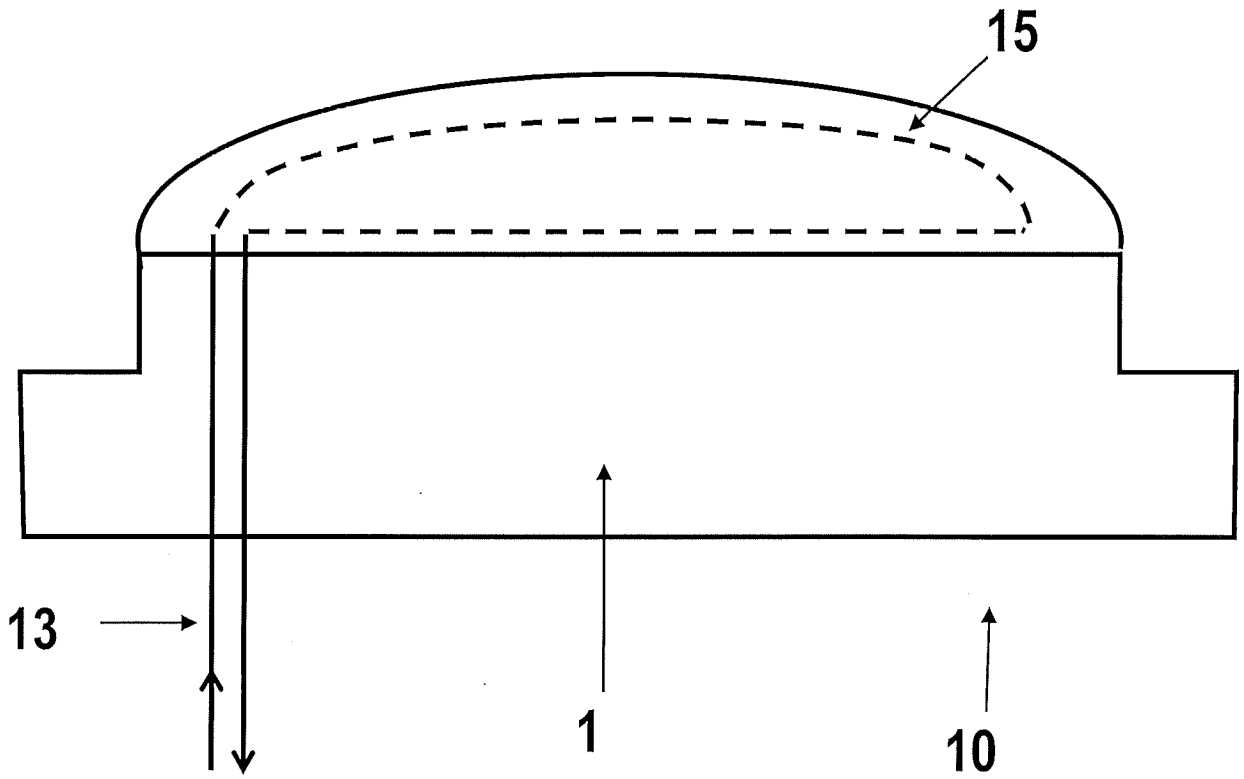

Figure 3

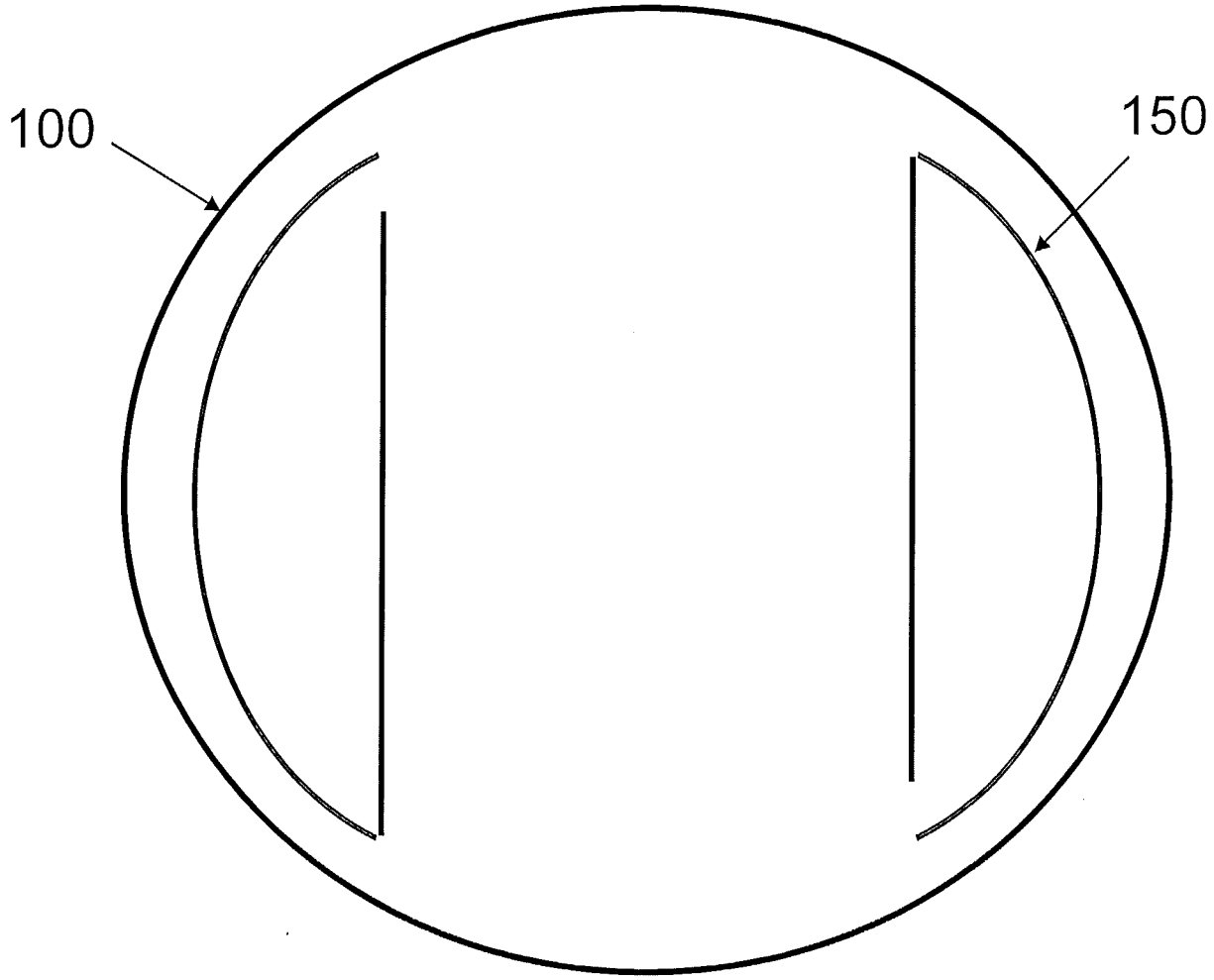

Figure 4

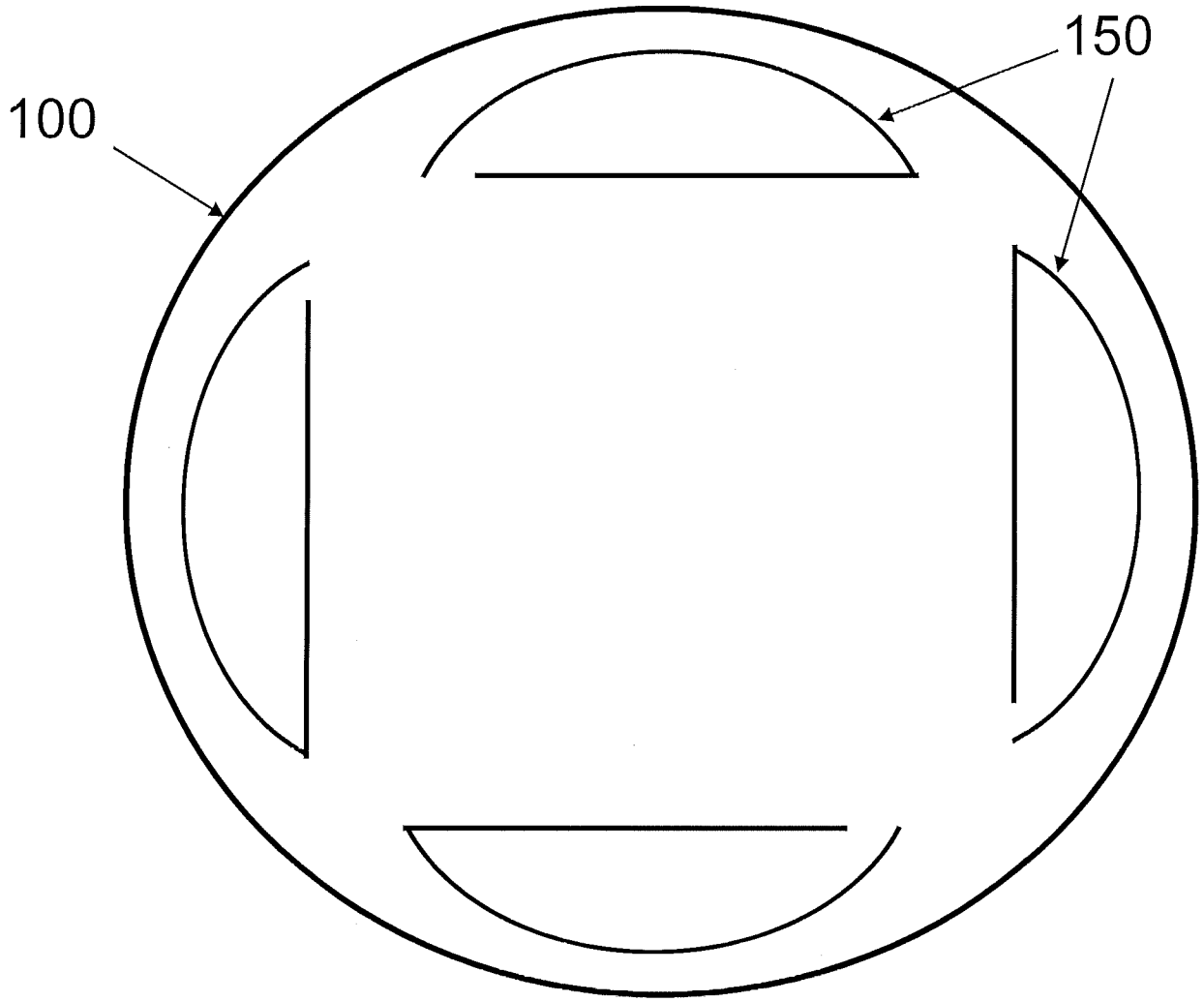

Figure 5

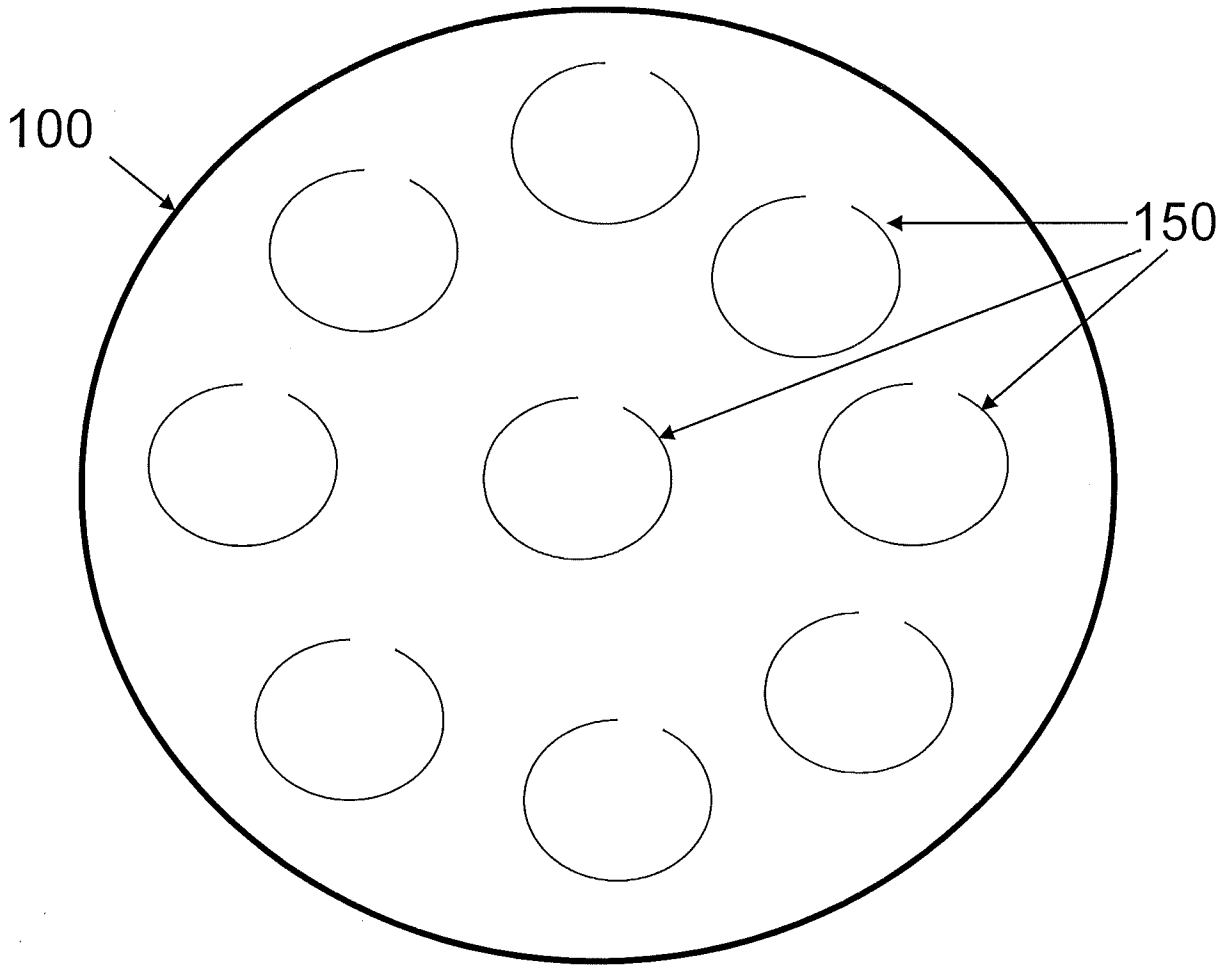

Figure 6

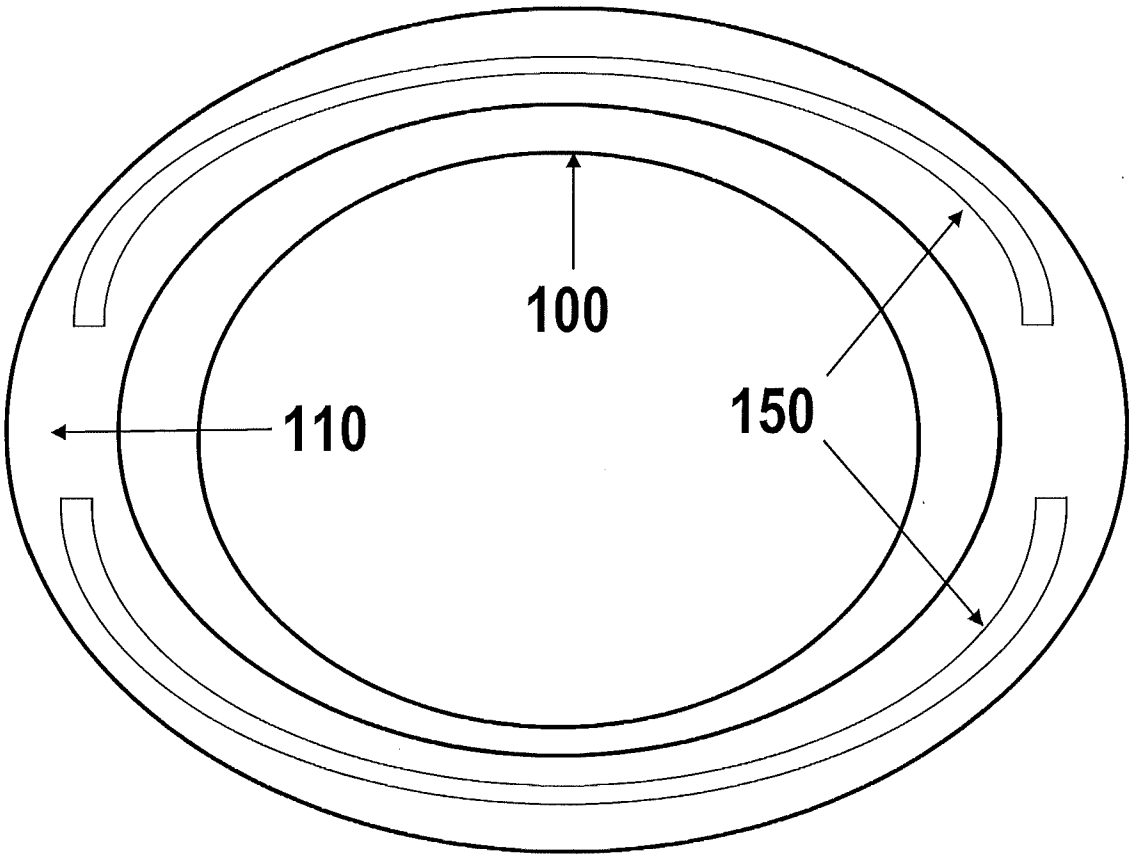

Figure 7

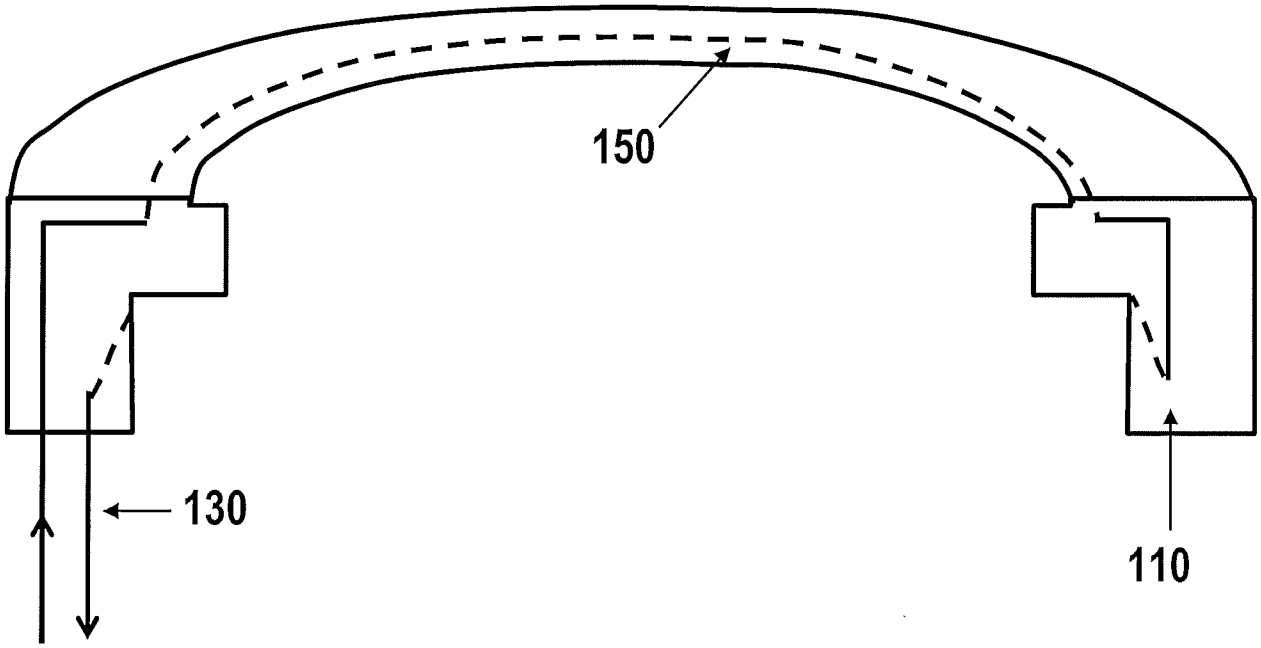

Figure 8

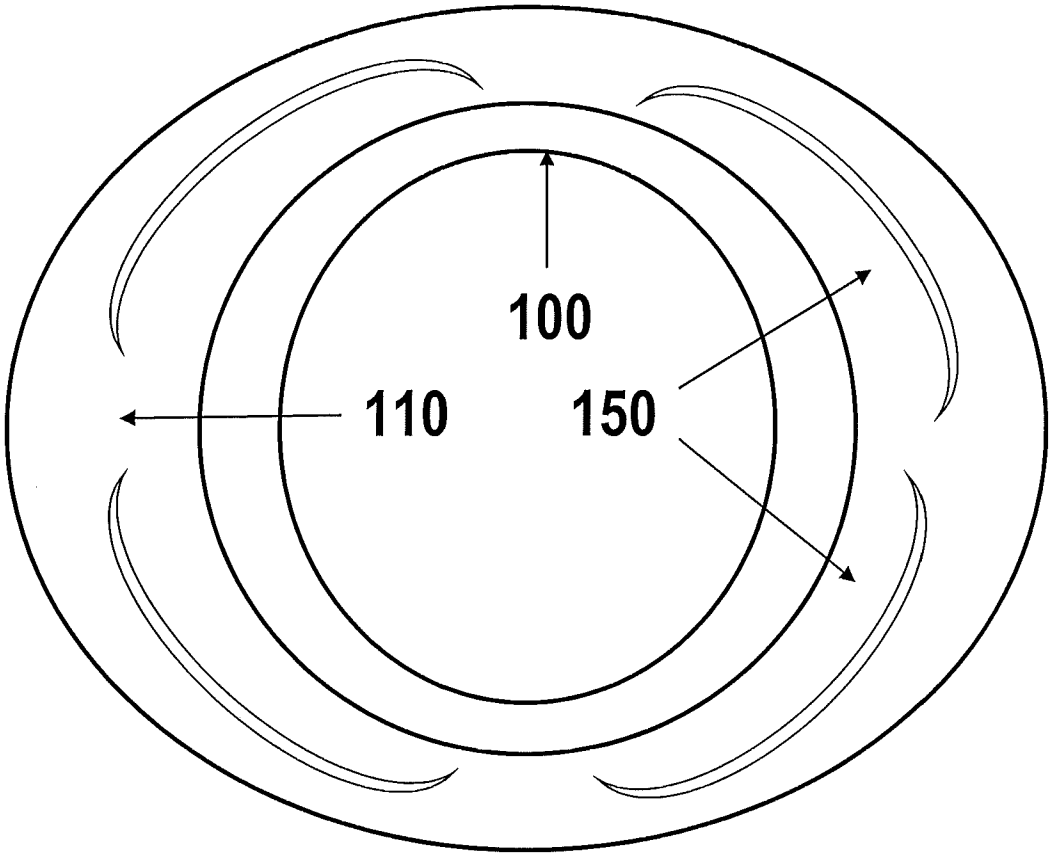

Figure 9

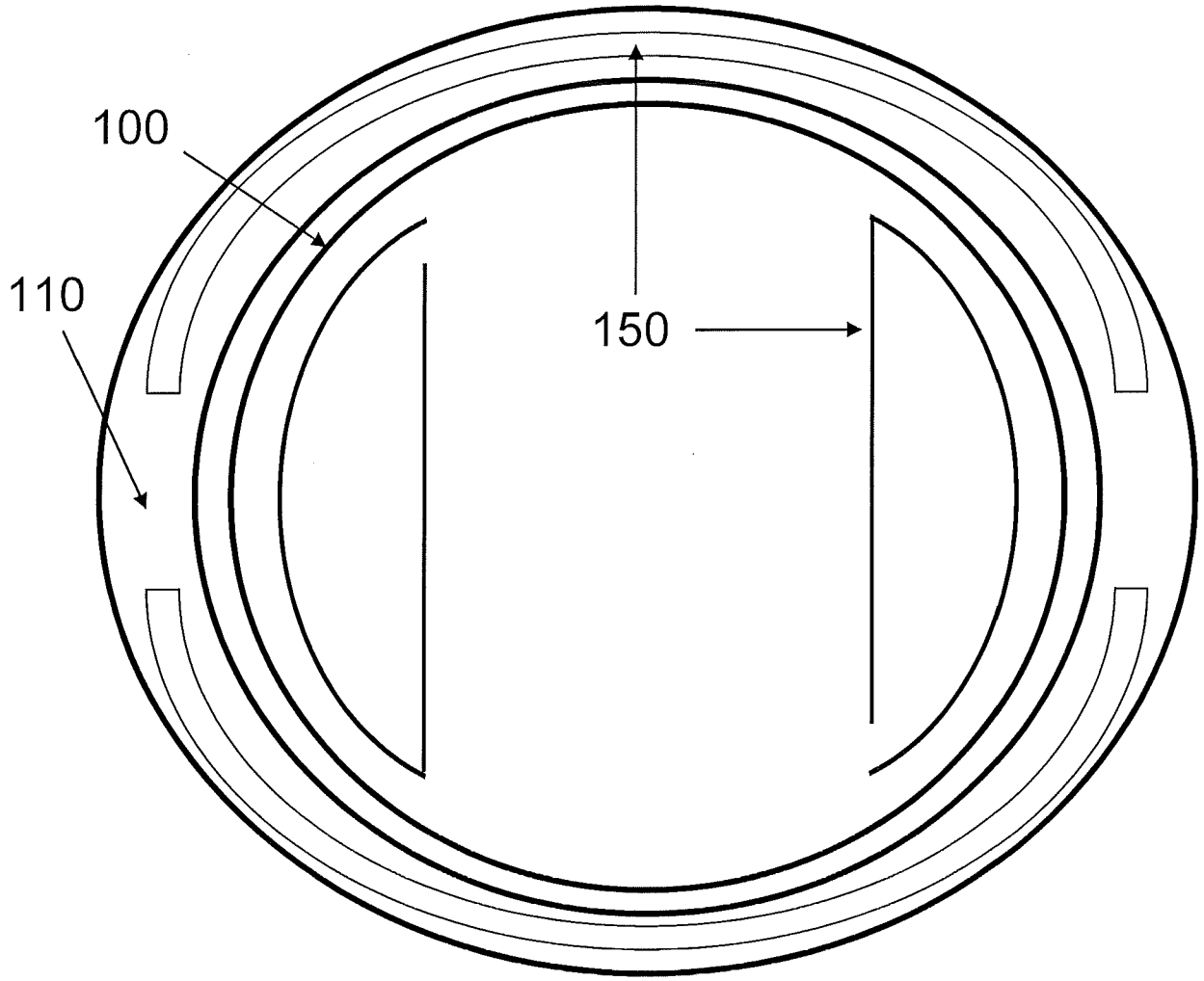

Figure 10

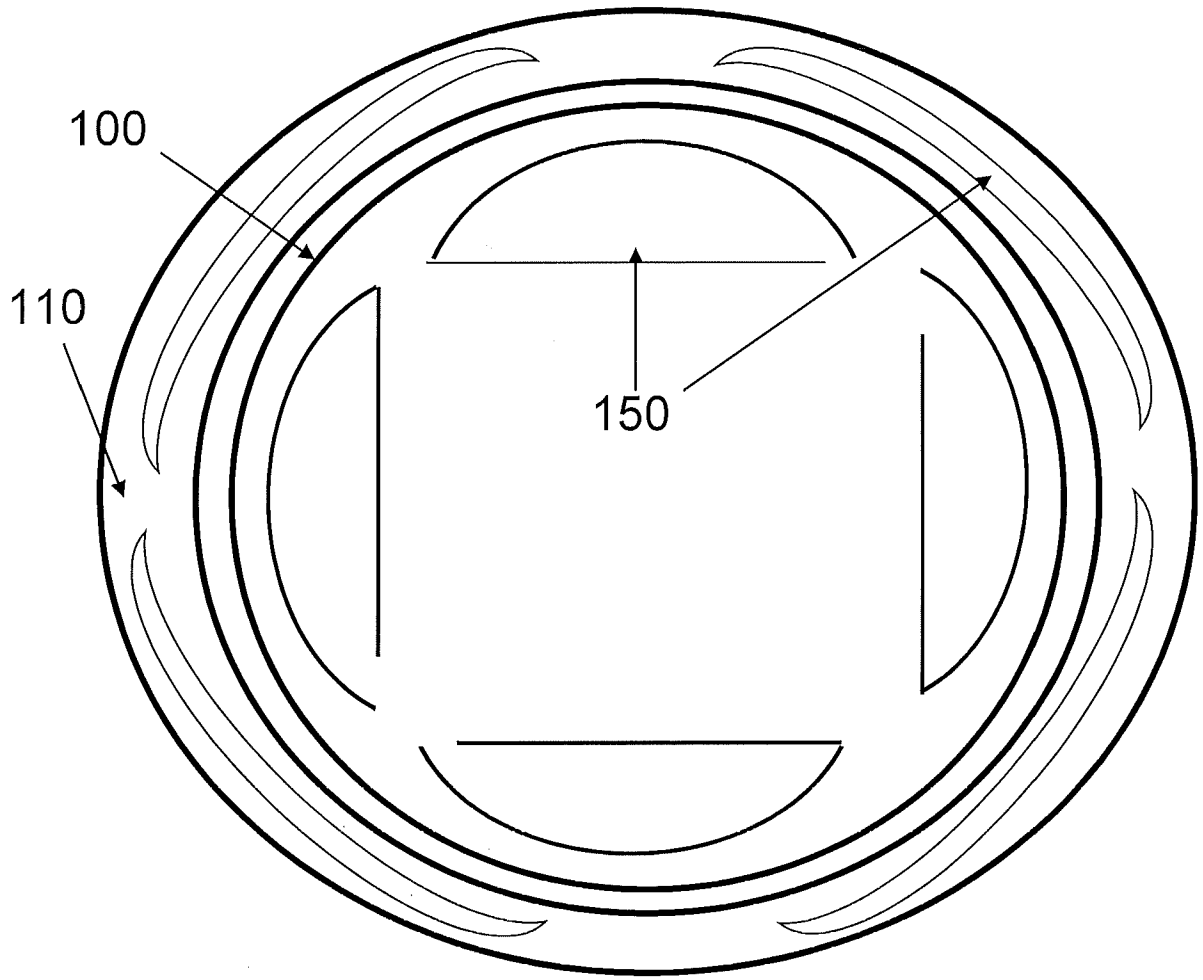

Figure 11

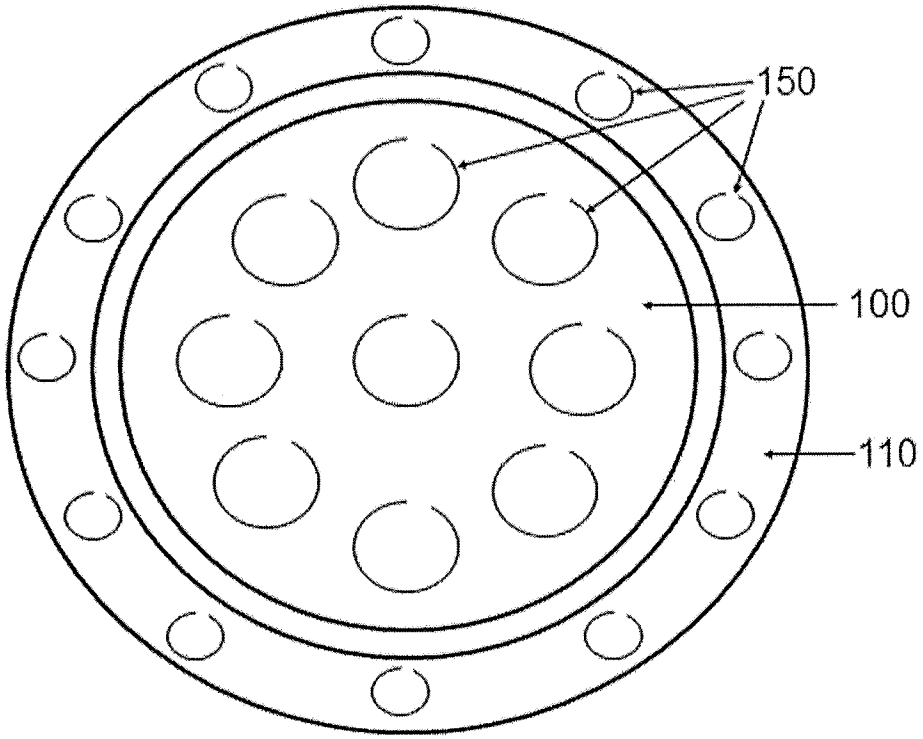

Figure 12

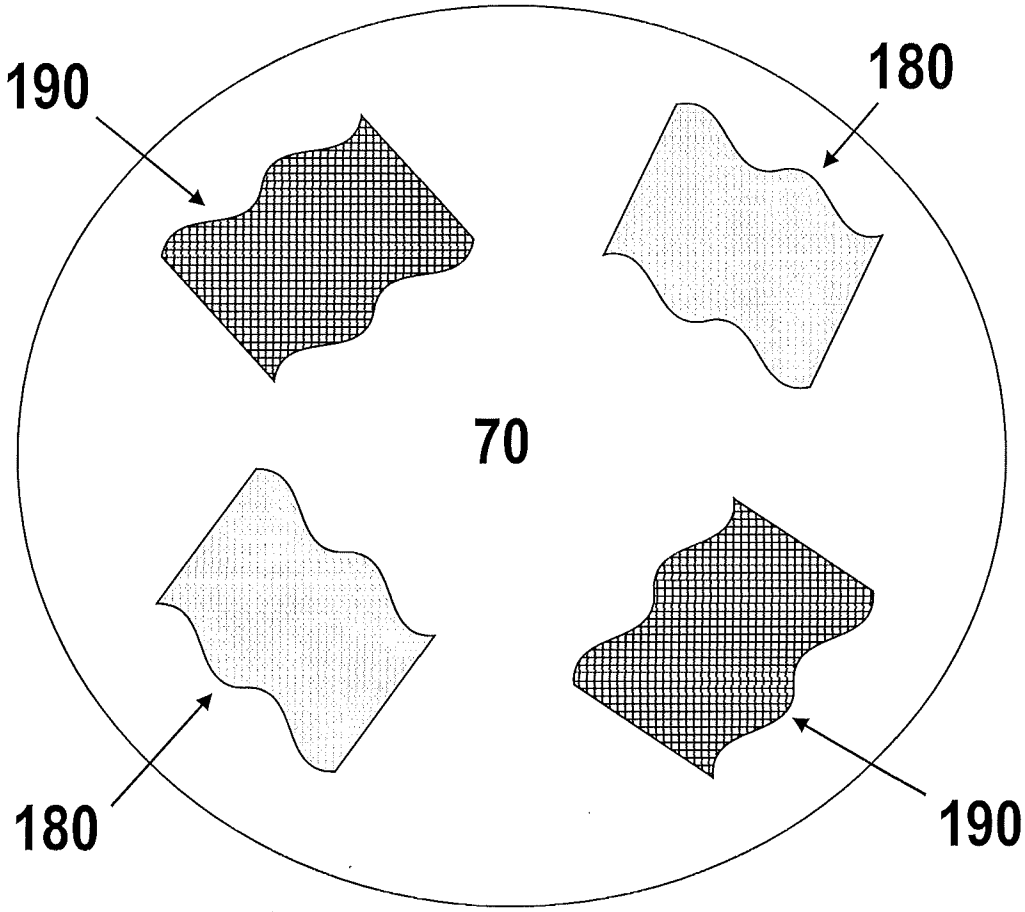

Figure 13

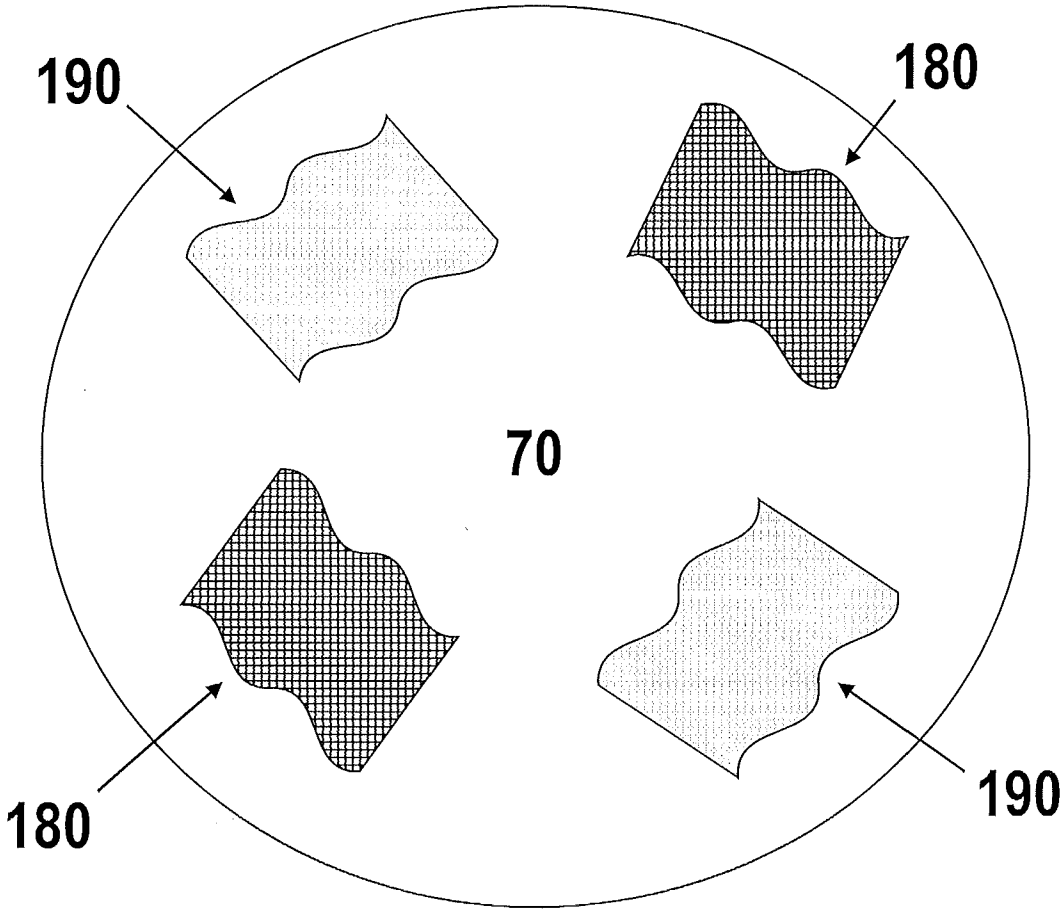

Figure 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/053386

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - C23C 16/00 (2012.01)
USPC - 118/728
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - C23C 16/00, 16/50; B23B 31/28 (2012.01)
USPC - 118/728, 725, 723R, 723I; 279/128

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Proquest, Orbit.com, Google Patents

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0092072 A1 (SINGH et al) 21 April 2011 (21.04.2011) entire document	1-20
Y	US 2005/0016465 A1 (RAMASWAMY et al) 27 January 2005 (27.01.2005) entire document	1-20
Y	US 6,095,084 A (SHAMOUILIAN et al) 01 August 2000 (01.08.2000) entire document	1-20
Y	US 6,475,336 B1 (HUBACEK) 05 November 2002 (05.11.2002) entire document	3, 16-17
Y	US 2009/0173445 A1 (YEOM et al) 09 July 2009 (09.07.2009) entire document	4
Y	US 2009/0000738 A1 (BENJAMIN) 01 January 2009 (01.01.2009) entire document	8-20
Y	US 6,175,175 B1 (HULL) 16 January 2001 (16.01.2001) entire document	12-13
Y	US 2006/0191637 A1 (ZAJAC et al) 31 August 2006 (31.08.2006) entire document	18
Y	US 2008/0202924 A1 (BLUCK et al) 28 August 2008 (28.08.2008) entire document	19
A	US 5,886,866 A (HAUSMANN) 23 March 1999 (23.03.1999) entire document	1-20
A	US 6,523,493 B1 (BRCKA) 25 February 2003 (25.02.2003) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 October 2012	16 NOV 2012

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774