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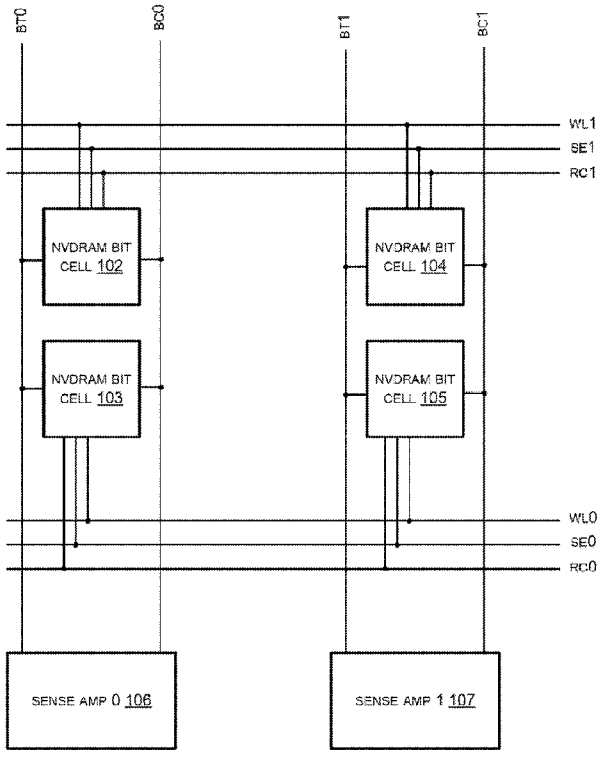

FIG. 1

(57) Abstract: A memory circuit includes a single transistor storing both volatile and nonvolatile bit charges. The single transistor may comprise a SONOS transistor or a Floating-Gate transistor. A method of operating a combined volatile and nonvolatile memory circuit may comprise causing a first charge representing a nonvolatile bit to be stored in a charge trapping region of a transistor; and causing a second charge representing a volatile bit to be stored outside the charge trapping region of the transistor. A device may comprise a processor coupled to interact with a memory system, the memory system comprising an array of memory cells each storing a single volatile bit and a single nonvolatile bit, each cell employing a single transistor to store the volatile bit and to store the nonvolatile bit.

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3T HIGH DENSITY NVDRAM CELL

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[0001] TECHNICAL FIELD

[0002] The present disclosure relates to electronic memory cells.

[0003] BACKGROUND

[0004] High speed volatile and non-volatile storage of data is an important feature in computer systems. Present solutions use specialized volatile memory technologies, like DRAM and SRAM with non volatile back up memories, such as BBSRAM, EEPROM and FLASH. In case of power loss significant amounts of volatile data may have to be stored in the non-volatile memory. This is typically done via signaling interfaces between volatile and nonvolatile memory regions, the interfaces having limited parallelism, high current requirements, and possibly using multiple processor cycles to manage the data transfer. A faster and less power intensive solution is nvSRAM memories, where each volatile cell is paired with a non-volatile cell and data may pass from one region to another without first being placed on a bus or other signaling interface. One disadvantage of present nvSRAM circuits is their limited density and relatively large memory cell size, typically involving 12 high and low voltage transistor.

[0005] BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In the drawings, the same reference numbers and acronyms identify elements or acts with the same or similar functionality for ease of understanding and convenience. To easily identify the discussion of any particular element or act, the most significant digit or digits in a reference number refer to the figure number in which that element is first introduced.

[0007] Figure 1 is a block diagram of an embodiment of a memory system including combined volatile nonvolatile bit cells.

[0008] Figure 2 is a block diagram of an embodiment of a combined volatile nonvolatile bit cell in more detail.

[0009] Figure 3 is an illustration of an embodiment of a combined volatile nonvolatile charge cell.

[0010] Figure 4 is a time line diagram of an embodiment of a volatile READ operation.

[0011] Figure 5 is a time line diagram of an embodiment of a volatile WRITE operation.

[0012] Figure 6 is a time line diagram of an embodiment of a nonvolatile STORE operation.

[0013] Figure 7 is a time line diagram of an embodiment of a nonvolatile RECALL operation.

[0014] Figure 8 is a time line diagram of an embodiment of a nonvolatile ERASE operation.

[0015] Figure 9 is a block diagram of an embodiment of a device system including a combined volatile nonvolatile memory.

[0016] DETAILED DESCRIPTION

[0017] References to "one embodiment" or "an embodiment" do not necessarily refer to the same embodiment, although they may.

[0018] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "above," "below" and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. When the claims use the word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

[0019] "Logic" refers to signals and/or information that may be applied to influence the operation of a device. Software, hardware, and firmware are examples of logic. Hardware logic may be embodied in circuits. In general, logic may comprise combinations of software, hardware, and/or firmware.

[0020] Those skilled in the art will appreciate that logic may be distributed throughout one or more devices, and/or may be comprised of combinations of instructions in memory, processing capability, circuits, and so on. Therefore, in the interest of clarity and correctness logic may not always be distinctly illustrated in drawings of devices and systems, although it is inherently present therein.

[0021] Embodiments comprising SONOS transistors are described herein. It should be appreciated that other types of nonvolatile storage elements may be employed, such as silicon nitride oxide semiconductor (SNOS) transistors, floating gate transistors, ferroelectric transistors, and capacitors, to name a few.

[0022] Figure 1 is a block diagram of an embodiment of a memory system including combined volatile nonvolatile bit cells. The system, which may be arranged as an array of cells, comprises bit cells **102 - 105**. The array comprises sense amplifiers **106** and **107.** Data is presented to and retrieved from cells **102-105** using bit lines BT0 and BT1, and compliment bit lines BC0 and BC1. Signal paths SE0 and SE1 are used for ERASE and STORE operations on nonvolatile memory. Signal paths RC0 and RC1 are also used for operations on nonvolatile memory, RECALL in particuar. The word lines WL0 and WL1 are activated for both volatile and nonvolatile operations, to couple internal structures of the cells **102-105** with the bit lines and their complement lines.

[0023] Each memory cell **102 - 105** acts to store a volatile and non-volatile memory bit. Additionally, each memory bit cell **102 – 105** acts to store a compliment to the volatile and nonvolatile memory bits. During some operations, such as READ, WRITE, and STORE, the sense amplifiers **106** and **107** may react to differential voltages on the bit lines BTx and complement bit lines BCx to drive the bit line voltage levels to unambiguous logical zeros and ones. During other operations, such as RECALL, the sense amplifiers **106** and **107** may react to current flows on the bit lines BTx and complement bit lines BCx to drive the bit line voltage levels to unambiguous logical zeros and ones.

[0024] The array provides both volatile and non-volatile memory capability, with each cell **102 –** 105 providing charge storage for both. Storing data into the volatile memory of cells **102 – 105** is performed using WRITE operations. Reading data from volatile memory of cells **102 – 105** is performed with READ operations. Storing data into the non-volatile memory of cells **102 -105** is performed using STORE (FLASH WRITE) operations. FLASH WRITE operations may be

preceded by a FLASH ERASE, which clears any stored nonvolatile bit. Reading data from the non-volatile memory of cells **102 - 105** is performed with RECALL (FLASH READ) operations.

[0025] In Figure 1, two nvDRAM bit cells **102** and **103** have been associated with BT0 and BC0. Two nvDRAM bit cells **104** and **105** have been associated with BT1 and BC1. Word line WL0 has two cells **103** and **105** associated with it. Word line WL1 has two cells **102** and **104** associated with it. Of course, these are merely examples for the purpose of illustration, and in practice many more cells may be associated with particular word lines and bit lines.

[0026] Figure 2 is a block diagram of an embodiment of a combined volatile nonvolatile bit cell in more detail. The bit cell **103** comprises two charge cells **201** and **202.** One charge cell **201** is coupled to bit line BT0. The second charge cell is coupled to compliment line BC0. When BT0 is used to write a one (e.g. high state) into charge cell **201,** BC0 may simultaneously be used to write the logical compliment, a zero, into charge cell **202,** and visa versa.

[0027] The word line WL0 and the signals SE0 and RC0 are each coupled to the two charge cells **201** and **202.**

[0028] Figure 3 is an illustration of an embodiment of a combined volatile nonvolatile charge cell. The charge cell **201** comprises three transistors **304, 306,** and **308.** Transistors **304** and **308** act as isolation transistors, isolating the charge storage transistor **306** from the bit line BT0 and from voltages at **310.** Transistor **306** stores charges representing both the non-volatile and volatile bits of the cell **201.** The transistor **306** may be a SONOS (silicon oxide nitride oxide semiconductor) device. This arrangement may involve fewer transistors and thus less expense and higher densities than prior solutions.

[0029] Those skilled in the art will recognize that SONOS is only one possible transistor technology that may be employed to implement the features described herein. For example, in some embodiments other types of transistors such as dedicated floating gate devices may be employed.

[0030] The charge cell **201** comprises a node **302,** also known as "bulk", which may be tied to a constant logical low, also known for example as Vss or ground.

[0031] Charge cell **201** comprises input **310** which is set low during DRAM operations. Signal **310** may be driven high for RECALL, to act as a source of current driven onto the bit line BT0. In some embodiments, **310** may go high during STORE as well, in order to reduce leakage current that may

otherwise be generated by the higher voltages associated with certain nonvolatile operations (higher than for volatile operations).

[0032] The bit line BT0 is coupled to transistor **308.** Transistor **308** acts to couple to the bit line BT0 to internal structures of the charge cell **201** during volatile and nonvolatile operation. Transistor **308** is turned on and off using the word line signal WL0.

[0033] Charge cell **201** comprises a signal line RC0 to the gate of isolation transistor **304.** Signal RC0 may be asserted during RECALL to couple current source **310** to the internals of the cell **201.**

[0034] Signal line SE0 is coupled to the gate of transistor **306.** Signal SE0 may be asserted during nonvolatile STORE to drive charge into the ONO region of transistor **306.** Transistor **306** stores the non-volatile charge as well as the volatile charge. Signal SE0 may also be asserted with a high negative voltage during ERASE to set the state of transistor 306 to a known state (e.g. a state similar to storing a logical nonvolatile "one").

[0035] Figures 4-8 are time line illustrations showing embodiments of signaling for various volatile and nonvolatile operations. Figure 4 is a time line diagram of an embodiment of a volatile READ operation. Figure 5 is a time line diagram of an embodiment of a volatile WRITE operation. Figure 6 is a time line diagram of an embodiment of a nonvolatile STORE operation. Figure 7 is a time line diagram of an embodiment of a nonvolatile RECALL operation. Figure 8 is a time line diagram of an embodiment of a nonvolatile ERASE operation.

[0036] Volatile READ

[0037] Referring to Figure 4 in conjunction with Figure 3, volatile READ operations involve signaling to transistors **306** and **308.** RC0 and the voltage at node **310** may be zero (low) during READ. SE0 may be high. Initially, WL0 is low, and thus transistor **308** is off, isolating the cell **201** from the bit line BT0.

[0038] To begin the READ, the bit line BT0 may be pre-charged, in some embodiments to a level around halfway between high and low, or Vcc/2 (T0). The charge representing the volatile bit is stored by capacitance(s) formed by the source, bulk, drain, and gate of transistor **306** (henceforth, the "v-bit" charge storage). More specifically, v-bit charge storage is accomplished via gate to bulk **302** capacitances and source to drain capacitances of transistor **306.** The v-bit charge is typically

[0039] When the stored volatile bit is a zero, the v-bit storage comprises no significant charge which is comparable to a zero, or low. This is the situation expressed in Figure 4. When WL0 is asserted, charge flows from BT0 to the v-bit storage. This pulls down the voltage on BT0. BC0 stays at approximately the pre-charge level. The sense amplifier engages and drives BT0 to zero, or low (T1-T2), and BC0 to one, or high.

[0040] After the volatile bit is sensed, the voltage on BT0 will determine the setting of v-bit. If BT0 is zero, v-bit remains uncharged and a zero volatile bit is stored when WL0 is dropped (T2-T3). The opposite occurs on the BC0 line. If BT0 is one, v-bit is recharged and a "one" volatile bit is stored when WL0 is dropped. In other words, v-bit and complement v-bit are "refreshed" during the READ operation.

[0041] After a READ, the bit lines may be reset to pre-charge levels (T4). During the READ, SE0 may be set to one or some comparable value to facilitate charge migration to and from v-bit.

[0042] Bit line voltage sensing during volatile READ operations may be based upon small differential voltages on the bit line and complement bit line. This may differ in some embodiments from bit line sensing during nonvolatile RECALL operations, which may be based more upon detecting current flows than on detecting small voltage differentials.

[0043] **Volatile WRITE**

[0044] Referring to Figure 5 in conjunction with Figure 3, volatile WRITE operations involve signaling to transistors **306** and **308.** RC0 and the voltage at node **310** may be zero (low) during WRITE. SE0 may be high. Initially, WL0 is low, and thus transistor **308** is off, isolating the cell **201** from the bit line BT0.

[0045] When writing a one to the volatile bit, BT0 is set to one, or high. This is the situation expressed in Figure 5. WL0 is set high (T0-T2). If there is no charge in v-bit storage (a previously stored volatile bit of zero), charge flows from BT0 to v-bit storage. The opposite will happen for complement v-bit. WL0 is brought low and a one is thus stored in v-bit storage as well as a zero being stored in complement v-bit. Transient effects may be seen on the bit line and complement bit line during the migration of charge (T1-T4).

[0046] WL0 may drop and the bit line and complement line may be reset to pre-charge levels (T5-T7). During the WRITE, SE0 may be set to one or some comparable value to facilitate charge migration to and from v-bit and complement v-bit.

[0047] When writing a zero to the volatile bit equal with one to complement v-bit, BT0 is set to zero, or low and BC0 to high. WL0 is set high. If there is a charge in v-bit storage (a previously stored volatile bit of one), charge drains from v-bit storage to BT0. The opposite occurs with respect to BC0. WL0 is brought low and a zero is thus stored in v-bit storage and a one is stored in complement v-bit.

[0048] **Non-Volatile STORE**

[0049] Referring to Figure 6 in conjunction with Figure 3, a STORE operation may be accomplished by first READing the v-bit and the complement v-bit charges to the bit lines BT0 (T0-T1) and BC0, respectively , then asserting SE0 to a "program" level Vprog (T3-T4). In some embodiments Vprog may be higher than the voltage representing a one bit. For example, when **306** is a SONOS transistor, Vprog may be approximately +10V.

[0050] Asserting Vprog causes the storage of the value of v-bit to nv-bit of transistor **306**. If no charge is stored in v-bit, meaning the volatile bit is zero, the sense amplifier will hold BT0 and thus the source of transistor **306** low (e.g. 0V), and charge will flow to the SONOS gate traps. If charge is stored in v-bit, meaning the volatile bit is one, the source of transistor **306** is held high by the sense amplifier, and by capacitive coupling the source voltage of **306** to a high voltage state with no significant voltage difference between the channel and gate of transistor **306,** consequently a nonvolatile one bit, which is equal to an ERASE state, is stored. The complement v-bit works in the same way. The latter is the situation expressed in Figure 6.

[0051] When WL0 is asserted, the sense amplifier will engage to pull the bit line BT0 to a one or zero, depending on whether v-bit stored a one or zero, respectively (T0-T1). See the discussion of volatile READ for more details.

[0052] After the nonvolatile bit and its complement are stored, the voltage on BT0 will determine the setting of v-bit. If BT0 is zero, v-bit remains uncharged and a zero volatile bit is stored when WL0 is dropped. If BT0 is one, v-bit is recharged and a one volatile bit is stored when WL0 is

dropped. In the same way determines BC0 the setting of complement v-bit. In other words, v-bit and its complement are "refreshed" during the STORE operation.

[0053] A STORE will not overwrite an nv-bit of one with a v-bit of zero. Thus nv-bit (and complement nv-bit) may be cleared (erased) prior to performing a STORE, in order to ensure that during STORE nv-bit either remains a zero (if v-bit is a zero) or is flipped to a one if v-bit is one.

[0054] In some embodiments the node **310** may be set high (e.g. logical one) during STORE. The STORE still proceeds as described above, however leakage current across transistor **304** may be reduced.

[0055] **Non-Volatile ERASE**

[0056] Referring to Figure 8 in conjunction with Figures 3 and 4, an ERASE removes the stored value of nv-bit and complement nv-bit. In some embodiments, to effect an ERASE, SE0 may be set to a relatively high negative value, such as (for **306** SONOS) -10V (T2-T4).

[0057] A READ of v-bit to BT0 (T0-T1) and complement v-bit to BC0 may precede the ERASE, and a WRITE from BT0 to v-bit and to complement v-bit from BC0 (T5-T6) may follow ERASE. This may act to prevent changes/destruction of v-bit during ERASE. In other words, v-bit is/can be "refreshed" during the ERASE operation.

[0058] **Non-Volatile RECALL**

[0059] Referring to Figure 7 in conjunction with Figure 3, a RECALL operation may be accomplished by first causing nv-bit / complement nv-bit to be represented on BT0/BC0 (nvREAD, T0-T6), then performing a WRITE to store the nv-bit value in v-bit and complement nv-bit value in complement v-bit.

[0060] To perform an nvREAD, RC0 and the voltage at node **310** are both set high (e.g. Vcc) (T0-T7). Setting RC0 high turns on transistor **304.** WL0 is also set high (T1-T8), turning transistor **308** on. BT0 and SE0 may be set low (T0-T1). Setting SE0 will result in the channel of transistor **306** to

[0060] Referring to Figure 7 in conjunction with Figure 3, a RECALL operation may be accomplished by first causing nv-bit / complement nv-bit to be represented on BT0/BC0 (nvREAD, T0-T6), then performing a WRITE to store the nv-bit value in v-bit and complement nv-bit value in complement v-bit.

[0061] To perform an nvREAD, RC0 and the voltage at node **310** are both set high (e.g. Vcc) (T0-T7). Setting RC0 high turns on transistor **304.** WL0 is also set high (T1-T8), turning transistor **308** on. BT0 and SE0 may be set low (T0-T1). Setting SE0 will result in the channel of transistor **306** to switch "off", unless nv-bit is "one", in which case **306** will remain "on" or at least allow some current to pass through from source to drain.

[0062] If nv-bit stores a one, the transistor **306** will pass current between **310** and BT0. BT0 will be pulled toward a high value (T2-T4), and the sense amplifier will engage to drive BT0 fully to one (T4-T6). Otherwise, if nv-bit stores a zero, transistor **306** will not pass current between **310** and BT0. BT0 will remain low. In either case, the sensed value of BT0 will represent the stored value of nv-bit, and the sensed value of BC0 represents complement nv-bit.

[0063] Bit line voltage sensing during nonvolatile RECALL operations may be based upon sensing current flows, or may use current flows from **310** to the bit line BT0 to charge the bit line. This may differ in some embodiments from bit line sensing during volatile READ operations, which may be based more upon detecting small voltage differentials on the bit lines than on sensing current flows.

[0064] A WRITE may then be performed to store the value of BT0 to v-bit (see Figure 5) and the value of BC0 to complement v-bit.

[0065] In some embodiments, the transistors **304** and **308** (which may be conventional CMOS) may be fabricated with different gate-oxide thicknesses from one another, to better suit the different voltage conditions applied to these transistors during nonvolatile operations. Thinner gate oxide layers in these transistors may improve the performance of RECALL operations.

[0066] Figure 9 is a block diagram of an embodiment of a device system including a combined volatile nonvolatile memory. The device will typically comprise at least one processor **902,** for example a general purpose microprocessor, an embedded special-purpose processor, a digital signal processor, and so on. The processor **902** may interact with a memory **904** to read and write data during system operation. The memory **904** may comprise a combined volatile nonvolatile array of cells, in accordance with the structures and techniques described herein. In the course of operation,

or upon imminent loss of system power, data may be stored from volatile regions of the memory **904** to the nonvolatile regions.

[0067] Those having skill in the art will appreciate that there are various vehicles by which processes and/or systems described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the processes are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a solely software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are several possible vehicles by which the processes described herein may be effected, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary. Those skilled in the art will recognize that optical aspects of implementations may involve optically-oriented hardware, software, and or firmware.

[0068] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood as notorious by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. Several portions of the subject matter described herein may be implemented via Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in standard integrated circuits, as one or more computer programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and/or firmware would be well within the skill of

one of skill in the art in light of this disclosure. In addition, those skilled in the art will appreciate that the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies equally regardless of the particular type of signal bearing media used to actually carry out the distribution. Examples of a signal bearing media include, but are not limited to, the following: recordable type media such as floppy disks, hard disk drives, CD ROMs, digital tape, and computer memory; and transmission type media such as digital and analog communication links using TDM or IP based communication links (e.g., packet links).

[0069] In a general sense, those skilled in the art will recognize that the various aspects described herein which can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or any combination thereof can be viewed as being composed of various types of "electrical circuitry." Consequently, as used herein "electrical circuitry" includes, but is not limited to, electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of random access memory), and/or electrical circuitry forming a communications device (e.g., a modem, communications switch, or optical-electrical equipment).

[0070] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use standard engineering practices to integrate such described devices and/or processes into larger systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a network processing system via a reasonable amount of experimentation.

[0071] The foregoing described aspects depict different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same

functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality.

CLAIMS

1. A memory circuit comprising:
a single transistor storing both volatile and nonvolatile bit charges.

2. The memory circuit of claim 1, wherein the single transistor storing both volatile and nonvolatile bit charges further comprises: a SONOS transistor.

3. The memory circuit of claim 1, wherein the single transistor storing both volatile and nonvolatile bit charges further comprises: a Floating-Gate transistor.

4. The memory circuit of claim 1, further comprising:
first and second isolation transistors.

5. The memory circuit of claim 4, wherein the first and second isolation transistors further comprise:
transistors having different gate-oxide thicknesses.

6. The memory circuit of claim 1, further comprising:
a sensing circuit responsive to voltage differentials for volatile operations, and responsive to current flow for at least one nonvolatile operation.

7. The memory circuit of claim 1, further comprising:
a bit cell comprising a pair of charge cells each storing both volatile and nonvolatile bit charges.

8. The memory circuit of claim 7, wherein a single transistor of each charge cell storing both volatile and nonvolatile bit charges further comprises:
a SONOS transistor of each charge cell.

9. The memory circuit of claim 7, further comprising:
a first charge cell of the pair storing both volatile and nonvolatile bit values, and a second charge cell of the pair storing complements of the volatile and nonvolatile bit values.

10. The memory circuit of claim 9, further comprising:
the first charge cell coupled to a bit line and the second charge cell coupled to a complement bit line.

11. The memory circuit of claim 7, wherein each charge cell further comprises:
first and second isolation transistors having different gate-oxide thicknesses.

12. A method of operating a combined volatile and nonvolatile memory circuit, comprising:
causing a first charge representing a nonvolatile bit to be stored in a charge trapping region of a transistor; and
causing a second charge representing a volatile bit to be stored outside the charge trapping region of the transistor.

13. The method of claim 12, further comprising:
detecting the second charge as a voltage disturbance to bit line precharge levels that are approximately halfway between zero and one.

14. The method of claim 12, further comprising:
detecting the first charge via a current flow enabled when the first charge is present and absent otherwise.

15. The method of claim 12, further comprising:
refreshing the second charge from a bit line after a memory operation that affects the first charge.

16. The method of claim 15, further comprising:

refreshing the second charge from the bit line after a volatile memory READ operation that affects the first charge.

17. The method of claim 15, further comprising:
refreshing the second charge from the bit line after a nonvolatile memory ERASE operation that destroys the first charge.

18. The method of claim 14, further comprising:
refreshing the second charge from the bit line after a nonvolatile memory STORE operation that affects the first charge.

19. A device comprising:
a processor coupled to interact with a memory system, the memory system comprising
an array of memory cells each storing a single volatile bit and a single nonvolatile bit, each cell employing a single transistor to store the volatile bit and to store the nonvolatile bit.

20. The device of claim 19, further comprising:
the single transistor a SONOS transistor.

21. The device of claim 19, further comprising:
each cell employing a single transistor to store a complement of the volatile bit and to store a complement of the nonvolatile bit.

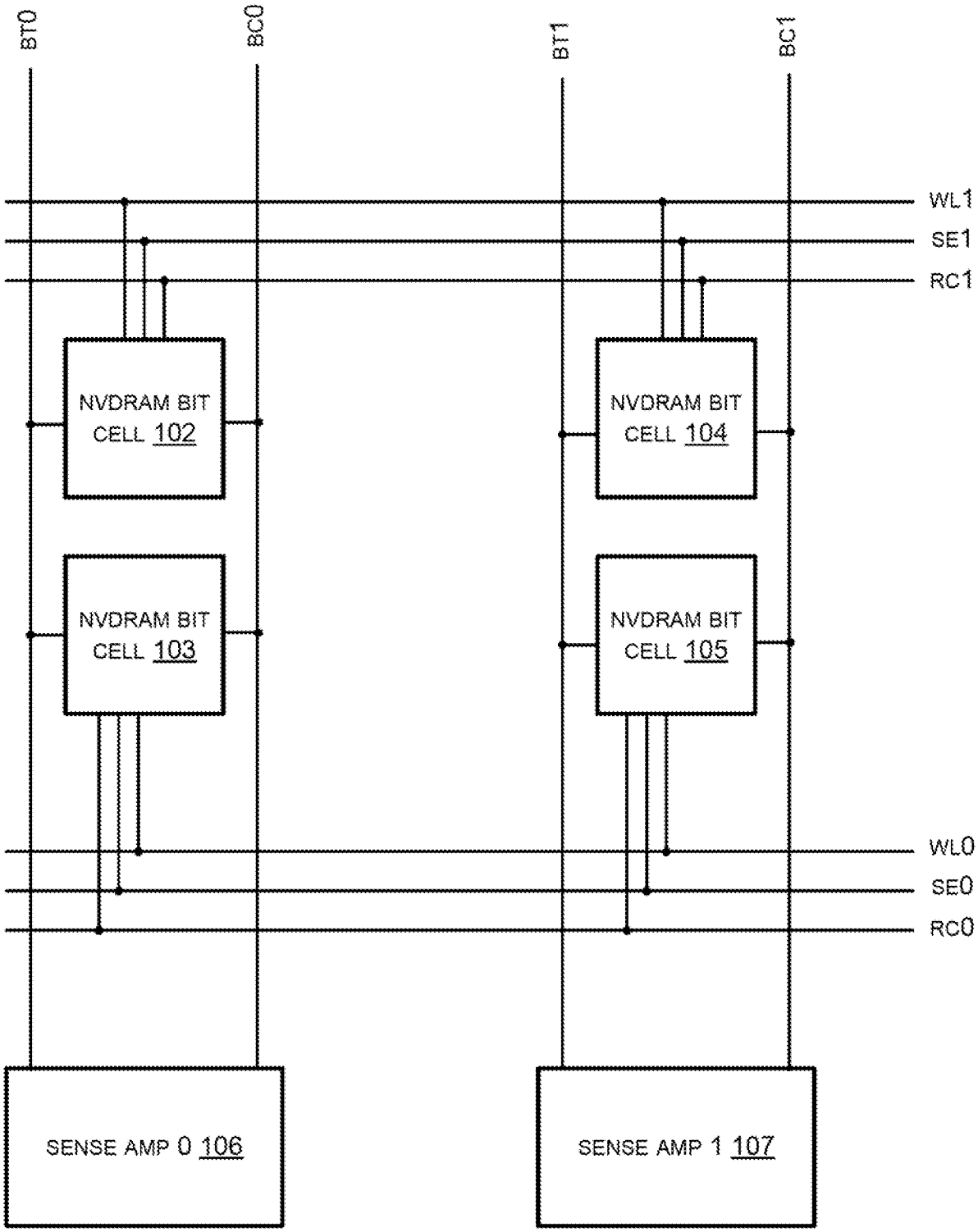
BT0
BC0
BT1
BC1
WL1
SE1
RC1
NVDRAM BIT CELL 102
NVDRAM BIT CELL 104
NVDRAM BIT CELL 103
NVDRAM BIT CELL 105
WL0
SE0
RC0
SENSE AMP 0 106
SENSE AMP 1 107

FIG. 1

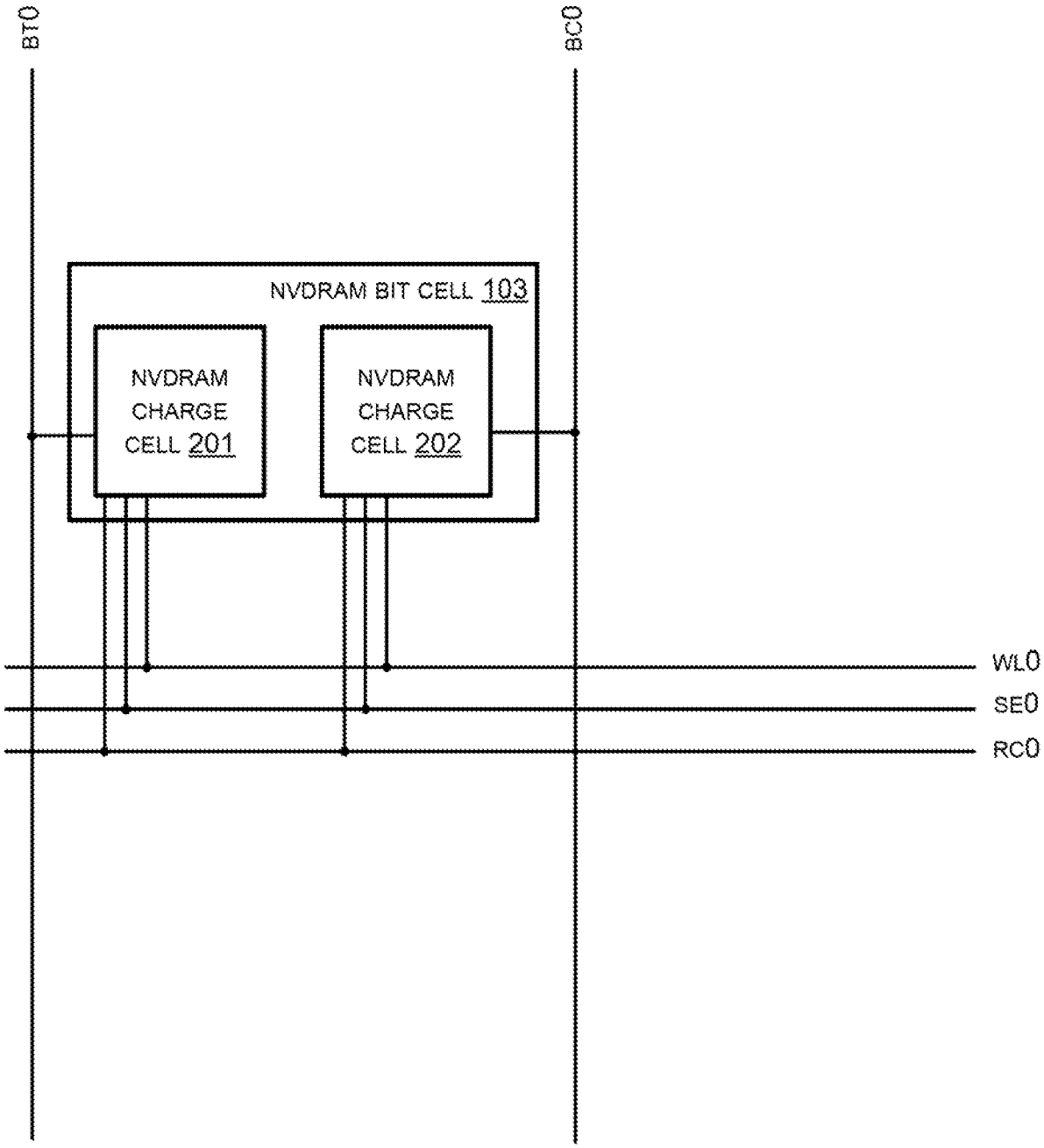
BT0
BC0
NVDRAM BIT CELL 103
NVDRAM CHARGE CELL 201
NVDRAM CHARGE CELL 202
WL0
SE0
RC0

FIG. 2

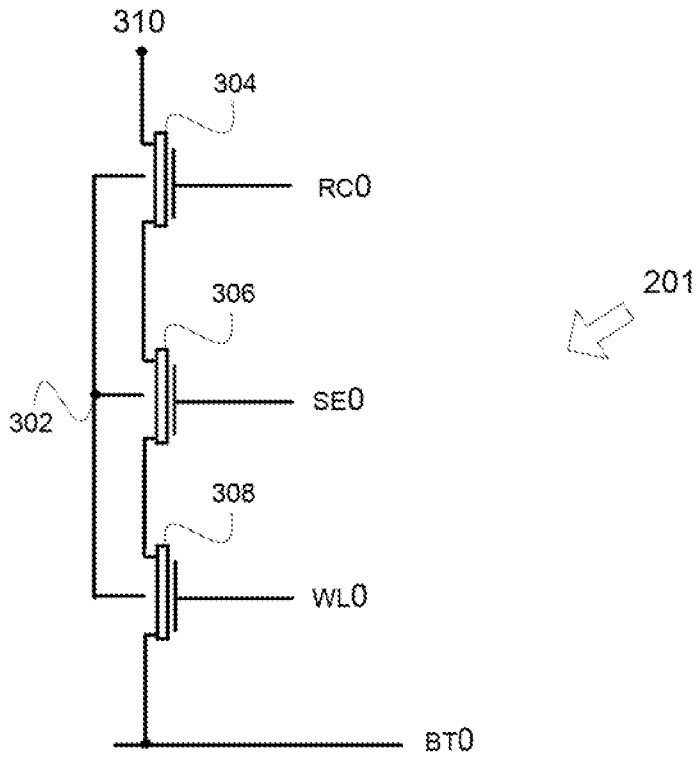

FIG. 3

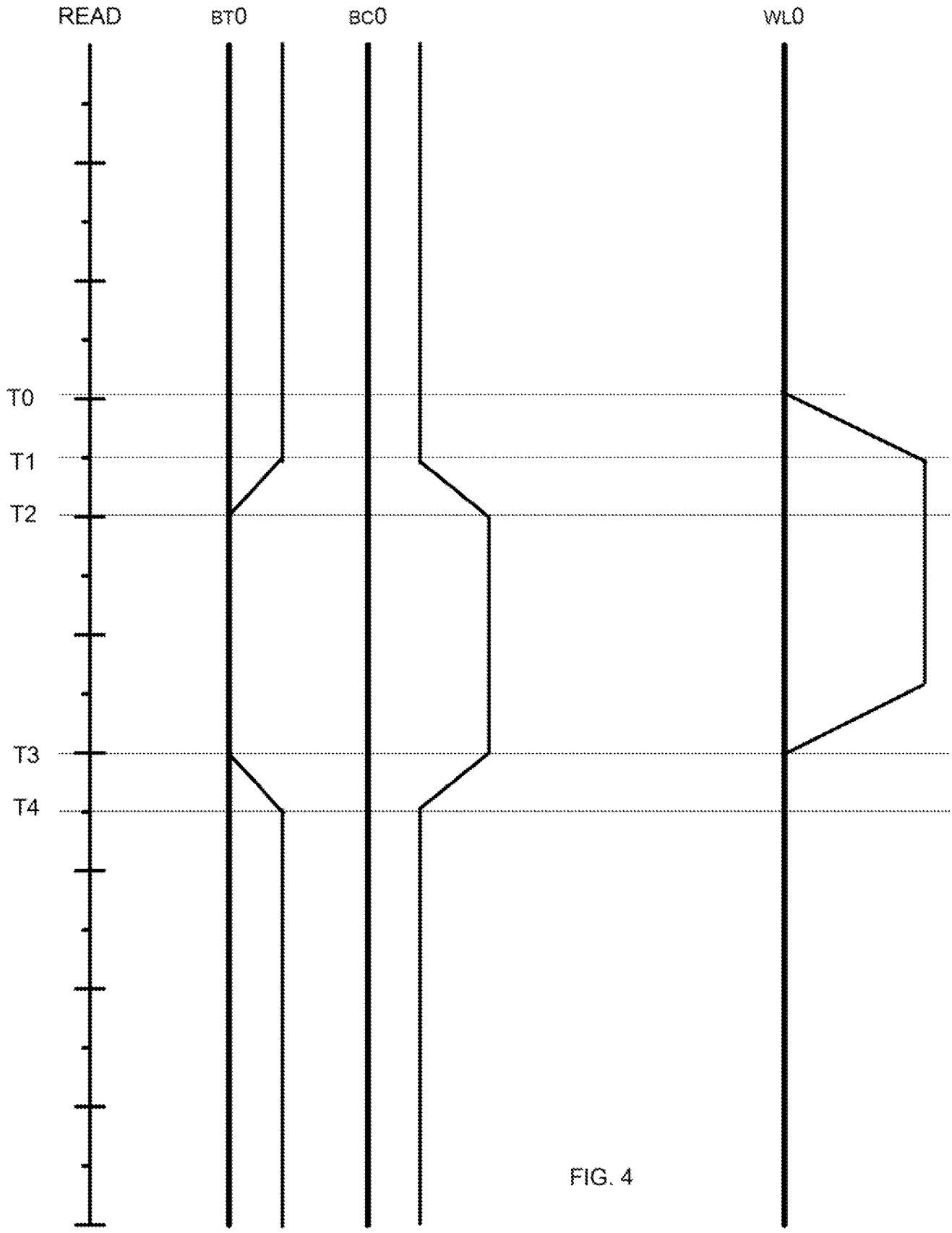

FIG. 4

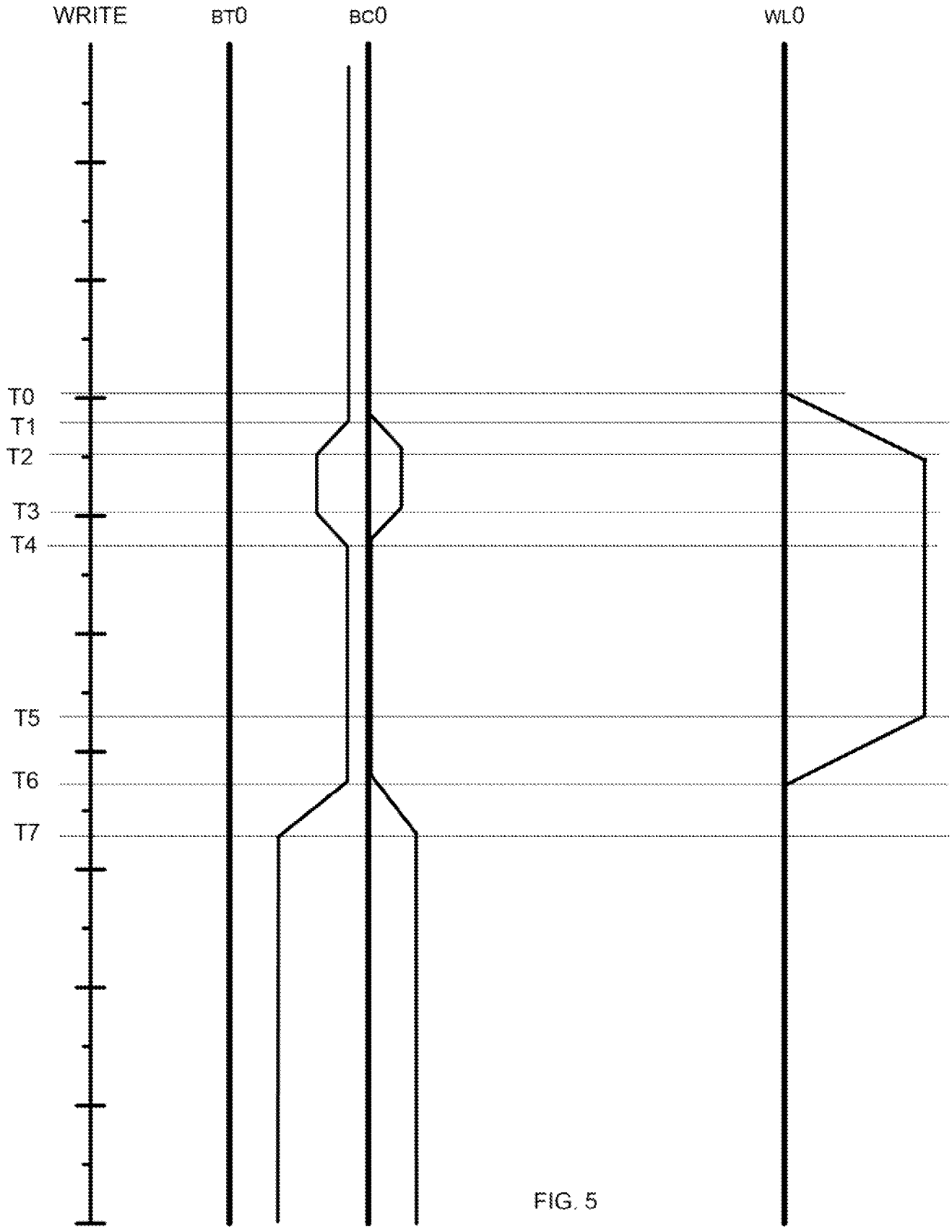

FIG. 5

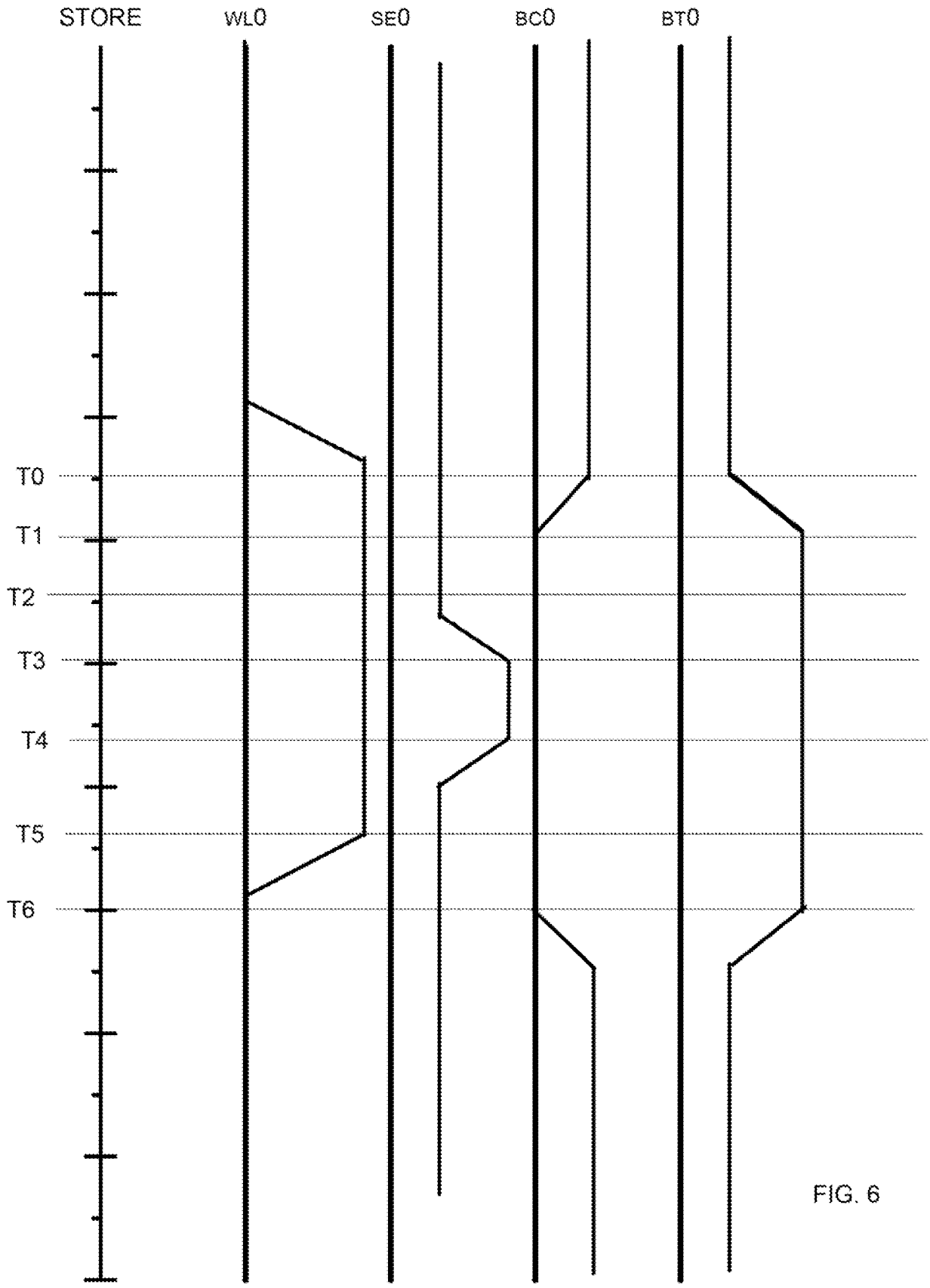

FIG. 6

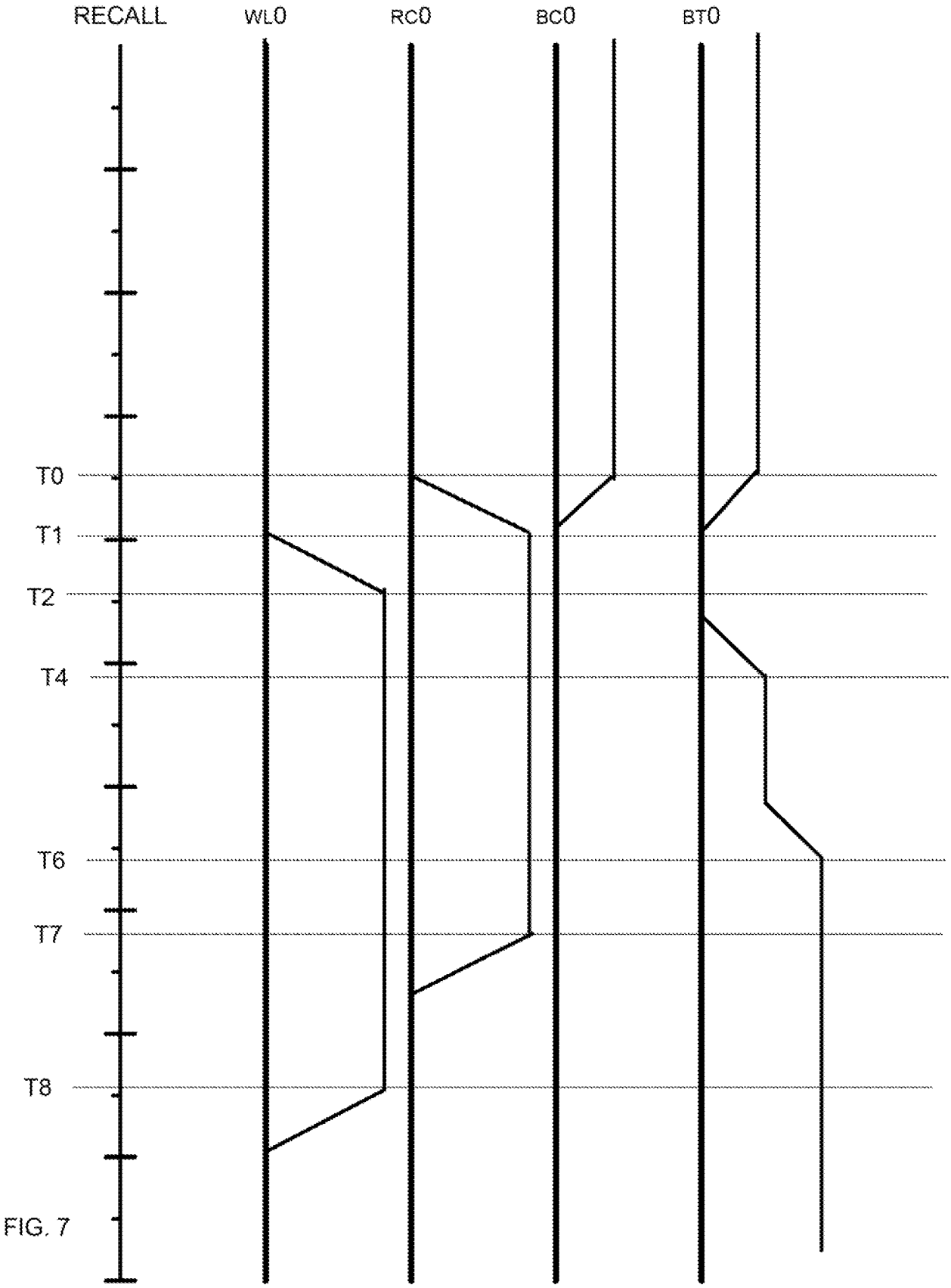

FIG. 7

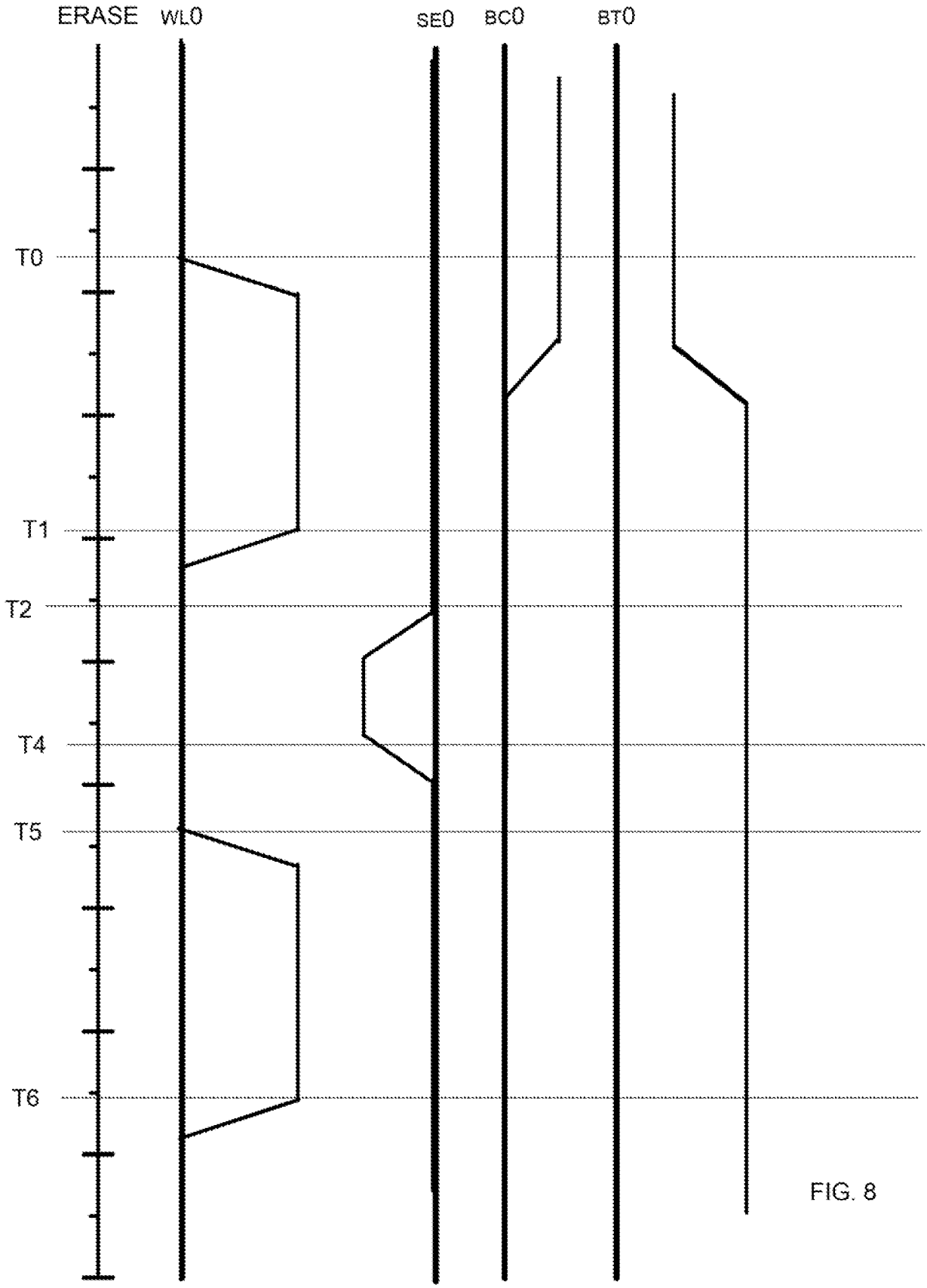

FIG. 8

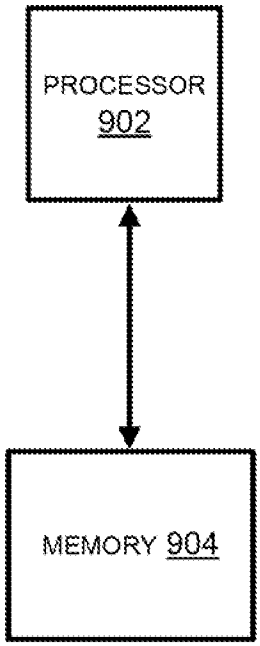

FIG. 9