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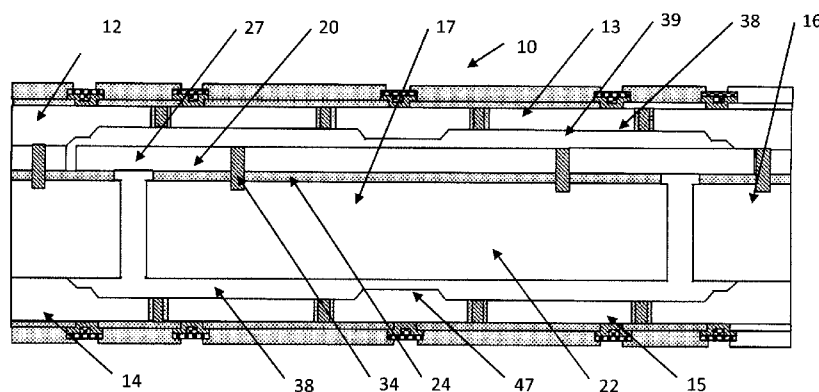


FIG. 1

(57) Abstract: A method for manufacturing a three dimensional MEMS sensor is provided. The MEMS sensor comprises first and second caps bonded to a central MEMS wafer, the central MEMS wafer comprising a MEMS structure. The method comprises a step of forming at least one recess on the inner side of at least one of the silicon-based cap wafers by growing thermal oxide films to consume a portion of silicon. The recess forms the capacitance gap in the MEMS sensor, between one the caps and the MEMS structure. The capacitor gap uniformity is improved by employing a local oxidation or LOCOS process and by removal of the oxide to produce the capacitor gap.



FABRICATION METHOD FOR 3D INERTIAL SENSOR

TECHNICAL FIELD OF THE INVENTION

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This present disclosure relates to a 3D Capacitive Microelectromechanical System (MEMS) pendulous Inertial Sensor, and more particularly to a method of fabricating the sensor using a LOCal Oxidation of Silicon (LOCOS) process.

10 RELATED APPLICATIONS

This patent application claims priority from US 62/054,136, the disclosure of which is incorporated therein, in its entirety, by reference.

15 BACKGROUND

Microelectromechanical System (MEMS) devices, in particular accelerometers and angular rate sensors or gyroscopes (i.e. inertial sensors), are being used in a steadily growing number of applications. Due to the significant increase in
20 consumer electronics applications for MEMS sensors, such as smart phones, optical image stabilization (OIS) for phones and cameras, and wearable electronics, there has been a growing interest in utilizing such technology for more advanced applications traditionally catered to by much larger, more expensive and higher grade non-MEMS sensors. These applications include
25 single and multiple axis devices for industrial applications, Inertial Measurement Units (IMUs) for navigation systems and Attitude Heading Reference Systems (AHRS), control systems for unmanned air, ground and sea vehicles and for precise personal indoor and even GPS-denied navigation. They also may include healthcare/medical and sports performance monitoring and advanced
30 motion capture systems for next generation virtual reality. These advanced applications require lower bias drift and higher sensitivity specifications well beyond existing consumer-grade MEMS inertial sensors on the market. In order

to expand these markets, the higher performance specifications must also be developed and addressed by producing a low cost and small size sensor and/or a MEMS inertial sensor-enabled system.

5 Almost all modern commercial inertial sensors use thin film surface micromachining techniques to fabricate the MEMS. They feature thin inertial masses in the 1-40 μm thickness range, which limits sensitivity and increases mechanical noise. Motion of the inertial proof mass is typically detected capacitively. The planar nature of thin film surface micromachining lends itself to
10 the use of comb capacitors to sense the motion. The capacitor gaps are patterned in the planar film so the dimensions can be controlled photolithographically.

The sensitivity to acceleration and angular velocity can be increased while
15 decreasing the sensitivity to thermal mechanical noise by using a thicker (100 – 1000 μm) pendulous inertial proof mass. The mass is suspended from flexible supports and moves in three dimensions in response to acceleration and angular velocity. The motion of the pendulous mass is detected by measuring changes in the differential capacitance between the proof mass and electrodes located
20 above and below the mass. The capacitor gap between the mass and the electrodes can be formed by etching a recess, either in the electrodes or in the proof mass. Alternatively the gap can be formed by depositing a spacer material between the electrode caps and the MEMS proof mass and removing it selectively beneath and above the proof mass. Both etching and thin film
25 deposition are limited to about 5-10% uniformity across a wafer. This non-uniformity gives rise to variability in each of the top and bottom capacitor gaps which can lead to offset errors in the measured differential capacitance.

In order to provide adequate measurement sensitivity it is desirable that the
30 sense capacitance be as large as possible. This can be accomplished in one of two ways: increasing the capacitor area and decreasing the capacitor gap.

Because of chip area limitations, minimizing the gap is attractive. Thus sense capacitor gaps are typically very small, in the 1-5 μm range. The plates of the sense capacitor can be caused to come into contact either from surface tension effects during fabrication or due to shock or over-ranging in operation. Once in
5 contact, the Van der Waal's force, which arises from inter-atomic attractive forces and is proportional to the contact area, can exceed the restoring force of the springs and cause the capacitor plates to stick.

In light of the preceding, there is a need for an improved fabrication process and
10 for an improved MEMS sensor.

SUMMARY OF THE INVENTION

The present invention addresses the capacitor gap non-uniformity by employing
15 a local oxidation or LOCOS process and complete oxide removal to produce the capacitor gap. Oxidation processes are slow, can be controlled much more accurately than etch and deposition processes, and can be performed on many wafers at the same time. Optionally, anti-stiction bumps can be formed using a two-step oxidation process.

20 According to the invention, an improved method for fabricating MEMS sensor is provided. The MEMS sensor is formed by top and bottom caps and a central MEMS wafer which includes a MEMS structure, such as a resonant structure or a membrane. The method uses a LOCOS process for controllably forming
25 recesses in top and bottom cap wafers, consequently forming more uniform capacitors gaps once the MEMS sensor is assembled.

In an embodiment, the method involves using a single-step LOCOS process for forming recesses on the inner side(s) of the top and/or bottom cap layers of a
30 MEMS device. The process comprises growing a first layer of oxide film on the inner sides and depositing a first layer of non-oxidizing film thereon; etching the

first layer of non-oxidizing film to expose a pattern in the first layer of oxide film corresponding to predetermined locations of recesses; etching the exposed first layer of oxide film, using the first layer of non-oxidizing film as a mask; growing a first thick layer of thermal oxide on the exposed silicon, thus consuming the underlying silicon; and removing the first layers of oxide film, non-oxidizing film and thick thermal oxide.

According to another embodiment, anti-stiction gaps are formed in the recesses. In this embodiment, the step of etching the first layer of non-oxidizing film exposes a pattern in the first layer of oxide film which includes un-exposed sections corresponding to predetermined locations of anti-stiction bumps.

According to yet another embodiment, the anti-stiction bumps are fabricated with a height t_1 , the difference between the bonding surface and the top of the bumps with a height t_2 , and the recesses with a thickness $t_1 + t_2$. Such an embodiment uses a two-step LOCOS process. In this case, the method described above further comprises the steps of growing a second layer of oxide film on the inner sides and depositing a second layer of non-oxidizing film thereon; etching the second layer of non-oxidizing film to expose a pattern in the second layer of oxide film corresponding to the predetermined locations of the recesses and of the anti-stiction bumps; etching the exposed second layer of oxide film, using the second layer of non-oxidizing film as a mask; growing a second thick layer of thermal oxide on the exposed silicon, thus consuming the underlying silicon; and removing the second layers of oxide film, non-oxidizing film and thick thermal oxide.

The LOCOS processes outlined in the present invention can be combined with existing fabrication methods for MEMS which involve the assembly of top and bottom cap layers to enclose the MEMS structure, such as a resonant structure for example. Once the recesses are formed using the method of the present invention, the layers of the MEMS device can be patterned and assembled using

know processes to complete the MEMS device, while having the particular advantage of having more uniform capacitor gaps provided by the LOCOS process.

- 5 According to an aspect, a method for manufacturing a three dimensional MEMS sensor is provided. The method includes the steps of: forming at least one recess on an inner side of a silicon-based first cap wafer by growing thermal oxide films to consume a portion of silicon in the first cap wafer; patterning trenches to form electrodes on the inner side of the first cap wafer; patterning first portions of a
- 10 MEMS structure in a first side of a MEMS wafer; bonding said first side of the patterned MEMS wafer to the inner side of the first cap wafer with the at least one recess facing the MEMS structure to form at least one capacitance gap, the electrodes of the first cap wafer being located over the MEMS structure and forming a capacitor therewith; patterning second portions of the MEMS structure
- 15 on a second side of the MEMS wafer; further bonding the second side of the patterned MEMS wafer to an inner side of a silicon-based second cap wafer; and removing a portion of an outer side of the first cap wafer to isolate the electrodes of the first cap wafer.
- 20 In an embodiment, the thermal oxide films include first and second thermal oxide films, and forming at least one recess includes the steps of: growing the first thermal oxide film on the inner side of the first cap wafer; depositing a first non-oxidizing film on the inner side of the first cap wafer on top of the first thermal oxide film; etching the first non-oxidizing film to create exposed areas at locations
- 25 along the inner side of the first cap wafer where the at least one recess is to be located; growing the second thermal oxide film in the exposed areas; and removing the first non-oxidizing film and the first and second thermal oxide films, thereby leaving the at least one recess in the first cap wafer.

In an embodiment, the step of forming at least one recess further includes the substep of etching the first thermal oxide film in the exposed areas prior to growing the second thermal oxide film.

- 5 In an embodiment, the step of etching the first thermal oxide film in the exposed area includes a wet etch process.

In an embodiment, the steps of removing the first non-oxidizing film, and the first and second thermal oxide films include wet etch processes.

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In an embodiment, the method further includes a step of forming at least one recess in the second cap wafer by growing at least some of the thermal oxide films to consume a portion of silicon in the second cap wafer.

- 15 In an embodiment, the second thermal oxide film is grown to a thickness greater than a thickness of the first thermal oxide film.

In an embodiment, the thickness of the second thermal oxide film is between 10 and 100 times the thickness of the first thermal oxide film.

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In an embodiment, the first thermal oxide film is grown to a thickness between 10 nm and 100 nm.

- 25 In an embodiment, the second thermal oxide film is grown to a thickness between 1 and 3 μm .

In an embodiment, the method further includes the step of forming at least one anti-stiction bump in the at least one recess in the first cap wafer.

In an embodiment, forming the at least one anti-stiction bump in the at least one recess in the first cap wafer includes growing the thermal oxide films to consume the portion of the silicon in the first cap wafer in a two-step oxidation process.

- 5 In an embodiment, the thermal oxide films further include third and fourth thermal oxide films, and the two-step oxidation process includes a first step including the substeps of: growing the first thermal oxide film on the inner side of the first cap wafer; depositing the first non-oxidizing film on the inner side of the first cap wafer on top of the first thermal oxide film; etching the first non-oxidizing film to
10 create the exposed areas, while also leaving covered areas at locations along the inner side of the first cap wafer where the at least one anti-stiction bump is to be located; growing the second thermal oxide film in the exposed areas; removing the first non-oxidizing film and the first and second thermal oxide films, thereby leaving behind the at least one recess and the at least one anti-stiction bump;
15 and a second step including the substeps of: growing the third thermal oxide film on the inner side of the first cap wafer; depositing a second non-oxidizing film on the inner side of the first cap wafer on top of the third thermal oxide film; etching the second non-oxidizing film to expose the at least one recess and the at least one anti-stiction bump; growing the fourth thermal oxide film on the exposed at
20 least one recess and the exposed at least one anti-stiction bump; removing the second non-oxidizing film and the third and fourth thermal oxidizing films, thereby leaving behind the at least one recess and the at least one anti-stiction bump in the at least one recess.
- 25 In an embodiment, the second thermal oxide film is grown to a first depth t_1 and the fourth thermal oxide film is grown to a second depth t_2 , thereby resulting in the at least one recess having a thickness t_1+t_2 and the at least one anti-stiction bump having a height t_1 .
- 30 In an embodiment, the depth t_1 is different than the depth t_2 .

In an embodiment, the depth t_2 is greater than the depth t_1 .

In an embodiment, growing the second and fourth thermal oxide films includes forcing an oxidizing agent to diffuse into the first cap wafer at predetermined
5 temperatures for predetermined periods of time, said predetermined temperatures and periods of time respectively corresponding to temperatures and times required to grow thermal oxide film in the silicon-based first cap wafer to depths t_1 and t_2 , respectively.

10 In an embodiment, the first cap wafer includes a single-layer silicon wafer, and the step of patterning the electrodes includes etching closed-loop trenches on the inner side of the first cap wafer along the at least one recess, and filling or lining said trenches with an insulated material to electrically insulate the electrodes from the remainder of the first cap wafer.

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In an embodiment the trenches are etched in the first cap wafer to a depth approximately equal to the final first cap thickness.

In an embodiment, the first cap wafer includes a first SOI wafer.

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In an embodiment, the method further includes the step of patterning trenches to form electrodes on the inner side of the second cap wafer.

In an embodiment, the second cap wafer includes a second SOI wafer, and the
25 step of forming the electrodes in the second cap wafer includes the substeps of etching, down to a buried oxide layer, closed-loop trenches on the inner side of the second cap wafer along the at least one recess, the trenches and buried oxide layer together electrically insulating the electrodes from the remainder of the second cap wafer.

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In an embodiment, the method further includes a step of forming at least first and second electrical contacts on the outer side of the first cap wafer, the first electrical contact being electrically connected to at least one of the electrode in the first cap wafer and the second electrical contact being electrically connected to at least one of the electrodes in the second cap wafer via insulated conducting channels extending from within the second cap wafer, through the MEMS wafer and through the first cap wafer.

In an embodiment, the method further includes a step of forming electrical contacts on an outer side of the second cap wafer, said electrical contacts on the outer side of the second cap wafer being electrically connected to the electrodes of the second cap wafer.

In an embodiment, the method further includes a step of forming at least first and second electrical contacts on the outer side of the first cap wafer, the first electrical contact being electrically connected to at least one of the electrodes of the first cap wafer and the second electrical contact being electrically connected to the MEMS structure via insulated conducting channels extending from within the MEMS wafer and through the first cap wafer.

In an embodiment, the MEMS wafer includes a third SOI wafer with a handle layer and a device layer, the first side of the MEMS wafer including the handle layer and the second side of the MEMS wafer including the device layer, and the MEMS structure includes a flexible element patterned in the device layer.

In an embodiment, the MEMS sensor includes an inertial sensor, the MEMS structure is a resonant structure, the flexible element includes springs suspending the resonant structure, and the steps of patterning the first and second portions of the MEMS structure include patterning portions of the resonant structure and spring in the device layer of the MEMS wafer, and

patterning remaining portions of the resonant structure and the spring in the handle layer of the MEMS wafer.

In an embodiment, the resonant structure is a proof mass.

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In an embodiment, the first and second cap wafers are bonded using a conductive bond.

10 In an embodiment, bonding the first and second cap wafer to the MEMS wafer includes hermetically sealing the MEMS structure between the first and second cap wafers.

15 In an embodiment, the step of growing the thermal oxide film to consume a portion of the silicon on the inner side of the first cap wafer is performed simultaneously on a plurality of wafers.

In an embodiment, the plurality of wafers is between 25 and 200.

20 In an embodiment, a variation between depths of the recesses formed in each of the plurality of wafers is less than 5%.

According to an aspect, a MEMS sensor is provided, the MEMS sensor being one manufactured by the method described above.

25 According to an embodiment, a three dimensional (3D) MEMS sensor is provided. The MEMS sensor includes: an electrically conductive MEMS wafer including a MEMS structure, the MEMS wafer having a first side and a second side; a silicon-based top cap having an inner top cap side and an outer top cap side, the inner top cap side having at least one recess formed by oxidation of a
30 portion of the silicon of the top cap, the at least one recess facing the MEMS structure to form at least one capacitance gap, the top cap having electrodes

patterned in the inner top cap side, the inner top cap side being bonded to the first side of the MEMS wafer, the electrodes of the top cap being located over the MEMS structure and forming a capacitor therewith across the capacitance gap, the outer top cap side having electrical contacts on or over the electrically
5 conductive top cap wafer, a silicon-based bottom cap having an inner bottom cap side and an outer bottom cap side, the bottom cap wafer being bonded to the second side of the MEMS wafer such that the MEMS wafer, the top cap wafer and the bottom cap wafer define a cavity for housing the MEMS structure; and first and second electrical contacts formed on at least the top cap wafer,
10 connected to the electrodes of the first cap wafer and to the MEMS structure.

In an embodiment, the sensor further includes at least one anti-stiction bump formed by oxidation in the at least one recess of the top cap.

15 In an embodiment, the at least one anti-stiction bump extends in the recess below a height thereof.

In an embodiment, a height of the at least one anti-stiction bump is less than half of the height of the recess,
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In an embodiment, the inner bottom cap side has at least one recess formed by oxidation of a portion of the silicon of the bottom cap.

In an embodiment, the at least one recess in the bottom cap faces the MEMS
25 structure to form at least one capacitance gap, the bottom cap having electrodes patterned in the inner bottom cap side, the electrodes of the bottom cap being located under the MEMS structure and forming a capacitor therewith across the capacitance gap, the outer bottom cap side having electrical contacts on or over the electrically conductive bottom cap wafer.

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In an embodiment, the sensor further includes at least one anti-stiction bump formed by oxidation in the at least one recess of the bottom cap.

Of course, other processing steps may be performed prior, during or after the
5 above described steps. The order of the steps may also differ, and some of the steps may be combined.

DESCRIPTION OF THE DRAWINGS

10 It is noted that the appended drawings illustrate only exemplary embodiments of the invention and are therefore not to be considered limiting of its scope, as the invention may admit to other equally effective embodiments.

Figure 1 is a cross section view of a possible embodiment of a MEMS 3D Inertial
15 Sensor fabricated with a local oxidation process.

Figure 2 is a cross section view of a top cap wafer of the MEMS 3D Inertial Sensor of FIG. 1, showing a possible step of the fabrication method.

Figure 3 is a cross section view of the top cap wafer of FIG. 2, showing the
20 patterning of non-oxidizing and thermal oxide films to form an oxidation mask for the recess and, optionally, anti-stiction bumps.

Figure 4 is a cross section view of the top cap wafer of FIG. 2, showing thermal oxidation to consume silicon in the recesses.

Figure 5 is a cross section view of the top cap wafer of FIG. 2, showing wet-etch removal of the non-oxidizing oxide films.

25 Figure 6 is a cross section view of the top cap wafer of FIG. 2, showing second thick oxide film growth following regrowth and patterning of the thin oxide and non-oxidizing films, according to an optional step of the fabrication method.

Figure 7 is a cross section view of the top cap wafer of FIG. 2, showing recesses and anti-stiction bumps patterned in the cap silicon following the LOCOS processes, according to an optional step of the fabrication method.

5 Figure 8 is a cross section view of the top cap wafer of FIG. 2, showing trench patterning to define cap electrodes and leads.

Figure 9 is a cross section view of the top cap wafer of FIG. 2, showing the trenches lined with an insulating film, in this case thermal oxide.

Figure 10 is a cross section view of the top cap wafer of FIG. 2, showing the trenches filled with a conducting or non-conducting film, in this case polysilicon.

10 Figure 11 is a cross section view of the top cap wafer of FIG. 2, showing the conductive or non-conductive fill and insulating lining films etched back to the silicon surface, leaving filled trenches.

Figure 12 is a cross section view of a bottom cap wafer of the MEMS Inertial Sensor of FIG. 1, fabricated using a similar process as illustrated in FIGS. 2
15 through 11.

Figure 13 is a cross section view of a MEMS wafer of the MEMS Inertial Sensor of FIG. 1, showing the start of the MEMS wafer process with an oxidized SOI wafer.

20 Figure 14 is a cross section view of the MEMS wafer of FIG. 13, showing the etching of trenches for the SOI shunts.

Figure 15 is a cross section view of the MEMS wafer of FIG. 13, showing the SOI shunt trenches filled with a conducting film, in this case polysilicon.

25 Figure 16 is a cross section view of the MEMS wafer of FIG. 13, showing the conducting fill film etched off of one surface (here the top surface or SOI layer) of the MEMS wafer, leaving filled SOI shunts, with the SOI device layer MEMS structures patterned.

Figure 17 is a cross section view showing the top cap wafer of FIG. 2 aligned and bonded to the patterned side (i.e. device layer) of the MEMS wafer of FIG. 13.

Figure 18 is a cross section view of the assembled top cap and MEMS wafers of FIG. 17, showing the conducting and insulating films etched off the other (non-processed) side of the MEMS wafer and the MEMS structures (in this case, feedthroughs and a proof mass) patterned.

- 5 Figure 19 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 1, showing the bottom cap wafer bonded to the MEMS wafer.

Figure 20 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 1, showing the top cap ground and polished to expose the insulating channels.

- 10 Figure 21 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 1, showing the top cap passivated with a protective insulating oxide layer, contacts etched through the oxide, and with lead and bond pad metallization applied.

Figure 22 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 1, showing bond pads and leads patterned in the metallization layer.

- 15 Figure 23 is a cross section view of a MEMS 3D Inertial Sensor according to one possible embodiment with top-cap-only bond pads, showing a thick protective passivation oxide layer deposited over the bond pads, where the bottom cap is ground, polished, and passivated with a thin oxide layer.

Figure 24 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 23, showing contacts opened over the bond pads.

- 20 Figure 25 is a cross section view of the MEMS 3D Inertial Sensor according to an embodiment with bond pads on both caps and before the top bond pad contacts are opened, showing bottom cap contacts patterned through the thin protective oxide, bond pad and electrical lead metallization deposited and patterned, and a deposited thick protective oxide.

- 25 Figure 26 is a cross section view of the MEMS 3D Inertial Sensor of FIG. 25, showing contacts opened over the bond pads on both the top and bottom caps, thus completing the MEMS fabrication.

Figure 27 is a cross section view of the top cap of the MEMS 3D Inertial Sensor according to an embodiment with no anti-stiction bumps, showing the recess patterned with a single thermal oxidation.

5 Figure 28 is a cross section view of the top cap of FIG. 27 showing the recess only.

Figure 29 is a cross section view of the completed MEMS according to an embodiment using the top cap of FIG. 28, showing the wafer with the recess and no anti-stiction bumps formed by a single recess oxidation.

10 Figure 30 is a cross section view of the bottom cap of the MEMS 3D Inertial Sensor according to an embodiment in which the bottom cap is fabricated from an SOI wafer, with the SOI buried oxide eliminating the need to use an insulating trench fill.

15 Figure 31 is a cross section view of the MEMS 3D Inertial Sensor according to the embodiment of FIG. 30, showing the wafer with the SOI bottom cap prior to top cap completion.

Figure 32 is a cross section view of the Completed MEMS 3D Inertial Sensor according to the embodiment of FIG. 30, showing the wafer with SOI bottom cap.

20 DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

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Figure 1 shows an embodiment of a MEMS sensor 10 fabricated using a possible embodiment of the present fabrication method. In the illustrated embodiment, the MEMS sensor is a 3D inertial sensor, but it should be appreciated that other types of MEMS sensors can also be fabricated using the present invention, such as a MEMS pressure sensor, for example. The sensor 10 consists of a proof mass 17 suspended by one or more springs 27 between two caps 12 and 14, each with four or more drive and sense electrodes 13, 15 disposed to measure the position of the proof mass in 3-dimensional space in response to acceleration and angular velocity. In a preferred embodiment, the proof mass 17 and springs

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27 are fabricated in a MEMS wafer 16, which in this case is a central silicon-on-insulator (SOI) wafer. The bulk of the proof mass 17 is in the handle layer 22 of the SOI wafer 16, and the springs 27 are patterned in the single crystal silicon (SCS) device layer 20. The device 20 and handle 22 layers of the SOI wafer are
5 separated by an insulating buried oxide layer 24, so conducting shunts 34 through the buried oxide are used to electrically connect the device and handle layers where required. The caps include one or more recesses 38 which form a capacitor gap 39 between the electrodes 13, 15 and the outer surfaces of the proof mass, as well as anti-stiction bumps 47. The capacitor gap 39 is the space
10 between the outer surfaces of the MEMS structure and the inner surfaces of the caps. Anti-stiction bumps 47 protrude slightly from the recessed portion of the caps, such that the height of the gap 39 is shorter opposite the bumps. The anti-stiction bumps are an optional feature but are included as part of the preferred embodiment. Anti-stiction bumps are projections protruding or projecting from the
15 respective inner surfaces of cap plates 12, 14, preventing the proof mass from "sticking" to the caps. Of course, it is possible that only one of the caps be provided with anti-stiction bump(s). The recesses and bumps in the caps are fabricated using a local oxidation process, also referred to as Local Oxidation of Silicon (LOCOS). The fabrication described therein comprises growing thermal
20 oxide films on silicon-based wafers to consume silicon in specific areas of the wafers.

Figure 2 shows the start of the manufacturing process. Fabrication of a gap 39 with an anti-stiction bump 47 will be described, the gap and bump being formed
25 with a two-step LOCOS process. The first step involves a first oxidation, while the second step involves a second oxidation.

As part of the first oxidation, a first silicon-based wafer 12 is provided. In the present embodiment, the first wafer 12 has inner 121 and outer 122 sides, and
30 will serve as a first or top cap in the assembled MEMS device. A first thermal oxide film 48 is grown on the wafer 12. The first thermal oxide is grown to a

thickness of approximately 50 nm, and can therefore be referred to as a thin thermal oxide film. Next, a first non-oxidizing film 49, such as silicon nitride, is deposited. Figure 3 shows the patterning of the films. The first non-oxidizing film 49 is patterned and etched to expose the thermal oxide 48 on the inner side 121 in the locations corresponding to the recesses. The first non-oxidizing film 49 can be removed using either a wet or dry etch. Next the exposed first thermal oxide film 48 is etched using the first non-oxidizing film 49 as a mask. Typically the oxide is etched using a wet etch to avoid damage to the underlying silicon. It is also possible to leave the thin oxide, without etching it.

Figure 4 shows the growth of a second thermal oxide film 50 on the exposed silicon 12. The second thermal oxide film 50 can be referred to as a thick thermal oxide in that it is generally thicker than the first thermal oxide film 48, for example 10 to 100 times thicker, or between 1 μm and 5 μm . The oxidation process consumes some of the underlying silicon. The rate of growth of thermal oxide is determined by several parameters: wet vs. dry process, temperature, and silicon crystal structure. The thickness of silicon consumed is typically about 46% of the thickness of the thermal oxide grown, due to the relative densities of silicon and silicon dioxide, and may vary by 2-4 per cent depending upon the quality of the oxide grown. In some variations of the LOCOS process, the thin thermal oxide is not etched. This affects the growth rate of the thermal oxide but not the ratio of silicon consumed to oxide grown. This first oxidation determines the difference in height between opposed anti-stiction bumps and the capacitor gap, which extends between the more recessed portions of the caps. In LOCOS processes where the thin oxide is not removed, the thermal oxidation time must take into account the additional time required to grow the thick film because of the additional diffusion time required through the thin oxide film. As can be appreciated, when growing the second thermal oxide film 50, these factors are taken into account to select a temperature and time required in order to grow the second thermal oxide film 50 to a predetermined depth which corresponds to the desired depth of the recess.

Figure 5 shows the removal of all of the first non-oxidizing film 49 and first 48 and second 50 thermal oxide films. Typically these are wet etch processes, again to avoid damaging the silicon. Silicon nitride can be etched using hot phosphoric acid and thermal oxide is typically etched using buffered hydrofluoric acid (Buffered Oxide Etch or BOE).

Figure 6 shows the second oxidation which involves the growth of another thick thermal oxide 50' in order to further define the recess 38 and bumps 47. First, a third thermal oxide film 48' is grown. Much like the first thermal oxide film, the third thermal oxide film 48' can be referred to as a thin film in that it also has a thickness of about 50 nm. Next, a second non-oxidizing film 49' is deposited and the films are patterned and etched as before. In this step the anti-stiction bumps 47 are left exposed with the rest of the recess 38. This way, when a fourth thermal oxide 50' is grown, part of the silicon forming the anti-stiction bump 47 is consumed as well. The fourth thermal oxide film 50' is a thick thermal oxide in that it is generally thicker than the third thermal oxide film 48', and may have a thickness between 1 μm and 5 μm , or be 10 to 100 times thicker than the third thermal oxide film 48'.

Figure 7 shows the second non-oxidizing film 49' and third 48' and fourth 50' thermal oxide films again removed using wet etches producing a recess 38 and anti-stiction bump 47. If the amount of silicon consumed by the second thermal oxide film during the first oxidation is t_1 and the amount consumed by the fourth thermal oxide film during the second oxidation is t_2 , then the recess thickness is t_1+t_2 , the anti-stiction bump height is t_1 , and the difference in height between the outer edge or bonding surface of the chip and the top of the bump is t_2 . The depths t_1 and t_2 can be chosen according to the needs of the device. For example, t_1 can be less than t_2 , resulting in the anti-stiction bump having a height less than half of the recess thickness.

As can be appreciated, by adjusting oxidation conditions for each oxidation, the total capacitor gap width and anti-stiction bump height can be adjusted independently. An advantage of the present method compared to other existing methods is that the height of the capacitor cap can be carefully controlled since thermal oxidation is a slow predictable process but is a batch process that can be applied to many wafers (such as up to 100-200) at a time. For example a typical oxidation process undertaken at 1000°C grows 1 micrometer of oxide in 4 hours, or 4 nm/minute. Controlling the oxidation time to one minute thus corresponds to 0.4 % reproducibility. In contrast, Si etches have higher rates and are more variable with around 5% reproducibility. Also Si etches are limited to single wafers in dry etchers and around 25 wafers in batch wet etches. As can be appreciated, after conducting this step, the entire oxide layers are removed.

Referring to Figure 8, next the silicon wafer 12 is patterned with the desired top cap electrode pattern by etching trenches 28 into the silicon 12 that penetrate partially into the wafer a distance approximately equal to the final cap thickness. Preferably, at least some of the trenches 28 are etched on the inner side 121 of the top cap 12, within the recess 38 formed using the LOCOS process. Figure 9 shows a thermal oxidation of the wafer to coat the surfaces of the trenches with an insulating oxide 30.

Figure 10 shows the filling of the trenches 28 with a conductive material 32 such as polysilicon. The purpose of the fill is mechanical, to provide a rigid hermetic seal in the trenches 28 when the sensor is assembled. Thus, alternatively, the trenches 28 can be filled with only an insulating material such as thermal oxide, LPCVD (Low Pressure Chemical Vapor Deposition) oxide, or other insulating film. Numerous trench etch and fill processes are available at different MEMS fabrication facilities and the insulating and conducting materials vary between them. The details of the trench etch and fill process are not critical. What is needed is that islands of silicon in the shape of the electrodes 13 be surrounded by insulating barriers which are patterned into the silicon a sufficient depth

greater than the final desired cap thickness. The conductive layer 32, here polysilicon, is etched back to or just below the surface of the silicon recess 38, and the oxide is wet etched from the surface and tops of the trenches, leaving an exposed bare silicon surface on the inner side 121, with electrodes 13 outlined by insulating trenches 28 as shown in Figure 11. The process is repeated on a second wafer 14 to form a bottom cap with the bottom cap electrode pattern 15 as shown in Figure 12.

Figure 13 shows the start of the MEMS wafer fabrication process, where first portions of a MEMS structure are patterned in the MEMS wafer 16. The process starts with a silicon-based wafer 16, referred to as a MEMS wafer. In the present embodiment, the MEMS wafer comprises a SOI (Silicon on Insulator) wafer 16 with a first side 161 and a second side 162, the wafer 16 consisting of a SOI device layer 20, a SOI handle layer 22, and buried oxide 24. The SOI wafer is first oxidized to form a protective thermal oxide layer 48 on the top and bottom sides 161, 162. Referring to Figure 14, the electrical SOI Shunts 34 on the MEMS 16 are formed next, between the SOI Device layer 20 and the SOI Handle layer 22 through the Buried Oxide 24. Trenches 28 are patterned in the desired spots to form conducting shunts, and are etched through the SOI device layer 20 and buried oxide 24 to or slightly into the SOI handle layer 22. Referring to Figure 15, these trenches 28 are then filled with a conducting material 32 which can be doped polycrystalline silicon (polysilicon), metal, or other conducting material. In this way an electrical path 34 is formed vertically between the SOI Device and handle layers 20, 22 at desired spots.

Referring to Figure 16, next the polysilicon or other conductor and protective oxide are etched off the SOI device layer 20. The desired MEMS structures including leads 36 and feedthroughs 25 are patterned, delimited by trenches 28 in the SOI device layer 20. In the case of an inertial sensor, the top portion of the proof mass will be delineated during this step.

Referring to Figure 17, the inner side 121 of the top cap wafer 12 is then aligned and bonded to the SOI Device layer 20 on the first side 161 of the MEMS wafer 16. The feedthrough pads 28 on the SOI Device layer 20 are aligned to the corresponding pads on the top cap wafer 12 and the electrodes 13 on the top cap 12 are aligned to the relevant electrodes 19 on the MEMS wafer 16. The wafer bonding process used should be one that provides a conductive bond such as fusion bonding, gold thermocompression bonding, or gold-silicon eutectic bonding.

Referring to Figure 18, once bonded to the top cap 12, second portions of the MEMS structure are patterned on the second side 162 of the MEMS wafer 16. As shown, the conducting polysilicon and protective thermal oxide are etched off of the second side 162 of the MEMS wafer 16 in the SOI handle layer 22. The SOI handle layer 22 is next patterned with additional MEMS structures (i.e. a proof mass 17 in the case of an inertial sensor) and feedthrough 19. Trenches etched around the feedthrough 19 isolate it from the rest of the layer. If the feedthrough is attached to a SOI Shunt on the Device layer, then it becomes an isolated electrical feedthrough. If it is not attached to a Silicon Via, the feedthrough becomes merely a mechanical support. In the case of an inertial sensor, at least one conducting channel or pathway preferably extends from the proof mass 17, through the flexural springs 27, and through the top or bottom cap, and is eventually connected to a bond pad.

Referring to Figure 19, the inner side 141 of the bottom cap wafer 14 is next bonded to the SOI handle layer 22 on the second side 162 of the MEMS wafer 16. Again a wafer bonding method such as fusion bonding, gold thermocompression bonding, or gold-silicon eutectic bonding should be used to provide electrical contact between the feedthroughs 19 in the MEMS wafer. In this manner, a conductive path is provided from the bottom electrodes through the bottom cap, handle feedthroughs, silicon vias, and SOI device layer to the top cap.

At this point the MEMS 16 is hermetically sealed between the cap wafers 12, 14 and aligned with the top cap and bottom cap. Because the insulating channels do not yet fully penetrate the caps, the electrodes on each cap are shorted together
5 through the remaining silicon. Referring to Figure 20, one cap wafer, here the top cap 12, is then ground and polished to expose the insulating trenches 28. The electrodes are thus electrically isolated except for the connections to the top cap bond pads through the feedthroughs and silicon vias. As can be appreciated, the feedthroughs and conducting shunts allow the bond pads on the top cap to be
10 electrically connected to the bottom cap and/or to the MEMS structure in the MEMS wafer.

Referring to Figure 21, the ground and polished cap is passivated with an insulating oxide layer 40 to protect it. Next, contacts 42 are opened in the top cap
15 12 and metallization 41 is applied. Referring to Figure 22, any electrical leads 36 and bond pads 23 are patterned in the metallization. In this way, the electrical connections from the top and bottom of the MEMS are accessible from the top for wire bonding, flip chip bonding, or wafer bonding.

Referring to Figure 23, a thick passivation layer 45 is deposited over the bond pads 23, and leads 36 to protect them. The wafer can then be inverted and the grind, polish and cap insulating layer 40 deposition processes are repeated on the other cap wafer, here the bottom cap 14. If electrical access to the MEMS is to be made only through the top of the MEMS chip, then bottom cap processing
25 is complete. In this case contacts 42 are opened in the thick passivation layer 45 over the bond pads 23 on the top cap 12 as shown in Figure 24. The MEMS wafer is now ready for dicing or wafer bonding to the IC wafer.

Referring to Figure 25, alternatively, if full insulated conducting pathways extending from the top cap 12 to the bottom cap 14 are desired, also referred as
30 "3D Through-Chip-Vias (3DTCVs) then after deposition of the thick passivating

layer 45 on the top cap 12, the steps of creating contacts 43 in the bottom cap insulation 40, depositing and patterning bottom cap bond pads 23, and depositing a thick passivation layer 45 are repeated on the bottom cap 14. Then openings can be made in the passivating layers 45 on both the top 12 and bottom 14 caps as shown in Figure 26. This completes wafer level fabrication of the hermetically sealed MEMS IMU sensor. At this point the electrical connections from the top, sides, and bottom of the MEMS are accessible from the top or bottom for dicing, wire bonding, flip chip bonding, or wafer bonding.

If anti-stiction bumps are not required, the cap process flow can be simplified with a single thicker gap oxidation as shown in Figure 27. The thin thermal oxide 48 and non-oxidizing 49 films are deposited as described earlier and etched to delineate the capacitor recess. Then a thick thermal oxide 50 is grown whose thickness is chosen to consume an amount of silicon appropriate for the capacitor gap width, typically 1 μm to 5 μm . Referring to Figure 28, the non-oxidizing film and thin and thick oxide films are stripped leaving a cap wafer 12 with a recess 38 of the desired depth etched into it. Referring to Figure 29, the process flow continues as described earlier resulting in a MEMS IMU sensor as before, without anti-stiction bumps, but with well-defined capacitor gaps 39.

If it is necessary only to bring signals out through the top of the MEMS IMU, an alternative approach can be used to fabricate the bottom cap. In this case, the trench etch, fill, and polish process for the bottom cap can be replaced by using an SOI (Silicon-On-Insulator) wafer for the bottom cap. Referring to Figure 30, the recess 38 and anti-stiction bump 47 processes are carried out on an SOI wafer 14 instead of a standard wafer. In this case the trench pattern 28 delineating the bottom cap electrodes 15 is etched down to the buried oxide 24. No fill or backside grind and polish are required since the electrodes 15 are isolated by the trenches 28 and the buried oxide 24. The SOI bottom cap can then be bonded to the MEMS 16 and top cap 12 combination as shown in Figure 31. Referring to Figure 32, processing of the top cap 12 proceeds as described

earlier. Of course, it is also possible to form the top cap with a SOI wafer, and to transmit the signals through the bottom cap instead.

5 The figures illustrate only an exemplary embodiment of the invention and are, therefore, not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments. The scope of the claims should not be limited by the preferred embodiments set forth in the examples, but should be given the broadest interpretation consistent with the description as a whole.

CLAIMS

1. A method for manufacturing a three dimensional MEMS sensor, the method comprising the steps of:

5 forming at least one recess on an inner side of a silicon-based first cap wafer by growing thermal oxide films to consume a portion of silicon in the first cap wafer;

 patterning trenches to form electrodes on the inner side of the first cap wafer;

10 patterning first portions of a MEMS structure in a first side of a MEMS wafer;

 bonding said first side of the patterned MEMS wafer to the inner side of the first cap wafer with the at least one recess facing the MEMS structure to form at least one capacitance gap, the electrodes of the first cap wafer being located over the MEMS structure and forming a capacitor therewith;

15 patterning second portions of the MEMS structure on a second side of the MEMS wafer;

 further bonding the second side of the patterned MEMS wafer to an inner side of a silicon-based second cap wafer; and

20 removing a portion of an outer side of the first cap wafer to isolate the electrodes of the first cap wafer.

2. The method according to claim 1, wherein the thermal oxide films comprise first and second thermal oxide films, and wherein forming at least one recess comprises the steps of:

25 growing the first thermal oxide film on the inner side of the first cap wafer;

 depositing a first non-oxidizing film on the inner side of the first cap wafer on top of the first thermal oxide film;

30 etching the first non-oxidizing film to create exposed areas at locations along the inner side of the first cap wafer where the at least one recess is to be located;

growing the second thermal oxide film in the exposed areas; and
removing the first non-oxidizing film and the first and second
thermal oxide films, thereby leaving the at least one recess in the first cap
wafer.

5

3. The method according to claim 2, wherein the step of forming at least one
recess further comprises the substep of etching the first thermal oxide film
in the exposed areas prior to growing the second thermal oxide film.

10

4. The method according to claim 3, wherein the step of etching the first
thermal oxide film in the exposed area comprises a wet etch process.

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5. The method according to claims 2 or 3, wherein the steps of removing the
first non-oxidizing film, and the first and second thermal oxide films
comprise wet etch processes.

20

6. The method according to any one of claims 2 to 5, further comprising a
step of forming at least one recess in the second cap wafer by growing at
least some of the thermal oxide films to consume a portion of silicon in the
second cap wafer.

25

7. The method according to any one of claims 2 to 6 wherein the second
thermal oxide film is grown to a thickness greater than a thickness of the
first thermal oxide film.

30

8. The method according to claim 7, wherein the thickness of the second
thermal oxide film is between 10 and 100 times the thickness of the first
thermal oxide film.

9. The method according to claims 7 or 8, wherein the first thermal oxide film
is grown to a thickness between 10 nm and 100 nm.

10. The method according to any one of claims 7 to 9, wherein the second thermal oxide film is grown to a thickness between 1 and 3 μm .

11. The method according to any one of claims 2 to 10, further comprising the step of forming at least one anti-stiction bump in the at least one recess in the first cap wafer.

12. The method according to claim 11, wherein forming the at least one anti-stiction bump in the at least one recess in the first cap wafer comprises growing the thermal oxide films to consume the portion of the silicon in the first cap wafer in a two-step oxidation process.

13. The method according to claim 12, wherein the thermal oxide films further comprise third and fourth thermal oxide films, and wherein the two-step oxidation process comprises a first step comprising the substeps of:

growing the first thermal oxide film on the inner side of the first cap wafer;

depositing the first non-oxidizing film on the inner side of the first cap wafer on top of the first thermal oxide film;

etching the first non-oxidizing film to create the exposed areas, while also leaving covered areas at locations along the inner side of the first cap wafer where the at least one anti-stiction bump is to be located;

growing the second thermal oxide film in the exposed areas;

removing the first non-oxidizing film and the first and second thermal oxide films, thereby leaving behind the at least one recess and the at least one anti-stiction bump; and

a second step comprising the substeps of:

growing the third thermal oxide film on the inner side of the first cap wafer;

depositing a second non-oxidizing film on the inner side of the first cap wafer on top of the third thermal oxide film;

etching the second non-oxidizing film to expose the at least one recess and the at least one anti-stiction bump;

growing the fourth thermal oxide film on the exposed at least one recess and the exposed at least one anti-stiction bump;

5 removing the second non-oxidizing film and the third and fourth thermal oxidizing films, thereby leaving behind the at least one recess and the at least one anti-stiction bump in the at least one recess.

10 14. The method according to claim 13, wherein the second thermal oxide film is grown to a first depth t_1 and the fourth thermal oxide film is grown to a second depth t_2 , thereby resulting in the at least one recess having a thickness t_1+t_2 and the at least one anti-stiction bump having a height t_1 measured from a bottom of the recess.

15 15. The method according to claim 14, wherein the depth t_1 is different than the depth t_2 .

16. The method according to claim 15, wherein the depth t_2 is greater than the depth t_1 .

20 17. The method according to any one of claims 14 to 16, wherein growing the second and fourth thermal oxide films comprises forcing an oxidizing agent to diffuse into the first cap wafer at predetermined temperatures for predetermined periods of time, said predetermined temperatures and periods of time respectively corresponding to temperatures and times
25 required to grow thermal oxide film in the silicon-based first cap wafer to depths t_1 and t_2 , respectively.

30 18. The method according to any one of claims 1 to 17, wherein the first cap wafer comprises a single-layer silicon wafer, and the step of patterning the

electrodes comprises etching closed-loop trenches on the inner side of the first cap wafer along the at least one recess, and filling or lining said trenches with an insulated material to electrically insulate the electrodes from the remainder of the first cap wafer.

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19. The method according to claim 18, wherein the trenches are etched in the first cap wafer to a depth approximately equal to the final first cap thickness.

10

20. The method according to any one of claims 1 to 17, wherein the first cap wafer comprises a first SOI wafer.

21. The method according to any one of claims 1 to 20, further comprising the step of patterning trenches to form electrodes on the inner side of the second cap wafer.

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22. The method according to claim 21, wherein the second cap wafer comprises a second SOI wafer, and the step of forming the electrodes in the second cap wafer comprises the substeps of etching, down to a buried oxide layer, closed-loop trenches on the inner side of the second cap wafer along the at least one recess, the trenches and buried oxide layer together electrically insulating the electrodes from the remainder of the second cap wafer.

20

23. The method according to claims 21 or 22, further comprising a step of forming at least first and second electrical contacts on the outer side of the first cap wafer, the first electrical contact being electrically connected to at least one of the electrode in the first cap wafer and the second electrical contact being electrically connected to at least one of the electrodes in the second cap wafer via insulated conducting channels extending from within the second cap wafer, through the MEMS wafer and through the first cap wafer.

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30

24. The method according to any one of claims 21 to 23, further comprising a step of forming electrical contacts on an outer side of the second cap wafer, said electrical contacts on the outer side of the second cap wafer being electrically connected to the electrodes of the second cap wafer.

25. The method according to any one of claims 1 to 22, further comprising a step of forming at least first and second electrical contacts on the outer side of the first cap wafer, the first electrical contact being electrically connected to at least one of the electrodes of the first cap wafer and the second electrical contact being electrically connected to the MEMS structure via insulated conducting channels extending from within the MEMS wafer and through the first cap wafer.

26. The method according to any one of claims 1 to 23, wherein the MEMS wafer comprises a third SOI wafer with a handle layer and a device layer, the first side of the MEMS wafer comprising the handle layer and the second side of the MEMS wafer comprising the device layer, and wherein the MEMS structure comprises a flexible element patterned in the device layer.

27. The method according to claim 26, wherein the MEMS sensor comprises an inertial sensor, the MEMS structure is a resonant structure, the flexible element comprises springs suspending the resonant structure, and wherein the steps of patterning the first and second portions of the MEMS structure comprise patterning portions of the resonant structure and spring in the device layer of the MEMS wafer, and patterning remaining portions of the resonant structure and the spring in the handle layer of the MEMS wafer.

28. The method according to claim 27, wherein the resonant structure is a proof mass.

29. The method according to any one of claims 1 to 28, wherein the first and second cap wafers are bonded using a conductive bond.

5 30. The method according to any one of claim 1 to 29, wherein in bonding the first and second cap wafer to the MEMS wafer comprises hermetically sealing the MEMS structure between the first and second cap wafers.

10 31. The method according to any one of claims 1 to 30, wherein the step of growing the thermal oxide film to consume a portion of the silicon on the inner side of the first cap wafer is performed simultaneously on a plurality of wafers.

15 32. The method according to claim 31, wherein the plurality of wafers is between 25 and 200.

20 33. The method according to claims 31 or 32, wherein a variation between depths of the recesses formed in each of the plurality of wafers is less than 5%.

34. A three dimensional MEMS sensor manufactured by the method according to any one of claims 1 to 33.

35. A three dimensional (3D) MEMS sensor comprising:

25 an electrically conductive MEMS wafer including a MEMS structure, the MEMS wafer having a first side and a second side;

a silicon-based top cap having an inner top cap side and an outer top cap side, the inner top cap side having at least one recess formed by oxidation of a portion of the silicon of the top cap, the at least one recess facing the MEMS structure to form at least one capacitance gap, the top cap having electrodes patterned in the inner top cap side, the inner top cap side being bonded to the first side of the MEMS wafer, the electrodes of the top cap being located over the MEMS structure and forming a

30

capacitor therewith across the capacitance gap, the outer top cap side having electrical contacts on or over the electrically conductive top cap wafer,

a silicon-based bottom cap having an inner bottom cap side and an outer bottom cap side, the bottom cap wafer being bonded to the second side of the MEMS wafer such that the MEMS wafer, the top cap wafer and the bottom cap wafer define a cavity for housing the MEMS structure; and

first and second electrical contacts formed on at least the top cap wafer, connected to the electrodes of the first cap wafer and to the MEMS structure.

36. The three dimensional (3D) MEMS sensor according to claim 35, further comprising at least one anti-stiction bump formed by oxidation in the at least one recess of the top cap.

37. The three dimensional (3D) MEMS sensor according to claim 36, wherein the at least one anti-stiction bump extends in the recess below a height thereof.

38. The three dimensional (3D) MEMS sensor according to claim 37, wherein a height of the at least one anti-stiction bump is less than half of the height of the recess.

39. The three dimensional (3D) MEMS sensor according to any one of claims 34 to 38, wherein the inner bottom cap side has at least one recess formed by oxidation of a portion of the silicon of the bottom cap.

40. The three dimensional (3D) MEMS sensor according to claim 39, wherein the at least one recess in the bottom cap faces the MEMS structure to form at least one capacitance gap, the bottom cap having electrodes patterned in the inner bottom cap side, the electrodes of the bottom cap being located under the MEMS structure and forming a capacitor therewith

across the capacitance gap, the outer bottom cap side having electrical contacts on or over the electrically conductive bottom cap wafer.

- 5 41. The three dimensional (3D) MEMS sensor according to claims 39 or 40, further comprising at least one anti-stiction bump formed by oxidation in the at least one recess of the bottom cap.

1/13

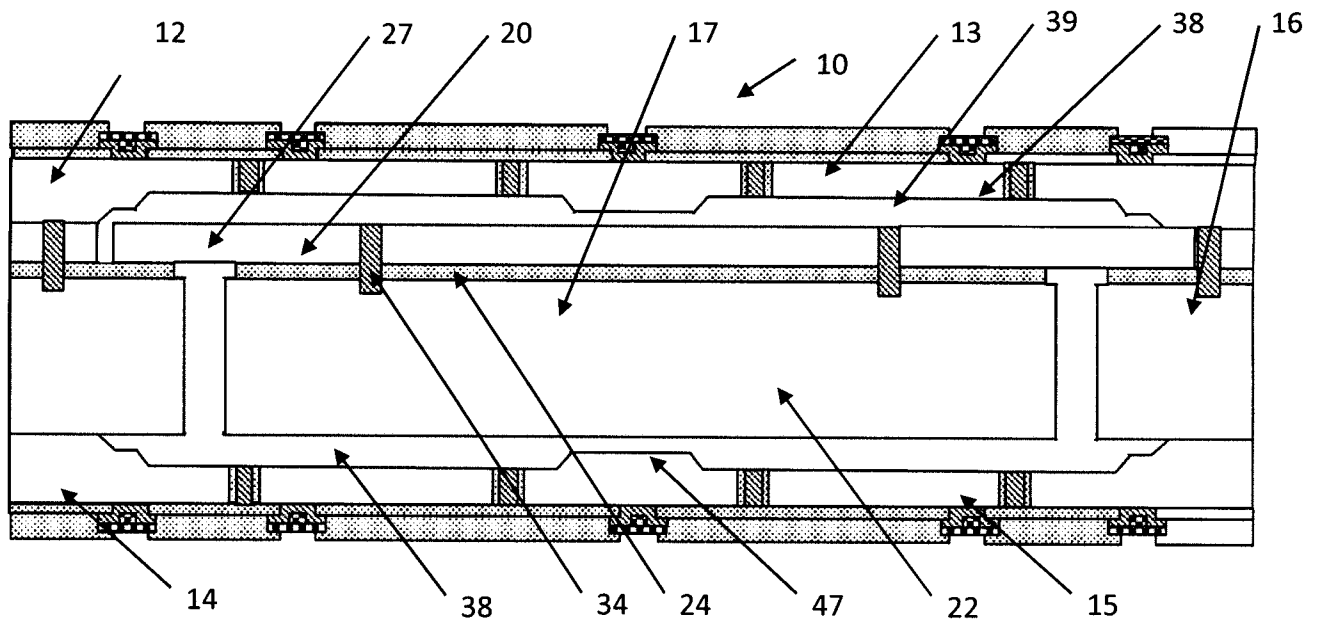


FIG. 1

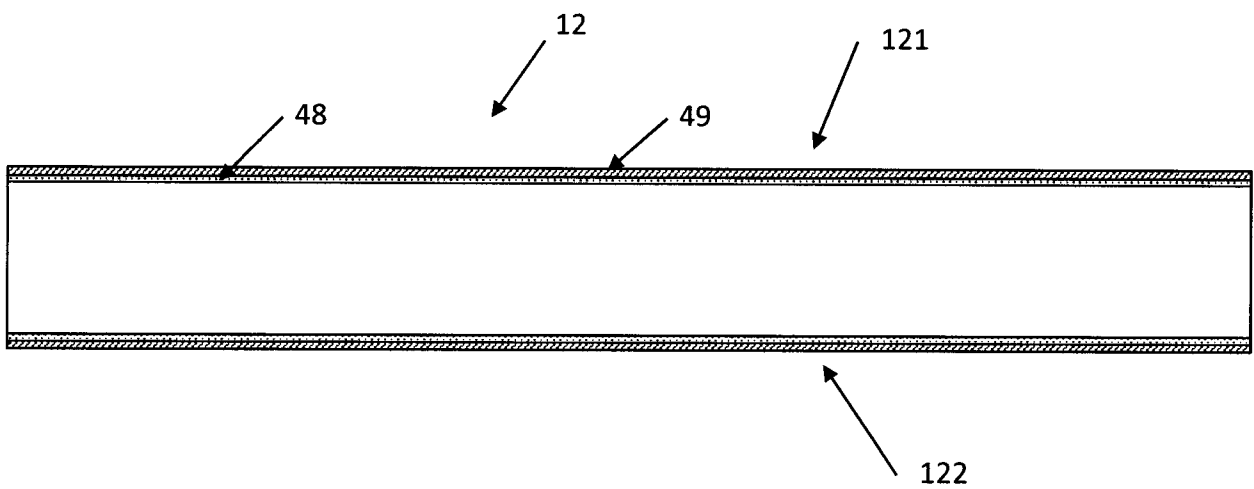


FIG. 2

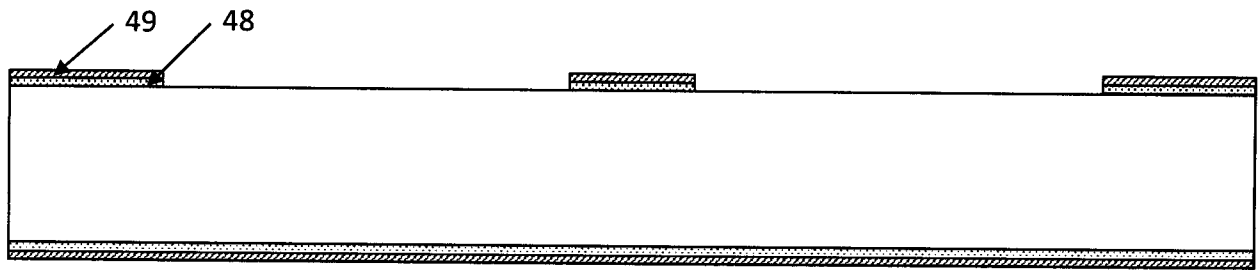


FIG. 3

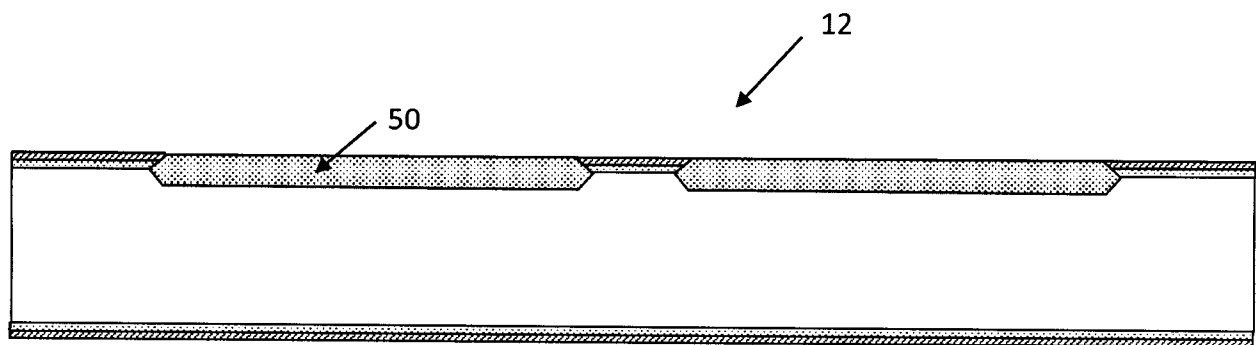


FIG. 4

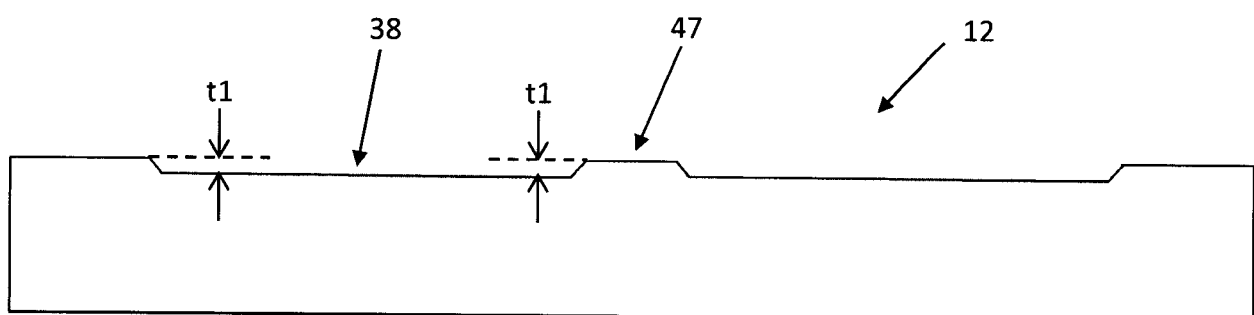


FIG. 5

3/13

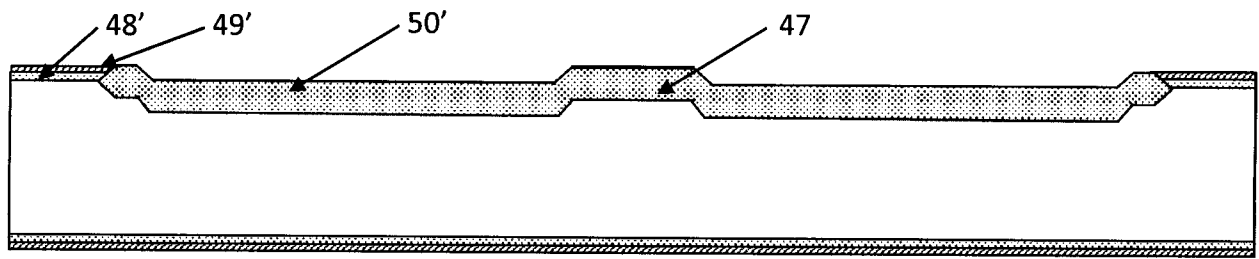


FIG. 6

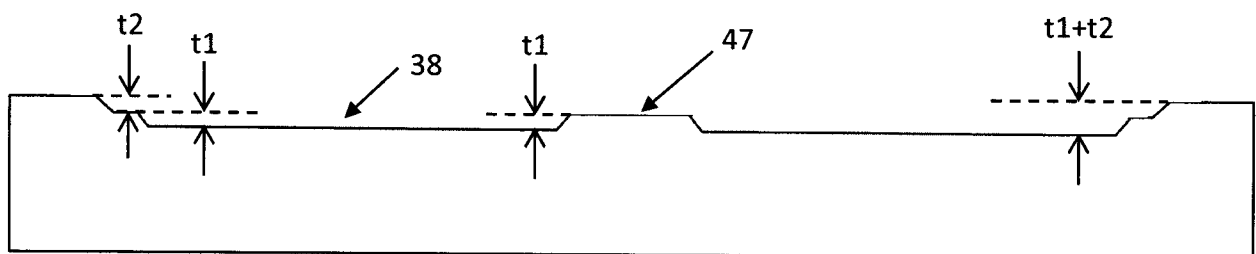


FIG. 7

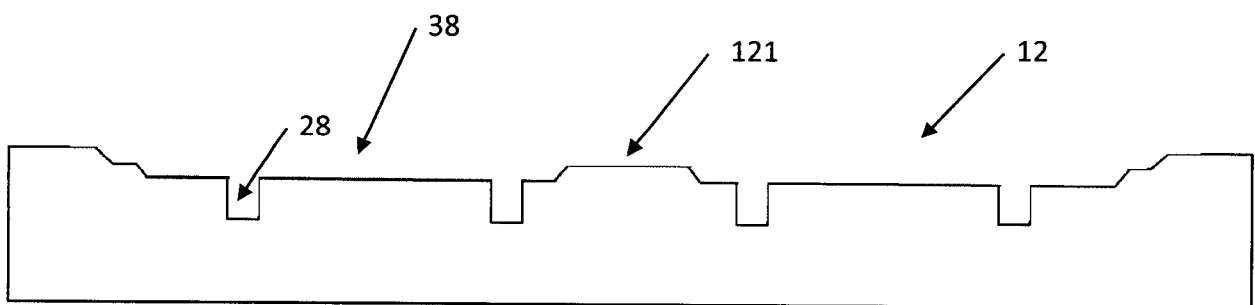


FIG. 8

4/13

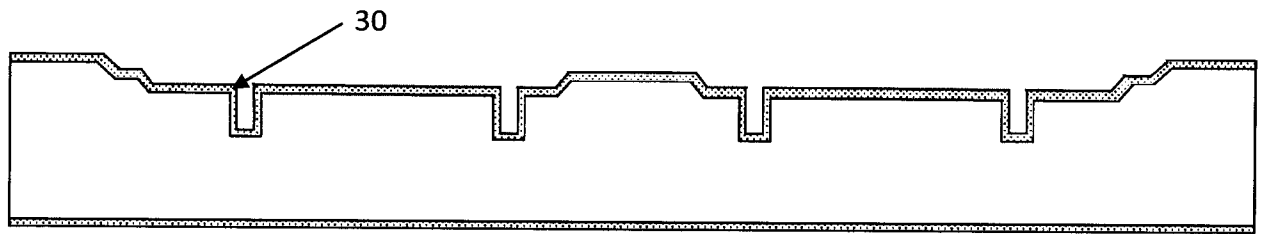


FIG. 9

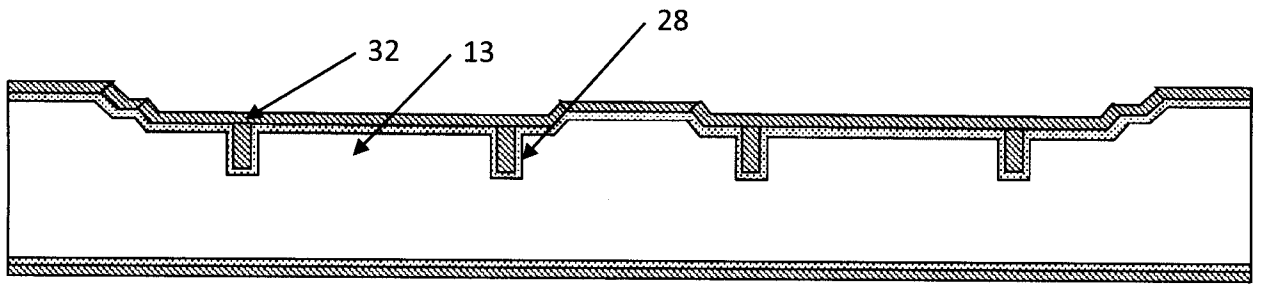


FIG. 10

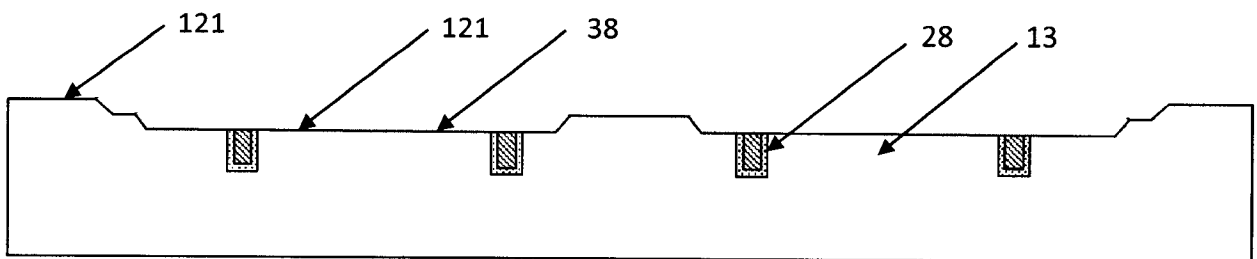


FIG. 11

5/13

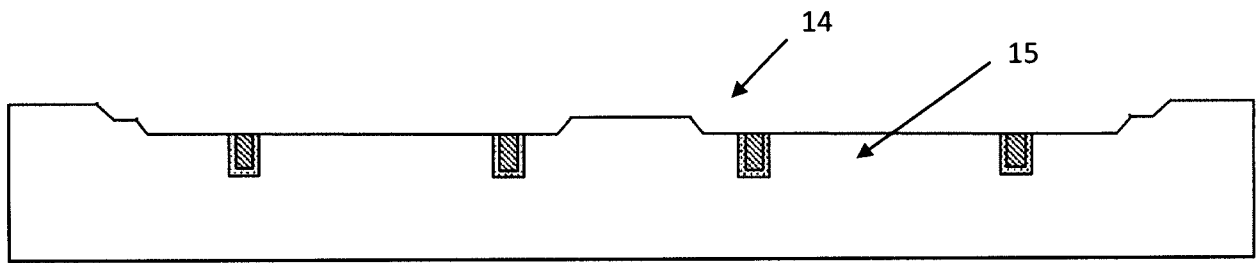


FIG. 12

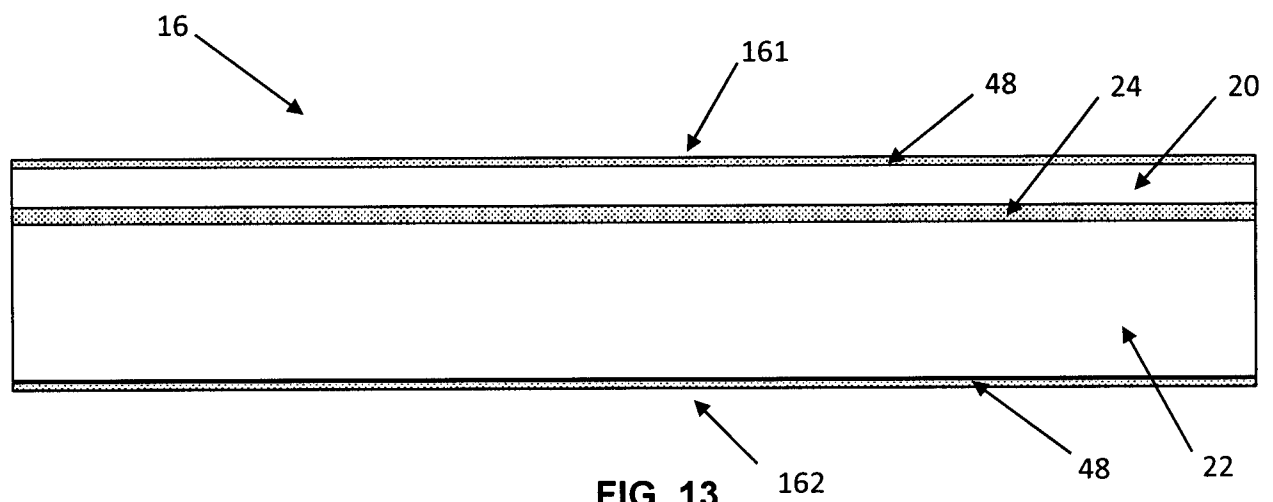


FIG. 13

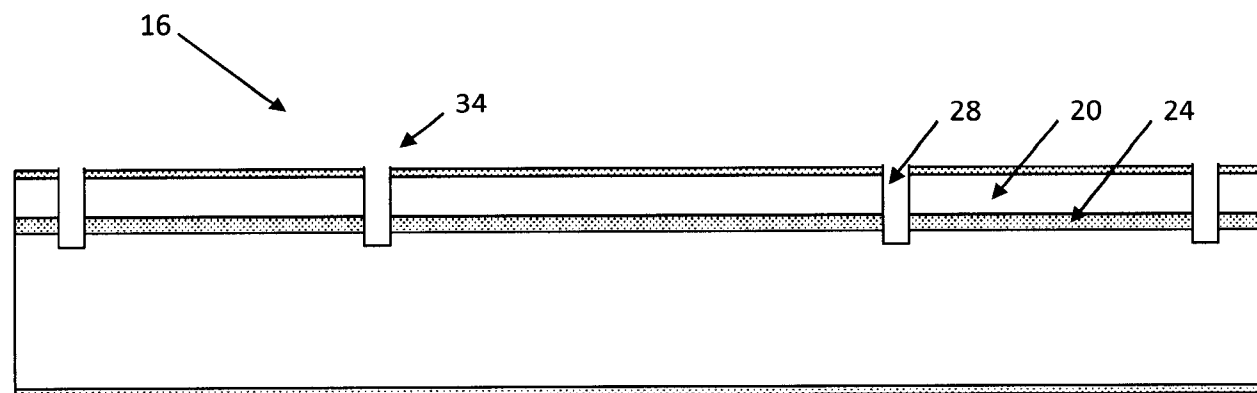


FIG. 14

6/13

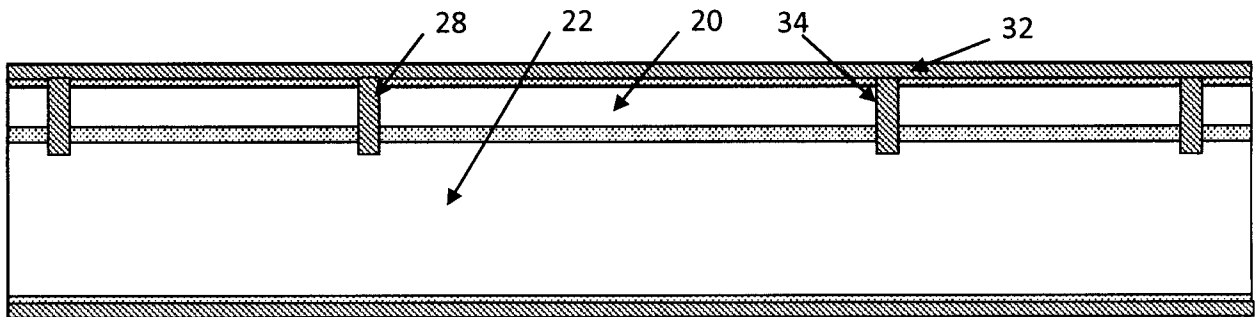


FIG. 15

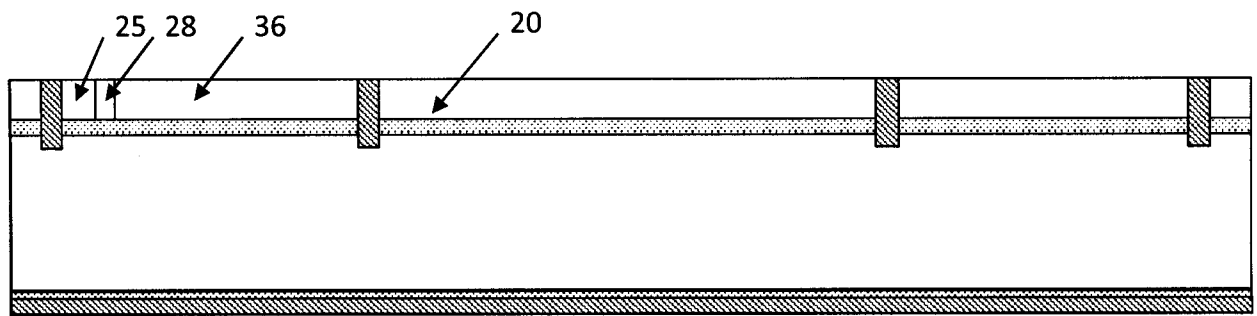


FIG. 16

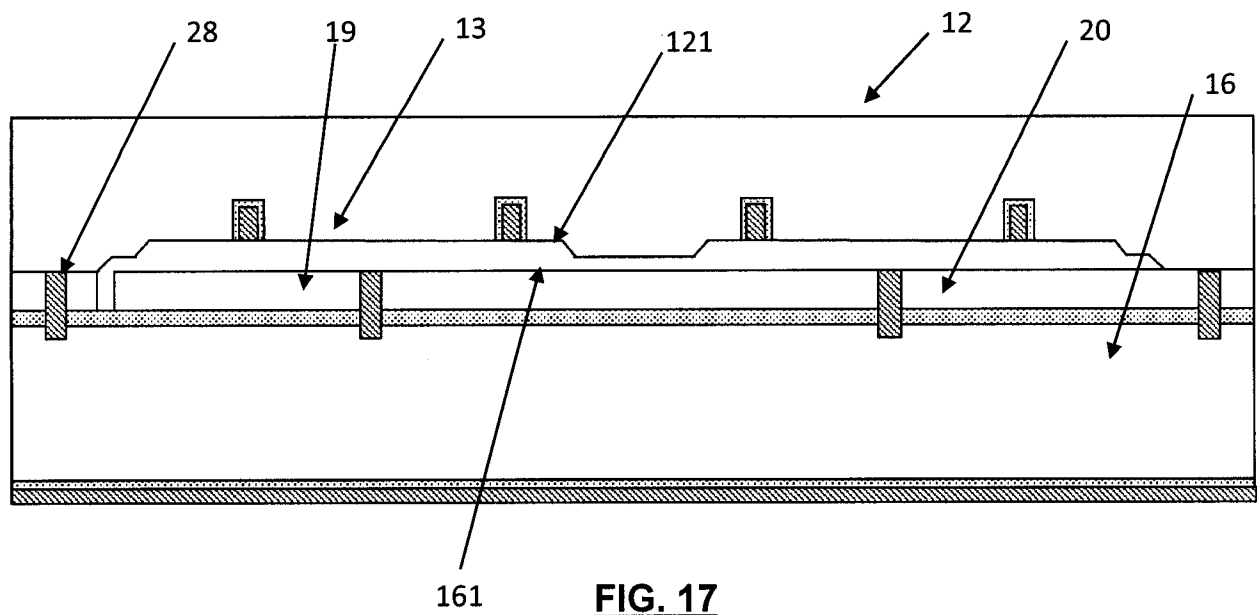


FIG. 17

7/13

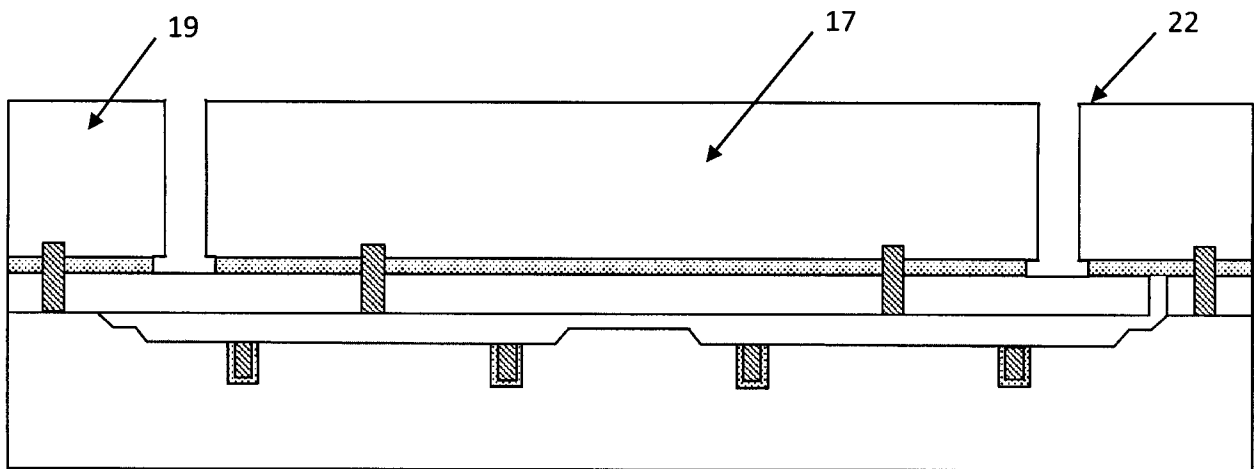


FIG. 18

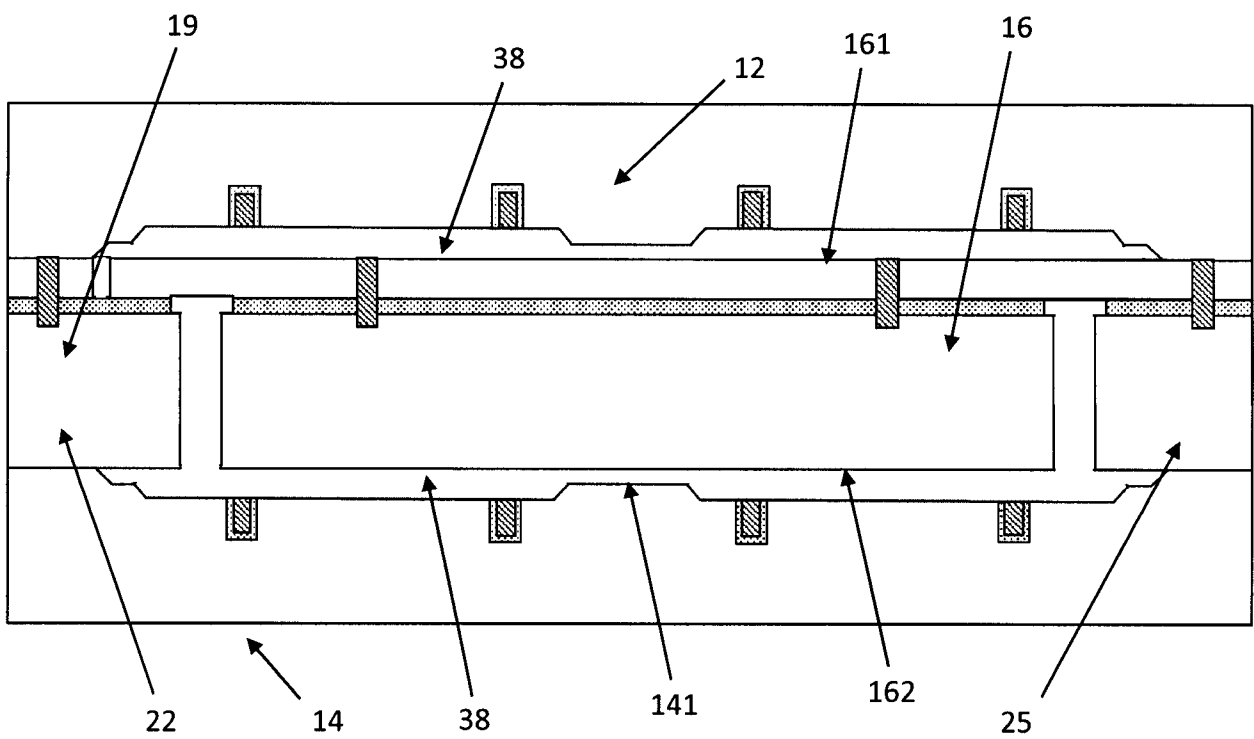


FIG. 19

8/13

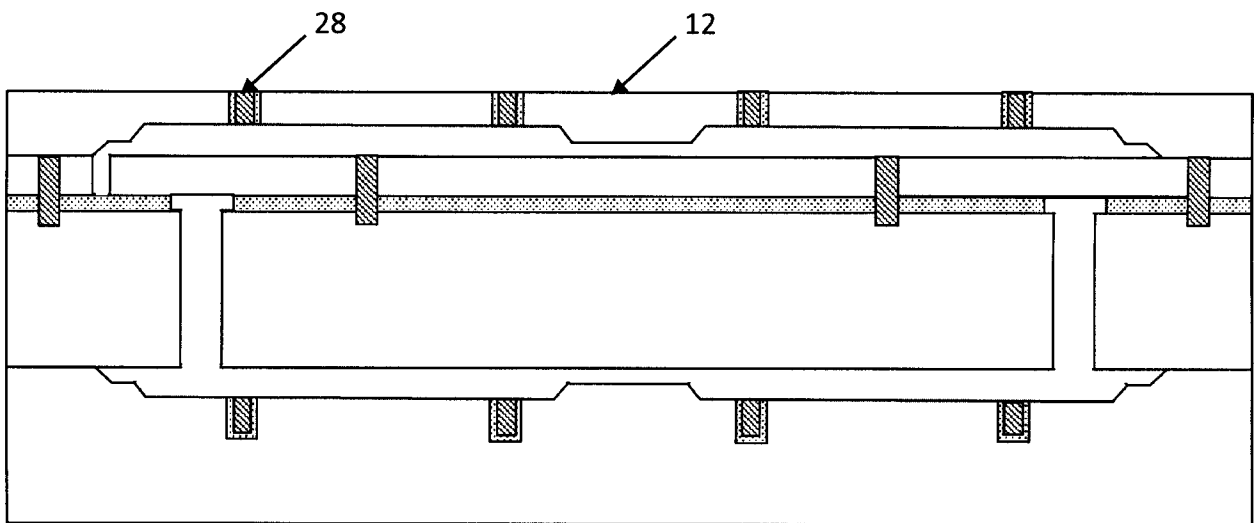


FIG. 20

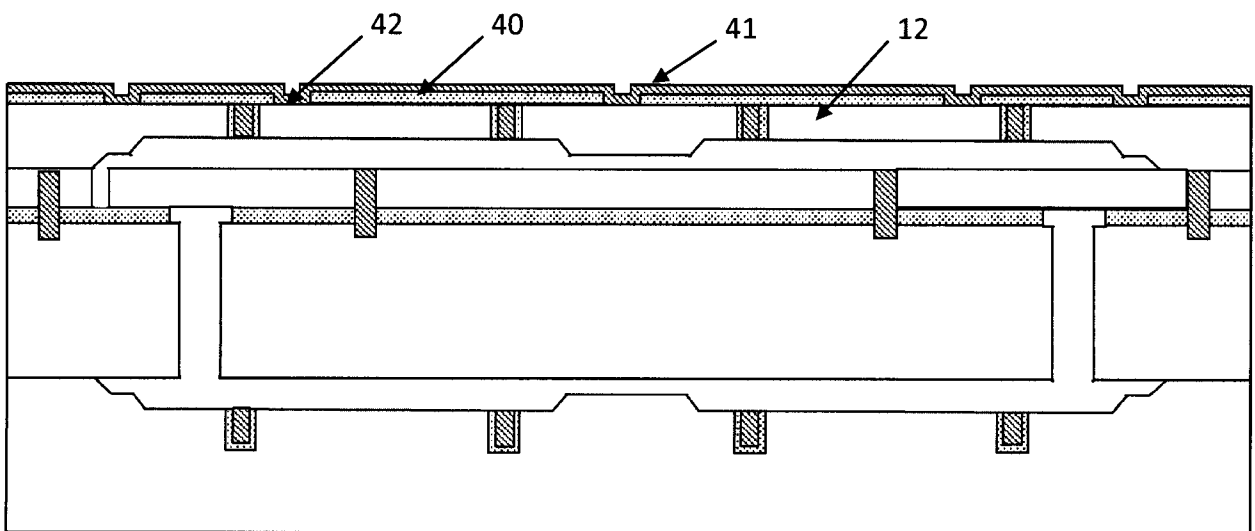


FIG. 21

9/13

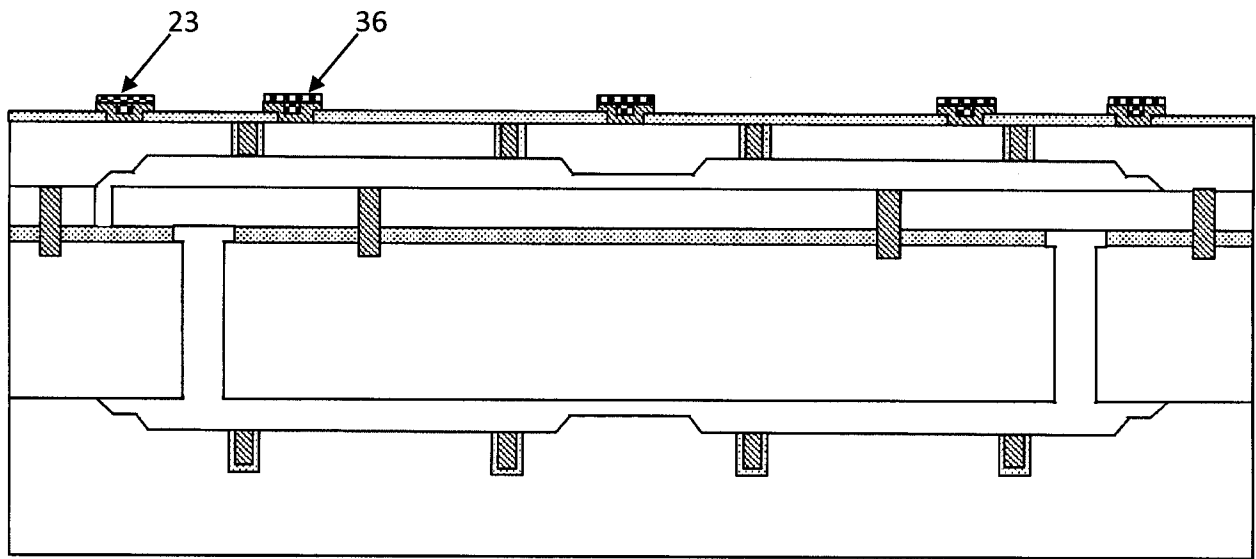


FIG. 22

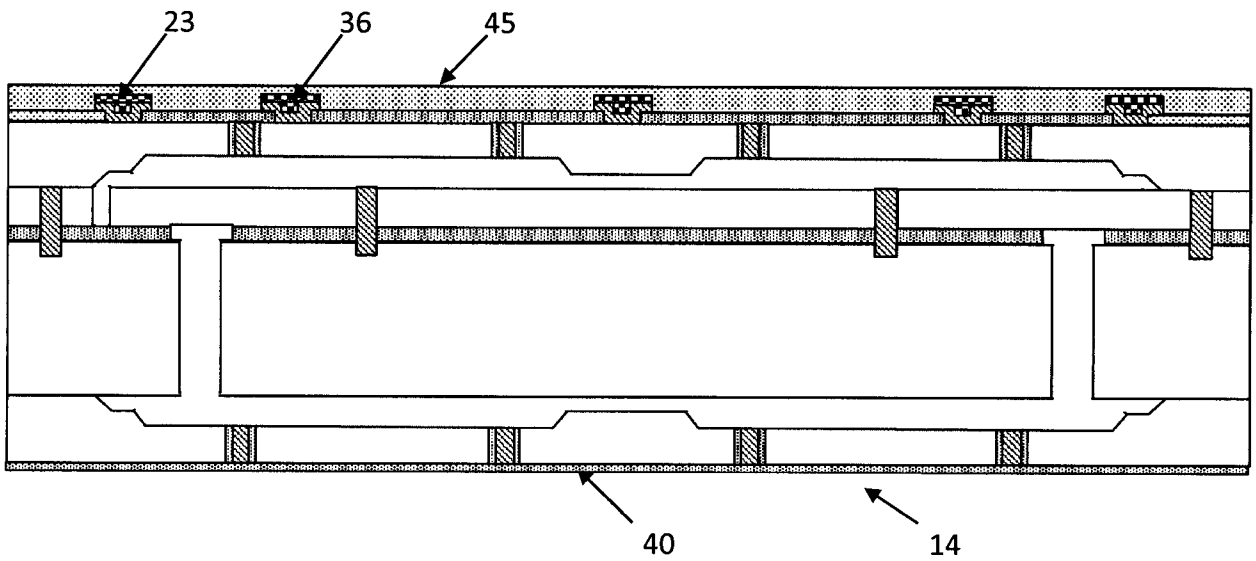


FIG. 23

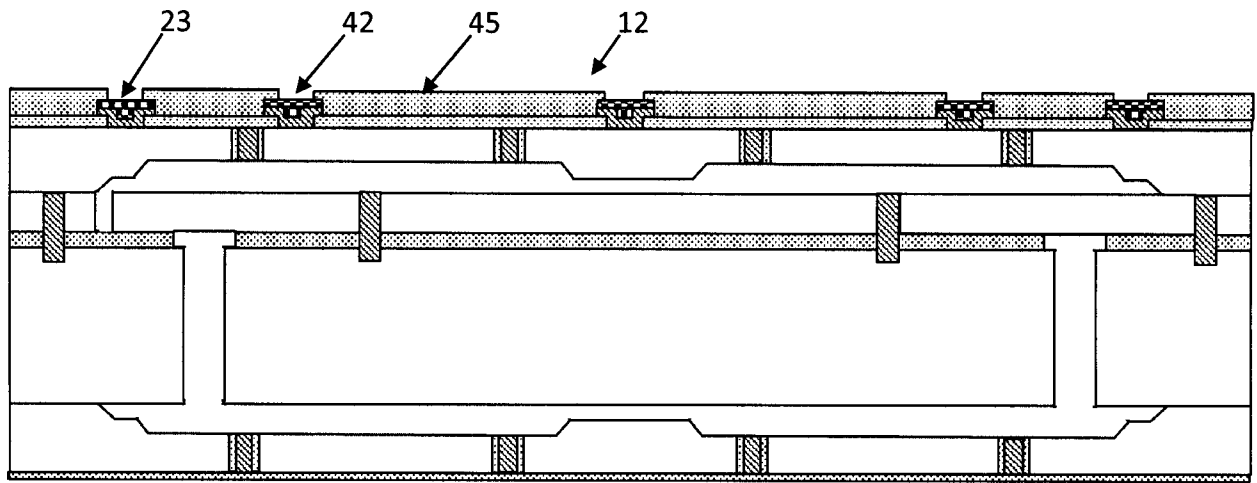


FIG. 24

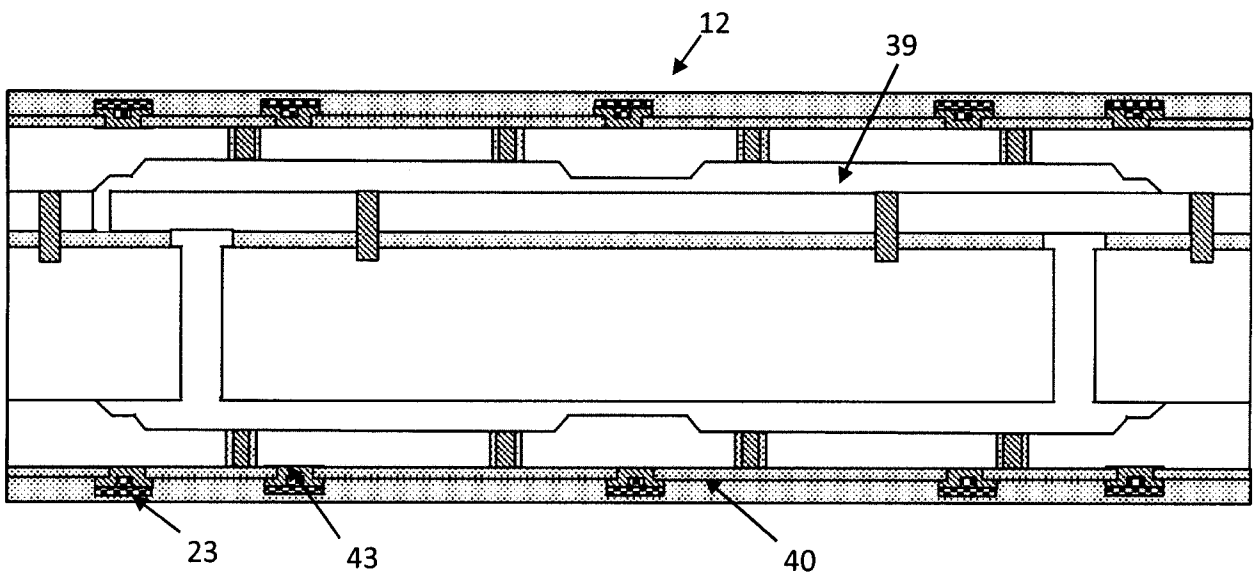


FIG. 25

11/13

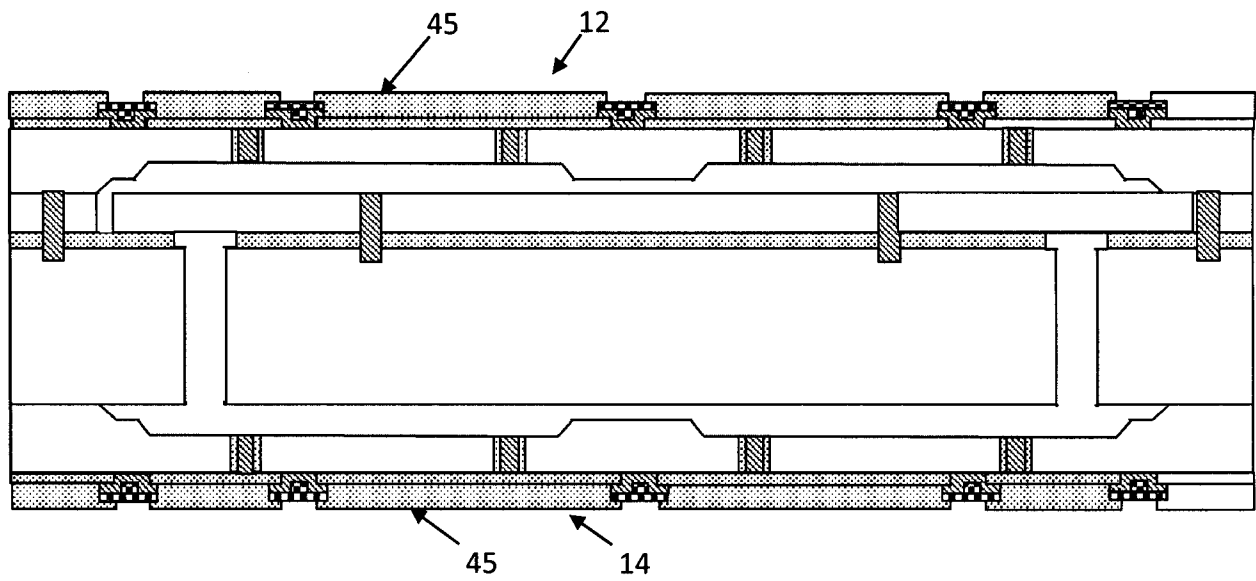


FIG. 26

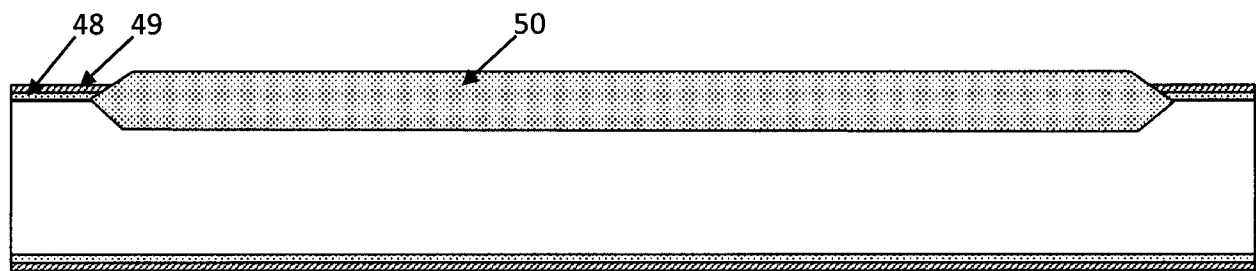


FIG. 27

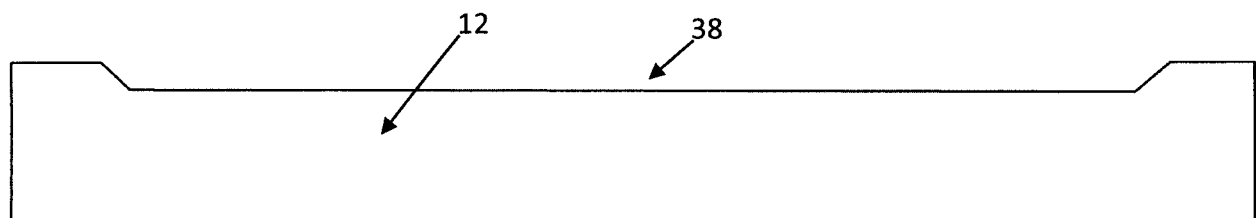


FIG. 28

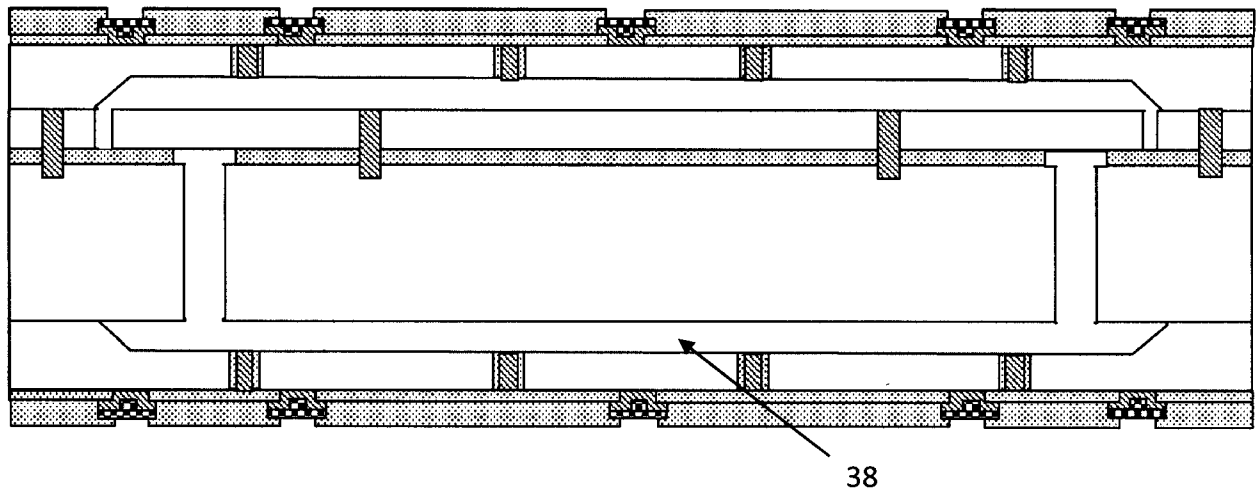


FIG. 29

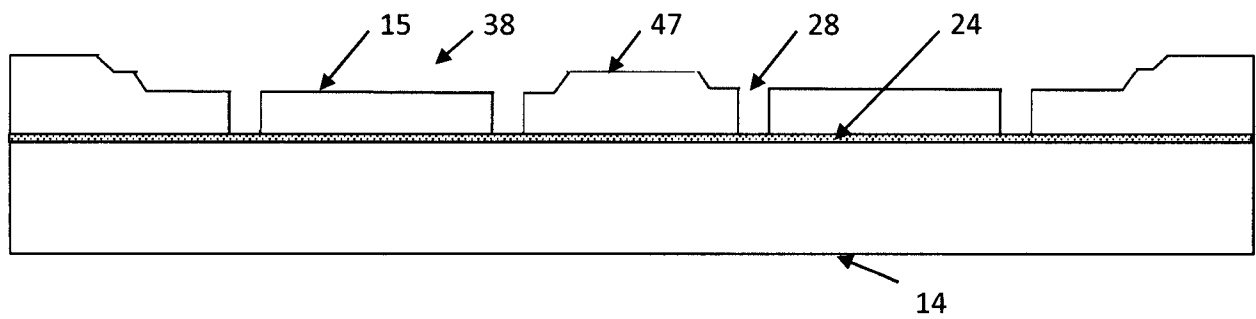


FIG. 30

13/13

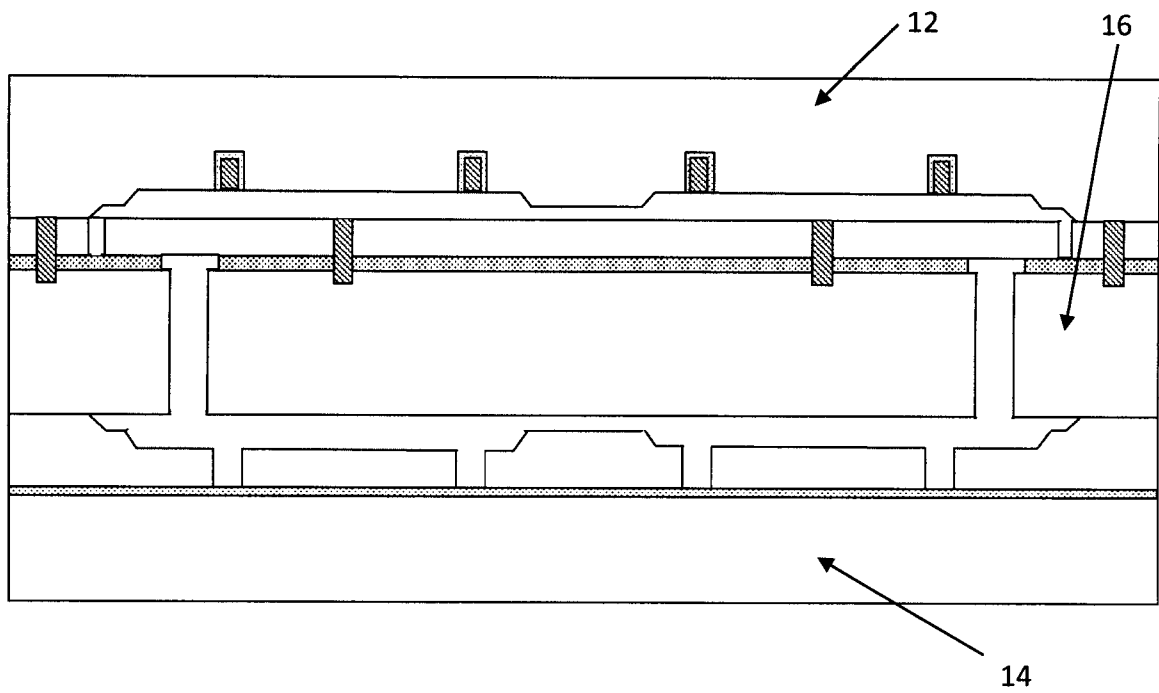


FIG. 31

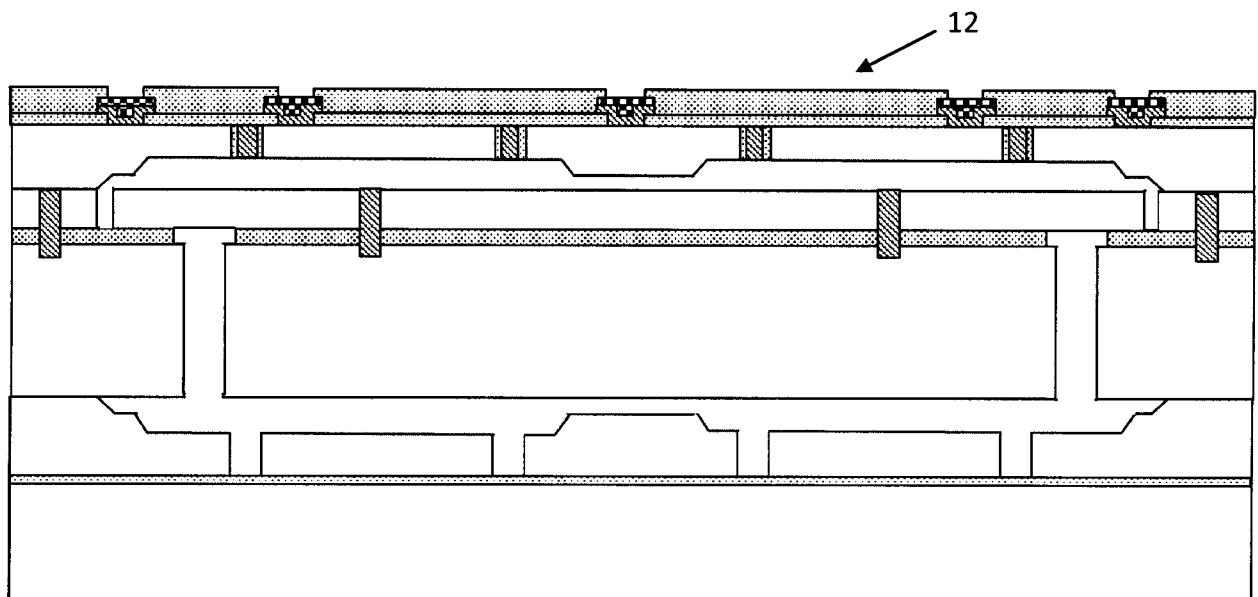


FIG. 32

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CA2015/050937

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **G01D 5/56** (2006.01), **B81B 7/02** (2006.01), **B81C 1/00** (2006.01), **G01C 19/5769** (2012.01),
G01P 15/02 (2013.01)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC (2006): G01D, B81B, B81C, G01C, G01P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

CIPO Orbit, IEEE Xplore, Google Patents, Canadian Patent Database (CIPO Intellect): MEMS, silicon, cap, wafer, recess, trench, electrode, thermal, oxide, film, oxidation, non-oxidizing, anti-stiction, bump, bond, capacitance, gap, capacitor, etch, isolate, grow, recess, inner, outer, side, exposed, area, thickness, insulate, contact, three dimensional, 3D, height and all such related terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 2015/0191345 A1 July 9, 2015 (09-07-2015)	1 to 41
X,P	WO 2015/042702 A1 April 2, 2015 (02-04-2015)	1 to 41
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A	US 7 518 493 B2 April 14, 2009 (14-04-2009)	1 to 41

 Further documents are listed in the continuation of Box C.

 See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search
 10 November 2015 (10-11-2015)

Date of mailing of the international search report
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Name and mailing address of the ISA/CA
 Canadian Intellectual Property Office
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 Gatineau, Quebec K1A 0C9
 Facsimile No.: 001-819-953-2476

Authorized officer

 Salvatore Ginese (819) 934-4888

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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